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Find the *Leonardo DRS / Catalina Research Chameleon* at our website: *Click HERE*

DRS TECHNOLOGIES

TACTICAL SYSTEMS WEST, Inc

Chameleon

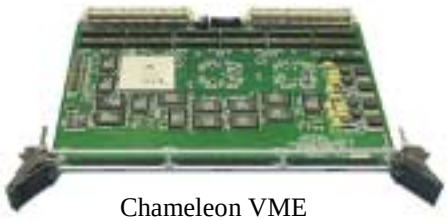
RECONFIGURABLE COMPUTING

Chameleon VME

6U VME64x
Reconfigurable Computing

Applications

- Digital filtering
- Imaging processing
- Polyphase filtering
- Pulse compression
- Radar/sonar signal processing
- SAR processing
- Signal intelligence
- Spectrum analysis

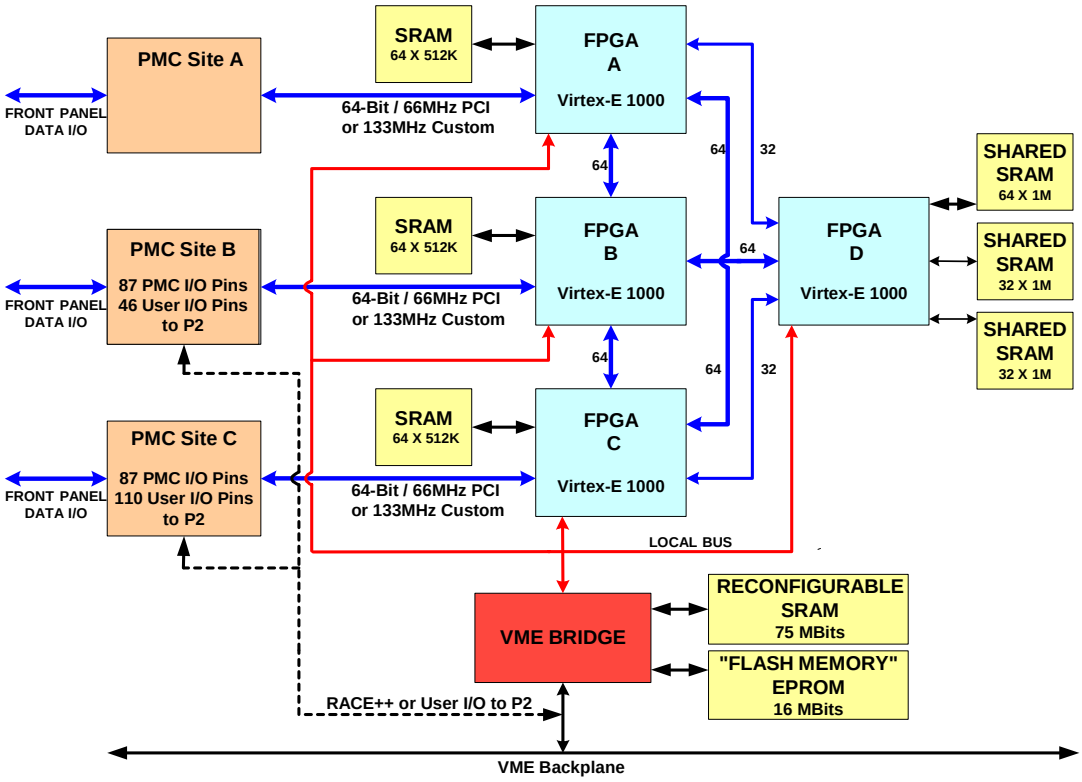


Chameleon VME

Key Features

- Three PMC daughtercard sites
- 28 Mbytes synchronous SRAM (upgradeable to 56 Mbytes)
- Four Xilinx® Virtex®-E 1000 FPGAs (upgradeable to Virtex-E 2000)
- 75 Mbits of configuration memory (upgradeable to 150 Mbits)
- Four clocks per FPGA, two user programmable up to 266 MHz; fixed clocks consist of one PCI 66/33 MHz and one local bus 66 MHz
- Supports a probe connector for an Agilent PC logic analyzer to assist with FPGA debug
- API, test and host C source code included
- Xilinx® MultiLINX™ connectors to enable Select-MAP configuration and ChipScope™ capabilities
- Xilinx® ISE ™ Development Software available directly from CRI
- Model Technology™ ModelSim®-PE suggested, ModelSim®-SE recommended

CHAMELEON-VME BLOCK DIAGRAM



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General Description

The heart of the Chameleon VME board consists of four Xilinx® Virtex®-E 1000 FPGAs, providing over four million reconfigurable system gates the user can apply to the application. Connected to FPGAs A, B, and C are independent synchronous SRAM blocks. Each bank is independent and can be used to provide large circular buffers. The FPGAs on the Chameleon VME link together in a ring with dedicated paths: A to B, B to C, and A to C. All three FPGAs also link back to D. These FPGA busses can be clocked at rates up to 133MHz.

The Chameleon VME has three high-speed I/O daughtercard sites compatible with the industry's PCI Mezzanine Card (PMC) standard. By enhancing PMC, the effort to tailor the Chameleon VME to specific I/O requirements reduce to driver integration instead of a full custom I/O daughtercard development task.

On the Chameleon VME board, FPGAs A, B, and C each have a dedicated connection to an I/O daughtercard. For PMC-based I/O applications, these links are separate 64-bit 66 MHz PCI busses. CRI provides a 'ready-to-go' PCI core. The daughtercard tied to FPGA C also contains additional connectivity to the VME64x P2 user defined pins, allowing connections to back plane interfaces such as RACE or Dual RACE++.

The Chameleon VME also supports an I/O approach where the user may elect not to use PMC as the interface protocol. For that case, the user's custom daughtercards would be PMC mechanical form factor, but the user would define the interface between the daughtercard and its respective processing element.

The VME bridge is automatically configured from an on-board EPROM at power-up. It has a full VME interface, where the control signals are decoded and translated to a local bus that is provided to the rest of the Chameleon VME resources. Through the VME, the user can read from or write to any of the FPGAs, memories, and daughtercards at standard VME bus rates. The VME is primarily used for configuration, control, and diagnostics.

Development Suite

The user defines the functionality of each FPGA through industry standard high-level tools supporting VHDL RTL-level code. The user receives a full VHDL model and test bench for the product, along with a VHDL library that allows the user to quickly develop their own custom applications. Sample applications, test benches, and test cares are also provided.

Software Support

Software drivers and API calls provide the user with the ability to control and configure the board over the host bus. They also provide a full range of diagnostics to isolate problems to the component level. VHDL netlist for the Xilinx® PCI core with DRS-TS enhancements are also included. Simulation is supported under the Model Technology™ ModelSim® environment. If required, DRS-TS is available to implement the entire board design and programming. DRS-TS also offers training classes on VHDL coding and programming of the board.

VHDL Library

Local Bus Arbiter
Local Bus Master
Local Bus Addressable Control/Status Registers
Local Bus Addressable Data Source
Local Bus Addressable Data Sink
Local Bus Addressable RAM Modules
Generic FIFO Module

Specifications

Power:
Programming dependent

PCI Signaling:
64-Bit 66 MHz at 3.3V

Processing Speed:
133 MHz clock rate

Performance:
Programming dependent

Environment:

Operating temperature:	0 - 50 degrees C
Cooling:	500 LFM minimum

Part Numbers:

CHM-VME-106-SS Chameleon 6U VME64x reconfigurable computing board; four Xilinx® Virtex®-E 1000-6 FPGAs; three 64-bit 66 MHz PMC expansion sites; 28 MB SRAM

CHM-VME-106-DS Chameleon 6U VME64x reconfigurable computing board; four Xilinx® Virtex®-E 1000-6 FPGAs; three 64-bit 66 MHz PMC expansion sites; 56 MB SRAM

CHM-VME-206-SS Chameleon 6U VME64x reconfigurable computing board; four Xilinx® Virtex®-E 2000-6 FPGAs; three 64-bit 66 MHz PMC expansion sites; 28 MB SRAM

Chameleon-VME also available with Xilinx® Virtex®-E 1000-8 FPGAs, Virtex®-E 2000-8 FPGAs, with 28 MB SRAM, with 56 MB SRAM or with ZBT RAM.

Specifications subject to change without notice. Trademarks used herein are the property of their respective companies.

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