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DS4120 ECU Interface Board

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Contains an illustration of the board, and shows the pinout of the different board connectors.

Signal Connection to External Devices....632
Shows the I/O circuits of the board and gives information on connecting the ECU.

Data Sheets....637
Summarizes the technical specifications of the hardware components.

Introduction to the Board

DS4120 Board Introduction

Board description	The DS4120 ECU Interface Board has been designed to provide the link between the customer's prototype or a production-type electronic control unit (ECU), and a PHS-bus-based system. The connection is effected via a POD (plug-on device).
Software support	The DS4120 is supported by the dSPACE software only up to dSPACE Release 6.3. As of dSPACE Release 6.4, the software no longer supports the DS4120.

DS4120 Components

Connecting external devices

Note

Before connecting external devices to the board, read the instructions provided in Connecting External Devices to the dSPACE System.

Where to go from here

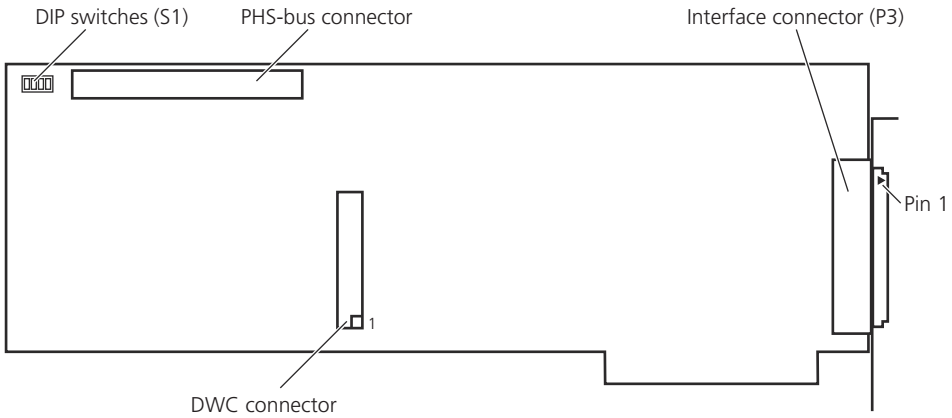
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Board Overview

Overview illustration

The illustration shows the locations of connectors and switches on the board. The illustration is not to scale.



Components

The DS4120 contains the following board elements (from left to right):

- *DIP switches (S1)* for setting the PHS-bus base address. Factory default setting: B0H (hex)/1011 (DIP switches).

  For detailed instructions, refer to How to Set the PHS-bus Address.
- *PHS-busconnector* for communication between the processor board and the I/O boards.
- *DWC connector*: Reserved for use by dSPACE.

- *Interface connector (P3)* is a 100-pin, high-density KEL connector. The signals available at this connector are described in Interface Connector (P3) on page 630.

  The shipment includes a ribbon cable with 100-pin, fine pitch connectors to match the interface connector (P3).

Interface Connector (P3)

Objective

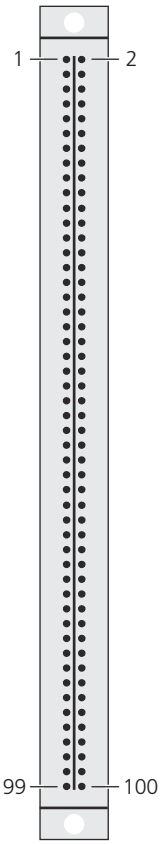
The interface connector (P3) is a 100-pin, high-density KEL connector. It is used to obtain access to the I/O signals of the board.

Location

The connector is located on the bracket of the DS4120, see Board Overview on page 629.

Pinout

The following illustration shows the numbering used (front view).

Interface Connector (P3)	Pin	Signal	Pin	Signal
	1	PODVCC (+5 V)	2	PODVCC (+5 V)
	3	ECUSENSE	4, 6 … 98, 100	GND
	5, 7 … 33, 35	A0, A1 … A14, A15		
	37	$\overline{\text{SEM}}$		
	39	$\overline{\text{CE}}$		
	41	$\overline{\text{WR}}$		
	43	$\overline{\text{OE}}$		
	45	$\overline{\text{UB}}$($\overline{\text{RDMMU}}$)		
	47	$\overline{\text{LB}}$($\overline{\text{WRMMU}}$)		
	49	$\overline{\text{INTR}}$(PROGMMU)		
	51	$\overline{\text{BUSY}}$		
	53, 55 … 81, 83	D0, D1 … D14, D15		
	85	AUXIN0		
	87	AUXIN1		
	89	AUXIN2		
	91	AUXIN3		
	93	AUXOUT0		
	95	AUXOUT1		
	97	AUXOUT2		
	99	AUXOUT3		

The signal names in parenthesis apply to external DPMEM (dual-port memory) operations. For a description of the I/O signals, refer to Signal Description on page 633.

NOTICE

To prevent damage to the hardware, do not apply voltages outside the TTL voltage range (0 … 5 V) to the pins.

Note

The total load for all connector pins that provide access to PODVCC (power supply to POD) must not exceed 400 mA.

PODVCC line protection

The PODVCC line is protected against short circuits or overload by a multifuse on the DS4120. If VCC is overloaded or short-circuited to ground, the multifuse heats up due to the overcurrent and abruptly raises its resistance. To reset the multifuse to its initial low resistance, turn off the power of the expansion box for a few minutes to allow the multifuse to cool down.

Order information

Connectors matching the interface connector (P3) and cables can be ordered by the stated suppliers/manufacturers:

- IDC (insulation displacement connection) connector: 8825E-100-175 (by KEL)
- 90° PCB (printed circuit board) connector: 8800-100-170L (by KEL)
- High-density ribbon cable: 136-100 (by Thomas & Betts)

Signal Connection to External Devices

Objective

This section provides descriptions of the signal connection to the ECU, describes the signals, gives information on the on-board I/O circuits, and lists important electrical characteristics. This information is vital when connecting an ECU to the board.

Connecting external devices

Note

Before connecting external devices to the board, read the instructions provided in Connecting External Devices to the dSPACE System.

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Connection to the ECU

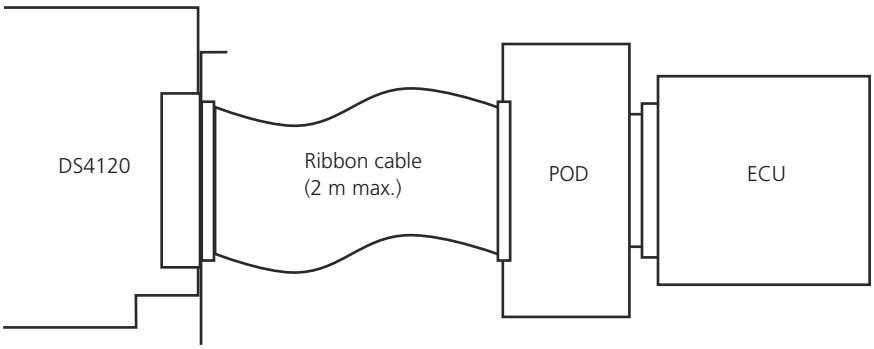
Objective

ECUs differ from manufacturer to manufacturer regarding access mechanisms, memory layouts, timing and pinout.

Each DS4120 is therefore complemented by a custom-designed plug-on device (POD) that adapts the ECU signals to the generic interface of the DS4120.

Connection example

The following illustration shows an ECU connected to the DS4120 via a POD.



Note

The ribbon cable for the link between DS4120 and POD must not exceed 2 m. Using longer cables degrades signal quality and may lead to incorrect results.

Signal Description

Descriptions

The directions (input, output) of various signal lines are different depending on the location of the DPMEM. In most cases the DPMEM on the DS4120 board is used (= onboard DPMEM), but it can also be mounted on the POD (= external DPMEM). In the latter case the DPMEM used can be selected by software.

The following table provides a description of the I/O signals available at the interface connector (P3):

Signal		Description	
A0 … A15		Address lines	Addresses refer to words, not bytes. The pins are inputs when using on-board DPMEM and outputs when using external DPMEM. (The onboard DPMEM address range is A0 … A12.)
D0 … D15		Data lines	–
AUXIN0 … AUXIN3		General purpose input lines	The lines can also be used to trigger DSP interrupts.
AUXOUT0 … AUXOUT3		General purpose output lines	–
$\overline{SEM}$	Semaphore enable	DPMEM (dual-port memory) control lines (active low)	The lines are inputs when using on-board DPMEM and outputs when using external DPMEM.
$\overline{CE}$	Chip enable		
$\overline{OE}$	Output enable		
$\overline{WE}$	Write enable		

Signal		Description	
$\overline{UB}$	Upper-byte	On-board DPMEM byte enable inputs (active low)	▪ For byte access, $\overline{CE}$ and $\overline{UB}$ or $\overline{CE}$ and $\overline{LB}$ must be low. ▪ For word access, $\overline{CE}$ and both $\overline{LB}$ and $\overline{UB}$ must be low.
$\overline{LB}$	Lower-byte		
$\overline{INTR}$		DSP to ECU interrupt output (active low)	Works only when using on-board DPMEM.
$\overline{BUSY}$		DPMEM hardware arbitration signal (active low)	▪ When using on-board DPMEM, $\overline{BUSY}$ is an output and can be used to generate wait states to the ECU processor. ▪ When using external DPMEM, $\overline{BUSY}$ is an input and generates wait states to the DSP.
$\overline{RDMMU}$		MMU programming lines	Used for programming the tag-RAM when it is installed on POD (plug-on device). Setting PROGMMU high selects the MMU program mode. This allows $\overline{RDMMU}$ and $\overline{WRMMU}$ to perform read and write accesses to tag-RAM locations addressed by A0 … A15.
$\overline{WRMMU}$			
PROGMMU			
ECUSENSE		ECU power-sense input	For details refer to ECU Power-Sense Input on page 635.

Memory Bus I/O

Objective

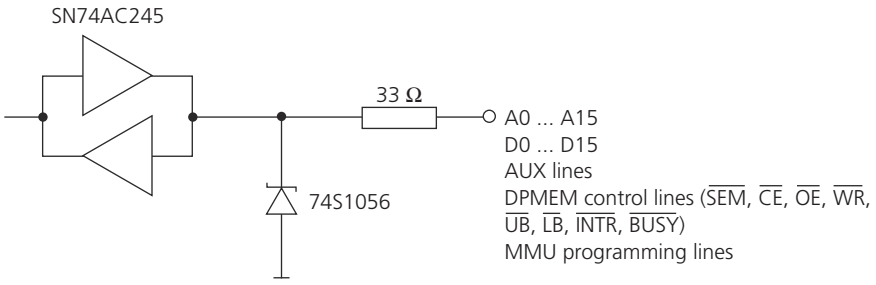
The memory bus I/O carries the signals described in Signal Description on page 633.

Features

For a feature description of the board's interface, refer to *ECU Interface Unit (DS4121 Features* 🕮*)*.

I/O circuit

The following illustration is a simplified diagram of the I/O circuitry.



Electrical characteristics

The memory bus I/O has TTL input/output levels with the following characteristics.

Parameter		Value [1]	
		Min.	Max.
Input voltage	High	3.2 V	5.0 V
	Low	0 V	1.3 V
Output voltage	High	3.5 V	5.0 V
	Low	0 V	0.7 V
Output current	High		–12 mA
	Low		+12 mA
Power-up default		AUXOUT0 … AUXOUT3 are cleared (= set to 0 V).	
Reaction to PHS-bus I/O error		None	

[1] Unless stated otherwise, the specifications are valid only if the dSPACE hardware is correctly connected to the power, switched on, and ready for operation.

ECU Power-Sense Input

Objective

The ECU power-sense input (ECUSENSE) can be used to change the status of the board's output signals depending on the on-state of the ECU:

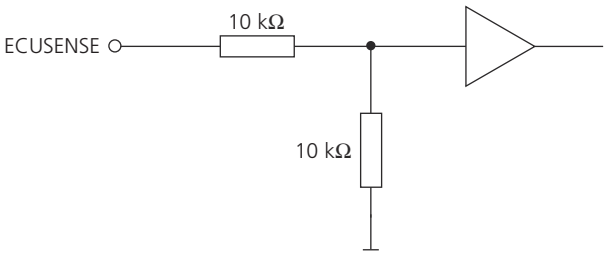
- If the ECU is not powered up, the ECUSENSE input is low (< 1.6 V). The DS4120 output buffers are disabled and set to the high impedance state.
- If the ECU is powered up, the ECUSENSE input is at high level (> 4 V) and the output buffers are enabled.

Note

If the buffer disable feature (and therefore the ECUSENSE pin) is not used, ECUSENSE must be connected to PODVCC.

Input circuit

The following illustration is a simplified diagram of the input circuitry.



Electrical characteristics

The input voltage of the ECUSENSE input must have the following characteristics.

Parameter		Value [1]	
		Min.	Max.
Input voltage	High	4.0 V	5.0 V
	Low	0 V	1.6 V

[1] Unless stated otherwise, the specifications are valid only if the dSPACE hardware is correctly connected to the power, switched on, and ready for operation.

Data Sheets

DS4120 Data Sheet

Technical data

The following table shows the data sheet of the DS4120:

Parameter	Specification [1]	
General	▪ Communication between processor board and ECU via dual-port memory ▪ Memory management unit (MMU) for advanced DPMEM control such as memory remapping and DWC triggering ▪ Slave interrupt control unit with up to 8 interrupt inputs ▪ 4 general-purpose input lines ▪ 4 general-purpose output lines	
Dual-port memory (DPMEM)	▪ Simultaneous access by processor board and ECU ▪ Supports 8- and 16-bit ECU access ▪ Processor board access with address auto-increment mode (useful for block transfers) ▪ Access arbitration through independent semaphores or hardware locking (wait states)	
	On-board DPMEM	8 K x 16
	On-board tag-RAM	8 K x 9
	On-board semaphores	8
	External DPMEM supported (POD or ECU)	64 K x 16 (maximum)
	External tag-RAM supported	64 K x 16 (maximum)
	External semaphores supported	8
Memory remapping	▪ ECU write accesses to DPMEM can be redirected to other addresses ▪ Allows bypassing of ECU algorithms ▪ Programmable individually per word	
DWC triggering	▪ Read and/or write operations can trigger events on DS5001 Digital Waveform Capture Board ▪ Up to 16 different events supported ▪ Programmable individually per word ▪ Complex trigger conditions can be implemented	
Interrupts	▪ 1 bidirectional interrupt for synchronization of data transfer between DPMEM and ECU ▪ 3 interrupts triggered by access to predefined DPMEM addresses ▪ 4 general-purpose interrupt lines (activated by external events)	
Voltage range	TTL output/input levels	
Output current	±12 mA max.	
Host interface	One 8- or 16-bit ISA slot (power supply only)	
Physical size	340 x 125 x 15 mm (13.4 x 4.9 x 0.6 in)	

Parameter	Specification [1]
Ambient temperature	0 … 70 °C (32 … 158 °F)
Power supply	+5 V ±5%, 1.2 A

[1] Unless stated otherwise, the specifications are valid only if the dSPACE hardware is correctly connected to the power, switched on, and ready for operation.

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