Dy 4 Systems

The future of high-integrity, embedded technology

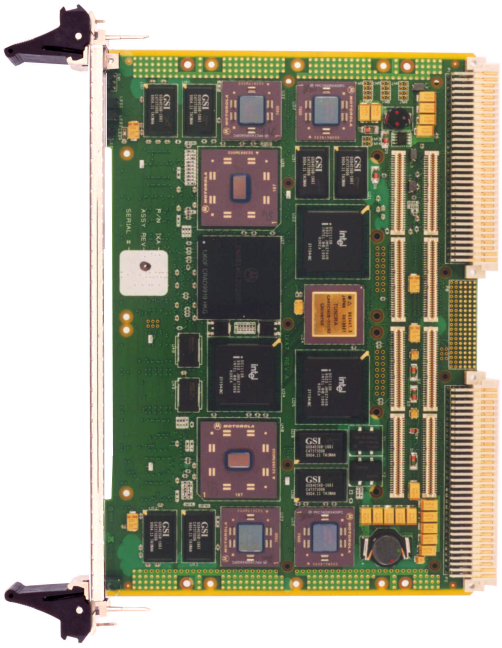
CHAMP-AV

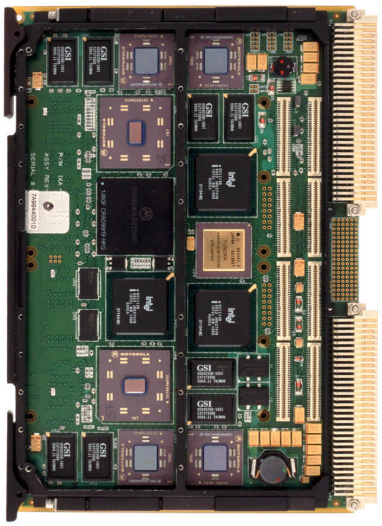
High Throughput DSP with Concurrent Multi-Processing Architecture

Features

- Processors
  - Four MPC7400/7410 PowerPC(TM) processors with AltiVec(TM) at 400-500 MHz
  - Over 16 GFLOPS peak floating point performance (four G4s at 500 MHz)
  - 200 MHz MPC8240 PowerPC core processor provides an additional 6.1 SPECint95
- Enhanced I/O
  - Support for two industry standard PMC I/O expansion modules, 3.3V or 5V
  - Advanced CHAMP (Common Heterogeneous Architecture for Multi-Processing) architecture allows concurrent PMC I/O, internal and VMEbus transfers
  - Bridges support up to 500 Mbytes/sec of cumulative, on-board, simultaneous I/O data movement
  - Seven DMA controllers
  - Advanced Universe IIb VMEbus host interface
  - Multi-channel interrupt multiplexer to control real-time applications
- Onboard Memory
  - Global SDRAM - 64 Mbytes, 64 bits wide, 100 MHz
  - Local SDRAM - 64 to 256 Mbytes per PowerPC pair, 64 bits wide, 100 MHz
  - L2 cache - 1 to 2 Mbytes per PowerPC
- Flash
  - 8 or 16 Mbytes
- Software Support
  - VxWorks(R) BSP with Shared Memory Networking
  - IXLibs-AV optimized Altivec DSP function library
  - I/OPlus with SmartDMA embedded runtime
  - IXAbsp board support libraries
  - HostAPI utilities

* Range of air- and conduction-cooled ruggedization levels available





Overview

The CHAMP-AV is the latest in the growing line of high-performance Digital Signal Processing (DSP) solutions. The CHAMP-AV provides over 16 GFLOPS of floating point performance in a single VMEbus slot. Supporting various high speed/high performance versions of the PowerPC G4 (with AltiVec) microprocessors from Motorola, the CHAMP-AV is ideal for a diverse range of real-time signal processing applications. Unique to the CHAMP-AV, the architecture supports two industry standard, PCI-based Mezzanine Cards (PMCs) providing a flexible and powerful I/O architecture that enables very high data flow rates and throughput.

The heart of the CHAMP-AV is its advanced, optimized data flow architecture (see Figure 1). The CHAMP-AV board is segmented into three isolated 64 bit, 66MHz PCI bus sections allowing the Core Processing Element (CPE) PowerPC processor (MPC8240) access to the VMEbus concurrently with I/O data transfer operations between either PMC sites and the four individual DSPs. The internal 64 bit/66 MHz PCI bridges allow concurrent and efficient data transfers between the independent DSP Signal Processing Elements (SPE) and the PCI bus sections which are 100% backward compatible with standard 32 bit/33 MHz PMC modules. The embedded MPC8240 CPE processor has access to the VMEbus, PMC I/O sites, and each SPE's local memory, allowing for flexible, free data flow and real-time control path implementations.

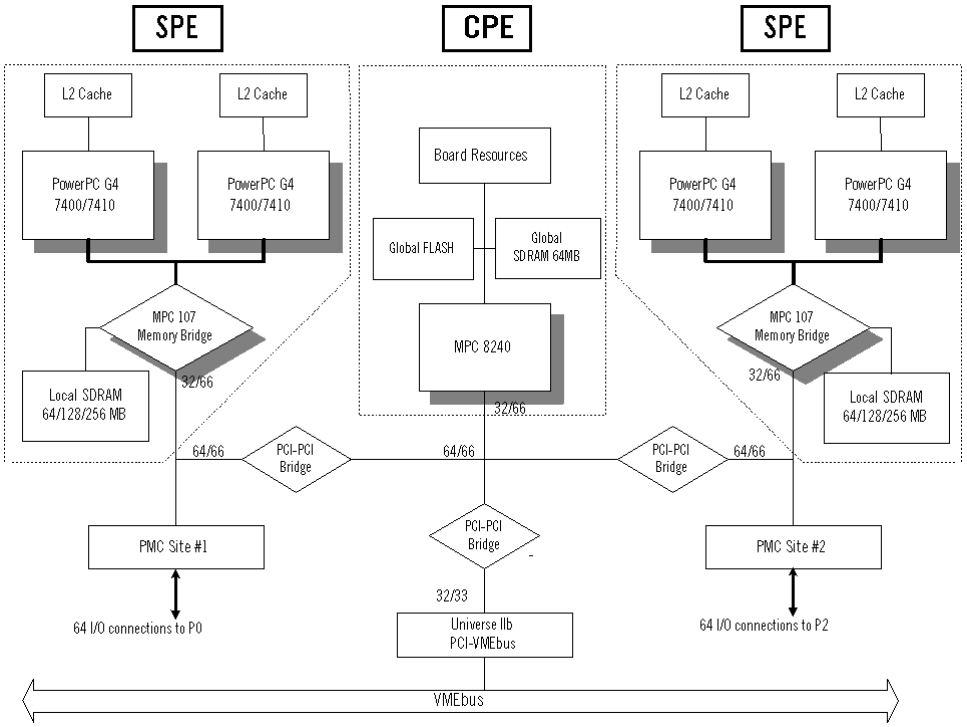


Figure 1: CHAMP-AV block diagram

The CHAMP Architecture

The CHAMP-AV is the second in a series of DSP processor boards from Dy 4 to support the Common Heterogeneous Architecture for Multi-Processing (CHAMP). The first was the highly successful CHAMP-C6, based on the TMS320C6x fixed and floating point DSP devices from Texas Instruments. The CHAMP architecture (see Figure 2) organizes the processing resources as two independent clusters of Signal Processor Elements (SPE's), each with the ability to have dedicated access to its PMC module for tightly coupled I/O resources. PCI-to-PCI isolation bridges allow for concurrent data movement on each isolated section of the PCI bus. The CHAMP architecture allows each processing cluster to perform I/O operations to its PMC module independently of other on-board data transfer operations. The MPC8240 embedded processor is also capable of performing I/O operations concurrently with the DSP clusters. The isolated triple PCI bus organization allows for up to 500 Mbytes/sec peak cumulative data transfer throughput.

Digital Signal Processors

The CHAMP-AV may be equipped with either two or four G4 PowerPC processors, which form the heart of the Signal Processing Elements (SPE's). The board supports either MPC7400 or MPC7410 processors (400 and 500 MHz). Every processor has access to all memory and I/O resources on the board including both local SDRAM arrays, global SDRAM, PMC sites and the VMEbus. This simplifies the programming as there are no restrictions on where application functions reside.

DSP Memory

The CHAMP-AV utilizes fast Synchronous Burst SRAM (SBSRAM) for the backside L2 cache and Synchronous DRAM (SDRAM) for local cluster memory. The SBSRAM interface supports up to 2 Mbytes of L2 cache memory per processor. The local SDRAM supports 64 to 256 Mbytes per SPE node with 100 MHz SDRAM in-page read access speeds.

Independent I/O Processor

The CHAMP-AV is equipped with a Core Processing Element (CPE) comprised of an MPC8240 integrated embedded processor/bridge device to handle I/O and general processing applications.

Running at 200 MHz, the MPC8240 provides 6.1 SPECint95 of additional computing performance. The MPC8240 can access up to 64 Mbytes of SDRAM, which may be used for I/O operations, data buffering, or general processing requirements. The board contains up to 16 Mbytes of on-board, user-programmable Flash.

The MPC8240 may be used in either of two ways, embedded or user-programmed.

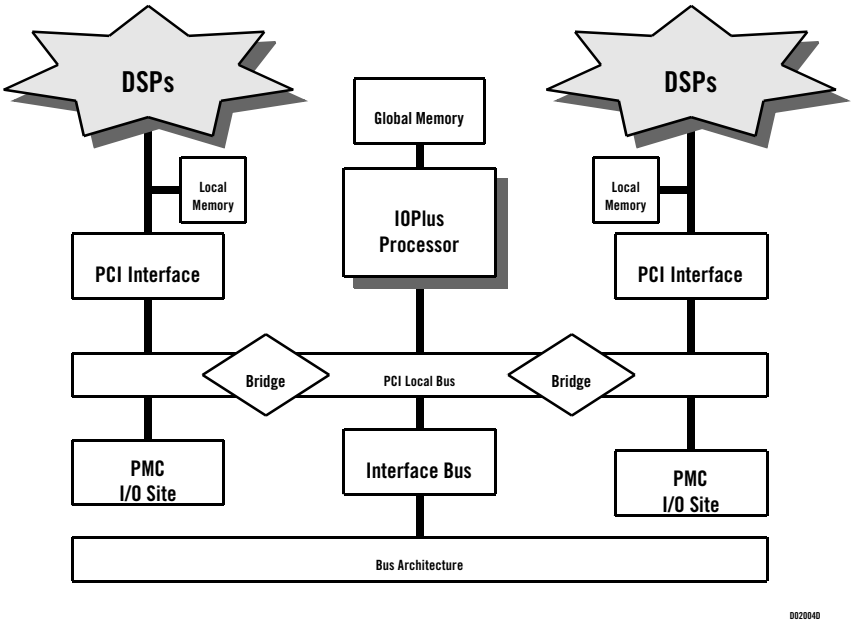
When used as an embedded processor, the user is not responsible to program the 8240. Instead the processor is delivered with SmartDMA firmware that provides data movement services independently of the G4 processors. SmartDMA works by utilizing the DMA controllers within the 8240. A users DSP application can send command messages to the SmartDMA firmware by using the supplied interface library. (Part of the IXATools software suite). SmartDMA can move data between any of the on-board memories, and also between memory and the VMEbus.

The other option is for the user to develop custom software to run on the 8240. This mode is fully supported with a VxWorks BSP (optional). This option affords the user the flexibility and power of isolating DSP tasks to the G4's, and keeping all I/O software running on the 8240. This can simplify the design of the DSP software, as it is not subject to asynchronous interrupts needed to service I/O devices. This is particularly relevant when special purpose PMC cards are employed.

DMA Controllers

A key aspect of maximizing the performance of a DSP application is to make optimum use of the various data busses on the card, so that data processing is balanced with data movement. The CHAMP-AV has seven independent DMA controllers that can be employed to move data while processing tasks occur simultaneously. Each MPC107 PCI-PowerPC bridge provides two DMA engines which operate in single or chained modes. The 8240 processor contains two others, and the Universe PCI to VME bridge provides a DMA controller for VME transfers.

Figure 2: The CHAMP Architecture



PMC Sites

The CHAMP-AV is equipped with two fully independent IEEE 1386.1 D2.0/VITA 32 D0.21 compatible PMC/PPMC sites. The PMC interfaces support 32-bit, 66MHz transfers to their associated pair of G4 processors. The board is compatible with either 32-bit or 64-bit PMC's at 33MHz or 66MHz. The conduction-cooled versions of the CHAMP-AV adhere to the ANSI/VITA 20-199x standard for conduction cooled PMC's. I/O is supported on both the front panel as well as the P2/P0 backplane connectors.

The two PMC sites provide industry-standard I/O mezzanine expansion for system developers. A large variety of standard modules are available from dozens of third parties to provide I/O, memory and processing expansion. Many system developers use PMC modules for their customized I/O circuitry, such as A/D, D/A, discrete, network interconnect fabric interfaces such as Fibre Channel, or point-to-point interfaces such as PCI and FPDP.

Other typical uses for PMC sites include:

- MIL-STD-1553B, Ethernet, Serial, Parallel, Analog
- Discrete digital lines and LVDS
- Custom interfaces to user-specific, proprietary hardware

Through strategic partnerships with several key PMC Dy 4 Embedded Partners Program members, Dy 4 offers a number of pre-configured PMC I/O system solutions ideal for digital radio, sonar, radar and high speed serial interconnect and fabric applications. Contact Dy 4 for assistance and suggestions in configuring other compatible PMC modules.

Inter-processor Messaging Interrupts and Semaphores

A multi-processor application needs to coordinate processing between processors. The CHAMP-AV allows the user to configure the hardware to suit any software/dataflow methodology. This is done with a sophisticated, multi-channel interrupt multiplexer that services 21 individual interrupt sources, and under software control, routes them to 9 unique destinations. This allows interrupt sources from the VMEbus, PCI buses and other sources to be individually routed to the PowerPC's and the MPC8240. Two input signals are provided at the P0/P2 connector to accept interrupts from external sources.

Four semaphore registers are available to help the user manage the sharing of board resources between multiple software tasks.

VMEbus Interface

The CHAMP-AV is equipped with a VME64x master/slave interface. The interface is implemented with the industry-standard Tundra Universe IIb supporting Slot One system controller functions, providing interrupter and interrupt handler and a full 64-bit capable VMEbus master and slave interface. Read-Modify-Write cycles are also supported. The Universe supports Geographical Addressing which enables the application program to determine which slot the board is plugged into. This is used to support the implementation of single software images on different boards within a system.

The CHAMP-AV draws both 5V and 3.3V power from the VMEbus backplane. In addition, advanced on-board power management circuitry isolates input power until both the 3.3V and 5V power rails stabilize within proper tolerances upon system power up. This ensures proper power sequencing protection for all on-board devices, and eliminates the requirements for sequencing or synchronizing within the system power-supply.

Software Support

The CHAMP-AV is supported with an extensive array of software items, which cover all facets of developing application code for the board.

- A VxWorks Board Support Package (BSP) is available that supports both the 8240 and 7400/7410 processors. Users have the option of using VxWorks on the 8240 alone, or on all five processors. The VxWorks BSP supports development of multi-tasking, Altivec-enabled applications under VxWorks 5.4, Tornado II. The BSP supports the VxWorks Shared Memory Networking feature. This allows the user to share a single network connection between multiple processors on one or many boards. In development, users can connect to a single Ethernet port, and then make TCP/IP connections to any processor in the system. An extension of this concept is that multiple software developers can share one connection into a rack of DSP cards and independently debug application code. For deployed systems, the shared network is especially beneficial as only a single Ethernet port must be cabled in the chassis to support in-system upgrades of software. The VxWorks BSP is delivered as part of the IXATools software suite. See the IXATools data sheet for detailed information.
- IXLibs-AV is a library of fully optimized DSP functions that take advantage of the Altivec instruction unit. By using IXLibs-AV the user is spared the complexity of programming the Altivec instruction unit. For customers with Altivec expertise, the library includes macros to support user assembly language development with a standard C compiler. The vector data structures are documented, so that a user can add their own functions to the library. See the IXLibs-AV data sheet for detailed information.

- The Board Resource Library contains C functions to access hardware features of the CHAMP-AV, such as interrupts, semaphores, VME, SmartDMA, Flash read/write and indicator LED's. The Board Resource Library is self-contained code that be can used without an operating system, or it can be used with VxWorks.
- The I/OPlus software runs on the 8240 to provide the SmartDMA capability which allows the G4's to command the 8240 to perform data movement operations. The I/OPlus software is delivered as firmware for the 8240, and as a linkable library for users writing applications for the 8240. The I/OPlus firmware also includes power-on diagnostics
- The Board Configuration Utility is an Windows-based program that is used to program the on-board Flash EPROM with configuration parameters and user application software.
- The HostAPI library is a set of functions that may be used on a Single Board Computer that is co-resident on the VMEbus with CHAMP-AV DSP cards. It provides functions to remotely load and start programs, check status, and program the CHAMP-AV on-board Flash. Contact Dy 4 for supported SBC's.
- The CHAMP-AV also supports the use of EST JTAG emulators in conjunction with a rear-transition module that provides the JTAG connections to the 8240 and the 7400/7410 processors. See the Options section.

Options

The following are optional items that work with the CHAMP-AV

- A backplane transition module containing an Ethernet interface and EIA-232 serial port is available to facilitate a VxWorks development environment, part number IXA-E1S.
- A PMC ENET-01 module is available as an alternate to the backplane transition module. It provides an Ethernet interface and an EIA-232 serial port. The PMC-ENET is available in commercial air-cooled, and rugged conduction-cooled versions.

Multiple Environmental Grades

The CHAMP-AV is available in a full range of environmental grades starting from commercial air cooled to extended temperature, rugged conduction cooled versions. This allows the customer to select the board to match the environmental requirements of the platform.

Table 1: Specifications

PROCESSORS	MEMORY
Four PowerPC 7410s at up to 500 MHz	1 to 2 Mbytes SRAM L2 cache per processor 64 to 256** Mbytes local SDRAM per processor pair
One MPC8240 CPE at 200 MHz	64 Mbytes of global SDRAM
	8 to 16** Mbytes of Flash EPROM
VME INTERFACE	
32-bit with VME64 capability, Slot One interface	Implemented with Universe IIb VME/PCI Bridge
5 Row P1/P2 VME64X connectors (160 pins)	P0 connector (95 pins)
6U Double Eurocard Form Factor (233.3 mm x 160 mm), single slot	A32/A24/A16, D32/D24/D16/D8 Master slave
PCI INTERFACE	
Primary internal PCI Bus: 32-bit/33 MHz, 64-bits/66 MHz	PCI Rev. 2.2 compliant PMC compliant
Secondary PCI buses: auto-configurable to 33 or 66* MHz, compatible with 32 or 64-bit interface	2 PMC slots: PMC1 I/O routed to user defined pins on P2 PMC2 I/O routed to user defined pins on P0
DEVELOPMENT INTERFACES	
10 Base T Ethernet	Interface via rear transition module (IXA-E1S), or front panel with PMC ENET module
JTAG PowerPC 7400/7410 and MPC8240 development	16 pin header on rear transition module IXA-E1S
EIA-232 serial port	Interface via rear transition module (IXA-E1S), or front panel with PMC ENET module
POWER REQUIREMENTS (without PMC)	
On-board circuitry isolated until 3.3 and 5V DC are stable/valid	
+5V	6.2 A typical ***
3.3V	2.7 A typical

* Refer to the Dy 4 Ruggedization Guidelines datasheet for more information.
** Availability is component driven, consult factory for additional information.
*** Detailed power consumption characterization report available.

Table 2: Environmental Specifications

	Air-cooled Level 0	Conduction-cooled Level 100*
Board Temperature		
Operating	0°C to 55°C (4 cfm at sea level)	-40°C to 71°C
Storage	-40°C to 85°C	-55°C to 85°C
Relative Humidity	Up to 95% non condensing	Up to 100% non condensing
Vibration **Sine** **Random**	 N/A N/A	 10 g peak, 15-2 kHz 0.1 g2/Hz, 15-2 kHz
Shock	N/A	40 g 11 ms ½ sine (peak)
Airflow	1.5 m/s	N/A
Base Card Dimension	per ANSI/VITA 1-1994	per IEEE 1101.2 -1992
Weight	<570 g (<1.26 lbs.)	<900 g (<1.98 lbs.)
Conformal Coat	Optional	yes

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References to other documents of the exact issue, or if not shown, the issue in effect at the time of publication form a part of this specification to the extent referenced herein. In the event of a conflict, this specification will be considered a superseding requirement.

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