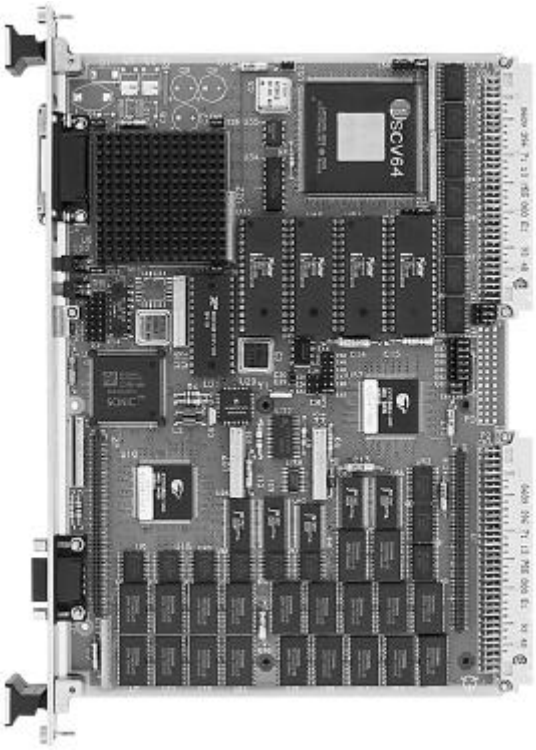
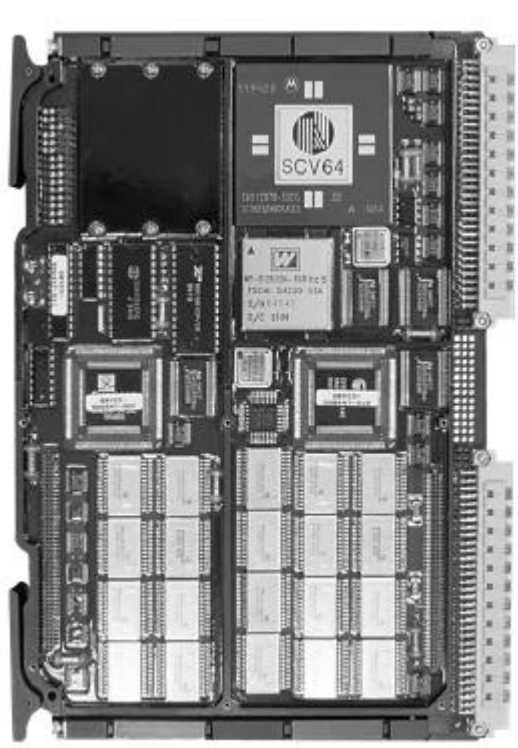
SVME/DMV-163

68040 Single Board Computer with MAXPack Interface





Features

- *68040 CPU at 25 or 33 MHz*
- *16M bytes or 32M bytes DRAM with parity (up to 64M bytes on SVME levels 000 and 100, and DMV level 100)*
- *512K bytes Flash™ EPROM, expandable to 4M bytes*
- *Support for one MAXPack module, providing flexible I/O expansion*
- *Advanced VME Interface Chip (SCV64)*
  - *A32:D32 VMEbus interface with A64:D64 MBLT support per ANSI/VITA 1-1994, VME64*
  - *Location monitor with FIFO buffer*
  - *Bus Isolation mode (BI-mode®)*
  - *Auto-ID and Auto-SYSCON*
  - *System controller functions*
- *512 byte serial EEPROM*
- *One 16-bit counter/timer*
- *Ethernet™ interface on SVME levels 000 and 100 and DMV level 100*
- *Two EIA-423 compatible serial channels*
- *Real-Time Clock (RTC)*
- *Tick and watchdog timers*
- *Built-In-Test (BIT)*
- *Foundation firmware including:*
  - *Debug monitor*
  - *Diagnostics*
  - *Card Support Services*
  - *Execution Sequencer*
- *Conduction cooled per IEEE 1101.2 (0.80-inch pitch) for MIL-E-5400/4158, and MIL-STD-2036 applications*
- *Optional levels of ruggedization available*

Description

The SVME/DMV-163 Single Board Computer, (SBC), built with state-of-the-art technology, combines a high-performance 33 MHz 68040 processor and up to 64M bytes of DRAM on one circuit card. The card is equipped with DY 4's MAXPack interface, a standard mezzanine module approach to achieve additional expansion capability. System designers can increase the SBC's functionality by incorporating one of several standard MAXPack modules, or by developing their own custom module. MAXPack modules provide a single-slot solution for customers whose systems require specialized I/O. Traditionally, using multiple boards has been the only way to fulfill such system requirements. Figure 1 shows a block diagram of the SVME/DMV-163 SBC.

The SVME/DMV-163's design features address mission-critical demands of military and aerospace systems integrators with increased computing performance, self-test coverage and functional density.

The card supports DY 4 Systems' standard features including an AVICS-based VMEbus interface, Built-In-Test (BIT), Bus Isolation mode (BI-mode®), location monitor, and Auto-ID. These features bring benefits in performance, logistics and maintenance.

DY 4's custom-designed SCV64 chip implements all VMEbus interface functions with software-programmable features. It combines low-latency access to the VMEbus with high sustained throughputs. BIT hardware features verify all operational circuits on the module. BI-mode® increases ease of testing and system fault location. The location monitor supports efficient inter-processor messaging, to minimize overhead in real-time software. Auto-ID allows boards to be self-configuring, based on slot location.

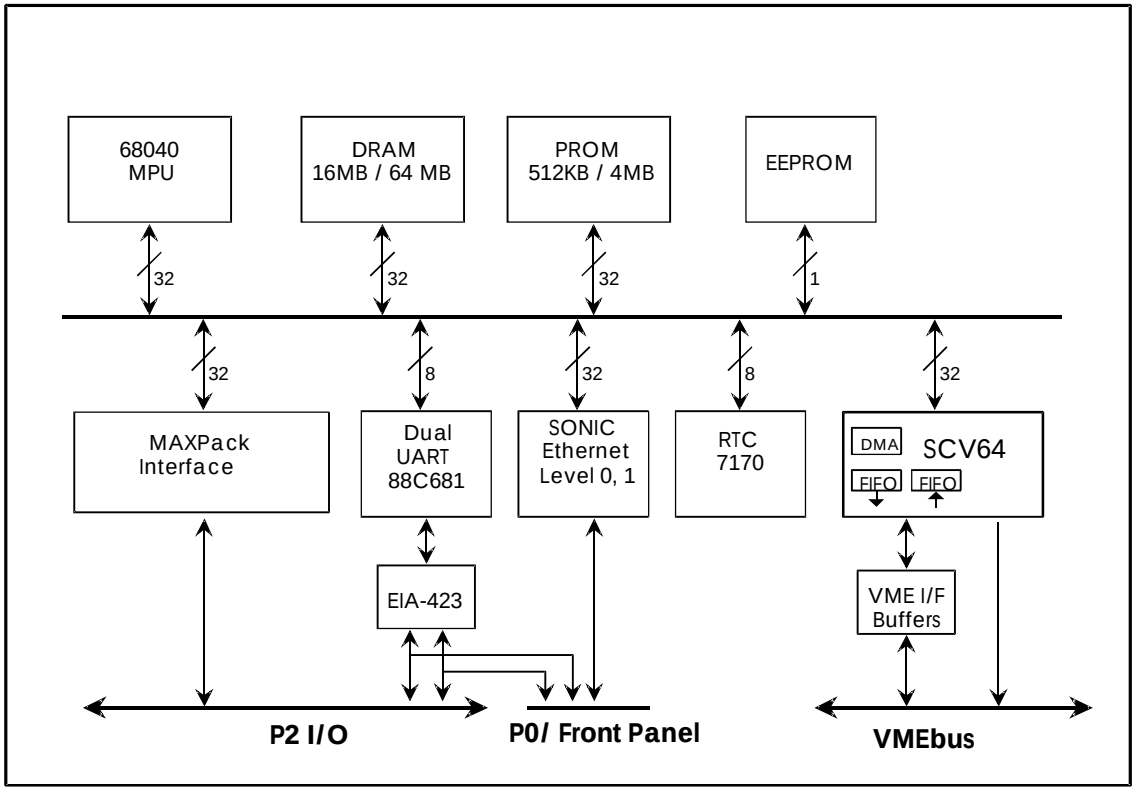


Figure 1: SVME/DMV-163 Block Diagram

These features allow users to:

- build high-performance multi-processor systems
- detect and isolate faults during operation
- minimize field maintenance and sparing logistics.

All versions of the SVME/DMV-163 are functionally identical, except for level 200 and 300 boards, which do not support Ethernet™. SVME versions for use in air-cooled environments are available in DY 4 ruggedization levels 000, 100, 200 and 300.

The conduction-cooled DMV version is designed for airborne, land-mobile, and naval military applications where circuit cards are sealed in a chassis to prevent moisture, salt-fog, sand, and dust contamination. DY 4 Systems' conduction-cooled products are designed for severe environmental conditions defined by MIL-E-4158, MIL-E-5400, and MIL-STD-2036. On Level 200 and 300 boards a single-piece aluminum thermal plane bonded to the PWB conducts heat away from the electronics. Its integral stiffening ribs improve heat dissipation and vibration resistance. Standard wedgelock fasteners give a reliable thermal connection to the chassis.

CPU

The 68040 CPU is a high-performance, 32-bit microprocessor from Motorola's third generation of the M68000 family. It is a virtual memory microprocessor using multiple, concurrent execution units and a highly integrated architecture. The 68040 CPU integrates the following:

- 68030-compatible integer unit
- 68881/68882-compatible Floating Point Processor (FPP)
- dual independent demand-paged Memory Management Units (MMU) for instruction and data stream accesses
- 4K byte instruction cache
- 4K byte data cache.

Memory

The memory of the SVME/DMV-163 SBC can be configured to support from 16M to 64M bytes of DRAM. The DRAM has byte parity protection. A parity error can be made to cause an interrupt to the CPU. The DRAM is accessible from the on-board CPU, the VMEbus, and the MAXPack interface. The memory interface design supports 68040 burst mode accesses. The burst performance is 4/3/2/2 for writes; 5/4/3/3 for reads. Random write accesses require four clock periods; reads require five.

There is a single memory bank for non-volatile storage. This 32-bit wide memory bank supports Flash™ EPROM, EEPROM and EPROM devices. Up to 4M bytes of storage is possible. Flash EPROM and EEPROM devices may be programmed on-board. Table 1 summarizes the memory configurations for the SVME/DMV-163 SBC.

The SVME/DMV-163 SBC also has a 512 byte serial EEPROM for storing configuration data.

LAN Interface

The level 000 and 100 versions of the SVME/DMV-163 SBC provide an IEEE 802.3 LAN interface at the three-pair AUI level. The transformer-coupled interface is routed to either a front panel connector or a backplane P0 connector. Using this LAN interface is beneficial during the software development process. Modern development systems often require a LAN connection to the target board for high speed downloading and debugger support. The LAN interface is implemented with a National Semiconductor 83932B SONIC™ device.

For users that require a level 200 or 300 board with a LAN interface, the SVME/DMV-163 SBC will accept the MAX-220 MAXPack that provides LAN, SCSI, serial and parallel interfaces.

Table 1 Memory Configurations			
Type	**Quantity**	**Width**	**Note**
DRAM	16M, 32M, 48M, 64M bytes	32-bit	1
Boot PROM	128K, 512K bytes, 1M, 2M, 4M bytes	32-bit	2

Notes:

1. The maximum DRAM capacity of level 200 and 300 boards is 32M bytes.

2. The maximum PROM capacity is dependent upon memory technology, EPROM, Flash EPROM, EEPROM and availability of components. Contact the factory for latest availability information.

MAXPack Interface

The SVME/DMV-163 SBC is equipped with a MAXPack mezzanine module interface. MAXPacks may be used to add a variety of I/O functions to the base board. MAXPack modules conform to an open specification that defines the electrical and mechanical interface, thus permitting customers to design special function modules. DY 4's RISC - based SBCs carry the same MAXPacks, thus providing a performance growth path that preserves the software invested in the MAXPack.

The MAXPack mechanical design is suited to high shock and vibration environments. The modules are rigidly mounted to the base board along three stiffening ribs and also along a rib parallel to the card edge. This arrangement is structurally rigid, and it provides a low-resistance thermal path for heat removal.

All I/O connections of the MAXPack module are brought out to the P2 connector of the SVME/DMV-163 SBC. Figure 2 shows a conceptual view of the assembly.

VME Interface

The VMEbus interface of the SVME/DMV-163 SBC is implemented with DY 4's Single Chip VMEbus Interface, SCV64, which provides all the elements of a complete VMEbus interface. The philosophy of the SCV64 design is to provide programmable features that eliminate the need for jumpers, thereby simplifying logistics and reducing sparing requirements. The SCV64 incorporates the following:

- System Controller
- Master/slave A64:D64 interface
- Tx and Rx FIFO's to decouple bus operations
- Location monitor with FIFO message queue
- Interrupter, interrupt handler
- Extensive BIT support

The SCV64 provides all VMEbus system controller and interrupt functions. It allows for full programmability of requester modes and levels, arbiter modes, bus timers, interrupt levels and vectors. The SCV64 also features extensive BIT support and BI-mode®.

A primary function of the SCV64 is to allow the CPU to access the VMEbus, and to allow the VMEbus to access on-board memory. The SCV64 contains transmit and receive FIFO's which are used to implement a store-and-forward technique of bus decoupling. SCV64-equipped CPUs can write to VMEbus locations without incurring a delay while the VMEbus is requested and arbitrated, and the bus grant is received.

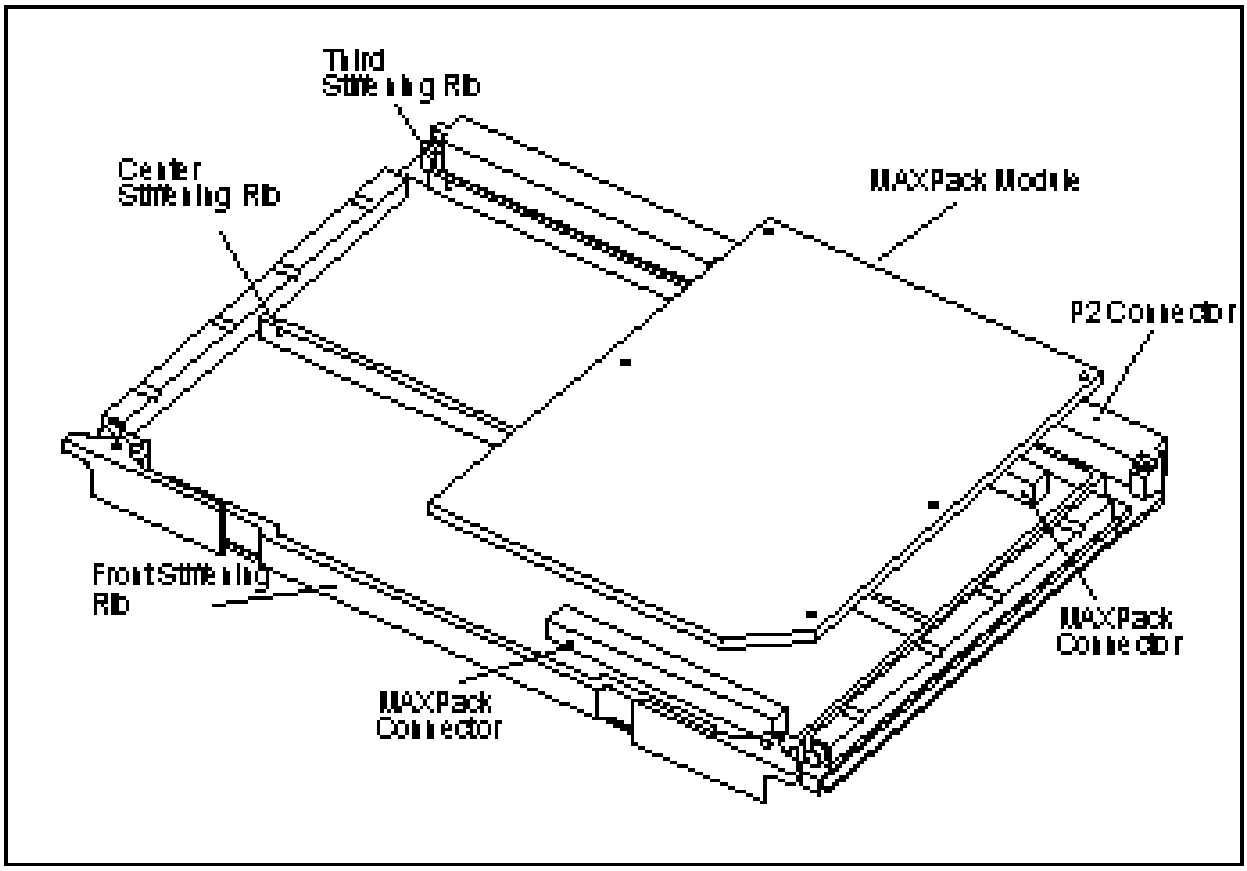


Figure 2: Base Board with MAXPack

For moving large blocks of data between on-board memory and the VMEbus, the SCV64 provides an integral DMAC. Bi-directional transfers can be configured to occur in discrete, block, or multiplexed block (D64) mode. Real throughput of up to 60M bytes/sec may be achieved.

To support inter-processor message passing, the SCV64 provides a location monitor (LM) with a built-in FIFO message queue. A write access to the LM results in capture of the data, and causes an interrupt to the CPU. The message queue is organized as a 32-bit wide FIFO with 31 entries.

Serial Interface

The SVME/DMV-163 is equipped with an 88C681 UART, which provides two asynchronous serial channels. The electrical interface of the serial channels is EIA-423, permitting communication with EIA-423, EIA-422, and EIA-232 interfaces. Baud rates are programmable from 75 to 38.4K baud. Interrupts are also programmable under software control. The serial channels are available at the P2 connector and at the front panel connector on the SVME version.

Real-Time Clock (RTC)

The SVME/DMV-163 is equipped with a Harris 7170 RTC chip to provide for time-of-day calculations. It contains registers for year, month, day, day-of-week, and seconds through to hundredths of seconds, and interrupt controls. Leap-year and days per month are automatically updated. The RTC is capable of periodic or alarm/wake-up interrupts to the CPU.

The RTC may be powered from the +5V STDBY line, therefore it can continue to maintain the time during loss of main power.

Timers

The SCV64 chip provides the user with two timers. A tick timer can be programmed to interrupt the CPU at regular intervals. A watchdog timer provides a fail indication and resets the CPU if it detects an execution failure.

An additional 16-bit timer provided by the 88C681 UART is available for use by the programmer.

System Status Signals

The SVME/DMV-163 SBC provides a status signal on the P2 connector. This signal asserts in the event of a card failure and corresponds to the front panel indicator LED, permitting a test connector to be incorporated in a sealed conduction-cooled chassis.

MAXPacks

The capabilities of the SVME/DMV-163 SBC can be enhanced by adding a MAXPack module. MAXPack modules are available in all standard DY 4 ruggedization levels, for use with both air-cooled and conduction-cooled base boards. MAXPacks that are available or are currently in development include:

- **MAX-220**: SCSI/Ethernet serial/parallel Controller, provides SCSI (single-ended), Ethernet , four asynchronous RS-232/RS-422 or two synchronous RS-232/RS-422 serial channels, and a 14-bit parallel interface.
- **MAX-230**: VSB and Ethernet
- **MAX-651**: Single 1553B, Utility Bus, serial I/O, parallel I/O and non-volatile memory.
- **MAX-654**: Dual 1553B Controller, provides two redundant 1553B interfaces. Support for 1553A, and 1553B Notice 2. Modes include BC, RT and BM.

Foundation Firmware

The SVME/DMV-163 SBC is supplied with a foundation firmware package consisting of:

- General Purpose Monitor (GPM) - provides comprehensive monitoring and debug functions for the system integrator (refer to General Purpose Monitor, document MS00053)
- Card Level Diagnostics (CLD) - provides diagnostic routines which perform a self-test function in conjunction with the Built-In-Test equipment (refer to Card Level Diagnostics, document MS00050)
- Card Support Services (CSS) - provides a common software interface to the hardware features on the card, device independent I/O functions, generic exception processing routines, and Auto-ID services (refer to Card Support Services, document MS00180)
- Execution Sequencer (ES) - controls the invocation order of the Software Configuration Items on the card (refer to Execution Sequencer, document MS00181).

Variants / Ordering Information

If an SVME-163 is required for development purposes or a quick-turn project, DY4 provides the following variants with reduced lead-time.

- **SVME-163-042** SBC with a 33 MHz 68040 CPU, 16MB DRAM, 4MB Flash EPROM, 512 serial EEPROM, Ethernet, a 16-bit timer/counter, two EIA-423 serial channels and a real-time clock.
- **SVME-163-044** includes all the features of the -042 plus the MAX-220 MAXPack which includes 4MB DRAM, a second Ethernet, SCSI, parallel and 4 EIA-232/422 interfaces.
- **SVME-163-045** includes all the features of the -042 plus the MAX-651 MAXPack which includes a dual redundant 1553B, a dual EIA-232/422 serial and a 10-bit parallel interface.
- **SVME-163-047** includes all the features of the -042 plus the MAX-654 MAXPack which includes two dual redundant 1553B interfaces.

Recommended Variants

Table 2 is a list of recommended variants. It includes a wide variety of configurations to match the features, performance and ruggedization levels required for most applications

Special Variants

Special variants can be provided if the one of the recommended variants is not suitable. Contact your local sales representative for cost and availability. SVME/DMV-163 options and accessories include:

- 16M bytes to 64M bytes of DRAM
- DRAM parity or no parity
- Processor clock frequency (25 or 33 MHz)
- PROM memory type and size
- Factory installation of MAXPacks
- P2 I/O cable for development use
- FlashProg Flash EPROM programming utility
- VxWorks Board Support Package
- Ruggedization levels

Other Single Board Computers from DY 4

DY 4 produces a full line of both CISC and RISC single board computers with a variety options.

- **SVME/DMV-162** SBC with 68040 CPU up to 8MB SRAM and 8MB Flash EEPROM.
- **SVME/DMV-166** SBC with 68040 CPU up to 8MB SRAM and 8MB Flash EEPROM.
- **SVME/DMV-170** SBC with PowerPC 603 RISC CPU, up to 12MB SRAM and 4MB Flash EEPROM.
- **SVME/DMV-171** SBC with PowerPC 603 RISC CPU, up to 64MB DRAM with Error Detection And Correction (EDAC) and 8MB Flash EEPROM.
- **SVME/DMV-180** SBC with MIPS R4600 64-bit RISC CPU, up to 8MB SRAM and 16MB Flash EEPROM.

For more information call your local sales representative.

Table 2
SVME/DMV-163 Matrix

Variant 163-	MAXPack	Clock Speed MHz	DRAM	Flash	Serial ports	SCSI	Ethernet	1553B	Other
x21		25	16M	512K	2		1		No parity
x22	MAX-220	25	16M	512K	2+4	1	2		No parity 14-bit parallel 4MB DRAM
x37		33	16M	2M	2		1		
x38	MAX-220	33	16M	2M	2+4	1	2		14-bit parallel 4MB DRAM
x39	MAX-654	33	16M	2M	2		1	1	
x52	MAX-654	33	16M	2M	2		1	2	
x40	MAX-651	33	16M	2M	2+2		1	1	10-bit parallel
x69	MAX-651	33	16M	2M	2+2		1		No parity
x70	MAX-651	33	16M	2M	2+2		1		
x42		33	16M	4M	2		1		
x44	MAX-220	33	16M	4M	2+4	1	2		14-bit parallel 4MB DRAM
x45	MAX-651	33	16M	4M	2+2		1	1	10-bit parallel
x46	MAX-651	33	16M	4M	2+2		1	1	10-bit parallel 128k EEPROM
x47	MAX-654	33	16M	4M	2		1	2	
x05		33	16M	512K	2		1		
x06	MAX-220	33	16M	512K	2+4	1	2		14-bit parallel 4MB DRAM
x08	MAX-654	33	16M	512K	2		1	1	
x01		33	32M	512K	2		1		
x02	MAX-220	33	32M	512K	2+4	1	2		14-bit parallel 4MB DRAM
x54	MAX-654	33	32M	2M	2		1	1	

Notes:

- SVME Level 000 versions of marked variants are available with reduced lead times.
- Only versions with the MAX-220 include Ethernet at level 200 and 300
- Includes 2 EIA-423 and 4 EIA-422/232 channels
- Includes 2 EIA-423 and 2 EIA-422/232 channels
- All SVME/DMV-163 cards include an A64:D64 VME interface, a real-time clock and a 16-bit timer.

Table 3
Specifications

ENVIRONMENTAL SPECIFICATIONS		
Temperature	**(Level 000)**	
Operating	0°C to 50°C	MIL-STD-810
Storage	-40°C to 85°C	Methods 501.3 & 502.3
Temperature	**(Level 100)**	
Operating	-40°C to 71°C	MIL-STD-810
Storage	-62°C to 85°C	Methods 501.3 & 502.3
Temperature	**(Levels 200, 300)**	
†Operating	-55°C to 85°C	MIL-STD-810
Storage	-62°C to 125°C	Methods 501.3 & 502.3
Humidity (DMV CCA and SVME CCA - Levels 100, 300)		
Operating	0 to 95% non-condensing	MIL-STD-810
Non-Operating	0 to 100% condensing	Method 507.3
Vibration (DMV)		
Sine	5g at 15 to 2,000 Hz	MIL-STD-810
Random	$0.1g^2$/Hz	Method 514.4
Shock (DMV)	40g/11ms half sine	MIL-STD-810 Method 516.4, Proc 1
Altitude (DMV)	21,350m (70,000 ft)	MIL-STD-810 Method 500.3

DIMENSIONS	DMV CCA	SVME CCA
Height	233.4 mm (9.2 in.)	233.4 mm (9.2 in.)
Depth	160 mm (6.3 in.)	160 mm (6.3 in.)
Thickness (base)	16.5 mm (0.65 in.)	20.0 mm (0.8 in.)
(base+MAXPack)	20.0 mm (0.8 in.)	20.0 mm (0.8 in.)
Weight	<900g (<2.0 lb)	<570g (<1.28 lb)

POWER REQUIREMENTS	maximum	typical
+5v (+5%, -2.5%)	2.8 A (16M bytes) 4.2 A (64M bytes)	2.3 A (16M bytes) 3.5 A (64M bytes)
+12v (+5%, -2.5%)	16 mA	
-12v (+5%, -2.5%)	16 mA	

† As a general design objective, the junction temperature of all components on the DMV-163 SBC is limited to 110°C maximum (when the chassis cold-wall temperature is 85°C.) When reliability or performance factors permit, a component's junction temperature may exceed 110°C marginally.
SVME board operating temperature is based on air flow of 11 cfm.

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References to other documents of the exact issue, or if not shown, the issue in effect at the time of publication form a part of this specification to the extent referenced herein. In the event of a conflict, this specification will be considered a superseding requirement.

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