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SVME-178-1850

Product Release Note

Revision	-	A	B	C
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Product Release Note

SVME-178-1850

Revision History

Rev	Title	Description of Changes	By	Affected Pages	Date
-	Product Release Note SVME-178-1850	Production Release	P. ST-Amour	All	Jan 25, 2000

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Product Release Note

SVME-178-1850

Contents...

This Product Release Note describes the unique characteristics of your particular variant. Specifically, this document provides the following information:

card features

hardware requirements

software requirements

compliance to ruggedization levels

variant configuration

memory map

P0 and P2 interface configuration

Foundation Firmware.

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Introduction

This document describes the options and features specific to the SVME-178-1850.

Product Description

The SVME-178-1850 has the following features:

- PowerPC 740 Microprocessor
  - 300 MHz Internal Bus Speed
  - 66 MHz Local Bus Speed
- 512KBytes L2 Cache SRAM
- 16MBytes of 64 bit wide non-volatile FLASH memory
- 0MBytes of 8 bit wide non-volatile FLASH memory
- 8KBytes Autostore NOVRAM
- 64MBytes of DRAM
- 33 MHz 32 bit Peripheral Component Interface (PCI) bus
- Slot 1 PCI Mezzanine Card (PMC 1) Interface
  · Not Populated
  Slot 2 PCI Mezzanine Card (PMC 2) Interface
  · Not Populated
- Super I/O Peripheral Device
  Providing two 16C550-compatible EIA-232 async serial (1 & 2) Cha.
- 85C30 SCC
  · Providing two EIA-422 sync/async serial channels (3 & 4)
- VMEbus IEEE STD1014-1987 compatible provided by the Universe II
- Ethernet 10BaseT/100Base-TX Interface · Populated
- SCSI 2 Interface · Populated
- Real Time Clock (RTC)
- P0 connector installed
- Four 16-bit Timers, Watchdog Timer
- One (User accessible) 4 KBit Serial E2PROM
- VMEbus system controller functions
- Bus isolation mode (BI-mode®) capability
- Built-In-Test support

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Related Documents

Refer to the following documents for additional information.

Document	Number
Circuit Card Assembly, SVME-178-1850	PL901106-037
DOC Package, SVME/DMV-178	807197
Programmer's Reference, VME-178, V8 FFW	807196
Acceptance Test Procedure, SVME-178-1850	809717
Circuit card assembly, SVME-178-1850, Generic	700775-007

Variant Requirements

Software Requirements

The SVME-178-1850 meets the following software requirements:

- Circuit card assembly is supplied with foundation firmware V8.0.

Test Requirements

The SVME-178-1850 meets the following test requirements:

- Implement Acceptance Test Procedure 809717
- Test Pattern is not required in the 64 bit site
- Write protection is not required

Other Requirements

The SVME-178-1850 meets the following other special requirements:

- None

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Compliance to Ruggedization Guidelines

HEADING	REQUIREMENT FOR SVME LEVEL 100 CCA	COMPLIANT
BOARD TEMPERATURE OPERATION/STORAGE	Operating -40ºC to 71ºC Storage -55ºC to 85ºC	Y
HUMIDITY OPERATING STORAGE	0 to 95% non-condensing 0 to 95% non-condensing	Y
VIBRATION SINE RANDOM	10G peak 15-2KHz 0.04g2/Hz 15-2KHz	Y
SHOCK	30g peak half sine 11ms	Y
ALTITUDE (ft) OPERATION/STORAGE	30,000 40,000	Y
CONFORMAL COATING	Yes	Y
IC PACKAGE	Plastic/Ceramic	Y
IC TEMPERATURE RANGE	As per DY4 Level 100 performance spec	Y

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Variant Configuration

There are no optional devices configured on this variant.

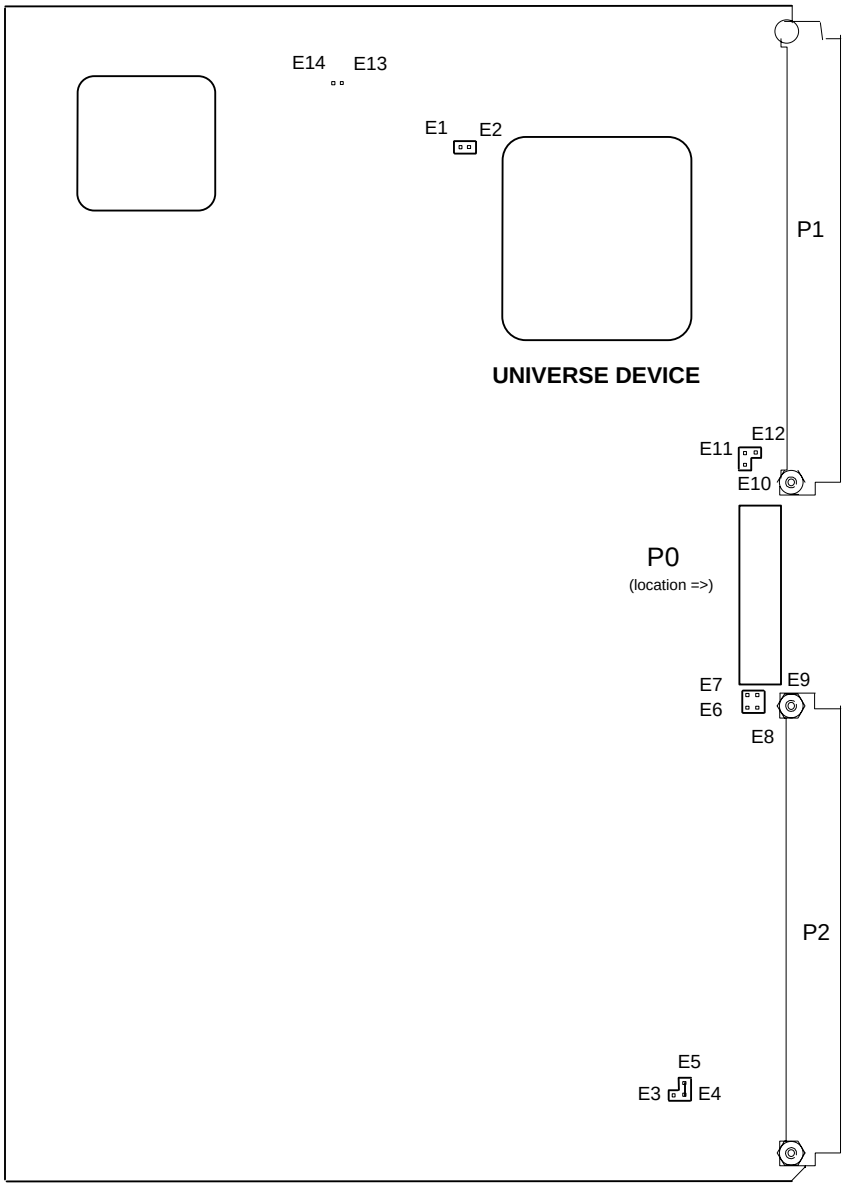
Strapping Explanation

The SVME-178-1850 is strapped in the following configuration:

- CLD is enabled after reset (E1-E2 open)
- NVRAM Chip Select uses supervisor (E4-E5 connected, E3 open)
- CCA boots from local 2Mx16 non-volatile memory, 64 bit site (E6-E7 open)
- Flash write protect is enabled (E8-E9 open)
- FLASH Vpp disconnected for both 8- and 64-bit banks (E10, E11, E12 open)

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Pictorial Representation Of Configuration



TYPE	CONFIGURATION	ITEM #
HEADERS	E1-E13	3 and 4
SHUNTS	None	-
WIRE LINKS	None	-
WIRE WRAP	E4-E5	24

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Circuit Card Modifications

- None

Memory Map

Local Memory Map

- Refer to VME-178 Hardware User's Manual document number 807195

VME Slave Memory Map

- Refer to VME-178 Hardware User's Manual document number 807195

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P0 and P2 Interface Usage

This chart shows how the base card and optional PMC module share the base card P0 and P2 interface connectors for this variant.

178 Parallel Port Mode

P2 Connector factory configured via 0 Ohm resistors to provide Base Card I/O to P2 Rows A and C.

	FRONT PANEL	P0	P2 ROWS A&C	P2 ROWS D&Z
SCSI	N/A	N/C	√	√
Ethernet	N/A	√	√	√
Serial 1 (RS232)	√	√	√	√
Serial 2 (RS232)	√	N/C	√	√
Serial 3 (RS422)	N/A	N/C	√	√
Serial 4 (RS422)	N/A	N/C	√	√
Parallel Port	N/A	N/A	√	N/A
PMC 1	N/A	√	N/A	N/A
PMC 2	N/A	N/A	N/C **(J4 PMC2 I/O connector removed)**	N/A

NOTE: No PMC Site 2 signals available on P2 Rows A and C, otherwise conflict will occur between Base Card I/O signals and PMC2 signals.

KEY :

N/A The interface cannot be configured to be available on this connector
N/C The interface is not configured to be available on this connector on this variant
√ The interface is available on this connector

EXCEPTION :

PMC not installed are: PMC 1, PMC 2
Features not populated are : None

Refer to the Getting Started or the Hardware Manual for more information.

Firmware

- Refer to VME-178 Programmer's Reference document number 807196

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