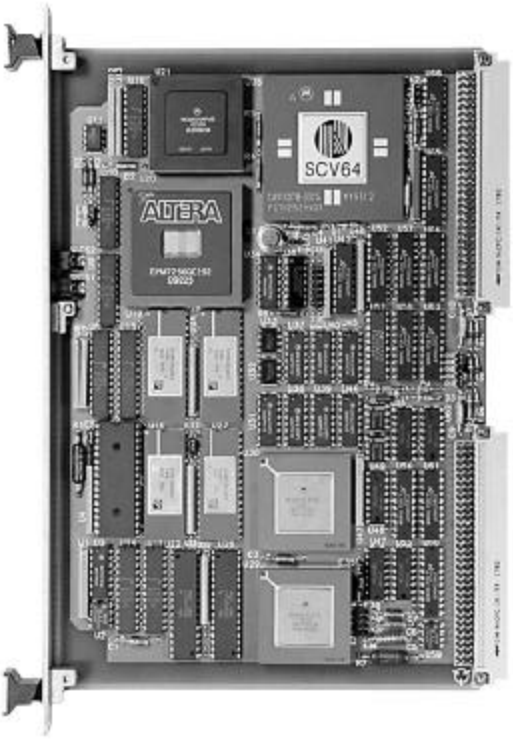
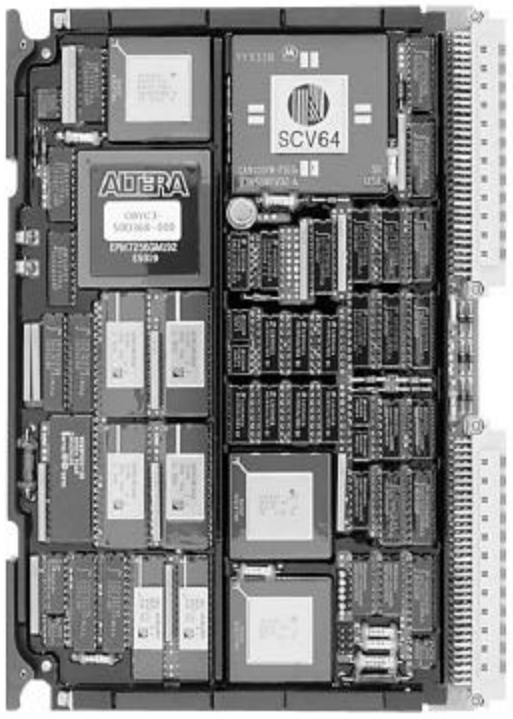
SVME/DMV-739

Intelligent Serial Communications Controller

Features

- *16 MHz 68020 CPU*
- *Data Link Communication Suite (DLCS) firmware providing synchronous and asynchronous services*
- *Six serial I/O channels*
  - *All channels software selectable between EIA-422 and EIA-423*
  - *Two channels selectable as EIA-485*
  - *EIA-422 channels support "party-line" applications*
  - *Programmable channel configuration for clocks and handshaking lines*
  - *Custom serial pre-processor*
- *Two 68302 Integrated Multiprotocol Processors (IMPs), each providing*
  - *Synchronous protocols such as HDLC/ SDLC™*
  - *Asynchronous operation*
  - *Six DMA channels*
- *512K bytes SRAM*
- *256K bytes of Flash™ EPROM in one 32-pin JEDEC byte-wide socket*
- *512 bytes of serial EEPROM*
- *A64:D64 VMEbus interface per ANSI/VITA 1-1994, VME64*
- *Auto-ID*
- *Location monitor*
- *Conduction cooled per IEEE 1101.2 (0.65-inch pitch) for MIL-E-5400/4158, and MIL-STD-2036 applications*
- *Optional levels of ruggedization available*
- *Built-In-Test (BIT)*
- *Bus Isolation mode (BI-mode ®)*





Description

The SVME/DMV-739 Intelligent Serial Communications Controller is a powerful communications controller which provides six full duplex serial ports. Two 68302 Integrated Multiprotocol Processors (IMPs) provide 12 DMA channels to handle the serial data and

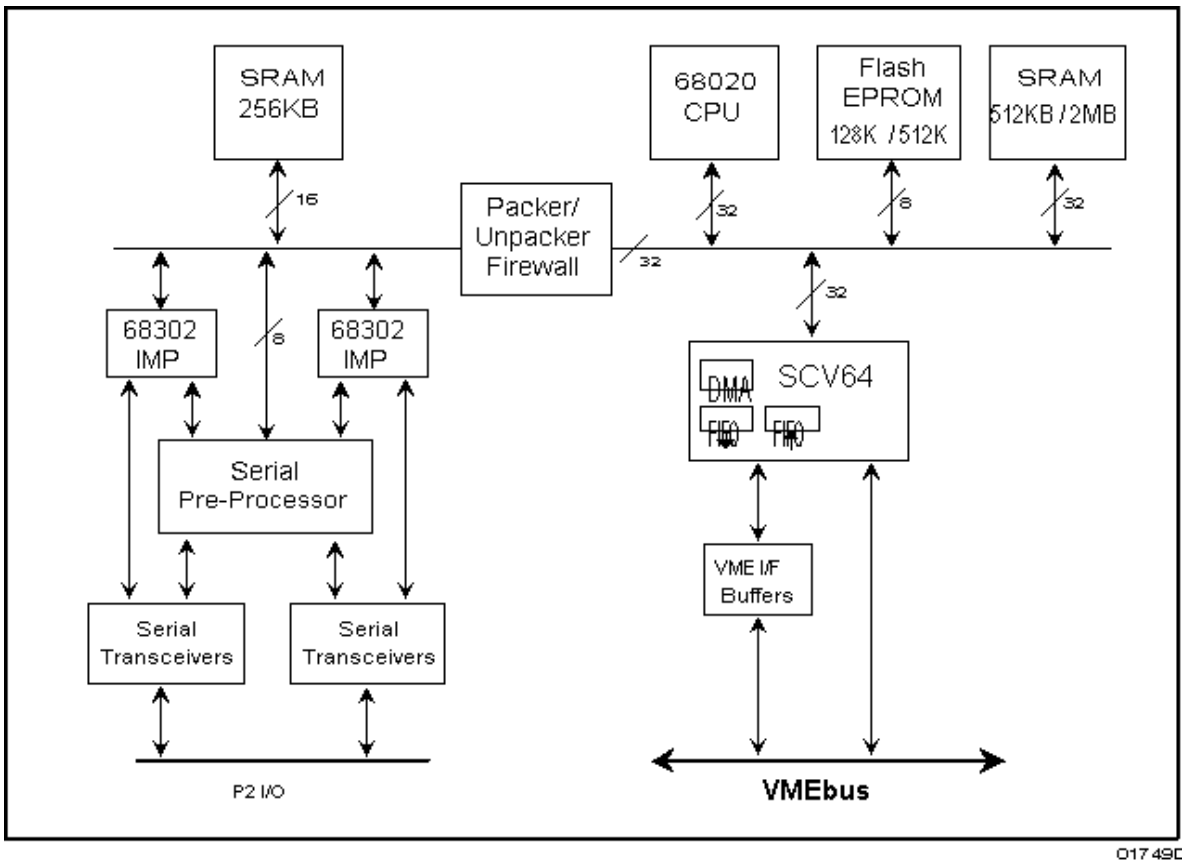


Figure 1: SVME/DMV-739 ISCC Block Diagram

two independent DMA channels for data movement within the serial data memory. The IMPs are provided with 256K bytes of SRAM. The 68020 CPU is provided with 512K bytes of SRAM in four 32-pin JEDEC sites and 256K bytes of Flash EPROM in one 32-pin JEDEC site. Future expansion allows for 2M bytes of SRAM and 512K bytes of Flash EPROM. The CPU is isolated from the serial data memory by a firewall, allowing the IMPs to operate without impeding CPU performance.

Figure 1 provides a functional block diagram of the SVME/DMV-739 Serial Communications Controller.

The card also supports DY 4 Systems' common features such as a location monitor, BIT, BI-mode®, and Auto-ID.

DY 4 Systems' common features support diagnostics, inter-processor communications, and logistics maintenance on-line. Built-In-Test (BIT) provides hardware features to verify all operational circuit blocks on the module. Bus Isolation mode (BI-mode) provides a means to electrically isolate the module from the VMEbus. The location monitor provides a fast, efficient means of inter-processor mailbox message passing to minimize software overhead in real-time operations. Auto-ID allows systems software to determine the physical location of all modules in a system on-line minimizing sparing and system configuration issues on-line. These features allow the users to perform fault detection and isolation during operation to build fault-tolerant systems. In addition, they allow for on-line maintenance and system configuration control to minimize field maintenance, repair time, and sparing logistics.

CPU Memory

One 32-pin JEDEC standard Flash™ EPROM device is provided. The EPROM operates at 3 wait states. To facilitate the use of the SVME/DMV-739 Serial Communications Controller in severe vibration environments where all components must be soldered, the Flash™ EPROM may be programmed on-board via the local CPU. This simplifies the installation of application code and makes on-site firmware upgrades possible.

There are 512K bytes of 32-bit-wide dual-ported static RAM provided. The dual-port SRAM array operates at 1 wait state to the local CPU. The memory design supports up to 2M bytes of SRAM.

The SVME/DMV-739 Serial Communications Controller is also equipped with 512 bytes of EEPROM. The EEPROM is accessed serially and provides a convenient method of storing system configuration data.

IMP Memory

The IMPs share a 256K byte bank of SRAM. The SRAM array operates at 0 wait states for IMP accesses. The IMPs have priority over the CPU/SCV64 for access to the serial data memory. Additional wait states are seen by any cycle master if a cycle is already in progress.

VMEbus Interface

The VMEbus interface of the SVME/DMV-739 ISCC is implemented with DY 4's Single Chip VMEbus Interface, (SCV64), which provides all the elements of a complete VMEbus interface. The philosophy of the SCV64 design is to provide programmable features that eliminate the need for jumpers, thereby simplifying logistics and reducing sparing requirements. The SCV64 incorporates the following:

- System Controller
- Master/slave A64:D64 interface
- Tx and Rx FIFO's to decouple bus operations
- Location monitor with FIFO message queue
- Interrupter, interrupt handler
- Extensive Built-in-Test support

The SCV64 provides all VMEbus system controller and interrupt functions. It allows for full programmability of requester modes and levels, arbiter modes, bus timers, interrupt levels and vectors. The SCV64 also features extensive BIT features and BI-mode®

A primary function of the SCV64 is to allow the CPU to access the VMEbus, and to allow the VMEbus to access on-board memory. The SCV64 contains transmit and receive FIFO's which are used to implement a store-and-forward technique of bus decoupling. SCV64-equipped CPUs can write to VMEbus locations without incurring a delay while the VMEbus is requested, arbitrated, and the bus grant received. For moving large blocks of data between on-board memory and the VMEbus, the SCV64 provides an integral DMAC. Bi-directional transfers can be configured to occur in discrete, block, or multiplexed block (D64) mode. Real throughput of up to 60M bytes/sec may be achieved.

To support inter-processor message passing, the SCV64 provides a location monitor (LM) with a built-in FIFO message queue. A write access to the LM results in capture of the data, and causes an interrupt to the CPU. The message queue is organized as a 32-bit wide FIFO with 31 entries.

Serial Ports

The SVME/DMV-739 Intelligent Serial Communications Processor provides six output channels. Each channel can be configured to have either EIA-422 or EIA-423 outputs. The EIA-423 interface allows interoperability with EIA-232 interfaces. In addition, two channels can be selected to operate as EIA-485 for multi-drop communications systems. The EIA-422 interfaces can be tri-stated under software control, permitting them to also be used in multi-drop situations. The configuration of each channel is selected by software. Table 1 details the signals that are available for each channel. Table 2 describes the electrical interface that is available for

each channel. The baud rate for each port is programmable for rates up to 333K baud in asynchronous mode and up to 1.6M bps in synchronous mode.

Serial Pre-Processor

The SVME/DMV-739 Intelligent Serial Communications Processor incorporates a programmable logic device that is used to extend the capabilities of the 68302 IMPs. The standard device provides FM0 data encoding. Other functions such as FM1 and Manchester encoding can be achieved with a customized variant. The serial pre-processor offers great flexibility for addressing particular customer requirements, where the SVME/DMV-739 is to be used to interface with a non-standard serial protocol. Consult the factory for information.

DMA Controller

There are 12 DMA channels which provide a DMA facility for Transmit and Receive on each of the serial ports. These DMA channels access the on-board memory and the serial communications device. Two independent DMA channels are provided for memory-to-memory data transfers.

Table 1
SVME/DMV-739 ISCC Signal Configuration

	Channels					
Signal	**1**	**2**	**3**	**4**	**5**	**6**
TxD	●	●	●	●	●	●
TxClk	●	●	●	●	●	●
RxD	●	●	●	●	●	●
RxClk	●	●	●	●	●	●
DCD	●					
DTR	●					
DSR	●					
RTS	●	●1	●1	●	● 1	● 1
CTS	●	● 2	● 2	●	● 2	● 2

Notes:

1. RTS can be selected instead of TxClk.
2. CTS can be selected instead of RxClk.
3. RxClks are all inputs, TxClk can be programmed to be driven from RxClk.
4. TxClks are outputs. On channels 1 and 4 TxClk may be input for EIA-485 operation.

Table 2
Electrical Interfaces

	Channels					
Interface	**1**	**2**	**3**	**4**	**5**	**6**
EIA-422	●	● 3	● 3	●	● 3	● 3
EIA-423	●	●	●	● 2	●	●
EIA-485	● 1			● 1		

Notes:
1. EIA-485 interface for signals TxD, TxClk, RxD, RxClk.
2. TxClk is not available in EIA-423 on channel 4.
3. EIA-422 interfaces on channels 2,3,5,6 can be tri-stated for party line applications.

Supported Firmware

The SVME/DMV-739 Serial Communications Controller provides the following firmware:

- General Purpose Monitor (GPM) - provides comprehensive monitoring and debug functions for the system integrator (refer to General Purpose Monitor, document number MS00053)
- Card Level Diagnostics (CLD) - provides diagnostic routines which perform a self-test function in conjunction with the Built-In-Test equipment (refer to Card Level Diagnostics, document number MS00050)
- Card Support Services (CSS) - provides a common software interface to the hardware features on the card, device independent I/O functions generic exception processing routines, and Auto-ID services (refer to Card Support Services, document number MS00180)
- Execution Sequencer (ES) - controls the invocation order of the Software Configuration Items on the card (refer to Execution Sequencer, document number MS00181)
- Data Link Communication Suite (DLCS) - provides SDLC™ , X.25 LAPB, and asynchronous services. Support for multiple host sessions. (refer to DLCS, document number MS00200)

Accessories/Variants

The SVME/DMV-739 is available in varying configurations to match the features, performance and ruggedizaton required for the target application. Additional items to assist in software development and system integration are available. The SVME/DMV-739 options and accessories consist of:

- memory type and speed
- customized serial pre-processor functions/algorithms
- P2 I/O cable for development system use
- FlashProg Flash EPROM programming utility
- VxWorks Board Support Package

The SVME-739 cards are available in ruggedization levels 0 to 3, and the DMV-739 cards are available in levels 2 and 3.

Table 3
Specifications

ENVIRONMENTAL SPECIFICATIONS		
Temperature	**(Level 0)**	
Operating	0°C to 50°C	MIL-STD-810
Storage	-40°C to 85°C	Methods 501.3 & 502.3
Temperature	**(Level 1)**	
Operating	-40°C to 85°C	MIL-STD-810
Storage	-40°C to 85°C	Methods 501.3 & 502.3
Temperature	**(Levels 2, 3)**	
†Operating	-55°C to 85°C	MIL-STD-810
Storage	-62°C to 125°C	Methods 501.3 & 502.3
Humidity (DMV CCA and SVME CCA - Levels 1,3)		
Operating	0 to 95% non-condensing	MIL-STD-810
Non-Operating	0 to 100% condensing	Method 507.3
Vibration (DMV)		
Sine	5g at 15 to 2,000 Hz	MIL-STD-810
Random	$0.1g^2/Hz$	Method 514.4
Shock (DMV)	40g/11ms half sine	MIL-STD-810 Method 516.4, Proc 1
Altitude (DMV)	21,350m (70,000 ft)	MIL-STD-810 Method 500.3

DIMENSIONS	**DMV CCA**	**SVME CCA**
Height	233.4 mm (9.2 in.)	233.4 mm (9.2 in.)
Depth	160 mm (6.3 in.)	160 mm (6.3 in.)
Thickness	15.0 mm (0.6 in.)	20.0 mm (0.8 in.)
Weight	<900g (<2 lb)	<570g (<1.28 lb)

POWER REQUIREMENTS		
+5v (+5%, -2.5%)	2.5 A (maximum)	1.8 A (typical)
+12v (+5%, -2.5%)	10 mA (maximum)	5 mA (typical)
-12v (+5%, -2.5%)	75 mA (maximum)	50 mA (typical)

† As a general design objective, the junction temperature of all components on the DMV-739 ISCC is limited to 110°C maximum (when the chassis cold-wall temperature is 85°C.) When reliability or performance factors permit, a component's junction temperature may exceed 110°C marginally.

SVME board operating temperature is based on air flow of 11 cfm.

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