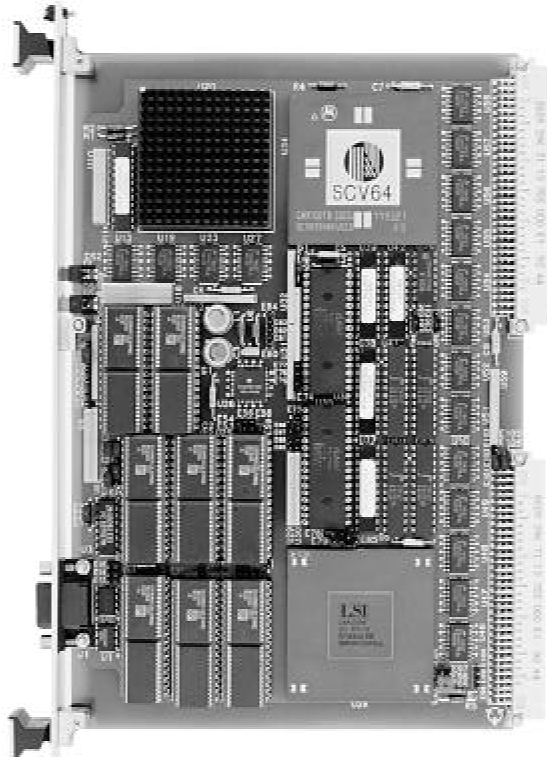
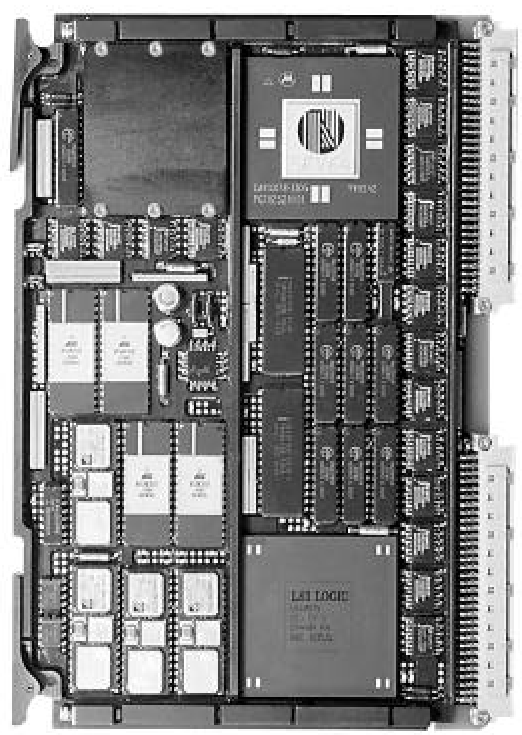
SVME/DMV-160

68040 Single Board Computer (SBC)

Features

- *68040 CPU at 25 MHz*
- *Ten 32-pin JEDEC sites for:*
  - *Capacity for a maximum of 4M bytes RAM and 1M byte PROM*
  - *Four 32-pin JEDEC sites for SRAM*
  - *Four 32-pin JEDEC sites for SRAM, Flash™ EPROM, or EEPROM*
  - *Two 32-pin JEDEC site for Flash™ EPROM or EEPROM*
- *Off-card battery back-up for SRAM*
- *512 byte serial EEPROM*
- *Advanced VME Interface Chip (SCV64)*
  - *A32:D32 VMEbus interface with A64:D64 MBLT support per ANSI/VITA 1-1994, VME64*
  - *Location monitor with FIFO buffer*
  - *Bus Isolation mode (BI-mode®)*
  - *Auto-ID and Auto-SYSCON*
  - *System controller functions*
- *VSB or Parallel interface options*
  - *on-board programmable VSB or Parallel interface*
  - *32-bit VSB master/slave interface*
- *Three 16-bit cascadable counter/ timers*
- *Two EIA-423-compatible serial channels*
- *Three general purpose P2 I/O lines*
- *Real-Time Calendar Clock (RTCC)*
- *Tick and watchdog timers*
- *Built-In-Test (BIT)*
- *Foundation firmware including:*
  - *Debug monitor*
  - *Diagnostics*
  - *Card Support Services*
  - *Execution Sequencer*
- *Conduction cooled per IEEE 1101.2 (0.65-inch pitch) for MIL-E-5400/4158, and MIL-STD-2036 applications*
- *Optional levels of ruggedization available*





SVME/DMV-160

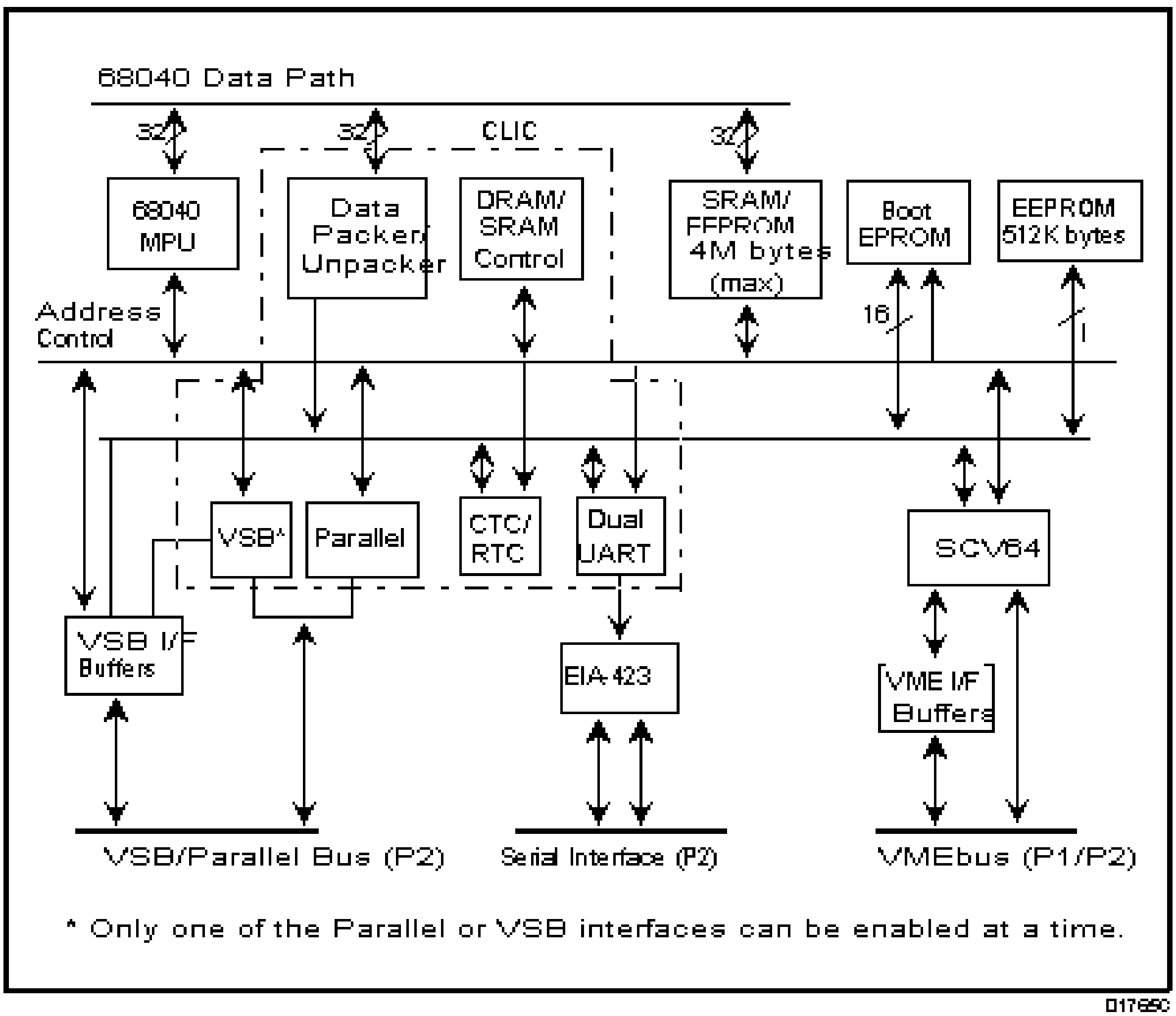
Description

The state-of-the-art SVME/DMV-160 SBC incorporates the latest technology, combining a high-performance, 25 MHz 68040 processor and up to 4M bytes of memory on one VME/VSB-compatible circuit card. Some of the important utility features found on the SVME/DMV-160 SBC include two serial ports, RTCC, and ten 32-pin JEDEC sites. Figure 1 shows a block diagram of the SVME/DMV-160 SBC. The SVME/DMV-160's design features address mission-critical demands of military and aerospace systems integrators with increased computing performance, self-test coverage and functional density.

The card supports DY 4 Systems' common features including an AVICS-based VMEbus interface, Built-In-Test (BIT), BI-mode®, location monitor, and Auto ID. These features bring benefits in performance, logistics and maintenance.

Figure 1: SVME/DMV-160 SBC Block Diagram

DY 4's custom-designed SCV64 chip implements all VMEbus interface functions with software-programmable features. It combines low-latency access to the VMEbus with high sustained throughputs. Built-In-Test (BIT) hardware features verify all operational circuits on the module. Bus Isolation mode (BI-mode®) increases ease of testing and system fault location. The location monitor supports efficient interprocessor messaging, to minimize overhead in real-time software.



Auto-ID allows boards to be self-configuring, based on slot location.

These features allow users to:

- build high-performance multi-processor systems
- detect and isolate faults during operation
- minimize field maintenance and sparing logistics.

All versions of the SVME/DMV-160 are functionally identical. SVME versions for use in air-cooled environments are available in DY 4 ruggedization levels 0, 2 and 3.

The conduction-cooled DMV version is designed for airborne, land-mobile, and naval military applications where circuit cards are sealed in a chassis to prevent moisture, salt-fog, sand, and dust contamination. DY 4 Systems' conduction-cooled products are designed for severe environmental conditions defined by MIL-E-4158, MIL-E-5400, and MIL-STD-2036. A single-piece aluminum thermal plane bonded to the PWB conducts heat away from the electronics. Its integral stiffening ribs improve heat dissipation and vibration resistance. Standard wedgelock fasteners give a reliable thermal connection to the chassis.

CPU

The 68040 CPU is a high-performance, 32-bit microprocessor from Motorola's third generation of the M68000 family. It is a virtual memory microprocessor using multiple, concurrent execution units and a highly integrated architecture. The 68040 CPU integrates the following:

- 68030-compatible integer unit
- 68881/68882-compatible Floating Point Processor (FPP)
- dual independent demand-paged Memory Management Units (MMU) for instruction and data stream accesses
- 4K-byte instruction cache
- 4K-byte data cache.

Memory

The memory configuration of the SVME/DMV-160 SBC uses ten 32-pin JEDEC sites for all memory. It supports the following memory configurations.

There are three banks of memory; two banks have four 32-pin JEDEC sites and the third bank has two 32-pin JEDEC sites. Bank 0 is installed with SRAM devices, Bank 1 can be populated with SRAM, Flash™ EPROM, or EEPROM, devices, and the third bank (the Boot PROM), can be installed with Flash™ EPROM, or EEPROM devices. The SVME/DMV-160 SBC supports the use of the VMEbus +5V STDBY line to power the SRAM in Bank 0. This preserves the volatile memory contents during loss of main power.

The SVME/DMV-160 SBC provides a maximum of 4M bytes of SRAM accessible from the on-board CPU, VSB and the VMEbus. The memory interface design supports the 68040 burst bus. This optimizes the memory bandwidth for access from the CPU, VMEbus or the VSB to minimize interference between contending sources.

The first cycle of a 4-cycle burst read is completed in a minimum of three clock periods, the remaining three cycles are completed in two clock periods each (referred to as a 3/2/2/2 burst). Random reads require three clock periods.

Table 1 summarizes the memory configurations for the SVME/DMV-160 SBC.

The SVME/DMV-160 SBC also has 512 bytes of serial EEPROM for storing configuration data.

VME Interface

The VMEbus interface of the SVME/DMV-160 SBC is implemented with DY 4's Single Chip VMEbus Interface, (SCV64), which provides all the elements of a complete VMEbus interface. The philosophy of the SCV64 design is to provide programmable features that eliminate the need for jumpers, thereby simplifying logistics and reducing sparing requirements. The SCV64 incorporates the following:

- System Controller
- Master/slave A64:D64 interface
- Tx and Rx FIFO's to decouple bus operations
- Location monitor with FIFO message queue
- Interrupter, interrupt handler
- Extensive Built-in-Test support

The SCV64 provides all VMEbus system controller and interrupt functions. It allows for full programmability of requester modes and levels, arbiter modes, bus timers, interrupt levels and vectors. The SCV64 also features extensive BIT features and BI-mode®

A primary function of the SCV64 is to allow the CPU to access the VMEbus, and to allow the VMEbus to access on-board memory. The SCV64 contains transmit and receive FIFO's which are used to implement a store-and-forward technique of bus decoupling. SCV64-equipped CPUs can write to VMEbus locations without incurring a delay while the VMEbus is requested, arbitrated, and the bus grant received.

Table 1
Byte-Wide Memory Configurations

Parameter	Bank 0	Bank 1	Boot PROM	Total
Data Width	32 Bits	32 Bits	16 Bits	
Memory Type				
SRAM	2M bytes 1M byte 512K bytes	2M bytes 1M byte 512K bytes		up to 4M bytes
Flash™ EPROM		2M bytes 1M byte 512K bytes	1M byte 512K bytes 256K bytes	up to 3M bytes
EEPROM		2M bytes 1M byte 512K bytes 128K bytes	1M byte 512K bytes 256K bytes 64K bytes	up to 3M bytes
EPROM		4M bytes 2M bytes 1M byte 512K bytes 128K bytes	2M bytes 1M byte 512K bytes 256K bytes 64K bytes	up to 6M bytes

CLIC

The Common Logic Integrated Circuit (CLIC) is a DY 4-designed ASIC that performs a number of utility functions for the circuit card. These functions consist of:

- dynamic bus sizing
- two serial interfaces
- Real-Time Calendar Clock (RTCC)
- VSB interface/Parallel I/O
- counter/timers
- memory control
- general purpose I/O.

Dynamic bus sizing allows software to be written without concern for the physical hardware configuration. Applications code can use 32-bit accesses to access non-32-bit ports. This is accomplished transparently. This dynamic bus sizing is compatible with the bus sizing provided on 68020/68030 processors.

The CLIC also provides three 16-bit counter/timer channels for general purpose timing. All of these channels are cascadable under software control. Timing ranges from less than 1 µs to greater than 2 seconds.

Serial Interface

The serial interface in the CLIC provides for two asynchronous serial channels. Each channel uses an EIA-423 interface. This permits communication with EIA-423, EIA-422, and EIA-232 interfaces. Baud rates are programmable from 150 to 38.4K baud. Interrupts are also programmable under software control.

Real-Time Calendar Clock (RTCC)

The on-chip RTCC provides for time-of-day calculation. It consists of registers for year, month, day, day-of-week, and seconds through to hundredths of seconds, and interrupt controls. Leap-year and days per month are automatically updated. The RTCC is capable of periodic or alarm/wake-up interrupts to the MPU.

VSB Interface

The SVME/DMV-160 SBC is equipped with a VME Subsystem Bus (VSB) master/slave interface offering the following features:

- 8-, 16-, and 32-bit data transfers
- assertion of LOCK* signal to effect indivisible TAS, CAS, and CAS2 instructions
- serial arbitration
- polled interrupt handler
- auto SYSCON detection.

The VSB interface is on the P2 connector.

Parallel Interface

The SVME/DMV-160 SBC's general purpose parallel port has the following features:

- Two modes of operation.
- Mode 1 provides 4 inputs, 3 outputs, and an 8-bit port configurable as input or output
- Mode 2 provides 3 inputs, 4 outputs, and an 8-bit port configurable as input or output
- 48 mA open collector TTL outputs.

The SVME/DMV-160 SBC can be configured to enable either the Parallel or VSB interface. This is determined by a combination of a hardware jumper and software initialization of the CLIC. The jumper protects against erroneous software selection.

System Status Interface

System status signals provided on the P2 connector allow interfacing to a test connector when the card is installed in a sealed conduction-cooled chassis.

One signal, CARDFAIL, asserts during fail conditions equivalent to the front panel FAIL LED. The VME SYSFAIL signal is also asserted during fail conditions. The other signal, CARDSTAT, asserts equivalent to the front panel status LED.

Foundation Firmware

The SVME/DMV-160 SBC is supplied with a foundation firmware package. This package consists of the following:

- General Purpose Monitor (GPM) - provides comprehensive monitoring and debug functions for the system integrator (refer to General Purpose Monitor, document number MS00053)
- Card Level Diagnostics (CLD) - provides diagnostic routines which perform a self-test function in conjunction with the Built-In-Test equipment (refer to Card Level Diagnostics, document number MS00050)
- Card Support Services (CSS) - provides a common software interface to the hardware features on the card, device independent I/O functions generic exception processing routines, and Auto-ID services (refer to Card Support Services, document number MS00180)
- Execution Sequencer (ES) - controls the invocation order of the Software Configuration Items on the card (refer to Execution Sequencer, document number MS00181).

Accessories/Variants

The SVME/DMV-160 SBC is available in varying configurations to match the features, performance and ruggedizaton required for the target application. Additional items to assist in software development and system integration are available. The SVME/DMV-160 SBC options and accessories consist of:

- SRAM capacity from 512K bytes to 4M bytes
- PROM memory type and size
- P2 I/O cable for development system use
- FlashProg Flash EPROM programming utility
- VxWorks Board Support Package

The SVME-160 cards are available in ruggedization levels 0, 2 and 3. The DMV-160 cards are available in levels 2 and 3

Table 2
Specifications

ENVIRONMENTAL SPECIFICATIONS		
Temperature	**(Levels 0)**	
†Operating	0°C to 50°C	MIL-STD-810
Storage	-40°C to 85°C	Methods 501.3 & 502.3
Temperature	**(Levels 2,3)**	
†Operating	-55°C to 85°C	MIL-STD-810
Storage	-62°C to 125°C	Methods 501.3 & 502.3
Humidity (DMV CCA and SVME CCA - Level 3)		
Operating	0 to 95% non-condensing	MIL-STD-810 Method 507.3
Non-Operating	0 to 100% condensing	
Vibration (DMV CCA)		
Sine	5g at 15 to 2,000 Hz	MIL-STD-810 Method 514.4
Random	0.1g^2/Hz	
Shock (DMV CCA)		
	40g/11 ms half sine	MIL-STD-810 Method 516.4, Proc 1
Altitude (DMV CCA)		
	21,350m (70,000 ft)	MIL-STD-810 Method 500.3

PHYSICAL DIMENSIONS	**DMV CCA**	**SVME CCA**
Height	233.4 mm (9.2 in.)	233.4 mm (9.2 in.)
Depth	160 mm (6.3 in.)	160 mm (6.3 in.)
Thickness	15.0 mm (0.6 in.)	20.0 mm (0.8 in.)
Weight	<700g (<1.54 lb)	<570g (<1.28 lb)

POWER REQUIREMENTS		
+5v (+5%, -2.5%)	5.5 A (maximum)	3 A (typical)
+12v (+5%, -2.5%)	16 mA (maximum)	8 mA (typical)
-12v (+5%, -2.5%)	16 mA (maximum)	8 mA (typical)

† As a general design objective, the junction temperature of all components on the DMV-160 SBC is limited to 110°C maximum (when the chassis cold-wall temperature is 85°C.) When reliability or performance factors permit, a component's junction temperature may exceed 110°C marginally.

SVME board operating temperature is based on air flow of 11 cfm.

SVME/DMV-160

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