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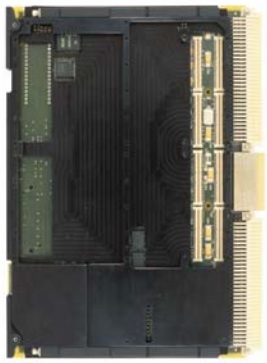
PRODUCT DATASHEET



# SVME/DMV-181

## PowerPC™ 7410 Single Board Computer with Dual PMC Interfaces

## Features



- PowerPC ™ 7410 (AltiVec Technology ™-enhanced) CPU
- CPU core frequency up to 500 MHz
- 100 MHz system bus and SDRAM frequency
- 512 Mbytes, or 1 Gbyte of Synchronous DRAM with ECC
- 2 Mbytes of L2 cache memory
  - Cache may be configured as direct-mapped SRAM
- Peak processor-memory bandwidth of 800 Mbytes/sec; peak L2 cache bandwidth of 1.143 Gbytes/sec
- 48 or 128 Mbytes of direct memory-mapped Flash
  - hardware write protection provided
- Permanent Alternate Boot Site (PABS) provides backup boot capability
- 32 Kbytes of AutoStore nvSRAM
- 512 bytes of Serial EEPROM
- Dual 64-bit PCI local buses, 528 Mbytes/sec peak data transfer rate
- Two 64-bit PMC sites for high-performance I/O expansion
  - One 66/33 MHz capable, the other 33 MHz capable
- Two 10/100BaseTX (twisted pair) Ethernet ™ ports
- 8- or 16-bit Ultra SCSI interface
- Two EIA-232 serial ports
- Up to four HDLC/SDLC-capable EIA-422/485 serial channels, each with full DMA support
- Two USB 1.1 interfaces
- 16 bits of discrete TTL I/O, each with interrupt capability
- Up to 16 bits (8 in, 8 out) of RS-422/485 differential discrete I/O, with interrupt on inputs
- Eight 32-bit general purpose timers
- Three 16-bit system timers
- Avionics-style watchdog timer with software programmable upper and lower bounds
- Real Time Clock with automatic +5V/+5V STDBY switchover
- Four general-purpose PCI DMA controllers
- Tundra Universe II ™ VME64 master/slave interface with VME DMA
- Support for VME64x geographic addressing
- Comprehensive Foundation Firmware with:
  - debug monitor and non-volatile memory programmer
  - suite of card support service routines
  - BIT firmware with 95%fault coverage
  - Ethernet connection option
- INTEGRITY Board Support Package from Green Hills Software (see separate datasheet for details)
- LynxOS ™ 4.0 reference port (see separate datasheet for details)
- TimeSys Linux Support Package from TimeSys (see separate datasheet for details)
- VxWorks ® /Tornado BSP and Driver Suite (see separate datasheet for details)

(feature list continued on following page)



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- IXLibs-AV AltiVec-optimized DSP Library (see separate datasheet for details)
- Occupies single .8 ” slot in all configurations
- Baseboard card uses +5 V only, backplane 3.3 V, 5 V and ±12 V are routed to the PMC sites
- Low-power design using switching regulator technology
- Optimum conduction-cooling with TherMax™ thermal frame
- Supported by a network of regional Field Application Engineers and a staff of factory-based Customer Support specialists
- Available in a range of ruggedization levels, both air and conduction-cooled

## Overview

The SVME/DMV-181 single board computer combines a processing core based on the powerful AltiVec-equipped PowerPC 7410 processor with an unmatched I/O complement highlighted by dual 10/100Base-T Ethernet ports, 6 serial channels, and two USB ports. Jam-packed with features to satisfy the real-world requirements of defense/aerospace systems integrators around the globe, the SVME/DMV-181 is designed with performance, reliability, and ease of use in mind. The SVME/DMV-181 delivers a complete hardware, software, and support-ware solution that is ready for the challenges of avionics, tactical ground vehicle, and rugged naval applications.

For retrofit and technology insertion applications, the SVME/DMV-181 offers a superset of the I/O features of earlier generations of our PowerPC SBCs and optional pin-out modes for backplane compatibility as well. As a member of our continuously evolving stream of PowerPC SBCs including the popular SVME/DMV-179, the SVME/DMV-181 supports the life-cycle model of successive technology insertions throughout a platform’s lifetime.

## Architecture Based on Advanced Processor and Multiple Independent 64-bit Busses with Crossbar Fabric

Figure 1 illustrates the architecture of the SVME/DMV-181. The level 2 (L2) cache connects directly to the processor via the back-side 64-bit L2 cache bus of the 7410 processor. A powerful GT-64260 Discovery™ system controller bridges the processor MPX bus to the SDRAM bus, two 64-bit PCI busses, and a high-performance device bus on which the Flash EPROM and non-PCI peripherals are found. The powerful crossbar fabric internal to the Discovery device allows for concurrent data transfers to take place on the various busses of the ‘181. Examples of data transfers that can occur concurrently on the ‘181 include:

- processor accesses to Flash concurrent with PCI-SDRAM transfers on either PCI bus
- processor accesses to one PCI bus concurrent with PCI-SDRAM transfers on the other PCI bus
- processor accesses to on-chip peripherals (Ethernet and serial ports) concurrent with PCI-SDRAM transfers on either PCI bus

The SVME/DMV-181 provides hardware-enforced cache coherency with respect to accesses to SDRAM from PCI and bus-mastering peripherals.

The Discovery system controller provides a separate device bus for Flash and peripherals, thus the SDRAM bus is reserved expressly for SDRAM devices. This results in reduced bus loading on the SDRAM bus, allowing for higher speed operation.

The Board Controller FPGA provides the bridge between the Discovery device bus and the Flash and non-PCI peripherals and implements a number of SVME/DMV-181 features including interrupt control, system timers, watchdog timer, discrete I/O registers, and Auto-ID Support Register. To increase the serviceability of the ‘181 over the long life cycles of the military/aerospace programs for which it is designed, the Board Controller FPGA is In-System Programmable (ISP) and can be reprogrammed in the field.


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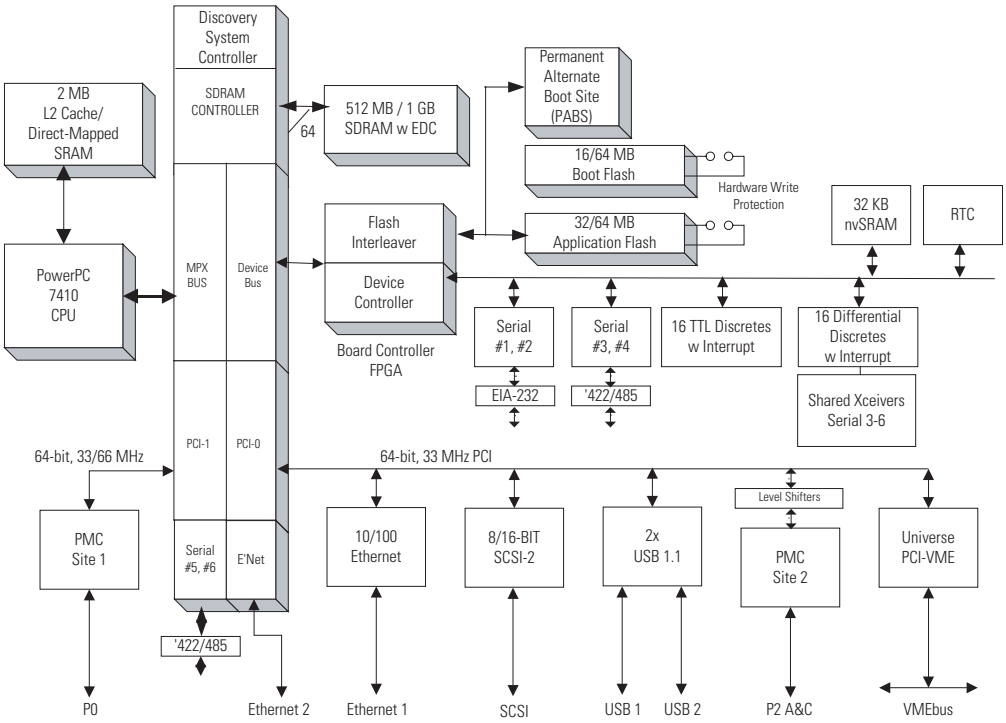



*Figure 1: SVME/DMV-181 Block Diagram (See Table 3 for I/O routing options)*

PCI bus 0 is a 64-bit, 33 MHz PCI bus providing a high-speed data path to the Universe™ PCI-VME bridge, the LSI Logic 53C885 10/100 Mbit/sec Ethernet/SCSI interface, the USB device, and PMC expansion site 2. PCI bus 1 is a 64-bit, 66 MHz PCI bus that is dedicated to PMC site 1. Offering a peak PCI transfer rate of 528 Mbytes/sec, PMC site 1 has the necessary bandwidth to support high performance PMC modules such as Fibre Channel NICs, graphics controllers, and custom high-speed interfaces.

The innovative use of high-efficiency switching regulators for all internal voltage requirements including 3.3V is integral to allowing all the functionality of the '181 to be powered by only 20 Watts (typical) of +5V power.

## Designed for Harsh Environments

To cost-effectively address a diverse range of military/aerospace applications, the SVME/DMV-181 is available in a range of ruggedization levels, both air- and conduction-cooled. All versions are functionally identical, with air-cooled versions (SVME) available in ruggedization levels 0, 100 and 200 and conduction-cooled versions (DMV) in levels 100 and 200. Our standard ruggedization guidelines define the environmental tolerance of each ruggedization level (see Ruggedization Guidelines data sheet for more information).

To ensure a long in-service life for the product, we carefully analyse the projected fatigue life of all solder joints and interconnections. The mounting of all components is reviewed to ensure that differential thermal expansion between the component and the Printed Wiring Board (PWB) does not unduly shorten the fatigue life of the solder joints.

In the particular case of ceramic Ball Grid Array (BGA) components, studies have shown that the large difference in coefficient of thermal expansion between the ceramic package and typical PWB materials leads to early joint breakage after temperature cycling unless special mounting provisions are used. To solve this problem we convert ceramic BGA components to Column Grid Array (CGA) components before soldering them to the board. The additional height of the column compared to a collapsed ball relieves temperature-induced stresses and avoids premature fatigue failures. This is a proven approach also used on the SVME/DMV-179 and SVME/DMV-178 PowerPC SBCs.

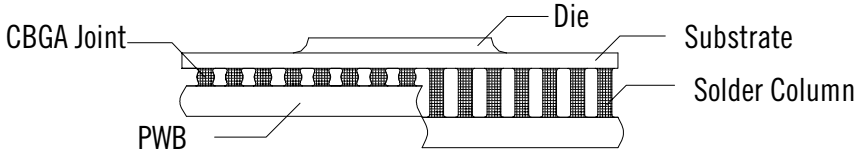



*Figure 2: Conversion of Ceramic Ball Grid Arrays (CBGA) to Ceramic Column Grid Arrays (CCGA)*

## Enhanced Thermal Management for Conduction Cooled Applications

Conduction cooling of the DMV-181 is performed by a combination of thermal management layers within the Printed Wiring Board (PWB) and an aluminum thermal frame that provides a cooling path for the PMC sites and for shunts to selected high-power components such as the processor and cache. To minimize the thermal resistance to the PMC sites and shunted high-power components, the DMV-181 employs an innovative thermal frame design approach termed TherMax. A TherMax™ thermal frame provides an unbroken metallic path from the PMC sites and shunted components to the back-side cooling surface of the card therefore minimizing the temperature rise to these devices.

The back side of a conduction-cooled VME card is the primary cooling surface due to the fact that the wedgelocks on the top side have a high thermal resistance. A typical thermal frame simply sits on top of the PWB and forces heat to flow through the PWB which has a high thermal resistance compared to aluminum.

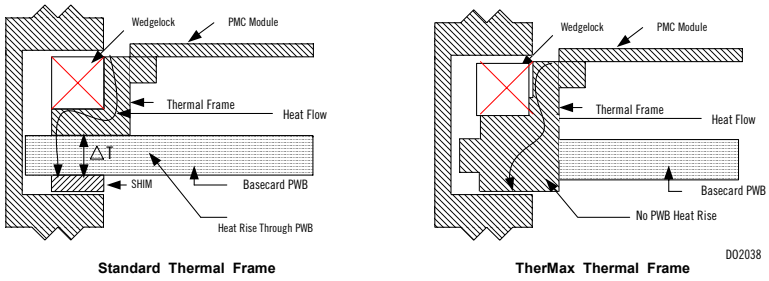



*Figure 3: .A TherMax thermal frame eliminates the PWB heat rise inherent in a standard thermal frame*

## Advanced 7410 PowerPC™ CPU

The SVME/DMV-181 is equipped with a high performance PowerPC 7410 CPU, a fourth generation member of Motorola®'s broad family of PowerPC family of 32/64-bit RISC microprocessors. Developed for a wide range of embedded computing applications, the 7410 provides industry-leading performance per watt. The '181's PowerPC processor runs at speeds of up to 500 MHz on-chip and offers estimated CPU benchmarks as shown in Table 1.

The 7410 processor incorporates Motorola's powerful AltiVec Technology, which enhances the PowerPC architecture through the addition of a 128-bit vector execution unit. The vector unit provides for highly parallel operations, allowing for the simultaneous execution of up to 16 integer operations or 8 floating point operations per clock cycle. At 500 MHz, this translates to a peak computational rate of 4.0 GFLOPS.

*Table 1: Device Manufacturer's Estimated Performance*

| Processor | SPECint95 | SPECfp95 |
|---|---|---|
| 7410 at 500 MHz | (1)22.8 | 17.0 |

(1) Motorola 7410 Fact Sheet, MPC7410FACT/D Rev. 0

## Two Mbytes of L2 Cache

The SVME/DMV-181 provides 2 Mbytes of L2 cache, implemented with synchronous burst RAM. Parity error detection is provided on the L2 data bus. Running at 142.9 MHz, the L2 cache bus is capable of a peak data transfer rate of 1.143 GBytes/sec. To provide more deterministic code execution times for repetitive algorithms, the 7410 processor can configure the L2 cache memory to be treated as high-performance direct-mapped SRAM. This provides software a straightforward way to load and maintain key code segments and associated data sets in high-speed memory.

## Up To 1 Gbyte of SDRAM

The main memory for the SVME/DMV-181 SBC is located entirely on the basecard with no need for extra mezzanine modules. The DRAM consists of either 512 Mbytes or 1 Gbyte of high performance synchronous DRAM (SDRAM). To preserve data integrity, the SDRAM is provided with Error Checking and Correcting (ECC) circuitry that detects and corrects all single-bit data errors, detects all double bit errors, and detects all three and four bit errors within the same nibble. With ECC enabled, the instantaneous peak data transfer rate to SDRAM is 800 Mbytes/sec.

The SDRAM is accessible from the processor and from both PCI busses. Via the Universe II™ PCI-to-VME interface device on PCI bus 0, the SDRAM is also accessible from the VMEbus.


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## Up To 128 Mbytes of Fast Flash Memory

The SVME/DMV-181 has the capacity for up to 128 Mbytes of contiguous, directly accessible, high-speed Flash memory.

To minimize system boot up time for applications such as avionics mission computers where fast restarts after power interruptions are critical, '181 users can run application code directly from Flash without first cross loading to DRAM. This is practical due to the high-performance architecture of the Flash array.

The Flash memory of the 181 is implemented two different ways depending on the version of the card. For versions of the 181 with 48 MB Flash, the Flash is implemented in three banks of 16 MB each using AMD 29DL323 devices. Bank 0 is considered to be the boot Flash as this is where the processor reset vector (0xFFF0_0100) is mapped. Banks 1 and 2 together are considered the application Flash. To provide accelerated bandwidth to Flash, logic within the Board Controller FPGA accesses the Flash banks 64 bits at a time and multiplexes the data onto the Discovery device bus.

For versions of the 181 with 128 MB Flash, the Flash is implemented in four 32-bit wide banks of 32 MB each using AMD 29PDL128G page mode devices. Bank 0 is the boot Flash, the other 3 banks together constitute the application Flash. The page mode capability of the Flash device allows for shorter access times for accesses that hit the same page as the previous access. The performance improvement is such that read performance with this Flash technology is similar to that of the 48 MB 181s with the 64-bit multiplexor.

Two separate software write protect bits are provided for enabling Flash reprogramming. One controls the boot Flash while the other controls the application Flash. To prevent inadvertent enabling, the two write protect bits are in separate registers.

For absolute protection against inadvertent Flash reprogramming or corruption, two hardware jumpers are provided to disable the Write Enable line to the Flash devices. As for the software write protect bits, one hardware write protect jumper is provided for the boot Flash while the other controls the application Flash. Cards are configured for shipment with Flash reprogramming enabled in hardware.

This logical separation of boot and application Flash minimizes accidental corruption of the boot firmware when reloading application code into Flash. However if desired, all but two Mbytes of the boot Flash can also be used for user code, at the expense of mixing boot firmware and user code in the same domain with respect to Flash write enabling.

Flash memory is reprogrammable using the Non-Volatile Memory Programmer (NVMP) utility (see NVMP data sheet) embedded into our standard foundation firmware. The Flash memory devices are specified for a minimum of 1,000,000 program-erase cycle and a data retention time of 20 years.

## Permanent Alternate Boot Site (PABS)

The PABS provides a backup boot capability in the event that the foundation firmware in the main boot bank (bank 0) becomes corrupted. This can occur because of an error during reprogramming or an incorrect image being loaded. The PABS provides users with a convenient mechanism to recover from corruption of the main boot bank without removing the card from the system in which it is installed. When a P0 backplane pin is asserted, the SVME/DMV-181 will boot from the PABS, and run a reduced-functionality version of our General Purpose Monitor which can then be used to restore the main Flash. For convenience in a development environment, there is an on-board jumper to force a boot from PABS.

## 32 KBytes of AutoStore nvSRAM

The AutoStore nvSRAM provides fast, non-volatile storage of mission state data that must not be lost when power is removed. During normal operation, application software reads and writes the AutoStore nvSRAM just like standard SRAM, with no special programming algorithm required. Upon detecting a power loss on the +5 V rail, an AutoStore cycle is performed and all 32 Kbytes are automatically transferred from the on-chip SRAM to the on-chip EEPROM using energy stored in an on-board capacitor. At the next power-up a recall cycle is performed to transfer the EEPROM contents back to the SRAM, where the application code can now utilize the stored data to continue normal operation. The number of recall cycles is unlimited: the maximum number of store cycles is 100,000 and the data retention period is 10 years.

## Serial EEPROM

The SVME/DME-181 provides 512 bytes of Serial EEPROM for storing configuration data used by card initialization firmware. User access to the Serial EEPROM is also provided.

## Two Ethernet™ Interfaces

The '181 is equipped with two IEEE 802.3-compliant 10BASE-T/100BASE-TX Ethernet interfaces. Ethernet 1 is implemented with an LSI Logic 53C885 SCSI/Ethernet device connected to PCI bus 0. A powerful chaining DMA controller and a 3 KByte FIFO for both



receive and transmit channels ensures efficient utilization of the PCI bus and minimal processor loading.

Ethernet 2 is implemented within the Discovery bridge device. The Discovery Ethernet unit integrates powerful DMA engines and an efficient buffer management scheme to keep processor overhead to a minimum.

On air-cooled cards Ethernet 1 is accessible from the front panel connector. See Table 3, '181 I/O Routing Options, for information on the routing of the Ethernet channels to backplane connectors.

## 8/16-Bit SCSI-2 Interface

The SVME/DMV-181 comes standard with a single-ended, 8-bit Ultra SCSI (SCSI-2) interface, based on the LSI Logic 53C885 SCSI/Ethernet controller. This configuration is capable of peak transfer rates on the SCSI bus of 20 Mbytes/sec in synchronous mode, or 7 Mbytes/sec asynchronous.

The '181 is also capable of providing 16-bit Ultra SCSI. See Table 3 in the I/O Routing Options section for information on I/O routing modes that provide 16-bit SCSI. In this configuration the device supports peak transfer rates of 40 Mbytes/sec synchronous and 14 Mbytes/sec asynchronous.

The SCSI controller of the 53C885 is highly autonomous and transfers data to and from SDRAM via an internal SCSI DMA controller and an associated 536-byte DMA FIFO, minimizing the loading of the main PowerPC processor by SCSI traffic. As a PCI master the 53C885 is capable of zero wait-state data bursts at 132 Mbytes/sec, conserving both PCI bus and main memory bandwidth.

The 181's SCSI interface includes a fuzed TERMPWR output and on-board terminators which can be enabled and disabled under software control.

## Two EIA-232 Serial Ports

Serial channels 1 and 2 are EIA-232 serial ports based on an Exar 16C2550 controller chip. An input clock of 1.8432 MHz allows for programmable asynchronous baud rates from 50 baud to 115.2 Kbaud. The baud rate of each port can be set independently. The DSR signal on serial channel 1 is used as a cable detect signal to force the card to boot into the General Purpose Monitor.

On air-cooled cards the two EIA-232 channels are accessible on the front panel in addition to being available on the rear-panel on both air- and conduction-cooled cards.

## Four EIA-422/485 Serial Ports

A total of four asynchronous and synchronous-capable EIA-422/485 ports are available on the SVME/DMV-181. Serial channels 3 and 4 are implemented with a Zilog 85C230 ESCC (Enhanced Serial Communications Controller). An input clock of 10 MHz provides for asynchronous communication at baud rates up to 153.6 Kbaud, and synchronous data rates up to 2.5 Mbps. To support high data rate applications without excessive loading of the PowerPC CPU, full DMA support is provided to the ESCC by four of Discovery's general-purpose DMA controllers.

Serial channels 5 and 6 are implemented with Discovery's Multi-Protocol Serial Controllers (MPSC). These powerful serial controllers handle standard asynchronous and synchronous HDLC/SDLC modes, and in addition provide a transparent mode. In synchronous mode a full range of data encoding schemes are supported (NRZ, NRZI Mark, NRZI Space, FM0, FM1, Manchester, and Differential Manchester). Based on an input clock of 100 MHz, all standard asynchronous baud rates up to 115.2Kbaud are provided as well as synchronous bit rates up to 10 Mbits/sec. The Discovery MPSC includes dedicated serial DMA controllers.

To support multi-drop or half-duplex operation, the output drivers (clock and data) of each channel can be disabled. At power-up the output drivers are enabled for EIA-422 compatibility.

See Differential Discrete I/O below for information on how the '181 provides the capability to control each of the RS-422/485 drivers and receivers as differential-mode discrete signals for use as serial control signals or general purpose I/O.

## Two USB 1.1 Ports

The SVME/DMV-181 incorporates an OPTi 82C861 PCI-to-USB device which provides a host controller and root hub driving two independent USB ports (total USB bandwidth 12 Mbits/sec nominal). One USB port is accessible on the front panel connector only, the other is accessible on the P0 connector only.

## 16 Bits of Discrete Digital I/O

The SVME/DMV-181 provides 16 bits of LVTTL-compatible discrete digital I/O. Each bit is individually programmable to be an input or output. In addition, each bit is capable of generating an interrupt upon a change of state, with the edge direction (high-to-low, low-to-high) also being programmable. On-board pull-up resistors are provided to allow direct connection to simple switch closure inputs. As outputs, the TTL discretes can sink 16 mA and source 12 mA.


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## Up to 16 Bits of Differential Discrete Digital I/O

The SVME/DMV-181 provides the capability to control each of the RS-422/485 drivers and receivers as differential-mode discrete signals via registers in the Board Controller FPGA. This allows flexibility in how the 8 drivers and 8 receivers are used. For instance, any Tx and Rx Clock signals that are not required on an asynchronous channel can be used as serial control signals (RTS, CTS, etc.,) for that channel or any other. Tx and Rx data signals from unused serial channels can be redeployed in the same way. In addition RS-422/485 drivers and receivers can also be used as general-purpose differential-mode control signals unrelated to serial I/O requirements. Differential discrete inputs can generate an interrupt upon a change of state, with programmable edge direction.

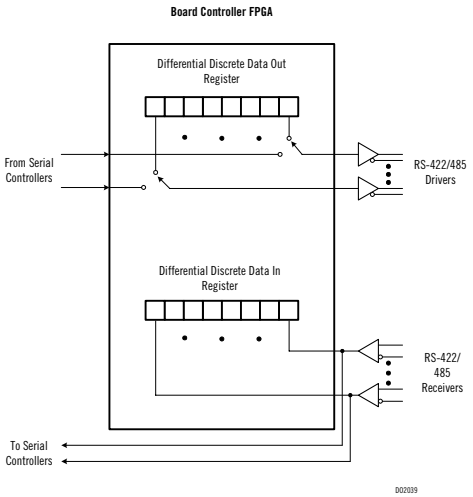



*Figure 4: Option for Discrete Control of RS-422/485 Drivers and Receivers*

## Real-Time Clock (RTC)

The RTC function is provided by a Dallas Semiconductor DS1685 real-time clock chip. It contains registers for century, year, month, day, day-of-week, and seconds. The RTC is capable of periodic and alarm/wake-up interrupts to the CPU.

The RTC draws its power from the standard +5 V input during normal operation. In the event of loss of +5 V power, the RTC will automatically switch over to draw current from the +5 V STDBY line.

## Extensive Timing Resources

The SVME/DMV-181 provides a large number of timing resources to facilitate precise timing and control of system events. The list of available timers is given in Table 2.


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## Avionics Watchdog Timer

The watchdog timer on the SVME/DMV-181 is a presettable down-counter with a resolution of 1 usec. Time periods from 1 usec to 16 seconds can be programmed. Initialization software can select whether a watchdog exception event causes an interrupt or a card reset. Once enabled to cause a reset, the watchdog cannot be disabled. A watchdog time-out log bit tells start-up code whether the last card reset was due to a watchdog exception.

The watchdog timer can be used in two ways. Used a standard watchdog timer, a single time period is programmed which defines a maximum interval between writes to the watchdog register. For increased system integrity, the watchdog can optionally be configured to operate in “Avionics” mode whereby a minimum interval between writes to the watchdog register is also enforced. I.e., writing to the watchdog register either too soon or too late causes an exception event.

*Table 2: SVME/DMV-181 Timing Resources*

| Timer Facility | Implementation | Type | Size | Tick Rate/ Period | Maximum Duration |
|---|---|---|---|---|---|
| Time Base Register | PowerPC | Free running counter | 64 bit | 25.0 Mhz/40.0 nsec. | 23,398 years |
| Decrementer | PowerPC | Presettable, readable downcounter | 32 bit | 25.0 Mhz/40.0 nsec. | 171.8 sec. |
| General Purpose #0-7 | Bridge chip | Presettable, readable downcounter with autoreload or stop options | 32 bit | 100.0 Mhz/10 nsec. | 42.95 sec. |
| RTC Periodic Interrupt | Real-time clock | periodic interrupt generator | - | from 122 usec. to 500 msec. by factors of two | 500 msec. |
| Watchdog Timer | FPGA | Presettable, readable downcounter with interrupt or reset on terminal count | 24 bit | 1 Mhz/1 usec. | 16.77 sec |
| System Timers #1-3 | FPGA | Presettable, readable, cascadeable, downcounters with interrupt on terminal count | 16 bit | 1 MHz/1 usec. | 65.5 msec. for single timer, 71.6 minutes for cascade of two, 8.9 years for cascade of three |

## Four General Purpose DMA Controllers

Four DMA controllers provided by the bridge chip are available for general purpose use. The four general purpose DMA controllers can be used for transferring blocks of data between the SDRAM, Flash memory, device bus peripherals, and the PCI busses without loading down the PowerPC CPU. The General Purpose DMA controllers are capable of sustaining burst transfers using the full 64-bit width of the PCI bus. Advanced features include DMA chaining and the ability to schedule DMA transfers via a general-purpose timer.

For transferring large blocks of data over the VMEbus, it is recommended that the DMA controllers internal to the Universe II device be used rather than the four general purpose DMA controllers. This is because the Universe II DMA controllers are capable of supporting maximum-size MBLT block sizes on the VMEbus.


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## VME Interface

The 64-bit PCI architecture of the SVME/DMV-181 combined with the Universe II's 64-bit PCI interface and extensive decoupling FIFOs allow for high-speed, bandwidth efficient data transfers between the VMEbus and on-board memory and PCI targets. VME data can be transferred at the full sustained rate of 50+ Mbytes/sec supported by the Universe II while only consuming only a fraction of the local PCI bus bandwidth of 264 Mbytes/sec.

Other key features of the '181's VME interface include:

- Full system controller capability with support for our own/ Tundra Auto-ID method
- Programmable DMA controller with linked list support
- Wide range of VMEbus address and data transfer modes;
  - > A32/A24/A16 master and slave, (not A64 or A40)
  - > D64/D32/D16/D08 master and slave, (no MD32)
  - > MBLT, BLT, ADOH, RMW, LOCK, and location monitors
- Four mailbox registers and four location monitors for inter-board communications and synchronization
- Nine programmable PCI-to-VME windows and four programmable VME-to-PCI windows
- Extensive support for Built-in-Test

The SVME/DMV-181 also provides support for five geographical addressing bits as defined by the ANSI/VITA 1.1-1997 (VME64 extensions) specification.

To preserve the Auto-ID context during a card-only reset from either the front panel or P0 input, the Board Controller FPGA contains an Auto-ID Support Register that remembers the Auto-ID results from the last power-up cycle. This value is used by foundation firmware after a card-only reset in order to set the card to the correct VME address.

## PCI Mezzanine Card (PMC) Expansion Sites

The functionality of the SVME/DMV-181 SBC can be substantially expanded via its two PMC sites. The two PMC sites interface to the outside world via 64-pins of back panel I/O per site. The placement of the PMC sites is such that a single, double width PMC module can also be fitted.

PMC site 1 (centre of card) is served by its own dedicated 64-bit, 66/33 MHz-capable PCI bus. Thus high-performance PMC modules such as networking modules or graphics modules can operate at 66 MHz independent of the speed at which the PMC module in PMC site 2 operates. PMC site 2 (bottom of card) is served by a 64-bit, 33 MHz PCI bus.

I/O routing is done in accordance with the IEEE P1386 specification, such that PMC site 1's I/O is routed to the P0 connector, while that of PMC site #2 is routed to A and C rows of the P2 connector. Front panel I/O is supported as a standard feature on air-cooled cards and, on a special order basis, for conduction-cooled cards. The SVME/DMV-181 conforms fully to the IEEE 1386/1386.1 requirement for a component keep-out area at the front of the PMC site for connectors or high components.

The 181 basecard drives 3.3V PCI signalling levels to both PMC sites at all times.

For PMC site 2, the Vio level is hard-wired to 5V. For PMC site #1 the selection of Vio is configurable, with a factory default of 5V. For "revision 3" boards (ones with 48 MB Flash), the Vio configuration is done with zero-ohm resistors. For "revision 4" boards (ones with 128 MB Flash), the Vio configuration is done with jumpers or wire-wrap.

For support of high-bandwidth PMC I/O signals such as Fibre Channel or digital video, both PMC site #1 and #2 are provided with five pairs of 150 ohm (nominal) differential impedance traces. Trace length is equalized within pairs.

## PMC Power Routing

The PMC sites are provided with 3.3V, +12V, and –12V power fron the VMEbus backplane. No 3.3V power is provided to the PMC sites by the regulators on the 181 basecard itself.

## Conduction-Cooled PMC Modules

To support the industry drive to open standards on conduction-cooled cards, the PMC site mechanical interfaces follow the VITA 20-2001 Conduction Cooled PCI Mezzanine Card draft standard. To optimize the thermal transfer from PMC modules to the base card the standard DMV-181 thermal frame incorporates both the Primary and Secondary thermal interfaces as defined by VITA 20-2001. See Figure 5 for a sketch of the thermal frame.


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To optimize the cooling of high-performance, high power PMCs such as our graphics modules, the DMV-181 thermal frame incorporates a mid-plane thermal shunt as illustrated in Figure 5. High power PMC's can include a mating cooling surface on the PMC module to contact the mid-plane thermal shunt. By taking advantage of the thermal shunt, suitably designed PMC modules can significantly lower the heat rise from the DMV-181 card edge to the PMC components. The mid-plane thermal shunt does not impinge on the VITA 20- specified component height.

The combination of the secondary thermal interfaces, the mid-plane thermal shunt, and our own unique TherMax™ thermal frame design provides optimum cooling for conduction-cooled PMC modules, allowing for higher power PMCs and/or increased long-term reliability through lower component temperatures.

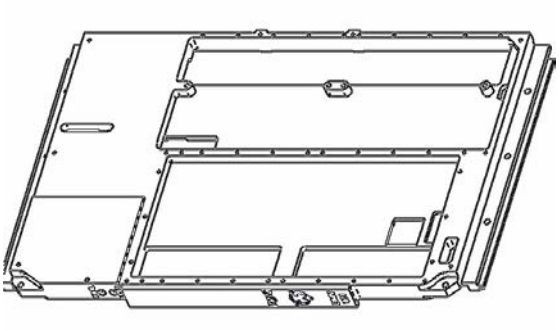


*Figure 5: Thermal Frame with VITA 20-2001 PMC Cooling Surfaces and Mid-Plane Thermal Shunt*

## Status Indicators and Controls

The SVME/DMV-181 SBC provides run/fail status by asserting a backplane signal and illuminating the red front panel LED in the event the diagnostics detect a card failure. There is also a software controlled green LED that the application can use to indicate status.

A card reset signal is available on the backplane connectors and on the front panel connector on air-cooled cards. The front panel and P0 break-out cables for the SVME-181 include a push button switch that interfaces to this signal to allow the card to be reset without doing a full system reset.

## COP and JTAG Test and Debug Interfaces

The Control and Observation Port (COP) of the PowerPC processor is accessible via the front panel on air-cooled cards. The COP interface is useful for software debug using a workstation tool such as Wind River's VisionICE emulation system.

To support factory acceptance testing the SVME/DMV-181 provides a JTAG scan chain that is accessible from a 5-pin header. The JTAG test chain coverage includes the processor, VMEbus interface chip, L2 cache, Discovery system controller, FPGA, FPGA Boot FLASH, SCSI/Ethernet, and USB. PMC modules are automatically added to the JTAG chain when present.


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# I/O Routing Options

To facilitate retrofit and technology insertion, the SVME/DMV-181 offers a superset of features and the option of pin-out compatibility with earlier generations of our PowerPC SBCs.

Table 3 shows the I/O routing for the SVME/DMV-181 in its native ('178/179-compatible) mode as well as its other modes.

*Table 3: SVME/DMV-181 I/O ROUTING OPTIONS*

| Mode | Description | Front Panel (air cooled only) | P0 Connector | P2 Rows A & C | P2 Rows D & Z |
|---|---|---|---|---|---|
| #1 | Standard 181 Configuration<br>(5-row P1/P2, 95-pin P0) | Ser 1, EIA-232<br>Ser 2, EIA-232<br>E'net 1 (LSI Logic)<br>USB 1<br>COP I/F<br>Ext card reset in | PMC Site #1 I/O<br>E'net 2 (disco)<br>16 discrete I/O<br>USB 2<br>Cardfail status out<br>Ext card reset in<br>ALT_BOOT input | PMC Site #2 I/O | E'net 1 (LSI Logic)<br>8-bit SCSI<br>Ser 1, EIA-232<br>Ser 2, EIA-232<br>Ser 3, EIA-422<br>Ser 4, EIA-422 |
| #2 | Optional 176/177 P0/P2 Compatibility Mode<br>(3-row backplane compatible) | Same as mode 1 | E'net 2 (disco)<br>8-bit SCSI<br>Ser 1, EIA-232<br>Ser 2, EIA-232<br>Ser 3, EIA-422<br>Ser 4, EIA-422<br>13 discrete I/O<br>USB 2<br>Ext card reset in<br>Cardfail status out<br>ALT_BOOT input | PMC Site #2 I/O | E'net 1 (LSI Logic)<br>8-bit SCSI<br>Ser 1, EIA-232<br>Ser 2, EIA-232<br>Ser 3, EIA-422<br>Ser 4, EIA-422 |
| #3 | Optional 176/177 P2-only Compatibility Mode<br>(3-row backplane compatible) | Same as mode 1 | P0 connector not installed | E'net 2 (disco)<br>8-bit SCSI<br>Ser 1, EIA-232<br>Ser 2, EIA-232<br>Ser 3, EIA-422<br>Ser 4, EIA-422<br>16 discrete I/O<br>Ext card reset in<br>Cardfail status out | E'net 1 (LSI Logic)<br>8-bit SCSI<br>Ser 1, EIA-232<br>Ser 2, EIA-232<br>Ser 3, EIA-422<br>Ser 4, EIA-422 |
| #4 | Optional 16-bit SCSI Mode | Same as mode 1 | PMC Site #1 I/O<br>E'net 2 (disco)<br>16 discrete I/O<br>USB 2<br>Cardfail status out<br>Ext card reset in<br>ALT_BOOT input | PMC Site #2 I/O | E'net 1 (LSI Logic)<br>16-bit SCSI<br>Ser 1, EIA-232<br>Ser 2, EIA-232<br>Ser 3, EIA-422<br>(no Tx Clk) |
| #6 | Optional 6-serial channel mode | Same as mode 1 | PMC Site #1 I/O<br>E'net 2 (disco)<br>16 discrete I/O<br>USB 2<br>Cardfail status out<br>Ext card reset in<br>ALT_BOOT input | PMC Site #2 I/O | E'net 1 (LSI Logic)<br>Ser 1, EIA-232<br>Ser 2, EIA-232<br>Ser 3, EIA-422<br>Ser 4, EIA-422<br>Ser 5, EIA-422<br>Ser 6, EIA-422 |
| #7 | Optional Full I/O mode | Same as mode 1 | PMC Site #1 I/O<br>E'net 2 (disco)<br>16 discrete I/O<br>USB 2<br>Cardfail status out<br>Ext card reset in<br>ALT_BOOT input | 16-bit SCSI | E'net 1 (LSI Logic)<br>Ser 1, EIA-232<br>Ser 2, EIA-232<br>Ser 3, EIA-422<br>Ser 4, EIA-422<br>Ser 5, EIA-422<br>Ser 6, EIA-422 |

Note 1: Optional I/O routings are controlled by factory-set configuration links. Boards with other than the standard mode #1 routing are built to order and set-up charges may apply.
Note 2: In all modes, the SVME/DMV-181 is equipped with 5-row P1 and P2 connectors.


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## Low Power Consumption

The application of advanced design techniques such as switching regulators for the 3.3 V and CPU core voltage requirements and maximum use of low power devices provides a low typical power of only 20 Watts for a fully populated basecard.

## Power Routing

The SVME/DMV-181 basecard uses only +5V and optionally +5V STDBY for the real-time clock. On-board regulators provide all necessary internal voltages. PMC sites are fed with +5 V, ±12 V, and 3.3V directly from the backplane.

## Mechanical Format

Conduction-cooled modules conform to the dimensions defined in IEEE 1101.2-1992, Standard for Mechanical Core Specifications for Conduction-Cooled Eurocards.

Air-cooled modules conform to the dimensions defined in ANSI/VITA 1-1994, American National Standard for VME64. Front panel hardware on air-cooled modules includes: injector/extractor handles, EMC strip, alignment pin, and keying provisions in accordance with ANSI/VITA 1.1, American National Standards for VME64 Extensions (and IEEE 1101.10).

For air-cooled applications where the enclosure is not compatible with the IEEE 1101.10-style front panels, traditional-style front panel kits can be purchased separately and fitted to the card by the customer.

## Foundation Firmware and BIT

The SVME/DMV-181 SBC is equipped with a comprehensive on-board firmware package called Foundation Firmware that includes:

- General Purpose Monitor (GPM) - provides monitoring, diagnostic, and board exerciser functions to facilitate system startup and integration activities (see General Purpose Monitor data sheet for more information)
- Built-in-Test (BIT) – a library of Card Level Diagnostic (CLD) routines is provided to support Power-up BIT (PBIT), Initiated BIT (IBIT) and Continuous BIT (CBIT) (see Card Level Diagnostics data sheet for more information)
- Card Support Services (CSS) - provides a common software interface to the hardware features of the card (see Card Support Services data sheet for more information)
- Execution Sequencer (ES) - controls the invocation order of the software configuration items on the card (see Execution Sequencer data sheet for more information)
- Non Volatile Memory Programmer (NVMP) - provides for in-circuit and closed chassis reprogramming of Flash memory over serial port or Ethernet (see Non-Volatile Memory Programmer data sheet for more information)
- Programming utility for FPGA Serial EEPROM

Our BIT firmware is designed to provide 95% fault coverage for testable functionality and supports tests in Power-up BIT (PBIT), Initiated BIT (IBIT), and Continuous BIT (CBIT) modes. PBIT consists of a reduced set of tests that provide confidence that the hardware is operating correctly while minimizing power-up time.

The IBIT capability allows users to initiate testing with a more comprehensive suite of tests to provide more robust testing in an off-line mode. CBIT allows applications to test hardware components in the background while the mission software operates as a higher priority task. The selection of tests for PBIT, IBIT, and CBIT is configurable.

## Operating System Software

The SVME/DMV-181 is supported by the following real-time operating systems:

- INTEGRITY Board Support Package from Green Hills Software (see separate datasheet for details)
- LynxOS ™ 4.0 reference port (see separate datasheet for details)
- TimeSys Linux Support Package from TimeSys (see separate datasheet for details)
- Wind River's VxWorks ® /Tornado BSP and Driver Suite (see separate datasheet for details)

Contact your local representative for updates on support for other operating systems.


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## IXLibs-AV DSP Library

Our IXLibs-AV DSP library allows customers to fully exploit the performance potential of the '181's AltiVec-equipped '7410 processor. IXLibs-AV provides a comprehensive set of AltiVec-optimized C-callable functions written primarily in assembly language, yielding a significant performance advantage over equivalent functions written only in a high-level language. This object-format library integrates easily with standard software development tools and supports real and complex array, vector, and scalar signal processing functions.

## Integration Support

We provide all the supporting items necessary to ensure a smooth system integration process. These include:

- Comprehensive hardware, firmware, and software documentation package, in hard copy and on CD-ROM
- Break-out cables for the front and rear-panel I/O to convert the '181-specific pin-outs to industry standard connectors for use in laboratory development environments. See Table 4.

*Table 4: SVME/DMV-181 Cable Set*

| Cable Number | Connects To | Description |
|---|---|---|
| CBL-SBC-FPL-000 | Front panel in all pin-out modes | Front panel break-out cable providing standard RJ-45 10/100BaseT Ethernet jack, connectors for two RS-232 channels, USB, JTAG/COP, and push-button switch for card reset. Compatible with SVME-181 and SVME-712 |
| CBL-SBC-P0-000 | P0 in modes 1, 4, 6, 7 (standard) | P0 break-out cable with separate branches and connectors for Ethernet interface 2, TTL discretes, USB port 2, and PMC I/O on our standard 78-way connector. Also includes reset switch |
| CBL-SBC-P0-001 | P0 in mode 2 | P0 break-out cable with separate branches and connectors for Ethernet interface 2, 8-bit SCSI interface (using 68-way 16-bit SCSI connector), 2 EIA-232 ports, EIA-422/485 ports 3 and 4, TTL discretes, and USB port 2. Also includes reset switch |
| CBL-SBC-P2-000 | P2 in modes 1, 2 (standard) | P2 break-out cable with separate branches and connectors for 8-bit SCSI interface (using 68-way 16-bit SCSI connector), 2 EIA-232 ports, EIA-422/485 ports 3 and 4, and PMC I/O on our standard 78-way connector. (No Ethernet branch.) |
| CBL-SBC-P2-001 | P2 in mode 3 | P2 break-out cable with separate branches and connectors for Ethernet interface 2, 8-bit SCSI (using 68-way 16-bit SCSI connector), 2 EIA-232 ports, EIA-422/485 ports 3 and 4, and TTL discretes. Also includes reset switch |
| CBL-SBC-P2-002 | P2 in mode 4 (16-bit SCSI) | P2 break-out cable with separate branches and connectors for 16-bit SCSI interface (using 68-way 16-bit SCSI connector), 2 EIA-232 ports, EIA-422/485 port 3, and PMC I/O on our standard 78-way connector |
| CBL-SBC-P2-003 | P2 in mode 6 (6 serial) | P2 breakout cable with separate branches and connectors for 2 EIA-232 ports, 4 EIA-422/485 ports, and PMC I/O on our standard 78-way connector. |
| CBL-SBC-P2-004 | P2 in mode 7 (Full I/O) | P2 breakout cable separate with separate branches and connectors for 16-bit SCSI interface (using 68-way 16-bit SCSI connector), 2 EIA-232 ports, and 4 EIA-422/485 ports |


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*Table 5: SVME/DMV-181 Specifications*

| POWER REQUIREMENTS | Maximum | Typical |
|---|---|---|
| +5 V (+5.0%, -2.5%) | 5.0 A | 4.0 A |
| +12 V | 0 A | Not used by the base card, only routed to the PMC sites. |
| -12 V | 0 A | Not used by the base card, only routed to the PMC sites. |
| 3.3 V | 0 A | Not used by the base card, only routed to the PMC sites. |
| +5 V STDBY: | | |
| - with +5 V present | <1 uA | <1 uA |
| - without +5 V | <2 mA | <1 mA |

| DIMENSIONS & WEIGHT | Dimensions | Weight |
|---|---|---|
| SVME card | per ANSI/VITA 1-1994 | <500 g (<1.21 lbs.) |
| DMV card | per IEEE 1101.2 | <750 g (<1.65 lbs) |

SVME cardAvailable in levels 0, 100 and 200*
DMV cardAvailable in levels 100 and 200*
*For the SVME/DMV-181 level 200 temperature range is -40°C to +85°C.

Refer to Ruggedization Guidelines datasheet for more details

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