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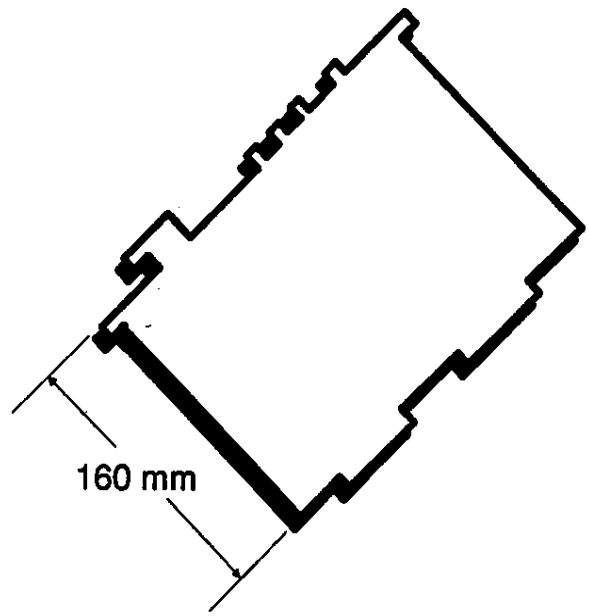
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Find the *Curtiss-Wright / DY-4 SVME-740* at our website: *Click HERE*

SVME-740

Intelligent IEEE 802.3 LAN Controller



Features

- *10 MHz 68010 CPU*
- *Local Area Network (LAN) compatible with IEEE 802.3*
- *Serial Interface Adapter (SIA) VLSI Manchester encoder/decoder*
- *DMA between on-board memory and LANCE*
- *512K bytes of dual-ported DRAM with parity*
- *Up to 128K bytes of EPROM in two byte-wide sockets*
- *Standby power-down memory operation*
- *Software-maskable interrupts on-board*
- *ROR/RWD Requester modes dynamically supported*
- *Requester supports early release of BBSY*
- *Requester level is jumper-programmable*
- *Periodic tick clock, one of four intervals*
- *Optional TCP/IP firmware*
- *Watchdog timer*
- *Location monitor*
- *Built-in-Test (BIT)*
- *Bus Isolation mode (BI-mode®)*
- *VMEbus interrupter programmable to one of seven levels*
- *Faceplate status and control indicators*
- *Two faceplate sense switches readable by software*
- *Five-bit card ID via P2 connector*
- *VMEbus IEEE P1014 compatible*
- *Optional levels of ruggedization available*

Description

The SVME-740 LAN Controller is an intelligent LAN controller that includes a 16-bit microprocessor, memory and IEEE 802.3 local area network interface via the P2 connector for connection to the cable transceiver. The implementation of the LAN via the VLSI devices allows control of interrupts and LAN functions via internal on-chip registers.

The card supports DY 4 Systems' common features such as a location monitor, Built-In-Test (BIT), and BI-mode.

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SVME-740

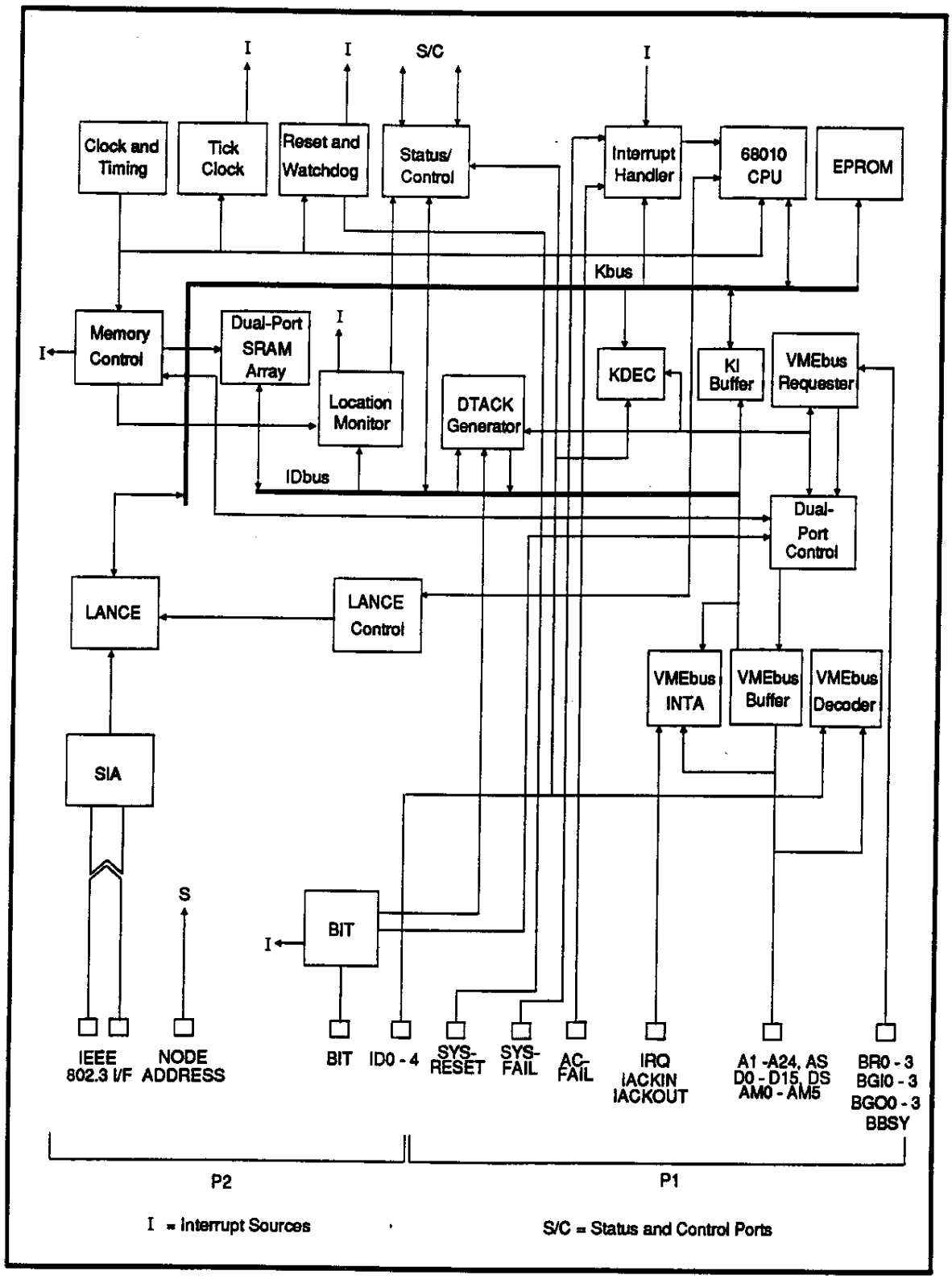


Figure 1: SVME-740 LAN Controller Block Diagram

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DY 4 Systems' common features support diagnostics, interprocessor communications, and logistics maintenance on-line. BIT provides hardware features to verify all operational circuit blocks on the module. BI-mode® provides a means to electrically isolate the module from the VMEbus. The location monitor provides a fast, efficient means of interprocessor mailbox message passing to minimize software overhead in real-time operations. These features allow the users to perform fault detection and isolation during operation to build fault-tolerant systems. In addition, they allow for on-line maintenance and system configuration control to minimize field maintenance, time, and sparing logistics.

Figure 1 shows the block diagram of the SVME-740 LAN Controller.

Memory

Two byte-wide EPROM sockets are supported. The EPROM is used for both boot function and non-volatile program store. On power-up or following a reset, the 68010 requires an initialization vector at location 0. As the contents of DRAM cannot be guaranteed, the EPROM is forced to be located at address 0 at reset.

The SVME-740 LAN controller has 512K bytes of dual-ported dynamic RAM, using 256K bit-devices. The DRAM array can be accessed by the local CPU and also by the VMEbus. The memory includes byte parity. The access address of the dual-ported RAM from the VMEbus is dependent on the 5-bit ID code present on the P2 connector or on-board jumpers.

RAM is byte and word-addressable and is parity checked on a byte basis on each read cycle. At power-up, software should write to all memory locations to initialize the parity bit.

An interrupt is generated when a parity error occurs. The parity error is latched and the latched status is readable by software. The interrupt is capable of being cleared or masked by a software-programmable control bit.

The DRAM is refreshed by a hardware circuit, transparent to the software. While the internal RESET line is asserted, refresh is still supplied by the hardware. Refresh does not interrupt a read-modify-write cycle from either the CPU or VMEbus.

The SVME-740 LAN controller provides power-down standby operation of the DRAM array. Through a jumper block option, standby power is provided by the +5V STDBY pin and one auxiliary power pin. Operation under standby conditions consists only of RAM refresh.

The RAM standby operation is invoked by the assertion of the internal reset signal. As long as the internal reset signal is active, the DRAM array operates in standby mode. Upon an ACFAIL* interrupt, the user software determines a "power-safe" period, after which the user must not access the DRAM array. Failure to adhere to this rule can result in corrupted dynamic RAM contents when the +5V mains become out-of-tolerance. The power-safe period is a system parameter derived from the system's power monitor module timing, if used.

Requester

The requester is compatible with single level (SGL), Priority (PRI) and Round Robin Select (RRS) arbitration schemes on the VMEbus. The Release on Request (ROR) or Release When Done (RWD) modes of operation are software-programmable. Both requester modes implement the early release of BBSY (Bus Busy). The requester level is programmed by jumper straps.

Interrupter

An interrupter is provided that allows software to interrupt the VMEbus on one of

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SVME-740

the seven levels. The interrupt level and Status/ID byte are software-programmable from the local CPU. The Status/ID is supplied to the VMEbus interrupt handler when it responds with an interrupt acknowledge cycle. The interrupter operates in the Release on Acknowledge (ROAK) mode.

Since the SVME-740 LAN controller is a peripheral card, no interrupt handler is provided.

Tick Clock

A tick clock is provided to generate a periodic interrupt of the on-board CPU. The periodic timer is a free-running clock and on each assertion of the clock, an interrupt request is generated. Detection of this clock assertion is enabled/disabled under software control. The interval is determined by jumper straps that allow the selection of one of four intervals.

Debug Monitor

The SVME-740 LAN controller is supplied with a powerful debug monitor offering the following features:

- Interrupt vector and I/O initialization
- Memory Dump
- Memory Move
- Memory Display/Modification
- Memory Write
- Register Display/Modification
- Execution Commencement
- Executive Breakpoint
- Motorola 'S" Record Serial Download
- Cold Initialization
- Warm Initialization
- Input/Output Processing
- User access to I/O functions
- Exception Handling
- User access to Exception Handling
- Single Step Execution
- Pass Through to Host
- Pass Through to Monitor

On-board Diagnostics

On-board firmware supplied with the SVME-740 LAN controller incorporates a debug monitor as well as diagnostic routines which perform a self-test function in conjunction with the Built-in-Test equipment. These diagnostics which are evoked under power-up or by system-supplied software provide for the following functional tests:

- Processor Confidence
- DRAM
- PROM Check Sum
- Location Monitor
- Periodic Clock
- Watchdog Timer
- Control Status Register
- LANCE Internal Loopback
- LANCE Internal Collision Detection
- Local Interrupts

Status and Control I/O

The SVME-740 LAN controller provides four status inputs and one control output available for system definition. The status inputs are pulled high via 4.7K ohm resistors and control output is an open collector driver, open on reset.

LAN Address

The P2 connector provides 8 bits of data in an I/O register. These data bits can be used to make the 48-bit LAN address slot-dependent or they can be used as general purpose input lines. The data bits are pulled high via 4.7K ohm resisters.

Optional Firmware

As an option, the LAN interface can include the TCP/IP firmware package. Refer to the

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Internet Protocol Suite Firmware Data Sheet, document number MS00070.

Table 1
Specifications

Temperature		
SVME-740 (Commercial)		
Operating	0°C to 50°C	
Storage	-55°C to 125°C	
SVME-740 (MIL-STD-883C)		
Operating	-55°C to 85°C	
Storage	-65°C to 125°C	
Humidity		
0 to 95%, non-condensing		
Physical Dimensions		
Height	233.4 mm	(9.2 in.)
Depth	160 mm	(6.3 in.)
Thickness	20.0 mm	(0.8 in.)
Weight	< 1.36 kg	(< 3 lb)
Power Requirements		
+5 V (+5%, -2.5%)	6.13 A (maximum) 3.7 A (typical)	
+5 V (+5%, -2.5%) Standby	1.8 A (maximum) 1.1 A (typical)	

Notes: Total +5 VDC requirement when operating is (3.7 A + 1.1 A). When internal standby is not required, the internal standby rail is jumpered to the main +5V VMEbus rail via an on-board jumper.

For additional specifications on the other levels of ruggedization, refer to the Product Ruggedization Guide, document number MS00149.

Ordering Information

Model Number	Product Description
SVME-740-005	Intelligent IEEE 802.3 LAN Controller, 10 MHz 68010 CPU, 512K bytes DRAM, serial interface adapter, TCP/IP software, LANCE, BI-mode®, and a location monitor. Refer to the Product Ruggedization Guide, document number MS00149.

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