PRODUCT DATASHEET

SVME/DMV-178

PowerPC™ 740 Single Board Computerwith Dual PMC Interface

Features

- PowerPC™ 740 CPU at 200/300 MHz
- Up to 64 Mbytes DRAM with ECC
- 512 Kbytes of L2 cache
- 8/16 Mbytes of 64-bit wide application Flash EPROM
- supports up to 2 Mbytes of byte-wide boot Flash EPROM (with 8 Mbytes 64-bit Flash)
- 8 Kbytes of Autostore NOVRAM
- 512 bytes of serial EEPROM
- Two IEEE P1386 PCI/PMC module sites for flexible I/O expansion
- On-board 10/100 Mbit Ethernet™ port with 10/100BaseTX (twisted pair) interface
- On-board fast SCSI-2 interface (Ultra SCSI)
- Optional IEEE 1284 ECP/EPP parallel port
- Two EIA-422 and two EIA-232 serial channels
- Four cascadable 16-bit timers, watchdog timer, Real Time Clock
- VME64 master/slave interface
- 95% BIT fault coverage
- 5-row P1 and P2 connectors
- 95-pin P0 connector standard (removable)
- Our Standard foundation firmware (ES/GPM/CSS/CLD/NVMP see data sheets)
- VxWorks® and LynxOS™ BSPs and drivers
- Available in a range of ruggedization levels (air and conduction cooled)

Overview

The SVME/DMV-178 is a member of our growing line of PowerPC™-based Single Board Computer (SBC) products for harsh environment computing. This PCI-based SBC combines a high-performance PowerPC 740 RISC processor with 64 Mbytes of DRAM with ECC, 512 Kbytes of Level 2 (L2) cache, together with up to 16 Mbytes of Flash EPROM all on a 0.8" single-slot VMEbus card. Numerous additional system interface functions including fast Ethernet, SCSI-2, and four serial ports (two with DMA support) are also included. In addition, this card is equipped with two air- and/or conduction-cooled PMC module interfaces.

PMC, an open industry standard mezzanine module with a PCI interface, allows system designers to increase the assembly's functionality by utilizing our standard PMC modules, available third party products, or developing their own PMC-based modules.

The SVME/DMV-178 provides a highly integrated PowerPC architecture in a single-slot solution with high processing performance, industry standard I/O and the flexibility of user-specific I/O which traditionally required multiple cards (Figure 2). The SVME/DMV-178's design features address real-time, mission- critical demands of military and aerospace systems integrators with increased computing performance, self-test coverage, and high functional density.

The card supports our common architecture feature set, including the option of compatible pin-out with previous SVME/DMV-176 or 177 PowerPC products, a feature-rich VME64 VMEbus interface with Built-In-Test (BIT), BI-mode®, read/write FIFOs, and Auto ID. These features bring benefits in performance as well as supporting technology insertion, reducing program logistics and maintenance costs.

Tundra's Universe II™ interface chip provides a PCI to VMEbus bridge which implements all VMEbus interface functions with software-programmable features. Based on the popular SCV64™, the Universe II combines low-latency access to the VMEbus with high sustained throughputs. Bus Isolation mode (BI-mode) increases ease of testing and system fault isolation/location. Additional Built-In-Test (BIT) hardware features verify correct operation to a high confidence level.

The Universe II internal FIFOs support write posting, enabling efficient interprocessor messaging thereby minimizing overhead in real-time software. Auto-ID allows cards to be self-configuring, based on geographical backplane slot location. These features allow users to:

- build high-performance multiprocessor systems
- detect and isolate faults during operation
- minimize field maintenance and sparing logistics

All versions of the SVME/DMV-178 are functionally identical, with air and conduction-cooled versions available in ruggedization levels of 0, 50 and 100.

The conduction-cooled DMV version is designed for harsh airborne, land-mobile, and naval military applications where circuit cards may be subjected to environmental extremes such as temperature, shock, vibration, and humidity. Our standard ruggedization guidelines define the environmental tolerance of each ruggedization level.

For thermal management, thermal layers within the PWB conduct heat away from the components, and an additional stiffening frame improves heat dissipation, plus shock and vibration resistance. Standard wedgelock fasteners ensure a reliable thermal and rigid mechanical connection to the chassis.

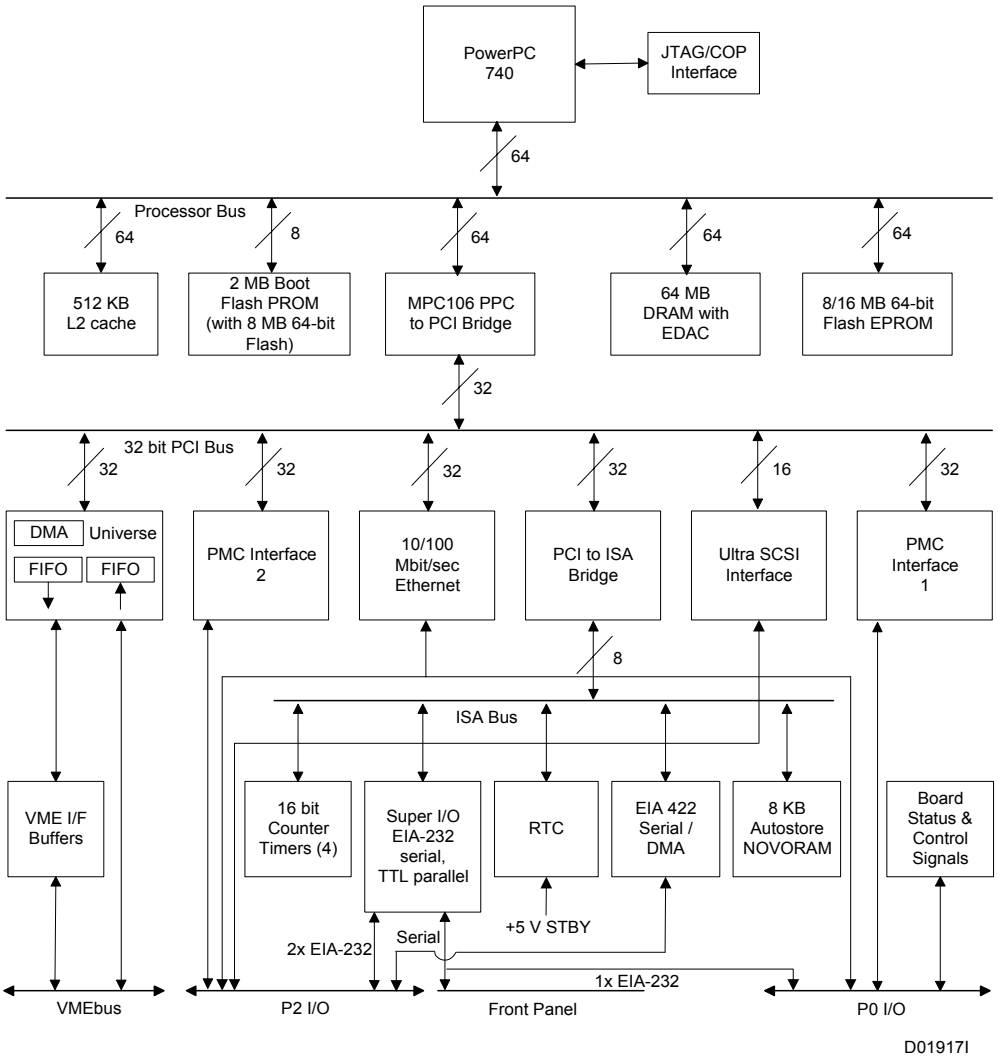

Figure 1: Block Diagram (see Table 1 for alternate I/O Routings)

Table 1: I/O Routing Options

Pin-out Mode	Description	Front Panel (air cooled cards only)	P0 Connector	P2 Rows A & C	P2 Rows D & Z
1	Standard Configuration (5-row P1/P2, 95-pin P0)	2x EIA-232	PMC Site #1 I/O Ethernet 1x EIA-232 Cardfail status out Ext. Card Reset in Boot Select in Flash Ext. Vpp in JTAG & COP I/F	PMC Site #2 I/O	Ethernet SCSI 2x EIA-232 2x EIA-422
2	Optional 176/177 P0/P2 Compatibility Mode	2x EIA-232	Ethernet SCSI 2x EIA-232 2x EIA-422 Cardfail status out Ext. Card Reset in Boot Select in Flash Ext. Vpp in JTAG & COP I/F	PMC Site #2 I/O	Ethernet SCSI 2x EIA-232 2x EIA-422
3	Optional 176/177 P2-only Compatibility Mode	2x EIA-232	P0 not installed	Ethernet SCSI 2x EIA-232 2x EIA-422 Parallel Port Ext. Card Reset in	Ethernet SCSI 2x EIA-232 2x EIA-422
4	Optional Parallel Port Mode	2x EIA-232	PMC Site #1 I/O Ethernet 1x EIA-232 Cardfail status out Ext. Card Reset in Boot Select in Flash Ext. Vpp in JTAG & COP I/F	Ethernet SCSI 2x EIA-232 2x EIA-422 Parallel Port Ext. Card Reset in	Ethernet SCSI 2x EIA-232 2x EIA-422

Note: Optional I/O routing modes are controlled by factory-set configuration links. Boards with other than the standard routing are built to order and set-up charges may apply.

CPU

The PowerPC 740 CPU is a high-performance, 64-bit RISC-based microprocessor developed for the growing real-time embedded industry. The 178's PowerPC runs at up to 300 MHz on-chip and offers estimated benchmarks as follows:

Table 2: Device Manufacturer's Estimated Performance

PowerPC 740		
Speed	SPECint95	SPECfp95
200 MHz	8.6	5.2
300 MHz	13.5	7.1

The PowerPC chip integrates all of the following onto a single monolithic die:

- Superscalar (multiple instruction-per-cycle)
- 32- and 64-bit Floating Point Processor (FPP)
- Six separate parallel instruction units
- 32 Kbyte instruction and data caches
- Variety of power saving modes
- 3.3 V I/O
- Low voltage core (2.5 - 1.9 V)

Memory

SVME/DMV-178 SBC main memory is located on the base board, consisting of up to 64 Mbytes high performance DRAM. In addition, user-programmable two bit detect, single bit correct EDAC is provided.

The SVME/DMV-178 supports a mix of nonvolatile storage devices for 10 or 16 Mbytes of on-board nonvolatile memory storage. On-board nonvolatile memory consists of:

- 64-bit wide Application Flash
- 8-bit wide boot Flash (when 8 Mbyte 64-bit Flash fitted)
- 8 Kbytes of Autostore NOVRAM

Application Flash provides the capability of high performance, 64-bit wide long word, ROM-resident program execution directly from EPROM. When configured with 8 Mbytes application Flash, a low-cost 2 Mbyte Flash memory boot site is also available, allowing the logical separation of boot-only and application software. Note that when the full 16 Mbytes of user Flash is installed the 8-bit Flash is not available and the boot firmware is loaded into the 64-bit Flash.

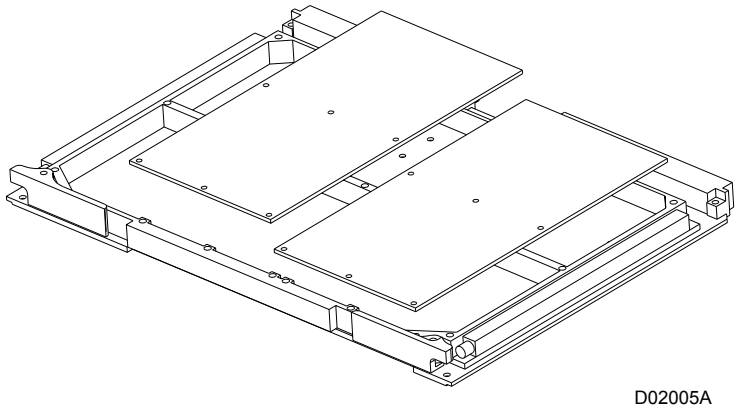

Figure 2: Base Card with two PMC Mezzanines

For safety, the non-volatile memory is not VME-visible, but is easily programmable via our own integrated Non-Volatile Memory Programmer utility over the VMEbus, the serial port, or the Ethernet port, allowing sealed chassis re-programming.

Autostore NOVRAM

The Autostore NOVRAM provides fast, non-volatile storage of system variables or position sensitive data as found in most real-time applications. Based on Shadow RAM technology, all 8 Kbytes are automatically transferred from the on-chip SRAM and stored within 10 ms to the on-chip EEPROM with a single user command (or power-down for safety). At the next power-up sequence the device automatically transfers the EEPROM contents to the SRAM, where the application code can now utilize those variables in its environment and continue normal operation.

PMC Interface

The SVME/DMV-178 SBC is equipped with two industry standard IEEE P1386.1 PCI/PMC mezzanine module interface sites. These PMC modules may be used to add a variety of diverse and flexible I/O functions to the base card. PMC modules conform to an open industry standard specification that defines the electrical and mechanical interface, thus permitting straightforward designs of special function modules. All PMC I/O connections are brought out on the backplane P0 and P2 connectors in accordance with IEEE P1386 (see Figure 2).

Our future generations of RISC-based SBCs will carry a compatible PMC interface, thus providing a performance and upgrade growth path that preserves the software invested in the PMC module and overall system.

Programmable Power Modes

The SVME/DMV-178 has several user-programmable power saving modes (Nap, Sleep, Doze...) which lower the power consumption under certain conditions, resulting in a very low power, full-featured rugged product. These modes are supported by the SVME/DMV-178 and its foundation firmware.

Serial EEPROM

The SVME/DMV-178 provides 512 bytes of serial EEPROM for storing configuration that used by card initialization firmware. User access to the serial EEPROM is also provided.

VME Interface

The VMEbus interface of the SVME/DMV-178 is implemented with Tundra's Universe II single chip VMEbus Interface. The Universe II is based on the popular SCV64, providing all the elements of a complete VMEbus interface. System designers can therefore more easily migrate and upgrade systems based on our existing SBCs that utilize the SCV64. In addition, the device implementation philosophy of the Universe II design allows programmable features, virtually eliminating the need for user-set jumpers, thereby simplifying logistics and reducing sparing and maintenance requirements. The Universe II incorporates the following features:

- System Controller with Auto-ID
- Master/slave A64:D64 interface, SYSCLK
- Tx and Rx FIFO's to decouple bus operations
- Interrupter, interrupt handler
- Extensive Built-in-Test support

A primary function of the Universe II is to allow the CPU to access the VMEbus and to allow the VMEbus to access on-board memory and resources. The Universe II contains transmit and receive FIFOs with write-posting, which implements a store-and-forward technique of bus decoupling. Universe II-equipped CPUs can write to VMEbus locations without incurring a delay while the VMEbus is requested, arbitrated, and the bus grant received. For moving large blocks of data between on-board memory and the VMEbus, the Universe II provides an integral DMA controller. Bidirectional transfers can be configured to occur in discrete, block, or multiplexed block (D64) mode.

To support inter-processor message passing, the Universe II provides a built-in FIFO message queue organized as a 32-bit wide FIFO with 31 possible entries and flexible user interrupt programmability.

Ethernet™ Interface

An on-board IEEE 802.3 10BaseT and high speed 100BaseTX compliant Ethernet™ interface (implemented with the Digital Equipment 21140A PCI device) is provided to eliminate the requirement for a separate Ethernet card located elsewhere in the development or deployed system. Available in both SVME and DMV versions, this LAN interface may be used for card-level download and debug, or may be incorporated into a deployed system for a 10 or 100 Mbit/sec communication port. A BaseT (twisted pair) interface is provided allowing a simple, four wire LAN providing a local, low latency and alternate high speed communications data bus.

SCSI-2 Interface

The SVME/DMV-178 provides a single-ended, 8-bit wide SCSI-2 compliant interface on the P0 connector also optionally routed to the P2 connector. Using the Symbios (NCR) 53C860 with an internal high speed DMA controller, peak SCSI bus speeds of up to 7 Mbytes/sec (asynch) or up to 20 Mbytes/sec (synch, Fast-20) are supported. The DMA controller acts independently of the CPU to transfer data between the local memory and the SCSI controller IC. This allows the PowerPC and the other on-board I/O processors to continue to handle processing tasks while data is being transferred to and from the SCSI bus.

Serial/Other Interfaces

The SVME/DMV-178 provides four (4) flexible, user configurable serial channels and, optionally a 10 bit parallel Centronics port. The EIA-232 ports are 16C550-compatible asynchronous ports with data rates programmable from 50 baud to 115.2 Kbaud. These two async serial channels are available at the P0 or P2 connector and on the connector located on the front panel of the air-cooled SVME versions. The remaining two serial ports are EIA-422 and are implemented via an 85C30 SCC and are also available at the P0 or P2 connectors. These two EIA-422 channels are software configurable for either synchronous or asynchronous operation and support sustained synchronous data rates of up to 1 Mbps with DMA. The serial port interrupts are user-programmable under software control.

Real-Time Clock (RTC)

The RTC function is provided by a Dallas Semiconductor DS17885, providing time-of-day calculations. It contains registers for century, year, month, day, day-of-week, and seconds through to hundredths of seconds. The RTC is capable of periodic or alarm/wake-up interrupts to the CPU. The century register alleviates the “year 2000” issue.

The RTC may be powered from either VCC or the +5V STDBY line, therefore continuing to maintain the time during loss of main power. An on-board battery location is provided as a convenience on the Level 0 product to support the software development environment.

Timers

There is an on-board tick timer which can be programmed to interrupt the CPU at regular intervals. A hardware watchdog timer provides a fail indication or resets the CPU if an execution failure is detected. The watchdog timer interval is pre-set to 100 ms.

There are three additional cascadable 16-bit timers available to the user providing a basic interrupt on the terminal count.

System Status Signals/Switches

The SVME/DMV-178 SBC provides a run/fail status signal on the P0 connector and a corresponding front panel red indicator LED. This signal is asserted in the event of a card failure. A card reset function is also available via the P0 connector. Access to these critical signals on the backplane allows a test connector to be incorporated on the front panel of a sealed conduction-cooled chassis to facilitate full systems testing for deployed maintenance purposes. In addition, a user-programmable green status LED is also included on the card’s front panel.

JTAG/COP Interface

The SVME-178 routes the PowerPC JTAG and Control and Observation Port (COP) functions to the P0 connector. The JTAG boundary scan features can be used for card-level testing while the COP features are used mainly for chip/code debug. The JTAG features and interface are compliant with IEEE 1149.1.

PMC Modules

The capabilities of the SVME/DMV-178 SBC can be further enhanced by adding either one or two optional PMC (IEEE-P1386.1) modules. The PMC mechanical design is well suited to high shock and vibration environments, where the modules are rigidly mounted to the base card along the stiffening ribs. On conduction cooled modules thermal interfaces provide a low-resistance thermal path for heat removal in both air and conduction cooled applications.

PMC modules are designed to be 100% functionally compatible in standard ruggedization levels for use with both air-cooled and conduction-cooled base boards.

We also offer a range of ruggedized PMC modules. Consult your local representative for additional information.

Foundation Firmware

The SVME/DMV-178 SBC is supplied with an on-board foundation firmware package, including:

- General Purpose Monitor (GPM) - provides comprehensive monitoring and debug functions for the system integrator (see General Purpose Monitor data sheet for more information)
- Card Level Diagnostics (CLD) - provides diagnostic routines which perform a self-test function (see Card Level Diagnostics data sheet for more information)
- Card Support Services (CSS) - provides a common software interface to the hardware features on the card and Auto-ID services (see Card Support Services data sheet for more information)
- Execution Sequencer (ES) - controls the invocation order of the Software Configuration Items on the card (see Execution Sequencer data sheet for more information)
- Non Volatile Memory Programmer (NVMP) - provides for in-circuit and closed chassis reprogramming of Flash memory (see Non-Volatile Memory Programmer data sheet for more information)

Built-in Test

Incorporated in Foundation Firmware via Card Level Diagnostics (CLD), our BIT is extensive and full-featured. Our CLD is designed to provide a 95% fault coverage level in testable functionality achieved with a 90% probability of fault isolation to a single board in a configured system.

CLD supports tests in Power-up BIT (PBIT), Continuous Background BIT (CBIT) and Initiated BIT (IBIT) modes. PBIT consists of a reduced set of tests which provides confidence that hardware is correctly operating while minimizing overhead at power-up time. CBIT allows applications to test hardware components in the background while mission software operates as a higher priority task. IBIT provides a mechanism for performing a complete set of diagnostic tests as a foreground task in order to ensure proper operation of the hardware. For more information, see the *Card Level Diagnostics* data sheet.

Software

A variety of real-time operating systems, application programs, and software tools are available for the SVME/DMV-178. Supported operating systems include VxWorks®/Tornado™ and LynxOS™.

Power Routing

The SVME/DMV-178 basecard uses only +5 V and optionally +5 V STDBY. Two on-board regulators provide the necessary 3.3 V and processor core voltage. PMC sites are fed with +5 V, ±12 V, and 3.3 V from the backplane.

Table 3: Specifications

RUGGEDIZATION LEVELS*		
SVME card	Available in levels 0, 50 and 100	
DMV card	Available in level 100	
POWER REQUIREMENTS (Basecard only- no PMC modules)		
Input	**Maximum**	**Typical**
+5 V **+5 V STDBY** **+12 V** **-12 V**	5.6 A 3 mA (for RTC if so configured) 0 0	4.6 A 1 mA (for RTC if so configured) 0 0
DIMENSIONS		
	Size	**Weight**
SVME card	per ANSI/VITA 1-1994	<530 g (<1.17 lbs.)
DMV card	per IEEE 1101.2	<560 g (<1.23 lbs.)

*Refer to Ruggedization Guidelines data sheet for more details.

Contact Information

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For technical support, please visit:

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