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SVME-122 SINGLE BOARD COMPUTER

OPERATIONS MANUAL

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800957

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1. GENERAL INFORMATION

1.1 General

The SVME-122 Single Board Computer (SBC) includes a 32-bit 68020 microprocessor, memory, two byte-wide memory units a VME Subsystem Bus (VSB) interface as per IEC 821, a Counter/Timer and Parallel I/O (CIO), a Serial Communications Controller (SCC), and a 32 bit Floating Point Processor (FPP). It is implemented on a double height, Eurocard board.

This book provides general information, hardware configuration, functional description, and the programming interface for the SVME-122 SBC. This book is divided into the following chapters:

(1) General Information: contains symbol description, features, physical description and references.
(2) Specifications: includes the environmental specifications, the power requirements, and the performance of the SVME-122.
(3) Functional Description: includes a description of each of the major functional blocks of the SVME-122.
(4) Hardware Configuration: includes the front panel connector and the two external P1 and P2 connectors.
(5) Programming Interface: includes the local CPU memory maps and the contents of the control/status registers.
(6) Appendix A - I/O Address Summary: includes the I/O address map of the SVME-122.

1.1.1 Symbol Description

The following is a brief description of the symbols that are used in this book.

The plus sign (+) after the signal name indicates that the signal is active HIGH.

The asterisk (*) symbol after the signal name indicates that the signal is active LOW and that it is from the VMEbus or VSB bus.

The slash (/) symbol after the signal name indicates that the signal is active LOW and that it is from anywhere else but the VMEbus or VSB bus.

Unless stated otherwise, all addresses are in hexadecimal.

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1.2 Features

The following features are provided on the SVME-122 Single Board Computer:

- A 16.7 MHz 68020 Microprocessor (uP),
- A 16.7 MHz 68881 Floating-Point Coprocessor (FPCU),
- Cache enable and write protect logic,
- 128 Kbytes EPROM,
- 16 Kbytes of Static RAM (SRAM),
- 16 Kbytes of on-board cache,
- Two bi-directional RS-232C serial I/O interface using a Serial Communications Controller (SCC), and with front panel I/O,
- Three 16-bit counter/timers using a 8536 Counter/timer and parallel I/O Unit (CIO),
- An on-board interrupt handler,
- Two software readable control function switches,
- Two status Light Emitting Diodes (LED), one FAIL LED on the front panel, and a HALT LED to indicate the card's functional status,
- A momentary toggle abort switch on the front panel,
- A VMEbus A32, A24, A16, D08 (EO), D16, and D32 master interface,
- A VMEbus interrupt handler in conjunction with the on-board interrupt handler,
- A programmable VMEbus location monitor with 8-bit wide by 512 deep address FIFO generating a maskable local interrupt for interprocessor message passing,
- A VSB D32 master interface,
- A VSB serial arbiter,
- 512 Bytes of EEPROM
- BITE including Board Isolation Capability

Figure 1-1 provides the functional block diagram of the SYSCPU.

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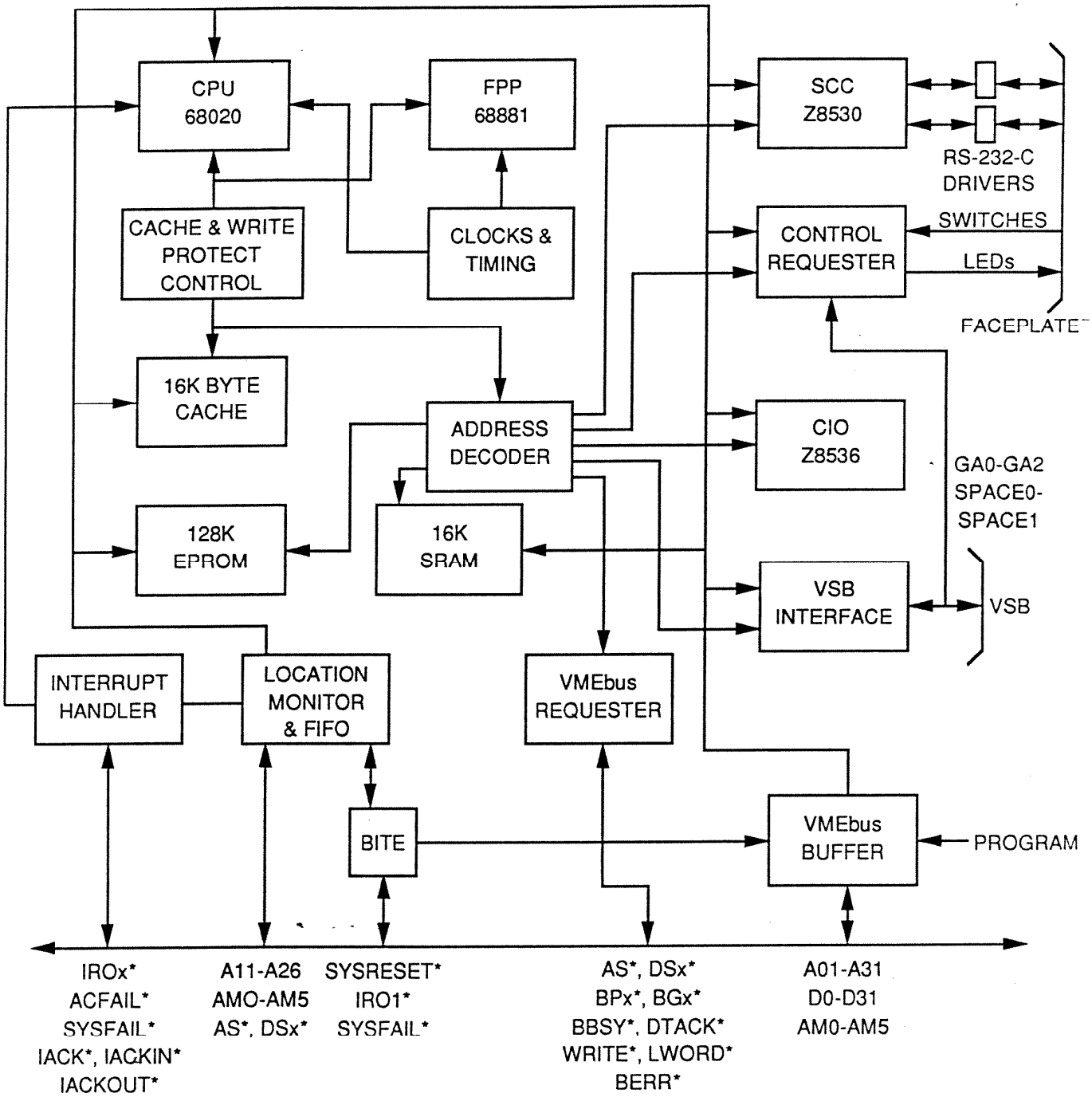


Figure 1-1 SVME-122 Single Board Computer Functional Block Diagram

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1.3 Physical Description

This section details the physical characteristics of the SVME-122 Single Board Computer. Refer to Figure 1-2, Component Layout of the SVME-122 Single Board Computer.

1.3.1 Dimensions

Refer to Table 1-1, Card Dimensions, and Figure 1-3, Dimensions of the SVME-122 Single Board Computer.

Table 1-1
Card Dimensions

Dimension	Metric	Imperial
Height	233.0 mm	9.2 in.
Depth	160.0 mm	6.3 in.
Width	20.0 mm	0.8 in.
PCB Thickness	1.6 mm	0.063 in.

1.3.2 Weight

The SVME-122 SBC weights less than 1360 grams (3 lbs.) with Ceramic Integrated Circuits (ICs) installed.

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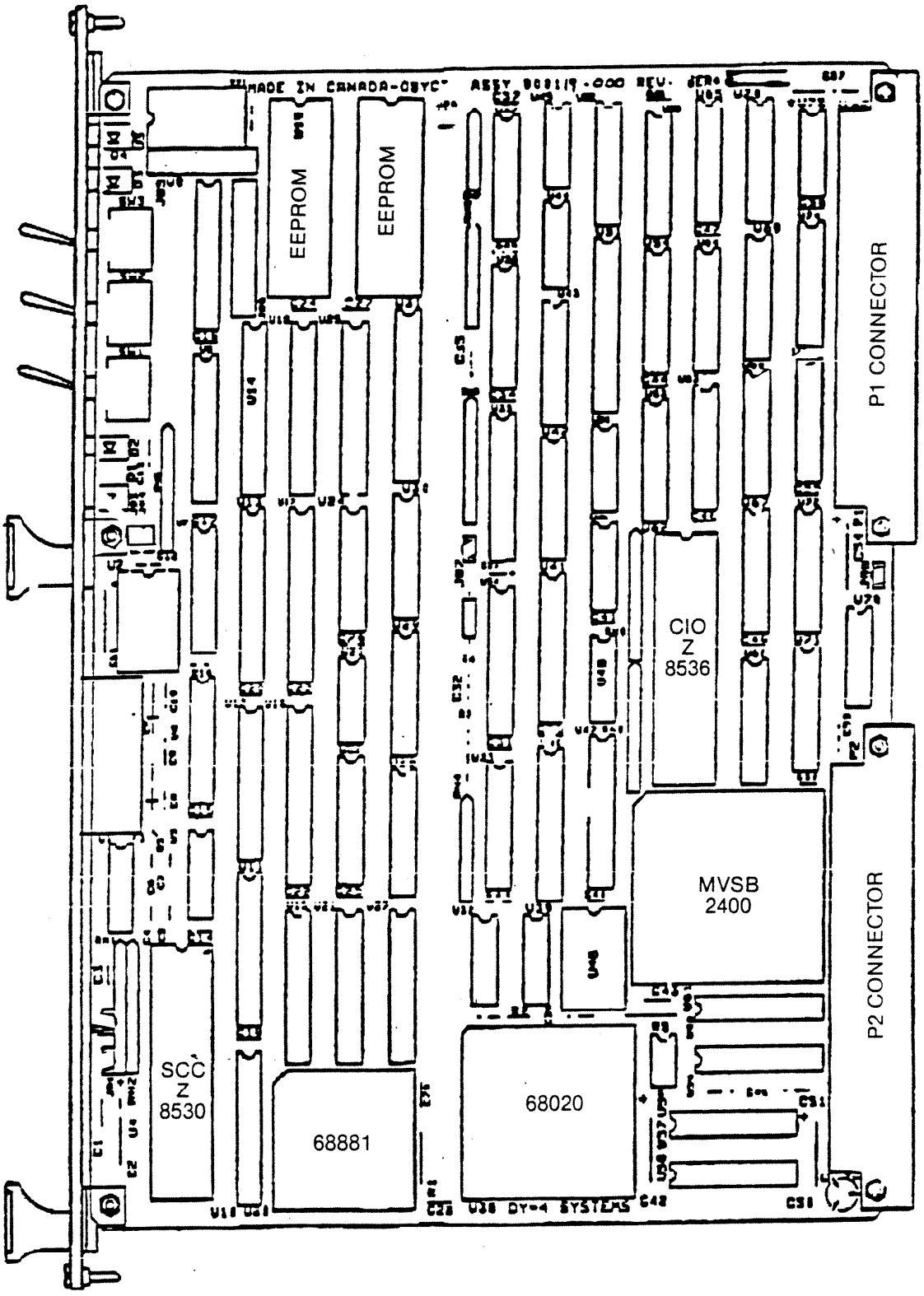


Figure 1-2. Component Layout of the SVME-122 Single Board Computer

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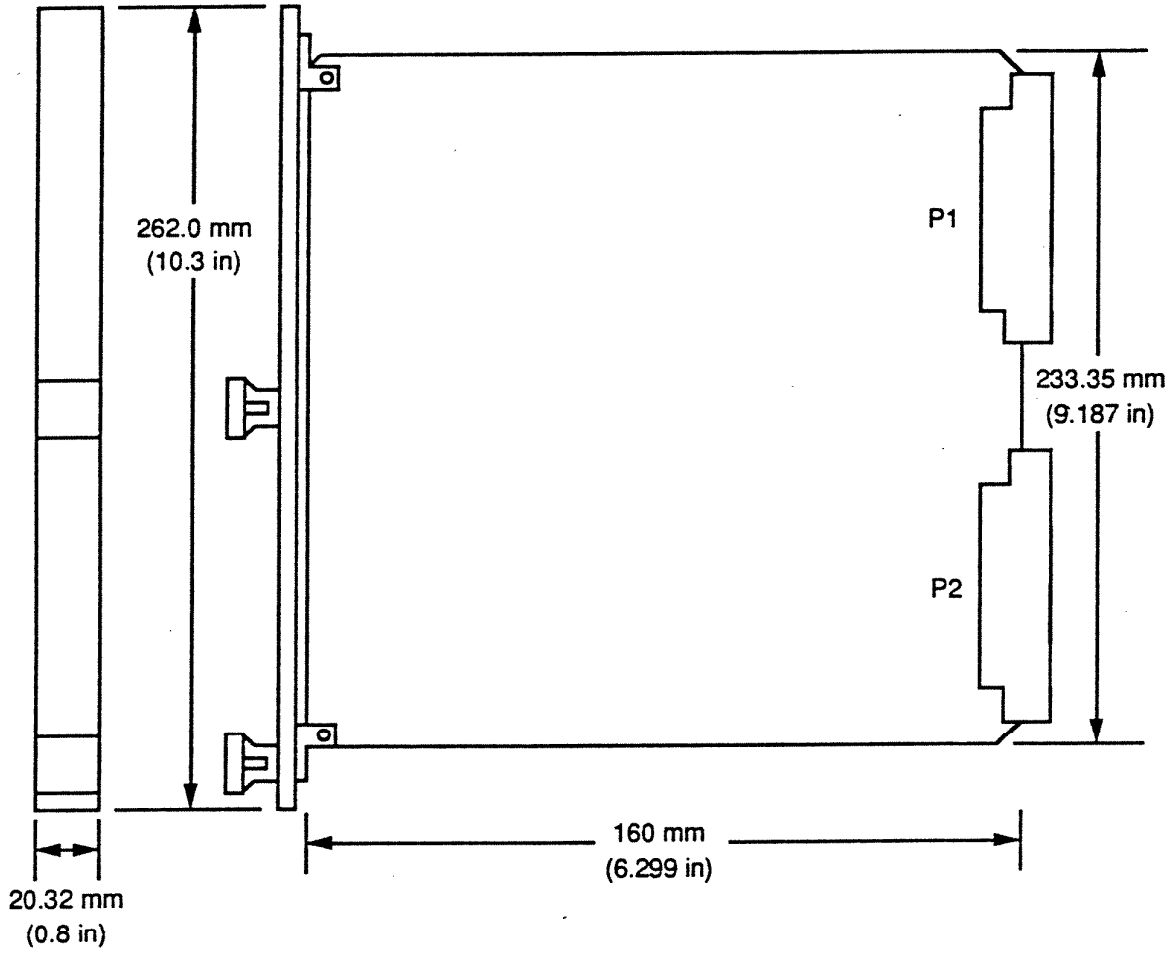


Figure 1-3 Dimensions of the SVME-122 Single Board Computer

EPS.00802.D11

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1.3.3 Faceplate

Figure 1-4, Faceplate Layout, shows the faceplate. From top to bottom, the faceplate includes the following:

* USLED (amber Upper Status LED)
* LSLED (amber Lower Status LED)
* FS0 (Faceplate Status Switch 0)
* FS1 (Faceplate Status Switch 1)
* ABT/RST (Abort/Reset Toggle Switch)
* FAIL (red FAIL LED)
* HALT (amber HALT LED)
* CH. A and CH. B (DE-9 Connector)

1.3.4 Mating Connector

The SVME-122 Single Board Computer uses both the P1 and P2 mating connectors specified in the IEEE P1014 (VMEbus) specification.

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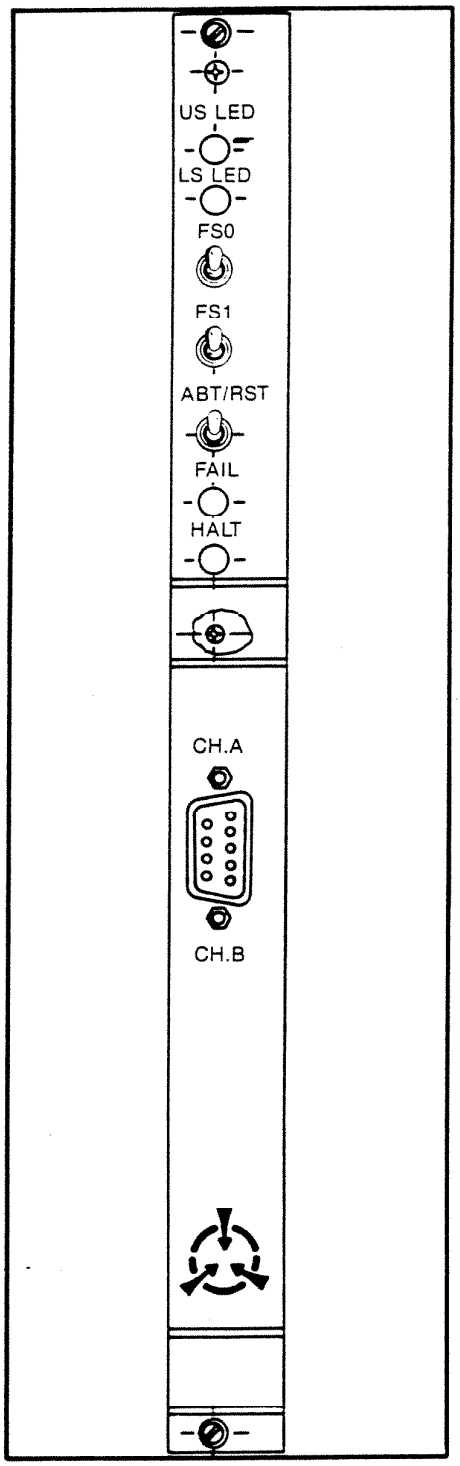


Figure 1-4. Faceplate Layout

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1.4 References

This section lists all documents referenced in this manual. The date of issue is included for each document; however, when a document is cited subsequently, the date is not included.

1.4.1 Manufacturer's Data Books

Fairchild	FAST Data Book, 1985
Integrated Device Technology	High Performance CMOS Data Book, 1986
Monolithic Memories	LSI Data Book, 7th Edition, 1986
Monolithic Memories	Programmable Logic Handbook, 5th Edition, 1986
Motorola	MC68020 User's Manual, 2nd Edition, 1985
Motorola	MC68881 Floating Point Coprocessor Users's Manual, First Edition, 1985
Motorola	MVSB2400, Advance Information VME Subsystem Bus (VSB) Gate Array, 1986
Texas Instruments	The TTL Data Book, Volumes 1-4, 1984
Xicor	Data Book, 1985
Zilog	Zilog Components Data Book, 1985

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1.4.2 Other Documents

EIA RS-232C	Interface for Equipment Employing Serial Binary Data Interchange,
EIA RS-449	General Purpose 37-Position and 9-Position Interface for Data Terminal Equipment Employing Serial Binary Data Interchange,
IEC MVBESB/D2	The Parallel Sub System Bus of the IEC 821 Bus, Revision C, November 1986
IEEE P1014/D1.2	A Proposed Standard Backplane Bus Specification for Advanced Microcomputer Systems, October 1985

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2. SPECIFICATIONS

2.1 General

This chapter lists the environmental specifications, the power requirements, and the performance of the SVME-122 Single Board Computer. This card meets the requirements of the IEE P1014 VMEbus Specification.

2.2 Environmental Specifications

The humidity and temperature ranges for both card operations and storage are:

* Operational Temperature and Humidity - 0 degree C - 50 degree C, 95% non-condensing, sea level to 5000 m

* Storage Temperature and Humidity - -62 degree C to 71 degree C, 100% non-condensing

2.3 Power Requirements

Refer to Table 2-1, Power Requirements.

Table 2-1
Power Requirements

Source	Voltage	Current Maximum	Current Typical
Main	+5.0 Vdc (+5%, -2.5%)	6.6 A	4.0 A
Main	+12.0 Vdc (+5%, -2.5%)	300 MA	180 MA
Main	-12.0 Vdc (+5%, -2.5%)	300 MA	180 MA

2.4 Performance

This section details the performance of the SVME-122 Single Board Computer with respect to its functional characteristics. These functional characteristics include:

* CPU Access to on-board devices

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2.4.1 Local CPU Access

Table 2-2, Local CPU Read and Write Access Times, lists the wait states that the local CPU experiences for read and write accesses when accessing on-board devices. These devices include the Floating Point Processor (FPP), the Serial Communications Controller (SCC), the Counter/Timer and Parallel I/O (CIO), and the various on-board memory devices.

Table 2-2
Local CPU Read and Write Access Times

Parameter	Number of Wait States Read Access	Write Access
CPU Access to EPROM	4	4
CPU Access to SRAM	0	0
CPU Access to Local Registers(1)	2	2
CPU Access to FPP	2-4	2-4
CPU Access to SCC (2)	14-22	14-22
CPU Access to Control Memory	2	2
CPU/Cache Hit Read Access	1	1
CPU Access to CIO (2)	14-22	14-22
CPU Access to MVSB-2400 CSR	4	4

NOTES: 1. Local registers refer to the following registers: Control Register A, Location Monitor FIFO Register, and Control Register B.

2. First Access to these devices is as indicated. Subsequent accesses are 63 wait states.

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3. FUNCTIONAL DESCRIPTION

3.1 General

This section describes the functions of the SVME-122 Single Board Computer under each major functional block. These major blocks are:

* 68020 microporocessor
* 68881 Floating Point Processor (FPP)
* Z8536 Counter Input/Output (CIO)
* Z8530 Serial Communications Controller (SCC)
* memory
* Location monitor
* reset conditions
* VMEbus interface
* interrupt controller functions
* Built-in Test Equipment (BITE)
* interrupt handler
* requester
* faceplate control
* system integration features

Refer to Figure 3-1, SMVE-122 Single Board Computer Block Diagram.

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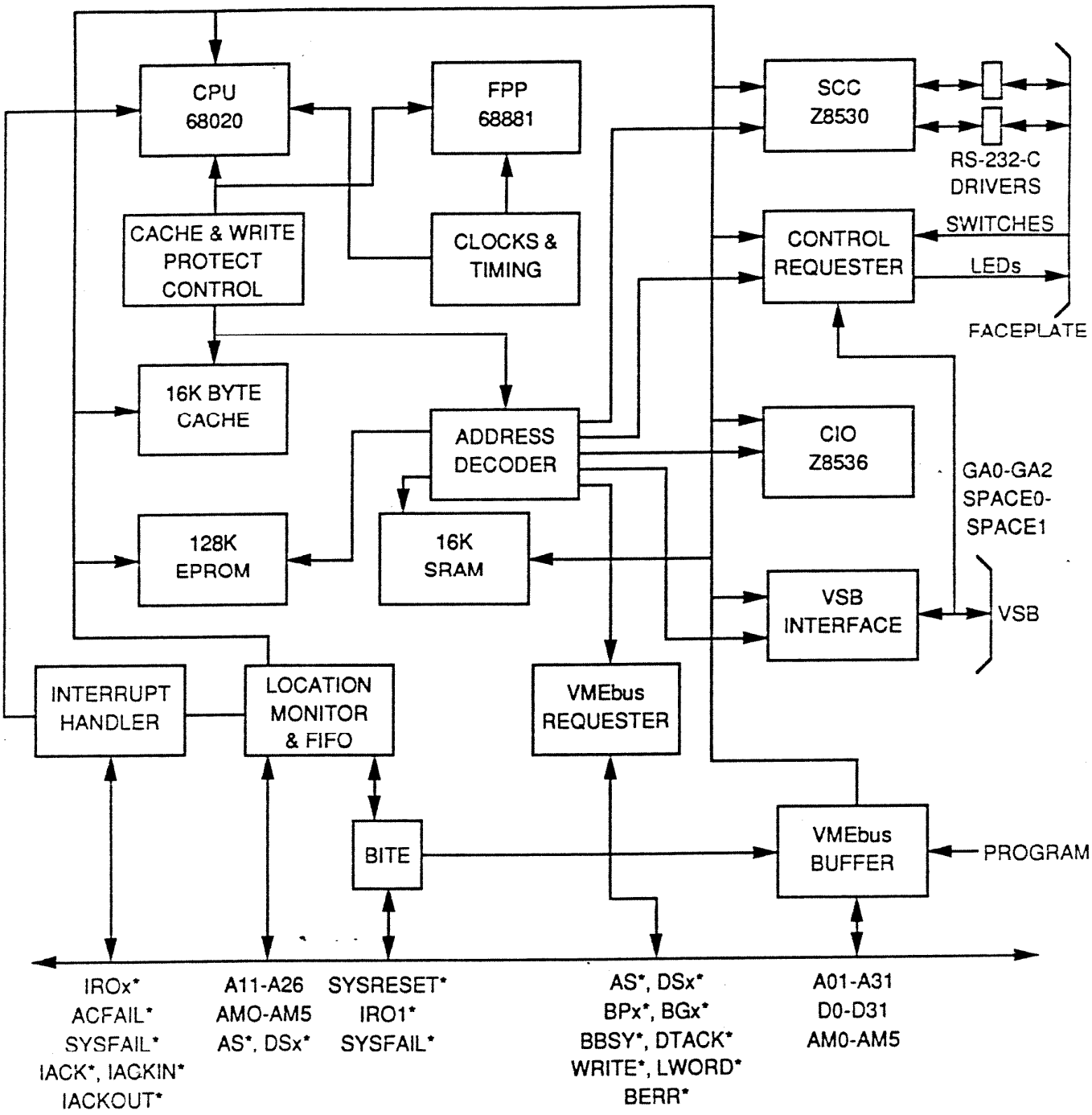


Figure 3-1. SVME-122 Single Board Computer Functional Block Diagram

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3.2 68020 Microprocessor

The SVME-122 Single Board Computer uses the 68020 microprocessor. The following specify the functions that deal with the CPU:

* CPU memory map
* clock circuitry
* reset logic
* halt logic
* bus error logic
* Data Size Acknowledge (DSACK) logic
* CPU interrupts
* CPU cache logic
* CPU Read-Modify-Write (RMW) cycles
* non-aligned transfers

3.2.1 CPU Memory Map

The CPU memory map is detailed in Chapter 5, Programming Interface

3.2.2 Clock Circuitry

There are two crystal controlled oscillators on the SMVE-122. The first oscillator provides a 33.333 MHz signal which, when divided by two, provides the CPU clock signal of 16.666 MHz. The second oscillator provides a 2.4576 MHz signal which provides the clock signal for the onboard SCC and CIO.

3.2.3 Local CPS Reset (RESET/)

The reset instruction, which does not affect any internal registers, does assert the RESET/ line. As an input, RESET/ provides the highest level of exception and provides system initialization and recovery from catastrophic failure.

Refer to Section 3.8, reset conditions, for detail.

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3.2.4 Local CPU Halt (HALT/)

During CPU double bus fault conditions, the CPU asserts the HALT/ signal as an output.

During EPROM programming mode when PROG/ signal is asserted, the HALT/ is asserted as an input to the CPU.

In any halt condition, when HALT/ is asserted the halt LED is activated.

3.2.5 Local CPU Bus Error (BERR/)

Asserting the local CPU bus error (BERR/) signal causes the CPU to execute exception processing. Bus error exceptions, which occur during a bus cycle when external logic aborts the cycle by asserting BERR/, occur under the following conditions:

* when the CPU attempts an access to any other coprocessor with a coprocessor ID different than 1 (refer to Section 5, Programming Interface),
* when the CPU attempts an access to the Floating Point Processor (FPP with a coprocessor ID=1) and the FPP is not installed (FPPSENSE/=1),
* when the CPU attempts a breakpoint acknowledge cycle,
* when the CPU attempts an "Access Level Control" cycle (when CPU attempts a call module (CALLM) or module return (RTM) instruction),
* when a VMEbus BERR* is asserted on VMEbus,
* when a VSB ERR* is asserted on VSB,
* or write accesses to VMEbus or VSB bus when the "Write Protect User" [and in "user mode"] or "write Protect Supervisor" [and in "Supervisor mode"] bits are asserted (state=high),
* when the CPU attempts to perform a VMEbus cycle while SVME-122 is in Bi-mode.

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3.2.6 Local CPU Data Size Acknowledge (DSACK/)

The Data Size Acknowledge (DSACK/) logic terminates local CPU cycle and informs the CPU what port size was accessed (refer to Table 3-1, Port Sizes). The DSACK/ signal timing enables the wait states to be inserted.

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Table 3-1
Port Sizes

Port Description	Port Size
EPROM	16 bits
SCRAM	32 bits
Serial Communications Controller (SCC)/ Counter Input/Output (CIO)	8 bits
Control/Status Registers	16 bits
FIFO	16 bits
Floating Point Processor (FPP)	32 bits
Control Memory	8 bits
VSB Control Registers	16 bits
VSB Access	32 bits
VMEbus Access	See Table 3-2

Table 3-2
VMEbus Access Port Sizes

CPU Address Range	VMEbus Address Cycle	Port Size
0000 0000 - 00FF FFFF	A24	32 bits
0100 0000 - FFD8 0000	A32	32 bits
FFF8 0000 - FFFC 0000	A32	32 bits
FFFF 0000 - FFFF FFFF	A16	32 bits

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3.2.7 Local CPU Interrupts

Interrupt Levels: The local CPU has seven prioritized interrupt levels. The SVME-122 SBC interrupts from the following sources:

* on-board interrupts
* any of the five VMEbus interrupts (see NOTE 1)
* VMEbus SYSFAIL*
* VMEbus ACFAIL*

NOTE 1: The VMEbus interrupt, IRQ1*, is used for Bi-mode entry and hence it is not usable as normal function for IRQ1*. The VMEbus interrupt request level 7, IRQ7* is not supported by SVME-122.

Vectors: A vectored interrupt occurs when the interrupting device places the interrupt vector number on the data bus. An auto-vectored interrupt occurs when the interrupted device (CPU) generates the vector number internally and then calculates the vector address. The source of vectored and auto-vectored interrupts are shown in Table 3-3.

Table 3-3. 68020 uP Interrupt Source Priority Levels

Priority Level	Interrupt Source
7	ACFAIL*, SYSFAIL*, BI-mode or abort switch (a)
6	CIO or VMEbus IRQ6* (b)
5	SCC or VMEbus IRQ5* (c)
4	VMEbus IRQ4*
3	VMEbus IRQ3*
2	VMEbus IRQ2*
1	VMEbus IRQ1* See Note 1 Above

NOTES: a) ACFAIL*, SYSFAIL* BI-mode, or abort switch generate an auto-vectored interrupt. Control/status bits are provided to determine which source generated the interrupt.
b) The CIO interrupt daisy-chain gives it priority over the VMEbus IRQ6*.
c) The SCC interrupt daisy-chain gives it priority over the VMEbus IRQ5*.

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3.2.8 CPU Cache Logic

The CPU cache memory stores the active code segment of the major routines. This saves the CPU from accessing the external memory and reduces the total execution time of the program. Refer to the MC68020 32-bit Microprocessor User's Manual for details.

The user-software can enable or disable the cache on the CPU.

3.2.9 CPU Read-Modify-Write (RMW) Cycles

The CPU provide multiprocessor operations which generate indivisible Read-Modify-write Cycles (RMC): Test and Set (TAS), Compare and Swap (CAS), and the dual-CAS (CAS2). Special provisions are required to allow proper VMEbus operation while using these operations.

In order to ensure that the SMVE-122 does not give up the VMEbus during RMC accesses, the requester shall not release the VMEbus AS* throughout the VMEbus RMW cycle. This prevents CAS2 instructions from operating on multiple addresses over the VMEbus. Therefore, the CAS2 instruction is not supported over the VMEbus by the SVME-122.

The SVME-122 VSB master interface asserts the VSB LOCK* signal during the CPU RMW cycles.

3.2.10 Non-Aligned Transfers

The CPU generates non-aligned bus cycles on the VMEbus (UART). Refer to the IEEE Standard for a Versatile Backplane Bus: VMEbus for details.

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3.3 68881 Floating Point Processor

A 68881 Floating Point Processor (FPP) is installed on the SVME-122 SBC. The FPP is accessed as a 32-bit coprocessor in the CPU space of the microprocessor as described in Chapter 5, Programming Interface. The FPP also supports the complete 68020 Coprocessor Interface. The FPP operates at the same clock rate as the CPU (16.7 MHz). The Coprocessor ID code is fixed at 1 (refer to Chapter 5, Programming Interface).

The FPPSENSE/signal enables the CPU to determine whether or not the FPP is present. The FPPSENSE/signal is readable by the CPU (refer to Chapter 5, Programming Interface). A bus error is returned to the CPU if an access is attempted to the FPP and no FPP is installed.

3.4 Z8536 Counter/Timer and Parallel I/O (CIO)

The Z8536 Counter/Timer and Parallel Input/Output (CIO) provides the following:

* three counter timers
* the local interrupt controller
* Control and Status Registers (refer to Chapter 5, Programming Interface).

3.4.1 Counter Timers

The Counter/Timer and Parallel Input/Output (CIO) is driven by a 2.4576 MHz clock signal. It has three 16-bit programmable counter/timers; each are provided with the 2.4576 MHz clock input signal. Refer to Chapter 5, Programming Interface, for the address of each timer and how each timer is accessed.

Counter/Timer 1 (Tick Clock): Counter/timer 1 can provide a tick clock functions. Each time this free-running clock times out, an interrupt (if enabled) is sent to the local CPU via the CIO interrupt request. Timer 1 provides tick periods up to 25 msec apart.

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Counter/Timer 2 (Watchdog Timer): Counter/timer 2 can provide a watchdog timer function. A watchdog timer is a low frequency timer which can be used as a sanity monitor for the CPU. The software must continuously restart it within a time-out period of each assertion of the watchdog timer. Note that the watchdog time-out period can be a maximum of 1500 seconds when timer 1 is used as a prescaler for the watchdog timer. This timer has no effect when it is timed out. The Watchdog function is inactive on local reset and does not start until timer 2 in initialized. (This timer may be configured to generate an interrupt).

Counter/Timer 3 (General Purpose Timer): Counter/Timer 3 is programmable as a general purpose timer. The time-out period is programmable up to .25 msec.

3.4.2 Interrupt Controller

The Counter/timer and Parallel Input/Output (CIO) is used as an interrupt controller as follows:

The port A of the CIO is used to concatenate the interrupt sources ACFAIL*, SYSFAIL*, ABT/RST, Bi-mode, VSB IRQ* and the Location Monitor (LM) interrupt.

The port B of the CIO is used as an output register to mask any or all of the lower six of the seven VMEbus interrupt requests (IRQ1* - IRQ7*) plus the ACFAIL*.

The port C of the CIO contains the two bits necessary to interface to the X2404M serial EEPROM, the FPPSENSE/ input and a VBBSYOUT/ input for Software Control (clearing this bit (set to 1) asserts the BBSY* Signal on pin 1B of P1 connector of the VMEbus).

NOTE: The CIO Software reset command should not be used.

3.5 Z8530 Serial Communications Controller (SCC)

The Z8530 Serial Communications Controller (SCC) provides two asynchronous serial channels with RS-232C interfaces.

The channels have independent software programmable baud rates up to 38400 baud. The SCC is capable of generating vectored interrupts to the local on-board CPU. The serial interface is a DE-9S type connector located on the front panel. Table 3-4 provides the serial port DE-9S pinouts.

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Table 3-4 DE-9S Pinouts

Pin No.	Signal Name	Direction
1	R_{xDB}	Input
2	TxDB	Output
3	RxDA	Input
4	TxDA	Output
5	Gnd	-
6	CTSB	Input
7	CTSA	Input
8	RTSA	Output
9	RTSB	Output

3.6 Memory

3.6.1 Erasable Programmable Read Only Memory (EPROM)

Types: The SVME-122 Single Board Computer has two byte-wide EPROM units which support JEDEC standard ROM. EPROM, or 28-pin paged EPROM devices. The EPROM can be used for both the boot function and non-volatile program storage. On power-up or reset, the microprocessor requires an initialization vector at address location 0000 0000. The byte wide devices (27512S) are organized to present a 16-bit port to the CPU (64K x 16-bit).

EPROM Map: The EPROM starts at address location FFE8 0000. If the selected device address range is smaller than the total allocated address range of the EPROM, then the contents of that device is repeated throughout the entire address range of the device. Therefore, there are eight images of the 128K byte EPROM in the allocated IM address space.

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Boot Program Location: On power-up/reset, the EPROM is mapped into address locations 0000 0000 to 0010 0000 and FFE8 0000 to FFF8 0000. During the monitor initialization period. The user-software may disable the BOOT/ bit which maps the VMEbus into the lower address location and leaves the EPROM in the upper address location only. Refer to Chapter 5, Programming Interface.

3.6.2 Serial Electrically Erasable Programmable Read Only Memory (EEPROM)

The SVME-122 SBC supports a single 512 x 8-bit serial Electrically Erasable Programmable Read Only Memory (EEPROM) for non-volatile storage. This device is an Xicor X2404 (or equivalent) and can be accessed via port C of the CIO. Refer to Chapter 5, Programming Interface, for details. Each byte in the EEPROM can only be write accessed 10,000 times before the memory retention of the cell degrades. The EEPROM is used for CLD/SLD purposes in which the System Configuration Table (SCT) is stored.

3.6.3 Static Random Access Memory (SRAM)

The SVME-122 Single Board Computer supports 4K by 32-bit wide static RAM. The SRAM read and write cycles are completed in zero wait states.

3.6.4 Cache Memory

The SVME-122 supports 4K by 32-bit wide Cache memory. This memory is the upper half of the four 8K x 8 SRAM chips on the SVME-122. The lower half of the SRAMs is used for normal SRAM accesses and was described in Para. 3.6.3. The Cache read (under Cache hit condition) cycle is completed in one wait state.

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3.7 Location Monitor

The location monitor is an interprocessor interrupt module that monitors write cycles that are being executed on other boards across the VMEbus. If an A32 access occurs which results in a match between A26-A19 address lines and the location monitor locations (programmable), the A32ON-bit is set to 1, and address bits A18-A10 are all high, then the address lines A02-A09 are latched into a FIFO after the FIFO's setup time requirement is met. When the data is latched into the FIFO, the Location Monitor interrupt is asserted to the Interrupt Controller (CIO port A input PA4). The Location Monitor interrupt is removed only when the FIFO is emptied.

If an A24 access occurs which results in a match between address lines A24-A16 and the location monitor locations, the A24ON-bit is set to 1, and address lines A15-A10 are all logic one then the address lines A09-A02 are latched into same FIFO after the FIFO's setup time is met. The FIFO is incapable to distinguish between the two address access modes (A24 of A32). The FIFO is an eight bit wide read-only register whose bits reflect the data currently at the top of the Location Monitor FIFO stack. This port must be read as a 16-bit port or the data may not end up in the correct byte location. After reset the FIFO is cleared and a read obtains indeterminate data.

The setup time requirement of the FIFO, which maybe thought of as a recovery time for subsequent latching of the data, mandate that the falling edge of the VMEbus AS* on a second location monitor access must occur at least 160 nsec after the falling edge of the VMEbus AS* for the first access. If cycles occur faster than 160 nsec, it becomes indeterminate which of the two data will be latched into the FIFO. The Location Monitor location is software programmable. The location bits are discussed in Chapter 5, Programming Interface.

3.7.1 Location Monitor/FIFO Error Conditions

If a write access is attempted to the Location Monitor FIFO when the FIFO buffer is full, the internal write pointer is blocked from write enable to the FIFO and external changes in write Enable (FWRITE/) will not affect the FIFO and the cycle is completed normally.

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If a read access is attempted from the Location Monitor FIFO when the FIFO buffer is empty, the internal read pointer is blocked from read enable to the FIFO and external changes in read enable (FREAD/) will not affect the FIFO and the cycle is completed normally and the received date is indeterminate.

3.7.2 Location Monitor/FIFO Interrupt

The CPU receives Location Monitor Interrupts (priority level 6, CIO or VMEbus IRQ6*) which can be software masked via the CIO. Refer to Chapter Five, Programming Interface and Table 3-3, Local CPU Interrupts.

The SVME-122 can access its own Location Monitor at the local (read) or VMEbus (write) address while another card in the system can only write access the SVME-122's Location Monitor at the VMEbus address. The LM interrupt is enabled by user by programming the CIO mask interrupt for LM interrupt enable.

3.8 Reset Conditions

3.8.1 Internal Reset (RESET/)

The internal reset line (RESET/) is asserted from:

* VMEbus system reset (SYSRESET*)
* ABT/RST switch

VMEbus System Reset (SYSRESET*): The RESET/ signal activates upon assertion of the SYSRESET* signal from the VMEbus.

3.8.2 VMEbus System Reset (SYSRESET)*

The VMEbus SYSRESET* line is asserted from the following sources:

* power-on reset
* software reset (SWRST) control bit (refer to Chapter 5, Programming Interface)

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Power-on Reset: The power-on reset circuit holds the VMEbus SYSRESET* signal in the reset state for 1.0 s (± 800 ms) after the +5 V power inputs have reached a minimum of 4.75 V.

NOTE: The VMEbus SYSRESET* assertion is done by the SVME-222 (SYSCON) card.

3.8.3 Internal Reset (RESET/) Assertion Effect

When the internal reset line (RESET/) is asserted the following events take place:

* SVME-122 goes into BI-mode
* All local devices (SCC, CIO, FPP, VSB-chip) are reset
* VSB is disabled
* All bits in the Control Register A (CRA) are set to zero

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3.9 VMEbus Interface

The SVME-122 Single Board Computer is compatible with the VMEbus standard as defined in IEEE P1014. The SVME-122, SBC provides a Master Interface only.

3.9.1 Master Interface

Data Path: The data path out of the card accommodates 8-, 16-, 24-, and 32-bit transfers. The VMEbus interface supports the indivisible Read-Modify-Write (RMW) cycles as described in Subsection 3.2.9, CPU Read-Modify-Write (RMW) Cycles.

Address Out Path: The 68020 microprocessor can access short, standard, and extended address spaces on the VMEbus. Refer to Table 3-5, VMEbus Accesses.

Table 3-5
VMEbus Accesses

Local Address Range	Type of Access	VMEbus Size Data	VMEbus Size Address
FFFF 0000 - FFFF FFFF	short VMEbus	32 bit	16 bit
FFF8 0000 - FFFC 0000	extended VMEbus	32 bit	32 bit
0100 0000 - FFD8 0000	extended VMEbus	32 bit	32 bit
0000 0000 - 00FF FFFF	standard VMEbus	32 bit	24 bit

Notes:

1. Long VMEbus cycles (32-bit transfers with LWORD* asserted) are generated in address spaces that have 32 bits of data.
2. The standard VMEbus access (D32, A24) allows the SVME-122 SBC to interface to cards with a 32-bit data bus.
3. If the VSB interface is enabled (refer to Chapter 5, Programming Interface), all accesses in the standard and extended VMEbus address ranges are attempted on the VSB first.

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Notes: If no device with that address is present on the VSB, a normal VMEbus cycle is endeavored provided that the BOUNCE control bit of the VSB register is set. Otherwise a VSB ERR* will occur.

4. During an A24:D32 standard VMEbus access, only the lower 24 bits of the address are used on the VMEbus.

3.9.2 Requester

The Requester has two modes of operation. These modes are: Release on Request (ROR) and Release When Done (RWD) and are selected by a control bit in the Control Register B (refer to Chapter 5, Programming Interface). Both modes use early release of the Bus Busy (BBSY*) signal. Note that the BBSY* signal is asserted for the duration of the RMW cycle regardless of the mode of operation. The Requester level is software programmable by a control bit in the Control Register B (refer to Chapter 5, Programming Interface).

3.9.3 Interrupt Handler (IH)

The Interrupt Handler supports six interrupt levels. Depending on the configuration of the Interrupt Mask Register (IMR), the interrupt handler responds to some of the VMEbus and the local CPU interrupt levels. Refer to Chapter 5, Programming Interface.

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3.10 VSB Interface

The SVME-122 SBC implements a master-only VME Subsystem Bus (VSB) Interface. The card is designed to be compatible with the IEC 821 VSB specification (Revision C). Refer to the Parallel Sub System Bus of the IEC 821 Bus Specification, for details.

The following features are supported by the SVME-122 SBC:

* serial bus arbitration
* 8-, 16- and 32-bit data transfers
* use of the VSB LOCK* signal for indivisible TAS, CAS and CAS2 instructions
* Wait and Address Decode Complete functions
* polled interrupt handling
* geographical addressing

The VSB interface on the SVME-122 SBC uses a Motorola MVSB2400 device. Refer to the Advance Information VME Subsystem Bus (VSB) Gate Array data sheet.

3.10.1 Enabling the VSB Interface

The VSB Interface on the SVME-122 SBC is enabled or disabled by the user via a write access to the VSBEN bit in the Control Register B (refer to Chapter 5, Programming Interface). The VSB interface is disabled on power-up, on internal or system reset and on entry into BI-mode.

When enabled, any VMEbus cycle attempted by the CPU (0100 0000 to FFD8 0000) is first attempted as a VSB cycle. If the address requested is not present on the VSB, the cycle is then attempted on the VMEbus in the normal procedure. It is recommended that the user disable the VSB interface when it is known that the address is not present on the VSB. Note that the BOUNCE Control bit must be set in the VSB Control register if a bounce need to occur.

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3.10.2 VSB Cycle Termination

If the VSB transfer is successful, or the transfer is completed normally across the VMEbus, the CPU cycle terminates normally and the user is not aware of which cycle just occurred. If the cycle terminates with a VSB ERR*, or a VMEbus BERR* signal, the CPU's bus error exception handler is executed, thus leaving the user unable to determine on which bus the error occurred. If the BOUNCE bit is not set, then no VMEbus cycle occurs in case of VSB cycle attempt when requested address is not available on the VSB. In this case only ERR* occurs.

The cycle maybe repeated while one bus access is disabled in order to determine which bus access caused the CPU's bus error exception handler execution, in case of repeat of the bus error.

3.11 Built-In Test Equipment (BITE)

3.11.1 Bus Isolation Mode (BI-mode)

Bus Isolation mode (BI-mode) prevents a hardware failure on the SVME-122 SBC from disrupting the VMEbus by not driving the VMEbus mastership bussed signals (except SYSFAIL*) and passing all daisy-chained signals unaffected. BI-mode does permit minimal slave accesses.

Bus Tri-Stating: Table 3-4, BI-mode Connector Usage, shows how the SVME-122 Single Board Computer configures the VMEbus and I/O signals in BI-mode.

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Table 3-4
BI-mode Connector Usage

Signal Name	Normal Usage	BI-mode™ Usage	Notes
VMEbus Mastership Bussed Signals			
D0 to D31	bidirectional data	tristated	-
A1 to A31	bidirectional address	input only	1
AM0 to AM5	bidirectional codes	input only	1
AS*, DS0*, DS1*	bidirectional strobes	input only	1
WRITE*	bidirectional write	input only	-
BERR*	bus error, input only	unaffected	-
DTACK*	data transfer acknowledge input	unaffected	-
IACK*	interrupt handler output and decode input	tristated	-
IRQ6*& TO IRQ1*	interrupt request inputs	unaffected	-
BR3* TO BR0*	possible outputs	not driven	-
ACFAIL*	input power FAIL	unaffected	-
SYSFAIL*	bidirectional FAIL	unaffected	-
BBSY*	bidirectional bus-busy	input only	-
LWORD*	bidirectional strobe	input only	1
SERCLK, SERDAT	not used	not used	-
Daisy-Chain Signals			
IACKIN*	as per P1014 usage	unaffected	-
IACKOUT*	as per P1014 usage	unaffected	-
BGXIN*	as per P1014 usage	unaffected	-
BGXOUT*	as per P1014 usage	unaffected	-

NOTE 1:
The SVME-122 exits BI-mode:

i) If local CPU writes to Control Register A (CRA) in such a way that the EXITBI-bit is asserted,
ii) if an access is made from the VMEbus to the SVME-122's Location Monitor.

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3.11.2 BI-mode Entry

The SVME-122 Single Board Computer enters BI-mode when one of the following is activiated:

* power-on reset
* the internal RESET line
* the VMEbus IRQ1* signal (if so strapped)
* the IRQ1* from VMEbus generates a level 1 auto-vectored interrupt to the local CPU

Entering BI-mode sends an interrupt to the CPU via the CIO.

The user software must enable the Interrupt Mask Register (IMR) in the CIO (refer to Chapter 5, Programming Interface).

Note that an interrupt can occur when the SVME-122 SBC enters or exits BI-mode. The BIMODE-bit in the Interrupt Control Register (refer to Chapter 5, Programming Interface), indicates when the SVME-122, SBC is in BI-mode.

Local CPU Accesses in BI-mode: In BI-mode, the local CPU can access all on-board devices. However, if the CPU tries to access the VMEbus (or a VSB access is bounced to the VMEbus) during BI-mode, on-board logic asserts the BERR/ signal.

VMEbus Master Accesses in BI-mode: A master on the VMEbus can perform a write access to the SVME-122 SBC's location monitor for one cycle. This cycle initiates the exit process from BI-mode. All other VMEbus attempts to access this card are ignored; the SVME-122 SBC is effectively removed from the VMEbus.

3.11.3 BI-mode Exit

The SVME-122 Single Board Computer exits BI-mode via one of the following methods:

* a VMEbus master writing to any odd word in the on-board location monitor
* a VMEbus master writing to any aligned long word in the on-board location monitor
* the local CPU writing to Control Register A which asserts the EXITBI-bit
* a VMEbus master writing to the on-board location monitor using a VMEbus Unaligned Transfer (UAT).

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3.11.4 BI-mode Master

If a card is compatible with BI-mode and the IRQ1* signal on the chassis backplane is strapped for BI-mode, the SVME-122 Single Board Computer can place that card in BI-mode by asserting a software control bit (refer to Chapter 5, Programming Interface). Asserting this software control bit asserts the P1 bussed IRQ1* signal (if so strapped).

When the SVME-122 Single Board Computer has been removed from BI-mode, it can remove other BI-mode compatible cards from BI-mode by accessing the location monitor on these cards.

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3.12 Faceplate Control

3.12.1 Faceplate LEDs

The following paragraphs describe the operation of the four faceplate LEDs on the SVME-122 Single Board Computer. Asserting the internal RESET signal turns on all LEDs except for the HALT LED.

USLED (Upper Status) LED: This amber LED turns on when the USLED/ signal (under user-software control) is set to 0. It also turns on when the internal RESET signal is activated. This LED turns off when the USLED/ bit in the Control Register A is set to 1 (refer to Chapter 5, Programming Interface). The default state of this LED is "ON".

LSLED (Lower Status) LED: This amber LED turns on when the LSLED/ signal is asserted (which is activated by the assertion of the internal RESET signal or by user-software). It turns off when the LSLED/ bit in the Control Register A is set to 1 (refer to Chapter 5, Programming Interface). The default state of this LED is "ON".

FAIL LED: This red LED turns on when the internal FAIL signal is activated, which is activated by the FAIL/ bit (refer to Chapter 5, Programming Interface). The FAIL/ bit is activated in hardware by an internal reset which asserts MYFAIL/ bit. This LED turns off when the MYFAIL/ bit is deasserted (refer to Chapter 5, Programming Interface). The default state of this LED is "ON".

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HALT LED: This amber LED turns on when the local CPU HALT signal is active. It turns off when the local CPU HALT signal is inactive. The HALT LED is lit dimly during access by CPU to the onboard I/O and the VSB. The dimly lighted state of the HALT LED should not be considered as halt state of the CPU. The default state of this LED is "OFF".

3.12.2 Status Switches

On the faceplate there are two toggle switches which are readable by user-software. They are labelled FS1 and FS0. Refer Chapter 5, Programming Interface, for their status bit definition. The state of these switches is reported in the ID Register (IDR).

3.12.3 ABT/RST Pushbutton

A momentary contact toggle switch (labelled ABT/RST) is located on the faceplate. The ABT/RST switch sends an interrupt to the local CPU directly. Note also that the status of this switch can be determined by reading the ABORT/ bit in the CIO port A (refer to Chapter 5, Programming Interface).

3.12.4 DE-9 Connector

The DE-9 connector (labelled CH.A and CH.B) is located on the faceplate. It provides the serial RS-232C signals. Refer to paragraph 3.5, Table 3-4 for connector pin configuration or to Chapter 4, Hardware Configuration.

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4. Hardware Configuration

4.1 General

This chapter describes the hardware configuration of the SVME-122 Single Board Computer and includes the following information:

* Factory Set Jumper Block Configuration
* External Connectors
* EPROM programming facilities for on-board programming

4.2 Factory Set Jumper Block Configuration

Table 4-1, Factory Set Jumper Block Configuration, details the configuration of the jumper blocks when this board is received from the vendor. Table 4-2, SVME-122, SBC, Jumper Configuration Reference indicates the configuration of each jumper block.

Figure 4-1 shows the location of the Jumper Blocks.

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HARDWARE CONFIGURATION

Table 4-1

SVME-122 SBC Factory Set Jumper Blocks

JUMPER BLOCK	TITLE	CONFIGURATION	DESCRIPTION OF FUNCTIONALITY
JB1	Test Jumper	-	Test 1
JB2	VSB Installation Select	-	VSB interface installed
JB3	BI-mode forced exit	1-2	EXITBI controlled by Control Register A
JB4	VMEbus/EPROM Boot	1-2	Boot from EPROM
JB5	EPROM configuration	1-2 5-6 7-8 9-10 15-16	Uses 27512's EPROM " " " "
JB6	EPROM Programming	3-4 5-6 7-8 9-10 13-14	Normal EPROM Operation " " " "
JB7	BI-mode Select	1-2	SVME-122 will enter BI-mode when IRQ1* is asserted on VMEbus
JB8	Watchdog Reset Reset Switch	-	No rest on watchdog time-out Abort interrupt only when ABT/RST switch is toggled

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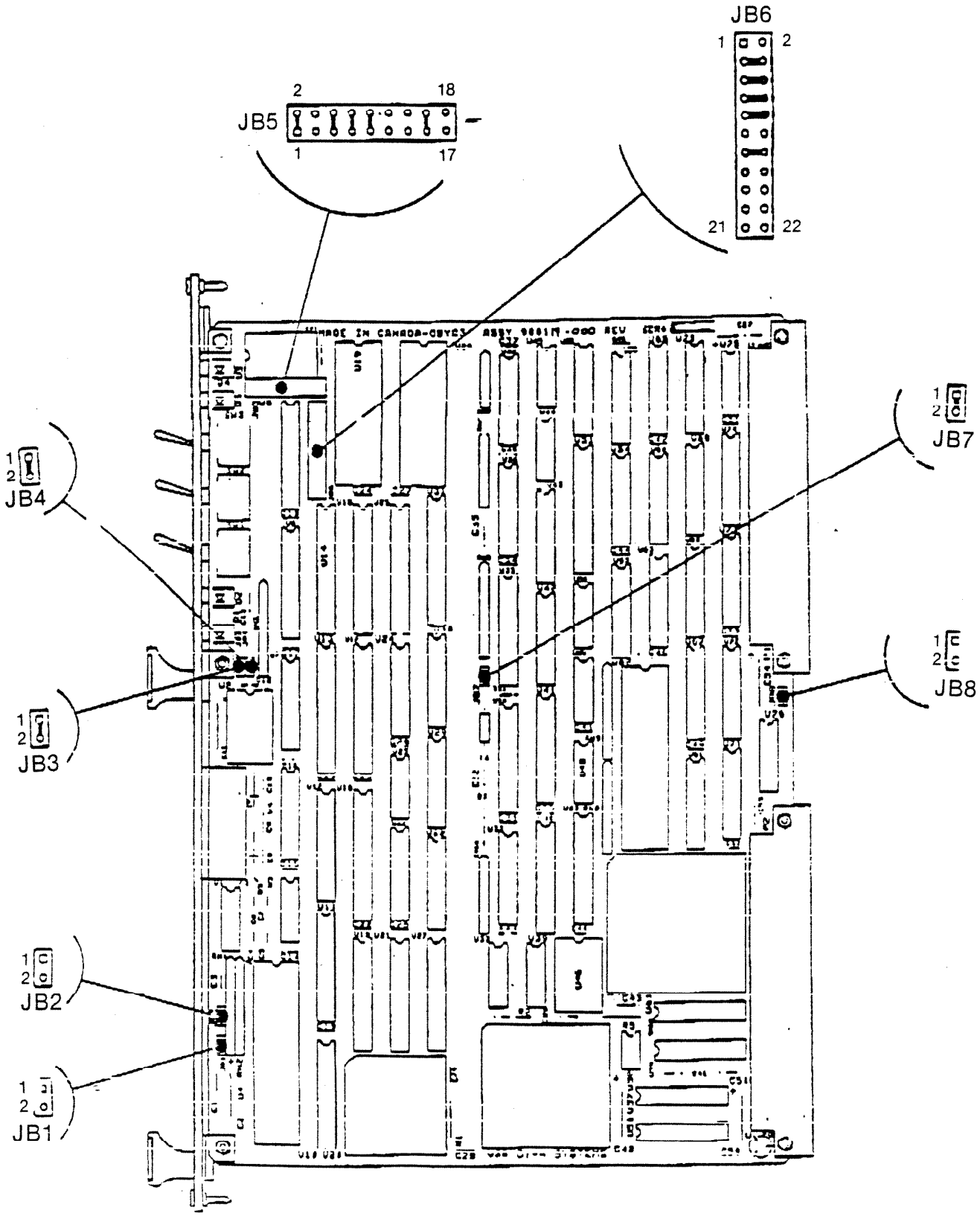


Figure 4-1. SVME-122 SBC Factory Set Jumper Blocks

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Table 4-2 SVME-122, SBC, Jumper Configuration Reference

JUMPER TABLE	
JB NO.	CONFIGURED
1	-----
2	-----
3	1 - 2
4	1 - 2
5	1 - 2 5 - 6 7 - 8 9 - 10 15 - 16
6	3 - 4 5 - 6 7 - 8 9 - 10 13 - 14
7	1 - 2
8	-----

Table 4-2 SVME-122, SBC, Jumper Configuration Reference

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4.3 External Connection Summary

4.3.1 P1 Connector

The pin assignments for the P1 connector is a standard IEEE P1014 configuration. Refer to Table 4-3, P1 Pin Assignments.

4.3.2 P2 Connector

The P2 connector is used as a VSB interface connector in addition to its VMEbus signals, according to standard IEEE P1014 and IEC 821 configuration . Refer to Table 4-4, P2 Pin Assignments.

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Table 4-3
P1 Pin Assignments

PIN NUMBER	ROW A SIGNAL MNEMONIC	ROW B SIGNAL MNEMONIC	ROW C SIGNAL MNEMONIC
1	D00	BBSY*	D08
2	D01	(BCLR*)	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG1OUT*	GND
10	(SYSCLK)	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	(SERCLK)	A17
22	IACKOUT*	(SERDAT)	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12 V	(+5 V STDBY)	+12 V
32	+5 V	+5 V	+5 V

NOTES:

1. Those signals enclosed in parentheses () are not used by the SVME-122 SBC Card.

2. All signals are at TTL levels, except for +12 V and -12 V.

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Table 4-4
P2 Pin Assignments

PIN NUMBER	ROW A SIGNAL MNEMONIC	ROW B SIGNAL MNEMONIC	ROW C SIGNAL MNEMONIC
1	AD00	+5V	AD01
2	AD02	GND	AD03
3	AD04	RESERVED	AD05
4	AD06	A24	AD07
5	AD08	A25	AD09
6	AD10	A26	AD11
7	AD12	A27	AD13
8	AD14	A28	AD15
9	AD16	A29	AD17
10	AD18	A30	AD19
11	AD20	A31	AD21
12	AD22	GND	AD23
13	AD24	+5V	AD25
14	AD26	D16	AD27
15	AD28	D17	AD29
16	AD30	D18	AD31
17	GND	D19	GND
18	IRQ*	D20	GND
19	DS*	D21	GND
20	WR*	D22	GND
21	SPACE0	D23	SIZE0
22	SPACE1	GND	PAS*
23	LOCK*	D24	SIZE1
24	ERR*	D25	GND
25	GND	D26	ACK*
26	GND	D27	AC
27	GND	D28	ASACK1*
28	GA0	D29	ASACK0*
29	GA1	D30	CACHE
30	GA2	D31	WAIT
31	BGIN*	GND	BUSY
32	BREQ*	+5V	BGOUT*

NOTE: All Signals are at TTL levels.

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4.4 DE-9 Connectors

The serial RS-232 signals appear at the DE-9 connector on the faceplate. Table 4-5 DE-9 Pin Assignments, details the pin out of the faceplate connector.

Table 4-5

DE-9 Pin Assignments

SIGNAL	MNEMONIC	DE-9 CONNECTOR PIN	DE-9 CONNECTOR DIRECTION
Receive Data, Port B	RxDB	1	input
Transmit Data, Port B	TXDB	2	output
Receive Data, Port A	RXDA	3	input
Transmit Data, Port A	TXDA	4	output
Signal Ground	GND	5	N/A
Clear to Send, Port B	CTSB	6	input
Clear to Send, Port A	CTSA	7	input
Request to Send, Port A	RTSA	8	output
Request to Send, Port B	RTSB	9	output

NOTES: 1. The DE-9 connector is configured as a DCE (Data Communications Equipment) interface.

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4.5 EPROM Programming Facilities For On-board Programming

4.5.1 GENERAL

Equipment required for the in-circuit programming includes the target card (i.e. the card to be programmed), a standard EPROM programmer, an adapter card, a test chassis, an umbilical cable, an EPROM cable, and wire-wrapping equipment.

The EPROM cable connects the programmer's socket to the adapter card. The programmer will still act as if an EPROM device was in its programming socket. It is the responsibility of the adapter card and the SVMB-122 card to ensure that the proper programming signals reach the EPROM.

The adapter card is plugged into the test chassis, and drives the VMEbus and the umbilical to the SVME-122 card with information derived from the EPROM programmer's signals. This information includes address, data, control information, and programming voltages. When received by the SVME-122 SBC, this information is used to program the on-board EPROMs.

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HARDWARE CONFIGURATION

Isolation of the signals required for normal operation and programming is achieved by using a wirewrapped header. During normal operation, the necessary connections are made by wirewrapping the appropriate pairs of header pins.

To prepare the SVME-122 for programming, the wire wraps are removed from the header and the umbilical cable's connector is inserted onto the header. For 512 Kbit EPROMs, the umbilical routes the programming voltages (+6V for Vcc and +12.5V for Vpp) and a signal named PROG/, which reconfigures the on-board logic to support the in-circuit programming. The SVME-122 is then plugged into the test chassis's VMEbus. The signals received over the VMEbus and umbilical drive the address, data, power supply and control pins of the EPROMs, which are programmed one at a time.

Note that additional signals described below are required for 1 Mbit and larger EPROMs (the current SVME-122 utilizes 512 Kbit EPROMs, 27512-type). The in-circuit EPROM may now be programmed as if it was in the programmer's socket. When the programming is done, the target board is removed from the test chassis, the umbilical cable removed, and the header rewrapped.

It is assumed that 30 AWG wire will be used for the wire wrapping, with each wrap able to carry 400 mA (derated). Since all EPROMs share a common OE*/Vpp signal and the current requirement for Vpp is low, a single header pin will suffice for Vpp (and for the other signals).

Table 4-6 describes the states and the sources of the various header signals for both programming and normal operation. The Vpp and PGM/ signals are only required for 1 Mbit and larger EPROMs. Note that a configuration jumper block will be placed between the programming header and the EPROMs for the accommodation of different sized EPROMs.

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Table 4-6

Signal States and Sources

SIGNAL	NORMAL OPERATION	PROGRAMMING	COMMENTS
Vcc	+5V VME power rails	+6V Programmer	
OE*/Vpp	OE* On-board decoder	Vpp Programmer	
PROG/	Inactive On-board pullup	Active low Adapter Card	
Vpp	+5V VME power rails	Vpp Programmer	See note 1
PGM/	Inactive On-board pullup	PGM/ Programmer	See note 1

NOTES: 1. The Vpp and PGM/ signals are only required for 1 Mbit and larger EPROMs.

Figure 4-2 shows the equipment configuration for programming the EPROMs on the SVME-122 SBC.

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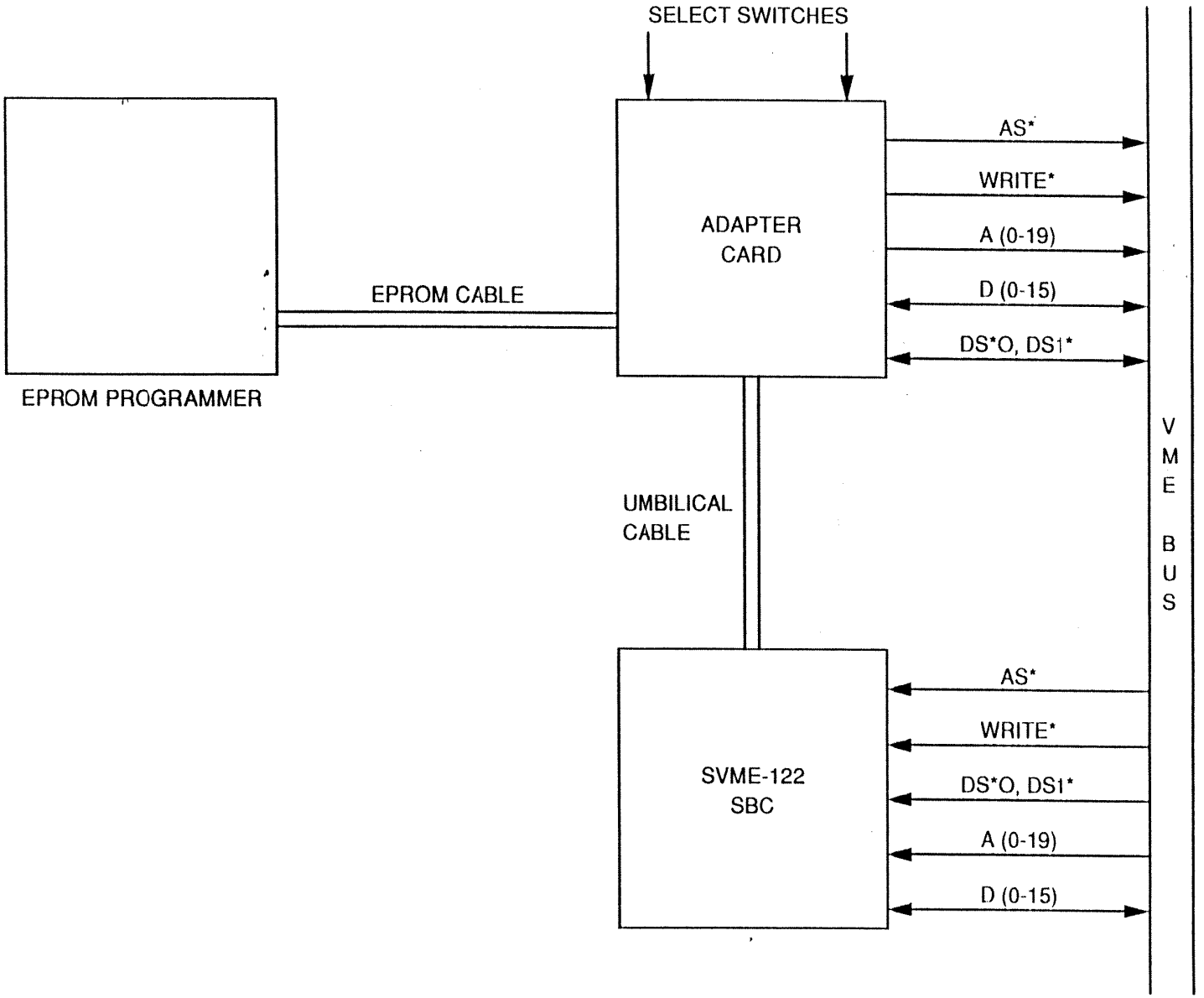


Figure 4-2. EPROM Programming Facilities

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4.5.2 Adapter Card Input Signals

The cable connecting the adapter card and the programmer's programming socket provides the following signals:

A0-A15	-	offset of byte within the EPROM
D0-D7	-	data to be programmed
Vcc	-	+6V for programming and verification
OE*/Vpp	-	+12.5V for programming, or V(il) for verification
CE*	-	used as a programming pulse and as a chip enable for verification

Note that D0-D7 are outputs for programming and inputs for verification. Figure 4-3 shows the relative signal timing for these EPROM programmer signals. Vcc is shown at either +5V or at +6V, OE*/Vpp at either V(il) or +12.5V, and the other signals at either V(ih) or V(il).

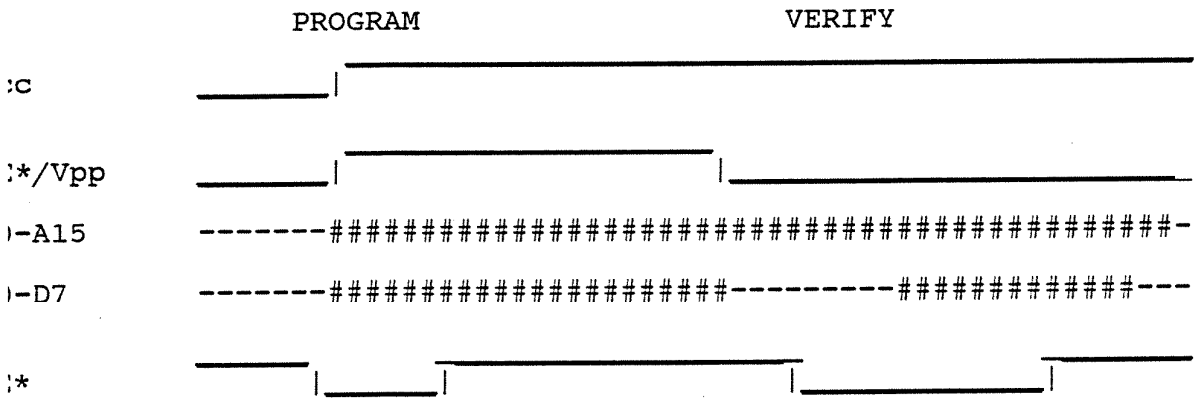


Figure 4-3 Relative EPROM Programmer Signal Timing

5.3 SVME-122 Card Behavior

The adapter card must generate a PROG/ signal, which is sent to the SVME-122 over the umbilical and causes it to enter a programming mode. All on-board activity is halted, the address and data buffers are turned on, and all other bus-driving logic is disabled.

The EPROM chip enable signals are derived from the address and data strobe signals from the VMEbus.

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Because the SVME-122 provides a D16 interface for on-board addressing of bytes within the EPROM, the addresses presented to the SVME-122 card must be incremented by two.

5.4 Adapter Card Description

5.4.1 Block Diagram

A block diagram of the adapter card is shown in Figures 4-4a and 4-4b. Note that all of the blocks shown are simple combinatorial logic blocks, mostly for decoding purposes. It requires a configuration switch, shown in Table 4-7, to customize its operation.

Table 4-7 Adapter Card Configuration Switches

SWITCH NAME	FUNCTION
Even/Odd Byte Select	Used to select a particular EPROM, and determines which VMEbus Data Strobe signal is used.

5.4.2 VMEbus Signals

The signals in Table 4-8 are output from the adapter card over the VMEbus. The exact timing of these signals is constrained only by the EPROM programmer's timing and the particular combinatorial delays associated with the adapter card, the VMEbus, and the SVME-122 card.

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Table 4-8 VMEbus Signals

D00-D15	data lines for byte read and write
A01-A22	address for CE* decoding and EPROM addressing
DS0*	odd byte select
DS1*	even byte select
WRITE*	controls data buffer direction for prog. (writing) and verification (reading)
LWORD*	select longword transfers

D00-D15 are the two byte lines for even and odd bytes. When programming, the same byte of data may be asserted on both byte lines if this simplifies the adapter's logic, but for verification, only one of the two byte lines will be routed back to the EPROM programmer. Selection of the proper data byte line is based on the even/add byte select switch. The direction and timing of the data buffers is derived form the programmer's OE*/Vpp signal. When OE*/Vpp is at +12.5V, the programmer is programming the EPROM, so the data buffers are writing to the VMEbus. When OE*/Vpp is at V(il), the programmer is verifying the EPROM data, so the buffers are reading from the VMebus. VMebus data lines D16-D31 are not used.

Table 4-9 defines the mapping between the programmer and the VMEbus addresses for the SVME-122. Note that address shift of one bit is required for the SVME-122.

Address lines A31-A20 are not used, since the SVME-122's decoders will be disabled for programming and they are not needed for addresssing future larger EPROMS.

Table 4-9 SVME-122 VMEbus Address Signals

VMEbus Signal	Derived from:
A01-A16	A0-A15 (programmer)
A17-A22	EPROM select switches (adapter)

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HARDWARE CONFIGURATION

The values of DS0* and DS1* shall be controlled by a switch that will select either the even or odd byte for programming. Note that only one of these signals will be active in any cycle, so a single switch is sufficient for controlling them. The SVME-122 CE* decoder uses the DSx* signals in its decoding, then the proper CE* timing (at the EPROM to be programmed) may be ensured by driving the proper DSx* line using the EPROM programmer's CE* output.

WRITE* will control the direction of the SVME-122'S data buffers. It operates in conjunction with the adapter's data buffers, and is derived in the same way as the data buffer direction. It must be inactive (i.e., reading from the traget card) during verification, when the programmer signal OE*/Vpp is low (at Vil), Vcc is at +6V, and CE* is low (active).

LWORD* is always inactive high, since only byte transfers will be allowed for programming the EPROMs.

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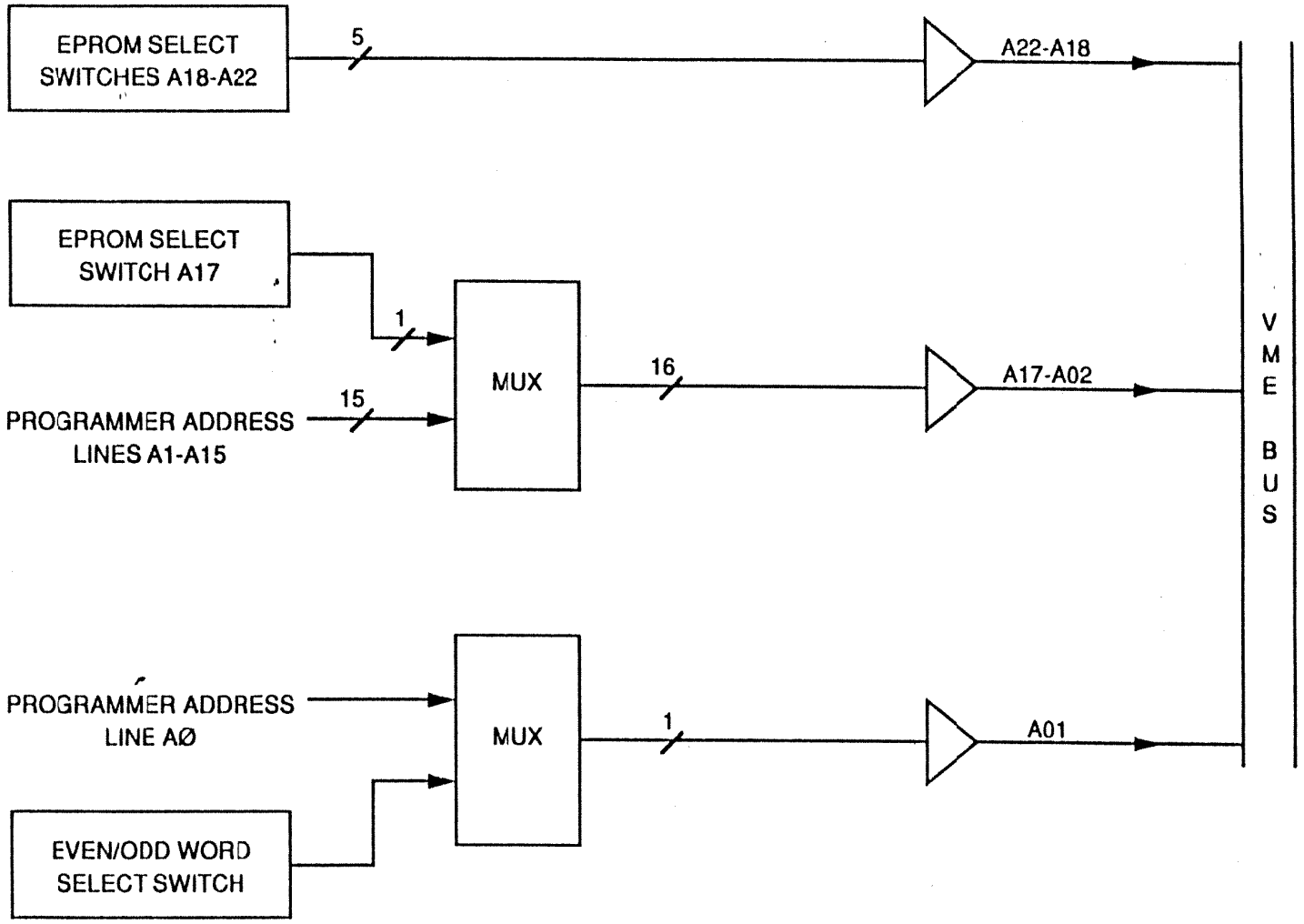


Figure 4-4a. VME bus Signal Generator (Adapter Card)

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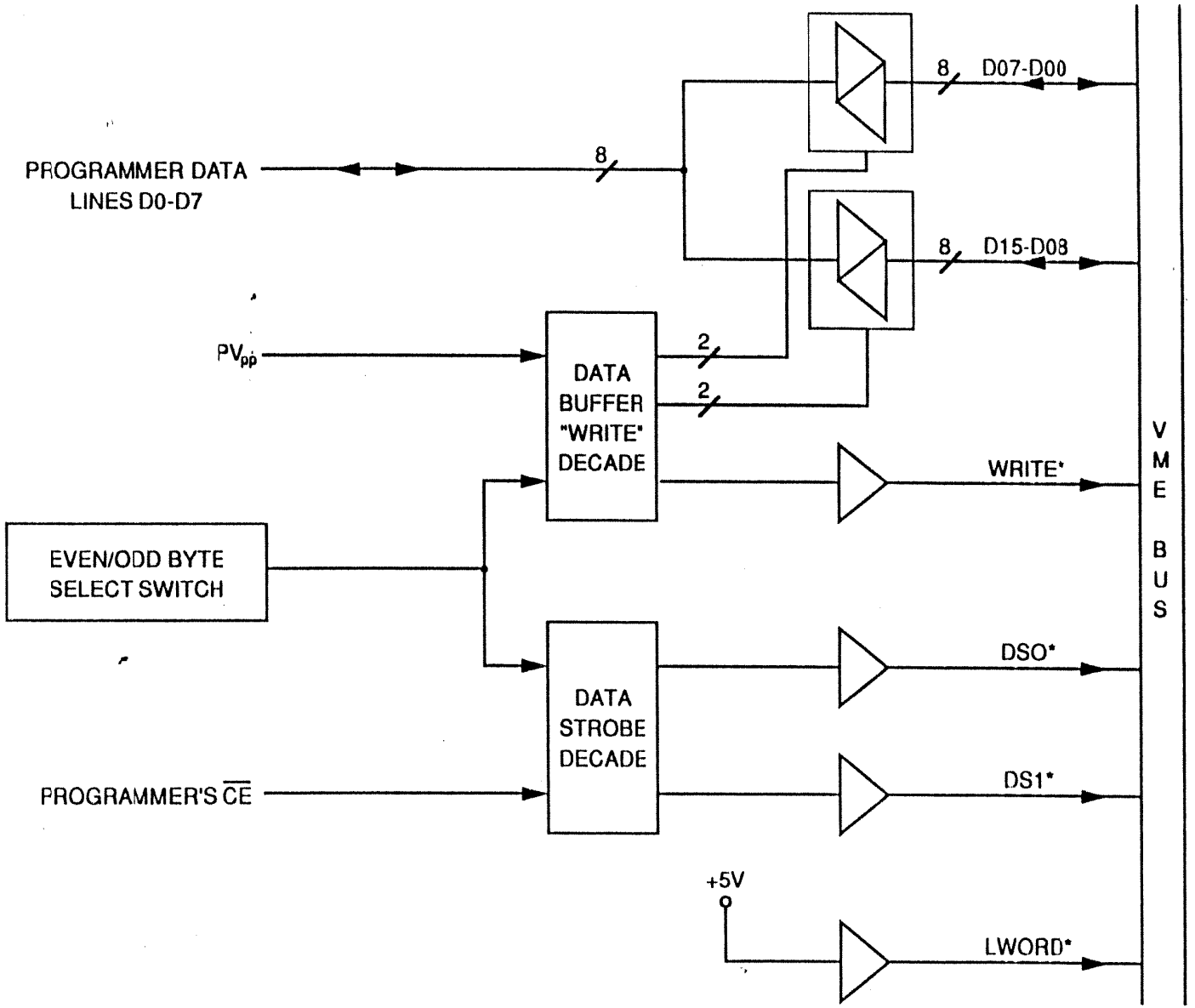


Figure 4-4b. VME bus Signal Generator (Adapter Card)

EPS 02802.D07

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.5.4.3 Umbilical Signals

The signals described in Table 4-10 is the output from the adapter card over the umbilical. The exact timing of these signals is determined by the EPROM programmer's timing and the particular delays associated with the adapter and the target card. The umbilical's Vpp (as opposed to the OE*/Vpp signal) and PGM/ signals are only used by EPROMs of 1Mbit or greater in size. While they may be provided for upgradeability, they are not discussed here.

Table 4-10 Umbilical Cable Signals

OE*/Vpp	+12.5V for programming. Vil for varifying.
Vcc	+6V for programming and verifying.
PROG/	used to reconfigure on-board logic.
GND	common ground.
Vpp	+12.5V (for 1Mbit EPROMs).
PGM/	programming pulse (for 1Mbit EPROMs).

The +6V programming voltage for Vcc could be routed directly to the SVME-122 from the programmer. The PROG/ signal is always active low for programming and is a low fanout signal.

5.4.4 Programming Header

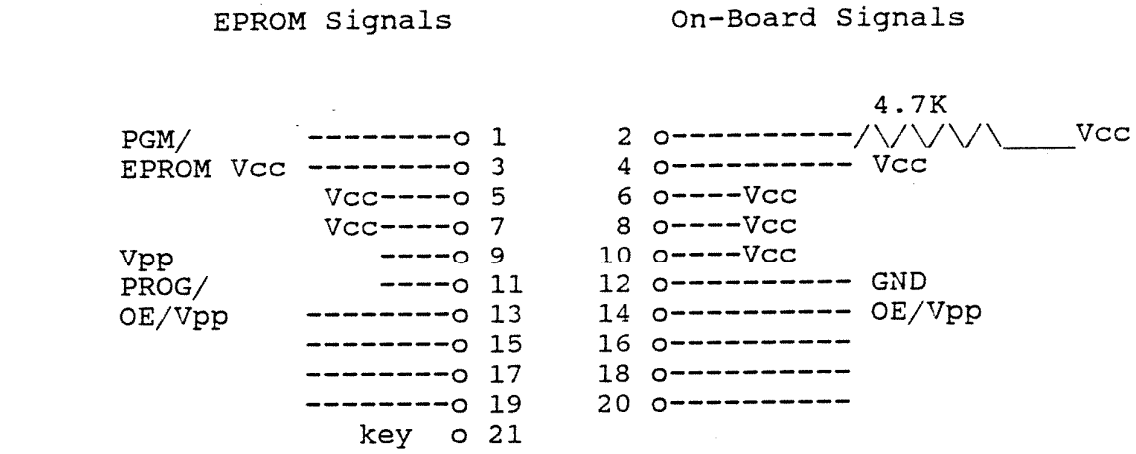
The SVME-122 card will have a programming header that will be used as a connection point for the umbilical and its signals. The header's wire wrap pins will also be used for making connections for normal operation. Figure 4-5 SVME-122 Header Pinouts, shows the header pins configuration for normal and programming modes.

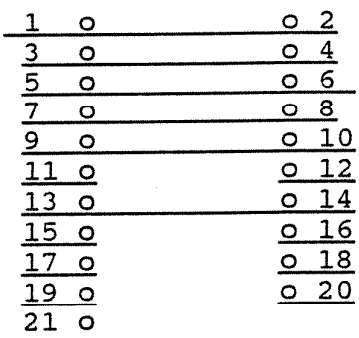
5.4.5 Umbilical Connector

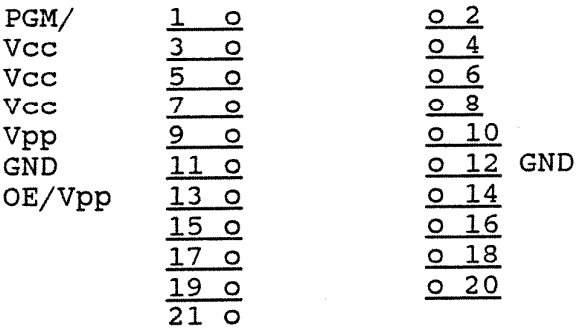
The umbilical connector is shown in Figure 4-6. The pinout shown should be superimposed on Figure 3 to determine connectivity to the onboard signals.

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HARDWARE CONFIGURATION







Normal Configuration

Programming Configuration

Figure 4-5 SVME-122 Header Pinouts

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Adapter Signals

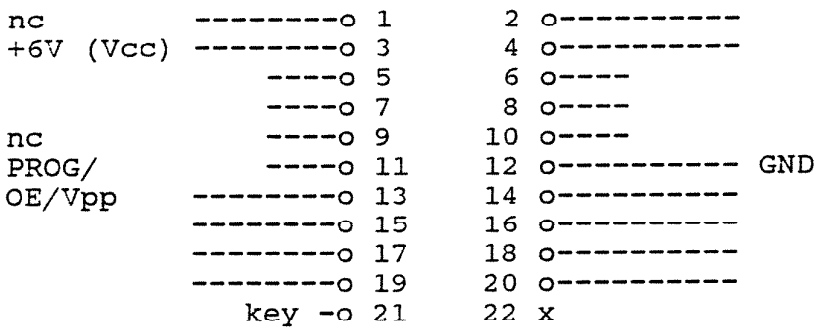


Figure 4-6 Umbilical Connector Pinout

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5. PROGRAMMING INTERFACE

5.1 General

This section describes the user-software interface. Included are the following:

* Local CPU Address Map
* CIO Accesses
* SCC Accesses
* Local I/O Accesses
* VMEbus Accesses
* CPU Space Address Decoding
* VSB Bus Address Decoding
* VSB Control Register Accesses
* VSB Memory Address Decoding

5.2 CPU Address Map

Table 5-1, CPU Address Map, details the address map for the 68020 microprocessor. Unless stated otherwise, all addresses are in hexadecimal notation and the unit of size is in Byte.

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Table 5-1 CPU Address Map

ADDRESS	DESCRIPTION	SIZE
FFFF FFFF		
	Short VME accesses (A16:D32)	64K
FFFF 0000		
	ID Register	32K
FFFE 8000		
	Location Monitor FIFO	32K
FFFE 0000		
	Control Register B	32K
FFFD 8000		
	Control/Status Register A	32K
FFFD 0000		
	CIO Accesses	32K
FFFC 8000		
	SCC Accesses	32K
FFFC 0000		
	VSB or VME (A32:D32) Accesses	127.988K
FFFA 000C		
	VSB Control Reg or VME (A32:D32)	12K
FFFA 0000		
	VSB or VMS (A32:D32) Accesses	128K
FFF8 0000		
	EPROM	1M
FFE8 0000		
	On-Board SRAM	1M
FFD8 0000		
	VSB or VME (A32:D32) Accesses	3.864G
0100 0000		
	Standard VME accesses (A24:D32)	15M
0010 0000		
	EPROM if BOOT asserted, else Standard VME accesses (A24:D32)	1M
0000 0000		

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5.2.1 CPU Space Address Decoding

The CPU space accesses are decoded as detailed in Table 5-2, CPU Address Decoding. Note that the CPU space is available when certain instructions occur (for example; coprocessor, breakpoint, call module, return module) and exception handling. Refer to MC68020 32-Bit Microprocessor User's Manual for details.

Table 5-2
CPU Address Decoding

CPU Space (A19 to A16)	Description	Response
0000	Breakpoint Acknowledge	BERR
0001	Access Level Control	BERR
0010	Coprocessor Communications	Note 1
1111	Interrupt Acknowledge	Note 2

NOTES:
1. Refer to Table 5-3, Coprocessor Communications Space for details.
2. Refer to Subsection 3.2.7, Local CPU Interrupts for details.

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Table 5-3
Coprocessor Communications Space

ID NUMBER	DESCRIPTION
0	BERR
1	FPP
2	BERR
3	BERR
4	BERR
5	BERR
6	BERR
7	BERR

NOTES:
1. A BERR occurs when the SVME-122 SBC attempts an access to any other coprocessor other than the Floating Point Processor (coprocessor ID 1).
2. ID Number 1 is FPP only if the FPP is installed; otherwise, the ID Number 1 is BERR.
3. ID Number refers to address lines A15-A13 when in CPU Space.

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5.3 Local I/O Accesses

Local I/O accesses are those accesses made to Control/Status registers, the Control memory, or to the SCC or the CIO. Accesses to the Control memory, SCC or CIO are made as accesses to an 8-bit port. Accesses to Control/Status registers are made to a 16-bit port.

The base address of the on-board Control/Status registers appear in Table 5-4, Local Registers Memory Map, which also indicates the port size and the access type. Table 5-5, abbreviations used in registers, defines the mnemonics used in Table 5-4 and within the contents of this section. Tables 5-6 to 5- detail the bit assignments of the registers in Table 5.

Table 5-4 Local Registers Memory Map

BASE ADDRESS RANGE	ACCESS TYPE	PORT-SIZE	REGISTER DESCRIPTION
FFFD 0000 to FFFD 7FFF	R/W	16-bit	CONTROL REGISTER A (CRA)
FFFD 8000 to FFFD FFFF	R/W	16-bit	CONTROL REGISTER B (CRB)
FFFE 0000 to FFFE 8000	R/O	16-bit	LOCATION MONITOR FIFO
FFFE 8000 to FFFE FFFF	R/O	16-bit	ID REGISTER (IDR)

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Table 5-5
Abbreviations Used in Registers

ABBREVIATION	MEANING
R/O	Read only (a WRITE to these bits causes no adverse effect)
R/W	Read/Write bit
W	Write only
N/A	Not Applicable (the sense of these bits are unknown at reset)
X	These bits are unused and unavailable
W/O	Write only
-	Value is dependent on the state of signal monitored

5.3.1 ID Register (IDR)

The ID Register is a 16-bit status register. It is Read/Only R/O) type. It is repeated 16K times in the address range of FFFE 8000 to FFFE FFFF, as indicated in Table 5-4. All 16 status bits reflect the states of the signals they monitor at all times.

The IDR is word addressable and its bit assignments are shown in Figure 5-1. Refer to Table 5-6, ID Register, for bit description.

D15	D14	D13	D12	D11	D10	D9	D8
X	FS1	FS0	SPACE1	SPACE0	GA2	GA1	GA0

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X

Figure 5-1 ID Register

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Table 5-6 ID REGISTER

BIT NAME	ACCESS RIGHTS	RESET CONDITION	DESCRIPTION
FS1	R/O	-	FACEPLATE SWITCH 1 0: UPPER FRONT PANEL SWITCH DOWN 1: UPPER FRONT PANEL SWITCH UP
FS0	R/O	-	FACEPLATE SWITCH 0 0: LOWER FRONT PANEL SWITCH DOWN 1: LOWER FRONT PANEL SWITCH UP
SP1	R/O	-	VSB SPACE 1 (SEE NOTE 1) 0: VSB SPACE 1 BIT LOW 1: VSB SPACE 1 BIT HIGH
SP0	R/0		VSB SPACE 0 (SEE NOTE 1) 0: VSB SPACE 0 BIT LOW 1: VSB SPACE 0 BIT HIGH
GA2	R/0		VSB GEOGRAPHICAL ADDRESS BIT 2 (NOTE 1) 0: GA2 BIT LOW 1: GA2 BIT HIGH
GA1	R/O		VSB GEOGRAPHICAL ADDRESS BIT 1 (NOTE 1) 0: GA1 BIT LOW 1: GA1 BIT HIGH
GA0	R/O		VSB GEOGRAPHICAL ADDRESS BIT 0 (NOTE 1) 0: GA0 BIT LOW 1: GA0 BIT HIGH

NOTE 1: The state of these bits are determined via backplace strapping.

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5.3.2 Location Monitor FIFO

The location monitor FIFO, which is a 16-bit ready/only register, is provided in the address range FFFE 0000 to FFFE 7FFF. The register is repeated 16K times in this range. A read from this register removes the top item from the location monitor FIFO.

The location monitor FIFO is word addressable and its bit assignments are shown in Figure 5-2. Refer to Table 5-7, Location Monitor FIFO, for bit description.

D15	D14	D13	D12	D11	D10	D9	D8
A9	A8	A7	A6	A5	A4	A3	A2

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X

Figure 5-2 Location Monitor FIFO

Table 5-7 Location Monitor FIFO

BIT NAME	ACCESS RIGHTS	RESET CONDITION	DESCRIPTION
A9..A2	R/O	-	STATE OF VMEBUS ADDRESS LINES A09...A02 DURING A WRITE ACCESS TO THE LOCATION MONITOR (LONGWORD WRITE ACCESS).

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5.3.3 Control Register B (CRB)

The Control Register B, which is a 16-bit control register, is read-writeable and is located in the address range of FFFd 8000 to FFFD FFFF. The register is repeated 16K times in this address range. On reset, all register bits are in an unknown state.

The bit pattern of CRB appears in Figure 5-3, and its bit description appears in Table 5-8, Control Register B.

D15	D14	D13	D12	D11	D10	D9	D8
RSTCH	ROR	MAE	VSBEN	A32ON	A24ON	BR1	BR0

D7	D6	D5	D4	D3	D2	D1	D0
LM7	LM6	LM5	LM4	LM3	LM2	LM1	LM0

Figure 5-3 Control Register B(CRB)

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Table 5-8 ID REGISTER

BIT NAME	ACCESS RIGHTS	RESET CONDITION	DESCRIPTION
LM7..LM0	R/W	N/A	Control bits for VMEbus base address of SVME-122 corresponding to valid VMEbus address lines A26..A19 for A32 accesses, and address lines A23..A19 for A24 accesses. LM2..LM0 are ignored for A24 accesses.
RSTCH	R/W	N/A	Reset Cache (Flush Cache) 0: Cache operates normally 1: Cache is flushed
ROR	R/W	N/A	Requester Option Selection 0: VMEbus ROR mode enabled (1) 1: VMEbus RWD mode enabled (1)
VSBEN	R/W	N/A	VSB Enable 0: VSB access is attempted in the given address range before a VMEbus access is tried (when the BOUNCE-bit is set in the VSB chip)(2) 1: No VSB access is attempted, direct VMEbus A32 occurs.
A32ON	R/W	N/A	Location Monitor A32 Address Selection 0: Location Monitor in A32 address range is enabled 1: Location Monitor Function in A32 address range is disabled
A24ON	R/W	N/A	Location Monitor A24 Address Selection 0: Location Monitor in A24 address range is enabled 1: Location Monitor in A24 address range is disabled
MAE	R/W	N/A	Memory Access Selection 0: The Control Memory is accessed when access to VMEbus/VSB is attempted 1: Access to VMEbus/VSB is normal
BR1.BR0	R/W	N/A	VMEbus Request Level Selection: BR1 BR0 VMEbus Request Level 0 0 Level 0 0 1 Level 1 1 0 Level 2 1 1 Level 3

NOTES: 1. ROR = Release on Request RWD = Release When Done
2. See VSB Control Register Access Section, Para.....

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5.3.4 Control Register A (CRA)

The Control Register A is a 16-bit register located in the address range FFFD 0000 to FFFD 7FFF. The CRA is read/writeable and is repeated 16K times in the indicated address range. On reset, all register bits are set to state 0.

The bit assignment of CRA appears in Figure 5-4. The bit description for CRA appears in Table 5-9, Control Register A.

D15	D14	D13	D12	D11	D10	D9	D8
X	X	X	X	X	X	X	X

D7	D6	D5	D4	D3	D2	D1	D0
EXITBI	BIMSK	LSLED	USLED	SYSFMSK	FAIL	ABITE	BOOT

Figure 5-4 Control Register A(CRA)

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5.4 Z8536 Counter Input/Output (CIO)

The SVME-122 is equipped with a Z8536 Counter/Timer Input/Output (CIO) chip to provide on board timing functions, and I/O bits to provide control and status functions. The CIO is equipped with four (4) on board registers for control of CIO functions.

Table 5-10, CIO Registers, provides the address of the CIO on-board registers. Refer to Zilog Components Data Book for further programming information.

Table 5-10 CIO Registers

ADDRESS	REGISTER ACCESSED
FFFC 8001	PORT C DATA
FFFC 8003	PORT B DATA
FFFC 8005	PORT A DATA
FFFC 8007	CONTROL REGISTER

There are 8K images of each register within the 32 Kbyte address space allocated for the CIO.

Access to the CIO registers is to an eight-bit (8-bit) port.

5.4.1 Port A of CIO, Interrupt Status Register (ISR)

An 8-bit interrupt status register is provided via the CIO Port A.

The bit assignment for the ISR is shown in Figure 5-5 and the bit descriptions are shown in Table 5-11.

Following an internal reset, the CIO output port is tri-stated, and must be programmed for interrupt operation.

The reset state of the bits reflects the state of their corresponding signal at that time.

D7	D6	D5	D4	D3	D2	D1	D0
SELFB1	TEST	VSBINT	LMINT	ACFAIL	SYSFAIL	ABORT	BIMODE

Figure 5-5 Interrupt Status Register

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Table 5-9 Control Register A(CRA)

BIT NAME	ACCESS RIGHTS	RESET CONDITION	DESCRIPTION
EXITBI	R/W	0	Exit Bimode locally 0: No effect 1: Exit Bimode (3)
B1MSK	R/W	0	Bimode Interrupt Mask Control 0: Bimode interrupt (level 7) is masked 1: Bimode interrupt (level 7) is enabled
USLED	R/W	0	Upper Status LED Control/Status 0: Upper statue LED ON 1: Upper statue LED OFF
LSLED	R/W	0	Lower Status LED Control/Status 0: Lower Status LED ON 1: Lower Status LED OFF
SYSFMSK	R/W	0	SYSFAIL* Interrupt Mask Control 0: SYSFAIL* interrupt (level 7) is masked 1: SYSFAIL* interrupt (level 7) is enabled
FAIL	R/W	0	SVME-122 Fail Status Control 0: SVME-122 Asserts VMEbus SYSFAIL* 1: SVME-122 Releases VMEbus SYSFAIL*
ABITE	R/W	0	Assert Bimode Line 0: Deassert BITE* By SVME-122 (1) 1: Assert BITE* by SVME-122
BOOT	R/W	0	Boot Code, in Local EPROM at address: 0000 0000 0: EPROM in lower CPU local memory address (2) 1: Normal (16 Mbytes) VMEbus A24 in lower CPU local memory address (2)

NOTES: 1. BITE* has been designated as the VMEbus IRQ1* line
2. See Table 5-1, CPU Address Map
3. Bimode exit will occur only if BITE* is not asserted or SELFBI is not asserted. See Interrupt Control Register (ICR) bit assignment.

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Table 5-11 Interrupt Status Register

BIT NAME	ACCESS RIGHTS	RESET CONDITION	DESCRIPTION
TEST	R/O	-	Test Jumper Status 0: Test Jumper installed (1) 1: Test Jumper not installed
VSBINT	R/O	-	VSB IRQ* 0: VSB interrupt pending 1: No VSB interrupt pending
LMINT	R/O	-	Location Monitor Interrupt 0: Location Monitor not empty 1: Location Monitor Empty
ACFAIL	R/O	-	VMEbus ACFAIL* 0: VMEbus ACFAIL* asserted 1: VMEbus ACFAIL* not asserted
ABORT	R/O	-	Faceplate ABT/RST Mometary Switch 0: ABT/RST switch depressed 1: ABT/RST switch released
BIMODE	R/O	-	SVME-122 Bimode Condition 0: SVME-122 in Bimode (2) 1: SVME-122 not in Bimode
SELFBI	R/W	*	Force SVME-122 into Bimode (3) 0: SVME-122 forced into Bimode 1: SVME-122 not in Bimode

NOTES: 1. The TEST is utilized in CLD/SLD purposes. If Test jumper is not installed, which asserts a 1 for TEST-bit, then the states of the faceplate switches FS0 and FS1 are used in determining the jump vector to which CLD software will exit to.
2. SVME-122 is capable of isolating itself from the VMEbus via SELFBI-bit or exit from isolation via EXITBI-bit.
3. Reset Condition is pulled high. Unpredictable results will occur if both SELFBI and the EXITBI are asserted simultaneously.

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5.4.2 Port B of CIO, Interrupt Mask Register (IMR)

An 8-bit interrupt mask control register is provided via the CIO Port B.

The bit assignment for the IMR is shown in Figure 5-6, and the bit descriptions are shown in Table 5-12.

The least significant bit of IMR is not available as an I/O pin. All writes to CIO Port B must have a logic 1 in this bit position.

Following a reset state, all IMR bits are tri-stated by the CIO but are pulled high by external logic.

D7	D6	D5	D4	D3	D2	D1	D0
ACMASK	MASK6	MASK5	MASK4	MASK3	MASK2	MASK1	1

Figure 5-6 Interrupt Mask Register

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Table 5-12 Interrupt Mask Register

BIT NAME	ACCESS RIGHTS	RESET CONDITION	DESCRIPTION
MASK 6	R/W	*	VMEbus IRQ6* Mask Control 0: IRQ6* will not cause interrupt 1: IRQ6* will cause interrupt
MASK 5	R/W	*	VMEbus IRQ5* Mask Control 0: IRQ5* will not cause interrupt 1: IRQ5* will cause interrupt
MASK 4	R/W	*	VMEbus IRQ4* Mask Control 0: IRQ4* will not cause interrupt 1: IRQ4* will cause interrupt
MASK 3	R/W	*	VMEbus IRQ3* Mask Control 0: IRQ3* will not cause interrupt 1: IRQ3* will cause interrupt
MASK 2	R/W	*	VMEbus IRQ2* Mask Control 0: IRQ2* will not cause interrupt 1: IRQ2* will cause interrupt
MASK 1	R/W	*	VMEbus IRQ1* Mark Control 0: IRQ1* will not cause interrupt 1: IRQ1* will cause interrupt
ACMASK	R/W	*	VMEbus ACFAIL* Interrupt Mask Control 1: ACFAIL* interrupt via Level 7 masked (disabled) 0: ACFAIL* interrupt via Level 7 enabled

* These bits are tri-stated by the CIO following a system reset, but are pulled high by external logic.

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5.4.3 Port C of CIO, Serial EEPROM Control Register (SECR)

Port C of the CIO is used as a 4-bit read/write control register.

The bit assignment for the SECR is shown in Figure 5-7. The bit descriptions for the SECR are shown in Table 5-13.

Following a reset state of all bits are tri-stated by the CIO, when applicable, but are pulled high by external logic.

D3	D2	D1	D0
ROMDAT	FPPSENSE	X	ROMCLK

Figure 5-7 Serial EEPROM Control Register

Table 5-13 Serial EEPROM Control Register

BIT NAME	ACCESS RIGHTS	RESET CONDITION	DESCRIPTION
ROMCLK	R/W	*	EEPROM Clock Input 0: Serial EEPROM clock input low 1: Serial EEPROM clock input high
ROMDAT	R/W	*	EEPROM Data (1) 0: Serial EEPROM data line low 1: Serial EEPROM data line high
FPPSENSE	R/O	-	Floating Point Processor (FPP) Status 0: FPP installed 1: FPP not installed

NOTES: (1) ROMDAT line should be programmed as "open drain."

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5.5 Z8530 Serial Communication Controller (SCC)

The Z8530 Serial Communication Controller (SCC) on the SVME-122 is clocked at 2.4576 MHz.

Table 5-14, SCC Registers, details the address of the available registers.

Refer to the Zilog Components Data Book for programming information.

The SCC provides two RS-232C Compatible Communications channels for the SVME-122.

There are 8K images of each register within the allocated 32Kbyte address space. Access to the SCC registers is to an 8-bit port.

Table 5-14 SCC Registers

ADDRESS	REGISTER
FFFC 0001	Channel B Command
FFFC 0003	Channel B Data
FFFC 0005	Channel A Command
FFFC 0007	Channel A Data

5.6 VSBchip Registers

The VSB interface to the SVME-122 SBC is provided via the XVSB2400 VSBchip from Motorola.

The VSBchip contains three 32-bit registers which are only accessible to the local processor. The organization of these registers is shown in Figure 5-8.

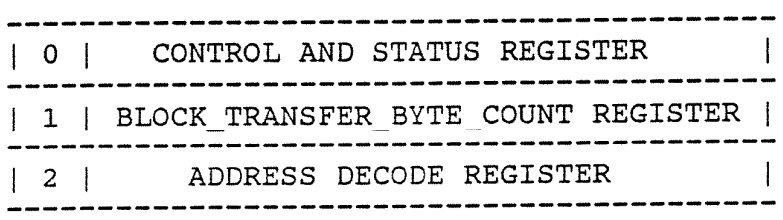


Figure 5-8 Registers of the VSBchip

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The Control and Status Register (CSR) allows software to control and configure the operation of the VSB chip. In addition it provides error status information that allows software to monitor the chip's interaction with the environment. Section 5.6.1 provides a detailed description of the CSR.

The Block-Transfer Byte-Count register allows software to control the number of bytes transferred during a VSB block-transfer cycle. In addition this register allows software to extend the 24-bit address of the 68010 to 32-bits. Section 5.6.2 provides a detailed description of the Block-Transfer Byte-Count register. The last register is the address decode register. It allows software to reconfigure the base address of the other two registers. This register is described in Section 5.6.3.

Note that DY-4's dual ported memory devices do not support block transfer cycle.

5.6.1 The Control and Status Register

The CSR allows software to control the operation of the VSBchip and to determine the cause of a bus error. Figure 5-9 shows the organization of the CSR. The CSR is accessed at an offset of 00 from the base address of the registers as defined by the contents of the address decode register (see Section 5.6.3). After the chip undergoes a reset sequence, and as long as the address decode register has not been changed, the CSR's address is FFFA0000. Bits 0-10 of the CSR provide control bits, while bits 11-15 provide status bits. Upon reset, the Control register, i.e., bits 00-10 of the CSR, are initialized to the binary value carried on the local data lines D00-D10. This feature allows the VSBchip to be configured to operate on a board that does not include a microprocessor. The CSR can be read and written to by software, allowing for dynamic reconfiguration of the operation mode of the chip.

D15	D14	D13	D12	D11	D10	D9	D8
ERR*	ASACK1*	ASACK0*	TIMEOUT*	WRERR*	FAIR*	ENTO0*	ENTO1*

D7	D6	D5	D4	D3	D2	D1	D0
X	MASTEREN*	READ ONLY	BOUNCE	TEN*	BLOCKEN*	X	SCON*

Figure 5-9 Control and Status Register

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PROGRAMMING INTERFACE

The bit descriptions for the VSBchip Control and Status Register appears in Table 5-15.

For detailed operatons of the VSBchip refer to the M(X)VSB2400 User's Manual, Revision 1.2, dated Dec. 14, 1987.

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Table 5-15 VSBchip Control and Status Register

BIT NAME	ACCESS RIGHTS	DESCRIPTION
SCON*	R/W	SYSTEM CONTROLLER The SCON* control bit is used to enable the VSB-chip to operate as the system controller. Clearing this bit to 0 enables the chip's arbiter.
BLOCKEN*	R/W	ENABLE BLOCK-TRANSFER MODE (2) In conjunction with the block-transfer byte count register, this bit allows software to initiate a block-transfer cycle. Writing a non zero value into the block-transfer byte=count register and then clearing BLOCKEN* to 0 will cause the master to operate in the block-transfer mode. The master will remain in the block-transfer mode until the byte-count register counts down to zero or ERR* was asserted in the course of the cycle which ever is encountered first.
TEN*	R/W	ENABLE 68010 MODE (2) The TEN* control bit allows software to configure the VSBchip to interface an MC68010 microprocessor to the VSB. This is accomplished by clearing the TEN* bit to 0. When in this mode, the master combines the upper eight bits of the block-transfer byte-count register with the 24-bits of address driven by the MC68010 to get the 32-bit address required by the VSB. In addition, during the data transfer phse of VSB cycles, the master swaps and replicates data bytes so as to comply with the data positioning requirements of both the VSB and the MC68010. When the TEN* control bit is set, the 68010 mode is disabled, and the master is configured to operate with a MC68020/MC68030 microprocessor. A detailed description of the operation of the master when in the 68010 mode is given in the VSBchip technical manual.
BOUNCE	R/W	ENABLE ADDRESS BOUNCE (4) The BOUNCE control bit allows software to increase the concurrency of the address decode and the address broadcast phase. Setting the BOUNCE bit to 1 enables the master to operate in the address-bounce mode. Clearing the bit to zero disables the address-bounce mode.

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Table 5-15 VSBchip Control and Status Register (Continued)

BIT NAME	ACCESS RIGHTS	DESCRIPTION
READONLY*	R/W	ENABLE READ ONLY MODE The READONLY* bit allows software to configure the chip to only use the VSB for the purpose of reading data. Clearing the bit to 0 enables the read-only mode, while setting it to one disables it.
MASTEREN*	R/W	ENABLE MASTER (3) The VSBchip allows onboard logic to disable the chip's VSB master by setting the MASTEREN* control bit to 1. This feature might be used when the ship is used to only provide a slave interface to the VSB. In this case, onboard logic will set the bit to one by driving D06 to high when RESET* is asserted. Clearing the MASTEREN* bit to 0 enables the master. However, it should be noted that the master will indeed be enabled only when both MASTEREN* is cleared and the SLAVE* input signal is negated.

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Table 5-15 VSBchip Control and Status Register (continued)

BIT NAME	ACCESS RIGHTS	DESCRIPTION
ENTO0 ENTO1	R/W	ENABLE TIMEOUT The transfer timer allows the subsystem to recover from a lockup condition when, due to a failure, a VSB slave does not properly respond to either address broadcast or the data transfer phase of VSB cycle. If a time-out occurs, the chip asserts the ERR* output signal, and the TIMEOUT* bit in the status register is cleared. The time-out period of the transfer timer is encoded as shown below: ENT01 / ENT00 / TIME-OUT PERIOD 0 / 0 / 64 microseconds 0 / 1 / 128 microseconds 1 / 0 / 256 microseconds 1 / 1 / Timer disabled
FAIR*	R/W	ENABLE FAIR REQUEST MODE The FAIR* bit is used to configure the requester to operate in the FAIR mode. Clearing the FAIR* bit to 0 will cause the requester to refrain from requesting the bus until the bus request line is negated. This allows bus requests from boards that are installed down the daisy-chain to be granted. NOTE: Fairness in accessing the bus will be achieved only if all the boards in the sub-system are configured to operate in the FAIR mode.
WRERR*	R/O	WRITE ERROR When cleared, this status bit indicates that on-board logic has attempted a write cycle to the VSB when the chip was configured to operate in the read-only mode. (1)
TIMEOUT*	R/O	BUS TIME OUT When cleared, this status bit indicates that the VSB transfer timer has timed out. (1)
ASACK0* ASACK1*	R/O	ADDRESS SIZE ACKNOWLEDGE (VSB) These two status bits reflect the state of the VSB ASACK0* and ASACK1* signal lines at the last time that ERR* was detected low. (1)
ERR*	R/O	VSB BUS ERROR (1) When cleared, this status bit indicates that the VSB ERR* signal was asserted in the course of a cycle.

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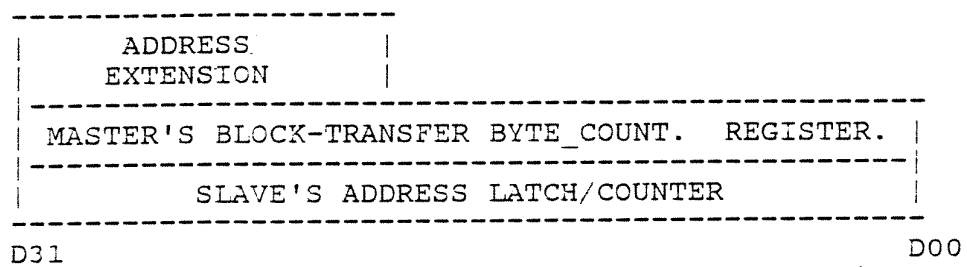


Figure 5-10 Uses of the Byte-Count Register

WARNING:

If software aborts a block-transfer cycle before it is completed and the chip relinquishes bus mastership, and if the chip's VSB slave is enabled, there is a possibility that the byte-count register will be overwritten with the address of the accessed byte locations. It is the responsibility of software to recover if the block-transfer cycle is to continue from the point of termination.

When the chip is configure to to operate in the 68010 mode the upper eight bits of the register constitute an address extension register. They are driven unto AD24-AD31 during the address broadcast phase of the VSB cycle, allowing a 69-1- to properly operate in the 32-bit address environment that the VSB provides.

WARNING:

When the 68010 mode is enabled, and at the same time, the master is enabled to operate in the block-transfer mode, all 32-bits of the byte-count register are considered to be a valid byte-count. It is the responsibility of software to correctly define the number of bytes to be transferred as a 32-bit data item, reinitializing the upper 8-bit address-extension register after the block transfer cycle is completed.

*The SVME-122 provides no block-transfer capability on VSB or on VMEbus.

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NOTES: 1) WRERR*, TIMEOUT*, ASACK0*, ASACK1* AND ERR* bits reflect the status when the most recent error condition was detected, i.e., ERR* was asserted. Reading the register causes all of its bits to be set to 1.

2) For SVME-122, set this bit to 1.

3) For SVME-122, SLAVE* is always negated.

4) For SVME-12 if BOUNCE=0 and VSBEN=0, then no access to VMEbus (A32:D32) is possible.

*5.6.2 Block-Transfer Byte-Count Register

The block-transfer byte-count register is accessed at an offset of 04 from the base address of the registers as defined by the contents of the address decode register (see Section 5.6.3. After the chip undergoes a reset sequence, and as long as the address decode register has not been changed, the register can be accessed at the address FFFA0004. The block-transfer byte-count register is designed tof ulfill multiple functions. Figure 5-10 shows the various function that the block-transfer byte-count register fulfills.

During the course of a master's block transfer cycle, all 32 bits of the register provide a byte-count register. Providing a 32-bit byte-count allows an onboard DMA controller to affect the transfer of up to 4 Gbyte of data in the course of a block-transfer cycle.

The clock transfer will be executed until the byte-count register decremented down to 0 or until ERR* was received low whichever occurs first.

When the chip's slave is responding to a VSB cycle, the 32-bit address carried on AD00-AD31 during the address broadcast phase, is latched into the block-transfer byte-count register. With each negation of DS* this address is incremented by four, providing the address for a potential subsequent data transfer executed in the course of a VSB block-transfer cycle.

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**5.6.3 Address-Decode Register

The address-decode register is used in master mode to hold the 32-bit staring address of the internal control and status registers. After reset the contents of this register are set to FFFA0000 which is the default address mentioned earlier. The contents of the address-decode register can be changed by using external logic to assert QAS* before AS*. PWRITE* must be asserted before asserting QAS* (see User's Manual). All transfers to this register should be 32-bit aligned.

**NOTE that the SVME-122 does not provide the external logic required to enable a change in the base address of the VSBchip Control and status register. Hence the base address of the VSBchip is not programmable.

5.7 VMEbus Accesses

VMEbus accesses are decoded to standard accesses, short accesses and extended accesses. The three access types are decoded per Table 5-15, VMEbus Accesses. The Standard (A24) and extended (A32) VMEbus accesses are cacheable.

Table 5-15 VMEbus Accesses

CPU ADDRESS	ACCESS TYPE	VMEbus SIZE	
		ADDRESS LINES	RANGE
FFFF FFFF	Short Accesses	16	64K
FFFF 0000			
FFFC 0000	Extended Accesses (1)	32	256K
FFF8 0000			
FFD8 0000	Extended Accesses (1)	32	3.864G
0100 0000			
00FF FFFF	Standard Accesses (1)	24	16M
0000 0000			

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NOTES: If BOOT/-bit is asserted (in CRA), then the bottom 1Mbyte of the A24 address space is remapped to EPROM space.

5.8 VSB Address Decoding

If the VSBEN bit is asserted in Control Register B, all addresses accessed by the CPU in the address range 0100 0000 to FFFB FFFF except those in the range FFFA 0000 to FFFA 000B and FFD8 0000 to FFFF8 FFFF are attempted on the VSB.

If no VSB slave responds to the accessed address, then a VMEbus (A32:D32) access will be attempted at the requested address provided the BOUNCE-bit in the VSBchip's Control Register, is set. Otherwise an ERR* will occur.

When the SVME-122 enters Bimode, the VSBEN-bit is cleared.

The VSB accesses (A32:D32) are cacheable.

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5.9 Memory Address Decoding

The EPROM is accsesible at location 0000 0000 if the BOOT bit is asserted and the VMEbus/EPROM BOOT jumper (JB4) is installed. The EPROM is also accessible at location FFE8 0000. The 128 Kbyte of EPROM available is repeated 8 times in the 1Mbyte address space allocated to the EPROM.

The SRAM is accessible at location FFD8 0000. The 16 Kbytes of SRAM available is repeated 64 times in the 1 Mbyte address space allocated to the SRAM.

The EEPROM is accessible at location FFFX 8001 which is the port C of the CIO. Refer to Section 5.4 for more details.

5.9.1 Cache

The SVME-122 is equipped with 16 Kbytes of direct mapped cache memory. The Cache memory is configured to acquire and maintain copies of up to 4K longwords. Cache writes occur only during aligned longword access to the VMEbus or the VSB. Cache reads occur only during access to the VMEbus or VSB. The SVME-122 on-board logic provides write protection and Cache enable/disable.

The available memory of the VMEbus and the VSB is divided into 8 Kbyte segments within the 128 Mbytes of off-board memory space. The on-board logic provides 4 attributes, under software control, for Cache and write protect on each 8 Kbyte segment of off-board memory. The 4 attributes are Cache Enable user, Cache Enable Supervisor, write Protect User, and Write Protect Supervisor.

The attributes for an 8 Kbyte segment are repeated 32 times throughout the 4G memory space on 128 Mbyte boundaries.

The attributes are software programmable via an array of 16K registers labelled as Control Memory.

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5.9.2 Control Memory

The control memory is a 16K x 4 register containing the 4 attribute bits for each of the 8 Kbyte segments. In normal operation, the Control Memory is not accessible by the local CPU.

The Control Memory may be programmed by assertion of the MAE bit in Control Register B (CRB). When the MAE bit is asserted, accesses to the VMEbus or VSB will not proceed and the local CPU then accesses the Control Memory.

The Control Memory is accessible as an array of 4-bit registers as shown below:

```
-----------------------------------------------------------
 AAAA   AAAA   AAAA   AAAA   AAAA   AAAA   AAAA   AAAA
 3322   2222   2222   1111   1111   1100   0000   0000
 1098   7654   3210   9876   5432   1098   7654   3210


 XXXX   XSSS   SSSS   SSSS   SSCC   CCCC   CCCC   CC
 |      ||                    ||                    |
 | DON'T||     8 K SEGMENT    ||          4K        |
 | CARE ||                    ||    CACHE LOCATION  |
-----------------------------------------------------------
```

S = Selected 8 Kbyte memory segment
C = Cache location
X = Address Don't Care

The Control memory attributes for a particular 8 Kbyte memory segment is read/writable at the VMEbus/VSB address shown. Attributes programmed at that address affect the VMEbus/VSB memory block segment at the same address during normal operations.

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The control memory is accessible as an eight-bit port.

Refer to Figure 5-11 for Control Memory register bit assignment. Refer to Table 5-16 for Control Memory register bit description.

D7	D6	D5	D4	D3	D2	D1	D0
CEU	CES	WPU	WPS	X	X	X	X

Figure 5-11 Control Memory Registers

Table 5-15 Control Memory Registers

BIT NAME	ACCESS RIGHTS	RESET CONDITION	DESCRIPTION
CEU	R/W	N/A	CACHE Enable User 1: Cache operates on User accesses 0: Cache disabled on User accesses
CES	R/W	N/A	CACHE Enable Supervisor 1: Cache operates on Supervisor accesses 0: Cache disabled on Supervisor accesses
WPU	R/W	N/A	Write Protect User 0: Write operations enabled for user accesses 1: Write operations disabled for user accesses
WPS	R/W	N/A	Write Protect Supervisor 0: Write operations enabled for Supervisor accesses 1: Write operations disabled for Supervisor accesses

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APPENDIX A I/O ADDRESS SUMMARY

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TABLE A-1 I/O ADDRESS SUMMARY

REGISTER NAME & ID	ACCESS RIGHTS	RESET CONDITION	BASE ADDRESS RANGE	BIT ASSIGNMENT D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
IDR	R/O	-	FFFE 8000 to FFFE FFFF	X	FS1	FS0	SPACE1	SPACE0	GA21	GA10	GA00	X	X	X	X	X	X	X	X
LM FIFO	R/O	-	FFFE 0000 to FFFE 7FFF	A09	A08	A07	A06	A05	A04	A03	A02	X	X	X	X	X	X	X	X
CRB	R/W	N/A	FFFD 8000 to FFFD FFFF	RSTCH	ROR	MAE	VSBEN	A32ON	A24ON	BR1	BR0	LM7	LM6	LM5	LM4	LM3	LM2	LM1	LM0
CRA	R/W	0	FFFD 0000 to FFFD 7FFF	X	X	X	X	X	X	X	X	EXITBI	BIMSK	LSLED	LSLED	SYSFMSK	FAILE	ABIT	BOOT
ISR PORT A CIO	R/O	-	FFFC 8005									SELFBI	TESTBIT	VSBINT	LMINTAIL	ACFAILI	SYSFAIL	ABORT	BIMODE
IMR PORT B CIO	R/W	*	FFFC 8003									ACMASK	AMSK6	AMSK5	AMSK4	AMSK3	AMSK2	AMSK1	1

(1)

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TABLE A-1 I/O ADDRESS SUMMARY (continued)

REGISTER NAME & ID	ACCESS RIGHTS	RESET CONDITION	BASE ADDRESS RANGE	BIT ASSIGNMENT D15 D14 D13 D12 D11 D10 D09 D08 D07 D06 D05 D04 D03 D02 D01 D00
SECR PORT C CIO	R/W	*	FFFC 8001	ROMDAT (3) FPSENSE (2) XXX ROMCLK
CONTROL REGISTER CIO			FFFC 8007	
CSR VSB CHIP	R/W		FFFA 0000	FAIR* ENT0 (4) ENT0 (4) XXX MASTEREN* READONLY* BOUNCE* TEN* BLOCKEN* XXX SCON*
	R/O(5)			ERR* ASSACK1* AACKOUT* TIMEOUT* WRERR*
CONTROL MEMORY REGISTER	R/W	NA	(6)	CEU CES WPU WPS XXXX
SCC CHB COM SCC CHB DATA SCC CHA COM SCC CHA DATA			FFFC 0001 FFFC 0003 FFFC 0005 FFFC 0007	

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NOTES:

(1) This bit is read-writable, and in its reset condition is tri-stated by the CIO but is pulled high by external logic.

(2) This bit is read/only and in its reset condition it reflects the state of the signal it monitors.

(3) This line should be programmed as "open drain".

(7) "_" signifies that the bit reflects the state of signal it is monitoring.

(8) "NA" signifies that the state of these bits are unknown at reset.

(4) These bits are encoded as follows:

ENT01	ENT00	TIME-OUT PERIOD
0	0	64 MICROSECONDS
0	1	128 " "
1	0	256 " "
1	1	TIMER DISABLED

(5) These bits reflect the most recent condition under which the RR* was asserted.

(6) Control Memory is accessible as an array of 4-bit registers at the address shown below:

```
-----------------------------------------
AAAA AAAA AAAA AAAA AAAA AAAA AAAA AAAA
3322 2222 2222 1111 1111 1100 0000 0000
1098 7654 3210 9876 5432 1098 7654 3210

XXXX XSSS SSSS SSSS SSCC CCCC CCCC CC

          8K SEGMENT     4K CACHE
-----------------------------------------
```


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