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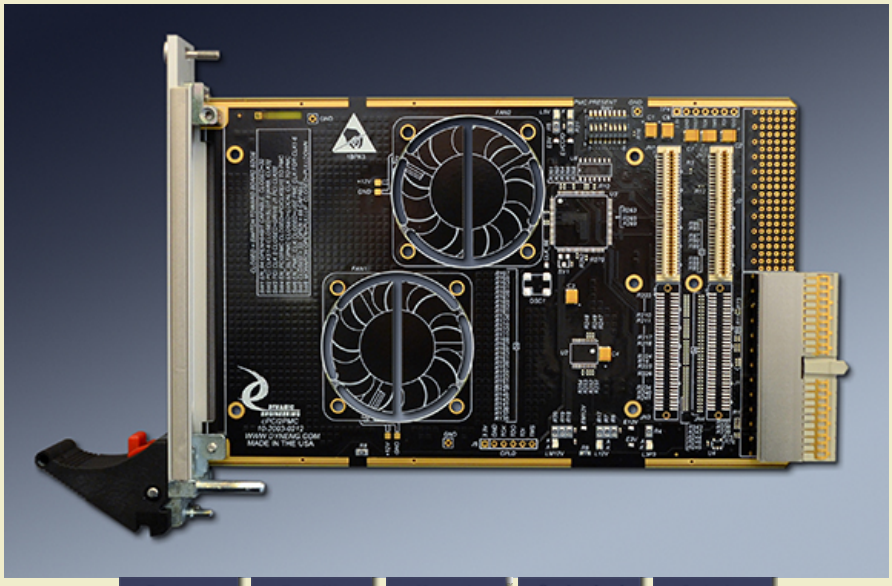
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Find the *Dynamic Engineering cPCI2PMC* at our website: *Click HERE*



150 DuBois St. Suite C Santa Cruz CA 95060 ph 831.457.8891 fx 831.457.4793 est 1988

cPCI2PMC



- cPCI, PMC compatible operation at 66/33 MHz and 64/32 bits.
- Front (bezel) and/or Rear(Pn4,J2) IO.
- 5V(12A), 3.3V(12A), +12V(1A), -12V(1A), VIO(4A) routed to PMC
- Status LED´s
- Industrial/Extended Temperature Range Standard (-40C <=> +85C)
- Slot Zero operation option - system house keeping
- Zero Slot Fan option - add cooling without taking up extra cPCI slots
- 1 year warranty standard. Extended warranty available.
- ROHS and Standard processing available

Download the shortform datasheet.

cPCI2PMC (cPCI to PMC) adapter/carrier converter card provides the ability to install one PMC or PrPMC card into a standard cPCI slot. cPCI2PMC has a PMC card slot mounted to a universal 3U 4HP cPCI card. Suitable for 32/64 with 33/ 66 MHz bus operation. The PMC user IO connector Pn4 is optionally connected to J2 for rear panel IO. The PMC bezel connector is mounted though the cPCI mounting bracket. Optional Slot 0 operation with Bus Arbitration, Reset, clock distribution provided.

The cPCI bus is buffered with 10 ohm series resistors. The PCI clock is distributed with a zero delay buffer. The cPCI2PMC design is passive with no added delays to access the PMC hardware. The traces are carefully routed with proper attention paid to the impedance and reference planes to maximize compatibility with your cPCI system. The passive design of the cPCI2PMC reduces system latency.

The PCI bus is interconnected to the PMC via 64 bit 66 MHz capable layout. The slower and more narrow device will determine the interface characteristics. The M66EN selection allows the user to specify the PCI speed capabilities. M66EN is interconnected between the cPCI bus, jumper, and PMC device.

cPCI VIO is interconnected to the PMC directly. The PCI backplane will determine the bus voltage reference. The voltage select pins are not installed on the cPCI2PMC and it is left to the user to properly select the PMC and cPCI motherboard for cPCI voltage level considerations. Many PMC´s are "universal" and can work with 3.3 or 5V cPCI backplanes. If you need to use a 3.3V card on a 5V backplane or vice-versa please consider the cPCIBPMC3U64ET design. The bridged implementation provides level shifting between the cPCI and PMC buses.

cPCI2PMC follows the PMC specs for maximum power consumption and heat dissipation. The power is routed from the cPCI to PMC connectors with mini-planes each of which is rated for more than the maximum PMC draw. 3.3, 5, VIO, +12, -12

The individual pins on the JN4 (PN4) connector are accessible when the IO option is specified. With 3U cPCI , J2 has two definitions - in a 64 bit PCI implementation J2 has the upper A/D and control signals, and in a 32 bit PCI implemention J2 has the rear panel IO. With resistor jumpers the IO or the PCI signals can be connected to J2. Please be sure to specify -IO, -64, or blank [neither]. The routing is impedance controlled and matched length.

With the RevK and later boards cooling fans are an available option. High velocity 12V fans can be mounted to the rear or medium velocity "Zero Slot" fans can be mounted to the board. WIth the "Zero Slot" fans no extra cPCI positions are used for the fan, and the fans are legal for a PMC height and cPCI height specifications. Approximately 5 CFM per installed "Zero Slot" fan. The fans can be installed to blow onto the PMC or to pull air away from the PMC and to blow onto the card in the next cPCI slot. Fan1 is above J1 and Fan2 above J2.

If you have custom requirements please call or e-mail us with the details.

cPCI2PMC Features

- **Size** 3U 4HP cPCI
- **PMC compatible slot** 1 PMC Position provided.
- **Clocks** cPCI bus can operate at 66 or 33 MHz. The PMC must be 66 MHz capable for 66 MHz operation to work properly. M66EN has a user switch to allow or disable 66 MHz. operation.
- **Access Width** Standard cPCI byte lanes supported for byte, word and long access dependent on installed PMC. 64 or 32 bit operation supported.
- **Software Interface** PMC register definitions as defined by installed hardware. No software set-up required by cPCI2PMC.
- **Interrupts** INTA, B, C, D routed to cPCI connector from PMC.
- **Signal Conditioning** PCI signals are series terminated with 10 ohm resistors as required by the cPCI specification. Zero delay buffer for PCI clock distribution.
- **Power** +5, +3.3, +12, -12V VIO supplied to PMC. Planes can source more than 1A per PMC power pin.
- **VIO** PCI IO Voltage is set by the PCI backplane. VIO is routed from the PCI connector to the PMC.
- **Thermal** The cPCI2PMC is a passive design with minimal heat dissipation for optimal PMC performance.
- **IO Interface** Front Bezel IO supported at cPCI bracket. Jn4 "user IO"

supported with interconnection to J2 when -J2 option specified.

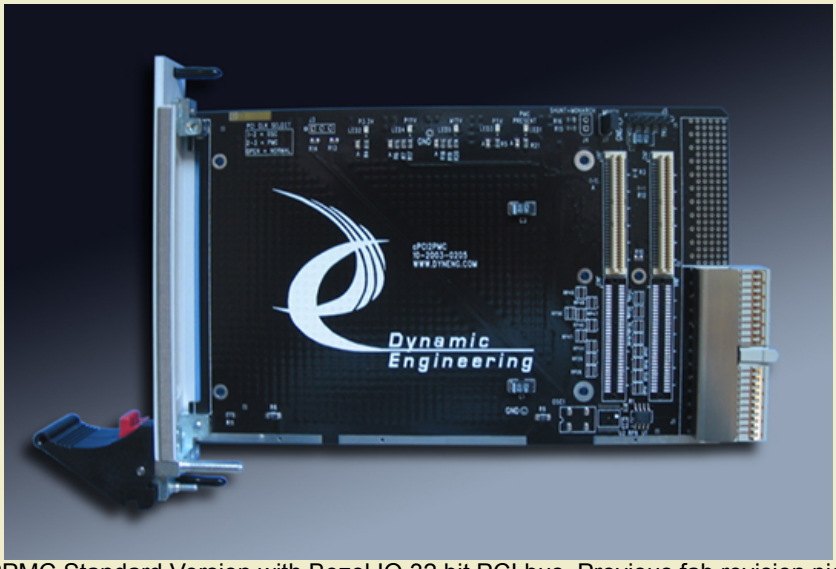
- **LED´s** — +3V, +5V, +12V, -12V and Busmode 1.
- **JTAG** — Optional JTAG header connected to PMC supplied. JTAG pin definitions are in the silkscreen.
- **Volatility** — Download the Statement of Volatility.

cPCI2PMC Benefits

- **Speed** — Now you have a choice between the cPCI**2**PMC and the cPCI**B**PMC. With the cPCI2PMC direct connect to the PCI bus the latency to the PMC is optimized. With the Bridged design of the cPCIBPMC the system speed is optimized. In some cases the possibility of doing 64 bit accesses to 32 bit PMC ports [memory] and 66 MHz primary PCI with a 33 MHz PMC secondary may be faster than the direct connect model. In either case your data will move quickly and reliably through the PCI bus to and from your hardware.
- **Price** — cPCI2PMC has the low price point. Make use of existing PMC designs in cPCI applications without paying for the expense of a new design and layout. Quantity discounts are available. Three basic versions are available. No J2, J2 IO and J2 cPCI extension.
- **Warranty** — 1 year warranty
- **Ease of Use** — cPCI2PMC is easy to use. A plug and play interface to the PMC site.
- **Availability** — cPCI2PMC is a popular board. We keep cPCI2PMC in stock. Send in your order and in most cases have your hardware the next day.
- **Size** — cPCI2PMC is a 3U 4HP cPCI board which conforms to the cPCI mechanical specifications. Eliminate mechanical interference issues. cPCI2PMC can be used in all cPCI slots.
- **PMC Compatibility** — cPCI2PMC is **PMC** compliant per the IEEE 1386 specification. All Dynamic Engineering PMC Modules are compatible with cPCI2PMC.
- **cPCI Compatibility** — The cPCI2PMC is not **cPCI** compliant. cPCI2PMC has trace lengths slightly in excess of the maximum specified by the PCI specification. The cPCI2PMC design includes several features to minimize the effects of the longer traces. The zero delay clock buffer keeps the PCI side of the clock length within specification, and the 10 ohm series resistors help to control the AD and control signals. All cPCI bus signals are properly referenced to planes.

  Single cPCI2PMC adapters can be expected to work in any PCI bus stub. If you need to operate multiple adapters per stub we recommend the cPCIBPMC which is completely cPCI specification compliant. cPCI2PMC is based on the PCI2PMC which is in use in hundreds of chassis and tested in multiple backplanes. cPCI2PMC is closer to specification than the PCI2PMC. Due to the mechanical configuration a passive design will not meet all of the length specifications. Now on Release L.

Originally released in 2003. Hundreds delivered and in operation.



cPCI2PMC Standard Version with Bezel IO 32 bit PCI bus. Previous fab revision pictured

cPCI2PMC Ordering Options

- **cPCI2PMC:** Standard cPCI2PMC J2 not installed, IO through Bezel (front panel).
- **cPCI2PMC-IO:** J2 installed and connected to Jn4 with standard rear panel IO definitions
- **cPCI2PMC-IOJn3:** J2 installed and connected to Jn4 with standard rear panel IO definitions. Jn3 is also installed.
- **cPCI2PMC-64 option:** J2 installed and connected to Jn3 for upper cPCI bus signals
- **cPCI2PMC-64Jn4 option:** J2 installed and connected to Jn3 for upper cPCI bus signals. Jn4 also installed
- **cPCI2PMC-64-16IO:** cPCI2PMC-64 with upper 16 IO lines *Note: 2 IO remapped to ALt. J2 pins (64-44 & 54-43)
- **cPCI2PMC-IO-SLT0:** J2 installed and connected to Jn4 with standard rear panel IO definitions, plus slot 0 functions: bus arbitration, reset, clock distrbution
- **cPCI2PMC-64-SLT0:** J2 installed and connected to Jn3 for upper cPCI bus signals plus slot 0 functions: bus arbitration, reset, clock distrbution
- **cPCI2PMC-NIO-SLT0:** Standard cPCI2PMC with 32 bit PCI and slot 0 functions and no other connections to the rear panel connectors.
- **-JTAG:** Add JTAG header to any build option
- **-FAN[0/1][HV][R]:** Add fans in position 1 and/or 2. Fan1 is above Jn3,Jn4 and Fan2 is above Jn1,Jn2. Standard orientation is to blow onto PMC. Add "R" to each fan callout to reverse that position. Zero Slot fans have approximately 5 CFM. For an 8 CFM fan add the "-HV" designation. Please note: HV fans are mounted on the rear and will interfere with the next slot.

Examples:
-FAN12 adds 2 fans in the standard orientation - air toward PMC.
-FAN12R adds a standard orientation fan in position 1, and a reversed fan in position 2.
-FAN1R2R has both installed, and air is pulled from PMC locations.
-FAN1HVR is mounted on the rear, and pulls from the PMC in position 1.
-FAN2HV is mounted on the rear, and blows toward the PMC in position 2.

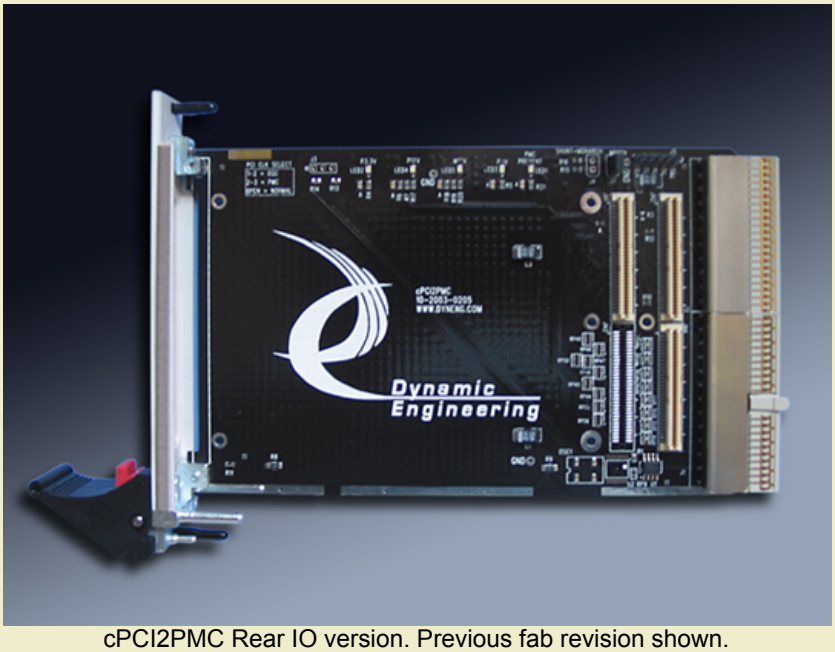
*Please note: the "M" options have been incorporated into the slot 0 function.

If you wish to order a version other than the standard cPCI2PMC, please select from below.

cPCI2PMC ▼ | No Fan1 ▼ | No Fan2 ▼

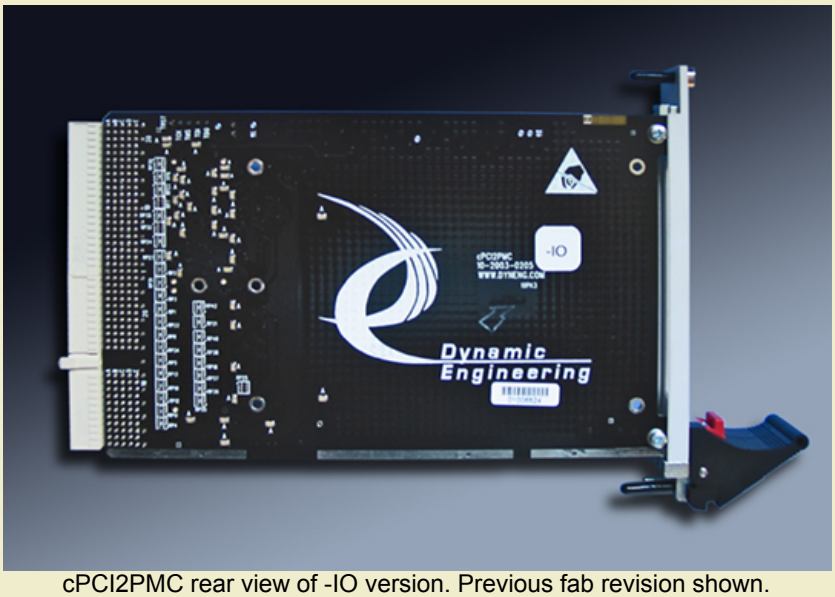
Standard Processing ▼

Quantity 1 Add to Cart View Cart



cPCI2PMC Rear IO version. Previous fab revision shown.

The "System Slot" version of the cPCI2PMC has the added capability to monitor the Bus Request signals, issue bus grants, create the system reset, and drive the clock signals to the appropriate J1, J2 pins per the cPCI slot 0 specification. The base design incorporates the features. The parts associated with the slot zero capability are not installed when this option is not requested. Please note that a PrPMC can be installed into the PMC slot. The PrPMC will need to take care of bus enumeration and other slot 0 functions associated with the system processor.



cPCI2PMC rear view of -IO version. Previous fab revision shown.

Manual

You must have Adobe Acrobat to read our PDF files
Download the cPCI2PMC Manual 6/6/13 Settings, connector maps, ordering options etc.

Related:

cPCIBPMC3U64 cPCI 3U 4HP Bridged 64 bit PMC carrier with optional ethernet wiring to backplane
cPCIBPMC3U64ET cPCI 3U 4HP PMC carrier with Extended Temperature
cPCIBPMC6UET cPCI 6U 4HP dual PMC carrier with Extended Temperature

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