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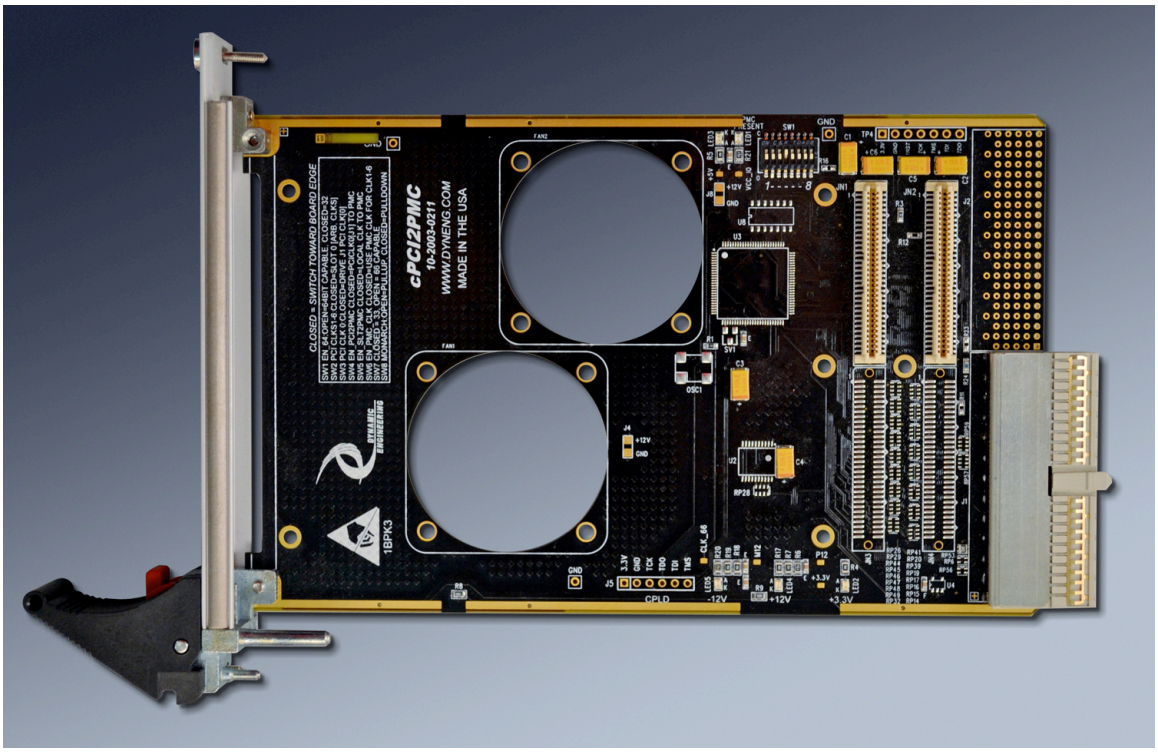
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Est. 1988

User Manual

cPCI2PMC

cPCI 1 Position PMC Compatible Carrier
With Options:
Slot 0 Controller, Rear IO and 64 bit PCI Bus



Revision L
Corresponding Hardware: Revision A-L
10-2003-0212 [current revision]

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cPCI2PMC
cPCI and PMC Compatible Carrier

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Product Description

cPCI2PMC is part of the cPCI and PMC Compatible family of modular I/O components. cPCI2PMC adapts one PMC to one cPCI slot.

Special features:
• cPCI 3U 4HP card.
• LED on PMC Busmode "Present"
• LED on plus 12
• LED on minus 12
• LED on plus 5
• LED on 3.3V
• 32 or 64 bit PCI operation
• Monarch mode options for clock sourcing
• 33 or 66 MHz operation
• M66EN jumper option
•10 ohm series resistors on AD31-0
• Zero delay buffer for PCI clock distribution
• Front panel connector access through cPCI bracket
• User IO [Pn4] available through J2
• Passive design for optimal electrical and thermal performance of PMC
• Option for Slot 0 Functions with Clock sourcing, Request and Grant arbitration, Reset control etc.
• Option to add "Zero Slot" fans to cool the installed PMC

cPCI2PMC is a passive design incurring no added delays in connection from the PCI to the PMC buses. The design incorporates features to prevent the physical length of the traces from affecting operation. There may be cases where the backplane can't support all slots with cPCI2PMC cards installed. The cPCIBPMC3U64-ET can be used when a bridged card is required.

The only standard shunt option on the cPCI2PMC is the one for M66EN. M66EN is pulled high on the backplane for each cPCI bus stub. If any device within that stub can't operate at 66 Mhz that device grounds M66EN to take the frequency to 33 MHz. The cPCI pin, PMC pin and shunt are tied together to allow the PMC, shunt or another device to select the frequency of operation. Please note that the master must be 66 MHz capable for any of the devices to operate at that frequency. The shunt is clearly marked on the silk screen.

The JTAG pins on the PMC are brought to a header for convenience. The pin

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definitions are in the silk screen. The JTAG pins on the cPCI connector are not recommended for use [per cPCI specification] and are not connected to the header. TDI is tied to TDO at the cPCI connector.

PrPMC devices are sometimes operated in “Monarch Mode” where the PMC drives the PCI clock. The Revision E and later fab has a feature which is the addition of an optional location for an oscillator and clock buffer. The backplane can drive the PMC clock, the oscillator can source the backplane and PMC or the PMC can drive the backplane depending on how the parts are assembled. J3 is used to select between the oscillator, PMC, and backplane clock when the monarch mode hardware is installed. J3 (1-2) selects the oscillator, J3(2-3) selects the PMC and open = backplane. Please note that resistor R1 is left off when the PMC or Oscillator options will be used to isolate the PLL. The PLL is part of the backplane clock distribution circuit.

In addition; when J4 has a shunt installed PN2 pin 64 is pulled low via a 1KΩ resistor, otherwise that pin is pulled high via 10KΩ. Pin 64 is sometimes used to select the mode the CPU on a PrPMC initializes into.

With **revision I & J** boards the slot 0 capabilities are enhanced to cover the Monarch mode options plus provide for the slot 0 “housekeeping” functions of reset, bus arbitration, clock driving etc. A CPLD has been added and more shunts for user selections. The oscillator ties directly to the CPLD and J3 is used to enable the slot 0 functions [installed] or disable [open]. With revision J this function is moved to a DIP Switch. The frequency selection is done with sensing M66EN. The backplane or PMC can control the M66EN signal on Rev I boards.

With **revision K** boards the shunts have been removed in favor of a DIPswitch. Please see the silk-screen on the board and the table later in this manual for the DIP switch definitions.

Slot 0 signals use J2 for connection to the backplane. With a –64 version the full PCI function is available in addition to the Slot 0 functions. With a – IO version card the upper IO signals from Pn4 conflict with the Slot 0 functions. Resistor jumpers are used to select between the options. The Slot 0 function takes precedence over the –IO when both are selected resulting in the upper 16 IO being disconnected from Pn4 to account for the clocks etc. Please refer to the pin out table for more information.

If your PMC uses the upper 16 lines for the clock, request and grant signals then you can use a Standard –IO card to have the Slot 0 functionality without needing the Slot 0 capability on the cPCI2PMC.

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Please refer to the ordering section for a description of the options.

DIPSwitch Settings

SW1 is an 8 switch DIP switch. Various shunts have been removed from the board in favor of the DIP switch. Please note that some switch settings only have functionality when a corresponding option is installed – Slot 0 function etc. The switch has Open and Closed positions. Please refer to the Silk-Screen
1: **Enable 64** signal. Open = 64 bit capable. Closed = 32 bit.
2. **PCI Clocks 1-6** Closed = Slot 0 function, Open = disabled.
3. **PCI Clock 0** Closed = drive PCI Clock 0 Open = tristated
4. **Enable PCI clock** to PMC Closed = drive J0 clock to PMC device
5. **Enable Slot clock** to PMC Closed = use local clock to source PMC
6. **Enable PMC Clock** Closed = Use PMC Clock for Clocks 1-6
7. **M66EN** closed = force to lower range, open = 66 MHz capable
8. **Monarch** Closed = '0' Open = '1' on this bit at the PMC.

For a standard [non slot 0 operation] installation the switch (4) should be closed to route the clock from the J0 connector through the zero delay buffer and to the PMC. The other clock switches will not have effect unless the Slot Zero option is installed and the card is being used in a standard slot. For consistency Switches 2,3,5,6 should be in the open position. M66EN can be open for automatic mode or closed to force 33 MHz. Enable 64 only has meaning if a slot 0 board and if the PrPMC is 64 bit capable.

For a Slot 0 board the system architecture and installed PrPMC will determine the correct clock routing. Switch 2 should be closed to enable the slot 0 functionality. Switch 3 will depend on whether there are devices using the PCI clock on J0 or not. Switch 4 will be open and 5 closed to use the local clock assuming the PMC is not sourcing the clock in which case 6 will be closed and 4 and 5 open.

As you can see there are a lot of options. The diagram on the following page is a good starting point. Map out the choices that make sense to you and then set the switches using the table. The names and switch numbers in the diagram match the table.

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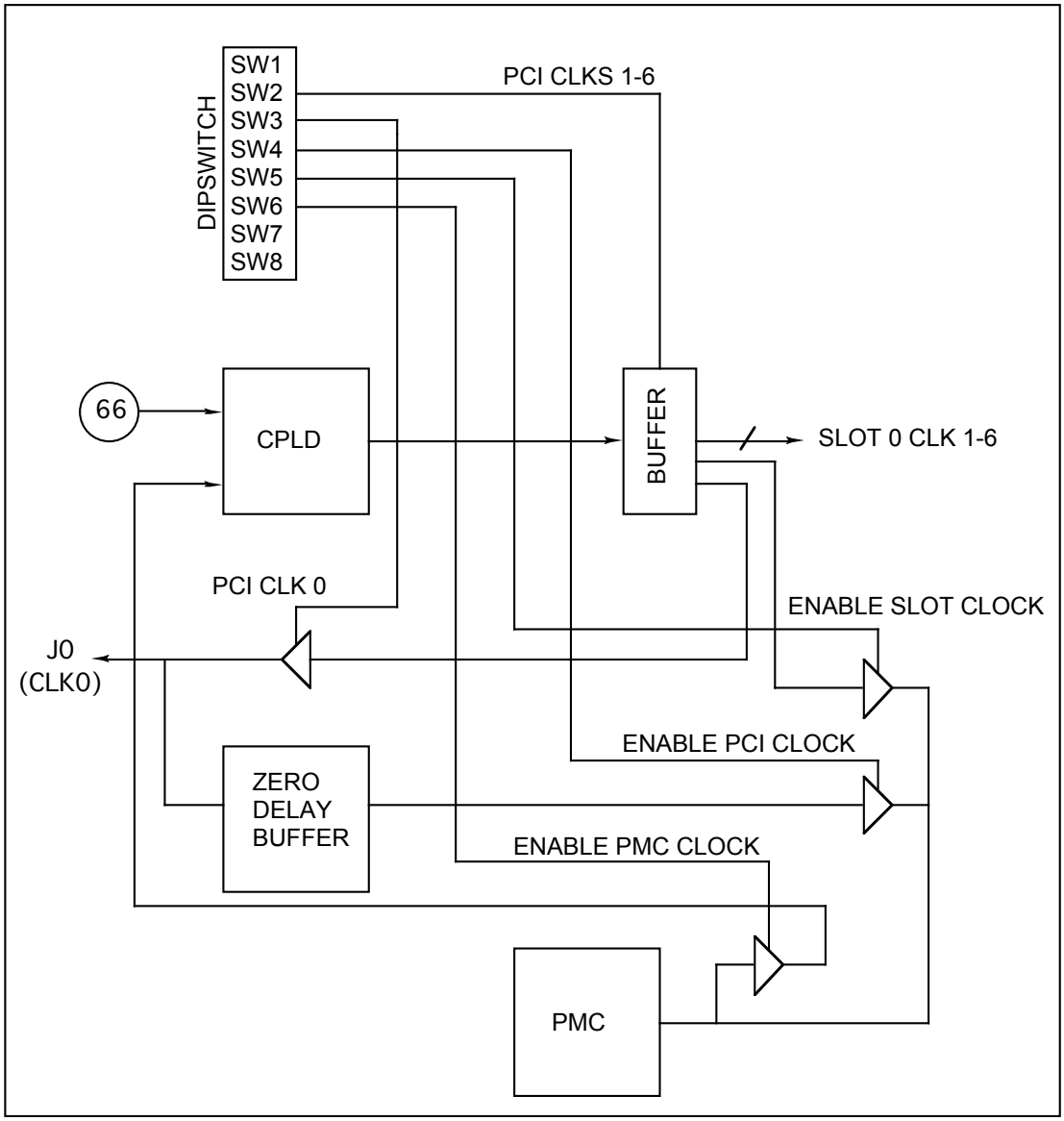


FIGURE 1 CPCI2PMC CLOCK OPTIONS

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Revisions

A: 7/6/02 Original Design.
B/C: 2/2/03 updated “as built”, minor feature enhancement
D: 11/25/03 Mechanical corrections, added AC decoupling
E: 3/3/04 Added Monarch mode capability
F: 10/17/05 updated Fab for ROHS compliance – no schematic changes
G: minor change to JTAG header
H: 5/7/07 added slot 0 clock and arbitration options
I: 2/13/08 updated to 0603’s for bypass caps
J: 11/10/09 Slot 0 corrections and enhancements
K: 1/10/11 add Fan option, switch to DIP switch instead of shunts
L: 6/6/13 update for 0402 series terminations and improved routing as a result of more flexibility with the terminations.

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PMC Module Backplane IO Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module IO Interface – from Pn4 to the cPCI J2 connectors. Please note that the connections shown are only in effect when the –IO option is selected. Also see the User Manual for your PMC board for more information. Additional power pins defined by cPCI spec. not shown.

J2		Pn4	
E13	D13	1	2
C13	B13	3	4
A13	E12	5	6
D12	C12	7	8
B12	A12	9	10
E11	D11	11	12
C11	B11	13	14
A11	E10	15	16
D10	C10	17	18
B10	A10	19	20
E9	D9	21	22
C9	B9	23	24
A9	E8	25	26
D8	C8	27	28
B8	A8	29	30
E7	D7	31	32
C7	B7	33	34
A7	E6	35	36
D6	C6	37	38
B6	A6	39	40
E5	D5	41	42
C5	B5	43	44
A5	E4	45	46
D4	C4	47	48
B4	A4	49	50
E3	D3	51	52
C3	B3	53	54
A3	E2	55	56
D2	C2	57	58
B2	A2	59	60
E1	D1	61	62
C1	B1	63	64

FIGURE 2 CPCI2PMC PN4 INTERFACE STANDARD

Read table:
J2-E13 = Pn4-1
J2-D13 = Pn4-2
etc.

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PMC Module Backplane 64 Bit Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module IO Interface – from Pn3 to the cPCI J2 connectors. Please note that the connections shown are only in effect when the –64 option is selected. Also see the User Manual for your PMC board for more information. Additional power pins defined by cPCI spec. not shown.

J2		Pn3	
		1	2
	C4	3	4 C_BE7#
E4	A5	5 C_BE6#	6 C_BE5#
D5		7 C_BE4#	8
	E5	9	10 PAR64
A6	B6	11 AD63	12 AD62
C6		13 AD61	14
	E6	15	16 AD60
A7	D7	17 AD59	18 AD58
E7		19 AD57	20
	A8	21	22 AD56
B8	C8	23 AD55	24 AD54
E8		25 AD53	26
	A9	27	28 AD52
D9	E9	29 AD51	30 AD50
A10		31 AD49	32
	B10	33	34 AD48
C10	E10	35 AD47	36 AD46
A11		37 AD45	38
	D11	39	40 AD44
E11	A12	41 AD43	42 AD42
B12		43 AD41	44
	C12	45	46 AD40
E12	A13	47 AD39	48 AD38
D13		49 AD37	50
	E13	51	52 AD36
A14	B14	53 AD35	54 AD34
C14		55 AD33	56
	E14	57	58 AD32
		59	60
		61	62
		63	64

FIGURE 3 CPCI2PMC PN3 INTERFACE STANDARD

Read table:
J2-C4 = Pn3-4
etc.

Undefined pins on Pn3 are GND or VIO
Undefined pins on J2 are open, power or ground per cPCI spec.

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Slot 0 and IO Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module IO Interface – from Pn4 to the cPCI J2 connectors. Please note that the connections shown are only in effect when the –IO and –Slot0 options are selected. Also see the User Manual for your PMC board for more information. Additional power pins defined by cPCI spec. not shown.

J2		Pn4		J2	Signal
E13	D13	1	2	A1	CLK1
C13	B13	3	4	C15	FAL#
A13	E12	5	6	D15	REQ5#
D12	C12	7	8	E15	GNT5#
B12	A12	9	10	C16	DEG#
E11	D11	11	12	C17	PRST#
C11	B11	13	14	D17	REQ6#
A11	E10	15	16	E17	GNT6#
D10	C10	17	18	A20	CLK5
B10	A10	19	20	A21	CLK6
E9	D9	21	22		
C9	B9	23	24		
A9	E8	25	26		
D8	C8	27	28		
B8	A8	29	30		
E7	D7	31	32		
C7	B7	33	34		
A7	E6	35	36		
D6	C6	37	38		
B6	A6	39	40		
E5	D5	41	42		
C5	B5	43	44		
A5	E4	45	46		
D4	C4	47	48		
B4	A4		(VIO)		
E3	D3	GNT4#	REQ4#		
C3	B3	GNT3#			
A3	E2	CLK4	REQ3#		
D2	C2	GNT2#			
B2	A2	CLK3	CLK2		
E1	D1	REQ2#	GNT1#		
C1	B1	REQ1#			

FIGURE 4 CPCI2PMC SLOT0 -IO INTERFACE STANDARD

Signals are listed showing J2 and Pn4 relationship and missing IO signals – preempted by Slot 0 functions. Signals without conflicts are shown in the second column. IO 49, 54, 58, and 64 are missing due to RP packaging issues.

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CPCI2PMC-64-16IO Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module IO Interface – from Pn4 to the cPCI J2 connectors for a -64 board with added IO.

Jn4	J2
64 (44)	B5
63	C1
62	D1
61	E1
60	A2
59	B2
58	C2
57	D2
56	E2
55	A3
54 (34)	B7
53	C3
52	D3
51	E3
50	A4
49	B4

FIGURE 5 CPCI2PMC-64-16IO INTERFACE STANDARD

*Please note, IO64 is routed to J2 IO 44 and IO54 is routed to J2 IO34 to avoid conflicts with power pins defined for slot 64 implementations.

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Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Installation
The PMC is mounted to the cPCI2PMC prior to installation within the chassis. For best results: with the PCI bracket installed, install the PMC at an angle so that the PMC front panel bezel penetrates the cPCI bracket then rotate down to mate with the PMC [PnX] connectors.

If the cPCI bracket is not installed, plug in the PMC and then attach the cPCI bracket. Use the mounting screws that come with the PMC to secure to the cPCI2PMC.

There are four mounting locations. Two into the PMC mounting bezel and two for the standoffs near the PMC bus connectors.

Start-up
Make sure that the "system" can see your hardware before trying to access it. Many BIOS will display the PCI devices found at boot up on a "splash screen" with the VendorID and CardId for the PMC installed and an interrupt level. Look quickly! If the information is not available from the BIOS then a third party PCI device cataloging tool will be helpful. We use PCIView from Bsquare.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Be careful when using a system that has partially powered operation. Make sure that the installed PMC can handle the live IO with power off situation. The cPCI2PMC is passive and unlikely to be damaged.

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Construction and Reliability

PMC Modules were conceived and engineered for rugged industrial environments. The cPCI2PMC is constructed out of 0.062 inch thick FR4 (hi temp., ROHS compliant) material. The components on the cPCI2PMC are passive and do not generate an appreciable thermal load.

Surface mounted components are used. The connectors are SMT for the PMC bus and through hole [compression fit] for the cPCI.

The PMC Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 100 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The PMC Module is secured against the carrier with the PMC connectors. It is recommended, for enhanced security against vibration, that the PMC mounting screws are installed. The screws are supplied with the PMC from the OEM. Dynamic Engineering has screws, standoffs, blank bezels and other PMC hardware available at a reasonable cost if your PMC was not shipped with some of the require attachment hardware or if it has been misplaced.

Thermal Considerations

The cPCI2PMC design consists of passive circuits. The power dissipation due to internal circuitry is very low. If the PMC installed has high heat dissipation then forced air cooling in the chassis is recommended. With the Revision K boards, Zero Slot Fans are available to help with cooling the PMC. With the Zero Slot technology no added slots are used by the fans.

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Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $130. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

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Specifications

Logic Interfaces:	cPCI Interface 33/32 ⇔ 66/64
Access types:	PCI bus accesses
CLK rates supported:	33 or 66 MHz PCI clock rates
Software Interface:	defined by PMC installed
Jumpers:	Slot 0 and Monarch options if installed
Interface:	PMC front bezel via cPCI bracket and User IO connector via J2 when –IO option installed. Matched length IO from Pn4 to J2 when installed.
Dimensions:	3U 4HP cPCI
Construction:	High Temp ROHS compatible FR4 Multi-Layer Printed Circuit board, Through Hole and Surface Mount Components. **ROHS** or Standard processing.
LED's	+12,-12,+5, 3.3, Present
Slot 0	Option for Clock generation, and Bus Arbitration.
Cooling	Option for added Fans with Zero Slot technology.

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Order Information

Standard Extended temperature range –40⇔85°C

http://www.dyneng.com/cPCI2PMC.html

cPCI2PMC
Standard cPCI2PMC J2 not installed, IO through Bezel (front panel).

cPCI2PMC-IO
J2 installed & connected to Jn4 with standard rear panel IO def.

cPCI2PMC-IOJn3
J2 installed and connected to Jn4 with standard rear panel IO definitions. Jn3 is also installed.

cPCI2PMC-64
J2 installed & connected to Jn3 for upper cPCI bus signals

cPCI2PMC-64Jn4
J2 installed and connected to Jn3 for upper cPCI bus signals. Jn4 also installed

cPCI2PMC-64-16IO
cPCI2PMC-64 with upper 16 IO lines *Note: 2 IO remapped to Alt. J2 pins (64-44 & 54-43)

cPCI2PMC-NIO-SLT0
Standard cPCI2PMC with 32 bit PCI and slot 0 functions and no other connections to the rear panel connectors.

cPCI2PMC-IO-SLT0
J2 installed and connected to Jn4 with standard rear panel IO definitions other than Upper lines used for Slot 0 functions. Adds system “housekeeping functions” – terminations, Request/Grant Arbitration, Clock driving, Reset etc.

cPCI2PMC-64-SLT0
J2 installed and connected to Jn3 with upper PCI rear panel IO definitions plus Slot 0 functions. Adds system “housekeeping functions” – terminations, Request/Grant Arbitration, Clock driving, Reset etc.

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