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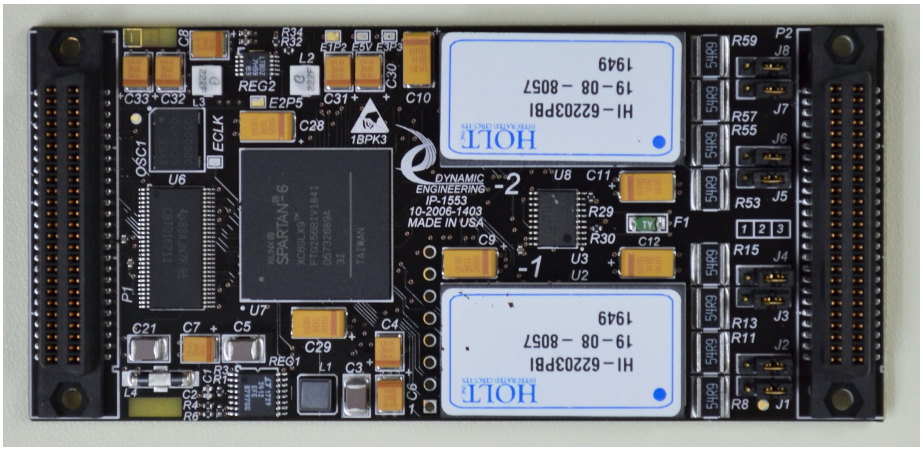
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Est. 1988

User Manual

IP-1553

MIL-STD-1553 Interface
1 or 2 Dual Redundant Ports
direct or transformer coupled

IndustryPack® Module



Revision 03P1
Corresponding Hardware: Revision 03
Flash revision 0401
10-2006-1403

IP-1553
MIL-STD-1553 Interface
IndustryPack® Module

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Product Description

IP-1553 is part of the IndustryPack® “IP” Module family of modular I/O components by Dynamic Engineering. IP-1553 provides two independent 1553 controllers each with redundancy. The Holt Integrated Circuits 62203 interf62203 provides the protocol processing, integrated transceivers and integrated transformers. Multiple taps provide the Direct or Transformer coupled capability. IP-1553 can be selectively built with one or two 1553 controllers. Please add the correct suffix to select the model you require. (-1, -2)

The 62203 supports programmable BC / MT / RT operation. To support the 62203, IP-1553 uses an FPGA to provide the IP decoding to 62203, clocking to the 1553 controller, interrupt processing, and other support functions.

The 62203 part has many features including the following [taken from the HOLT IC data sheet]
Dual Redundant MIL-STD-1553A/B/1760 channel
SW compatible with DDC ACE®, Mini-ACE®, Enhanced Mini-ACE®, Micro-ACE®, Mini-ACE Mark3® and Total-ACE®
Multiple Configurations: -- BC/RT/Monitor, and RT/MT modes
Integrated Dual Isolation Transformers
Highly Autonomous BC with Built-In Message Sequence Controller
Choice of Single, Double, and Circular RT Buffering Options
Selective Message Monitor
Comprehensive Built-In Self-Test

The internal decoding performed within the FPGA is synchronized to the 1553 clock. A frequency doubler is used to allow tighter timing control over the asynchronous interface the 62203 employs. With the tighter timing fewer wait-states are required for an access from the IP bus. The internal rate is 40 MHz and the 62203 is provided a 20 MHz. reference.

IP-1553 is 8 and 32 MHz compatible. 32 MHz is recommended. The 62203 provides a done signal; the local state-machine utilize to determine the end of each transfer. Reads and Writes are performed with optimized interaction to the 62203. The 62203 has registers and memory.

The 64K memory within each 62203 device exceeds the size of the IP IO space. The Memory space is used to decode the 62203 addresses. Address bit 18 is used to select the 62203 device and Address bit 17 to select between Register and Memory within each 62203. The IO space is used to decode the control registers within the FPGA.

Each channel has a control register within the FPGA to set the channel specific options. Each channel has a portion of the IP Memory space allocated to allow direct offsets based on the 62203 addresses to be utilized.

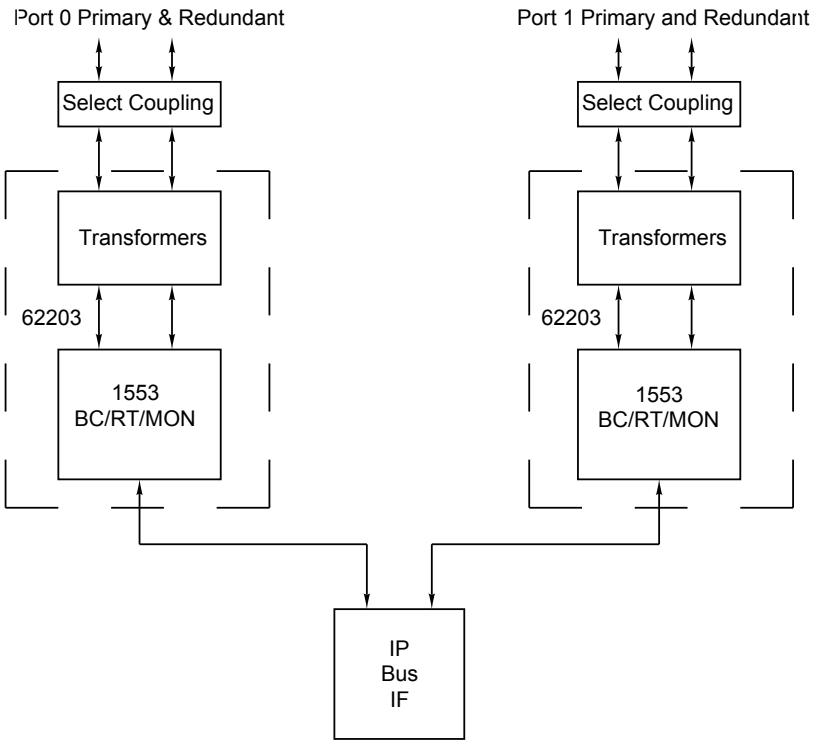


FIGURE 1 IP-1553 BLOCK DIAGRAM

All FPGA configuration registers support read and write operations for maximum software convenience. 62203 has register dependent R/W capability.

IP-1553 conforms to the IndustryPack® standard. This guarantees compatibility with compliant carrier boards. Because the IP-1553 may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one Carrier board, with final system implementation on a different one. For example the PCIe3IP – PCI carrier for IP Modules can be used for development in a conventional PC. Later the hardware and software can be ported to the target. http://www.dyneng.com/PCIe3IP.html

With the Dynamic Engineering Windows driver collection for IP and carrier modules a Parent – Child architecture is employed. The IP portion of the driver is directly portable

between the various Dynamic Engineering IP carriers [PCI3IP, PCI5IP, PCIe3IP, PCIe5IP, PC104pIP, PC104p4IP, cPCI2IP, cPCI4IP etc]. The parent portion of the driver contains the carrier specific design information. This means that software developed for the IP-1553 on one platform can be directly ported to another. PCIe to cPCI for example.

Designers can even make use of the Dynamic Engineering carrier driver for non-Dynamic Engineering IP modules using the Generic IP capability built into the parent portion of the driver. IP modules that the carrier driver does not recognize are installed as "generic" and accessed with an address, data interface model. Software developed for the Generic mode can also be ported between modules.

IP-1553 is tested with a combination of internal and external tests. The registers can be tested with R/W tests, the ports can be tested with self-tests, and the ports can be tested with an inter-channel loop test. The ATP for IP-1553 includes FPGA internal, Local to 62203 [RAM, Protocol, Register] and external loop-back tests.

Interrupts are supported by IP-1553. The 62203 has several programmable interrupts for RX, TX and error conditions. Each channel has a separate interrupts and enables. All interrupts are individually maskable. In addition, a board level SW interrupt is provided for test and software development purposes.

IP-1553 is implemented with the idea of offloading the CPU as much as possible. The 62203 incorporates internal RAM to cut down on the number of interrupts. With address masking only the messages of interest can be received to further reduce CPU traffic. Most registers retain their information between messages allowing for quick reload and send once the initial programming has been implemented.

62203 Transceivers are coupled to the MIL-STD-1553 bus via internal transformers. The transformers have multiple taps to support direct and transformer coupled connections to the main bus. The Direct and Transformer coupled options are provided with shunts and the J1-4 /J5-8 header blocks. 54.9 Ω resistors are provided in the Direct coupled path. Each header has 3 pins. 1-2 for Direct and 2-3 for transformer coupled. Usually the Primary and Secondary are selected in the same configuration, however, Primary and Redundant can be opposite configurations. J1,J2 for port 0 A. J3,J4 for Port 0 B. J5,J6 for Port1 A. J7,J8 for port 1 B.

62203 devices can be programmed to use an external clock and support an external trigger. The signals are routed from the IO connector through the FPGA to the 62203 devices. If further conditioning is required please contact Dynamic Engineering.

In addition, the RTA address and parity bit are provided on the IO connector and terminated with pull-ups. The signals can be programmed with software or within the cable. Separate addresses are provided for each channel. Pull-ups and device are referenced to 3.3V. 2.2K ohms. Ground to make 0's in the address.

The JTAG connections to the FPGA along with a 3.3V and Ground reference are also supplied on the IO connector to allow field updates.

Address Maps

Address Map Internal

```
IP-1553_BASE          0x0000   // 0 base control register offset
IP-1553_VECTOR        0x0002   // 1 Vector Register offset
IP-1553_STATUS        0x0004   // 2 Base Status register
IP-1553_CarrierSlot   0x0006  // 3 Carrier Slot Information Register
IP-1553_Revision      0x000A // 5 Major,Minor Revision
IP-1553_ControlReg0   0x0014   // 10 Channel 0 control register
IP-1553_StatusReg0    0x0016   // 11 Channel 0 status register
IP-1553_ControlReg1   0x0028   // 20 Channel 1 control register
IP-1553_StatusReg1    0x002A   // 21 Channel 1 status register
```

FIGURE 2 IP-1553 INTERNAL ADDRESS MAP

// Controller internal accesses are on word boundaries in **Memory Space**
// Channel 0/1 is offset based on address bit 18
// Memory versus Register based on address bit 17

Address Map Channel 0

```
#define  IMR1_0          0x00000  //0 R/W
#define  CR1_0           0x00002  //1 R/W
#define  CR2_0           0x00004  //2 R/W
#define  SRR_0           0x00006  //3 WR
#define  CSP_0           0x00006  //3 RD
#define  BC_COUNT_0      0x00008  //4 R/W
#define  TIME_TAG_0      0x0000a  //5 R/W
#define  ISR1_0          0x0000c  //6 RD
#define  CR3_0           0x0000e  //7 R/W
#define  CR4_0           0x00010  //8 R/W
#define  CR5_0           0x00012  //9 R/W
#define  RT_MON_SAR_0    0x00014  //a RD
#define  BC_FTR_0        0x00016  //b RD
#define  BC_TRNM_0       0x00018  //c RD
#define  AUX1_0          0x0001a  //d RW Enhanced mode
#define  FRAMETIME_0     0x0001a  //d RW
#define  RT_STAT_0       0x0001c  //e RD only
#define  RT_BIT_0        0x0001e  //f RD only
#define  TMR0_0          0x00020  //10
#define  TMR1_0          0x00022  //11
#define  TMR2_0          0x00024  //12
#define  TMR3_0          0x00026  //13
#define  TMR4_0          0x00028  //14
#define  TMR5_0          0x0002a  //15
#define  TMR6_0          0x0002c  //16
#define  TMR7_0          0x0002e  //17
#define  CR6_0           0x00030  //18 R/W
#define  CR7_0           0x00032  //19 R/W
                                  // address 1a = RESERVED
#define  BC_CCR_0        0x00036  //1b RD
#define  BC_GPF_0        0x00036  //1b WR
#define  BIT_0           0x00038  //1c RD
#define  IMR2_0          0x0003a  //1d R/W
#define  ISR2_0          0x0003c  //1e RD
#define  QP_0            0x0003e  //1f RW

#define  SPA_0           0x20200  //memory stack pointer address offset 0
#define  SPA_RX_0        0x20000  //memory RX data offset
#define  SPA_TAG_0       0x20002  //memory tag offset
```

FIGURE 3 IP-1553 CHANNEL 0 ADDRESS MAP

Address Map Channel 1

```
#define  IMR1_1          0x40000  //0 R/W
#define  CR1_1           0x40002  //1 R/W
#define  CR2_1           0x40004  //2 R/W
#define  SRR_1           0x40006  //3 WR
#define  CSP_1           0x40006  //3 RD
#define  BC_COUNT_1      0x40008  //4 R/W
#define  TIME_TAG_1      0x4000a  //5 R/W
#define  ISR1_1          0x4000c  //6 RD
#define  CR3_1           0x4000e  //7 R/W
#define  CR4_1           0x40010  //8 R/W
#define  CR5_1           0x40012  //9 R/W
#define  RT_MON_SAR_1    0x40014  //a RD
#define  BC_FTR_1        0x40016  //b RD
#define  BC_TRNM_1       0x40018  //c RD
#define  AUX1_1          0x4001a  //d RW Enhanced mode
#define  FRAMETIME_1     0x4001a  //d RW
#define  RT_STAT_1       0x4001c  //e RD only
#define  RT_BIT_1        0x4001e  //f RD only
#define  TMR0_1          0x40020  //10
#define  TMR1_1          0x40022  //11
#define  TMR2_1          0x40024  //12
#define  TMR3_1          0x40026  //13
#define  TMR4_1          0x40028  //14
#define  TMR5_1          0x4002a  //15
#define  TMR6_1          0x4002c  //16
#define  TMR7_1          0x4002e  //17
#define  CR6_1           0x40030  //18 R/W
#define  CR7_1           0x40032  //19 R/W
                                  // address 1a = RESERVED
#define  BC_CCR_1        0x40036  //1b RD
#define  BC_GPF_1        0x40036  //1b WR
#define  BIT_1           0x40038  //1c RD
#define  IMR2_1          0x4003a  //1d R/W
#define  ISR2_1          0x4003c  //1e RD
#define  QP_1            0x4003e  //1f RW

#define  SPA_1           0x60200  //memory stack pointer address offset 0
#define  SPA_RX_1        0x60000  //memory RX data offset
#define  SPA_TAG_1       0x60002  //memory tag offset
```

FIGURE 4 IP-1553 CHANNEL 1 ADDRESS MAP

Programming

Programming IP-1553 requires only the ability to read and write data from the host. The base address refers to the first user address for the slot in which the IP is installed.

Depending on the software environment, it may be necessary to set-up the system software with IP-1553 "registration" data. Other OS may be more “plug and play”. The Dynamic Engineering Windows Drivers operates in a “plug and play” mode using parent ⇔ child architecture.

In order to receive and or transmit data the software is required to enable the controller for the channel(s) of interest. The initialization procedure is a multi-step process determined by the 62203, and the desired mode of operation. It is recommended that the user who is writing their own driver refer to the HOLT IC Application notes for the 62203.

Interrupts are used to help manage the data transfer process. When a programmed transfer is completed, the interrupt can be generated to alert the host to program a new transfer. The transfers are independent for each channel allowing the CPU interaction to be minimized.

The Dynamic Engineering IP-1553 driver for Windows 10 manages the interaction and can set-up the transfer for you. The UserAp is easily integrated into a Visual Studio programming environment to allow you to customize to your requirements Please refer to the driver manual for more information.

Register Definitions

IP-1553_BASE

IP-1553_BASE 0x0000 // 0 base control register offset

BASE Control Register

DATA BIT	DESCRIPTION
15-1	Spare
0	INTFORCE

FIGURE 5 IP-1553 BASE CONTROL REGISTER BIT MAP

Intforce when set causes an interrupt to be generated to the system. Useful for debugging and software test.

IP-1553_VECTOR

IP-1553_Vector 0x0002 // 1 IP vector port

Vector Port

DATA BIT	DESCRIPTION
15-8	Spare
7-0	vector

FIGURE 6 IP-1553 VECTOR BIT MAP

If the system uses a vectored interrupt approach then the vector port should be initialized to the vector value assigned to this device. IP-1553 can be used as vectored or auto-vectored. In auto-vectored situations this port is unused. The Status port can be used to determine the source of any pending interrupts from IP-1553.

Default is 0xFF for data.

IP-1553_STATUS

IP-1553_STATUS 0x0004 // 2 base Status register

CONTROL RX

DATA BIT	DESCRIPTION
15-11	Spare
10	Ext Tag CLK Locked
9	1553 CLK Locked
8	IP CLK Locked
7	Spare
6	CH1_INT
5	Spare
4	CH0_INT
3-1	Spare
0	LOC_INT

FIGURE 7 IP-1553 INTERRUPT STATUS BIT MAP

LOC_INT is set when INTFORCE, CHO_INT or CH1_INT are set and the corresponding mask is enabled. This bit is cleared by dealing with the interrupt source.

CH0_INT and CH1_INT are the interrupts from channel 0 and channel 1 1553 interface devices. The bits are before the interrupt mask and will be set even if the channel interrupt mask is not set to allow polled operation.

The interrupt signals are inverted in hardware to provide an active high status. Each interrupt can be enabled to be set from a variety of sources. Please refer to the IMR, registers for additional channel interrupt control.

IP CLK Locked is set '1' when the local DCM is locked to the reference IP clock. Should be '1' with a stable IP clock. If '0' check your carrier clock reference.

1553 CLK Locked is set '1' when the 50 MHz reference oscillator has been locked onto, and the local 20 MHz and 40 MHz clocks generated. Should always be '1'. If '0' the oscillator or FPGA needs attention.

Ext Tag CLK Locked when '1' means an external clock is present and locked onto. If no clock is present this bit should be '0'. The external clock can be any frequency between 5 and 25 MHz. It must be stable. If expected and not present check proper connections, pin definitions etc.

IP-1553_CarrierSlot

IP-1553_CarrierSlot 0x0006 // 3 Carrier Slot Information Register

CONTROL RX

DATA BIT	DESCRIPTION
15-0	User RW Register
10-3	Initialized to Carrier Switch setting by driver
2-0	Initialized to Slot location by driver

FIGURE 8 IP-1553 CARRIER SLOT BIT MAP

The CarrierSlot Information Register is used to pass the host carrier switch setting and local slot number from the parent driver to the child driver. The carrier level driver has access during initialization to the IP location information. Due to the way some OS work the child driver [1553 in this case] do not have direct access to the location information. The carrier user switch information is read and copied to the CarrierSlot register along with the slot location [A= 0, E = 4 etc.]. Please note: this feature was added with revision 03 and later.

The user application can read the information from the CarrierSlot location to deterministically select the IP to be controlled.

The information is read when the child driver is launched and stored in local memory. The user can write over the information if the register would be useful for some other purpose.

IP-1553_Revision

IP-1553_Revision 0x000A // 5 Revision Register

CONTROL RX	
DATA BIT	**DESCRIPTION**
15-8	Major Revision
7-0	Minor Revision

FIGURE 9 IP-1553 REVISION REGISTER

The Major and Minor FLASH revisions are stored in this register. The Major Revision is copied into the IDPROM and reported when the ID Sp62203 is accessed. The Major Revision is updated when large changes are made – for example switching FPGA types. The Minor Revision is updated when any change is made to a previously released Major Revision. Added with revision 04.

See the Title page for the current Major.Minor. Also reported with the IP-1553 Win10 reference SW package.

IP-1553_ControlReg0, IP_1553_ControlReg1

IP-1553_ControlReg0,1 0x0014,0x0028 // 10,20

CHANNEL CONTROL REGISTER

DATA BIT	DESCRIPTION
15	Interrupt Mask
14	SLEEPN
13	RSTBITN
12	CH_RSTN
11-0	Spare

FIGURE 10 IP-1553 LOCAL CONTROL BIT MAP

CH_RSTN is tied to the RSTN [MSTCLRN] line on the 62203. When '0' the 62203 is held in reset. When '1' the 62203 can operate normally.

RSTBITN when set to '0' and the 62203 brought out of reset will cause the 62203 to do a BIT test. If this bit is set to '1' the BIT test is not performed. BIT can also be commanded through the SRR register. If using automatic BIT the 62203 registers will not be writeable until the BIT completes. The BIT register can be used to determine when the test is complete or a timer set.

SLEEPN when '1' allows the 62203 to go into a low power mode [transceivers]. Normally set to '0'.

Interrupt Mask when set '1' enables the channel interrupt to cause an IP level interrupt. When '0' the interrupt from the channel can still be used as a status bit, and the interrupt will not cause an IP level interrupt.

IP-1553_StatusReg0, IP_1553_StatusReg1

IP-1553_StatusReg0,1 0x0016,0x002A // 11,21

CHANNEL STATUS REGISTER	
DATA BIT	**DESCRIPTION**
15-1	Spare
0	Channel Interrupt Status CHx_INT

FIGURE 11 IP-1553 LOCAL STATUS BIT MAP

Unmasked status bit for 1553 interrupt. Same status copied in board level status register. Clear by programming action with 62203 device for appropriate channel.

Interrupts

IP-1553 interrupts are treated as auto-vectored. When the software enters into an exception handler to deal with an IP-1553 interrupt the software must read the status register(s) to determine the cause(s) of the interrupt, clear the interrupt request(s) and process accordingly. Power on initialization will provide a cleared interrupt request and interrupts disabled.

The interrupt is mapped to INT0, which is mapped to a system interrupt via the host [carrier] device. The source of the interrupt is obtained by reading the Interrupt Status register. The status remains valid until that bit in the status register is cleared.

When an interrupt occurs, the Master channel interrupt enable should be cleared and the status register read to determine the cause of the interrupt. Next perform any processing needed to remove the interrupting condition, clear the status and enable the channel interrupt again.

The individual enables operate after the interrupt holding latches, which store the interrupt conditions for the CPU. This allows for operating in polled mode simply by monitoring the Interrupt Status register.

Loop-back

The Engineering kit has reference software, which includes an external loop-back test. The test requires an external cable with the following pins connected. Channel 0A to Channel 0B and channel 1A to channel 1B.

SIGNALs	0	1
CH0AP/CH0BP	26	32
CH0AN/CH0BN	27	33
CH1AP/CH1BP	42	48
CH1AN/CH1BN	43	49

In addition either 78 or 39 ohms between P & N is added for termination depending on shunt position.

Select Direct/Transformer Coupled

J1-4 is are used for Channel 0. J5-8 are used for channel 1. Each set allows 4 shunts to be installed to select the P&N for A&B on each channel. 1-2 = Direct Coupled with 54.9Ω resistors in the path and requiring 39Ω termination. 2-3 = transformer coupled and uses the 78Ω termination resistor. We use two IP-Debug-IO cards with the two resistor values set plus loop-back wiring to make the loop-back test fixture. IP-Debug-IO has two sets of connections allowing the wiring to be added in one set and the resistors in the alternate set.

ID PROM

Every IP contains an ID PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects, and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires that a particular revision be present, it may check for it directly.

The location of the ID PROM in the host's address space is dependent on which carrier is used.

Standard data in the ID PROM on the IP-1553 is shown in the figure below. For more information on IP ID PROMs refer to the IP Module Logic Interface Specification.

Address	Data	
01	ASCII "I"	($49)
03	ASCII "P"	($50)
05	ASCII "A"	($41)
07	ASCII "H"	($48)
09	Manufacturer ID	($1E)
0B	Model Number	($0B) IP-1553
0D	Revision	($Current Major Revision)
0F	reserved	($00) Customer Number
11	Driver ID, low byte	($00) Design Number
13	Driver ID, high byte	($00)
15	No of extra bytes used	($0C)
17	CRC	($DD)

FIGURE 12 IP-1553 ID PROM

IP-1553 Logic Interface Pin Assignment

The figure below gives the pin assignments for the IP Module Logic Interface on the IP-1553. Pins marked n/c below are defined by the specification, but not used on the IP-1553. Also see the User Manual for your carrier board for more information.

GND	GND	1	26
CLK	+5V	2	27
Reset*	R/W*	3	28
D0	IDSEL*	4	29
D1	n/c	5	30
D2	MEMSEL*	6	31
D3	n/c	7	32
D4	INTSEL*	8	33
D5	n/c	9	34
D6	IOSEL*	10	35
D7	n/c	11	36
D8	A1	12	37
D9	n/c	13	38
D10	A2	14	39
D11	n/c	15	40
D12	A3	16	41
D13	INTREG0*	17	42
D14	A4	18	43
D15	n/c	19	44
BS0*	A5	20	45
BS1*	n/c	21	46
n/c	A6	22	47
n/c	Ack*	23	48
+5V	n/c	24	49
GND	GND	25	50

NOTE 1: The no-connect signals above are defined by the IP Module Logic Interface Specification, but not used by this IP. See the Specification for more information.

NOTE 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. This table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked in the silk-screen on the IP Module.

FIGURE 13 IP-1553 LOGIC INTERF62203

IP-1553 IO Pin Assignment

The figure below gives the pin assignments for the IP Module IO Interface on the IP-1553. Also see the User Manual for your carrier board for more information.

TDI	CH0AP	1	26
TMS	CH0AN	2	27
TCK	GND	3	28
TDO	GND	4	29
F3.3V	GND	5	30
RTAD0P	GND	6	31
RTAD04	CH0BP	7	32
RTAD03	CH0BN	8	33
RTAD02		9	34
RTAD01		10	35
RTAD00		11	36
EXT-TAG-CLK	GND	12	37
XTRIG0	GND	13	38
XTRIG1	GND	14	39
INCMD0	GND	15	40
INCMD1	GND	16	41
RTAD1P	CH1AP	17	42
RTAD14	CH1AN	18	43
RTAD13	GND	19	44
RTAD12	GND	20	45
RTAD11	GND	21	46
RTAD10	GND	22	47
	CH1BP	23	48
	CH1BN	24	49
		25	50

NOTE 1: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. This table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked on the IP Module.

Rev 03 and later PCB for this pin definition.
F3.3V is fused 3.3V 100 mA

FIGURE 14 IP-1553 CONNECTOR PINOUT

Applications Guide

Interfacing

The pin-out tables are displayed with the pins in the same relative order as the actual connectors. The pin definitions are defined with noise immunity in mind. The pairs should be connected with standard 1553 cabling or twisted pair wiring for best results.

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power-consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Connecting external voltage to the IP-1553 when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. Alternatively, use the isolated version.

Keep cables short. Flat cables, even with alternate ground lines, are not suitable for long distances. IP-1553 does not contain special input protection. The connector is pinned out for a standard Header cable to be used. The twisted pairs are defined to match up with the IP-1553 pin definitions. It is suggested that this standard cable be used for most of the cable run.

Custom cables can be manufactured with discrete wire header and direct connection to your mating equipment.

Terminal Block. We offer a high quality 50-screw terminal block that directly connects to the ribbon cable. The terminal block can mount on standard DIN rails. HDRterm50 [http://www.dyneng.com/HDRterm50.html]

We provide the components. You provide the system. Safety and reliability can be achieved only by careful planning and practice. Inputs can be damaged by static discharge, or by applying voltage outside of the 1553 devices rated voltages.

Construction and Reliability

IP Modules were conceived and engineered for rugged industrial environments. IP-1553 is constructed out of 0.062 inch thick high temp FR4 material.

The IP Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured against the carrier with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications they are not required.

The 4 countersunk screws are included with purchase of an IP from Dynamic Engineering. Carriers [PCIe3IP etc.] come with the standoffs preinstalled.

The IP Module provides a low temperature coefficient of .89 W/^{o}C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-^{o}C, and taking into account the thickness and area of the IP. The coefficient means that if .89 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The IP-1553 design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading forced air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.

http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering, contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 DuBois St Suite C
Santa Cruz, CA 95060
831-457-8891
831-457-4793 fax
support@dyneng.com

Specifications

Host Interface:	IP Module 8 and 32 MHz capable
1553 Interface:	1/2 Redundant Ports with full protocol support
Tx Data rates generated:	Programmable. 20 MHz reference to 62203
Software Interface:	Control Registers, Status Ports
Initialization:	Hardware Reset forces all registers [except vector] to 0.
Access Modes:	IO, Memory, ID, INT spaces (see memory map)
Wait States:	minimized based on programmed clock rate
Interrupt:	Interrupt for each 1553 port Software interrupt
Onboard Options:	Most Options are Software Programmable. Shunt options for direct and transformer coupled operation
Interface Options:	IP IO connector routed through IP Carrier. ARINC 1553 compatible cable with proper termination recommended
Dimensions:	Type II IP Module.
Construction:	High temp FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components. Programmable parts are socketed.
Temperature Coefficient:	.89 W/^{o}C for uniform heat across IP
Power:	Typical **XX** mA @ 5V in Direct Coupled Mode running channel to channel test
Temperature Range	Industrial Temperature rated –40 + 85C. Conformal Coating option for condensing environments

Order Information

IP-1553-1	IP Module with 1 redundant MIL-STD-1553 channel
IP-1553-2	IP Module with 2 redundant MIL-STD-1553 channels Holt 62203 per channel
Eng Kit–IP-1553	IP-Debug-IO - IO connector breakout IP-Debug-Bus - IP Bus interface extender
	Data sheet reprints are available from the manufacturer's web site reference software.

***Note**: The Engineering Kit is strongly recommended for first time* IP-1553 *purchases.*

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