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Est. 1988

User Manual

# IP-BiSerial-NG4

## Bi-directional Serial Data Interface IP Module

Revision A
Corresponding Hardware: Revision A

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IP-BiSerial-NG4
Bi-directional Serial Data Interface
IP Module

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# Product Description

IP-BISERIAL is part of the IP Module family of modular I/O components. The IP-BISERIAL is capable of providing multiple serial protocols. The standard protocol implemented provides a Data, Clock and Strobe interface with Ready control. The –NG4 version is a custom modification featuring two protocols, the use of synchronization signals, 32 bit data with programmable parity, delays and edge definitions.

In addition to the NG4 version other custom interfaces are available. Please see our web page for current protocols offered. If you do not find it there we can re-design the state machines and create a custom interface protocol. That protocol will then be offered as a “standard” special order product. Please contact Dynamic Engineering with your custom application.

The IP-BISERIAL-NG4 supports both 8 and 32 MHz IP Bus operation. The IP Clock and on-board oscillator are used to derive the reference clocks for the serial operation. Please be sure to select the proper clock divisors and source selector after reset to insure proper operation. Please refer to the programming section for details.

Both single ended and differential I/O are available on the serial signals. The differential drivers and receivers conform to the RS-485 specification (exceeds RS-422). The RS-485 input signals are terminated with 180Ω. The single ended driver signal is characterized as an open drain driver with 24 mA of sink. For convenience A 2KΩ pull-up is supplied on board, for faster termination a second pull-up can be added at the receiving end of the circuit. Single ended signals are received through 33Ω resistors. Care should be taken with the single ended signals, as transients can damage the board.

All configuration registers support read and write operations for maximum software convenience. Word and byte operations are supported (please refer to the memory map).

The IP-BISERIAL-NG4 conforms to the VITA standard. This guarantees compatibility with multiple IP Carrier boards. Since the IP maintains plug and software compatibility while mounted on different form factors, system prototyping may be done on one IP Carrier board, with final system implementation done on a different one.

The serial channels are supported by 32K by 16 bit FIFOs, which support word accesses. An on-board read/write path exists for loop-back testing.



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The serial receive channel looks for data in 32 bit transfers. The received bit stream is loaded into the input FIFO. The data length loaded is determined by the programmed word count, or if the RX_ALL bit is set, until the start bit is cleared or a time-out occurs. The host can poll or wait for the message complete or FIFO almost-full interrupt. The message can be read directly from the input FIFO. Several error conditions are checked including parity, framing, and over-run. Parity is ignored when the “none” option is selected.

The serial transmit channel reads data from the output FIFO and sends it out serially, msb first. Each word has a parity bit is appended. The parity is programmable for odd, even and none. The message can be any number of words long. The Transmitter supports both 3 and 4 wire operation with the parity selection. The Frame signal is always output. In 3 wire mode the Frame is ignored by the receiving hardware.

The IP-BISERIAL-NG4 utilizes the IP clock and reference oscillator as a source for the clock generator. The oscillator is 50 MHz. A programmable divider creates variable clock rates from the base rates. Please refer to the clock selection part of the programming section for details.

Interrupts are supported by the IP-BISERIAL-NG4. The interrupt occurs at the end of the transmission when data is received or sent or both. The programmable interrupts are available to provide an almost empty indicator for Tx and almost full indicator for Rx. The interrupts are individually maskable and the interrupt vector is user programmable by a read/write register. The interrupt occurs on IntReq0. The status is available for the FIFOs making it possible to operate in a polled mode.



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# Theory of Operation

The IP-BISERIAL-NG4 is designed for the purpose of transferring data from one point to another with a serial protocol.

The IP-BISERIAL-NG4 features a Xilinx FPGA. The FPGA contains all of the registers and protocol controlling elements of the BISERIAL design. Only the drivers, receivers, boot PROM and FIFOs are external to the Xilinx device.

The IP-BISERIAL-NG4 is a part of the IP Module family of modular I/O products. It meets the IP Module Vita Standard. In standard configuration it is a Type 1 mechanical with no components on the back of the board and one slot wide. Contact VITA for a copy of this specification. It is assumed that the reader is at least casually familiar with this document and logic design.

A logic block within the Xilinx device contains the decoding and timing elements required for the host CPU to interface with the IP bus. The timing is referenced to the 8 or 32 MHz IP logic clock. The IP responds to the ID, INT, MEM, and IO selects. The DMA control lines are connected to the Xilinx for future revisions, but are not used at this time. The BISERIAL design requires wait states for read or write cycles to any address. Hold cycles are supported as required by the host processor. Data remains enabled during a read until the host removes the SEL line. Local timing terminates a write cycle prior to the SEL being de-asserted. If no hold cycles are requested by the host, the IP-BISERIAL-NG4 is capable of supporting 16+ MB per second data transfer rate with a 32 MHz reference rate.

The serial I/O can support many protocols. The NG2 4-wire timing for a 32-bit transfer is shown in figure 1. The clock is free running, the data is valid on the falling edge of the clock, and the Frame and Word Sync frames the data.

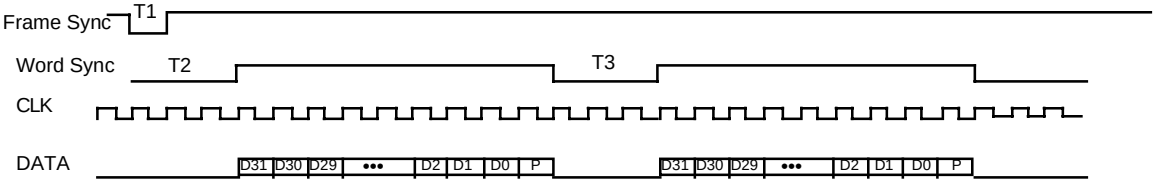



FIGURE 1 IP-BISERIAL-NG4 SERIAL PROTOCOL TIMING



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In three wire mode the receiver ignores the Frame Sync signal. The Word Sync is used to synchronize in 3 Wire mode. The transmitter still generates Frame Sync in 3 wire mode, but the signal is ignored by the receiver.

A pair of state machines within the FPGA control all transfers between the FIFO and FPGA, and the FPGA and the data buffers. The Tx state machine reads from the transmit FIFO and loads the shift register before sending the data. The Rx state machine receives data from the data buffers and takes care of moving data from the shift register into the Rx FIFO.

After the output FIFO is loaded and the start bit is detected high, the transfer begins. The Frame Sync is asserted low for a programmable length of time [T1]. The Word Sync remains low until a second time [T2] has expired. The data is read from the FIFO and loaded into the shift register. The MSB is then present at the output of the data buffer and the strobe is activated at the same time. One-half clock period later the Falling edge of the data clock is driven to the output clock buffer. One-half clock period later the data is transitioned to the next value. The MSB-1 is now on the data lines. The process repeats until the first word is transferred. Parity can be appended and sent as a 33$^{rd}$ data bit. Word sync is held low for [T3] an additional programmable inter-word gap time. Assuming that there is data to be sent in the FIFO a second word is read and loaded into the shift register and sent out onto the bus. The process is repeated until the FIFO is detected to be empty when it is time to load. The data stream is based on 32 bit words. The FIFOs are 16 bits wide. Each serially transmitted word represents two words from the FIFO. At the end of the transfer the start bit is automatically reset.

In Three Wire mode T1 and T2 can be minimized to reduce the start-up delay. T2>T1. 0x02 and 0x04 are the values used in our test software for T1 and T2 respectively in 3 wire mode. All times are counts based on the selected frequency [period].

Some IP Carriers support 32 bit data writes to IP slots performing an auto-conversion to 16 bits saving 1/2 of the data transfers. The PCI3IP and PCI5IP support auto-incrementing and static address conversion from 32 to 16 bits. http://www.dyneng.com/pci5ip.html

The receive function is similar. If the receiver is enabled and 4-wire mode is selected then the state machine scans for the Frame Sync transitioning from high to low, and then the Word Sync transitioning from low to high. Data is loaded into the receive shift register on the falling edge of the data clock. Once a word has been received the data is loaded into the receive FIFO. Parity can be checked for each word received. When the



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programmed number of words has been received an interrupt to the host is generated (if enabled). The receiver checks for over-run, parity and framing errors, depending on the mode, and if an error is detected the appropriate bit in STAT1 is set. The RX_ALL option will over-ride the word count selection to allow un-bounded length messages to be received. An interrupt stream can be generated with the Programmable Almost Full interrupt to manage the data being received.



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# Address Map

| Function | | Offset | Width | Type |
|---|---|---|---|---|
| BIS_CNTL0 | EQU | $00 | byte on word boundary | read/write |
| BIS_CNTL1 | EQU | $02 | byte on word boundary | read/write |
| BIS_CNTL2 | EQU | $04 | byte on word boundary | read/write |
| BIS_VECTOR | EQU | $06 | byte on word boundary | read/write |
| BIS_STAT0 | EQU | $08 | word | read |
| BIS_STAT1 | EQU | $0A | byte on word boundary | read/write |
| BIS_CNTL11 | EQU | $16 | word | read/write |
| BIS_CNTL12 | EQU | $18 | word | read/write |
| BIS_CNTL13 | EQU | $1A | word | read/write |
| BIS_CNTL14 | EQU | $1C | byte on word boundary | read/write |
| BIS_CNTL15 | EQU | $1E | word | read/write |
| BIS_FTX_W | EQU | $10 | word | write |
| BIS_FTX_R | EQU | $22 | word | read |
| BIS_FRX_W | EQU | $20 | word | write |
| BIS_FRX_R | EQU | $40 | word | read |

FIGURE 2 IP-BISERIAL-NG4 INTERNAL ADDRESS MAP

The address map provided is for the local decoding performed within the IP-BISERIAL-NG4. The addresses are all offsets from the IO space base address. The BIS_FTX_W and BIS_FRX_R ports are also mapped to the entire MEM address space and the BISERIAL_IDPROM is mapped to the ID space. The carrier board that the IP is installed into provides these addresses.



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# Programming

Programming the IP-BISERIAL-NG4 requires only the ability to read and write data in the host's I/O space. The base address is determined by the IP Carrier board. This documentation refers to the address where the IO space for the slot that the IP is installed in begins as the base address.

In order to receive data the software is only required to enable the Rx state machine, program the length count and FIFOs. If desired, the interrupt can be enabled and the interrupt vector written to the vector register. Data will be loaded into the FIFOs as it is received. Other options include automatic clearing of the start bit at the end of a message.

A typical sequence would be to first write to the vector register with the desired interrupt vector. For example $40 is a valid user vector for the Motorola 680x0 family. Please note that some carrier boards do not use the interrupt vector. The interrupt service routine should be loaded and the mask should be set. When the start bit is set the hardware looks to make sure that the sync is not active then begins looking for it to be active. In this manner the data received is protected from receiving partial messages. Once a new strobe assertion is detected the data loading process begins. When the word count is reached the interrupt request is asserted to let the host know that the data is available. The software can set-up a loop counter to efficiently read the data from the FIFOs. If the auto-clear feature is enabled, the Rx start bit will be cleared when the message completes and will have to be re-written before another message can be received. If continuous data is expected the PAF interrupt may be more interesting than the end of reception interrupt. Using the PAF interrupt would allow larger data blocks to be moved from the –NG2 to host memory.

The end of transmission interrupt will indicate to the software that an outgoing message has been started and that the message has terminated. If both the Tx and Rx interrupts are enabled then the SW needs to read BIS_STAT1 to see which source caused the interrupt. In order to avoid missing an interrupt, the bits in this register must be explicitly cleared by writing the appropriate bit as a '1'. The INTACK cycle will clear the actual interrupt. The interrupt status should be cleared after the INTACK cycle in order to avoid resetting the status bit. It is a good idea to clear the status bits before Start is enabled to insure that the RX_INT or TX_INT value read by the interrupt service routine came from the current reception.

Before transmitting data the FIFOs are enabled and the data loaded. The baud rate selections are used to select the output rate. The divided version



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or the base rate can be selected for the reference rate on the Tx state machine. Once the complete message is loaded and the controls set properly the start bit can be set to cause the transfer to begin. If a slow clock rate is selected and a long message is to be sent then data can be loaded during transmission to save operational time. When the Tx interrupt is received the transmission has been completed and another message can be loaded.

Messages longer than 32K words can be accommodated by the –NG4 hardware. The FIFOs are 32K deep allowing 32K words to be stored. The transmission length is determined by the FIFO MT condition. Longer transmissions can be supported by using the MT and Full flags on the FIFOs to poll during the transfer…fill the Tx FIFO and when not full add more data until full. The PAE flag can be used to provide a length programmable almost empty interrupt to allow the Tx side to operate in an interrupt driven mode with longer messages. On the receive side poll and when not empty read the data until empty. Similarly the PAF can be used to provide an almost full interrupt from the receive side to allow interrupt driven long message capability.

Refer to the Theory of Operation section above and the Interrupts section below for more information regarding the exact sequencing and interrupt definitions.



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# REGISTER DEFINITIONS

## BIS_CNTL0

$00 BISERIAL Transmit Control Register Port read/write

CONTROL REGISTER 0

| DATA BIT | DESCRIPTION |
|---|---|
| 8 | TX Parity Disable |
| 7 | spare |
| 6 | TX Odd Even Parity |
| 5 | TX clock Inverted |
| 4 | spare |
| 3 | INT FORCE |
| 2 | INT ENABLE FAE |
| 1 | INT ENABLE TX |
| 0 | START TX |

FIGURE 3 IP-BISERIAL-NG4 TRANSMIT CONTROL REGISTER 0 BIT MAP

0. START TX is set to send data. The bit is auto cleared at the end of a transmission.

1. INT ENABLE TX is the Interrupt Enable bit for the Transmit channel. The default state is off. If enabled and the master interrupt enable is also enabled then an interrupt is requested when the transmission is complete. The interrupt is cleared by an Interrupt Acknowledge cycle or disabling the interrupt.

2. INT ENABLE FAE is the Interrupt Enable bit for the Programmable Almost Empty condition. The default state is off. If enabled and the master interrupt enable is also enabled then an interrupt is requested when the FIFO level falls to the almost empty count. The interrupt is cleared by an Interrupt Acknowledge cycle or disabling the interrupt.

3. INT FORCE is used to create an interrupt for test and software development purposes. Set the bit to cause the interrupt and clear the bit to remove the interrupt. Requires the master interrupt enable to be '1' to have effect.

5. The TX clock is normally aligned to have the data change on the rising edge and stable on the falling edge. When this bit is set the clock is inverted to reverse the relationship.



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6. When the TX_ODD_EVEN bit = '1' odd parity is selected for the transmitter. If the parity bit is appended to the data sent, it is related to the data by an XOR function. If odd parity is selected then the parity bit is set to force an odd number of bits to be set [D31-0,parity]. If the parity selection is even then the parity bit is set to cause an even number of bits to be set. Example: 0x01020304 = data. If odd parity is selected then the parity bit would be = '0" because there are 5 bits set within the data making an odd total.

7. When the TX_PAR_DIS bit = '1' no parity bit is appended to the end of the data stream transmitted and the Word Sync is shortened to account for the missing bit. This bit is typically set for 3 wire mode operation. Default = append parity.

BIS_CNTL1

$02 BISERIAL Receive Control Register Port read/write

CONTROL REGISTER 1

| DATA BIT | DESCRIPTION |
|---|---|
| 10 | RX Mode Select |
| 9 | RX ALL |
| 8 | RX Parity Disable |
| 7 | ENABLE FIFO |
| 6 | RX Odd Even Parity |
| 5 | spare |
| 4 | RX AUTO-CLEAR ENABLE |
| 3 | spare |
| 2 | INT ENABLE FAF |
| 1 | INT ENABLE RX |
| 0 | STRT_RX |

FIGURE 4 IP-BISERIAL-NG4 RECEIVE CONTROL REGISTER 1 BIT MAP

0. START_RX is used to enable the receive state machine to receive messages. If the auto-clear function is enabled, the start bit is auto-cleared at the end of a received message.

1. INT ENABLE RX is used to enable the receive interrupt. The default is disabled. If enabled and the master interrupt enable is also enabled then an interrupt is requested when the Strobe returns to the off state. The interrupt is cleared by an Interrupt Acknowledge cycle or disabling the interrupt.



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2. INT ENABLE FAF is used to enable the Programmable Almost Full interrupt. The default is disabled. If enabled and the master interrupt enable is also enabled then an interrupt is requested when FIFO fills to the almost full condition. The interrupt is cleared by an Interrupt Acknowledge cycle or disabling the interrupt.

4. RX AUTO-CLEAR ENABLE when '1' enables the clearing of the start bit at the end of a message. When set to '0' the receiver will stay enabled at the end of a "frame" and receive a new frame without software intervention.

6. When the RX_ODD_EVEN bit = '1' odd parity is selected for the receiver. The parity bit is appended to the data received and is related to the data by an XOR function. The parity is calculated for the incoming word based on the odd-even selection and tested against the parity received with the data. If the parity bit does not match the parity calculated an error is flagged. The error is set in the Status Register (1). This setting should match the transmitter that the receiver is connected to for proper operation.

7. ENABLE FIFO is used to reset the FIFOs. The default state is reset and the FIFOs must be enabled to be used to store data. This signal must be set high then low then high while the FIFO clock is running to cause a proper reset with guaranteed flag operation. We suggest using the IP clock as the reference for this process. Please refer to FTX_LD and FRX_LD (control reg 2).

8. When the RX_PAR_DIS bit = '1' no parity bit is checked at the end of the data stream received This bit is typically set for 3 wire mode operation. Default = check for parity.

9. RX_ALL when '1' causes the RX state-machine to ignore the word count and to collect all data received. When set, the RX state machine will only stop operation if an error is detected and the RX_Auto_clear is set or if the Start_Rx bit is cleared by the software. If Start_RX is set to '0' while in operation the state-machine will wait until the end of the current word being received and then stop. If the receive state-machine stops due to running out of data the framing error bit will be set in the status register.

10. RX Mode is set to 3-wire with '1' and 4-wire with '0'. In three wire mode the Frame Sync is not utilized by the receiver.



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BIS_CNTL2

$04 BISERIAL Control Register Port read/write

| CONTROL REGISTER 2 | |
|---|---|
| DATA BIT | DESCRIPTION |
| 8 | RX_CLK_INV |
| 7 | EXT/INT RX CLOCK |
| 6 | MASTER INT ENABLE |
| 5 | FRX_LD |
| 4 | FTX_LD |
| 3 | spare |
| 2 | spare |
| 1 | spare |
| 0 | RX_TTL_422 |

FIGURE 5 IP-BISERIAL-NG4 CONTROL REGISTER 2 BIT MAP

0. RX_TTL_422 is the control bit to select whether the data, clock, and strobe should be received as TTL or 422 signals. Default state = 0 = 422 [485] a '1' selects TTL inputs.

4,5. FRX_LD is tied to the RX FIFO WE2/_LD pin. FTX_LD is tied to the Tx FIFO WE2/_LD pin. When the FIFOs are taken out of reset it is possible to set-up the FIFO to accept commands to program the levels at which the programmable almost empty and programmable almost full signals operate. *In the standard transfer mode these pins are set hi before CLR_FIFO is released to use as a second WE control pin*. If the PAE and PAF flags are used at a different than default depth then the flags will require programming. The default is 7 from full or 7 before empty. Please refer to the PAE PAF Programming section or the Cypress data sheet for the proper sequence.

6. MASTER INT ENABLE is the master interrupt enable. Default is 0. If set to 1 then the RX, TX, PAE, or PAF interrupts can occur based on individual interrupt enables. If the master interrupt enable is off [0] then no interrupts will be generated. The status register can still see the interrupt requests to allow polled operation.

7. EXT/INT RX CLOCK is used to select the reference clock to the Rx state machine and FIFOs. When '0' the IP clock is used to allow the interface to keep up with the IP Bus requirements. Default is '0', normal operation is 1.

8. RX_CLK_INV when '0' selects the standard falling edge reference for the received controls and data. When '1' the clock is inverted before use and the rising edge is used to capture data and sync. This setting should



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match the transmitter that the receiver is connected to for proper operation.

BIS_VECTOR

$06 BISERIAL Interrupt Vector Port read/write
The interrupt vector for the BISERIAL is stored in this byte wide register. This read/write register is initialized to 0XFF upon power-on reset or software reset. The vector is stored in the odd byte location [D7..0]. The vector should be initialized before the interrupt is enabled or the mask is lowered. The interrupt is automatically cleared when the CPU acknowledges the interrupt.



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## BIS_STAT0

$08 BISERIAL Status Port [read only]

| Data Bit | Status | |
|---|---|---|
| 7 | FTX_FF | 1 = transmit FIFO full |
| 6 | FTX_PAE | 1 = transmit FIFO almost empty |
| 5 | FTX_MT_1 | 1 = transmit FIFO 1 empty |
| 4 | FTX_MT_0 | 1 = transmit FIFO 0 empty |
| 3 | FRX_FF_0 | 1 = receive FIFO 0 full |
| 2 | FRX_FF_1 | 1 = receive FIFO 1 full |
| 1 | FRX_PAF | 1 = receive FIFO almost full |
| 0 | FRX_MT | 1 = receive FIFO empty |

FIGURE 6 IP-BISERIAL-NG4 STATUS REG 0 BIT MAP

7-0. The FIFO flags are active high. When the empty bit is '1' then the FIFO is empty. When the empty flag is '0' then the FIFO has at least one piece of data stored. When the Full Flag is set the FIFO is full. When not set then the FIFO still has room

## BIS_STAT1

$0A BISERIAL Status Port [read only]

| Data Bit | Status | |
|---|---|---|
| 8 | INT REQUEST | 1 = interrupt pending |
| 7 | Parity Error | 1 = error detected |
| 6 | Overrun Error | 1 = error detected |
| 5 | Frame Error | 1 = error detected |
| 4 | gnd | set to '0' |
| 3 | FAF_INT | 1 = interrupt pending |
| 2 | FAE_INT | 1 = interrupt pending |
| 1 | RX_INT | 1 = Interrupt pending |
| 0 | TX_INT | 1 = Interrupt pending |

FIGURE 7 IP-BISERIAL-NG4 STATUS REG 1 BIT MAP

0-3. RX_INT, TX_INT, FAF_INT, FAE_INT are set when the respective interrupt conditions exist and the interrupts are enabled. The master interrupt can be disabled and still have the benefit of the status.

4-7. Frame, Overrun, and Parity errors are tested for when a reception is



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in progress. If detected then the status bit is set. Frame error is set when the word sync control is not in the correct state. Overrun is set when the FIFO is full at the time data needs to be written to the FIFO. Parity is set if the parity calculated on the received data does not match the parity received and parity checking is enabled.

8. INT REQUEST is high when an interrupt condition exists. This bit is not masked by the MASTER INT ENABLE.

Note: All the status bits in this register are individually clearable by writing a '1' to the corresponding bit.

## BIS_CNTL11

$16 BISERIAL Control Register Port read/write

| CONTROL REGISTER 11 | |
|---|---|
| DATA BIT | DESCRIPTION |
| 14-13 | CLOCK PRE-SELECTOR |
| 12 | CLOCK POST-SELECTOR |
| 11-0 | DIVISOR |

FIGURE 8 IP-BISERIAL-NG4 CONTROL REGISTER 11 BIT MAP

CLOCK PRE-SELECTOR

| | |
|---|---|
| 00 | IP Clock |
| 01 | Oscillator |
| 10 | Oscillator |
| 11 | IP Clock |

The clock pre-selector is used to select which reference clock to use with the divisor hardware (clock source).

POST-SELECTOR when '1' sets the output clock to the divided clock, when '0' sets the output clock to the pre-selector reference value (clock source).

DIVISOR[11-0] are the clock divisor select bits. The clock source is divided by a 12-bit counter. The output frequency is {reference / [2(n+1)]}, n≥1. The reference oscillator is 50 MHz. The counter divides by N+1 due to counting from 0 to n before rolling over. The output is then divided by 2 to produce a square wave output.

If the desired frequency is 6.125 MHz., then selecting Oscillator, divided clock and a factor of 8. 2(N+1) = 8 => N = 3. 0x3003 would be the correct value to write to the Clock Control Register [Bis_cntl11].



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Please note that the standard 485 buffers are rated for 10 MHz. With most systems the larger divisors will be used. The smaller divisors are provided for use with external oscillators and the external clock line. Faster 485 buffers are available by special order. [40 MHz.]

## BIS_CNTL12

$18 BISERIAL Control Register Port read/write

| CONTROL REGISTER 12 | |
|---|---|
| DATA BIT | DESCRIPTION |
| 15-0 | T1 |

FIGURE 9 IP-BISERIAL-NG4 CONTROL REGISTER T1 BIT MAP

The value in BIS_CNTL12 will control the amount of time that the Frame Sync is asserted low for the transmitter. The delay = the count +1 with a period equal to the clock rate selected in BIS_CNTL11. The transmitter requires this parameter to be set for either mode of operation – 3 and 4 wire.

## BIS_CNTL13

$1A BISERIAL Control Register Port read/write

| CONTROL REGISTER 13 | |
|---|---|
| DATA BIT | DESCRIPTION |
| 15-0 | T2 |

FIGURE 10 IP-BISERIAL-NG4 CONTROL REGISTER T2 BIT MAP

The value in BIS_CNTL13 will control the amount of time that Word Sync is asserted low at the beginning of a frame for the transmitter. The delay = the count +1 with a period equal to the clock rate selected in BIS_CNTL11. The value in T2 *must be larger* than the value in T1 for proper operation. The time for both T1 and T2 start with the assertion of Frame Sync. The transmitter requires this parameter to be set for either mode of operation – 3 and 4 wire. The values can be minimized for 3 wire operation to reduce transmit delay.



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## BIS_CNTL14

$1C BISERIAL Control Register Port read/write

| CONTROL REGISTER 14 | |
|---|---|
| DATA BIT | DESCRIPTION |
| 7-0 | T3 |

FIGURE 11 IP-BISERIAL-NG4 CONTROL REGISTER T3 BIT MAP

The value in BIS_CNTL14 will control the Word GAP – the time when Word Sync is set low between words transmitted within a frame. The delay = the count +1 with a period equal to the clock rate selected in BIS_CNTL11.

## BIS_CNTL15

$1E BISERIAL Control Register Port read/write

| CONTROL REGISTER 15 | |
|---|---|
| DATA BIT | DESCRIPTION |
| 15-0 | RX_WRD_CNT |

FIGURE 12 IP-BISERIAL-NG4 CONTROL REGISTER RECEIVED WORD COUNT BIT MAP

The value in BIS_CNTL15 will control the number of words that are received per frame received. The receive state-machine when enabled will wait for the proper sequence of frame sync and word sync then capture data. RX_WRD_CNT words are captured, then the state-machine returns to the Frame Sync detection mode or the idle state depending on the state of the clear start [rx] bit.



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BIS_FTX_W

$10 BISERIAL TX FIFO Write

By writing a to this address data is loaded into the Tx FIFO. In addition a write to the Memory Space (any address) will also write to the Tx FIFO. The memory space write is a useful feature for software that would naturally auto-increment the address, or systems where the addresses are auto-incremented. This is the mechanism used in the auto-start mode. The write address is used to determine when sufficient data has been written to complete a message.

BIS_FTX_R

$22 BISERIAL TX FIFO Read

A loop-back path is provided for the Tx FIFO to allow the host to read the data stored in the Tx FIFO. Reading from this address fetches data from the Tx FIFO. The clock must be set to IP for source and '0' for the post-selector before reading from this register. *Once the data is read from the FIFO the data is no longer available for transmission*.

BIS_FRX_W

$20 BISERIAL RX FIFO Write

A loop-back path is provided for the Rx FIFO to allow the host to load data into the Rx FIFO. Writing to this address loads data into the Rx FIFO. This operation competes with and should not be performed during normal operation. The clock selector (BIS_CNTL2 bit7) needs to be set to internal for the Rx reference clock.



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### BIS_FRX_R

$40 BISERIAL RX FIFO Read

The data stored in the Receive FIFO can be accessed through this port. A read from the Memory space (any address) will also access this port. Use the memory space for 32 bit auto-incrementing accesses and faster transfers if your carrier supports that. Non-compelled DMA is also an option with the MEM space access.

## PAE PAF PROGRAMMING

To use the PAF and PAE flags with a setting other than the default of seven, the FIFO must be programmed. The FIFOs are configured as two 8-bit data paths in parallel The upper byte is where the flags are generated [D15-8], the lower byte flags are not used. This data path carries the programming information when the FIFO is taken out of reset with the LD controls set low. The Rx FIFO is written with the loop-back path and requires the clock settings for loop-back. The Rx and Tx FIFO can be programmed using the following procedure.

- reset the FIFOs and place into the programmable flag mode
- program the PAE/PAF flag to trigger at new value
- put into operational mode

- set LD control low with enable hi – set low for flag levels to be programmed
- set LD control low with enable low
- set LD control low with enable hi to clear the FIFO with the WE control in the load mode

- program the PAE [and PAF] to be at the new value
- first write with LD low = LSB of PAE, second = upper bits of PAE
  third = LSB of PAF and 4th = upper bits of PAF
- raise LD Control hi to resume normal FIFO operation

# INTERRUPTS

All IP Module interrupts are vectored. The vector from the IP-BISERIAL-NG4 comes from a vector register loaded as part of the initialization process. The vector register can be programmed to any 8 bit value. The default value is $FF which is sometimes not a valid user vector. The software is responsible for choosing a valid user vector.

The IP-BISERIAL-NG4 state-machines generate an interrupt request when a transmission or reception is complete and the enable bit in the control registers are set. The transmission is considered complete when the strobe line is deactivated. The interrupt is mapped to interrupt request 0.



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The CPU will respond by asserting INT. The hardware will automatically supply the appropriate interrupt vector and clear the request when accessed by the CPU. The source of the interrupt is obtained by reading BIS_STAT1. The status remains valid until the status register bits are cleared.

The interrupt level seen by the CPU is determined by the IP Carrier board being used. The master interrupt can be disabled or enabled through the BIS_CNTL2 register. The individual enables for Tx and Rx are controllable through BIS_CNTL0 and BIS_CNTL1. The enables operate before the interrupt holding latch, which stores the request for the CPU. Once the interrupt request is set, the way to clear the request is to reset the board, service the request, or disable the interrupt. Toggling the interrupt enable low will clear the interrupt input to the latch, but the STAT1 bits must be cleared before the Master interrupt enable is re-asserted or another interrupt will be generated. The interrupt enables can be set back to enabled immediately. INT ENABLE TX enables and clears the Tx interrupt and INT ENABLE RX enables and clears the Rx interrupt.

If operating in a polled mode and making use of the interrupts for status then the master interrupt should be disabled and the individual interrupts of interest enabled. When BIS_STAT1 shows and interrupt pending the appropriate FIFO action can take place and the enable toggled to remove the interrupt request then BIS_STAT1 is written to clear that interrupt request before starting the next transfer.

Power on initialization will provide a cleared interrupt request, interrupts disabled, and interrupt vector of $FF.

The programmable interrupts operate in much the same way. The programmable interrupts are triggered by FIFO level instead of Tx / Rx completion. The interrupts are cleared with the individual enables or the INTACK cycle. The levels are programmable to allow the software to respond before the FIFO is empty or full so that longer transfers can be handled without using larger FIFOs.



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## ID PROM

Every IP contains an ID PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects, and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires that a particular revision be present, it may check for it directly.

The location of the ID PROM in the host's address space is dependent on which carrier is used. Normally the ID PROM space is directly above the IPs I/O space, or at IP-base + $80. Macintosh drivers use the ID PROM automatically.

Standard data in the ID PROM on the IP-BISERIAL-NG4 is shown in the figure below. For more information on IP ID PROMs refer to the IP Module Logic Interface Specification, available from Dynamic Engineering.

Each of the modifications to the IP-BiSerial-IO board will be recorded with a new code in the DRIVER ID location. NG4 is set to 0x04 with a customer number of 0x30.

| Address | Data | |
|---|---|---|
| 01 | ASCII "I" | ($49) |
| 03 | ASCII "P" | ($50) |
| 05 | ASCII "A" | ($41) |
| 07 | ASCII "H" | ($48) |
| 09 | Manufacturer ID | ($1E) |
| 0B | Model Number | ($01) |
| 0D | Revision | ($A0) |
| 0F | reserved | ($30) |
| 11 | Driver ID, low byte | ($04) |
| 13 | Driver ID, high byte | ($00) |
| 15 | No of extra bytes used | ($0C) |
| 17 | CRC | ($94) |

FIGURE 13 IP-BISERIAL-NG4 ID PROM



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# Loop-back

The Engineering kit has reference software, which includes an external loop-back test. The test requires an external cable with the following pins connected.

| | |
|---|---|
| Frame Sync | 5 – 17 |
| Frame Sync | 6 - 18 |
| Word Sync+ | 14 - 26 |
| Word Sync- | 15 - 27 |
| Data+ | 8 - 20 |
| Data- | 9 - 21 |
| Clock+ | 11 - 23 |
| Clock- | 12 – 24 |



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## IP Module Logic Interface Pin Assignment

The figure below gives the pin assignments for the IP Module Logic Interface on the IP-BISERIAL-NG4. Pins marked n/c below are defined by the specification, but not used on the IP-BISERIAL-NG4. Also see the User Manual for your carrier board for more information.

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| GND | | GND | | 1 | | 26 | |
| | CLK | | +5V | | 2 | | 27 |
| Reset* | | R/W* | | 3 | | 28 | |
| | D0 | | IDSEL* | | 4 | | 29 |
| D1 | | n/c | | 5 | | 30 | |
| | D2 | | MEMSEL* | | 6 | | 31 |
| D3 | | n/c | | 7 | | 32 | |
| | D4 | | INTSEL* | | 8 | | 33 |
| D5 | | n/c | | 9 | | 34 | |
| | D6 | | IOSEL* | | 10 | | 35 |
| D7 | | n/c | | 11 | | 36 | |
| | D8 | | A1 | | 12 | | 37 |
| D9 | | n/c | | 13 | | 38 | |
| | D10 | | A2 | | 14 | | 39 |
| D11 | | n/c | | 15 | | 40 | |
| | D12 | | A3 | | 16 | | 41 |
| D13 | | INTREG0* | | 17 | | 42 | |
| | D14 | | A4 | | 18 | | 43 |
| D15 | | n/c | | 19 | | 44 | |
| | BS0* | | A5 | | 20 | | 45 |
| BS1* | | n/c | | 21 | | 46 | |
| | n/c | | n/c | | 22 | | 47 |
| n/c | | Ack* | | 23 | | 48 | |
| | +5V | | n/c | | 24 | | 49 |
| GND | | GND | | 25 | | 50 | |

NOTE 1: The no-connect signals above are defined by the IP Module Logic Interface Specification, but not used by this IP. See the Specification for more information.

NOTE 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module.

FIGURE 14 IP-BISERIAL-NG4 LOGIC INTERFACE



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# IP Module IO Interface Pin Assignment

The figure below gives the pin assignments for the IP Module IO Interface on the IP-BISERIAL-NG4. Also see the User Manual for your carrier board for more information.

| | | | | | |
|---|---|---|---|---|---|
| GND | RX WRD SYNC+ | 1 | | 26 | |
| REFCLK_422+ | RX WRD SYNC- | | 2 | | 27 |
| REFCLK_422- | GND | 3 | | 28 | |
| GND | tx frm sync_TTL | | 4 | | 29 |
| RX FRM SNC+ | GND | 5 | | 30 | |
| RX FRM SNC- | rx data_TTL | | 6 | | 31 |
| GND | GND | 7 | | 32 | |
| TXDATA + | rx clk_TTL | | 8 | | 33 |
| TXDATA - | GND | 9 | | 34 | |
| GND | rx wrd sync_TTL | | 10 | | 35 |
| TXCLK + | GND | 11 | | 36 | |
| TXCLK - | rx frm sync_TTL | | 12 | | 37 |
| GND | GND | 13 | | 38 | |
| TX WRD SNC + | GND | | 14 | | 39 |
| TX WRD SNC- | open | 15 | | 40 | |
| GND | GND | | 16 | | 41 |
| TX FRM SNC+ | GND | 17 | | 42 | |
| TX FRM SNC- | tx dataTTL | | 18 | | 43 |
| GND | GND | 19 | | 44 | |
| RXDATA + | GND | | 20 | | 45 |
| RXDATA - | tx clk TTL | 21 | | 46 | |
| GND | GND | | 22 | | 47 |
| RXCLK + | GND | 23 | | 48 | |
| RXCLK - | tx wrd sync TTL | | 24 | | 49 |
| GND | GND | 25 | | 50 | |

NOTE 1: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module.

FIGURE 15 IP-BISERIAL-NG4 IO INTERFACE

NG4 uses the 422 versions of data, clock, and strobe. Tx refers to the transmit and Rx refers to Receive relative to the BiSerial board.



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# Applications Guide

## Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power-consuming loads should all have their own ground wires back to a common point.

Keep cables short. Flat cables, even with alternate ground lines, are not suitable for long distances. IP-BISERIAL-NG4 does not contain special input protection.

We provide the components. You provide the system. Safety and reliability can be achieved only by careful planning and practice. Inputs can be damaged by static discharge. Proper anti-static handling proceedures must be followed.

Terminal Block. We offer a high quality 50 screw terminal block that directly connects to the flat cable. The terminal block mounts on standard DIN rails. [http://www.dyneng.com/HDRterm50.html ]

Many flat cable interface products are available from third party vendors to assist you in your system integration and debugging. These include connectors, cables, test points, 'Y's, 50 pin in-line switches, breakout boxes, etc.

IndustryPacks® are mezzanine cards which require an adapter to work in any system. IP Modules are commonly used and frequently systems have “extra” slots where the modules can be located. Dynamic Engineering has carriers for the PCI and cPCI buses. IndustryPacks are portable and can be used on third party carriers when the hardware is compliant with the IP specification.
http://www.dyneng.com/pci_3_ip.html
http://www.dyneng.com/pci5ip.html
http://www.dyneng.com/cpci2ip.html



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Different platforms have different operating system requirements. If you need a driver please contact Dynamic Engineering. Dynamic Engineering has driver expertise for Windows NT, 2000, and XP. Dynamic Engineering also writes drivers for Linux and has plans for VxWorks and Labview. We can support your effort with driver and application software or help for your software designers. Dynamic Engineering hardware designs have features to help the integrator to write and test their software quickly and efficiently – we can help you.



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## Construction and Reliability

IP Modules were conceived and engineered for rugged industrial environments. The IP-BISERIAL-NG4 is constructed out of 0.062 inch thick FR4 material.

Through hole and surface mounting of components are used. IC sockets use gold plated screw machine pins. High insertion and removal forces are required, which assists in the retention of components. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the corner pins of each socketed IC into the socket, using a grounded soldering iron.

The IP Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured against the carrier with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications they are not required.

The IP Module provides a low temperature coefficient of 0.89 W/$^{o}$C for uniform heat disipation. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-$^{o}$C, and taking into account the thickness and area of the IP. The coefficient means that if 0.89 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.



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## Thermal Considerations

The BISERIAL design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading then forced air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

# Warranty and Repair

Dynamic Engineering warrants this product to be free from defects in workmanship and materials under normal use and service and in its original, unmodified condition, for a period of one year from the time of purchase. If the product is found to be defective within the terms of this warranty, Dynamic Engineering's sole responsibility shall be to repair, or at Dynamic Engineering's sole option to replace, the defective product. The product must be returned by the original customer, insured, and shipped prepaid to Dynamic Engineering. All replaced products become the sole property of Dynamic Engineering.

Dynamic Engineering's warranty of and liability for defective products is limited to that set forth herein. Dynamic Engineering disclaims and excludes all other product warranties and product liability, expressed or implied, including but not limited to any implied warranties of merchandisability or fitness for a particular purpose or use, liability for negligence in manufacture or shipment of product, liability for injury to persons or property, or for any incidental or consequential damages.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.



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## Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

### Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

## For Service Contact:

Customer Service Department
Dynamic Engineering
435 Park Dr.
Ben Lomond, CA 95005
831-336-8891
831-336-3840 fax
Internet Address support@dyneng.com



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# Specifications

| | |
|---|---|
| Logic Interface: | IP Module Logic Interface |
| Serial Interface: | RS-485 RDY, Data, Clk, Frame Sync, Word Sync 4 and 3 wire modes. 32 bit data MSB first. Programmable parity N/O/E. |
| Tx CLK rates generated: | IP CLK, Oscillator, plus 12 bit divider to create output frequencies |
| Software Interface: | Control Registers, ID PROM, Vector Register, Status Ports, FIFOs |
| Initialization: | Hardware Reset forces all registers to 0 except the Vector Register which resets to 0XFF. |
| Access Modes: | Word in IO Space (see memory map)<br>Word in ID Space<br>Word or LW in Memory space<br>Vectored interrupt |
| Access Time: | back-to-back cycles in 500ns (8MHz.) or 125 nS (32 MHz.) to/from FIFO |
| Wait States: | 1 to ID space, 2 to IO, MEM, or INT space except for loop-back FIFO access |
| Interrupt: | Tx interrupt at end of transmission<br>Rx interrupt at end of transmission<br>Programmable Almost Empty<br>Programmable Almost Full |
| DMA: | No Logic Interface DMA Support implemented at this time<br>Memory space non-compelled supported to FIFOs. |
| Onboard Options: | All Options are Software Programmable |
| Interface Options: | 50 pin flat cable<br>50 screw terminal block interface<br>User cable |
| Dimensions: | Standard Single IP Module. 1.8 x 3.9 x 0.344 (max.) inches |
| Construction: | FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components. Programmable parts are socketed. |
| Temperature Coefficient: | 0.89 W/$^0$C for uniform heat across IP |
| Power: | Max. 220 mA @ 5V |



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# Order Information

| | |
|---|---|
| IP-BISERIAL-NG4 | IP Module with 1 Tx and 1 Rx serial channel,<br>Programmable data rates<br>NG4 protocol support,<br>RS-485 drivers and receivers<br>16 bit IP interface |
| Tools for IP-BISERIAL-NG4 | IP-Debug-Bus - IP Bus interface extender<br>http://www.dyneng.com/ipdbgbus.html<br>IP--Debug-IO - IO connector breakout<br>http://www.dyneng.com/ipdbgio.html |
| Eng Kit–IP-BISERIAL | IP-Debug-IO - IO connector breakout<br>IP-Debug-Bus - IP Bus interface extender<br>Technical Documentation,<br>1. IP-BISERIAL Schematic<br>2. IP-BISERIAL Reference test software<br>Data sheet reprints are available from the manufacturer's web site<br>reference software. |

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