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Est. 1988

User Manual
IP-QuadUART-485-PA2
Backplane RS-485 Bus Emulator IP Module

Revision B
Corresponding Hardware: Revision A
Corresponding Firmware: Revision B
10-2002-1701

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IP-QuadUART-485-PA2
Backplane RS-485 bus emulator
IP Module

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Product Description and Operation

The IP-QuadUART-485-PA2 is part of the IP Module family of modular I/O components. It is based on the IP-QuadUART-485 with the UART and all of the IO removed except for two RS-485 transceivers. Also the Xilinx FPGA has been enhanced to an XC2S100 in order to have enough internal block-RAM to accommodate the design.

The module consists of two independent interfaces that send and receive 16-bit words using RS-485 transceivers. The data is sent msb first at a 4 Mbit rate with one preceding start bit. The marking state of the link is low and the start bit is high.

The target interface is the focus of the module, but a master interface is also implemented to allow for standalone testing of the module.

All transactions are instigated by the master interface and consist of either a read or a write command and a 16-bit data word to be written to a write register or that was read from a read register. The module has 64 read registers at offset 0 – 0x7E in the IP MEM space and 64 write registers at offset 0x80 - 0xFE. These registers can be both written and read from the IP bus, but can only be read or written over the RS-485 bus.

The command word is structured as follows:

ST B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15

ST => Start bit (high)
B0 => Broadcast (low) not implemented
B1 => Write (low) or Read (high)
B2-B5 => Board address
B6-B9 => Reserved
B10-B15 => Register address

If the command is a write command, an additional 16-bit word follows that is to be written to the register determined by the register address. This data is then written to the appropriate register by the target interface.

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If the command is a read command, the data from the addressed register is read and returned by the target interface as a response to the read command.

The IP-QuadUART-485-PA2 supports both 8 and 32 MHz. IP Bus operation. The ID, IO, MEM, and INT spaces are used by the IP-QuadUART-485-PA2 design.

The IP-QuadUART-485-PA2 conforms to the VITA standard. This guarantees compatibility with multiple IP Carrier boards. Because the IP may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one IP Carrier board, with final system implementation on a different one. The PCI3IP card makes a convenient development platform in many cases. http://www.dyneng.com/pci_3_ip.html

Interrupts are supported by the IP-QuadUART-485-PA2. These consist of data received and framing error interrupts for both the master and target interfaces and an overrun error interrupt for the command FIFO. The interrupt conditions are individually maskable. The interrupt occurs on IntReqO. The vector is user programmable by a read/write register and can be read in the IO space or automatically when the INT space is accessed.

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Address Map

Function	Offset	Width	Type
IO space			
BASE_CONTROL	0x00	word	read/write
VECTOR	0x02	byte	read/write
STATUS	0x04	word	read only
COMMAND	0x06	word	write only
RESPONSE	0x06	word	read only
WRITE_DATA	0x08	word	read/write
FIFO_COUNT	0x0A	word	read only
FIFO_DATA	0x0C, 0x0E	word	read only
Memory space			
READ_REGS	0x00 - 0x7E	word	read/write
WRITE_REGS	0x80 - 0xFE	word	read/write

FIGURE 1 IP-QUADUART-485-PA2 INTERNAL ADDRESS MAP

The address map provided is for the local decoding performed within the IP-QuadUART-485-PA2. The addresses are all offsets from a base address. The carrier board that the IP is installed into provides the base address.

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Programming

Programming the IP-QuadUART-485-PA2 requires only the ability to read and write data in the host's I/O space. The IP Carrier board determines the base address of its IP modules. The carrier also supplies the IP clock and other control interface signals including the interrupt connection. See your IP carrier user manual for information on IP clock speed selection and other pertinent interface controls.

All control bits for both the Target and Master interface are in the Base Control register of the IP-QuadUART-485-PA2 (see below). Once the interfaces are configured and enabled, the Target interface will do nothing until it receives a command. If the Master interface is connected to the Target through the RS-485 I/O, read or write transactions can be initiated by writing to the COMMAND port.

The read register contents can be initialized and the write registers read using the IP MEM space address offsets. In this way full loop testing of the Target interface can be accomplished.

If interrupts are to be used, typical sequence would be to first write to the vector register with the desired interrupt vector. Please note that some carrier boards do not use the interrupt vector. The interrupt service routine should be loaded and the mask set. The desired interrupt conditions enabled and the master interrupt enabled.

A 32-bit write/read with some CPUs will result in two 16-bit accesses to the hardware with automatic incrementing addresses. This 32-bit access is quite a bit faster than a software loop. The PCI3IP, PCI5IP, and cPCI2IP are examples of carriers that support 32-bit to16-bit mapping automatically. The command FIFO data read port is on a long word boundary to utilize this feature when available.
http://www.dyneng.com/pci_3_ip.html
http://www.dyneng.com/pci5ip.html
http://www.dyneng.com/cpci2ip.html

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Register Definitions

BASE_CNTL

$00 PA2 Control Register Port - read/write

CONTROL REGISTER BASE

DATA BIT	DESCRIPTION
15-12	Board address setting
11	Check board address 0 = ignore, 1 = check
10	Enable master 0 = disabled, 1 = enabled
9	Enable target 0 = disabled, 1 = enabled
8	FIFO overrun interrupt, 1 = enabled
7	Response data frame error interrupt
6	Response data received interrupt, 1 = enabled
5	Received data frame error interrupt, 1 = enabled
4	Target data received interrupt, 1 = enabled
3	IP clock speed flag, 0 = 8 MHz, 1 = 32 MHz
2	Force interrupt, 1 = force
1	Master interrupt enable, 1 = enabled
0	Reset memory registers and FIFO, 1 = reset

FIGURE 2 IP-QUADUART-485-PA2 BASE CONTROL REGISTER BIT MAP

Bit 0: When set to '1' this bit causes all 64 read and 64 write registers to be cleared to "0x0000" and the command FIFO to be cleared and the FIFO data count set to zero. Set to '0' for normal operation

Bit 1: When set to '1' this bit allows the IP interrupt to be asserted when an enabled interrupt condition occurs. When set to '0', all interrupts are disabled.

Bit 2: When set to '1' this bit forces an IP interrupt to occur if the master enable is enabled. Set to '0' for normal operation.

Bit 3: When the IP carrier is configured to supply a 32 MHz IP clock, set this bit to '1' to allow the proper timing between the '485 interface and the IP interface. Set to '0' when an 8 MHz IP clock is being used.

Bit 4: When set to '1' this bit enables an interrupt to be generated whenever data is received by the target interface, provided the master interrupt is enabled. When set to '0', the target data received interrupt is disabled.

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Bit 5: When set to '1' this bit enables an interrupt to be generated when a framing error occurs in the target data received. This condition is detected when the RS-485 input is high after the last bit has been received. When set to '0', the target data framing error interrupt is disabled.

Bit 6: When set to '1' this bit enables an interrupt to be generated when response data is received by the master interface, provided the master interrupt is enabled. When set to '0', the master data received interrupt is disabled.

Bit 7: When set to '1' this bit enables an interrupt to be generated when a framing error occurs in the master data received. This condition is detected when the RS-485 input is high after the last bit has been received. When set to '0', the master data framing error interrupt is disabled.

Bit 8: When set to '1' this bit enables an interrupt to be generated when a command FIFO overrun error occurs. This condition is detected when the command FIFO is full when a write to the FIFO is attempted. When set to '0', the FIFO overrun error interrupt is disabled.

Bit 9: When set to '1' this bit enables the target interface to receive data over the RS-485 bus and to send a response when requested. When set to '0', the target interface is disabled.

Bit 10: When set to '1' this bit enables the master interface to send data and to receive response data over the RS-485 bus. When set to '0', the master interface is disabled.

Bit 11: When set to '1' this bit causes the board address field in a serial command to be checked against the board address bits in this register. If the bits match, the read or write operation will be performed, otherwise no read or write will occur. When set to '0', the read or write operation will be performed regardless of the board address in the command.

Bits 12..15: This field contains the board address to be checked against when checking is enabled (see the description for bit 11).

VECTOR

$02 Interrupt Vector Port - read/write

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The Interrupt vector for the IP-QuadUART-485-PA2 is stored in this byte wide register. This read/write register is initialized to 'xxFF' upon power-on reset. The vector is stored in the odd byte location [D7..0]. The vector should be initialized before the interrupt is enabled or the mask is lowered.

STATUS

$04 Status Port - read only

Interrupt Status

DATA BIT	DESCRIPTION
15-11	spare
10	FF_FL 1 = command FIFO full
9	FF_MT 1 = command FIFO empty
8	FIFO_OVRN 1 = overrun error detected
7	RSP_FERR 1 = framing error detected
6	RSP_INTR 1 = response word received
5	RX_FERR 1 = framing error detected
4	RX_INTR 1 = word received
3	spare
2	spare
1	INTRO 1 = active
0	INT_REQ 1 = active

FIGURE 3 IP-QUADUART-485-PA2 STATUS BIT MAP

Bit 0: When a '1' is read, this bit indicates that an IP interrupt has been requested. This will result in an interrupt being driven off the card if the master interrupt enable is set to a '1'.

Bit 1: When a '1' is read, this bit indicates that IP interrupt 0 has been asserted.

Bit 4: When a '1' is read, this bit indicates that a data word has been received by the target interface. The bit is latched and will be held until this register is read.

Bit 5: When a '1' is read, this bit indicates that a framing error has been detected in a data word received by the target interface. The bit is latched and will be held until this register is read.

Bit 6: When a '1' is read, this bit indicates that a response data word has been received by the master interface. The bit is latched and will be held until this register is read.

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Bit 7: When a '1' is read, this bit indicates that a framing error has been detected in a response word received by the master interface. The bit is latched and will be held until this register is read.

Bit 8: When a '1' is read, this bit indicates that a FIFO overrun has occurred in the command FIFO. The bit is latched and will be held until this register is read.

Bit 9: When a '1' is read, this bit indicates that the command FIFO is empty. When a '0' is read, it indicates that the command FIFO is not empty. This bit is not latched.

Bit 10: When a '1' is read, this bit indicates that the command FIFO is full. When a '0' is read, it indicates that the command FIFO is not full. This bit is not latched.

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COMMAND

$06 Command Data Port - write only
Writing to this address will cause the master interface to send out the data written in a serial bit-stream. This is used to test the target interface.

RESPONSE

$06 Response Data Port - read only
When a read command has been sent by writing the appropriate data word to the Command port, the response returned by the target interface can be read from this port.

WRITE_DATA

$08 Write Data register - read/write
When a write command has been sent by writing the appropriate data word to the Command port, the data to be written that is sent in the subsequent data word is obtained from this register.

FIFO_COUNT

$0A FIFO Count Port - read only
The value read from this register is the number of commands stored in the command FIFO. Each command stored is 32 bits, a 16-bit command word and a 16-bit data word that is either written or read to/from the register memory depending on the type of command.

FIFO_DATA

$0C, $0E FIFO Data Port - read only
The FIFO command data can be read from this port. Two consecutive addresses to the same port are provided so that an entire 32-bit command can be read from the IP carrier in one operation whether or not address incrementing is enabled.

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Interrupts

All IP Module interrupts are vectored. The vector from the IP-QuadUART-485-PA2 comes from a vector register loaded as part of the initialization process. The vector register can be programmed to any 8-bit value. The default value is $FF which is sometimes not a valid user vector. The software is responsible for choosing a valid user vector.

The IP-QuadUART-485-PA2 state machines generate an interrupt request when a programmed condition is detected on the IO lines. The interrupt is mapped to interrupt request 0. The CPU will respond by asserting INT. The hardware will automatically supply the appropriate interrupt vector when accessed by the CPU. The interrupt cause can be read from the Status register. There are five interrupt conditions: Rx data received, Rx data framing error, Response data received, Response data framing error, and Command FIFO overrun. If more than one type of interrupt is in use, then the status register should be read first to determine which interrupt cause is active. The exception handler can then respond to all of the current interrupt requests.

Some carrier boards pre-fetch data. If your carrier board pre-fetches the interrupt status, then the status may be cleared when the SW goes to look at it. If this is an issue then be careful with the order of reading the registers to prevent the pre-fetching function from affecting operation.

The interrupt level seen by the CPU is determined by the IP Carrier board being used. The master interrupt and individual interrupts can be disabled or enabled through the BASE_CNTL register. These enables operate after the interrupt status latches. The Interrupt acknowledge cycle fetches the vector, but does not clear the interrupt request in this design.

If operating in a polled mode and making use of the interrupts for status then the master interrupt should be disabled.

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ID PROM

Every IP contains an ID PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, identifies the installed devices by reading the ID PROM. The ID PROM contains the manufacturing revision level of the IP. If a driver requires a particular revision to be present, it may check for it directly.

The location of the ID PROM in the host's address space is dependent on the carrier used.

Standard data in the ID PROM on the IP-QuadUART-485-PA2 is shown in the figure below. For more information on IP ID PROMs refer to the IP Module Logic Interface Specification, available from Dynamic Engineering.

Each of the modifications to the IP-QuadUART-485 board will be recorded with a new code in the DRIVER ID and reserved fields.

Address		Data
01	ASCII "I"	$49
03	ASCII "P"	$50
05	ASCII "A"	$41
07	ASCII "H"	$48
09	Manufacturer ID	$1E
0B	Model Number	$07
0D	Revision	$A0
0F	reserved	$00
11	Driver ID, low byte	$01
13	Driver ID, high byte	$00
15	No of extra bytes used	$0C
17	CRC	$1A

FIGURE 4 IP-QUADUART-485-PA2 ID PROM

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IP-QuadUART-485-PA2 Logic Interface Pin Assignment

The figure below gives the pin assignments for the IP Module Logic Interface on the IP-QuadUART-485-PA2. Pins marked n/c below are defined by the specification, but not used on the IP-QuadUART-485-PA2. Also see the User Manual for your carrier board for more information.

GND		GND	1	26	
	CLK	+5V	2		27
Reset*		R/W*	3	28	
	D0	IDSEL*	4		29
D1		DMAReq0*	5	30	
	D2	MEMSEL*	6		31
D3		DMAReq1*	7	32	
	D4	IntSel*	8		33
D5		DMAck*	9		34
	D6	IOSel*	10		35
D7		n/c	11	36	
	D8	A1	12		37
D9		DMAEnd*	13	38	
	D10	A2	14		39
D11		n/c	15	40	
	D12	A3	16		41
D13		IntReq0*	17		42
	D14	A4	18		43
D15		IntReq1*	19		44
	BS0*	A5	20		45
BS1*		n/c	21	46	
	n/c	A6	22		47
n/c		Ack*	23	48	
	+5V	n/c	24		49
GND		GND	25	50	

NOTE 1: The no-connect signals above are defined by the IP Module Logic Interface Specification, but not used by this IP. See the Specification for more information.

NOTE 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module.

FIGURE 5 IP-QUADUART-485-PA2 LOGIC INTERFACE

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IP-QuadUART-485-PA2 IO Interface Pin Assignment

The figure below gives the pin assignments for the IP Module IO Interface on the IP-QuadUART-485-PA2.

n/c		n/c		1		26	
	n/c		MSTR+		2		27
TGT+		MSTR-		3		28	
	TGT-		n/c		4		29
n/c		n/c		5		30	
	n/c		n/c		6		31
n/c		n/c		7		32	
	n/c		n/c		8		33
n/c		n/c		9		34	
	n/c		n/c		10		35
n/c		n/c		11		36	
	n/c		n/c		12		37
n/c		n/c		13		38	
	n/c		n/c		14		39
n/c		n/c		15		40	
	n/c		n/c		16		41
n/c		n/c		17		42	
	n/c		n/c		18		43
n/c		n/c		19		44	
	n/c		n/c		20		45
n/c		n/c		21		46	
	n/c		n/c		22		47
n/c		n/c		23		48	
	n/c		gnd		24		49
n/c		gnd		25		50	

NOTE 1: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module. Unused pins should not be connected.

FIGURE 6 IP-QUADUART-485-PA2 IO INTERFACE

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Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power-consuming loads should all have their own ground wires back to a common point.

Keep cables short. Flat cables, even with alternate ground lines, are not suitable for long distances. The IP-QuadUART-485-PA2 does not contain special input protection.

We provide the components. You provide the system. Only careful planning and practice can achieve safety and reliability. Integrated circuits can be damaged by static discharge. Proper anti-static handling procedures must be followed.

Terminal Block. We offer a high quality 50-screw terminal block that directly connects to the flat cable. The terminal block mounts on standard DIN rails. [http://www.dyneng.com/HDRterm50.html]

Many flat cable interface products are available from third party vendors to assist you in your system integration and debugging. These include connectors, cables, test points, 'Y's, 50 pin in-line switches, breakout boxes, etc.

IndustryPacks® are mezzanine cards which require an adapter to work in any system. IP Modules are commonly used and frequently systems have “extra” slots where the modules can be located. Dynamic Engineering has carriers for the PCI and cPCI buses. IndustryPacks are portable and can be used on third party carriers when the hardware is compliant with the IP specification.
http://www.dyneng.com/pci_3_ip.html
http://www.dyneng.com/pci5ip.html
http://www.dyneng.com/cpci2ip.html

Different platforms have different operating system requirements. If you need a driver please contact Dynamic Engineering. Dynamic Engineering has driver expertise for Windows NT, 2000, and XP. Dynamic Engineering also writes drivers for Linux and has plans for VxWorks and Labview. We can support your

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effort with driver and application software or help for your software designers. Dynamic Engineering hardware designs have features to help the integrator to write and test their software quickly and efficiently – we can help you.

Loop-back Connections

The ATP software we use to test the IP-QuadUART-485-PA2 includes loop-back tests. The Engineering Kit for the IP-QuadUART-485-PA2 includes the source code for the ATP. The loop-back test is facilitated with an IP-Debug-IO card with added wire-wrapped interconnections.

Pin3 to Pin27

Pin4 to Pin28

Construction and Reliability

IP Modules were conceived and engineered for rugged industrial environments. The IP-QuadUART-485-PA2 is constructed out of 0.062 inch thick FR4 material.

Through hole and surface mounting of components are used. IC sockets use high quality plated screw machine pins. High insertion and removal forces are required, which assists in the retention of components. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the corner pins of each socketed IC into the socket, using a grounded soldering iron.

The IP Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured against the carrier with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications, they are not required. Dynamic Engineering IndustryPack Modules are shipped with a mounting kit.. [IP-MTG-KIT is available if you misplace the mounting hardware or if another IP was not shipped with the standoffs and screws]

The IP Module provides a low temperature coefficient of 0.89 W/^{o}C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-^{o}C, and taking into account the thickness and area of the IP. The coefficient means that if 0.89 Watts are applied uniformly on the component

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side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The IP-QuadUART-485-PA2 design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than one a Watt is required to be dissipated due to external loading then forced-air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

Warranty and Repair

Dynamic Engineering warrants this product to be free from defects in workmanship and materials under normal use and service and in its original, unmodified condition, for a period of one year from the time of purchase. If the product is found to be defective within the terms of this warranty, Dynamic Engineering's sole responsibility shall be to repair, or at Dynamic Engineering's sole option to replace, the defective product. The product must be returned by the original customer, insured, and shipped prepaid to Dynamic Engineering. All replaced products become the sole property of Dynamic Engineering.

Dynamic Engineering's warranty of and liability for defective products is limited to that set forth herein. Dynamic Engineering disclaims and excludes all other product warranties and product liability, expressed or implied, including but not limited to any implied warranties of merchandisability or fitness for a particular purpose or use, liability for negligence in manufacture or shipment of product, liability for injury to persons or property, or for any incidental or consequential damages.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty

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repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering

435 Park Dr.
Ben Lomond, CA 95005
831-336-8891
831-336-3840 fax
e-mail support@dyneng.com

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Specifications

Logic Interface:	IP Module Logic Interface
Features:	2 RS485 Transceivers
Software Interface:	Control Registers, ID PROM, Vector Register, Status Port, 128 16-bit registers in the IP MEM space
Initialization:	Hardware Reset forces all registers to 0.
Access Modes:	Word/Byte I/O Space (see memory map) Word in MEM Space Word in ID Space Vectored interrupt
Access Time:	back-to-back cycles in 500ns (8MHz.) or 125 nS (32 MHz.)
Wait States:	1 to all spaces
Interrupt:	Receive and Response data received and framing error interrupts and Command FIFO overrun error interrupt.
DMA:	No Logic Interface DMA Support implemented at this time.
Onboard Options:	All Options are Software Programmable
Interface Options:	50 pin flat cable 50 screw terminal block interface [HDRterm50] User cable
Dimensions:	Standard Single IP Module. 1.8 x 3.9 x 0.344 (max.) inches
Construction:	FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components. Programmable parts are socketed.
Temperature Coefficient:	0.89 W/^{0}C for uniform heat across IP
Power:	Typical **52** mA @ 5V unloaded. Additional current will be required depending on the loads applied

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Order Information

Tools for IP-QuadUART-485-PA2

IP-Debug-Bus - IP Bus interface extender with testpoints, isolated power & quickswitch technology to allow hot swapping or power cycling without powering down the host. http://www.dyneng.com/ipdbgbus.html

IP-Debug-IO II - IndustryPack IO connector breakout with testpoints, ribbon cable headers, and locations for user circuits. http://www.dyneng.com/ipdbgio.html

HDRterm50 - Ribbon cable compatible 50 pin header to 50 screw terminal header. Comes with DIN rail mounting capability. http://www.dyneng.com/HDRterm50.html

HDRribn50 – Ribbon cable in several standard lengths plus custom, with strain relief and cable pull attached. http://www.dyneng.com/HDRribn50.html

PCI3IP - 1/2 length PCI card with 3 IP slots. http://www.dyneng.com/pci_3_ip.html

PCI5IP - PCI card with 5 IP slots. http://www.dyneng.com/pci5ip.html

cPCI2IP - cPCI card with 2 IP slots. http://www.dyneng.com/cpci2ip.html

IP-MTG-KIT – 4 metric stainless screw and stand-off pairs to retain IP-QuadUART-485-PA2 against the carrier board. Flat head screws match IP Specification mounting requirements. http://www.dyneng.com/IPHardware.html

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