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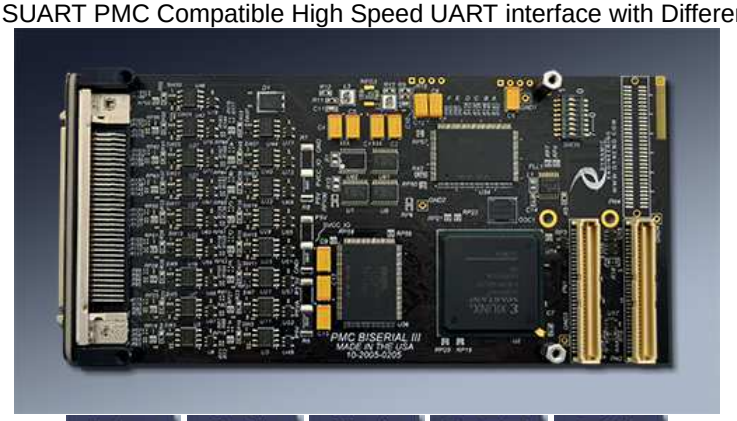
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Find the *Dynamic Engineering PMC Serial III-LM6* at our website: *Click HERE*



PMC-HSUART PMC Compatible High Speed UART interface with Differential IO



The PMC BiSerial family has been updated to include a Spartan III [Xilinx] based card with expanded capabilities.. Building on the knowledge and experience gathered from multiple IP and PMC BiSerial implementations and adding in the latest technology has created the PMC-BiSerial-III. The BiSerial III features completely isolated FIFOs with 32 bit ports for increased adaptability and performance. The [34] RS-485 / LVDS buffers have programmable termination, and direction control. Half-Duplex, Full-Duplex and single ended systems can be configured with software and VHDL. The denser, faster FPGA will implement the most complex state-machines. If you need conduction cooling the PMC BiSerial III Trans is available.

The PMC BiSerial III is recommended for new designs.

Fully independent and highly programmable RS-485 / RS-422 / LVDS IO channels are provided by the PMC-BiSerial III design. The channels are supported by two independent state-machines created within the Xilinx FPGA. The channels can have the same or different protocols. Manchester encoding and decoding, standard serial [UART], control, command, instrumentation, and custom protocols can be implemented.

Two external [to the FPGA] FIFO´s are available with 16-512K bytes each. The FIFOs are 32 bits wide to optimize data transfer from the PCI bus. The interface is optimized to minimize the latency on the PCI bus. The data transfer size can be any length on the IO side. The FIFOs support internal loop-back testing. The loop-back test can be used for BIT and for software development. The programmable FIFO flags are supported on both sets of FIFOs. Programmable Almost Full, Programmable Almost Empty, plus Full, Half Full, and Empty. The programmable flags can be set to any debth to allow the software a programmable delay from event to empty or full. The interrupts can be very useful when sending or receiving messages larger than the FIFO size. The interrupts are programmable and provisions are made to allow polling.

New with the Spartan III are internal memories. With the Spartan III 1500 and larger devices 32 1Kx16 FIFOs can be configured making for multiple channels with internal memory support when the full size FIFOs are not required. In addition the internal memories can be configured as Dual Port RAM to allow direct addressing and retransmission of repeated patterns.

The PMC-BiSerial-III has 34 transceivers which can be used for any combination of input and output functions. Parallel and serial data, multiple channels, and different hand-shaking schemes can be implemented with the quantity of IO on the PMC-BiSerial. The RS-485 transceivers support up to 40 Mhz clock and data rates. The LVDS transceivers are rated at better than 200 MHz.

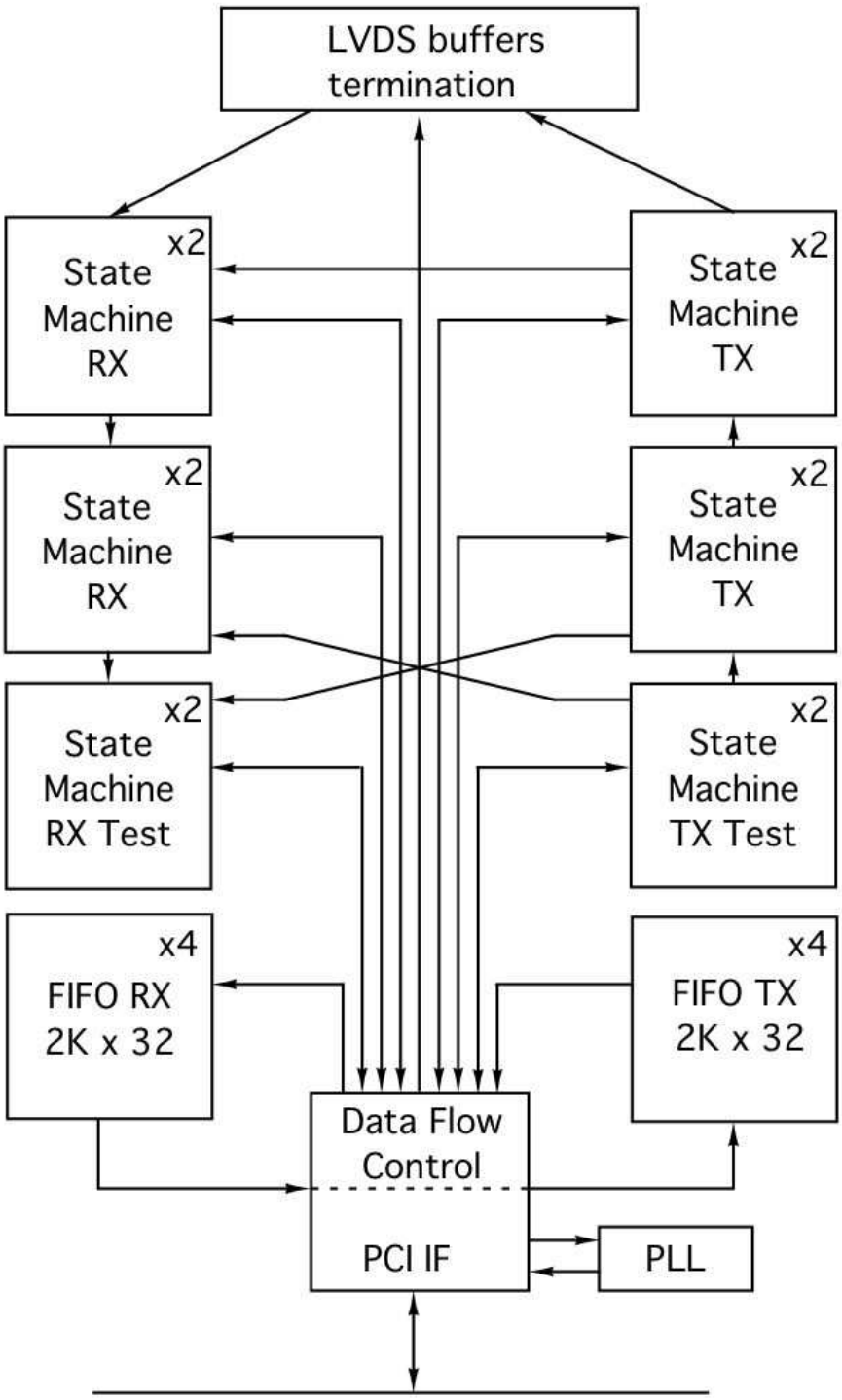
The base design has a clock multiplexer coupled with a programmable divider to provide PCI, local oscillator, PLL, and external clocking options along with divided versions. Custom oscillator frequencies can be installed when an exact frequency is required. The standard oscillator is 50 MHz. The DCM in the Xilinx along with the PLL can be used to create custom frequencies based on readily available references to allow quick turn prototyping, and on-the-fly

frequency changes.

"Channelized DMA"™ is an important feature of the PMC-BiSerial-III design. With "Channelized DMA"™ you have a separate DMA engine for each channel within the PMC BiSerial III design. Each state-machine can be serviced independently with DMA without requiring intervention from the host. Large data transfers can happen between multiple connection while the CPU is off doing something else. In non channelized designs the CPU will have to intervene each time a different port needs to be serviced. With a channelized approach the hardware takes care of the local arbitration, and eliminates the intervention for better system performance and less latency.

If your situation demands a custom application then we will update the Xilinx FPGA. Send us your timing and we will send you the interface....
Please refer to the bottom of this page for previously completed “customerized” PMC BiSerial III implementations.
email us your wish list or call today

PMC-BiSerial III Example Block Diagram



PMC BiSerial III LM6 version block diagram

See the bottom of Dynamic Data Sheet for more options

PMC-BiSerial-III Features

• Size	Standard Single PMC
• Transmit Speeds	Up to 40 MHz RS485, and up to 200 MHz LVDS signaling supported. Designed in clock generator and PLL. Location for reference oscillator for specific frequency requirements.
• PCI Speed	Standard 33 MHz. operation "Channelized DMA"™.
• PCI Access Width	Standard 32 bit operation supported.
• Software Interface	PMC registers are read-writeable. Transmit and Receive functions separated.
• Interrupts	Transmit and Receive state-machines, FIFO Programmable almost empty [transmit] and programmable almost full [receive] have programmable interrupts. Status can be polled for non-interrupt driven operation as well.
• Signaling	34 RS-485 / RS-422 / LVDS compatible IO are provided. Any combination of transmit or receive channels can be created. LVDS and RS-485 can be mixed. RS-485 bandwidth is lower when mixed [12 MHz]. Programmable termination. Pull-up and Pull-down option on IO to allow controlled level when tri-stated. Option for marking or low state.
• IO	The IO is available via the PMC bezel connector and / or the PMC “user IO” connector Pn4. The differential IO is properly routed with impedance control, pitch, and space plus matched lengths across all of the pairs. 0 ohm resistor packs are used to isolate the front and rear panel IO to allow single port designs to remove the bus stub to the removed port. Please specify if you do not want rear or front panel IO. Please note that the lower 32 channels [only] are routed to Pn4 due to pin limitations.
• Interface	Custom programmed interfaces are available. Please send us a timing diagram, and we can program one for you. Most interfaces can be adapted from our large library of designs within 1-2 weeks including the updated VHDL, Windows Driver, reference manuals etc. We can support on-site [ours] integration to help you get your application level software working. Build on our experience to save you schedule and money. You can also choose one of the already completed versions and purchase that off-the-shelf.
• Power	+5 only. 3.3V, 2.5V and 1.25V converted with on-board power supply.
• Memory	Separate FIFOs / Dual Port RAM are provided for all channels. Internal FPGA Block RAM memory modules for fast access. Optional discrete FIFOs 4K x 32, 8K, 16K, 32K, 64K, and 128K x 32 are available.
• FPGA	Xilinx Spartan III 1500 is the standard FPGA installed. Options for the “2000” or “1000” models too.

PMC BiSerial III Benefits

• Speed	The PMC-BiSerial-III is optimized for serial interfacing requirements. The FIFO memories and programmable interrupts off-load the CPU from most of the management other implementations require. The FIFO access is optimized for the PCI bus further reducing overhead by speeding up the data transfer. On the IO side the PMC BiSerial has independent channel functions. Channels can operate at maximum rate in parallel. With the Spartan III "Channelized DMA"™ can be implemented and still have plenty of gates left for your application.
• Price	The PMC BiSerial is easily programmed to implement new functions. Many previously implemented “custom designs” are available too. Without the costs of schematic level design, layout, debugging etc. a modified PMC-BiSerial-III will represent a large cost savings in your budget.
• Ease of Use	The PMC-BiSerial-III is easy to use. Point and shoot - just fill the FIFO and set the start bit to get your custom protocol transmitting. Built in loop-back capabilities and engineering kits help with integration into your system. We can write a custom Windows® or Linux driver for you.
• Availability	Dynamic Engineering works to keep the PMC BiSerial III in stock. Send in your order and in most cases have your hardware the next day. With a custom design a 1-2 week design period is usually required. We can support immediately with the another version then send updated FLASH Files later to help get your project going - right away.
• Size	The PMC BiSerial III is a standard single width PMC card and meets the PMC mechanical specifications. The PMC BiSerial III can be used in all PMC slots.
• PMC Compatibility	The PMC BiSerial is **PMC** compliant per the IEEE 1386 specification.
• PCI Compatibility	The PMC BiSerial is **PCI** compliant. You can develop with a PCI to PMC adapter - PCI2PMC or PCIBPMC.

Engineering Kits

PMC-BIS-III-ENG-1
Engineering Kit for PMC-BiSerial-III includes: Board level Schematics [PDF], Reference Software [WIN XP/2000 Driver Visual C ZIP file], HDEterm68-MP, HDEcabl68
PMC-BIS-III-ENG-2
Engineering Kit for PMC-BiSerial III includes: PCI2PMC adapter card, board level Schematics [PDF], Reference Software WIN XP/2000 Driver Visual C ZIP file], HDEterm68-M, HDEcabl68

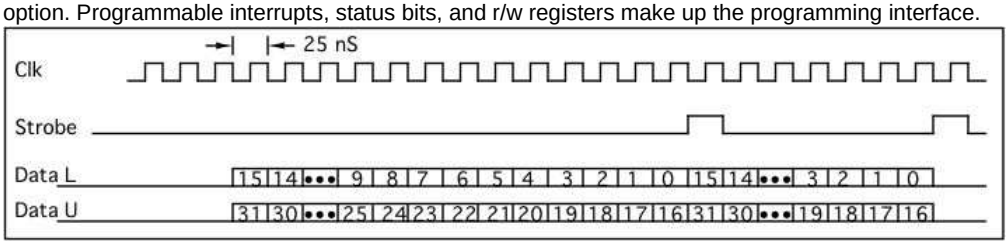
Customer Special Versions

You can order these too or request that we design one for you

PMC BiSerial III version HW1
Customer: The Goebel Company
The HW1 protocol implemented provides 32 Manchester encoded data channels per card. Each channel can operate with a selectable frequency, RX or Tx mode, unidirectional or bidirectional. CRC, Manchester, Ready_Busy, and other status provided. Internal Dual Port RAM blocks [512 x 32] used for each of the 32 channels.
Download the HW1 Hardware manual
Download the HW1 Windows® manual

PMC BiSerial III version HW2
Customer: The Goebel Company
The HW2 version implements 8 channels of the HW1 protocol, plus 24 blocks of Asynchronous or SDLC IO. The SDLC takes 4 blocks per channel and the Asynchronous takes two. Each HW1 channel can operate with a selectable frequency, RX or Tx mode, unidirectional or bidirectional. CRC, Manchester, Ready_Busy, and other status provided. Internal Dual Port RAM blocks [512 x 32] used for each of the 32 blocks. The SDLC channels are programmable for frequency using the PLL. The Asynchronous channels are designed with a UART style protocol. Please see the hardware manual for the details.
Download the HW2 Hardware manual
Download the HW2 Windows® manual

PMC Biserial III version LM5
Customer : Lockheed Martin
8 channels of half duplex serial interface. Each serial interface channel is supported with clock, strobe, and two data bits. With a 40 MHz serial clock 80 MHz data is effectively transmitted. Each channel is supported with memory in the form of a 1K x 32 FIFO to store transmit data or received data. Each channel is independent and can be programmed to be a transmitter or receiver. The IO is supported with LVDS devices and can be implemented with RS-485 as an option. Programmable interrupts, status bits, and r/w registers make up the programming interface.



Download the LM5 Hardware manual

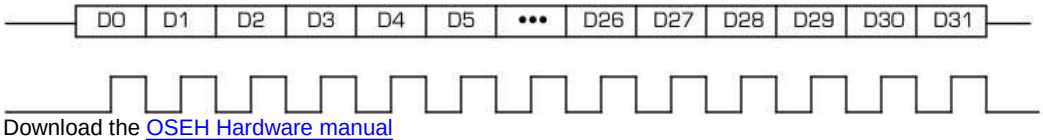
PMC Biserial III version LM6
Customer : Lockheed Martin
The protocol implemented provides four I/O channels each consisting of LVDS transmit and receive data and clock. The on-board PLL is used to generate the two clocks required for the design. The PLL is programmable, and uses a 40 MHz reference oscillator to generate a wide range of frequencies. The target rates for this design are 10 Mbits/sec for channels zero and one and 62.5 Mbits/sec for channels two and three.

Data for all channels is received MSB first using start and stop bits to separate data words. Channels zero and one send and receive 36-bit words (packets) consisting of two start bits (Œ1¹s) a 32-bit data field a parity bit and one stop bit (Œ0¹) with data changing on the falling edge of the clock (stable on the rising edge). The parity bit is calculated using even parity over the data field. A data frame is terminated with an idle packet consisting of a 36-bit word of all Œ0¹s. When no data is being sent, the data line remains in a Œ0¹ state.

Channels two and three use different formats for transmitted and received data. A transmit packet consists of one start bit (Œ1¹), a 32-bit data field, an odd parity bit and one stop bit (Œ0¹) for a total of 35 bits. The received data-word is 66 bits long consisting of one start bit (Œ1¹), a 64-bit data field and one stop bit (Œ0¹). Each data-frame begins with a sync word in the upper-half of the first data word. If this is not seen, data will still be stored, but a framing error will be latched. Parity is not used on this interface. Both interfaces have data changing on the rising edge of the clock (stable on the falling edge).
Download the LM6 Hardware manual
Download the Windows® Driver manual

PMC BiSerial III version MDS1
Customer: MDS Aero - Canada
The MDS1 protocol implemented provides 4 channel Manchester encoded serial interface. Each channel can operate with a selectable frequency, RX or Tx mode, unidirectional or bidirectional. CRC, Manchester, Ready_Busy, and other status provided. Internal Dual Port RAM blocks [512 x 32] used for each of the 32 channels.
Download the MDS1 manual

PMC BiSerial III version OSEH
Customer: restricted
The OSEH protocol implemented provides a single transmit and receive channel each consisting of an RS-485 clock and data. The transmitter can use either an external clock reference, or an internal clock reference supplied by the on-board PLL.



Download the OSEH Hardware manual
Download the OSEH Driver manual

Download the MDS1 Linux driver manual

Related Products:

HDEcabl68 SCSI II/III Cable
HDEterm68 SCSI II/III to 68 pin terminal block
PCI2PMC PCI to PMC adapter card
PCIBPMC bridged PCI to PMC adapter card
cPCI2PMC cPCI to PMC adapter card 3U 4HP
PMC Extendio II PMC extension cable set - move your PMC up to 12" away from the host.

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