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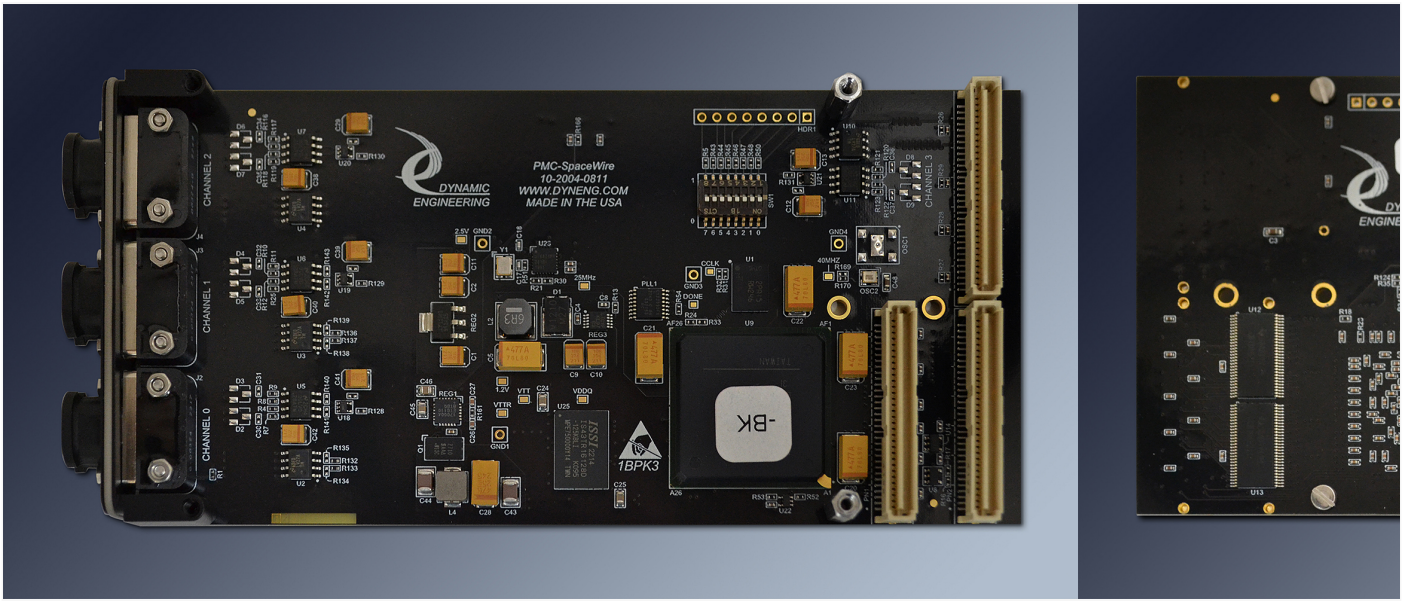
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PMC-SpaceWire

Use PMC adapter for PCIe applications



‹ Prev Next ›

Description | Features | Benefits | Ordering Info | Drivers | Manuals

PMC-SpaceWire Description

- PMC bridge to SpaceWire with 4 channels
- Designed for rapid user integration with included reference software
- Large User allocatable memory [256 MBytes] with 32 Mbyte default per port
- 8 Independent Scatter-Gather DMA engines to support the 8 SpaceWire ports
- Fast: 1-200 MHz. with autobauding on Rx ports. Each Tx port has a separate PLL reference plus divider
- Low latency, FIFO based design
- Time Code support
- Easy-to-use: heirachical design featuring a direct memory map
- 1 year warranty standard. Extended warranty available.
- Extended Temperature standard.

- ROHS and Standard processing available



Utilize SpaceWire to communicate with European Space Agency and NASA equipment utilizing the ECSS-E-ST-50-12C specification. SpaceWire is configured using routers to create a heirarchical point-to-point system with high speed parallel paths.

PMC-SpaceWire implements SpaceWire in a convenient PMC format. Four fully independent and highly programmable LVDS IO ports are provided by the PMC-SpaceWire design. The SpaceWire protocol is advanced with link testing, error handling, command and data protocols built in. The SpaceWire electrical interface is point-to-point with token based flow control. With the SpaceWire protocol it is easy to build a heirarchical architecture system with routers or a home-run wired system. Your equipment can interact with any other node in the system. PMC-SpaceWire provides a bridge from PCI ⇔ SpaceWire. Port based DMA offloads the CPU and increases performance in your system. Time Code support provides a complete solution. Please refer to the manuals tab for detailed information

Each port has memory to support RX and TX functions. **BK models have more than 32 MBytes per port.** The memory is organized as FIFOs 32 bits wide to optimize data transfer from the PCI/PCIe bus. The FIFOs are a combination of internal block RAM and attached DDR memory.

Multiple programmable interrupts are avaialble. The FIFO flags are supported for interrupt driven or polled operation. Programmable Almost Full, Programmable Almost Empty, plus Full, Half Full, and Empty. The programmable flags can be set to any debth to allow software a programmable delay from event to empty or full. The interrupts can be very useful when sending or receiving messages larger than the FIFO size. In addition interrupts and status are available for packet completion, various error conditions etc.

The FIFO design supports loop-back and can be used for Built In Test [BIT]. Memory can be accessed with target or DMA accesses. The host side interface is optimized with independent DMA controllers for each port [8 total]

SpaceWire features automatic link testing when a node is brought on line - released for operation via software. The transmitter sends NULLs until NULLs are received and then sends FCTs until FCTs are received. The initial frequency is specified [ECSS-E-ST-50-12C] to be 10 MHz. Once the auto link test has passed, the hardware can switch to the programmed rate. A local oscillator is used to supply the 10 MHz reference clock for initialization. A programmable PLL is used to support operation once the link is established. The PLL is programmed via software and is referenced to the oscillator.

The SpaceWire protocol has flow control. The local memory on PCIe-SpaceWire will not overrun. The buffering issue may be upstream - if there is an unbuffered or under-buffered data source that will loose data if the link is throttled back the large storage capability will help. The larger FIFOs will provide more room to accumulate data if the system is not ready to allow PCIe-SpaceWire to DMA transfer immediately. The DMA transfers are higher bandwidth than the SpaceWire transfers allowing the system to catch-up once the DMA transfers restart. At 100 MHz and 80% data transfer the 8Mx32 FIFO will provide about 3.2 seconds of data storage per port. The host would have to ignore the PCIe-SpaceWire interrupt requests for longer than 3.2 seconds before throttling would occur. In most systems this is sufficient time to stay out of the throttled

mode. To unload a full FIFO with DMA running it will take 8M/50M = .16mS => the unload to load multiplier is stongly in favor of the host side allowing the host to catch-up to the SpaceWire link once the delaying event has passed. The actual DMA time will be a bit higher due to system interaction to initialize etc. The actual transfer time is shown.

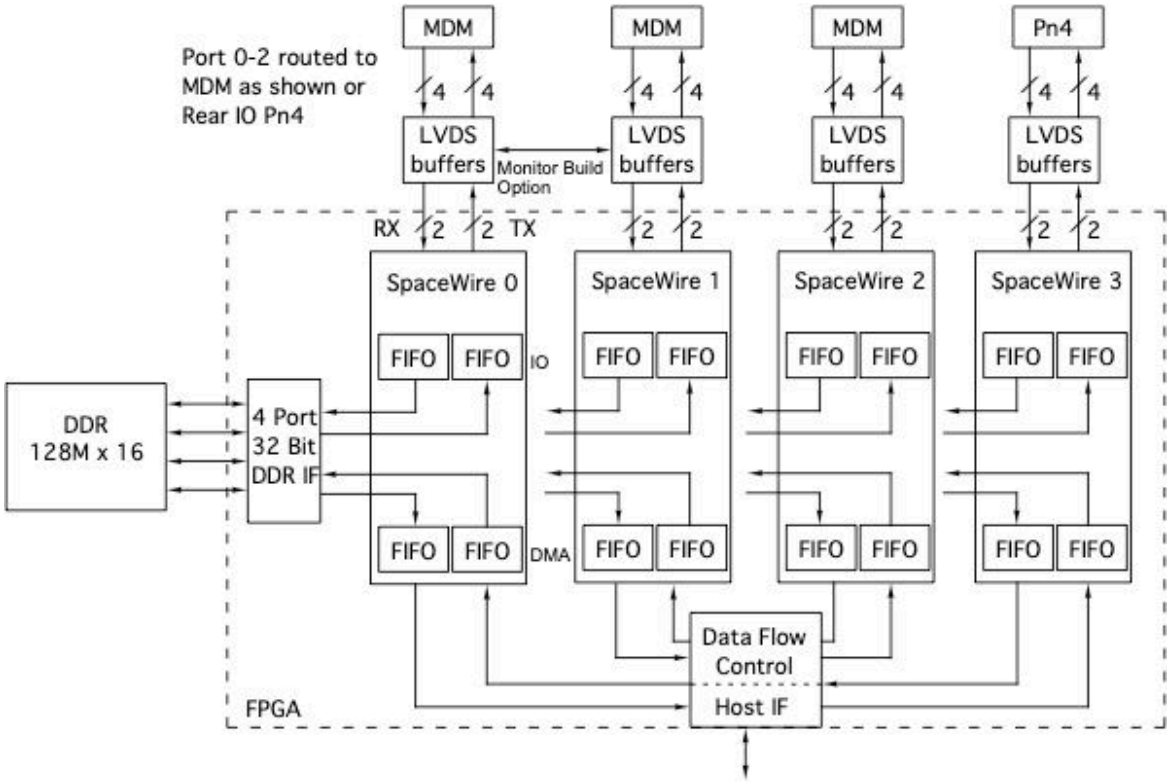
The Dynamic Engineering software packages support each of the board features including PLL programming - supply the .jed file and our SW takes care of programming, FIFO loop-back, external loop-back etc. The reference software is a great starting point for your system software.

Model -BK is recommended for new projects and projects that want an upgrade. For PMC-SpaceWire the K revision is now depricated and only available on special request.

PMC-SpaceWire is supported with the DESWBO (deswbo.html) Dynamic Engineering SpaceWire BreakOut tool for debugging SpaceWire systems, cables (SpaceWireCable.html), and the DESWCB (deswcb.html) Dynamic Engineering SpaceWire Connector Board which provides a SpaceWire Cable to system cable interface.

If your situation demands a custom application then we will update the Xilinx FPGA. Send us your timing and we will send you the interface.... email (mailto:engineering@dyneng.com) us your wish list or call today!

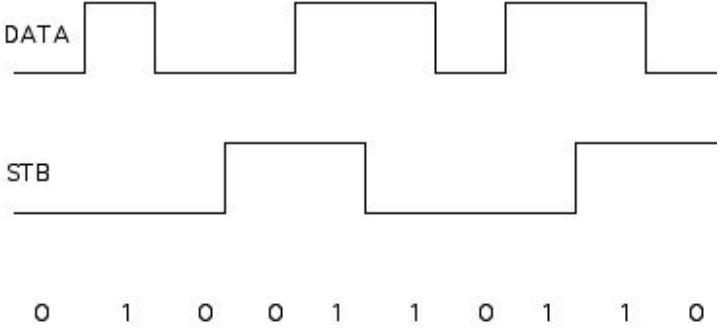
PMC-SpaceWire-BK Block Diagram



Model BK diagram shown

The standard timing uses the data and strobe to transmit and to receive the data. The data is transmitted as a command or data. The strobe provides the transitions for clocking when the data is unchanged between adjacent bit times.

PMC-SpaceWire Standard Timing



Related Products

PCIeBPMCX1 (pciebpmcx1.html)
4 Lane PCIe adapter for PMC

cPCIBPMC3U32 (cPCIBPMC3U32.html)
cPCI adapter for PMC-SpaceWire-BK

PC104p-SpaceWire (pc104p_SpaceWire.html)
PC104p with SpaceWire ports, PLL, DMA

PCI-SpaceWire (pci_SpaceWire.html)
1/2 length PCI with 4 SpaceWire ports, PLL, DMA

DESWBO (deswbo.html)
Analyze SpaceWire Link Operation

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