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# V660

## Programmable Clock Generator



The Model V660 is a single-width, C-size, register-based, VXIbus module providing a very flexible, programmable, multi-step clock generator for clocking ADCs and other front-end data acquisition modules.

It provides a programmable sequence of clock rates for applications requiring different sampling rates during different phases of data collection.

Creates custom clock rate profiles for digitizing signals

## APPLICATIONS

Acoustic/vibration measurements

High-speed dynamic tests

General-purpose analog data recording

## FEATURES

- Programmable frequency sequence of up to 256 steps
- Programmable frequency range from 0.5961 Hz to 10.24 MHz
- Strobe and gate outputs to delineate groups of output clocks (steps) programmably by number of clocks per group, number of external input triggers, or by VXI command
- Optional interrupt generation at end of each program step


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## GENERAL DESCRIPTION

The Model V660 is a single-width, C-size, register-based, VXIbus module providing a very flexible, programmable, multi-step clock generator for clocking ADCs and other front-end data acquisition modules. It provides a programmable sequence of clock rates for applications requiring different sampling rates during different phases of data collection. In addition, it provides the ability to synchronize data sampling with external triggers as well as the ability to use an external clock source for output clock generation.

The V660 provides storage for sequences as long as 256 steps in which the frequency and duration of each step can be programmed. The module derives the output clock from one of three sources: a 10 MHz crystal clock, a 10.24 MHz crystal clock, or an external clock. Each step is defined by a division factor by which the base clock is divided. The duration of each step is determined by an associated count or external trigger. In the case of external trigger, the next step is initiated synchronously with the second tick of the base clock. An optional interrupt can be generated at the end of any step to signal the host processor that a new step has been initiated. The current frequency division, current step, sample count, previous step sample count, and program step address are directly accessible registers.

The frequency steps are loaded by software into the Program RAM. Each step includes a base frequency divisor, a step termination selection based on a specific count, external trigger, or software command only as well as a flag word that selects various options on a step-by-step basis. The frequency divisor is a 16-bit, modulo-N value by which the base frequency is divided. This provides a frequency range from 152.59 Hz to 10 MHz for the 10 MHz base clock. For low frequency applications, the base clock may be pre-divided by 256, providing frequency ranges of 0.5961 Hz to 39.062 kHz (10 MHz base clock) or 0.6104 Hz to 40.0 kHz (10.24 MHz base clock). A 24-bit count field permits up to 16 Msamples per step. When external trigger is selected, these bits are used to select a trigger divisor. A value of "4" would, for example, terminate the step on the 4th trigger.

The module is also capable of generating the following signals at the completion of a step:

- Generate an interrupt,
- Generate a 35 ns, high-true, TTL output pulse on one or two front-panel Step Complete Strobes,
- Generate a 35 ns, high-true, TTL output pulse at the completion of the last program step.

Additionally, the module can selectively set or clear a TTL-level signal at the start of each step. This signal is available on the Gate Out LEMO connector on the front panel.

The following control options are associated with each program step:

- Select External Trigger, output pulse count, or software step termination,
- Disable clock output pulse for step duration (used to generate a delay).

The base clock frequency is selected by bits in a register in Operational Space.

A Previous Pulse Count register is provided. It is loaded with the current sample count at the end of each step and is accessible by VXI command. This register may be read following the completion of a step to determine the number of samples from that previous step. Thus, the actual number of samples acquired during a step that was terminated by an external trigger or VXI command can be determined.

The V660 supports both static and dynamic configuration. It may be accessed using A24/A16, D16 data transfers.

| Item | Specification |
|---|---|
| Output Pulse Width | Half of selected clock source period |
| Clock Selection | 10 MHz, 10.24 MHz, or external; programmable |
| Internal Clock Source<br>Overall stability | <br>±0.0025%, 0°Cto+70°C |
| External Clock Source<br>Maximum input frequency<br>Minimum pulse width | <br>10 MHz<br>45 ns |
| Output Connector Types | Single-pin LEMO receptacle, shell size 00 |
| Power Requirements<br>+5 V | <br>2.1 A, typical |
| Environmental and Mechanical<br>Temperature range<br>Operational<br>Storage<br>Relative humidity<br>Cooling requirements<br>Dimensions<br><br>Front-panel potential | <br><br>0°C to +50°C<br>-25°C to +75°C<br>0 to 85%, non-condensing to 40°C<br>10CFM<br>340 mm x 233.35 mm x 30.48 mm (C-size VXIbus)<br>Chassis ground |

**RELATED PRODUCTS**

| | |
|---|---|
| Model 5857-Axyz | Cable—1-contact LEMO to Unterminated |
| Model 5 85 7-Bxyz | Cable— 1 -contact LEMO to 1 -contact LEMO |
| Model 5857-Hxyz | Cable—1-contact LEMO to BNC shielded |
| Model 5 910-Z1A | Connector— 1 -contact LEMO |

## ORDERING INFORMATION

| MODEL | DESCRIPTION |
|---|---|
| V660-ZA11 | Programmable Clock Generator |

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