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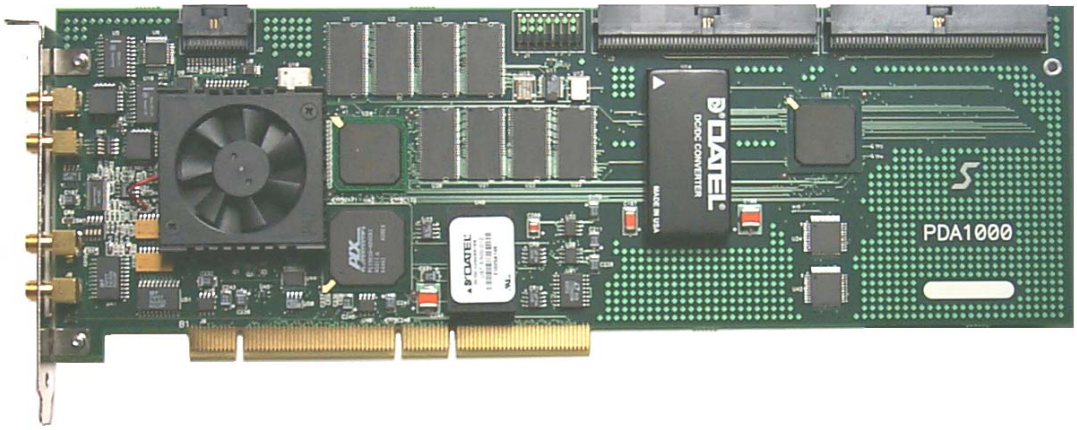
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Find the *DynamicSignals / Signatec PDA1000* at our website: ***Click HERE***

Product Information Sheet

PDA1000

1 GHz Waveform Digitizer



FEATURES

- Single channel at up to 1 GHz sample rate
- Bandwidth from DC-500 MHz
- 256 Megabytes of on-board memory
- 500 MB/s transfer via Signatec Auxiliary Bus (SAB)
- 266 MB/s transfer (peak) over PCI bus
- 8 bit resolution
- 64/32 bit PCI Plug and Play compatible board

APPLICATIONS

- Radar
- Mass Spectroscopy
- Mass Spectrometry – Time of Flight
- Communications
- Ultrasound
  Medical Diagnostics / Non Destructive Testing
- Laser Doppler Velocimetry
- High Speed Waveform Capture

OVERVIEW

The PDA1000 is the state of the art in ultra high-speed waveform capturing systems. It features an analog bandwidth of DC to 500 MHz and digitization rates of up to 1 GHz. It employs an extraordinary memory depth of 256 megasamples for capturing extremely long events. The entire memory may be used as a giant FIFO for acquiring data directly to either the SAB or PCI bus.

The PDA1000 is a 64-bit PCI compatible board equipped with standard 'Plug and Play' features common in PCI systems. It is capable of Bus Master DMA data transfers at a sustained rate of 250 megabytes/second. It can also operate in 32-bit PCI slots in which case the transfer rate will be limited to about 120 megabytes per second.

The PDA1000 incorporates the advanced Signatec Auxiliary Bus (SAB) that allows for data transfers of up to 500 megabytes/second. This allows for the high-speed transfer of data to fast processor boards, such as Signatec's PMP8A, or other peripherals. The SAB also incorporates device control features for operating the PDA1000 independent of the host bus.

The PDA1000 is equipped with an interconnect port to allow multiple boards to be interconnected in a Master/Slave configuration. Up to three Slave boards may be operated with one Master. Master/Slave connections are via a ribbon cable that connects at the top of the board. In this configuration the clock and trigger signals from the Master drive the Slave boards so that data sampling on all boards occurs simultaneously.

The PDA1000 has six software selectable signal amplitude ranges from a maximum of 3.2 volts down to 200 millivolts full scale. Extreme care was taken in the design of the front-end analog circuitry to minimize noise and distortion.

External clock and trigger signals are provided via SMA connectors on the back bracket. Also provided is a user selectable digital output signal for synchronization purposes. Effectively, eleven internal clock frequencies may be selected from 1.0 GHz down to 977 kHz in factors of 2.

The PDA1000 supports single shot, segmented, and pretrigger triggering modes with delayed triggering or pretrigger samples.

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HARDWARE DESCRIPTION

Refer to the PDA1000 block diagram page that shows a simplified mechanization for the PDA1000. The input signal may be set for either DC or AC coupling. The amplifier/attenuator may be set to one of six full scale voltage ranges from 200 millivolts to 3.2 volts peak-to-peak. For test purposes, the ADC input may be fed a sine wave test signal (via multiplexer MX5) for measuring the AC performance at a single frequency.

When sampling at 1 GHz the ADC outputs 2 samples (16 bits) every 2 nanoseconds. The demultiplexer widens the data width to 64 bits and drops the update rate to 8 nanoseconds or 125 MHz. The Pretrigger Samples Shift Register is programmable in length up to 32k samples. It can be used to capture pretrigger samples in either the Single Shot or Segmented trigger modes. Before a trigger is received, data is written into the shift register but goes no further. After receiving a trigger, data samples are passed down the data path. See the section "Trigger Modes and Options" for trigger mode details.

The Data Byte Shifter shifts the location of the 8 data bytes within the 64-bit data stream, based on the occurrence of the trigger signal. Byte 0 will be set to be the first sample that occurred after the trigger signal.

The Clock Divider Multiplexer is the means by which the effective digitization rate is reduced. The ADC always operates at 1 GHz when the internal clock is used or else at the external clock frequency. To operate at other digitization rates this circuit is used to effectively reduce the sample rate by dropping out the appropriate data bytes from the data stream. Thus the effective sample rate is divided from 2 to 1024 in factors of 2.

Data is written into the SDRAM via FIFO1 and read from RAM via FIFO2. The RAM operates at a clock rate of 133 MHz so it has a bandwidth capability of slightly greater than 1 GSPS. When data is being acquired at a 1 GHz sample rate the only operation possible is writing it to RAM via FIFO1. At an acquisition rate of 500 MHz or lower it becomes possible to interleave read and write operations to the RAM. This makes it possible to operate the RAM as a very large FIFO when acquiring data directly to the PCI bus or SAB.

The PDA1000 has 13 operating modes:

- Off
- Standby
- Acquisition to RAM
- Acquisition to PCI Bus (Direct)
- Acquisition to PCI Bus (Buffered)
- Acquisition to SAB (Direct)
- Acquisition to SAB (Buffered)
- Data Transfer, RAM to PCI bus
- Data Transfer, RAM to SAB
- PCI write to RAM
- SAB write to RAM
- PCI Read Time Stamps
- SAB Read Time Stamps

The Off mode powers down most of the circuitry on the PDA1000 board to reduce power consumption and heat buildup. At system power up the board defaults to this mode. The Standby mode applies power to all circuitry except (possibly) the data acquisition circuits, depending on user settings.

In the Acquisition-to-Bus modes, Direct Acquisition passes data directly from FIFO1 to the chosen output bus while Buffered Acquisition passes data from FIFO1 to RAM to FIFO2 and then to the bus, effectively using the RAM as a very large FIFO. Direct Acquisition is primarily used when minimum data latency at the output bus is important.

The RAM write modes may be used to test the on-board memory by writing data via the PCI or SAB bus. Data may be read back using the matching data transfer mode.

External Inputs/Outputs

Besides the signal input, the PDA1000 also provides SMA connections for a clock input, a trigger input, and a digital output signal. The clock input can be selected as the ADC sample clock. The external trigger can be used to synchronize the start of data acquisition with an external event. Trigger parameters such as trigger level, slope, etc. are user programmable. The digital output is a user selectable signal. A synchronous clock and trigger plus other useful signals are available.

Trigger Modes and Options

In data acquisition mode three triggering methods are available: single shot, segmented, or pretrigger.

With single shot, a valid trigger signal causes the entire active memory to be filled. With segmented triggering, a separate trigger signal is required to successively fill each memory segment until the designated number of *Total Samples* is acquired.

With *Pretrigger Sampling* (not the same as pretrigger samples), the board is armed and continuously fills the entire active memory until a stop trigger is detected, after which a programmed number of post trigger samples may be taken. Pretrigger sampling is primarily used when the most important information to be acquired happens before the occurrence of the triggering signal. When using pretrigger sampling the delayed trigger is functional and can be used to capture a number of samples after the trigger.

Samples Settings

There are several board settings that affect the quantity and method of acquiring samples.

Total Samples – In the "post-trigger modes" this is the number of samples that will be taken after which the memory will be considered "full" and the acquisition is terminated. When a full condition is detected, a flag is set which may be read, or an interrupt signal may be generated for the PCI or SAB buses. The amount of memory that is activated for data acquisition may be set from 8 bytes to the full 256 megabytes in steps of 8 bytes.

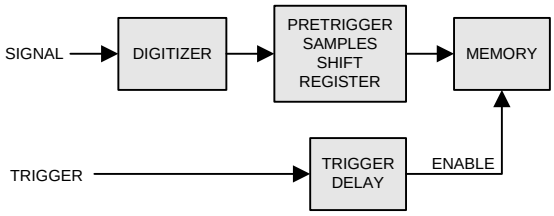
Segment Size – In Segmented Mode this is the number of samples that will be taken each time a valid trigger signal is detected.

Pretrigger Samples – In Single Shot or Segmented Modes, this is the number of samples that will be recorded into RAM that occurred before the trigger.

Delayed Trigger – This sets a delay between the actual applied trigger and the effective trigger for the board. The delay range is from 0 to 524,280 digitizer clock cycles in steps of 8 cycles. In Pretrigger Samples mode the delayed trigger setting establishes the number of post-trigger samples that will be recorded.

Pretrigger Samples and Delayed Trigger

The manner in which pretrigger samples and trigger delay affect data acquisition is depicted in the figure below.



With single shot or segmented triggering the digitized analog waveform is passed to the pretrigger samples shift register as soon as the board is placed into one of the acquisition modes. The length of this shift register is user programmable. As the data exits the shift register it is not stored into memory until after a trigger is detected and the trigger delay is completed.

Normally, if the delayed trigger function is used the pretrigger samples are set to zero. Conversely, if pretrigger samples are desired the trigger delay would typically be set to zero. This is because one counteracts the other. For example, if the trigger delay and pretrigger samples are both set to 100 then the net effect is that the stored data reflects 0 trigger delay and 0 pretrigger samples.

If Pretrigger Sampling is selected (not to be confused with pretrigger samples), digitized data is passed through the pretrigger samples shift register and into memory as soon as the board is placed into one of the acquisition modes. The delayed trigger signal is now used as a disable signal for the memory. Pretrigger samples should normally be set to 0 in this mode and the trigger delay can be used to acquire post-trigger samples. At the end of acquisition the ending memory address can be read so that the location of the trigger signal within the waveform data can be determined. In this mode RAM will operate as a circular buffer.

Time Stamps

In Segmented Mode "time stamps" allow for storing the time relationship between the memory segments. Time Stamps are 32 bit timer values with a clock resolution of 8 nanoseconds. Up to 2048 time stamps are accumulated in memory separate from the data. Time stamps are read after the acquisition is completed using one of the "Read Time Stamps" operating modes.

SAB Operation

The PDA1000 can perform SAB data transfers at 64 bits, or at 32 bits over either the high (SABH) or low (SABL) bus ports. This provides flexibility when multiple boards are incorporated into a system. At 64 bits the maximum transfer rate is 500 MB/s.

PCI Operation

The PDA1000 is capable of sustaining a data transfer rate over the PCI bus of approximately 250 megabytes per second when installed in a 64 bit PCI slot. It can also be installed in traditional 32-bit slots in which case the maximum rate is about 120 megabytes per second.

Using RAM as FIFO

The PDA1000 incorporates 256 megabytes of on-board memory (RAM). While the size is unprecedented, even more important is how the memory can be utilized. Traditionally, data acquisition boards must first acquire to the RAM and then, after the RAM is full, transfer the data off-board. The PDA1000 incorporates *Buffered Acquisition* modes whereby the entire on-board memory may be utilized as a giant FIFO. This allows off-board data transfers to occur while data acquisition is still in progress.

The large memory size makes it possible to perform acquisitions to the PCI bus with no data "drop-outs". In today's PC systems the PCI bus will be periodically taken over for system tasks and during these times an acquisition board must have a sufficiently large buffer to prevent data loss. With the PDA1000, direct acquisition to PC RAM at more than 200 MHz sample rate is possible. Under these conditions several gigabytes of data can be acquired.

GLOSSARY

Buffered Acquisition: A data acquisition mode in which the PDA1000's on-board RAM is used as a FIFO. Digitizer data is placed into the RAM FIFO and read out over either the PCI or SAB bus at a rate that the bus can handle.

Delayed Trigger: This sets a delay between the actual applied trigger and the start of data recording. In Pretrigger Samples mode the delayed trigger setting establishes the number of post-trigger samples that will be recorded.

Pretrigger Samples: For Single Shot or Segmented triggering, this is the number of samples that will be written into RAM that occurred before the trigger.

SAB: Signatec Auxiliary Bus; This is a 64-bit bus located at the top right side of the board. It provides a 500 megabyte/sec data path to other boards such as Signatec's PMP8A DSP board, DAC200 Waveform Generation board, or to a user's proprietary design. An SAB specification is available at the Signatec web site.

Second Harmonic Distortion: The ratio of the power at twice the fundamental frequency to the power of the fundamental sinusoid.

Segment Size: In Segmented Mode this is the size of the "memory segment", which is the number of samples taken each time a valid trigger signal is detected

SFDR: Spurious Free Dynamic Range: The ratio of the fundamental sinusoidal power to the power of the next highest spurious signal. Normally the highest spurious signal is the second or third harmonic.

SINAD: Signal to Noise and Distortion: The ratio of the fundamental sinusoidal signal power to the total noise and distortion component power. In other words this is the ratio of the fundamental signal power to the measured power from the remainder of the detectable spectrum from dc to 500 MHz.

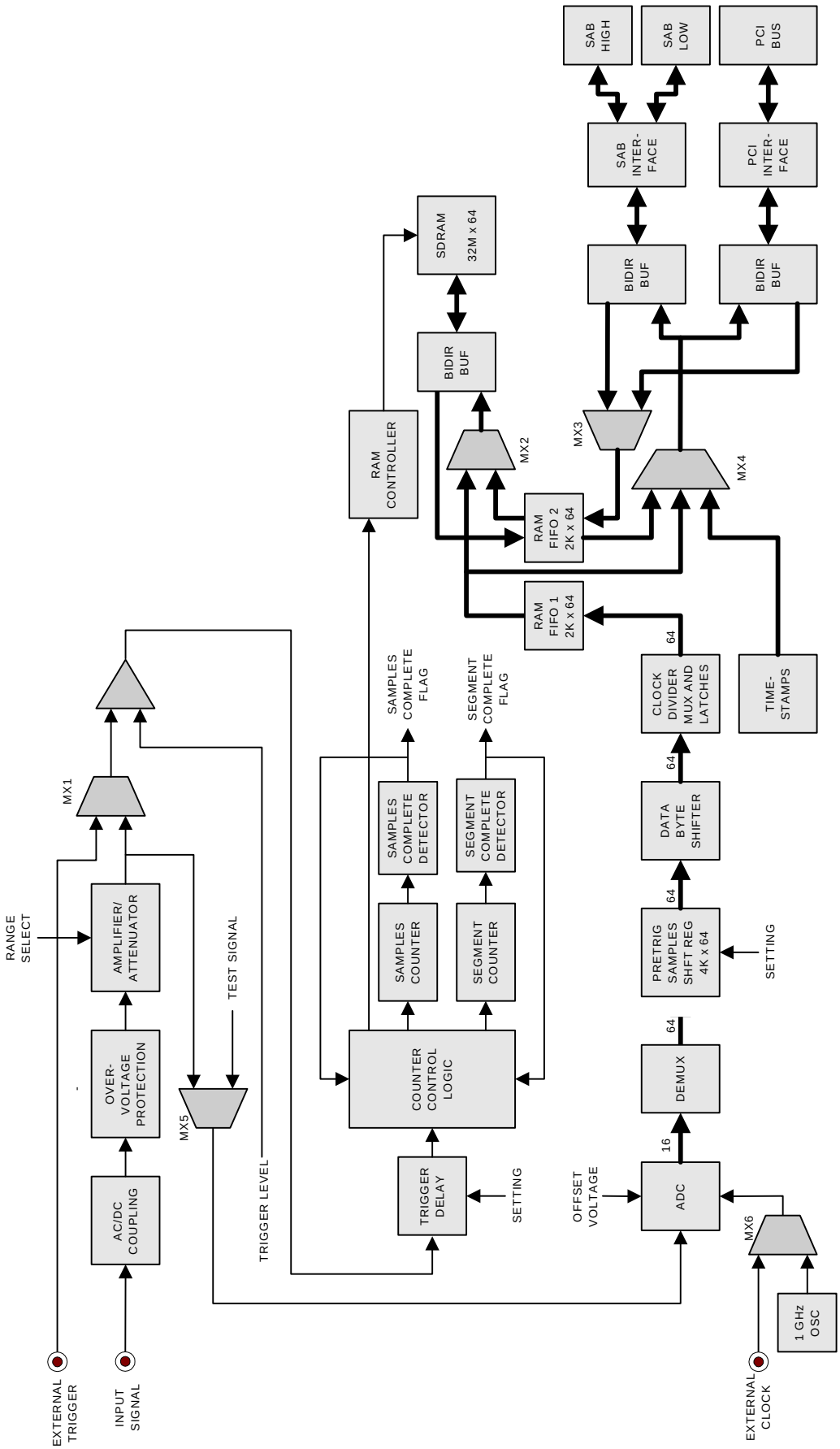
SNR: Signal to Noise Ratio: The ratio of the fundamental sinusoidal signal power to the noise power. For this data sheet noise is considered to be the power from all spectral components except for the fundamental signal, the first harmonic, and the second harmonic.

THD: Total Harmonic Distortion: The ratio of the total power of the second and third harmonics to the fundamental sinusoidal power.

Third Harmonic Distortion: The ratio of the power at three times the fundamental frequency to the power of the fundamental sinusoid.

Time Stamps: A 32-bit timer value that denotes the relative time of occurrence for each memory segment when segment triggering is selected.

Total Samples: Typically this is the total number of samples that will be acquired before acquisition is complete.



PDA1000 SIMPLIFIED BLOCK DIAGRAM

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SOFTWARE, SYSTEM, AND PERFORMANCE DETAILS

Software

The PDA1000 is supplied with the following software:

- Windows NT/2000/XP & Linux Drivers
- C Function Library with source code
- PDA1000 Class (C++) that wraps the Library functions and handles the tedious initializations and basic operations.
- Software manual that describes how to use the available library of functions to create larger applications or systems.
- A board diagnostics self test program.
- Multiple Coding examples
  - ✓ Acquire with DMA transfer to PC
  - ✓ Digital oscilloscope interface software
  - ✓ Using multiple PDA1000 boards (with Master/Slave support)
  - ✓ SAB data transfer examples

Maestro support for the PDA1000

- Menu driven board settings for multiple PDA1000 boards
- Using the PDA1000 as a high-speed recording system
- Using the PDA1000 as a high-speed recording system with the PMP8A (or any other SAB Active Slave capable device)
- Data Analysis tools for poking/peeking onboard memory

System Capabilities

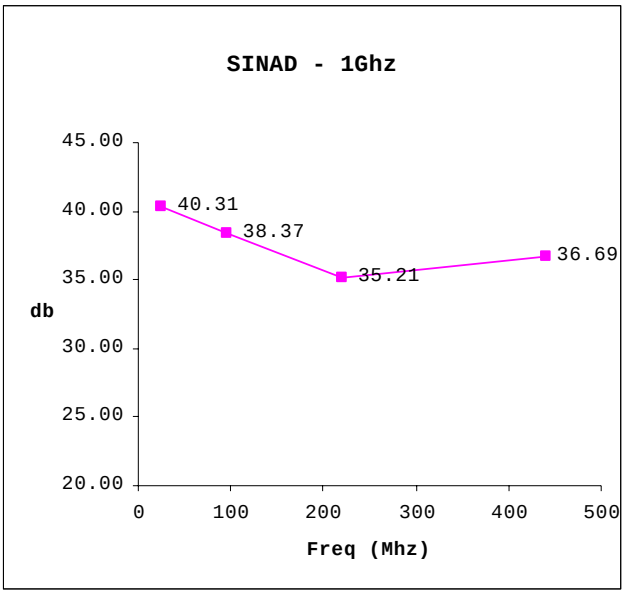
The system solution offered by Signatec is based on supplying a comprehensive range of products incorporating the Signatec Auxiliary Bus. This 64-bit bus provides transfer rates up to 500 MB/s. SAB boards act as modular building blocks for constructing high performance systems that mechanize a wide variety of applications. Shown in the figure below are elements of such a system. Many systems can be constructed using standard desktop PC's. For demanding applications Signatec can supply a total turnkey system utilizing one of our industrial computer systems.

Devices connected to the SAB may communicate via SAB interrupt and control lines. This allows the boards to accomplish multiple acquisition, transfer, and processing cycles under control of the signal processor device, without PC intervention. Bypassing the host bus and operating system can significantly improve system performance.



Typical Performance

(dB versus Frequency in MHz)



Other Performance Curves
To Be Determined

TEST METHOD

A filtered sine wave signal is applied to the channel 1 input. Test frequencies used are 1.0, 25.01, 95.0, 230.0, and 480 MHz. The digitizer clock setting is 1 GHz. The voltage range is 1.00V. Signal amplitude is set for 95% of full scale. Performance measurements are made using a 4096 point FFT with a Blackman-Harris window. Signatec uses the first 10 bins to represent the DC term, 9 bins centered around the peak for the fundamental signal power, 9 bins centered at twice the fundamental for the second harmonic and 9 bins centered at three times the fundamental for the third harmonic. All other bins are considered to be noise.

PDA1000 SPECIFICATIONS AND ORDERING INFORMATION

Input Signals
Analog Signal Input
External Trigger In
External Clock In, Clock Out, Trigger Out
External Connectors : 3 SMA

Digital Output[1]
Synchronized Trigger
ADC Clock Div 8
External Connectors : 1 SMA

Analog Input
Full Scale Volt. Ranges: 200mV, 333mV, 600mV, 1.00V, 1.80V, 3.00V p-p
Impedance : 50 ohms
Bandwidth : 500 MHz
Equivalent Noise : 0.5 lsb RMS (typical)
Coupling : AC or DC[2]

External Trigger
Trigger In
Impedance : 50 ohms / 1k ohms[2]
Trigger Level : ±250 mV @ 50 ohms, ±2.5 V @ 1k ohm
Adjustment Method : via 8 bit DAC
Bandwidth : 350 MHz @ 50 ohms, 10 MHz @ 1k ohms
Coupling : DC

External Clock
Clock In
Signal Type : sine or square wave
Impedance : 50 ohms to ground
Frequency : 200 MHz to 1 GHz
Amplitude : 100 mV p-p to 2.0 V p-p
Clock Out
Type : TBD
Max Frequency : 250 MHz
Suggested Load : 50 ohms
Amplitude : TBD

DC Offset Voltage
8 bit DAC, ±270 mV at ADC input

Digitizer
Voltage Range : ±250 mV full scale
Resolution : 8 bits
Linearity, Integral : ±0.5 lsb max.
Linearity, Differential : ±0.75 lsb max.
Aperture Jitter : < 0.5 pS typical
Internal Clock Rates : 1 GHz down to 976.6 kHz, in factors of 2
Internal Clock Accuracy: ± .01%

Trigger Modes
Post-Trigger : single start trigger fills active memory
Pre-Trigger : single trigger stops acquisition
Segmented : start trigger for each memory segment

Trigger Options
Pre-Trigger Samples : samples prior to trigger are stored; up to 32K samples
Delayed Trigger : delay from trigger to data storage; up to 512K digitizer clock samples

Memory
Active Size : Up to 256 Megasamples
Segment Size : Up to 128 Megasamples
Start Address Setting : Anywhere in memory
Segment Re-arm Time[4]: 150 nanoseconds
Addressing : DMA transfers from starting address
Memory Address (PC) : Plug and Play selected

I/O Addressing
PCI Controller Address: 64 bytes, Plug and Play selected
Control/Status Registers: 32 bytes, Plug and Play selected

Signatec Auxiliary Bus
Data Transfer Modes : Block or Packet
Data Transfer Rates : 500 MB/s max @ 64 bits
Data Direction : output only

Power Down Features
Off Mode : Board Deactivated; Power usage less than 350 mW
Power Down : Acquisition circuits deactivated; power reduced by 2/3
Thermal Shutdown : ADC temp. greater than 65 C deactivates power

Power Requirements
+12 : 100 mA max.
-12 : 10mA max.
+5 : 2.5A max. (acquisition) ; 0.7A max. (power down)
+3.3 : 3A max.

Absolute Maximum Ratings
Analog Inputs : ±5 volts
Trigger Input : ±5 volts
Clock Input : 5 volts peak to peak
Ambient Temperature : 0 to 50 C

PDA1000 Board
Part Number: PDA1000

SAB Cables
Refer to the "SAB Cable Assembly Ordering Guide" to select and order the appropriate cable assemblies.

Master-Slave Cables
Refer to the "PDA1000 Master/Slave Cable Ordering Guide" to select and order the appropriate cable assemblies.

Documentation & Accessories
The PDA1000 is supplied with a comprehensive operator's manual that thoroughly describes the operation of both the hardware and the software. Also supplied are two four-foot coaxial cables with BNC to SMA connectors. Extra cables may be purchased from Signatec. Supplied software disk includes DOS and WINDOWS function libraries for Borland and Microsoft C/C++, application programs and examples, and source code.

Customer Support
Customer Support and Software Updates can be obtained from the Signatec Web Site at www.signatec.com.

Product Warranty
All Signatec products carry a full 3-year warranty. During the warranty period, Signatec will repair or replace any defective product at no cost to the customer. This warranty does not cover customer misuse or abuse of the products or physical damage not reported within 15 days of the time of shipment by Signatec.

Notes:
1. Software selectable.
2. Switch selectable.
3. Jumper selectable.
4. In segmented mode, time from the end of a segment until a trigger will be accepted to begin another segment acquisition.

Signatec reserves the right to make changes in this specification at any time without notice. The information furnished herein is believed to be accurate, however no responsibility is assumed for its use.

Data Sheet Revision 1.00 - Date 05-16-2005

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