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Signatec FAST PRODUCTS
For an Impatient World

Product Information Sheet

PDA500

500 MHz Waveform Digitizer



FEATURES

- Bandwidth from DC-500 MHz
- 4 megabytes memory on board
- Memory expandable to 1 gigabyte or more
- 500 MB/s data transfer via SAB Interface
- 8-bit resolution
- PCI compatible board

APPLICATIONS

- Radar
- Mass Spectroscopy
- Mass Spectrometry - Time of Flight
- Communications
- Ultrasound
  Medical Diagnostics / Non Destructive Testing
- Laser Doppler Velocimetry
- High Speed Waveform Capture

OVERVIEW

The PDA500 is the state of the art in high speed waveform capturing systems. With an analog bandwidth of DC to 500 MHz and a 500 MHz digitizer with 8-bit resolution, waveform frequencies up to 500 MHz can be captured. The PDA500 is available with 4 megabytes of on-board memory.

The PDA500 has two input channels and a multiplexer to select one of the two channels as the digitization source. A digitally controlled attenuator allows the input voltage range to be adjusted in 2 dB steps from 200mV p-p to 3.0V p-p. This gives the PDA500 fourteen input voltage settings.

Provisions are included to connect up to four PDA500 boards in a Master/Slave configuration. This allows the clock and trigger signals from the Master to drive the Slave, allowing synchronized data samples on multiple boards. Master/Slave connections are via a 26-conductor ribbon cable at the top of the board.

The PDA500 incorporates version 3 of the Signatec Auxiliary Bus (SAB). This bus provides a high speed connection to other high speed products such as signal processors or data storage devices. Both block transfers and packetized data transfers are supported. Packetized data transfers can be very effective in maximizing the utilization of bus bandwidth in systems incorporating 3 or more devices on the bus. Sustained transfers of 500 MB/s are possible.

External clock and trigger connections are provided via SMA connectors on the back bracket. Either may be set by the user to function as an input or as an output. It is also possible to mechanize the two connections as a trigger in / trigger out combination. The output trigger is precisely synchronized to the start of data acquisition so that if used as a trigger to a pulsed system, such as for ultrasound, any trigger-to-clock jitter is completely eliminated from the data record.

The PDA500 is equipped with multiple acquisition and trigger modes. For single event acquisitions, the PDA500 is equipped with a single shot mode allowing pretrigger, normal, or delayed trigger storage. For multi-trigger acquisitions, segmented triggering is possible. Delayed and pretrigger features may also be used when acquiring segmented data.

HARDWARE DESCRIPTION

MECHANIZATION

The figure below shows the hardware mechanization for the PDA500. The input signal coupling may be selected as either DC or AC. The input amplifiers may be set for a gain of 0 dB or 12 dB. A software controlled multiplexer selects either channel 1 or channel 2 input as the signal source. A programmable attenuator may be set from 0 to 14 dB. Proper setting of the amplifier gain and attenuator value allows for a system gain of +12 dB to -14 dB in 2 dB steps. The full scale input voltage of the ADC is fixed at ±270 mV. The offset voltage DAC is used to position the ADC input voltage as needed by the user.

The ADC clock input may be selected as 500 MHz, 200 MHz, or external. In addition, a divide by 5 input to the ADC may be selected to internally divide down the ADC data output rate. The ADC output data rate may be further reduced in factors of 2 from 2 up to 128 via the output clock divider circuit.

The demultiplexer circuit widens the output data from 8 bits to 64 bits, so that at the maximum clock rate of 500 MHz, the output data rate is reduced to 62.5 MHz. This permits the use of fast CMOS static RAM ICs with an access time of 12 nanoseconds so that large amounts of memory may be attached.

OPERATING MODES

The PDA500 has 8 operating modes as follows: Off, Standby, Acquisition #1 (normal), Acquisition #2 (to SAB), Acquisition #3 (to PCI), Transfer #1 (to PC bus), Transfer #2 (to SAB), RAM write, and Ready.

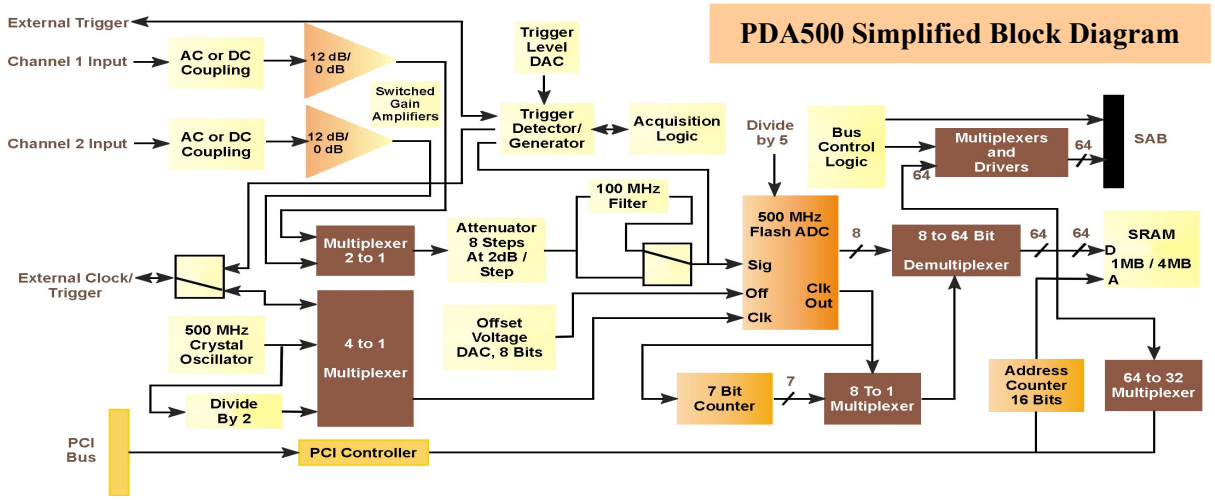
The Off mode powers down most of the circuitry on the PDA500 board to reduce power consumption and heat buildup. At system power-up, the board defaults to this mode. The Standby mode applies power to all circuitry except the data acquisition circuits. Acquisition mode applies power to all circuits. In addition to the explicit power down modes, the data acquisition circuits are automatically powered down in the data transfer modes.

Acquisition mode #1 stores data samples in the on-board signal memory to be transferred later to the PC. In Acquisition mode #2, data output is directly to the SAB. Acquisition mode #3 acquires data directly to the PCI bus to be stored in system memory. In this acquisition mode, the maximum sampling rate is limited by the ability to store the data samples in system memory.

Two triggering modes and two trigger methods are provided on the PDA500. The trigger modes are single shot and segmented modes. In the single shot mode, following the detection of a trigger signal, all active memory is filled. In the segmented mode, a separate trigger signal is required to successively fill each memory segment until all of the active memory is filled. The trigger method determines the relationship of the stored data samples to a trigger event. The trigger methods provided are pretrigger and delayed trigger. Pretrigger acquisitions allow a specified number of samples which occur prior to the trigger event to be stored in either trigger mode. Delayed trigger acquisitions allow a software programmable number of samples to be disregarded after the trigger event and before data storage begins in either trigger mode. The trigger source selection can be channel 1, channel 2, external or software.

PCI INTERFACE

The PDA500 is a 32-bit, 5 Volt PCI board that is "Plug and Play" compatible. Each PDA500 installed in a system can be uniquely identified by the board serial number which can be read from the board through the PCI bus. The control and monitoring registers of the PDA500 are accessed from the PCI bus with 32-bit I/O transfers. The PDA500 is capable of becoming a PCI Bus Master allowing data to be transferred using 32-bit burst direct memory access (DMA) transfers. The PDA500 is capable of transferring one 32-bit word on each PCI bus clock cycle, theoretically making it possible to transfer data at the maximum rate of the PCI bus. The actual transfer rate realized in a system will be less than this and is dependent upon the host system. Signal data can also be transferred using 32-bit memory operations via standard software functions.



SAB Interface

The Signatec Auxiliary Bus makes it possible to construct high-performance instrumentation systems using cost effective PC platforms. The PDA500 implements version 3 of the bus which supports both Block and Packetized data transfers. Both modes can sustain transfers of 500 megabytes per second. Packetized data transfers substantially increases bus bandwidth utilization in system applications involving multiple simultaneous transfers.

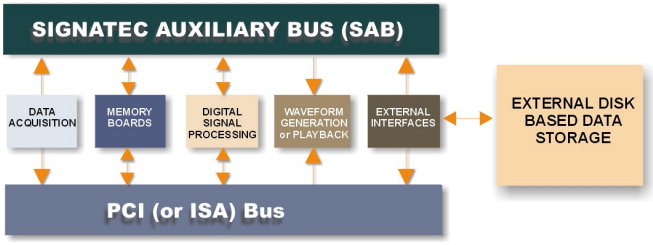
The SAB does not replace the host bus but augments it. An optimized application uses the SAB for time critical data movements and the host bus for less critical operations. Since both buses are in simultaneous operation, system throughput is maximized. Additionally, multiple SABs can be implemented in a single computer, further increasing available system data bandwidth.

Compatible System Components and Software

System Components

Signatec offers a range of products incorporating the SAB. These boards act as the modular building blocks for constructing high performance systems that mechanize a wide variety of applications. Figure 3 shows the present product groups available.

DSP Products can perform as a SAB Bus Controller that manages board operations and data flow on the bus. This allows an integrated acquisition system to accomplish multiple acquisition, transfer, and processing cycles without PC intervention, thereby maximizing system performance.



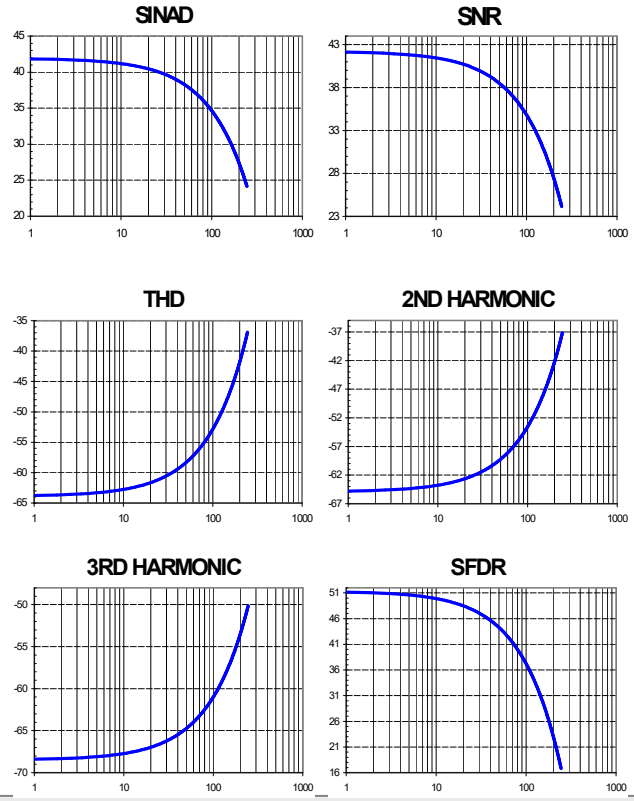
SAB and Supporting Products

Software

The PDA500 is supplied with device drivers for Windows95/98 and WindowsNT 3.51/4.0, and a library of C language functions, making it easy to create custom applications without writing extensive code. DOS and Windows based application programs are also supplied. These application programs can be used as stand-alone software to operate the board. Since the source code is also supplied, users can modify these programs to meet their specific needs, or cut and paste the source code into a larger application.

Typical Performance

(dB versus Frequency in MHz)



Definition of Terms

SINAD - Signal to Noise and Distortion: The ratio of the fundamental sinusoidal signal power to the total noise and distortion component power.

SNR - Signal to Noise Ratio: The ratio of the fundamental sinusoidal signal power to the noise power.

SECOND HARMONIC DISTORTION - The ratio of the power at twice the fundamental frequency to the power of the fundamental sinusoid.

THIRD HARMONIC DISTORTION - The ratio of the power at three times the fundamental frequency to the power of the fundamental sinusoid.

THD - Total Harmonic Distortion: The ratio of the total power of the second and third harmonics to the fundamental sinusoidal power.

SFDR - Spurious Free Dynamic Range: The ratio of the fundamental sinusoidal power to the power of the next highest spurious signal. Normally, the highest spurious signal is the second or third harmonic.

TEST METHOD

A filtered sine wave signal is applied to the channel 1 input. Test frequencies used are 1.0, 25.01, 95.0, 230.0, and 480 MHz. The digitizer clock setting is 500 MHz. The attenuator setting is 0dB. Signal amplitude is set for 95% of full scale. Performance measurements are made using a 4096 point FFT with a Blackman-Harris window. Signatec uses the first 10 bins to represent the DC term, 9 bins centered around the peak for the fundamental signal power, 9 bins centered at twice the fundamental for the second harmonic, and 9 bins centered at three times the fundamental for the third harmonic. All other bins are considered to be noise.

PDA500 ELECTRICAL SPECIFICATIONS AND ORDERING INFORMATION

SPECIFICATIONS

INPUT SIGNALS

Channel 1 Analog Input
Channel 2 Analog Input
External Trigger (in/out) [1]
External Clock (in/out) [1]
External Connectors : 4 SMA

ANALOG INPUTS

full scale voltage : 200 mV p-p to 3.0 V p-p[2]
impedance : 50 ohms
bandwidth : 100 Mhz or 500 MHz[1]
equivalent noise : 0.5 lsb RMS (typical)
coupling : AC or DC[1]

ANALOG MULTIPLEXER

switching speed : 30MHz

EXTERNAL TRIGGER[4]

impedance[6] : 50 ohms / 1k ohms[1]
trigger level[6] : ±250 mV @ 50 ohms, ±2.5 V @ 1k ohm
adjustment method[6] : via 8 bit DAC[2]
bandwidth[6] : 350 MHz @ 50 ohms, 10 MHz @ 1k ohms
coupling[6] : AC or DC[1]
output trigger[7] : ECL synchronous with data clock

EXTERNAL CLOCK[5]

signal type[6] : ECL logic or sine/square wave input
impedance[6] : 50 ohms to -2 V or ground[1]
frequency[6] : 50 MHz to 500 MHz[8]
amplitude[6] : 100 mV p-p to 2.0 V p-p
output clock[7] : TTL clock one-eighth digitizer frequency

ATTENUATOR

range : 0 to 26 dB
steps : 14, 2 dB per step
control : digital, 4 bits[2]

DC OFFSET VOLTAGE

8 bit DAC, ±270 mV at ADC input

DIGITIZER

voltage range : ±270 millivolts full scale
resolution : 8 bits
linearity, integral : ±0.5 lsb max.
linearity, differential : ±0.75 lsb max.
aperture width : 270 pS typical
aperture jitter : 2 pS typical
internal clock rates : 500 MHz to 781.25 kHz in factors of 2,
200 MHz to 312.5 kHz in factors of 2,
divide by 5 of all above frequencies
internal clock accuracy:±.01%

TRIGGER MODES

single shot : single start trigger fills active memory
segmented : start trigger for each memory segment

TRIGGER METHODS

Pretrigger : samples prior to trigger are stored
0 to 4k samples in steps of 64
Delayed Trigger : delay from trigger to data storage
0 to 65k digitizer clocks in steps of 8

MEMORY

Size : 4 megabytes
Start Address Setting[9] : 0 to memory size in steps of 8
End Address Setting[9] : 0 to memory size in steps of 32
segment re-arm time[10] : 150 nanoseconds
Addressing : via Memory Mapping or DMA
Memory Address (PC): Plug and Play selected

I/O ADDRESSING

PCI Controller Address :64 bytes, Plug and Play selected
Control/Status Registers :32 bytes, Plug and Play selected

SIGNATEC AUXILIARY BUS

data transfer modes : block
data transfer width : 64 bits or 32 bits
data transfer rates : 500 MB/s max in 64-bit; 250 MB/s max in 32-bit
data direction : output only

POWER DOWN FEATURES

Off Mode : Board Deactivated; Power usage less than 350 mW
Power Down : Deactivation of acquisition circuits reduces
power by 2/3
Thermal Shutdown : ADC temp. greater than 65°C deactivates power

POWER REQUIREMENTS

+12 : 1.5 Amps max. (normal operation)
190 mA max. (power down and off mode)
-12 : 10 mA max. (all modes)
+5 : 1.8 Amps max. (acquisition)
1.1 Amps max. (power down)
0.5 Amps max. (off mode)

ABSOLUTE MAXIMUM RATINGS

Analog Inputs : ±5 volts
Trigger Input : ±5 volts
Clock Input : 5 volts peak to peak
Ambient Temperature : 0 to 50°C

ORDERING INFORMATION

PART NUMBER

PDA500-4M 4 Megasample memory

SAB CABLES

Refer to the "SAB Cable Assembly Ordering Guide" to select and order the appropriate cable assemblies.

MASTER-SLAVE CABLES

The PDA500 is configured to operate as a Master or a Slave via solder jumpers on the board which can be set by Signatec. In order to operate in a Master/Slave configuration, a 26-pin ribbon cable is required to connect multiple boards. This cable is ordered using the basic part number PDA500MS-X where X is the total number of boards connected together. Master/Slave boards must occupy adjacent slots. The maximum number of boards to be connected is one master and three slaves. The part number for this cable is: PDA500MS-4.

DOCUMENTATION & ACCESSORIES

The PDA500 is supplied with a comprehensive operators' manual which thoroughly describes the operation of both the hardware and the software. Also supplied are two four foot coaxial cables with BNC to SMA connectors. Extra cables may be purchased from Signatec. Supplied software disks contain a DOS function library for Borland C, Windows 95/NT function libraries for Borland and Microsoft Visual C/C++, example programs, and all source code to libraries and examples.

CUSTOMER SUPPORT

Customer Support and Software Updates can be obtained from the Signatec web page at www.signatec.com, e-mail address techsupport@signatec.com, or by calling Signatec at (909) 734-3001.

PRODUCT WARRANTY

Most Signatec products carry a full three-year warranty. During the warranty period, Signatec will repair or replace any defective product at no cost to the customer. This warranty does not cover customer misuse or physical damage not reported within 15 days of the time of shipment by Signatec.

NOTES:

1. Selected via dip switch.
2. Software selectable.
3. Deleted.
4. External Trigger connector is selected as trigger input or an output trigger synchronized with start of acquisition using a dip switch
5. External Clock connector is selected as clock input or an output clock via a dip switch.
6. Applies to input only.
7. Applies to output only.
8. Internal divider is operational.
9. Active memory of acquisition is end address minus start address.
10. In segmented mode, time from the end of a segment until a trigger will be accepted to begin another segment acquisition.

Signatec reserves the right to make changes in this specification at any time without notice. The information furnished herein is believed to be accurate, however, no responsibility is assumed for its use.

Data Sheet Revision Date 1-25-02.

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