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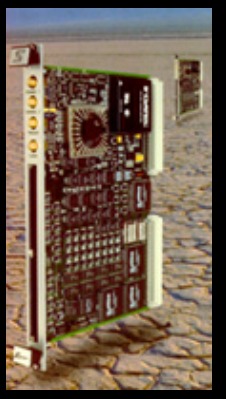
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Find the *DynamicSignals / Signatec VDA500* at our website: *Click HERE*

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VDA500

Download this Product Information Sheet



FEATURES

- VME Rev. C.1 compatible board (6U)
- Bandwidth from DC-500 MHz
- 8 bit resolution
- 256k bytes memory on board
- Memory expandable to 1 gigabyte or more
- 200 megabytes/sec data transfer rate over Signatec Auxiliary Bus(SAB)

APPLICATIONS

- Radar
- Mass Spectroscopy
- Mass Spectroscopy - Time of Flight
- Communications
- Ultrasound - Medical Diagnostics / Non Destructive Testing
- Laser Doppler Velocimetry
- High Speed Waveform Capture

Overview

The VDA500 is the state of the art in high speed waveform capturing systems. With an analog bandwidth of DC to 500 MHz and a 500 MHz digitizer with 8 bit resolution, waveform frequencies up to 500 MHz can be captured. The on board memory is 256k bytes in length.

The VDA500 incorporates the Signatec Auxiliary Bus (SAB) a high speed bus that allows for data transfers of up to 200 megabytes/sec. This allows for the high speed transfer of data to fast processor boards (such as Signatec's VSP20), large memory boards (such as Signatec's VMEM500) or other peripherals.

The VDA500 has two input channels and a multiplexer to select one of the two channels as the digitization source. Normally, signal data is collected from only one channel at a time. An interleaved data mode is available, however, to alternate the data values collected between the two input channels. Due to multiplexer switching speed limitations, in this mode the maximum digitization rate is limited to 50 MHz or 25 MHz per channel.
Provisions are included to connect two VDA500 boards in a Master/Slave configuration. Using the Master/Slave interconnect allows for synchronizing the data samples between two VDA500 boards. Master/Slave connections are made via a conductor ribbon cable using Signatec Auxiliary Bus

The output amplitude of the signal multiplexer may be digitally controlled by an attenuator which allows for adjusting the signal level to the ADC in 2 dB steps over a 26 dB range.

The VDA500 supports single shot, segmented, and pretrigger triggering modes and features various power down modes to minimize power dissipation. The on board crystal clock circuitry allows for selecting 1 of 28 different digitization frequencies from 312.5 kHz to 500 MHz.

External clock and trigger inputs are provided via SMA connectors on the front panel of the VDA500 board.

Hardware Description

Mechanization

The figure below shows the hardware mechanization for the VDA500. The input signal coupling may be selected as either DC or AC. The input amplifiers may be set for a gain of 0 dB or 12 dB. A software controlled multiplexer selects either channel 1 or channel 2 input as the signal source. A programmable attenuator may be set from 0 to 14 dB. Proper setting of the amplifier gain and attenuator value allows for a system gain of +12 dB to -14 dB in 2 dB steps. The full scale input voltage of the ADC is fixed at ±270 mV. The offset voltage DAC is used to position the ADC input voltage as needed by the user.

The ADC clock input may be selected as 500 MHz, 200 MHz or external. In addition a divide by 5 input to the ADC may be selected to internally divide down the ADC data output rate. The ADC output data rate may be further reduced in factors of 2 from 2 up to 128 via the output clock divider circuit.

The demultiplexer circuit widens the output data from 8 bits to 64 bits so that at the maximum clock rate of 500 MHz the output data rate is reduced to 62.5 MHz. This permits the use of fast CMOS static RAM ICs with an access time of 12 nanoseconds so that large amounts of memory may be attached.

Operating Modes

The VDA500 has 8 operating modes as follows: Off, Standby, Ready, Acquisition #1 (normal), Acquisition #2 (to SAB), Data Transfer #1 (to VME bus), Data Transfer #2 (to SAB), RAM write.

The Off mode powers down most of the circuitry on the VDA500 board to reduce power consumption and heat buildup. At system power up the board defaults to this mode. The Standby mode applies power to all circuitry except the data acquisition circuits. The ready mode applies power to all circuits. In addition to the explicit power down modes, the data acquisition circuits are automatically powered down in the data transfer modes.

In data acquisition mode #2 data is output directly to the SAB. The data acquisition clock is restricted to a maximum of 200 Mhz in this mode. In either data acquisition mode three triggering modes are available: single shot, segmented, or pretrigger. In the single shot mode, following the detection of a trigger signal, all of the active memory is filled. In the segmented mode a separate trigger signal is required to successively fill each memory segment until all of the active memory is filled. In the pretrigger mode the board is armed and continuously fills the active memory until a stop trigger is detected, after which a programmed number of post trigger samples are taken before acquisition is terminated. The pretrigger mode may be used to see signal information both before and after the trigger signal.

Memory Addressing

For data transfer over the VME bus, the memory contents of the VDA500 are accessable via a 16 megabyte memory block in the VME system's 4 gigabyte address space. Dip switches may be set to select 1 of 256 memory block addresses.

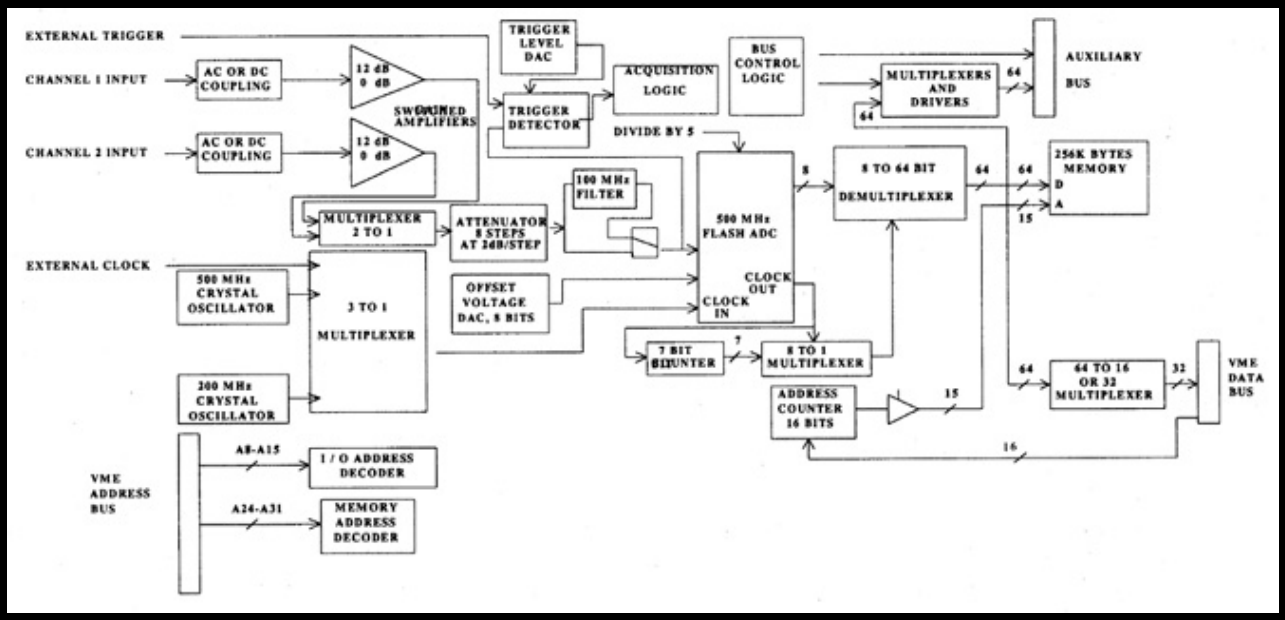
The amount of memory that is activated for data acquisition may be set from 2 kilobytes to 1 gigabyte in factors of 2.

This allows for operation with up to 4 VMEM500 memory boards. A memory full detector monitors the appropriate address counter bit for a low to high transition. When a full condition is detected, further data storage is inhibited and a flag is set which may be read by the PC or software selected to cause a PC interrupt.

Power Control and Thermal Management

The VDA500 implements automatic power control features and is equipped with a fanned heatsink to prevent thermal problems. A temperature monitor is included to cause an electrical shutdown if the ADC overheats due to fan failure or air flow restriction.

VDA500 SIMPLIFIED BLOCK DIAGRAM



Software, System, and Performance Details

Software

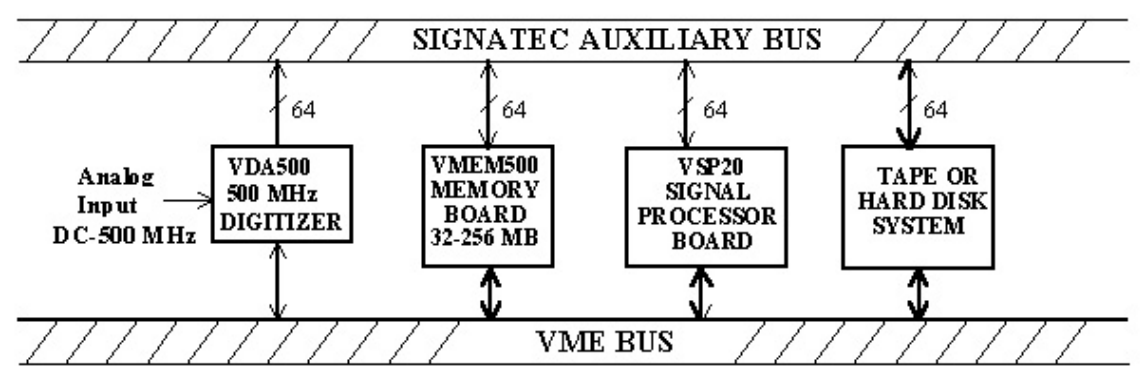
Libraries of C/C++ language functions are supplied with the VDA500 which make it easy to control its operation. The functions were compiled into libraries using Borland's C/C++ 4.0 and Microsoft C/C++ 1.52. A Windows Dynamic Linked Library (DLL) is also provided. The DLL has been tested with the C/C++ compilers listed above and with Microsoft Visual Basic. Also included are extensive examples of how to use the functions in C programs, as well as Windows application programs using the three compilers listed above.

Watch for future support for the VDA500 using Maestro, Signatec's graphical code generating program. With Maestro a complete application program can be created much more simply than using conventional techniques. See the Maestro product information sheet for more details.
System Capabilities

The VDA500 implements the Signatec Auxiliary Bus (SAB), a 64 bit high speed data bus. The SAB allows the implementation of very high speed data capture, processing and storage systems. Shown in the figure below are the elements of such a system. The VMEM500 board stores up to 256 megabytes of signal information and up to 4 boards may be connected to a single VDA500 to achieve a memory capacity of 1 Gigabyte. Mass storage systems using the SAB are currently under development. Check with Signatec for availability.

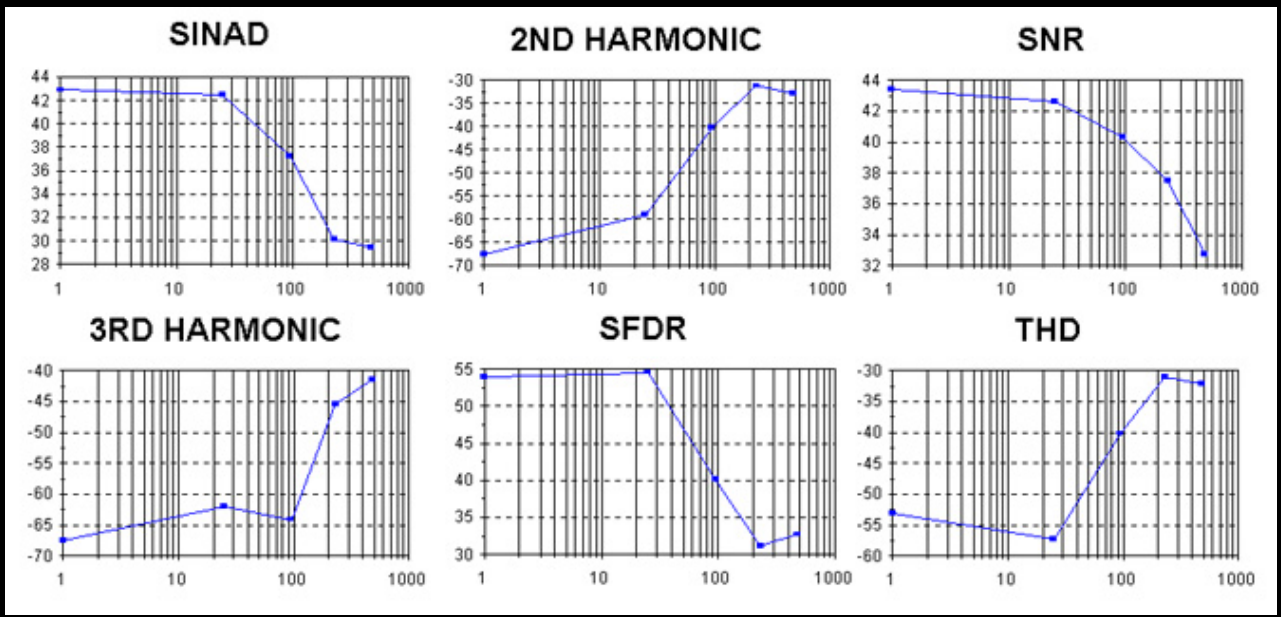
Signatec's VSP20 DSP board offers high performance processing and transfers data at the full SAB bandwidth. Devices connected to the SAB, including the VDA500 and SP20, may communicate via SAB interrupt and control lines. This allows the boards to accomplish multiple acquisition, transfer, and processing cycles under control of the VSP20 independent of any other VME bus activity, thereby maximizing system performance. Check for availability of VMEM500 and VSP20.

HIGH PERFORMANCE WAVEFORM CAPTURE SYSTEM



TYPICAL PERFORMANCE

(dB versus Frequency in MHz)



DEFINITION OF TERMS

SINAD - Signal to Noise and Distortion: The ratio of the fundamental sinusoidal signal power to the total noise and distortion component power.
SNR - Signal to Noise Ratio: The ratio of the fundamental sinusoidal signal power to the noise power.
THD - Total Harmonic Distortion: The ratio of the total power of the second and third harmonics to the fundamental sinusoidal power.
SECOND HARMONIC DISTORTION - The ratio of the power at twice the fundamental frequency to the power of the fundamental sinusoid.
THIRD HARMONIC DISTORTION - The ratio of the power at three times the fundamental frequency to the power of

the fundamental sinusoid.
SFDR - Spurious Free Dynamic Range: The ratio of the fundamental sinusoidal power to the power of the next highest spurious signal. Normally the highest spurious signal is the second or third harmonic.

TEST METHOD

A filtered sine wave signal is applied to the channel 1 input. Test frequencies used are 1.0, 25.0, 95.0, 230.0, and 480 MHz. The digitizer clock setting is 500 MHz. The attenuator setting is 0dB. Signal amplitude is set for 95% of full scale. Performance measurements are made using a 4096 point FFT with a Blackman-Harris window. Signatec uses the first 10 bins to represent the dc term, 9 bins centered around the peak for the fundamental signal power, 9 bins centered at twice the fundamental for the second harmonic and 9 bins centered at three times the fundamental for the third harmonic. All other bins are considered to be noise.

VDA500 Electrical Specifications and Ordering Information

Specifications

Input Signals

```
Channel 1 Analog Input
Channel 2 Analog Input
External Trigger
External Clock
External Connectors     : 4 SMA, 2 100 pin (SAB)
```

Analog Inputs

```
full scale voltage      : 200 mV p-p to 3.0 V p-p
impedance               : 50 ohms
bandwidth               : 100 MHz or 500 MHz[1]
equivalent noise        : 0.5 lsb RMS (typical)
coupling                : AC or DC[2]
```

Analog Multiplexer

```
switching speed         : 20 nanoseconds[3]
```

External Trigger

```
impedance               : 50 ohms / 1k ohms[3a]
trigger level           : ±250 mV @ 50 ohms, ±2.5 V @ 1k ohm
adjustment method       : via 8 bit DAC[2]
bandwidth               : 350 MHz @ 50 ohms, 10 MHz @ 1k ohms
coupling                : AC or DC[2]
```

External Clock

```
signal type             : ECL logic or sine/square wave input
impedance               : 50 ohms to -2 V or ground[3a]
frequency               : 50 MHz to 500 MHz[4]
amplitude               : 100 mV p-p to 2.0 V p-p
```

Attenuator

range	: 0 to 26 dB
steps	: 14, 2 dB per step
control	: digital, 4 bits[2]

DC Offset Voltage

8 bit DAC, ±270 mV at ADC input

Digitizer

voltage range	: ±270 millivolts full scale
resolution	: 8 bits
linearity, integral	: ±0.5 lsb max.
linearity, differential	: ±0.75 lsb max.
aperture width	: 270 pS typical
aperture jitter	: 2 pS typical
internal clock rates	: 500 Mhz to 3.90 MHz in factors of 2, 200 MHz to 1.56 MHz in factors of 2, divide by 5 of all above frequencies

Trigger Modes

single shot	: single start trigger fills active memory
segmented	: start trigger required for each memory segment until active memory is filled
pretrigger	: single trigger stops sampling after post trigger samples are collected

Memory

on board	: 256 kilobytes
expansion	: 1 Gigabyte or more using SAB[6]
memory settings[7]	: 2k bytes to 1 Gigabyte in factors of 2
segment sizes[8]	: 64 bytes to 64k bytes in factors of 2
post trigger samples[9]	: 256,1k,4k,16k,32k,64k,128k,256k
Addressing	: 16 megabyte block of SP32 memory space[1]
I/0 Addressing	: 256 sequential I/O addresses[1]

Auxiliary Bus[10]

data transfer modes	: 64 bit burst, 32 bit burst, 16 bit handshake
data transfer rates	: 200 MB/s max in burst mode (25 Mhz clock) 20 MB/s max in 16 bit mode
data direction	: output only

Power Down Features

Off Mode	: Board Deactivated; Power less than 350 mW
Power Down	: Deactivation of acquisition circuits reduces power by 2/3
Thermal Shutdown	: ADC temp. greater than 65°C deactivates power

Power Requirements

+12	: 1.1 Amps max. (normal operation) 15 mAmp max. (power down and off mode)
-12	: 10 mAmps max. (all modes)
+5	: 2.2 Amps max. (normal operation) 0.5 Amps max. (power down) 100 mA max. (off mode)

Absolute Maximum Ratings

Analog Inputs	: ±5 volts
Trigger Input	: ±5 volts

```
Clock Input             : 5 volts peak to peak
Ambient Temperature     : 0 to 50°C
```

Ordering Information

VDA500 Board

Specify either VDA500 or VDA500-S. VDA500 is the default configuration. VDA500-S indicates board will be used as a slave board coupled to a master VDA500 board. Slave boards have solder jumpers which must be set at the factory.

SAB Cables

Refer to the "SAB Cable Assembly Ordering Guide" to select and order the appropriate cable assemblies.

Master-Slave Cables

A master-slave connection cable is supplied free of charge with VDA500-S boards.

Documentation & Accessories

The VDA500 is supplied with a comprehensive operators manual which thoroughly describes the operation of both the hardware and the software. Also supplied are two four foot coaxial cables with BNC to SMA connectors. Extra cables may be purchased from Signatec. Supplied software disk includes DOS and WINDOWS function libraries for Borland and Microsoft C/C++, application programs and examples, and source code.

Customer Support

Customer Support and Software Updates can be obtained by calling Signatec at (909) 734-3001, or BBS at (909) 734-7491.

Product Warranty

All Signatec products carry a full 3 year warranty. During the warranty period, Signatec will repair or replace any defective product at no cost to the customer. This warranty does not cover physical damage not reported within 15 days of the time of shipment by Signatec.

Notes:

1. Selected via dip switch.
2. Software selectable.
3. Can support 25 MHz data acquisition on 2 channels in Interleaved Data Mode.
3a. Jumper selectable.
4. Internal dividers are operational.
5. Maximum limit for full speed operation (500 MHz).
6. 1 gigabyte is the maximum amount of memory for which the on board memory full detector is functional. Using off board memory full detection there is no limit to the amount of memory which may be connected using the SAB. This port limits the maximum acquisition rate to 200 MHz.

7. Memory full detector settings.
8. Applicable to segmented mode only.
9. Number of samples after stop trigger in pretrigger samples mode.
10. Signatec's Auxiliary Bus (SAB) is a double wide implementation of Data Translation's DT Connect III bus. A complete specification for the SAB is available via Signatec's BBS, or phone direct for hard copy.
11. DT-Connect III is a trademark of Data Translation, Inc

Signatec reserves the right to make changes in this specification at any time without notice. The information furnished herein is believed to be accurate, however no responsibility is assumed for its use.

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