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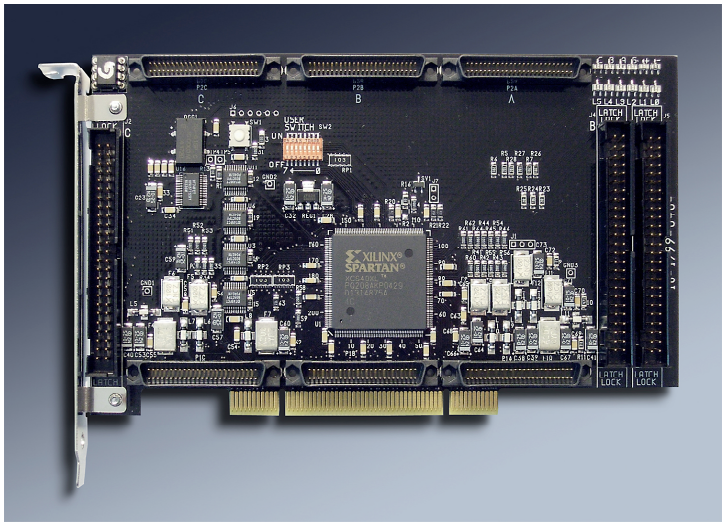
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User Manual

PCI3IP

PCI 3 Slot IP Module Carrier



Manual Revision J
Corresponding Hardware: Revision D
Corresponding Firmware Revision J
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PCI3IP
PCI based IP Compatible Carrier

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Table of Contents

PRODUCT DESCRIPTION 5

THEORY OF OPERATION 9

ADDRESS MAP 12

PROGRAMMING 13

Register Definitions 14
pci3ip_intreg0 14
pci3ip_intreg1 16
pci3ip_intreg2 17
pci3ip_alt_regA-C 18

APPLICATIONS GUIDE 20

Interfacing 20

Construction and Reliability 20

Thermal Considerations 22

WARRANTY AND REPAIR 22

Service Policy 23
Out of Warranty Repairs 23

For Service Contact: 23

SPECIFICATIONS 24

ORDER INFORMATION 25

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List of Figures

FIGURE 1	PCI3IP ADDRESS MAP	12
FIGURE 2	PCI3IP CONTROL PORT	14
FIGURE 3	PCI3IP INTERRUPT STATUS PORT	16
FIGURE 4	PCI3IP USER SWITCH PORT	17
FIGURE 5	PCI3IP ALTERNATE CONTROL REGISTER PORTS	18
FIGURE 6	PCI3IP CONNECTOR REFERENCE	26

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Product Description

IndustryPack® Modules are an important part of solutions for Embedded situations. Rugged, Small, light .. just right for many applications. IndustryPack® Modules require a “carrier” in most cases to adapt them to the system. Dynamic Engineering has carrier solutions for a variety of formats. The PCI3IP is designed to support PC computer based solutions.

PCI3IP is part of the IP Compatible family of modular I/O components. The PCI3IP provides three IndustryPack® module sites in one PCI slot.

PCI3IP is supported with Windows® compliant [WDM32] drivers for XP and 2000. The drivers come with a generic IP driver to allow use with “unknown” IP’s – IP’s that do not have a driver designed yet. For example, third party IP’s.

The PCI accesses are handled by the PCI core. The IndustryPack® interface is controlled by the IP core. All of the logic is in VHDL making adaptations to user requirements reasonable to do.

Dynamic Engineering has made several updates to add new – user requested – features to this design and welcomes more new ideas for implementation. Dynamic Engineering makes every effort to keep backward software compatibility when new features are implemented. Set all unused bits to “0” when accessing to remain compatible with new features as they arise. “0” will correspond to the “old way” and “1” to enabling the new feature.

The PCI3IP design is flexible supporting each of the slot options with slot specific registers and independent operation.

ID, IO, INT, and MEM access types are supported for read and write cycles. The full 8 Mbytes of address space is allocated to each of the MEM spaces. A smaller memory footprint “mini map” version is available with a smaller MEM Space.

The PCI bus is 32 bits wide and most industry packs are 16 bit devices. Byte, word, and long word accesses are supported. Bytes can be to any address. Word accesses need to be word aligned. Long word accesses need to be long word aligned. Each of the access types has a one-to-one correspondence to the hardware. There are no "extra" accesses with the PCI3IP design.

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A long word access will automatically be converted into two back-to-back IP accesses with the address incrementing between cycles unless the increment disable function is selected (see control register description). For a read, one 32-bit data will be returned. For example a long word read to the ID space would yield 0xff50ff49 for many boards as the "0" location has $49 and the next address has $50. The long word mode happens automatically when all 4 of the byte lane enables are detected asserted. The overall throughput is greatly enhanced with this mode of operation.

A new addition to the design of the PCI3IP is to tag all accesses from the PCI bus. IP Modules can take longer than the PCI response specification leading to the use of retry cycles on the PCI bus. In a single CPU system the retry accesses are done serially. The current IP access will be the correct one to respond to the retry access. In a multi-cpu system it is possible to get out of sequence accesses, and potentially have the IP response sent to the wrong retry access. By storing the PCI parameters for the IP access and then only responding to the correct retry cycle multiprocessor cross contamination is avoided. This feature is new with the revision J PROM. Revision J PROM's can be obtained from Dynamic Engineering should you need to upgrade previously fielded HW for use in multiprocessor systems.

PCI3IP has a watchdog timer function, which completes the IP access if the IP does not respond within 7.6 uS. The watchdog timer has a status bit and an optional interrupt output.

Each slot is programmable for 8 or 32 MHz. operation. The control register has separate bits for slot A, B, C and state-machine. The state machine speed defines the speed between cycles. It is recommended to use the 32 MHz speed when your IP Module supports the higher rate. Shorter PCI access cycle times result and less traffic on the PCI bus, plus higher rates of execution for the control program.

PCI3IP supports interrupts from each slot with separate mask bits. Two interrupts from each of the three slots. In addition, an interrupt force bit is supplied to aid in software development. The masked interrupts are tied together and connected to INTA on the PCI bus.

PCI3IP has LED's for power and user functions. The three voltages from slot A are connected to three LED's. An additional 6 LED's are supplied which are controlled via the control register for user defined purposes.

An 8 bit "dip switch" is provided on the PCI3IP. The switch configuration is

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readable via a register. The switch is for user defined purposes. We envision the switch being used for software configuration control or test purposes. The Dynamic Engineering driver supports using the switch for IP Module identification.

The PCI Bus is enumerated at each power up cycle. The address range for a particular PCI3IP / IP Module combination can change when changes are made to the system. By using the switch on the PCI3IP the particular carrier can be identified if there are more than 1 in the system. Each IP is further identified by slot for positive identification. It can be important to “know” which external device you are reading or controlling.

The ID is stored as a number on the IP module in a register designed for this purpose or reusing a register without side affects. The IP driver when it starts up reads the information and has it available in system memory for application access. With a dedicated register the information will remain after application use. With a double use register the information will be overwritten by the application. In either case the information is available from the IP Module Driver.

The location of the register and offset for the bits is stored into the “INF” file for the carrier driver. IP Modules have updated INF files stored along with the IP Module driver to allow updating of the version that came with the carrier to handle situations where the IP Module was developed more recently than the Carrier driver.

Drivers can be developed for third party products and integrated into the auto detecting, marking and loading system. Alternatively the “generic” IP driver can be used to access third party IP Modules without a specific driver. The Generic IP Module driver is supplied with the Carrier driver.

The reset switch provided can be used to reset the IP devices without affecting the PCI bus. Power-on, PCI reset, and the control register reset bit also cause the IP Reset to be activated. The reset is controlled to be synchronous to the 8 MHz. clock. Alternatively, in development, the IP-Debug-Bus card also has a reset switch, which allows for individual slot resets.

The IO are routed from the IP Module IO connector to individual 50 pin headers. The headers are suitable for ribbon cable or individual wire type connectors. The HDRterm50 is a 50 in breakout connector that maps the 50 pin ribbon connector to 50 screw terminals for a neat, robust cabling system.
http://www.dyneng.com/HDRterm50.html

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The headers are available with or without ejectors. Please note the default is no ejectors to retain PCI compliance for height on the component side of the card.

PCI3IP conforms to the VITA standard for IndustryPack Carriers. This guarantees compatibility with multiple IndustryPack compatible modules.

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Theory of Operation

PCI3IP is used to act as a bridge from PCI to IP bus specifications. The PCI bus will be the master with the IP's accessed for read or write cycles.

The FPGA on the PCI3IP interfaces with the PCI interface and converts to the IP bus interface. The PCI bus provides multiplexed address and data plus control lines. The data is separated from the address and the control lines decoded to provide the inputs to the IP Interface state machines. The address is tested to determine which slot the access belongs to and which type of access. The IP strobes are generated. When acknowledge is detected to be asserted the cycle is terminated back to the host. The PCI bus will see a retry mode while the access is taking place and "disconnect with data" when the cycle is completed.

The disconnect with data state is delayed until the IP module acknowledges and the correct retry is received. With revision J and later PROM's the retry access type is tested to match the current IP access. After acknowledge is received from the IP, incorrect retry cycles are "retry'd" until the correct cycle type is received. A counter is used to insure a lock-out condition can't happen. After 256 retry cycles that do not match the correct access the hardware [PCI3IP] assumes a lockout condition and restarts. Restarting causes the overriding request to become the current access and complete. The original access will then be recaptured and completed.

For non multi-processor implementations this is not an issue. For multiprocessor implementations that prioritize one access type over another – interrupts for example – it can be an issue. It is recommended to use the board level masks to disable interrupts within the interrupt service routine, and to release the priority "lower the mask" so the original cycle can complete first. Using the local [PCI3IP] registers to mask off the interrupt will allow the request to be removed without introducing a new IP access at a higher priority.

Each IP has 2 interrupts each of which is routed to the FPGA. Individual masks are used before combining to create the board level interrupt. Status is provided to determine the active interrupt sources.

The IP Module has Interrupt, ID, IO and Memory cycle types defined. The FPGA uses the stored cycle captured from the PCI bus to generate the appropriate cycle type to interact with the IP Module. The full IP Module Memory space is allocated for each IP module. A mini-map version of the design is available for

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applications with PCI memory space limitations. The CBE lines on the PCI bus are encoded with the Byte lane information during part of the PCI access. The byte lanes active will determine the size and address at the IP Module.

The PCI bus is 32 bits wide. The IP Module bus is 16 bits wide. Byte and word accesses are possible to the IP Modules on the PCI3IP. When LW accesses are attempted they are automatically broken into 2 accesses and both completed before acknowledging back to the PCI bus.

IP Modules can be operated at 8 or 32 MHz. Some IP Modules are restricted to 8 MHz only and some can do either frequency. It is recommended to use the highest frequency the IP Module is rated for. The PCI accesses will be shorter with the 32 MHz rate. Each slot on the PCI3IP is individually programmable to 8 or 32 MHz. 8 MHz is the default rate to allow all modules to operate in the default state.

Feature List

- 3 IP compatible slots
- 8 or 32 MHz operation in each slot independently
- byte, word, long word access
- Incrementing or static access to each IP slot from long word access
- Bus error abort response
- 1:1 50 pin headers
- IP Reset Switch
- 8 position "DIP Switch"
- 6 User LED's
- 3 Power LED's
- Fused Filtered Power with resettable fuses in each slot.
- Continued development with a "PROM" program
- SW option to use style slot register definitions or original PCI3IP design
- Slot-specific bus error latched status bit in the above slot registers
- Windows XP/2000 driver
- Linux driver.

We are adding new drivers for various products to our product line. All of the IP drivers added will work with any of our carrier designs. If you develop a driver for one of our products or a third party IP to work with our carrier and are willing to allow others to use it we will add it to the web site as a free of charge download and, if desired, give credit to the author.

As Dynamic Engineering adds features to the hardware we will update the

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PCI3IP page on the Dynamic Engineering website. If you want some of the new features, and have already purchased hardware, we will support you with a PROM update. We will ship a new PROM with the updated program to you for shipping plus $25 per PROM. If you are interested please send a PO with shipping instructions, the serial numbers of the boards to upgrade and the programming charge.

The basic PCI identifying information will not change with the updates. The revision field will to allow configuration control. Current revision is 0x0A.

Firmware Revision Table

A Initial Release
B Alter timing to accommodate non-compliant IP modules.
C Add 32 bit access feature
D Add bus error timer feature
E Update 32 bit access to allow static and auto-incremented address behavior
F Add separated registers for slots A,B,C and retain default of unified control register
G Add slot-specific bus error latched status in the separated registers. Add a force interrupt bit and IP interrupt status bits in the slot control register. Also change PCI class code to PCI bridge - subclass other.
H, I developmental control
J Multiprocessor capability added

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Address Map

Function	Offset	description
// PCI relative addresses //		
#define pci3ip_intreg_0	0x00000000	base cntl reg
#define pci3ip_intreg_1	0x00001000	interrupt request read back
#define pci3ip_intreg_2	0x00002000	read back of switch
#define pci3ip_alt_reg_A	0x00003000	Alternate control reg Slot A
#define pci3ip_alt_reg_B	0x00004000	Alternate control reg Slot B
#define pci3ip_alt_reg_C	0x00005000	Alternate control reg Slot C
// control register internal to Xilinx part. clock selection, interrupt enable and set, IPACK size //		
#define pci3ip_ida_st	0x50000	start address slot A ID space
#define pci3ip_idb_st	0x60000	start address slot B ID space
#define pci3ip_idc_st	0x70000	start address slot C ID space
#define pci3ip_ioa_st	0x90000	start address slot A IO space
#define pci3ip_iob_st	0xa0000	start address slot B IO space
#define pci3ip_ioc_st	0xb0000	start address slot C IO space
#define pci3ip_inta_st	0xd0000	start address slot A INT space
#define pci3ip_intb_st	0xe0000	start address slot B INT space
#define pci3ip_intc_st	0xf0000	start address slot C INT space
#define pci3ip_mema_st	0x00800000	start address slot A MEM space
#define pci3ip_mema_en	0x00ffffff	end address slot A MEM space
#define pci3ip_memb_st	0x01000000	start address slot B MEM space
#define pci3ip_memb_en	0x017fffff	end address slot B MEM space
#define pci3ip_memc_st	0x01800000	start address slot C MEM space
#define pci3ip_memc_en	0x01ffffff	end address slot C MEM space

FIGURE 1 PCI3IP ADDRESS MAP

The address map provided is for the local decoding performed within PCI3IP. The addresses are all offsets from a base address, which, along with the interrupt level, is provided by the host in which the PCI3IP is installed.

The host system will search the PCI bus to find the assets installed during power-on initialization. The VendorId = 0x10EE and the CardId = 0x0003 for the PCI3IP. Interrupts are requested by the configuration space.

Once the initialization process has occurred and the system has assigned an address range to the PCI3IP card, the software will need to determine what the address space is. We refer to this address as the base address. The Base

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Control register is located at this address and all others are offsets relative to this address. The first time through it is handy to use a PCI viewing tool to see the address space and interrupt assigned to the PCI3IP. The revision of the PROM is also shown with most tools.

The next step is to initialize the PCI3IP. The main control register is written to for clock selection, and interrupt mask. The default of no interrupts enabled and 8 MHz. operation will be valid in many cases.

For new software development it is recommended to use the channel control registers. The originial base control register is provided for legacy support.

Programming

Dynamic Engineering recommends using the PCI3IP Windows® or Linux drivers. The drivers will handle the system resources and provide a stable platform for your IP driver to work with. The Parent/Child driver combination is designed to provide plug-n-play operation with automatic loading of the required drivers and automatic selection of the generic driver if a matching IP driver is not found.

Each Dynamic Engineering Carrier has a unique “parent” driver to support it. Each of the drivers have been carefully designed to provide a consistent interface to the IP drivers. The consistency makes the IP driver completely portable between different carriers and different architectures. For example you can develop in your desktop PC and then port to your cPCI system without having to redo the IP driver.

Should you need to support a different OS or just want to do your own please refer to the memory map and register map information. All of the details needed to program the card are covered in those sections. Please feel free to send any questions to engineering@dyneng.com.

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Register Definitions

pci3ip_intreg0

[$00 Main Control Register Port read/write]

CONTROL REGISTER 0	
DATA BIT	**DESCRIPTION**
31	Reset 1 = reset IPs 0 = normal
30	spare
29	LED5 1 = ON 0 = OFF
28	LED4
27	LED3
26	LED2
25	LED1
24	LED0
23	spare
22	spare
21	Bus Error Int/Status Clear
20	Bus Error Int En
19	Alternate Register set selection
18	RES
17	High Word Access C
16	Increment Disable C
15	High Word Access B
14	Increment Disable B
13	High Word Access A
12	Increment Disable A
11	INT FORCE 1 = FORCE 0 = NORMAL
10	INT EN C1 1 = ENABLED 0 = DISABLED
9	INT EN C0
8	INT EN B1
7	INT EN B0
6	INT EN A1
5	INT EN A0
4	SPARE
3	CLK SEL DEFAULT 1 = 32 0 = 8
2	CLK SEL C
1	CLK SEL B
0	CLK SEL A

FIGURE 2 PCI3IP CONTROL PORT

Reset when set causes a reset to the IP slots. Reset is active as long as the Reset signal is asserted.

LED5-0 are the user LED's situated just below the power status LED's near Slot A. Each LED can be activated by setting the corresponding data bit and

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deactivated by clearing the same bit.

Spare means unused and unplanned

RES means unused and planned for future enhancements

INT FORCE will when set cause INTA on the PCI bus to be asserted. This bit can be useful for software debugging. Set this to simulate an IP interrupt when the hardware is not available.

CLK SEL Default is set to cause the statemachine for the IP interface to operate at 32 MHz. when not accessing IP hardware. 0 sets the default speed to 8 MHz.

Bus Error Int En when ‘1’ allows the bus error detection circuit to cause an interrupt to the host when a Bus Error is detected. The status is available on the Interrupt status register. When ‘0’ the status is still valid but no interrupt is generated when a bus error is detected. The bus error is detected when an access to one of the 3 IP slots is not responded to by IP hardware within the time-out period of approximately 7.3 uS. The bus error circuit is always enabled and automatically responds as if the IP had responded. The data read will typically be $FF if the IP is not driving the bus for a bus error read. For a bus error write the write should be assumed to not have taken place. The host will not know that the bus error has taken place unless the host checks the status. The interrupt can provide a prompt to check the status during operation. During initialization if the software is checking to “see” what is installed or what address range is valid on an IP then the status can be polled to see if the IP responded.

Bus Error Status / INT Clear when ‘1’ will clear the status bit and interrupt request [if enabled]. The Clear bit needs to be reset to ‘0’ to be able to capture the next Bus Error. The bus error timer hardware operates independent of clearing the status and will continue to monitor and intercede whether the status is read or cleared.

Please note that the Alternate Register Selection bit affects the following bit definitions. When ‘0’ the base register definitions are used. When ‘1’ the separated register definitions are used.

CLK SEL A,B,C are used to select the slot clock speed.
1 = 32 MHz. 0 = 8 MHz. PLL used to generate and low skew drivers to allow switching the clock speed on-the-fly.

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Increment Disable A,B,C, when ‘1’, turns off the address increment, for the respective slot, that normally occurs between 16-bit IP cycles when a 32-bit PCI access is performed. This is useful if, for instance, a FIFO is mapped to a single IP address since it allows double IP accesses to the same address with a single PCI transfer. All types of access are affected (i.e. MEM, IO, INT, and ID). Only 32 bit accesses are affected.

High Word Access A,B,C controls which 16-bit word is accessed when the Increment Disable is asserted. When ‘0’ the lower word is accessed twice, when ‘1’ the upper word is accessed twice. This bit only has an effect when the Increment Disable bit is ‘1’. For correct functioning, make sure the PCI access is on a long-word boundary.

INT EN A0..C1 individual masks for the 2 interrupts from each of the three slots. 0 corresponds to INT0 and 1 corresponds to INT1.

pci3ip_intreg1

[$1000 pci3ip interrupt register read only]

CONTROL REGISTER 1

DATA BIT	DESCRIPTION
31-15	unused
14	Bus Error 1= occurred 0 = none
13	UNMASKED C1
12	UNMASKED C0
11	UNMASKED B1
10	UNMASKED B0
9	UNMASKED A1
8	UNMASKED A0 1 = SET 0 = NOT SET
7	INTRN 1 = SET, 0 = NOT SET
6	INT FORCE
5	MASKED C1
4	MASKED C0
3	MASKED B1
2	MASKED B0
1	MASKED A1
0	MASKED A0 1 = SET 0 = NOT SET

FIGURE 3 PCI3IP INTERRUPT STATUS PORT

The interrupt requests from each of the IP slots are available as status from this port. The interrupt requests are inverted to make them active high for software usability. The requests are available in a masked and unmasked form to allow

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polling with the PCI interrupt masked off. When an interrupt is detected this register should be accessed to determine the source or sources and then appropriate action take to clear the interrupt at the IP or clear the mask on pci3ip_intreg0.

The PCI3IP provides direct access to the interrupt space. If the IP causing the interrupt requires an interrupt vector fetch to clear the interrupt then the appropriate INT space should be accessed. Address bit A1 selects between Int0 and Int1. A1 follows the word address to allow access to both INT0 and INT1 clearing addresses within the INT space.

If the IP does not require a Vector fetch then proceed with IO or other accesses as necessary.

The Bus Error status bit is set high when a Bus Error is handled by the internal watch dog timer circuit. The status will stay high until cleared with the Bus Error Int / Status Clear bit in the base control register. The Bus Error status bit is or'd into the interrupt request logic and if enabled will cause a level sensitive interrupt to the host. The interrupt will remain asserted until the status is cleared.

pci3ip_intreg2

[$2000 User Switch Port read only]

CONTROL REGISTER 2	
DATA BIT	**DESCRIPTION**
7..0	Sw7..0

FIGURE 4 PCI3IP USER SWITCH PORT

The user switch is read through this port. The bits are read as the lowest byte. Access the port as a long word and mask off. Read only The switches are pulled-up on board. The dip-switch when "on" grounds the corresponding bits. "OFF" = 1 and "ON" = 0 in the PCI3IP silkscreen.

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pci3ip_alt_regA-C

[$3000, 0x4000, 0x5000 Alternate Control Register bit defintions]

CONTROL REGISTER A,B,C	
DATA BIT	**DESCRIPTION**
17	Interrupt Status 1
16	Interrupt Status 0
15-9	Spare
8	Bus Error Status/Clear
7-6	Reserved
5	Interrupt Enable 1
4	Interrupt Enable 0
3	High Word Access
2	Increment Disable
1	Force Interrupt
0	Clock Select

FIGURE 5 PCI3IP ALTERNATE CONTROL REGISTER PORTS

Please note that the Alternate Register Selection bit affects the following bit definitions. When ‘0’ the base register definitions are used. When ‘1’ the following register definitions are used.

CLK SEL is used to select the slot clock speed.
1 = 32 MHz. 0 = 8 MHz. PLL used to generate and low skew drivers to allow switching the clock speed on-the-fly.

Force Interrupt when ‘1’ causes an interrupt cycle, which will be interpreted as a IP slot interrupt. This bit was added to support interrupt service routine development when using the generic IP driver.

Increment Disable when ‘1’, turns off the address increment, for the respective slot, that normally occurs between 16-bit IP cycles when a 32-bit PCI access is performed. This is useful if, for instance, a FIFO is mapped to a single IP address since it allows double IP accesses to the same address with a single PCI transfer. All types of access are affected (i.e. MEM, IO, INT, and ID). Only 32 bit accesses are affected.

High Word Access controls which 16-bit word is accessed when the Increment Disable is asserted. When ‘0’ the lower word is accessed twice, when ‘1’ the upper word is accessed twice. This bit only has an effect when the Increment Disable bit is ‘1’. For correct functioning, make sure the PCI access is on a long-word boundary.

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Interrupt Enable 0, 1: Individual masks for the two interrupts from the respective IP slot. 0 corresponds to INT0 and 1 corresponds to INT1. When these bits are ‘1’, the interrupt is enabled, when ‘0’ the corresponding interrupt is disabled.

Bus Error Status/Clear when ‘1’ indicates that a bus error has occurred while attempting to access the respective IP slot.

Interrupt Status 0, 1: These are read-only status bits indicating, when the bit is a ‘1’, that the corresponding IP interrupt is active. However, the interrupt will not be passed on to the PCI bus unless the respective interrupt enable is also set.

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Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Start-up
Make sure that the "system" can see your hardware before trying to access it. Many BIOS will display the PCI devices found at boot up on a "splash screen" with the VendorID 0x10EE and CardId 0x0003 and an interrupt level. Look quickly! If the information is not available from the BIOS then a third party PCI device cataloging tool will be helpful.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Connecting external voltage to the PCI3IP when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. This applies more to the IP's installed into the PCI3IP than the PCI3IP itself, and it is smart system design when it can be achieved.

Connector definition. Slot A's IO connector is tied 1:1 to J5 which is nearest the card edge on the Slot A side. Slot B is tied to J4 and Slot C to J2. Standard ribbon cable can be used as well as discrete wiring to the header connector. HDEterm50 provides a ribbon cable to screw terminal interface. Custom cables are available for specific IP Modules.

Construction and Reliability

IP Modules were conceived and engineered for rugged industrial environments. The PCI3IP is constructed out of 0.062 inch thick High temp ROHS compliant FR4 material. Both ROHS and standard processing are available. Standard is the default and is the traditional leaded solder method. ROHS uses ROHS compliant devices and solder/flux etc.

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Through hole and surface mounting of components are used. High insertion and removal forces are required, which assists in the retention of components. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the corner pins of each socketed IC into the socket, using a grounded soldering iron.

The IP Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amps per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP Module can be secured against the carrier with the connectors. If more security against vibration is required then IP mounting kit can be used to attach the IP to the carrier.

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Thermal Considerations

The PCI3IP design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading then forced air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished. The installed IP Modules will be the driving factor in thermal calculations.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.

http://www.dyneng.com/warranty.html

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Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 DuBois St. Suite C
Santa Cruz, CA 95060
831-457-8891
831-457-4793 fax
support@dyneng.com

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Specifications

Logic Interfaces:	IP Logic Interface, PCI Interface -33 MHz. 32 bit Universal Voltage
Access types:	IO,ID,MEM,INT IP Spaces supported via PCI bus accesses
CLK rates supported:	8 mhz or 32 MHz slot by slot selectable 33 MHz. PCI
Software Interface:	Control Registers, and Installed IP
Initialization:	Programming procedure documented in this manual. Default to 8 MHz, interrupts disabled.
Access Modes:	LW, Word or Byte to IP registers LW to Internal PCI Interface Control registers
Access Time:	Depends on IP Module installed. State-Machine controlled, PCI compliant.
Interrupt:	2 Interrupts per IP slot with separate enables.
DMA:	No DMA Support implemented at this time
Onboard Options:	All Options are Software Programmable
Interface:	50 pin Header Connectors
Dimensions:	1/2 length PCI board.
Construction:	High Temp FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components. Programmable parts are socketed.
Temperature Coefficient:	2.17 W/^{o}C for uniform heat across IP
Power:	Filtered and fused to each IP slot. Resettable fuses. LED's (3) on slot A power (±12,5)
User	8 position software readable switch 6 software controllable LED's

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Order Information

Standard temperature range 0-70°C	
PCI3IP	1/2 length PCI card with 3 IP positions http://www.dyneng.com/pci_3_ip.html
Extended temperature range -40 - 85°C	
-**ET**	1/2 length PCI card with 3 IP positions
-**FPCO**	Front Panel with cutout to facilitate cabling to the outside through the PCI3IP Bezel
-ROHS	Use ROHS processing. Please note: standard "leaded" solder etc. used without this option. Boards with ROHS processing are marked "ROHS".
-EJ	Use Header Connectors with ejectors installed. Please note the increased height will be taller than PCI specification – for end slots or with an open slot next to the PCI3IP
-ENG	Engineering Kit for the PCI3IP Software, Schematic, Debugging tools
-XP	WindowsXP/2000 driver for the PCI3IP
-**LNX**	Linux driver for the PCI3IP
IP-DEBUG-BUS	http://www.dyneng.com/ipdbgbus.html IP test points, reset switch, fused power, quick switch isolated interface lines to allow hot swapping of IP cards.
IP-DEBUG-IO	http://www.dyneng.com/ipdbgio.html Isolate the IO connector to help with debugging. 50-pin header for system cable connection 50 testpoints suitable for wire-wrap to allow loop-back connections Locations for power and user circuits
HDRterm50	http://www.dyneng.com/HDRterm50.html 50-pin header to 50-screw terminal converter with DIN rail mounting
HDRribn50	http://www.dyneng.com/HDRribn50.html Ribbon cable with strain relief and cable pull tab Available in several lengths and custom

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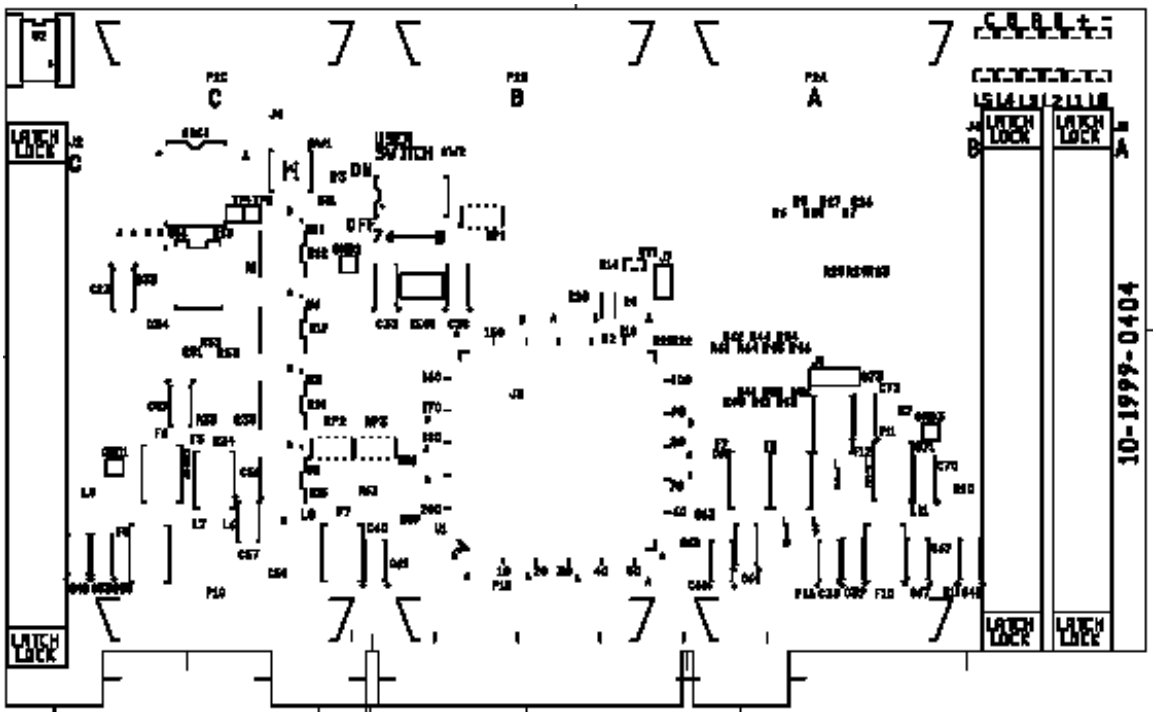
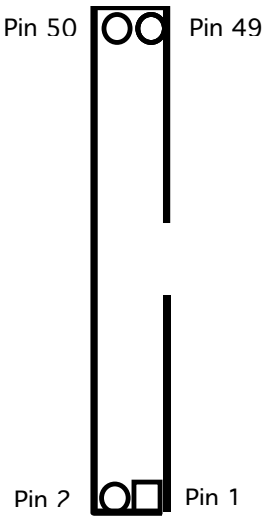


FIGURE 6 PCI3IP CONNECTOR REFERENCE

PCI3IP has three slots (A,B,C) and three header connectors associated with those slots.

The wiring is 1:1 from the IP IO connector to the PCI3IP header connector. The connectors are numbered to match standard ribbon cable as shown in the figure to the right.



50 Pin Header

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