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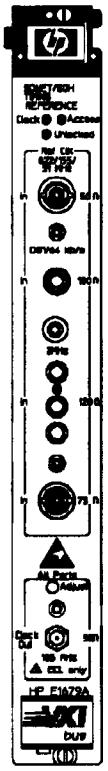
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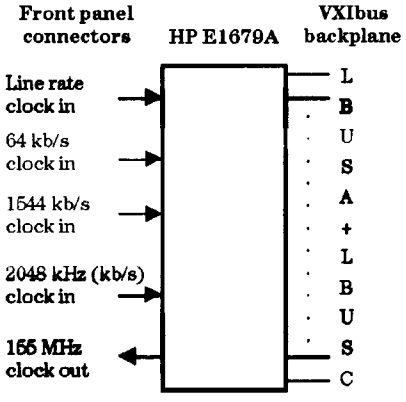
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HP E1679A SONET/SDH timing reference

An optional module, the HP E1679A timing reference adds frequency offset capability and a range of clock operating modes to the HP 75000 Series 90 analyzer. In addition, it provides a pointer sequencer capable of generating both standard (ANSI T1X1.6 and ITU-T G.783) and user-defined pointer adjustment sequences. For correct operation, the HP E1679A timing reference must be used in conjunction with the HP E1671A SONET/SDH transport overhead generator.





Clock source

Internal clock
Frequency: 51.84, 155.52, 622.08 MHz.
Setting accuracy: ±0.5 ppm.
Stability: ±3.0 ppm.
Ageing: ±1.0 ppm.

Loop timed
Available when operating in conjunction with HP E1672A SONET/SDH transport overhead receiver. Analyzer's transmitter section timed from the received clock signal input to the HP E1672A receiver. With the HP E1679A timing reference installed in a Series 90 analyzer, loop-timed clocking is supported in both terminal and thru-mode test configurations.
Frequency: 51.84, 155.52, 622.08 MHz.
Tolerance: ±20 ppm.

External clock
Frequency: 51.84, 155.52, 622.08 MHz.
Tolerance: ±20 ppm.
Waveform: Sinewave or squarewave.
Duty cycle: 50% ± 5% (typical).
Amplitude: 1 Vp-p (nominal).
Impedance: 50 ohm (nominal) to ground.
Interface: ac coupled.
Connector: BNC.

DS1 bits interface
Data rate: 1544 kb/s.
Tolerance: ±20 ppm.
Waveform: Framed all ones signal as per TA-TSY-000378.
Amplitude: ±3 Vpk (nominal) rectangular pulses.
Impedance: 100 ohm (nominal) balanced.
Connector: Bantam (screen grounded).

2048 kHz synchronization interface
Frequency: 2048 kHz.
Tolerance: ±20 ppm.
Waveform: Squarewave as per ITU-T G.703 (section 10).
Amplitude: 1.0 to 1.9 Vpk (120 ohm input); 0.75 to 1.5 Vpk (75 ohm input).
Impedance: 120 ohm balanced and 75 ohm unbalanced (both impedance values are nominal).
Connector: 3-pin Siemens (120 ohm) and BNC (75 ohm) (screens grounded).

2048 kb/s synchronization interface
Data rate: 2048 kb/s.
Tolerance: ±20 ppm.
Waveform: HDB3 coded data as per ITU-T G.703 (section 6).
Amplitude: 3 Vpk ± 10% (120 ohm input); 2.37 Vpk ± 10% (75 ohm input).
Impedance: 120 ohm balanced and 75 ohm unbalanced (both impedance values are nominal).
Connector: 3-pin Siemens (120 ohm) and BNC (75 ohm) (screens grounded).

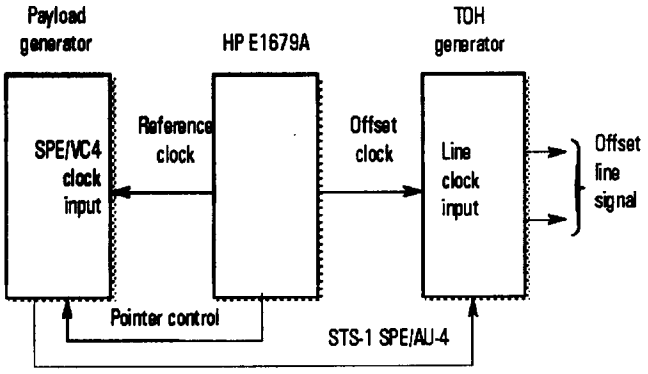
64 kb/s centralized clock interface
Data rate: 64 kb/s.
Tolerance: ±20 ppm.
Waveform: AMI with code violations as per ITU-T G.703 (section 1.2.2).
Amplitude: 0.9 to 3.5 Vpk.
Impedance: 110 ohm balanced, 120 ohm balanced (both nominal).
Connector: Bantam (110 ohm) and 3-pin Siemens (120 ohm) (screens grounded).

Frequency offset operation

Five frequency offset operating modes are supported by the HP E1679A timing reference.

- STS/STM line offset (compensating STS/AU-4 pointer adjustments)
- STS/STM line offset (compensating VT/TU pointer adjustments)
- STS-1 SPE/VC-4 offset
- VT/TU offset
- System offset.

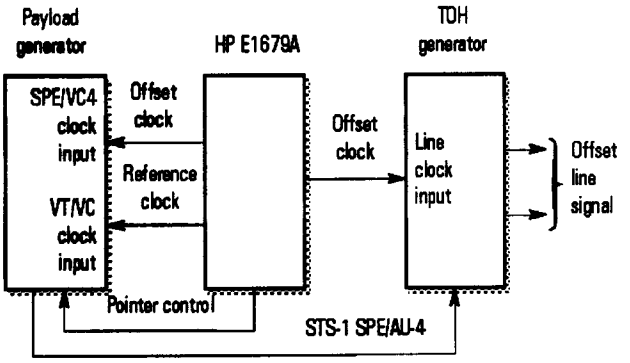
When frequency offset is selected, the HP E1679A timing reference generates two clock signals derived from the selected synchronization clock source – a reference clock and an offset clock. The reference clock is locked to the selected clock source, while the offset clock is based on, but offset from, the clock source. Depending on which frequency offset mode is selected, one HP E1679A timing reference generated clock is used to time the STS/STM line signal while the second is used to time internally generated payload signals. In line, SPE/VC-4 and VT/TU offset modes, evenly distributed pointer adjustments are generated to compensate for the selected frequency offset.



STS/STM line offset (compensating STS/AU-4 pointer adjustments)

STS/STM line signal timed by HP E1679A timing reference's offset clock while the STS-1 SPE/VC-4 payload is timed by HP E1679A reference clock. Synchronization of the payload signal to the line signal is accomplished by STS/AU-4 pointer adjustments (generated under control of the HP E1679A timing reference).

Offset range: 0 to ±100 ppm.
Resolution: 0.1 ppm.
Accuracy: ±0.02% of selected offset value.

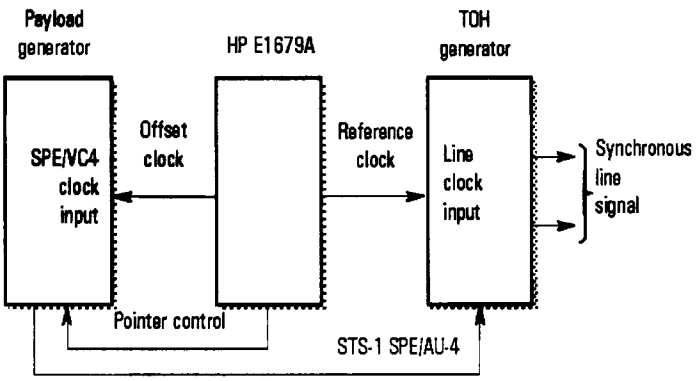


STS/STM line offset (compensating VT/TU pointer adjustments)

STS/STM line signal and STS-1 SPE/VC-4 payload timed by the HP E1679A timing reference's offset clock. A selected test VT/VC, generated as part of the STS-1 SPE/VC-4, is timed by the HP E1679A timing reference clock. Synchronization of the test VT/VC to the STS-1 SPE/VC-4 is accomplished by VT/TU pointer adjustments (generated under control of HP E1679A timing reference).

Pointer control: VT1.5, VT2, VT6, TU-11, TU-12, TU-2.
Offset range: 0 to ±100 ppm.
Resolution: 0.1 ppm.
Accuracy: ±0.02% of selected offset value.

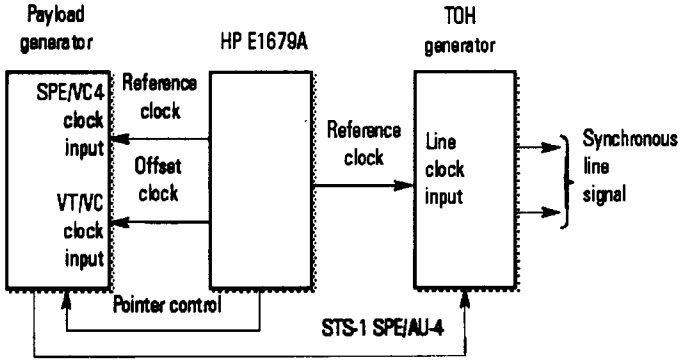
STS-1 SPE/VC-4 offset



STS/STM line signal timed by HP E1679A timing reference's clock while the STS-1 SPE/VC-4 payload is timed by HP E1679A timing reference's offset clock. Synchronization of the payload signal to the line signal is accomplished by STS/AU-4 pointer adjustments (generated under control of HP E1679A timing reference).

Offset range: 0 to ±100 ppm.
Resolution: 0.1 ppm.
Accuracy: ±0.02% of selected offset value.

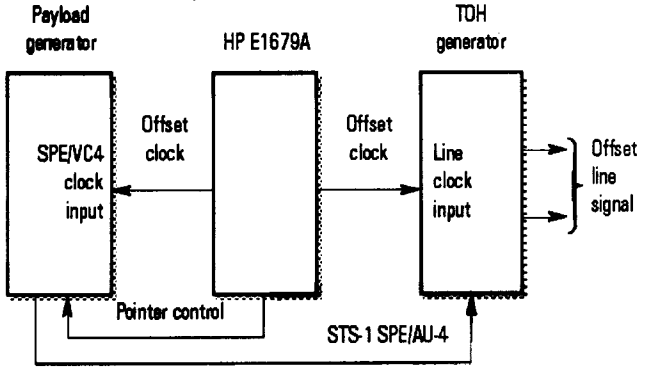
VT/TU offset



STS/STM line signal and STS-1 SPE/VC-4 payload timed by the HP E1679A timing reference's clock. A selected test VT/VC, generated as part of the STS-1 SPE/VC-4, is timed by HP E1679A timing reference's offset clock. Synchronization of the test VT/VC to the STS-1 SPE/VC-4 is accomplished by VT/TU pointer adjustments (generated under control of HP E1679A timing reference).

Pointer control: VT1.5, VT2, VT6, TU-11, TU-12, TU-2.
Offset range: 0 to ±100 ppm.
Resolution: 0.1 ppm.
Accuracy: ±0.02% of selected offset value.

System offset



STS/STM line signal and all parts of an STS-1 SPE/VC-4 payload are timed by the HP E1679A timing reference's offset clock. No pointer adjustments are generated.

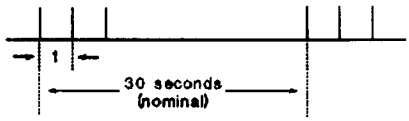
Offset range: 0 to ±100 ppm.
Resolution: 0.1 ppm.
Accuracy: ±0.02% of selected offset value.

Pointer adjustment sequence generation

In sequence mode, pointer adjustments are generated by offsetting the payload signal relative to the STS/STM line signal. For details on internal clocking configuration, refer to STS-1 SPE/VC-4 offset and VT/TU offset.

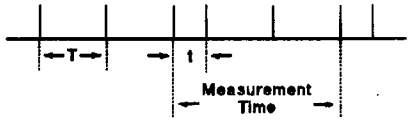
T1X1.6 pointer sequences

Burst



Pointer control: STS-1 SPE, AU-4.
Adjustment polarity: Incrementing or decrementing.
t: 500 µs (4 frames).

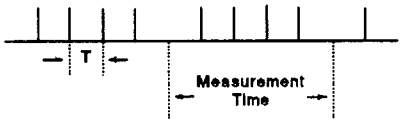
Periodic with additional



Pointer control: STS-1 SPE, VT1.5, VT2, VT6, AU-4, TU-11, TU-12, TU-2
Adjustment polarity: Incrementing or decrementing.
t: 500 µs (4 frames) for STS/AU-4 pointer; 2 ms (4 multiframes) for VT/TU pointer.
T: 10 to 15000 ms. Selected value rounded to nearest sub-multiple of measurement time.
Accuracy: ±0.02% of actual time interval (T).
Measurement time:

Pointer type	Measurement period	Accuracy
STS/AU-4	30.369 s	± 0.012%
VT1.5/TU-11	30.041 s	± 0.012%
VT2/TU-12	30.071 s	± 0.012%
VT6/TU-2	30.001 s	± 0.012%

Periodic with canceled



Pointer control: STS-1 SPE, VT1.5, VT2, VT6, AU-4, TU-11, TU-12, TU-2.
Adjustment polarity: Incrementing or decrementing
T: See periodic with additional.
Measurement time: See periodic with additional.

ITU-T G.783 pointer sequences

Alternating single adjustments



STS/STM line signal: Timed by HP E1679A timing reference clock.
Payload signal: Timed by HP E1679A timing reference clock.
Pointer control: STS-1 SPE, VT1.5, VT2, VT6, AU-4, TU-11, TU-12, TU-2.
T: 10 to 10000 ms in 10 ms steps.

Alternating double adjustments



STS/STM line signal: Timed by HP E1679A timing reference clock.
Payload signal: Timed by HP E1679A timing reference clock.
Pointer control: STS-1 SPE, VT1.5, VT2, VT6, AU-4, TU-11, TU-12, TU-2.
t: 500 µs (4 frames) for STS/AU-4 pointer; 2 ms (4 multiframes) for VT/TU pointer.
T: 10 to 10000 ms in 10 ms steps.

Regular with additional
See T1X1.6 periodic with additional sequence.

Regular with canceled
See T1X1.6 periodic with canceled sequence.

Periodic pointer sequences

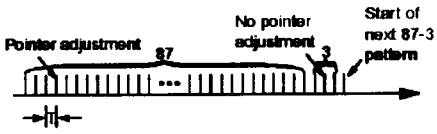
Periodic adjustments



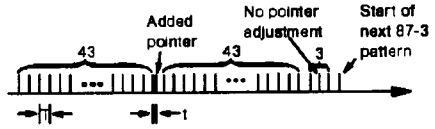
Pointer control: STS-1 SPE, VT1.5, VT2, VT6, AU-4, TU-11, TU-12, TU-2.
Adjustment polarity: Incrementing or decrementing.
t: 500 µs (4 frames) for STS/AU-4 pointer; 2 ms (4 multiframes) for VT/TU pointer.
T: 0.5 to 10000 ms for STS/AU-4 pointer; 2 to 10000 ms for VT/TU pointer.
Selected value rounded to nearest sub-multiple of Tmax.
Accuracy: ±0.02% of actual time interval (T).
Tmax:

Pointer type	Tmax	Accuracy
STS/AU-4	1639.91 s	± 0.012%
VT1.5/TU-11	49386.60 s	± 0.012%
VT2/TU-12	36687.19 s	± 0.012%
VT6/TU-2	12000.48 s	± 0.012%

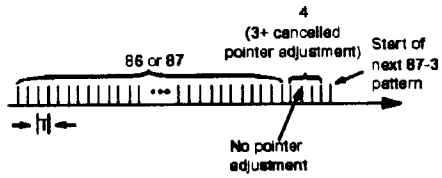
Gapped pointer sequences



Gapped with additional

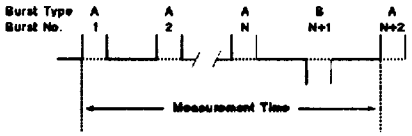


Gapped with canceled



User-defined pointer sequences

Supports generation of user-defined pointer adjustment sequences consisting of two separate programmable bursts (Burst type A and B).



Pointer control: STS-1 SPE, VT1.5, VT2, VT6, AU-4, TU-11, TU-12, TU-2.
Burst ratio (A:B): N to 1 (where N = 0 to 4095).
Measurement time: 10 to 45000 ms.

Burst generator A
Adjustments per burst: 0 to 16.
Adjustment separation: 4 to 16 frames for STS/AU-4 pointer; 4 to 16 multi-frames for VT/TU pointer.
Adjustment polarity: Incrementing or decrementing.

Burst generator B
Same controls as for burst generator A.

Note: Minimum measurement time is 10 ms or a value determined by the operator programmed bursts and burst ratio (A:B).

Clock output

Frequency: 155.52 MHz (nominal).
Timing: Locked to STS/STM line clock.
Waveform: Squarewave.
Duty cycle: 50% ± 5% (typical).
Level: Nominal ECL when externally terminated by 50 ohm to -2 V.
Interface: dc coupled.
Connector: SMA.

Status indicators

Front panel LEDs
Access: Module currently being addressed via VXI control bus.
Clock: Indicates presence of transitions at selected clock source (internal or external).
Unlocked: Timing PLL out of lock - selected clock source not present or outwith frequency range.

VXIbus characteristics

Device type: Register based. Operates as a servant of the HP E1671A module within the HP 75000 Series 90.
VXIbus backplane connectors: P1 and P2 (as defined in VXIbus specification rev. 1.3).
Local bus connection: Active connection to LBUSA to LBUSC.
Module keying: ECL.

Power requirements

Maximum current drawn from VXIbus dc voltage rails:

Volts dc	Current dc	Dynamic current
+5 V	1.25 A	125 mA
-5.2 V	1.75 A	175 mA
-2 V	400 mA	40 mA
+12 V	500 mA	50 mA
-12 V	100 mA	10 mA

Power dissipation: 23 W (max).

Physical

Size: 1 slot, C-size.
Weight: 1.6 kg (3.5 lb) (nominal).

Environmental

Operating temperature: 0 to +55°C.
Storage temperature: -40 to +75°C.
Humidity: 50% to 95% relative humidity from +25 to +40°C.
EMC: Meets CISPR11 Level A and EN50082-1.

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