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INSTRUCTION MANUAL

6056

SIGNAL CONDITIONER MODULE

PUBLICATION NO. 980727

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RACAL

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RETURN of PRODUCT

Authorization is required from Racal Instruments before you send us your product for service or calibration. Call your nearest Racal Instruments support facility. A list is located on the last page of this manual. If you are unsure where to call, contact Racal Instruments, Inc. Customer Support Department in Irvine, California, USA at 1-800-722-3262 or 1-949-859-8999 or via fax at 1-949-859-7139. We can be reached at: helpdesk@racalinstruments.com.

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FOR YOUR SAFETY

Before undertaking any troubleshooting, maintenance or exploratory procedure, read carefully the **WARNING** and **CAUTION** notices.

This equipment contains voltage hazardous to human life and safety, and is capable of inflicting personal injury.

If this instrument is to be powered from the AC line (mains) through an autotransformer, ensure the common connector is connected to the neutral (earthed pole) of the power supply.

Before operating the unit, ensure the conductor (green wire) is connected to the ground (earth) conductor of the power outlet. Do not use a two-conductor extension cord or a three-prong/two-prong adaptor. This will defeat the protective feature of the third conductor in the power cord.

Maintenance and calibration procedures sometimes call for operation of the unit with power applied and protective covers removed. Read the procedures and heed warnings to avoid "live" circuit points.

Before operating this instrument:

1. Ensure the instrument is configured to operate on the voltage at the power source. See Installation Section.

2. Ensure the proper fuse is in place for the power source to operate.

3. Ensure all other devices connected to or in proximity to this instrument are properly grounded or connected to the protective third-wire earth ground.

If the instrument:

- fails to operate satisfactorily
- shows visible damage
- has been stored under unfavorable conditions
- has sustained stress

Do not operate until performance is checked by qualified personnel.

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Racal Instruments

EC Declaration of Conformity

We

Racal Instruments Inc.
4 Goodyear Street
Irvine, CA 92718

declare under sole responsibility that the

6056 Signal Conditioner
P/N 407144-003

conforms to the following Product Specifications:

Safety: EN 61010-1

EMC: CISPR 11:1990/EN 55011 (1991): Group 1 Class A
IEC 801-2:1991/EN 50082-1 (1992): 4 kV CD, 8 kV AD
IEC 801-3:1984/EN 50082-1 (1992): 3 V/m, 27-500 MHz
IEC 801-4:1988/EN 50082-1 (1992): 1 kV

Supplementary Information:

The above specifications are met when the product is installed in a Racal Instruments certified mainframe with faceplates installed over all unused slots, as applicable.

The product herewith complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC.

Irvine, CA, October 7, 1997

Quality Manager

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SECTION 1 GENERAL INFORMATION

1.1 Introduction

1.1.1 The Racal-Dana Model 6056 Signal Conditioner Module (SCM) is a microprocessor-controlled instrument which consists of three functional blocks.

1. Two identical Level Threshold Detectors (LTD) which convert analog signals into digital format.

2. Two identical Time Constant Filters (TCF) designed to filter analog signals.

3. A window generator which outputs logically combined outputs of the two LTDs.

1.1.2 The 6056 is designed to be used under the direction of the Slot 0 System Resource Manager of a VXIbus compatible mainframe. The 6056 conforms to the VXIbus System Specification Revision 1.3.

1.1.3 The 6056 can only be controlled remotely over the VXIbus. No local control of the instrument is possible. The command set the SCM responds to is designed to conform to the Standard Control for Programmable Instruments (SCPI) Version 1992.0. The instrument will also interpret IEEE-488.2 compatible commands. Refer to Section 3 of this manual for details of the Command Set.

1.1.4 Refer to Figure 1.1 for an illustration of the 6056.

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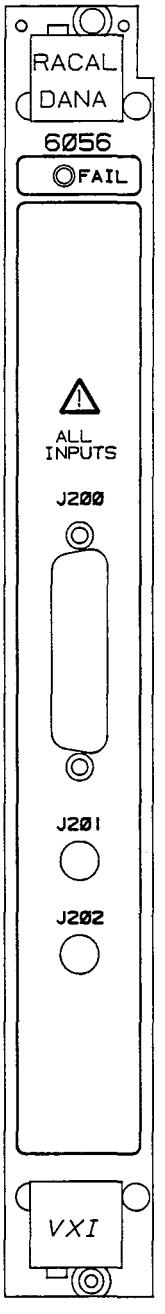


Figure 1-1, Model 6056 Front Panel

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1.2 Performance Specifications

1.2.1 Level Threshold Detector

Analog Input	
Frequency Range	DC to 100 KHz minimum
Input Impedance	402kohms +/-1%
Inputs	Isolated LTD1 and LTD2 on 25 way DSUB (J200) LTD1 HI pin13 LTD1 LO pin25 LTD2 HI pin12 LTD2 LO pin24 VXI TTLTRG* lines on P2 Connector
Hysteresis	-60mV to +60mV nominal at signal input, centered on programmed threshold value
Isolation	500 MOhm. The input is isolated from the system output and system ground
Maximum Input Without Damage	250V DC or AC RMS (Switched) 300V DC or AC RMS (Unswitched)
Signal Operating Range	-40V to +40V
Trigger Accuracy	+/-1% +/-150mV
Resolution	20mV
Propagation_Delay Time (Analog Input or TTLTRG Input)	<500nS

1.2.2 Output Requirements

Main Output Level	10V nominal
Output Impedance	50Ω
Connector Type	25 way DSUB (J200) LTD1 HI pin 22 LTD1 LO pin 9 LTD2 HI pin 21 LTD2 LO pin 8
High Level	$4.6V_{MIN}$ into 50ohms
Low Level	$0.4V_{MAX}$ into 50ohms

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Maximum Rise/Fall Time (RI = 50 Ohm, CI = 15 pF)	100nS

The Main outputs shall be programmable to trigger in either of the following modes:

a) Rising edge on input, main output goes HI;
Falling edge on input, main output goes LO

b) Rising edge on input, main output goes LO:
Falling edge on input, main output goes HI

1.2.3 Time Constant Filter

Input Requirements

Analog Input

Connector Type	25 way DSUB (J200)	
	TCF1 HI pin3	TCF2 LO pin 15
	TCF2 HI pin1	TCF2 LO pin 14
Frequency Range	DC to 100 kHz	
Signal Operating Range	-40V to +40V	
Maximum Input Without Damage	250V DC or AC RMS (Switched)	
	300V DC or AC RMS (Unswitched)	
Coupling	DC, isolated from ground	

1.2.3.1 Filter Requirements

The filter shall be a single pole, passive low pass filter with a time constant programmable between 0µS and 4096µS as defined below.

The filter shall be designed to fulfill all design criteria when a 160pF capacitance and 1 MOhm resistance is applied at the output.

Time Constant Range	X1	0 µS and 3.2µS to 409.6 µS
	X10	0 µS to 4096 µS
Resolution	X1	1.6 µS
	X10	16 µS

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Accuracy (Time constant)		32µS to 409.6µS ±10%
(Source Z = 50 Ohm, Load Z = 1 MOhm)		12.8µS to 30.4µS ±20%
Load C = 160pF		4.8µS to 11.2µS ±50%
		3.2µS ±100%
Insertion Loss	X1	0.6% nominal
(Into 1 Mohm Load)	X10	6% nominal

Output Requirements

Analog Output

Connector Type	SMC (TCF1 J201, TCF2 J202)
Coupling	DC, isolated from ground

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1.2.4 Window Generator

1.2.4.1 Modes of Operation

The window output shall be able to be set into one of six modes whose logic shall behave as follows below. Either of the LTD outputs (window inputs) may be inverted prior to logical operation.

MODE	LTD 1	LTD 2	Window O/P
OFF	Don't Care	Don't Care	LO
AND	LO LO HI HI	LO LO LO HI	LO LO LO HI
OR	LO LO HI HI	LO HI LO HI	LO HI HI HI
NAND	LO LO HI HI	LO HI LO HI	HI HI HI LO
NOR	LO LO HI HI	LO HI LO HI	HI LO LO LO
XOR	LO LO HI HI	LO HI LO HI	LO HI HI LO

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1.2.4.2 Output Requirements

Window Output Level	10V nominal
Output Impedance	50Ω
Connector Type	25 way DSUB (J200) Window HI pin 20 Window LO pin 7
High Level	$4.6V_{MINIMUM}$ into 50ohms
Low Level	$0.4V_{MAXIMUM}$ into 50ohms
Maximum Rise/Fall Time	100 nS Max
Propagation Delay (Analog or TTLTRG Input)	500 nsec Max

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1.2.5 TTLTRG Lines

These lines are used to input and output signals from the SCM under program control.

1.2.5.1 Input Requirements

LTD#1 TTLTRG* LTD#2 TTLTRG*	The VXI backplane trigger for LTD#1 and LTD#2
Trigger Protocol	Inputs conform to the TTLTRG* SYNCHRONOUS (SYNC) Trigger Protocol
Input Trigger Selection	Program control selects from TTLTRG0 to TTLTRG7
LTD#1, LTD#2 Input Source	Program control selects either LTD#1/2 Analog or LTD#1/2 TTLTRG* as input source

1.2.5.2 Output Requirements

LTD#1 TTLTRG* LTD#2 TTLTRG* WINDOW TTLTRG*	The LTD#1/2 signals and WINDOW signal transmitted onto the VXI backplane using the TTLTRG lines
Trigger Protocol	User defined protocol as the outputs do not conform to SYNC, ASYNC, SEMI-SYNC, CLOCK TRANSMISSION, DATA TRANSMISSION or START/STOP protocols. Signals are buffered versions of the output signals LTD#1/2 and WINDOW with the same pulse duration.
I/O Phase	IN or OUT of Phase
TTLTRG Output Line	Each signal will be assigned to one of the eight TTLTRG0-7 lines under program control.
Output Disable	The TTLTRG output can be disabled under program control. The output is an open collector type which is disabled HIGH.

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1.2.6 IRQ Lines

1.2.6.1 Input Requirements

IRQ Inputs: LTD#1 LTD#2 LTD#1 OR LTD#2 LTD#1 AND LTD#2	Local Interrupt source for 6056 microprocessor is selected under Program Control. LTD outputs can be phase inverted before logical operation. Further interrupts are ignored until Interrupt Acknowledge is received from the Slot 0 Controller.

1.2.6.2 Output Requirements

IRQ Output	The 6056 microprocessor outputs interrupt on VXI backplane after local interrupt received from LTDs as above.
IRQ Output Line	One of IRQ1* - IRQ7* lines is selected either under Program Control or Manually.
Output Disable	The IRQ outputs can be disabled under program control. The output is an open collector type which is disabled HIGH.

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1.2.7 Power Supply Requirements

1.2.7.1 The maximum currents which may be drawn from each VXI Supply rail for this one slot unit are as follows:

+24V	1.0A
+12V	1.0A
+5V	7.0A
-2V	2.0A
-5.2V	5.0A
-12V	1.0A
-24V	1.0A

1.2.7.2 The maximum power which the unit may consume shall not exceed 45 Watts.

1.2.8 Mechanical Details

1.2.8.1 The unit will occupy one slot in a C-sized VXI chassis. There will be a single PCB in a folded sheet metal enclosure. Attention will be paid to ensure that the case forms a good RF screen, but some holes will be made for connectors, cooling, etc.

Unit Height	262mm
Unit Width	30.18mm
Unit Depth	355mm
Unit Weight	TBA

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1.2.9 Environmental and EMC Performance

1.2.9.1 Cooling Requirements

Air inlet holes must be provided in the bottom face of the instrument and, exhaust ports in the top face.

1.2.9.2 Environmental

Meets the requirements of MIL-STD-28800D, Type III, Class 5 with the following exceptions:

Operating Temperature	0°C to 50°C
Storage Temperature	-40°C to +70°C
Relative Humidity	up to 75% from 11°C to 30°C up to 65% from 31°C to 40°C up to 45% from 41°C to 50°C

1.2.9.3 EMC

Meets the following (except where stated in the Quality Plan for ATE Series 6):

VXIbus System Specification, Revision 1.3, July 14, 1989, Section B8
MIL-STD-28800.

1.2.10 Interface Functions

The instrument shall use Word Serial protocols to communicate over the VXIbus and conform to IEEE 488.2.

1.2.10.1 VXIbus Interface Compatibility

The interface shall be compliant with VXIbus Specification 1.3. It shall be a message-based servant VXI device implementing A16 addressing, and provide the following VXI capabilities:

1.2.10.1.1 VXI Device Type - A16, Message-Based Servant

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1.3 Safety

1.3.1 The 6056 incorporates a protective earth terminal and is designed to meet international safety requirements. Refer to the "**FOR YOUR SAFETY**" page preceding the Table of Contents. Follow all **NOTES, CAUTIONS** and **WARNINGS** to ensure personal safety and prevent damage to the instrument.

1.4 Product Support

1.4.1 Racal-Dana supports the 6056 with Product Engineering, Service and Parts Departments. A complete listing of service centers and field representatives is a provided on the last two pages of this manual.

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SECTION 2 INSTALLATION

2.1 Introduction

2.1.1 This section describes the unpacking and inspection, reshipment, installation and environmental requirements of the Racal Dana Model 6056 Signal Conditioner Module.

2.2 Unpacking and Inspection

2.2.1 Before unpacking the 6056, check the exterior of the shipping carton for any signs of damage. All irregularities should be noted on the shipping bill. Remove the instrument from its carton, preserving the factory packaging as much as possible. Inspect the unit for any defect or damage. Notify the carrier immediately if any damage is apparent. Have a qualified person check the unit for safety before use.

2.3 Reshipment Instructions

2.3.1 Use the original packing if it is necessary to return the unit to Racal-Dana for calibration or servicing. The original shipping carton and the instruments plastic foam will provide the necessary support for safe reshipment. If the original packing is unavailable, wrap the unit in plastic sheeting and use plastic spray foam to surround and protect the unit. Reship in either the original or a new, sturdy shipping carton.

2.4 Interrupt Level and Logical Address Setting

2.4.1 The Logical Address and Interrupt Level of the 6056 are both manually and dynamically selectable via switches SW1 and SW2. If it is necessary to manually change either the logical address or the interrupt level setting, it must be done prior to installing the 6056 into the mainframe. Use the following procedure for setting up the interrupt level and logical address.

2.4.1.1 Place the front edge of the unit to your right, and locate the access slot in the top edge of the 6056. Two switches (SW1 and SW2) can be observed through this opening. Switch SW2 is the switch nearest the front edge of the unit. SW1 is located to the left, toward the rear of the unit. See Figure 2-1.

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2.4.1.2 Switch SW1 is used to set the logical address of the 6056. Set SW1 to the binary equivalent of the logical address desired. Logical addresses between 1 and 255 (FF_{HEX}) are permitted. The OFF switch positions on SW1 correspond to binary 1. The 6056 is shipped from the factory with the logical address set at 03. For dynamic logical address configuration, set the switches to FF_{HEX}.

2.4.1.3 Switch SW2, bits 1 through 3, are used to set the interrupt level of the 6056. Set SW2 to the binary equivalent of the interrupt level desired. Interrupt levels between 1 and 7, inclusive, are permitted. The OFF switch positions on SW2 correspond to binary 1. The 6056 is shipped from the factory with the interrupt level set at 02.

2.4.1.4 Switch SW2 bit 4 shall determine whether the interrupt level is set manually or dynamically. Set SW2 bit 4 to the ON position for manual interrupt selection.

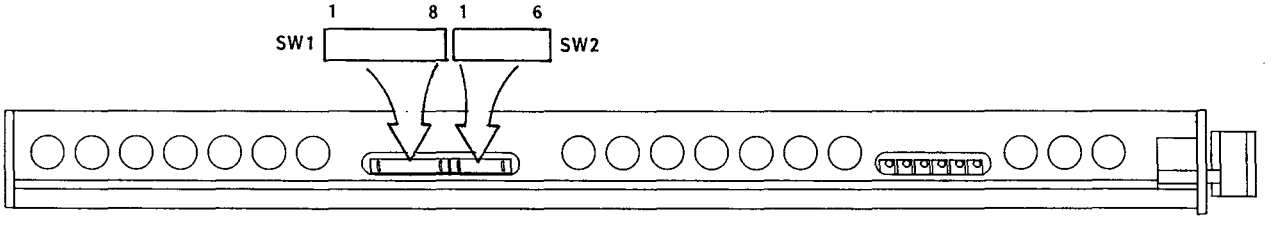


Figure 2-1. Switch Location - SW1 and SW2

2.5 Installation

2.5.1 Before installation of the 6056, carry out a visual inspection of the instrument. Pay particular attention to connectors P1 and P2 on the rear of the instrument, and ensure there are no bent, damaged or missing pins. Repair any damage before proceeding.

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2.5.2 To install the 6056 in a C-size, VXI mainframe, ensure the instrument has rear connector P1 oriented to mate with the corresponding connector on the mainframe backplane. Align the 6056 with the guides for the slot selected, and slide the unit into the mainframe. Push the unit home to connect the 6056 to the mainframe. Secure the unit to the mainframe with the captive screws provided at the top and bottom edges of the unit.

2.5.2.1 Poor mechanical alignment of rear connectors P1 and P2 may require the unit to be reseated in the VXI mainframe. Do NOT use undue force to seat the unit.

2.5.3 Power-up the mainframe. Ensure the SYSFAIL LED on the 6056 front panel lights and extinguishes after a few seconds to show the instrument has passed its power-up self-test. The 6056 is now ready for use.

2.5.4 To remove the 6056 from the VXI mainframe, power-down the mainframe, and release the captive screws that secure the unit to the mainframe. Use the plastic levers provided on the top and bottom edges to eject the 6056 from the mainframe. Pull the instrument along the guides provided, and out of the mainframe.

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SECTION 3 SYSTEM OPERATION

3.1 Introduction

3.1.1 This chapter describes the operation and programming of the 6056 Signal Conditioner Module (SCM).

3.2 6056 Home State

3.2.1 The 6056 Home State is the configuration the 6056 will adopt on powering up and upon receiving the "*RST" command. Refer to Table 3-1 for details of the 6056 home state.

Table 3-1, 6056 Home State Configuration

Feature	Default Setting
LTD 1/2 Thresholds	: Set to +40.0V
Time Constant Filter (TCF) 1/2	: Enabled
TCF Time	: 1.6 µs
Main 1 output	: Connected to LTD 1 input
Main 2 output	: Connected to LTD 2 input
Main 1 polarity	: Normal
Main 2 polarity	: Normal
TTLTRGn outputs	: Disconnected
Window Function	: Low
Interrupt Function	: LTD 1 input, disabled

3.3 Command Set Overview

3.3.1 The 6056 SCM is programmed using ASCII commands which conform to SCPI or IEEE-488.2 syntax.

3.3.2 IEEE-488.2 commands perform operations which are common to many instruments. These include commands to reset the instrument, read the status byte, enable interrupts based on instrument status, etc. All IEEE-488.2 commands begin with an asterisk (*) character.

3.3.3 The SCPI standard defines the syntax for commands which are not defined in IEEE-488.2. The syntax is described using a tree structure, with the root of the tree defining the command subsystems, and each level of the tree defining the subcommands which may be used in the command subsystem.

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3.3.4 SCPI Commands may be sent in either of two forms: the *long* form or the *short* form. The *long* form requires all characters in the command be sent; the *short* form requires only the first three or four characters (depending on the command) be sent. As an example of long and short forms, the "INPUT" command is shown in the command tree as "INPut". The short form includes only the upper case characters in the command ("INP"), while the long form includes ALL of the characters ("INPUT").

3.3.5 The SCPI standard requires that commands are separated from their subcommands by a colon (:) character.

3.3.6 Often, a command in the command tree will be optional. When a command is optional, it is shown in the SCPI command tree enclosed in square brackets ([]). Optional command parameters are also shown enclosed in square brackets. When a single value must be selected from a list of values, the values are separated using a vertical bar (|). Finally, when a parameter may take any of a number of values, the parameter is shown enclosed in "less than/greater than" characters (< >).

3.3.7 To illustrate the use of optional commands, the INPUT subsystem syntax is described with the command tree:

```
INPut
      : FILTer<N>
            [ : LPASs ]
                  [ : STATe ]  ON | OFF | 1 | 0

                     : TIME  <numeric value>
```

3.3.7.1 The following commands may be used to turn the filter for input A on:

INP:FILT1:LPAS:STAT ON	--	Short form, all optional commands used
INPUT:FILTER1:LPASS:STATE ON	--	Long form, all optional commands used
INPUT:FILT1:LPASS:STAT ON	--	Mix of long and short forms, all optional commands used
Input:Filter1:Lpass:State ON	--	Long form, mixed cases, all optional commands used
INPUT:FILTER1 ON	--	Long form, no optional commands used

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INPUT:FILT1:STATE ON	--	Mix of long and short forms, the optional LPASS command is not used

3.3.7.2 Almost all SCPI commands have a corresponding query. The query is formed by appending a question mark (?) at the end of the command. For example, the command

INPUT:FILTER1:STATE

has a corresponding query:

INPUT:FILTER1:STATE?

3.3.8 Unless otherwise specified, all SCPI commands in this manual have a corresponding query form.

3.3.9 Command parameters may be numeric or a string of literal characters. Where a numeric value is accepted or returned by a command, the number will be described as <NR1>, <NR2>, or <NR3> in accordance with the IEEE-488.2 standard. Consult Subsection 3.7 for a further description of the numeric formats.

3.4 IEEE-488.2 Common Commands

3.4.1 IEEE-488.2 Common Command Summary

3.4.1.1 The 6056 SCM accepts all required IEEE-488.2 Common Commands. These commands are summarized in Table 3-2, and described in more detail in the following text.

3.4.1.2 Many of the IEEE-488.2 commands and queries are associated with the reporting of instrument status. See Subsection 3.6 for a discussion of status and error reporting as implemented by the 6056 SCM.

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Table 3-2, Supported IEEE-488.2 Commands

Command	Description
*CLS	Clear IEEE-488.2 status
*ESE	Enable Standard Event Status Register conditions to feed through to the Status Byte Register
*ESE?	Read the value currently programmed for the Standard Event Status Register
*ESR?	Read the instrument status information from the Standard Event Status Register
*IDN?	Read the instrument identification string
*OPC	Set the OPC bit in the Standard Event Status Register when all pending operations have completed
*OPC?	Place a '1' in the output queue when all pending operations have completed
*RST	Reset the instrument hardware to the power-up configuration
*SRE	Set the Service Request Enable register to enable the conditions to generate an interrupt
*SRE?	Read the value currently programmed for the Service Request Enable Register
*STB?	Read the Status Register value
*TST?	Perform an instrument self-test. Return the result of the self-test in the output queue
*TRG	Trigger the instrument (This has no effect, but is included for IEEE-488.2 compliance.)
*WAI	Wait to continue until all pending operations have completed

3.4.2 *CLS Command

3.4.2.1 The *CLS command clears the Event Status Register. The Status Byte Register is cleared with the exception of the Message Available bit (MAV), which is set or cleared depending on the state of the output queue.

3.4.2.2 The syntax for the *CLS command is

*CLS

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3.4.3 *ESE Command

3.4.3.1 The *ESE command enables conditions from the Event Status Register to be fed through to the Event Status Bit (ESB) of the Status Byte Register. The ESB bit acts as a summary which indicates one or more of the enabled events have occurred since the last reading or clearing of the Standard Event Status Register.

3.4.3.2 The ESB summary bit is assigned to bit 5 of the Status Byte Register. The ESB bit will be set when:

a) A bit is set in the Event Status Register and the *ESE command is sent with the corresponding bit set; or

b) A bit becomes set in the Event Status Register after the bit has been previously enabled with the *ESE command.

3.4.3.3 The syntax for the *ESE command is

*ESE <enable mask>

where <enable mask> is an <NR1> format number in the range 0 to 255.

3.4.3.4 The bits are assigned in accordance with the IEEE-488.2 standard. The bit assignments are shown in Table 3-3.

Table 3-3, Standard Event Status Register Bit Assignment

Bit #	Weight	Name	Description
0	1	OPC	Operation Complete
1	2	RQC	Request Control (always 0)
2	4	QYE	Query Error
3	8	DDE	Device Dependent Error
4	16	EXE	Execution Error
5	32	CME	Command Error
6	64	URQ	User Request (always 0)
7	128	PON	Power On

3.4.3.5 For example, the command

*ESE 5

will cause the ESB bit of the Status Byte to be set when either the Operation Complete bit or the Query Error bit becomes set in the Standard Event Status Register.

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3.4.3.6 At power-up, the *ESE value is set to 0. The *RST command does NOT alter the *ESE value.

3.4.4 *ESE? Query

3.4.4.1 The *ESE? query reads the value presently programmed into the Standard Event Status Enable Register. This query will return a reply in <NR1> format. The reply will be 0 after a power-up, or a value between 0 and 255 after the *ESE command has been received by the instrument.

3.4.4.2 The syntax for the *ESE? query is

*ESE?

3.4.5 *ESR? Query

3.4.5.1 The *ESR? query destructively reads the Standard Event Status Register. After the value is read with the *ESR? query, the bits in the Standard Event Status Register are cleared to 0.

3.4.5.2 The bit assignments for the *ESR? query are the same as those used for the *ESE command. Consult table 3-3 for a description of the bit assignments.

3.4.5.3 The *ESR? query will return a reply in <NR1> format.

3.4.5.4 The syntax for the *ESR? query is

*ESR?

3.4.6 *IDN? Query

3.4.6.1 The *IDN? query reads the instrument identification string from the SCM.

3.4.6.2 The identification string is a series of four ASCII character fields. Each field is separated by a comma (,). The fields are:

Field 1	Manufacturer
Field 2	Model
Field 3	Serial Number or 0
Field 4	Firmware Revision

3.4.6.3 The response from the instrument for the *IDN? query is

Racal-Dana Instruments,6056,0,X.Y

where the "X.Y" will be replaced by the current firmware revision of the SCM.

3.4.6.4 The syntax for the *IDN? query is

*IDN?

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3.4.7 *OPC Command

3.4.7.1 The *OPC command causes the instrument to set the OPC bit in the Standard Event Status Register when all pending operations have completed.

3.4.7.2 A typical use of the *OPC command would be:

a) Send the "*ESE" command with the OPC bit set (e.g. "*ESE 1")

b) Send a series of operational commands to change the filter settings, voltage thresholds, etc.

c) Send the "*OPC" command.

d) Perform a VXI READ STB command to read the Status Byte Register. When the ESB bit (bit 5) of the Status Byte is set, all operations have completed.

3.4.7.3 The syntax for the *OPC command is

*OPC

3.4.8 *OPC? Query

3.4.8.1 The *OPC? query causes the instrument to place an ASCII "1" in the output queue when all pending operations have completed.

3.4.8.2 A typical sequence for the "*OPC?" query would be:

a) Send operational commands to configure the instrument

b) Send the "*OPC?" query

c) Read the Status Byte Register by using the VXI "Read STB" command. When the MAV bit (bit 4) is set, then read the instrument and check that string "1" is returned.

3.4.8.3 The syntax for the "*OPC?" query is

*OPC?

3.4.9 *RST Command

3.4.9.1 The *RST command places the instrument hardware in the Home State as described in Table 3-1.

3.4.9.2 The *RST command does NOT alter the status reporting structures (i.e., Status Byte Register, Standard Event Enable Register, etc.), nor does it affect the output queue.

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3.4.9.3 The VXI Clear command and the IEEE-488.2 *CLS command should be used in conjunction with the *RST command to place the instrument into the power-up state. In general the following sequence should be performed:

a) send the VXI clear command ($FFFF_{16}$)

b) send the *CLS command to clear the status

c) send the *RST command to reset the hardware

3.4.9.4 The syntax for the *RST command is

*RST

3.4.10 *SRE Command

3.4.10.1 The *SRE command selects the conditions which will set the MSS bit (bit 6) in the Status Byte Register. The conditions are represented by bits 0 through 5, and bit 7, of the Status Byte Register.

3.4.10.2 The syntax for the *SRE command is

*SRE <enable mask>

where <enable mask> is an <NR1> format number in the range 0 to 255.

3.4.10.3 The bits are assigned in accordance with the IEEE-488.2 standard. The bit assignments are shown in Table 3-4.

Table 3-4, Status Byte Register Bit Assignment

Bit #	Weight	Name	Description
0	1	n/a	Not used, always 0
1	2	n/a	Not used, always 0
2	4	n/a	Not used, always 0
3	8	DSB	Device-specific, set when the card has received an interrupt from the LTD 1/2 interrupt circuit
4	16	MAV	Message Available, set when a message is in the output queue
5	32	ESB	Event Status Bit, set when one or more *ESE enabled bits are set
6	64	MSS	Message Status Summary, set when one or more the *SRE enabled bits are set
7	128	n/a	Not used, always 0

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3.4.10.4 For example, the command

*SRE 48

will cause MSS bit of the Status Byte Register to be set when either the Event Status Bit or the Message Available bit become set.

3.4.10.5 At power-up, the *SRE value is set to 0. The *RST command does NOT alter the *SRE value.

3.4.10.6 A transition of the MSS bit from 0 to 1 will cause a VXI Request True Event if the Request True Event is enabled. A transition of the MSS bit from 1 to 0 will cause a VXI Request False Event if the Request False Event is enabled. Events are enabled using the VXI Asynchronous Mode Control and Control Event commands.

3.4.11 *SRE? Query

3.4.11.1 The *SRE? query reads the value presently programmed into the Service Request Enable Register. This query will return an <NR1> reply. The reply will be 0 after a power-up, or a value between 0 and 255 after the *SRE command has been received by the instrument.

3.4.11.2 The syntax for the *SRE? query is

*SRE?

3.4.12 *STB? Query

3.4.12.1 The *STB? query reads the current value in the Status Byte Register. No bits are cleared as a direct result of executing the *STB? query.

3.4.12.2 The reply from the "*STB?" query will be an <NR1> format number. The bit assignments for the Status Byte Register are shown in Table 3-4.

3.4.12.3 The syntax for the "*STB?" query is

*STB?

3.4.13 *TST? Query

3.4.13.1 The *TST? query initiates an instrument self-test. At the conclusion of the self-test, the instrument places a numeric reply in it's output queue. The reply is in <NR1> format. The number assignments for the self-test results are shown in Table 3-5.

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Table 3-5, Self-Test Error Codes

Code	Description
0	Test successful
100	RAM failed
101	ROM checksum failed
102	BIT Latch A wrap-around test failed
103	BIT Latch B wrap-around test failed
104	BIT Latch C wrap-around test failed
105	Main A output failed. Selftest relay and/or LTD 1 DAC are suspect
106	Main B output failed. Selftest relay and/or LTD 2 DAC are suspect
107	Window LOW function failed
108	Window AND function failed
109	Window OR function failed
110	Window XOR function failed
111	IRQ on LTD 1 failed; interrupt circuitry suspect
112	IRQ on LTD 2 failed; interrupt circuitry suspect
113	IRQ on "LTD 1 OR LTD 2" failed
114	IRQ on "LTD 1 AND LTD 2" failed
115	At least one filter relay is stuck closed
116	TCF 1 x1/x10 select relay (K8) has failed
117	TCF 1 enable relay (K9) has failed
118	TCF 2 x1/x10 select relay (K10) has failed
119	TCF 2 enable relay (K11) has failed
120	TCF 1, 250 pF relay has failed (U94)
121	TCF 1, 500 pF relay has failed (U95)
122	TCF 1, 1000 pF relay has failed (U96)
123	TCF 1, 2000 pF relay has failed (U97)
124	TCF 1, 4000 pF relay has failed (U98)
125	TCF 1, 8000 pF relay has failed (U99)
126	TCF 1, 16000 pF relay has failed (U100)
127	TCF 1, 32000 pF relay has failed (U101)
128	TCF 1, discharge relay has failed (U102)
129	TCF 2, 250 pF relay has failed (U103)
130	TCF 2, 500 pF relay has failed (U104)
131	TCF 2, 1000 pF relay has failed (U105)
132	TCF 2, 2000 pF relay has failed (U106)

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Table 3-5, Self-Test Error Codes (continued)

Code	Description
133	TCF 2, 4000 pF relay has failed (U107)
134	TCF 2, 8000 pF relay has failed (U108)
135	TCF 2, 16000 pF relay has failed (U109)
136	TCF 2, 32000 pF relay has failed (U110)
137	TCF 2, discharge relay has failed (U111)

3.4.13.2 If the self-test fails, the Execution Error bit (EXE, bit 4) of the Standard Event Status Register will be set.

3.4.13.3 If the self-test fails, an error will be placed in the error queue. The error may be read by sending the "SYSTEM:ERROR?" query, and then reading the instrument.

3.4.13.4 Upon completion of the self-test, the instrument will be placed in the home state. All status structures will be cleared. The only exception is the EXE bit, which will be set in case of test failure.

3.4.13.5 The syntax for the *TST? query is

*TST?

3.4.14 *TRG Command

3.4.14.1 The *TRG command is included solely for compliance with IEEE-488.2. The *TRG command has no effect on the instrument.

3.4.14.2 The syntax for the *TRG command is

*TRG

3.4.15 *WAI Command

3.4.15.1 The *WAI command is similar in effect to the *OPC command. Upon receipt of the *WAI command, the instrument will not process any new commands or queries until all pending operations have completed. Unlike the *OPC command, no Standard Event Status Register bits are set as a result of executing the *WAI command.

3.4.15.2 The syntax for the *WAI command is

*WAI

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3.5 Operational Commands

3.5.1 Operational Command Summary

3.5.1.1 The 6056 uses the SCPI syntax rules for forming operational commands. The SCPI rules are described in Subsection 3.3.

3.5.1.2 The 6056 command set is comprised of seven subsystems. The subsystems, and the hardware affected, are summarized in Table 3-6.

Table 3-6, Attribute Vs. Command Cross-Reference

6056 Attribute	Command Subsystem
TCF 1 and 2 Filters	INPUT
LTD 1 and 2 thresholds	SENSE
Main 1/2 input connection	ROUTE
Main 1/2 output polarity	OUTPUT
Main 1/2 + Window output trigger connections	OUTPUT
Window Function selection	SENSE
Interrupt Condition selection	SENSE
Read interrupt state/cause	FETCH
Reset system	SYSTEM
Read errors	SYSTEM
Extended status registers	STATUS

3.5.2 SYSTEM Command Subsystem

3.5.2.1 SYSTEM Command Tree

3.5.2.1.1 The SYSTEM Command Tree is as follows:

```
SYSTem
      :PRESet
      :ERRor?
      :VERSion?
```

3.5.2.2 SYSTem:PRESet Command

3.5.2.2.1 The "SYSTEM:PRESET" command does the following:

a) Places the 6056 hardware in the Home State (see Table 3-1)

b) Clears the input and output buffers

c) Clears the status structures and error queue

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3.5.2.2.2 In short, the "SYSTEM:PRESET" command places the 6056 into the power-up state. The only exception to this is the PON bit (bit 7) of the Standard Event Status Register is clear after executing the "SYSTEM:PRESET" command.

3.5.2.2.3 The "SYSTEM:PRESET" command has no query form. This is a command only.

3.5.2.2.4 The syntax for the "SYSTEM:PRESET" command is

SYSTEM:PRESET

3.5.2.3 SYSTem:ERRor? Query

3.5.2.3.1 The 6056 maintains a queue of errors. Each time an error is discovered, such as a command syntax error, an error is placed in the error queue.

3.5.2.3.2 The 6056 maintains a queue of up to 10 errors. If more than 10 errors are placed on the queue, the Device-Dependent Error bit (DDE, bit 3) is set in the Standard Event Status Register. An attempt to place more than 10 errors in the queue also results with the message

-350,"Queue overflow"

being placed last on the error queue.

3.5.2.3.3 Every response to the "SYSTEM:ERROR?" query uses the form

<error number>,"<error message>"

where

<error number> is in the range -1000 to 0; and,
<error message> is a descriptive string enclosed in double quotes.

3.5.2.3.4 The error codes and associated error messages are shown in Table 3-7. The table also shows which Standard Event Status Register bit will be set when the error is discovered.

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Table 3-7, Error Code and Message Summary

Error	Error Text	ESR Bit
0	"No error"	-
-100	"Command error;<additional explanation>"	CME
-103	"Invalid separator;Command separator expected near '<s>'"	CME
-104	"Data type error;Error detected near '<s>'"	CME
-200	"Execution error;Trigger ON request with no TTLTRG line"	EXE
-222	"Data out of range;<additional explanation>"	EXE
-330	"Self-test failed;<self-test failure>"	DDE
-350	"Queue overflow"	DDE
-400	"Query error;<additional explanation>"	QYE
-410	"Query interrupted;<additonal explanation>"	QYE

3.5.2.3.5 Many of the errors in Table 3-7 include additional text to clarify the error condition. For example, the "Command error" error message will be followed by additional text, such as

Numeric data expected near '<s>'

where <s> will hold the text scanned by the parser when the error was detected.

3.5.2.3.6 The SYSTEM:ERROR? query is used to read the first (oldest) error from the error queue. After an error is read, it is removed from the queue. When no errors remain in the queue, the response

0,"No error"

will be returned.

3.5.2.3.7 Whenever the DDE, CME, or QYE bits are set in the Standard Event Status Register, the "SYSTEM:ERROR?" command is used to read the cause of the error.

3.5.2.4 SYSTem:VERSion? Query

3.5.2.4.1 The "SYSTEM:VERSION?" query reads the SCPI revision to which this instrument complies. There are a few non-SCPI command sequences, so this instrument is not strictly compliant. When the "SYSTEM:VERSION?" query is received, the 6056 responds by placing the string

0.0

in the output queue.

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3.5.3 INPUT Command Subsystem

3.5.3.1 INPUT Command Tree

3.5.3.1.1 The INPUT Command Tree is as follows:

```
INPut
        :FILTer<N>
                [ :LPASs ]
                        [ :STATe ]      ON | OFF | 1 | 0

                          :TIME         <filter time>
```

3.5.3.1.2 The FILTer<N> may be replaced by FILTer1 for Time Constant Filter (TCF) 1, and by FILTer2 for TCF 2.

3.5.3.2 INPut:FILTer<N>:STATe Command

3.5.3.2.1 The "INPut:FILTER<N>:STATE" command (and its variants) enable or disable the selected filter.

3.5.3.2.2 When a filter state changes from ON to OFF the filter capacitors are discharged in a sequence which requires approximately 120 milliseconds to execute.

3.5.3.2.3 The query form of the command is one of the following:

```
INPUT:FILTER<N>?
INPUT:FILTER<N>:STATE?
```

The query returns an <NR1> format, with "0" indicating the filter is disabled, and "1" indicating the filter is enabled.

3.5.3.2.4 The following are examples and descriptions of the "INPUT:FILTER<N>:STATE" command:

```
INPUT:FILTER1:LPASS:STATE ON      Turn TCF 1 on
INPUT:FILTER2:STATE OFF           Turn TCF 2 filter off
INUT:FILT1 0                      Turn TCF 1 filter off
INPUT:FILT2 ON                    Turn TCF 2 filter on
```

3.5.3.3 INPut:FILTer<N>:TIME Command

3.5.3.3.1 The "INPUT:FILTER<N>:TIME" command sets the time-constant for the selected filter.

3.5.3.3.2 The syntax for this command is

```
INPut:FILTer<N>:TIME <filter time>
```

where

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<filter time> is an NR2 or NR3 number in the range 1.6 x 10^{-6} to 4096.0 x 10^{-6} seconds (1.6 µs to 4096.0 µs). The value 0.0 is accepted, and will cause the instrument to set the filter state to OFF.

3.5.3.3.3 Filter time constants programmed in the range 1.6E-6 to 409.6E-6 will be programmed with a resolution of 1.6 microseconds. Filter time constants greater than 409.6E-6 and less than or equal to 4096.0E-6 will be programmed with a resolution of 16 microseconds.

3.5.3.3.4 Time constants are rounded to the nearest multiple of the selected resolution. For example, if a time constant of 3.5 microseconds is specified, the programmed time constant will be 3.2 microseconds. Similarly, if a time constant of 3210 microseconds is specified, the programmed time constant will be 3216 microseconds.

3.5.3.3.5 When the time constant is changed for a filter which is already ON, the filter capacitors are discharged in a sequence which requires approximately 120 milliseconds to execute.

3.5.3.3.6 The query form of the command is

INPUT:FILTER<N>:TIME?

The instrument responds with an <NR3> format reply.

3.5.3.3.7 The following are examples and descriptions of the "INPUT:FILTER<N>:TIME" command:

INPUT:FILTER1:LPASS:TIME 32.0E-6	Set TCF 1 to 32 µs
INPUT:FILT2:TIME 400.0E-6	Set TCF 2 to 400 µs

3.5.4 ROUTe Command Subsystem

3.5.4.1 ROUTe Command Tree

3.5.4.1.1 The ROUTe Command Tree is as follows:

ROUTe
:CLOSe <channel-list>

3.5.4.2 ROUTe:CLOSe Command

3.5.4.2.1 The "ROUTE:CLOSE" command is used to connect either the LTD inputs or a TTLTRG line to the MAIN outputs.

3.5.4.2.2 The syntax for the "ROUTE:CLOSE" command is

ROUTe:CLOSe <channel> [, <channel>]

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where

<channel> is an ASCII at sign (@) followed by a number. The valid <channel> values are shown in Table 3-8.

Table 3-8, ROUTe Command Channel Description

Channel	Description
@1	Connect LTD 1 input to MAIN 1 output
@2	Connect LTD 2 input to MAIN 2 output
@10	Connect TTLTRG0 to MAIN 1
@11	Connect TTLTRG1 to MAIN 1
@12	Connect TTLTRG2 to MAIN 1
@13	Connect TTLTRG3 to MAIN 1
@14	Connect TTLTRG4 to MAIN 1
@15	Connect TTLTRG5 to MAIN 1
@16	Connect TTLTRG6 to MAIN 1
@17	Connect TTLTRG7 to MAIN 1
@20	Connect TTLTRG0 to MAIN 2
@21	Connect TTLTRG1 to MAIN 2
@22	Connect TTLTRG2 to MAIN 2
@23	Connect TTLTRG3 to MAIN 2
@24	Connect TTLTRG4 to MAIN 2
@25	Connect TTLTRG5 to MAIN 2
@26	Connect TTLTRG6 to MAIN 2
@27	Connect TTLTRG7 to MAIN 2

3.5.4.2.3 When a ROUTe command is executed for a selected output, any existing connection to the output is broken before the specified input is connected.

3.5.4.2.4 The command allows one or two channels to be programmed. If two channels are programmed, and both affect the same output, only the second channel will be connected when the command is completed. That is, if the command

ROUTE:CLOSE @2,@23

is sent, TTLTRG3 will be connected to the MAIN 2 output after the command is executed.

3.5.4.2.5 The query form of the command is

ROUTE:CLOSE?

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3.5.4.2.6 The instrument responds with an ASCII format reply in the form

<MAIN 1>,<MAIN 2>

where

<MAIN 1> will be the input channel connected to MAIN 1 (@1, @10, @11, ..., @17)

<MAIN 2> will be the input channel connected to MAIN 2 (@2, @20, @21, ..., @27)

3.5.5 OUTPut Command Subsystem

3.5.5.1 OUTPut Command Tree

3.5.5.1.1 The OUTPut Command Tree is as follows:

```
OUTPut
      :POLarity<N>          NORMal | INVerted
      :TRIGger<N>
            :STATe          ON | OFF | 1 | 0
            :TTLTrg<x>
```

3.5.5.2 OUTPut:POLarity<N> Command

3.5.5.2.1 The "OUTPUT:POLARITY<N>" command is used to select the polarity of the MAIN 1 and MAIN 2 outputs. The MAIN 1 output polarity is programmed by specifying "POLarity1", while the MAIN 2 output is programmed by specifying "POLarity2".

3.5.5.2.2 The syntax for this command is

OUTPUT:POLARITY<N> NORMAL | INVERTED

3.5.5.2.3 The query form of this command is

OUTPUT:POLARITY<N>?

3.5.5.2.4 The instrument will respond with an <NR1> format reply. The reply will be "0" if the specified polarity is NORMAL, or "1" if the polarity is INVERTED.

3.5.5.2.5 Examples and descriptions of valid commands are shown below:

```
OUTPUT:POL1 NORM          -- MAIN 1 polarity is normal
OUTPUT:POL2 INVERTED      -- MAIN 2 polarity is
                             inverted
Outp:Polarity1 Inv        -- MAIN 1 polarity is
                             inverted
```

3.5.5.3 OUTPut:TRIGger<N>:STATe Command

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3.5.5.3.1 The "OUTPUT:TRIGGER<N>:STATE" command is used to connect or disconnect one of the MAIN 1, MAIN 2, or WINDOW outputs to one of the VXI TTLTRG lines.

3.5.5.3.2 The MAIN 1 output is connected or disconnected if "TRIGGER1" is specified. The MAIN 2 output is connected or disconnected if "TRIGGER2" is specified. The WINDOW output is connected or disconnected if "TRIGGER3" is specified.

3.5.5.3.3 The selected output is connected to the TTLTRG line specified by the last "OUTPUT:TRIGGER<n>:TTLTRG<x>" command. If no "OUTPUT:TRIGGER<N>:TTLTRG<x>" commands have been received since the last power-up cycle, "*RST" command, or "SYSTEM:PRESET" command, an error will result. This error will be error -200 as described in Table 3-7.

3.5.5.3.4 The syntax for this command is

OUTPUT:TRIGGER<N>:STATE ON | OFF

where

<N> is a number in the range 1 to 3 inclusive

3.5.5.3.5 The query form of this command is

OUTPUT:TRIGGER<N>:STATE?

3.5.5.3.6 The instrument will respond with an <NR1> format reply. The reply will be "0" if the output is disconnected, or "1" if the output is connected to a TTLTRG line.

3.5.5.3.7 Examples and descriptions of valid commands are shown below:

OUTPUT:TRIGGER1:STATE ON	-- connects MAIN 1 to last specified TTLTRG line
OUTPUT:TRIGGER2:STATE OFF	-- disconnects MAIN 2 from all TTLTRG lines
Outp:Trig3:Stat OFF	-- disconnects WINDOW from all TTLTRG lines

3.5.5.4 OUTPut:TRIGger<N>:TTLTrg<X> Command

3.5.5.4.1 The "OUTPUT:TRIGGER<N>:TTLTRG<X>" command is used to select one the VXI TTLTRG lines to which the specified output will be connected.

3.5.5.4.2 The MAIN A output is selected if "TRIGGER1" is specified. The MAIN B output is selected if "TRIGGER2" is specified. The WINDOW output is selected if "TRIGGER3" is specified.

3.5.5.4.3 Upon power-up, and after receipt of either the "SYSTEM:PRESET" command or the "*RST" command, the MAIN 1, MAIN 2, and WINDOW outputs are

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disconnected from the TTLTRG lines. The "OUTPUT:TRIGGER<N>:STATE" command **MAY NOT BE USED** until an "OUTPUT:TRIGGER<N>:TTLTRG<X>" command is received by the 6056 for output <N>.

3.5.5.4.4 Each output may be connected to at most one TTLTRG line at any one time. If the state of the "OUTPUT:TRIGGER<N>" is ON and a "OUTPUT:TRIGGER<N>:TTLTRG<X>" command is received, the output will be disconnected from its present TTLTRG line before it is connected to the new TTLTRG line.

3.5.5.4.5 Two outputs may NOT be connected to the same TTLTRG line. A current connection will be broken before the new connection is made. For example, if MAIN 1 is currently connected to TTLTRG3, and the command

"OUTPUT:TRIGGER2:TTLTRG3"

is received, MAIN 1 will be disconnected from TTLTRG3 before MAIN 2 is connected. In this example, the state of TRIGGER1 will be set to OFF.

3.5.5.4.6 The syntax for this command is

OUTPUT:TRIGGER<N>:TTLTRG<X>

where

<N> is a number in the range 1 to 3 inclusive
<X> is a number in the range 0 to 7 inclusive

3.5.5.4.7 The query form for this command is

OUTPUT:TRIGGER<N>?

The instrument will reply with a an <NR1> format reply:

0	-- output is/will be connected to TTLTRG0
1	-- output is/will be connected to TTLTRG1
2	-- output is/will be connected to TTLTRG2
3	-- output is/will be connected to TTLTRG3
4	-- output is/will be connected to TTLTRG4
5	-- output is/will be connected to TTLTRG5
6	-- output is/will be connected to TTLTRG6
7	-- output is/will be connected to TTLTRG7
-1	-- no TTLTRG line has been established (e.g., after power-up)

3.5.5.4.8 Note this query returns the TTLTRG line connection to be made when the next "OUTPUT:TRIGGER<N>:STATE ON" command is received. It does NOT return the current ON/OFF state of the TRIGGER<N> output. The present ON/OFF state is returned using the query "OUTPUT:TRIGGER<N>:STATE?".

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3.5.5.4.9 Examples and descriptions of valid commands are shown below. The examples are shown in a sequence of operations to show the effect one command may have on the next.

OUTPUT:TRIGGER1:TTLTRG3	-- establishes that MAIN 1 will be connected to TTLTRG3
OUTPUT:TRIGGER1:STATE ON	-- connects MAIN 2 to TTLTRG3
Output:Trig3:TTLT3	-- establishes that WINDOW will be connected to TTLTRG3. Disconnects MAIN A from TTLTRG3
Output:Trig3:STATE ON	-- connects WINDOW to TTLTRG3
Output:Trig3:TTLTRG5	-- disconnects WINDOW from TTLTRG3. Connects WINDOW to TTLTRG5.
Output:Trig3:STATE OFF	-- disconnects WINDOW from TTLTRG5.
Outp:Trig3:Stat OFF	-- disconnects WINDOW from all TTLTRG lines

3.5.6 SENSe Command Subsystem

3.5.6.1 SENSe Command Tree

3.5.6.1.1 The SENSe Command Tree is as follows:

```
[ SENSe ]
      :VOLTage
            :DC
                  :REFerence<N> <threshold>

      :FUNCTION      <window function>
      :INTerrupt     <interrupt condition>
            :STATE   ON | OFF | 1 | 0
            :EVA     <event A value>
            :EVB     <event B value>
```

3.5.6.2 SENSe:VOLTage:DC:REFerence<N> Command

3.5.6.2.1 The "SENSE:VOLTAGE:DC:REFERENCE<N>" command is used to program the threshold for the LTD inputs. If "REFERENCE1" is specified, the threshold for LTD 1 is programmed; if "REFERENCE2" is specified, the threshold for LTD 2 is programmed.

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3.5.6.2.2 The LTD inputs to the card are disabled while the thresholds are being programmed. This may generate spurious interrupts to the card if the card interrupt have been enabled (see the "SENSE:INTERRUPT:STATE" command). The card interrupt should be disabled before the threshold is programmed.

3.5.6.2.3 The syntax for this command is

[SENSE:]VOLTAGE:DC:REFERENCE<N> <threshold>

where

<N> is either 1 or 2
<threshold> is a voltage value in the range -40.0 to +40.0.

3.5.6.2.4 The SENSE keyword is optional. The command

VOLTAGE:DC:REFERENCE1 32.0

is equivalent to

SENSE:VOLTAGE:DC:REFERENCE1 32.0

3.5.6.2.5 The query form of the command is

SENSE:VOLTAGE:DC:REFERENCE<N>?

The 6056 will respond with a reply using the <NR2> format.

3.5.6.2.6 Examples and descriptions of valid commands are shown below:

SENSE:VOLTAGE:DC:REF1 2.04	-- programs LTD A threshold to 2.04 Volts
VOLT:DC:REF2 -24.8	-- programs LTD B threshold to -24.8 Volts
VOLT:DC:REF2?	-- returns the present LTD threshold (e.g. "-24.8")

3.5.6.3 SENSe:FUNCtion Command

3.5.6.3.1 The "SENSE:FUNCTION" command is used to select the logical function for the WINDOW output, and the polarity of the LTD 1 and LTD 2 inputs to the logical function.

3.5.6.3.2 The syntax for this command is

[SENSE:]FUNCTION <window function>

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where

<window function> is one of the following:

"LOW"
"OFF"
"<A state> AND <B state>"
"<A state> OR <B state>"
"<A state> NAND <B state>"
"<A state> NOR <B state>"
"<A state> EXOR <B state>"

<A state> is "A" or "NOT A", and specifies the polarity of LTD 1
<B state> is "B" or "NOT B", and specifies the polarity of LTD 2

3.5.6.3.3 The "LOW" and "OFF" functions are equivalent. When either of these are selected, the WINDOW output will be continuously low.

3.5.6.3.4 The A and/or B input to the window function may be inverted by preceding the input name with the "NOT" keyword.

3.5.6.3.5 The WINDOW output is produced based on the LTD 1 (A) and LTD 2 (B) inputs. The WINDOW output state is shown in Table 3-9.

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Table 3-9. WINDOW Output Level Generation

Input AB	Function	WINDOW Output
00	LOW	0
01		0
10		0
11		0
00	AND	0
01		0
10		0
11		1
00	OR	0
01		1
10		1
11		1
00	NAND	1
01		1
10		1
11		0
00	NOR	1
01		0
10		0
11		0
00	EXOR	0
01		1
10		1
11		0

3.5.6.3.6 The SENSE keyword is optional.

3.5.6.3.7 The query form of the command is

SENSE:FUNCTION?

3.5.6.3.8 The query will return a string which reflects the programmed window function. The returned string will not necessarily be identical to the programmed value; it will be logical equivalent. The card uses inverters for the A and B inputs and one of the functions (LOW, AND, OR, or EXOR) to produce the programmed logical function. If the command

SENSE:FUNCTION "A NOR B"

is programmed, and the function query is sent, the instrument will respond with

NOT A AND NOT B

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3.5.6.3.9 Examples of valid commands are shown below:

SENSE:FUNCTION "LOW"
Sense:Function "not A and B"
Function "A EXOR not B"

3.5.6.4 SENSe:INTerrupt Command

3.5.6.4.1 The "SENSE:INTERRUPT" command is used to select the logical combination and polarity LTD 1 and LTD 2 inputs which generate an interrupt to the card.

3.5.6.4.2 The interrupt to the card will not be generated until it is enabled. The interrupt is enabled with the "SENSE:INTERRUPT:STATE" command.

3.5.6.4.3 The syntax for this command is

[SENSE:]INTERRUPT <interrupt condition>

where

<interrupt condition> is one of the following:

"A"
"B"
"NOT A"
"NOT B"
"A OR B"
"NOT A OR B"
"A OR NOT B"
"NOT A OR NOT B"
"A AND B"
"NOT A AND B"
"A AND NOT B"
"NOT A AND NOT B"

3.5.6.4.4 "A" specifies the LTD 1 input is to be applied using normal polarity. "NOT A" specifies the LTD 1 input is to be applied using inverted polarity.

3.5.6.4.5 "B" specifies the LTD 2 input is to be applied using normal polarity. "NOT B" specifies the LTD 2 input is to be applied using inverted polarity.

3.5.6.4.6 The SENSE keyword is optional.

3.5.6.4.7 The query form of the command is

SENSE:INTERRUPT?

3.5.6.4.8 The query will return a string which reflects the programmed interrupt condition. The string will be in all capital letters, with a single ASCII space between each of the words in the interrupt condition. For example, if the string

SENSE:INTERRUPT "A anD Not b"

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is programmed, and the query is sent, the instrument will respond with

A AND NOT B

3.5.6.4.9 Examples of valid commands are shown below:

SENSE:INTERRUPT "not A or B"
Sense:Int "A"
Interrupt "NOT B"

3.5.6.5 SENSe:INTerrupt:STATe Command

3.5.6.5.1 The "SENSE:INTERRUPT:STATE" command is used to enable or disable the generation of interrupts from the 6056 SCM.

3.5.6.5.2 The interrupt MUST be enabled for a VXI interrupt to be generated when the SENSE:INTERRUPT conditions are met.

3.5.6.5.3 When the interrupt is enabled and the interrupt conditions are met, the 6056 SCM generates a VXI user-defined event interrupt. The format of the status ID word passed to the commander during the interrupt acknowledge cycle is shown in Figure 3-1. The value of bits 8 through 13 is determined by the values programmed with the "SENSE:INTERRUPT:EVA" and "SENSE:INTERRUPT:EVB" commands.

Figure 3-1. User-Defined Event Status Word Format

Bit #

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	User-Defined (EVA/EVB)						Sender's Logical Address							

3.5.6.5.4 Once a VXI user-defined event is generated by the card, further interrupts are disabled until the SCM receives one of the following commands:

SENSE:INTERRUPT:STATE ON
FETCH:INTERRUPT?

3.5.6.5.5 The "SENSE:INTERRUPT:STATE" command clears bit 3 (DSB) of the Status Byte. The Status Byte is read with either a VXI READ STB command or the IEEE-488.2 "*STB?" query prior to issuing the "SENSE:INTERRUPT:STATE" command if the DSB bit of the status byte is of interest.

3.5.6.5.6 The syntax for this command is

[SENSE:]INTERRUPT:STATE ON | OFF | 1 | 0

3.5.6.5.7 The SENSE keyword is optional.

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3.5.6.5.8 The query form of the command is

SENSE:INTERRUPT:STATE?

The query will return the string "0" if the interrupt is disabled, or "1" if the interrupt is enabled.

3.5.6.5.9 Examples of valid commands are shown below:

SENSE:INTERRUPT:STATE ON
Sense:Interrupt:Stat 1
Int:State ON

3.5.6.6 SENSe:INTerrupt:EVA Command

3.5.6.6.1 The "SENSE:INTERRUPT:EVA" command (along with the "SENSE:INTERRUPT:EVB" command) is used to program the value returned in bits 8 through 13 of the VXI user-defined event generated by the SCM.

3.5.6.6.2 The syntax for this command is

[SENSE:]INTERRUPT:EVA <event A value>

where

<event A value> is in the range 1 through 63.

3.5.6.6.3 The <event A value> will be placed in bits 8 through 13 of the user-defined event status word if LTD 1 is the sole cause of the interrupt. If both LTD 1 and LTD 2 cause the interrupt, the value in bits 8 through 13 of the user-defined event status word will contain the bitwise OR of the <event A value>, and the <event B value> which is programmed with the SENSE:INTERRUPT:EVB command.

3.5.6.6.4 As an example, assume the <event A value> is programmed to 3 and the <event B value> is programmed to 4. Table 3-10 shows the value which will be returned in bits 8 through 13 of the user-defined event status word.

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Table 3-10, Example Using EVA and EVB Event Values

Interrupt Condition	A (LTD #1)	B (LTD #2)	Bits 8-13 of Event
"A"	1	X	3
"B"	X	1	4
"NOT A"	0	X	3
"NOT B"	X	0	4
"A OR B"	1	0	3
"A OR B"	0	1	4
"NOT A OR B"	0	0	3
"NOT A OR B"	1	1	4
"A OR NOT B"	1	1	3
"A OR NOT B"	0	0	4
"NOT A OR NOT B"	0	1	3
"NOT A OR NOT B"	1	0	4
"A AND B"	1	1	7
"NOT A AND B"	0	1	7
"A AND NOT B"	1	0	7
"NOT A AND NOT B"	0	0	7

Notes:
<event A value> = 3
<event B value> = 4
X = don't care value

3.5.6.6.5 The default value for <event A value> is 1.

3.5.6.6.6 The SENSE keyword is optional.

3.5.6.6.7 The query form of the command is

SENSE:INTERRUPT:EVA?

3.5.6.6.8 The query will return an <NR1> format reply which reflects the programmed <event A value>.

3.5.6.6.9 Examples of valid commands are shown below:

SENSE:INTERRUPT:EVA 32
Sense:Int:Eva 18
Interrupt:EVA 8

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3.5.6.7 SENSe:INTerrupt:EVB Command

3.5.6.7.1 The "SENSE:INTERRUPT:EVB" command is used (along with the "SENSE:INTERRUPT:EVA" command) to program the value returned in bits 8 through 13 of the VXI user-defined event generated by the SCM.

3.5.6.7.2 The syntax for this command is

[SENSE:]INTERRUPT:EVB <event B value>

where

<event B value> is in the range 1 through 63.

3.5.6.7.3 The <event B value> will be placed in bits 8 through 13 of the user-defined event status word if LTD 2 is the sole cause of the interrupt. If both LTD 1 and LTD 2 cause the interrupt, the value in bits 8 through 13 of the user-defined event status word will contain the bitwise OR of the <event A value> and the <event B value>.

3.5.6.7.4 As an example, refer to Table 3-10.

3.5.6.7.5 The default value for <event B value> is 2.

3.5.6.7.6 The SENSE keyword is optional.

3.5.6.7.7 The query form of the command is

SENSE:INTERRUPT:EVB?

3.5.6.7.8 The query will return an <NR1> format reply which reflects the programmed <event B value>.

3.5.6.7.9 Examples of valid commands are shown below:

```
SENSE:INTERRUPT:EVB 16
Sense:Int:Evb 24
Interrupt:EVB 4
```

3.5.7 FETCh Command Subsystem

3.5.7.1 FETCh Command Tree

3.5.7.1.1 The FETCh Command Tree is as follows:

```
FETCh
      [ :INTerrupt ]?
```


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3.5.7.2 FETCh:INTerrupt? Query

3.5.7.2.1 The "FETCh:INTerrupt?" query is used to read the states of the A and B inputs which were recorded at the point the last "SENSE:FUNCTION" interrupt was generated. This is typically done after the 6056 has interrupted the controller, and the controller has determined the interrupt was caused due to the "SENSE:FUNCTION" interrupt (e.g, the VXI user-defined event interrupt is received OR by reading bit 3 of the Status Byte Register).

3.5.7.2.2 The syntax for this query is

FETCH[:INTERRUPT]?

3.5.7.2.3 The INTERRUPT keyword is optional. The query

FETCH?

is equivalent to

FETCH:INTERRUPT?

3.5.7.2.4 The 6056 responds to the "FETCH:INTERRUPT?" query by returning an <NR1> format number in the range "0" to "7". This number is a bit-weighted as shown in Table 3-11.

Table 3-11, FETCH:INTERRUPT? Reply Bit Assignment

Bit #	Weight	Description
0	1	State of input A (or NOT A) when interrupted
1	2	State of input B (or NOT B) when interrupted
2	4	Set to 1 only if card was interrupted

3.5.7.2.5 Table 3-11 shows the state of the A and B inputs are captured at the time of the interrupt in bits 0 and 1 of the reply. If the "SENSE:INTERRUPT" condition inverts an input, the INVERTED state is captured and sent in the reply. That is, if the interrupt condition is "A and NOT B", and the card detects A is high and B is low, the reply from the card in response to the "FETCH?" command will be "7".

3.5.7.2.6 The "FETCH:INTERRUPT?" query clears bit 3 (DSB) of the Status Byte. The Status Byte should be read with either a VXI READ STB command or the IEEE-488.2 "*STB?" query prior to issuing the "FETCH:INTERRUPT?" query, if the DSB bit of the status byte is of interest.

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3.5.8 STATUS Command Subsystem

3.5.8.1 STATUS Command Tree

3.5.8.1.1 The STATUS Command Tree is as follows:

```
STATus
        :OPERation
                [:EVENt]?
                :CONDition?
                :ENABle
                :ENABle?

        :QUEStionable
                [:EVENt]?
                :CONDition?
                :ENABle
                :ENABle?

        :PRESet
```

3.5.8.2 The STATUS subsystem is provided solely for compliance with the SCPI standard. This instrument does not use the SCPI status registers which are controlled by these commands, so these commands have no effect on the operation of the instrument.

3.6 IEEE-488.2 Status Reporting Implementation

3.6.1 Introduction

3.6.1.1 The IEEE-488.2 Standard defines a model for status reporting. The 6056 SCM adheres to this model. The model is briefly described in this section for ease of reference. For a more comprehensive discussion, refer to Section 11 of the IEEE-488.2 standard.

3.6.1.2 In short, the IEEE-488.2 defines a Status Byte Register, a Standard Event Status Register, a Standard Event Status Enable Register, and a Service Request Enable Register. The relationship between these are described in the subsequent paragraphs.

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3.6.2 Standard Event Status Register

3.6.2.1 The Standard Event Status Register tracks the history of instrument events. The bit assignments for the Standard Event Status Register are (from Table 3-3).

Bit #	Weight	Name	Description
0	1	OPC	Operation Complete
1	2	RQC	Request Control (always 0)
2	4	QYE	Query Error
3	8	DDE	Device Dependent Error
4	16	EXE	Execution Error
5	32	CME	Command Error
6	64	URQ	User Request (always 0)
7	128	PON	Power On

3.6.2.2 As conditions become set, they are latched into this register. The conditions are cleared only when:

a) The "*ESR?" command is received
b) The "*CLS" command is received
c) The "SYSTEM:PRESET" command is received
d) Power-up (bit 7, PON, is set)

3.6.2.3 The bits of the Standard Event Status Register are described in the following subparagraphs.

3.6.2.3.1 Bit 7 - PON, Power On. This bit is set when the off-to-on transition occurs in the SCM (VXI) power supply.

3.6.2.3.2 Bit 6 - URQ, User Request. This bit is set when the device-dependent User Request Control has been activated. For the 6056, this bit is always clear.

3.6.2.3.3 Bit 5 - CME, Command Error. This bit is set when one of the following events has occurred:

a) A syntax error has been detected by the parser

b) A semantic error, such as an unrecognized header, was detected by the parser

c) A Group Execute Trigger (GET) was placed into the input buffer inside of a program message (as defined in IEEE 488.2)

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3.6.2.3.4 Bit 4 - EXE, Execution Error. This bit is set when:

a) A program data element is outside the device's legal input range

b) A valid program message (command) was not executed due to some device condition

3.6.2.3.5 Bit 3 - DDE, Device-Specific Error. This bit is set by the 6056 only when one of two events has occurred:

a) Self-test has failed

b) The error queue has overflowed

3.6.2.3.6 Bit 2 - QYE, Query Error. This bit is set when either:

a) An attempt is made to read data from the output queue when no output is present or pending

b) Data in the output queue has been lost. For example, sending a query without reading the response

3.6.2.3.7 Bit 1 - RQC, Request Control. This bit is set when the device is requesting to become the active controller in charge. For the 6056, this bit is always 0.

3.6.2.3.8 Bit 0 - OPC, Operation Complete. This bit is generated in response to an "*OPC" command. This bit is set after all selected pending operations have completed. This bit may be used to ensure synchronization with the device.

3.6.2.4 The present value of the Standard Event Status Register is read using the IEEE-488.2 "*ESR?" query. The Standard Event Status Register is cleared after it is read by this query.

3.6.3 Standard Event Status Enable Register

3.6.3.1 The Standard Event Status Enable Register enables one or more of the bits in the Standard Event Status Register to set the Event Summary Bit (ESB, bit 5) of the Status Byte Register. The ESB bit is set high when one or more of the enabled bits of the Standard Event Status Register are high. The ESB bit is defined as:

(ESR bit 0 AND ESE bit 0) OR
(ESR bit 1 AND ESE bit 1) OR
(ESR bit 2 AND ESE bit 2) OR
(ESR bit 3 AND ESE bit 3) OR
(ESR bit 4 AND ESE bit 4) OR
(ESR bit 5 AND ESE bit 5) OR
(ESR bit 6 AND ESE bit 6) OR
(ESR bit 7 AND ESE bit 7)

Where

ESR = Standard Event Status Register
ESE = Standard Event Status Enable Register

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3.6.3.2 Conditions are enabled or disabled by sending the "*ESE" command to the instrument. For example, the command "*ESE 56" will enable the CME, EXE, or DDE conditions from the Standard Event Status Register. When any of these conditions is detected, the ESB bit is set in the Status Byte Register.

3.6.3.3 The presently programmed Standard Event Status Enable Register value is read with the "*ESE?" query.

3.6.4 Status Byte Register

3.6.4.1 The Status Byte Register maintains the current state of the instrument. The bit assignments for the Status Byte Register are (from Table 3-4):

Bit #	Weight	Name	Description
0	1	n/a	Not used, always 0
1	2	n/a	Not used, always 0
2	4	n/a	Not used, always 0
3	8	DSB	Device-specific status bit, set when the card has received an interrupt from the LTD A/B interrupt circuit
4	16	MAV	Message Available, set when a message is in the output queue
5	32	ESB	Event Status Bit, set when one or more *ESE enabled bits are set
6	64	MSS	Message Status Summary, set when one or more the *SRE enabled bits are set
7	128	n/a	Not Used

3.6.4.2 The bits of the Status Byte Register are described in the following subparagraphs.

3.6.4.2.1 Bit 7 - Device-dependent. This bit is not used and is always 0.

3.6.4.2.2 Bit 6 - MSS, Master Summary Status. This bit is set when one or more of the enabled status bits is set high. Status Byte Register bits are enabled via the Service Request Enable Register by issuing the "*SRE" command. In short, MSS is defined as:

(STB bit 0 AND SRE bit 0) OR
(STB bit 1 AND SRE bit 1) OR
(STB bit 2 AND SRE bit 2) OR
(STB bit 3 AND SRE bit 3) OR
(STB bit 4 AND SRE bit 4) OR
(STB bit 5 AND SRE bit 5) OR
(STB bit 7 AND SRE bit 7)

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Where

STB = Status Byte Register
SRE = Service Request Enable Register

3.6.4.2.3 Bit 5 - ESB, Event Status Bit. This bit is set when one or more of the enable Standard Event Status Register bits is set.

3.6.4.2.4 Bit 4 - MAV, Message Available. This bit is set when the device's output queue is not empty. In short, when the MAV bit is set, the 6056 has a response for the controller to read.

3.6.4.2.5 Bit 3 - DSB, Device-dependent Status Bit. This bit is device-dependent. For the 6056, this bit is set when the card has received an interrupt generated by the conditions of the LTD 1 and/or LTD 2 inputs. The "SENSE:INTERRUPT" command is used to select and enable the card interrupt. The "SENSE:INTERRUPT:STATE" command and "FETCH:INTERRUPT?" query clear this bit.

3.6.4.2.6 Bit 2 - Device-dependent. This bit is not used and is always 0.

3.6.4.2.7 Bit 1 - Device-dependent. This bit is not used and is always 0.

3.6.4.2.8 Bit 0 - Device-dependent. This bit is not used and is always 0.

3.6.4.3 The present value of the Status Byte Register is read using the IEEE-488.2 "*STB?" query. The Status Byte Register value is also read using the VXI "READ STB" command ($CFFF_{16}$).

3.6.4.4 If the VXI Request True Event is enabled, a 0-to-1 transition of the MSS bit generates an interrupt. The 6056 will place a Request True Event in its Status/ID register in this case. The VXI Request True interrupt is enabled at power-on. It may be enabled or disabled via the VXI "Control Event" command.

3.6.4.5 If the VXI Request False Event is enabled, a 1-to-0 transition of the MSS bit generates an interrupt. The 6056 will place a Request False Event in its Status/ID register in this case. The VXI Request False interrupt is enabled at power-on. It may be enabled or disabled via the VXI "Control Event" command.

3.6.5 Service Request Enable Register

3.6.5.1 The Service Request Enable Register enables bits from the Status Byte Register. A 1 in an enabled bit position of the Status Byte Register will set Master Summary Status bit (MSS, bit 6) of the Status Byte Register.

3.6.5.2 Setting bit 6 of the Service Request Enable Register is allowed eventhough it has no meaning. Only bits 0 through 5, and bit 7, are meaningful in this register.

3.6.5.3 The Service Request Enable Register may be programmed with the "*SRE" command. The current value programmed for this register may be read with the "*SRE?" query.

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3.7 Input Message Format

3.7.1 Message Termination

3.7.1.1 All commands and queries must be terminated with one of the following:

a) ASCII line feed (hex_{16} 0A)

b) Sending the END BIT with the VXI Byte Available command on the last character of the command

c) Sending the END BIT with an ASCII line feed

3.7.2 Numeric Formats

3.7.2.1 Numeric formats may be any of three types as defined in the IEEE-488.2 standard: <NR1>, <NR2> or <NR3>. Any of the three formats are accepted by the 6056 for any command which expects a numeric parameter value.

3.7.2.2 The <NR1> format specifies an integer value. The general syntax for the <NR1> format is

[+ | -] <digits>

where

<digits> ::= one or more digits in the range 0 to 9

3.7.2.3 In addition to <NR1> format decimal numbers, the 6056 accepts numbers in base 2 (binary), base 8 (octal), or base 16 (hexadecimal).

(a) Binary numbers use the form:

#B<binary digits>

(b) Octal numbers use the form:

#Q<octal digits>

(c) Hexadecimal numbers use the form:

#H<hex digits>

where

<binary digits> is one or more digits which are either 0 or 1
<octal digits> is one or more digits in the range 0 to 7
<hex digits> is one or more digits in the range 0 to 9, or A to F

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3.7.2.4 The <NR2> format specifies a real value. The general syntax for the <NR2> format is

[+ | -] <digits> . <digits>

where

<digits> ::= one or more digits in the range 0 to 9

3.7.2.5 The <NR3> format specifies a real value using exponential format. The general syntax for the <NR3> format is

[+ | -] <digits> . <digits> E + | - <digits>

where

<digits> ::= one or more digits in the range 0 to 9

3.7.2.6 Examples of numbers are shown below:

```
132          -- <NR1> format number, decimal 132
-6           -- <NR1> format number, decimal -6
#B001001     -- binary format number, decimal 9
#Q000377     -- octal format number, decimal 255
#HFF         -- hexadecimal format number, decimal 255
24.6         -- <NR2> format number
-0.000001    -- <NR2> format number
-32.0E-6     -- <NR3> format number
```

3.8 Output Message Format

3.8.1 All responses from the 6056 will be terminated with an ASCII line feed. The VXI END bit will be set with the line feed.

3.8.2 All numeric responses will be in either <NR1>, <NR2>, or <NR3> format. Consult the individual command and query descriptions to determine which format will be used for the response messages from the SCM.

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SECTION 4 THEORY OF OPERATION

4.1 Introduction

4.1.1 This section describes the Theory of Operation for the Model 6056.

4.1.2 Integrated circuits (ICs) in the following circuit descriptions are designated by circuit references provided on the supporting simplified block and schematic diagrams. The IC designations employed in the following key circuit descriptions follow those found in the supplied schematics.

4.1.3 When an IC package contains more than one circuit, suffix letters are used to distinguish them (e.g., U1a). If it is necessary to identify a specific pin of an IC, the reference designator with a suffix letter is followed by a hyphen and the required pin number (e.g., U1a-1).

4.1.4 Functional Blocks

4.1.4.1 The 6056 contains two main functional blocks; the Level Threshold Detector Block and the Time Constant Filter Block. As both of these blocks are independent of each other, their theory of operation will be discussed separately below. The Time Constant Filters are controlled by the microprocessor, and the latter's operation is described in the Level Threshold Detector section along with the power supply description.

4.2 Theory Of Operation

4.2.1 Level Threshold Detector Block

4.2.1.1 The Level Threshold Detector Block consists of the following functional blocks:

a. Level Threshold Detector 1, 2 Block

b. Trigger Source Block

c. Window Block

d. Main Output Block

e. Interrupt Logic Block

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f. Microprocessor Block

g. VXI Interface Block

h. Power supplies

4.2.1.2 The functional relationship between the LTD blocks is illustrated in Figure 4-1. The LTD block is internally configured by the microprocessor in response to commands sent via the VXIbus. Once the unit is configured no further action is required of the user unless a change to the test parameters is required.

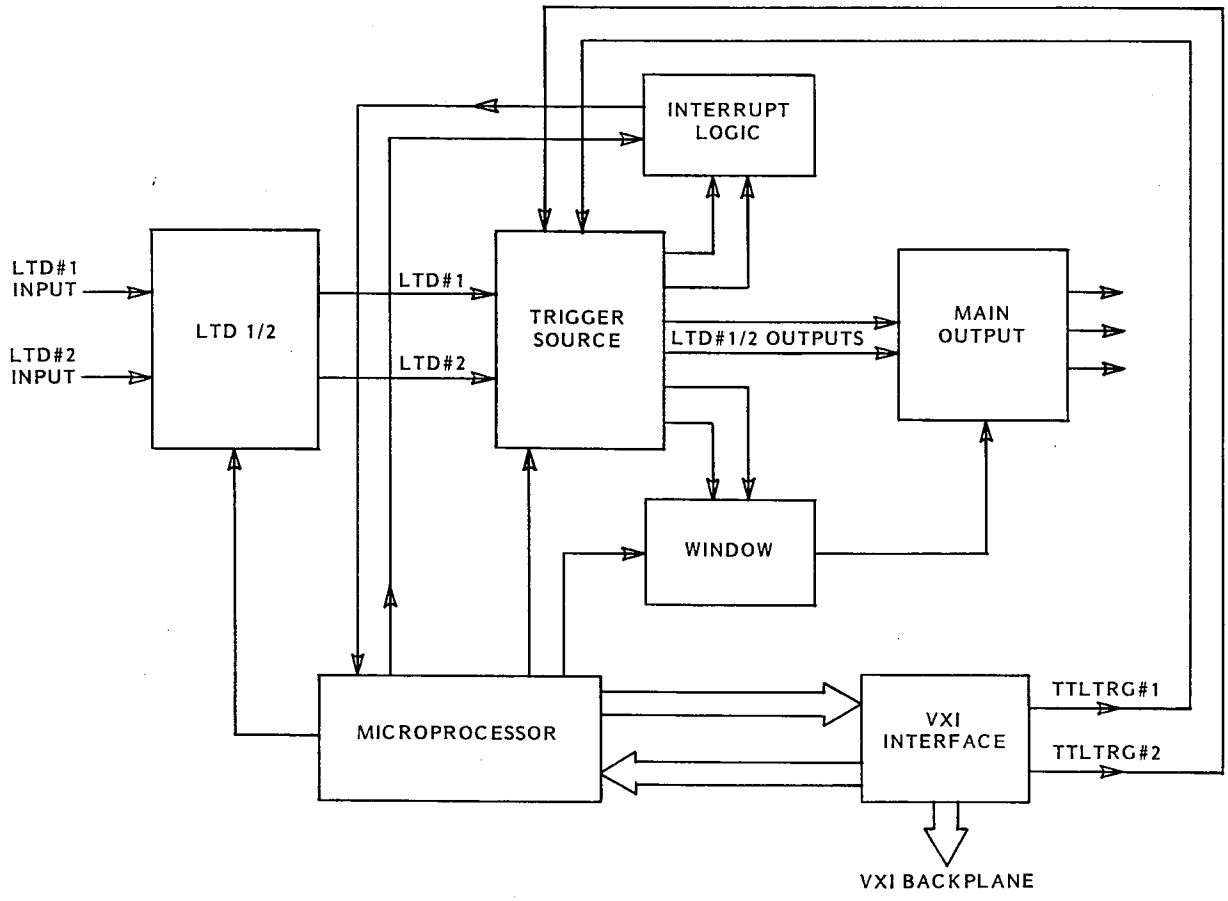


Figure 4-1, LTD Block Diagram

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4.2.2 Level Threshold Detector 1/2 Block

4.2.2.1 The Level Threshold Detector block consists of two identical level threshold detectors (LTD#1 and LTD#2). Refer to Figure 4-2 for block diagram. Each LTD is fully isolated from the remainder of the instrument and from each other.

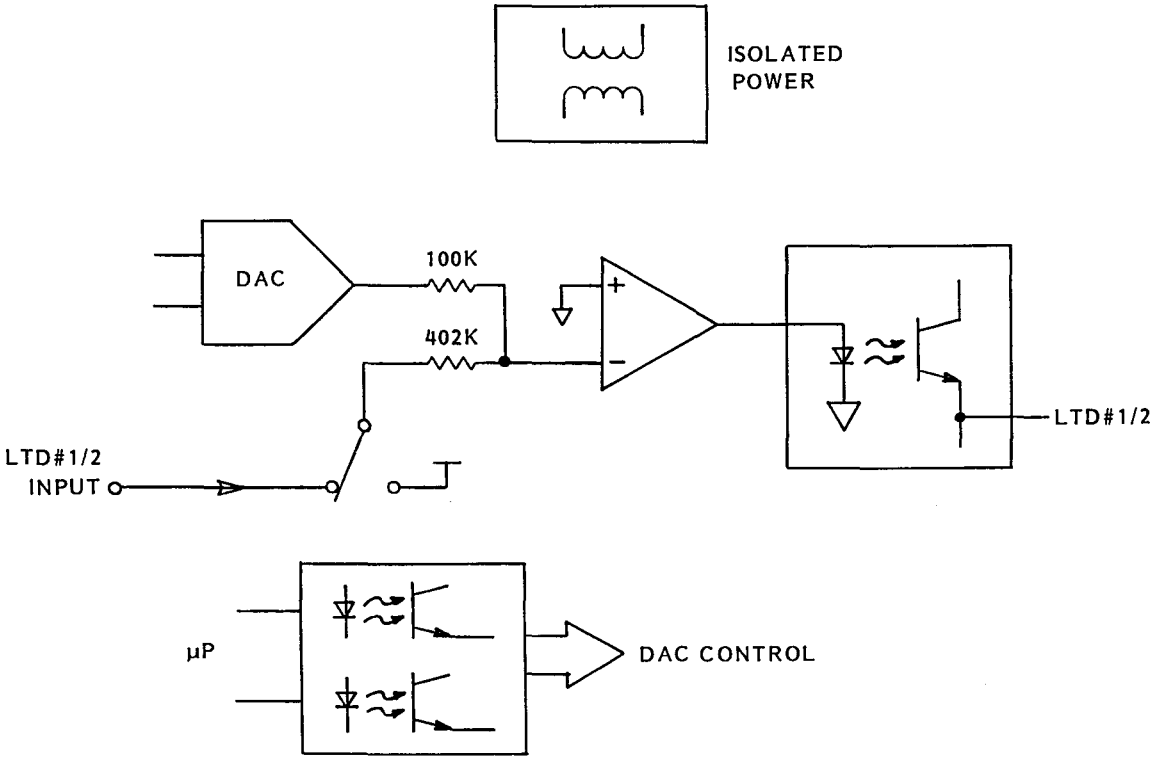


Figure 4-2, LTD 1/2 Block Diagram (One LTD Shown)

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4.2.2.2 LTD#1 and LTD#2 process signals applied at their respective inputs to produce digital pulses which are fed to the Trigger Source Block.

4.2.2.3 The input signals are applied to a comparator. The trigger threshold of the comparator is supplied by a DAC which has previously been configured by the microprocessor.

4.2.3 Level Threshold Detector 1/2 Block Circuit Description

4.2.3.1 The description will reference components used on LTD#1. The same description applies to LTD#2.

4.2.3.2 Relay K1 is controlled by latching data bit D11 into U81. Driver U75 provides the correct voltage to energize the relay. The operation of this relay allows signals applied on the input connector J200 pin 13,25 to route to the comparator. In its default state, +5V is applied to the comparator input for self-test purposes.

4.2.3.3 The 402kohm input impedance is provided by R23. This resistor is rated to withstand the maximum input voltage and power dissipation. C8 and C158 provide frequency compensation for the input signal path. Diodes D3 and D4 limit the voltage potential at the comparator input to approximately +/- 1V.

4.2.3.4 A summing junction is formed at the comparator input U46 pin 3. The junction is made from the signal input and the DAC output. The DAC output U45 pin 17 is connected to a 100kohm. This resistor creates an X5 attenuation for the input signal (i.e., a -10V output on the DAC will trigger a +40V minimum signal at the input).

4.2.3.5 The second signal input to the comparator U45 pin 2 is connected to R20 and R21. This resistor arrangement provides approximately +/-12mV of hysteresis at the comparator input or +/-60mV relative to the signal input.

4.2.3.6 The comparator output U45 pin 7 is an open collector which is pulled up to +5V. It is connected to U45 (a fast opto-coupler) which provides isolation from the next circuit. U45 output is disabled during changes of the DAC settings. The control line is derived from D0 at U86 pin 2.

4.2.3.7 R14 allows for offset adjustment of the comparator inputs.

4.2.3.8 R26 and R27 provide offset and gain adjustment for the DAC. Copious decoupling has been provided to reduce the impact of power supply noise.

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4.2.3.9 The 16-bit digital input to the DAC is supplied from serial shift registers U93 and U90. In conjunction with the quad d-type latch U89, data is serially shifted into the shift registers via dual opto-coupler U87. The latter provides isolation between the microprocessor interface and the LTD.

4.2.3.10 Isolation from the power plane is given by the DC-DC convertor U51. The voltage output from this device is +/-15V. Inductive and capacitive coupling has been provided to counteract any switch noise. The +/-15V is supplied to both the DAC and regulators U113 (LM7805) and U115 (LM7905). The regulators output +5V and -5V to provide isolated voltage to the comparator, shift registers and various resistors.

4.2.4 Trigger Source Block

4.2.4.1 The trigger source block is designed to route the signals from both LTD#1 and LTD#2, or the TTLTRG* inputs from the VXIbus backplane to the Main Output Block, the Window Block and the Interrupt Logic Block. Refer to Figure 4-3 for block diagram.

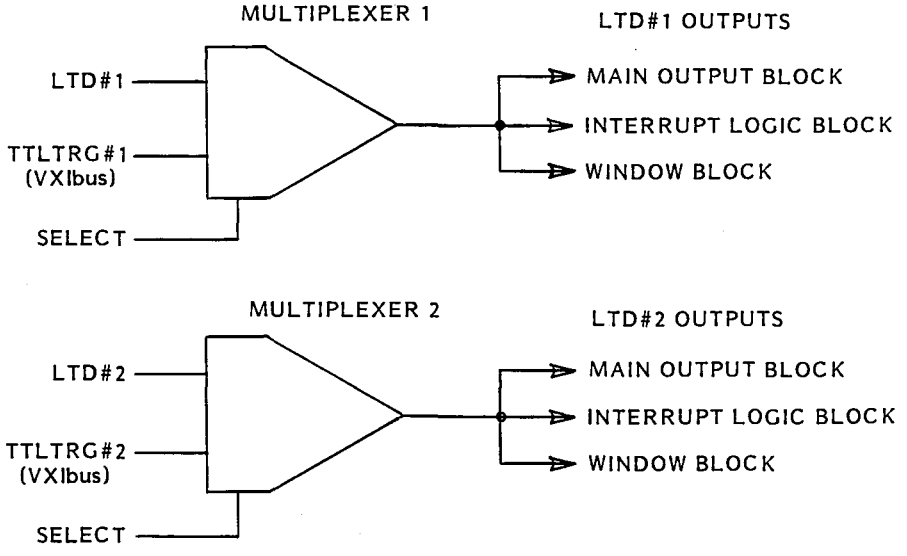


Figure 4-3, Trigger Source Block Diagram

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4.2.5 Trigger Source Block Circuit Description

4.2.5.1 The Trigger Source Block Consists of two 2-1 Multiplexers. Multiplexer 1 selects between signals from LTD#1 and TTLTRG*#1. Multiplexer 2 selects between signals from LTD#2 and TTLTRG*#2.

4.2.5.2 The multiplexer design is incorporated into U63 (26V12) PLD. The control signal for selecting Multiplexer 1 output is D0 at U85 (logic 0 selects LTD#1, logic 1 selects TTLTRG*#1). The control signal for selecting Multiplexer 2 output is D1 at U85 (logic 0 selects LTD#2, logic 1 selects TTLTRG*#2).

4.2.6 Window Block

4.2.6.1 The Window block performs a logical function on LTD#1 and LTD#2 outputs. The Window output can be selected from logic LOW, (LTD#1 AND LTD#2), (LTD#1 OR LTD#2), and (LTD#1 XOR LTD#2). The LTD#1/2 signals can be phase inverted prior to the logical operation to allow for logical NAND, NOR and XNOR functions. Refer to Figure 4-4 for block diagram.

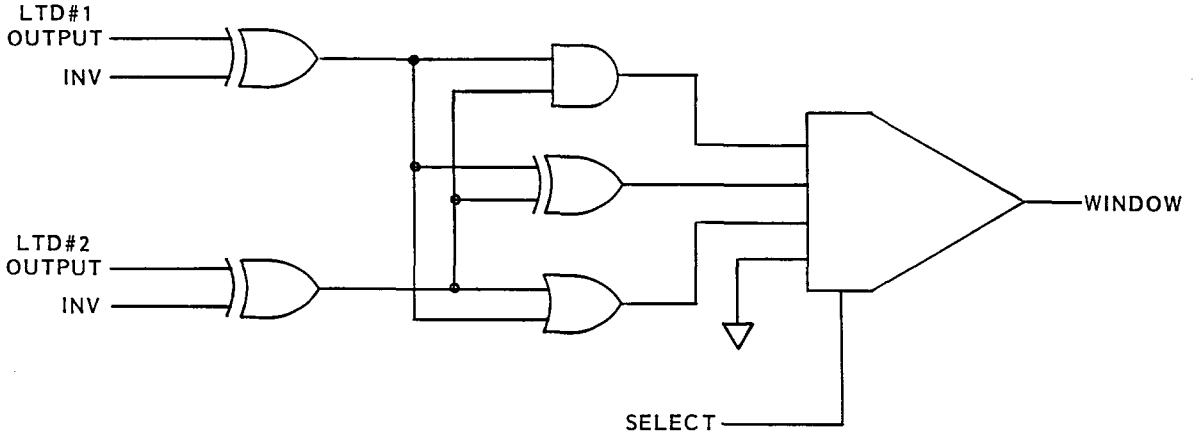


Figure 4-4, Window Block Diagram

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4.2.7 Window Block Circuit Description

4.2.7.1 The AND, OR and XOR functions are performed in U63 (26V12) PLD. LTD#1/2 phase inversion is done through XOR gates in the PLD, and is controlled from D0 (LTD#1) and D1 (LTD#2) at latch U124 where a logic high gives inversion.

4.2.7.2 The three logical outputs from the PLD and logic LOW are applied to U68, an 8-1 multiplexer. One of these four signals is selected via D2 and D3 at latch U124, and the multiplexer output is directed to the Main Output Block.

4.2.8 Main Output Block

4.2.8.1 The Main Output Block converts LTD#1, LTD#2 and Window Outputs to 10V, 50ohm outputs. When connected to a 50ohm load, the voltage at the load is 5V. The circuits for each of the three outputs are identical. The three outputs are connected to the 6056 front panel DSUB connector. Refer to Figure 4-5 for block diagram.

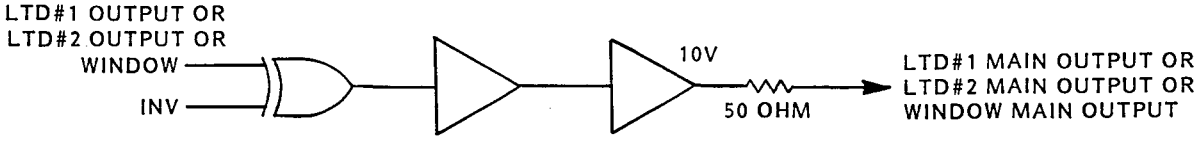


Figure 4-5, Main Output Block Diagram

4.2.9 Main Output Block Circuit Description

4.2.9.1 The circuit description applies to all three output drivers.

4.2.9.2 The Multiplexer 1/2 outputs from the Trigger Source Blocks and the multiplexer output from the Window Block are applied to a 7406 TTL open collector driver. The output is tied to a potential divider which combines as a pull-up circuit. The 620ohm and 3kohm resistors allow the output to toggle from 0.4V to 10V. A 68pF capacitor-to-ground is included to reduce overshoot caused by the following buffer.

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4.2.9.3 The 0.4V to 10V signal is buffered by the LT1010 which can output up to 150mA. The buffer output is connected to two 90.9ohm 1/2W resistors which, when combined with the output impedance of the buffer, give an overall output impedance of 50ohms.

4.2.9.4 Each output is monitored for self-test purposes. Two resistors (6.8kohms and 2.7kohms) divide the 10V output down to TTL compatible inputs for U86. These signals are read back by the microprocessor on data lines D2, D3 and D4.

4.2.9.5 To overcome the high saturation voltage of the LT1010, a +15V regulator is provided for the positive power rail. Powered from the VXI +24V rail, two 3.3V 5W zener diodes are placed in series with the LM7815 regulator to reduce the volt drop (and hence power dissipation) across it. The negative power rail is sourced from the VXI -12V rail.

4.2.10 Interrupt Logic Block

4.2.10.1 The Interrupt Logic Block is designed to interrupt the microprocessor when a selected event occurs. The event is chosen from LTD#1, LTD#2, (LTD#1 AND LTD#2) and (LTD#1 OR LTD#2), and is level sensitive. In addition, the LTD#1/2 signals are phase inverted prior to logical operation to allow further event options. When the selected event occurs, the conditions of LTD#1 and LTD#2 are latched. The latched data is checked to verify which event caused the interrupt. In conjunction with the VXIbus interface, the microprocessor sends an interrupt out on selected VXI IRQ* lines (refer to Figure 4-6 for block diagram and the VXI Interface Block).

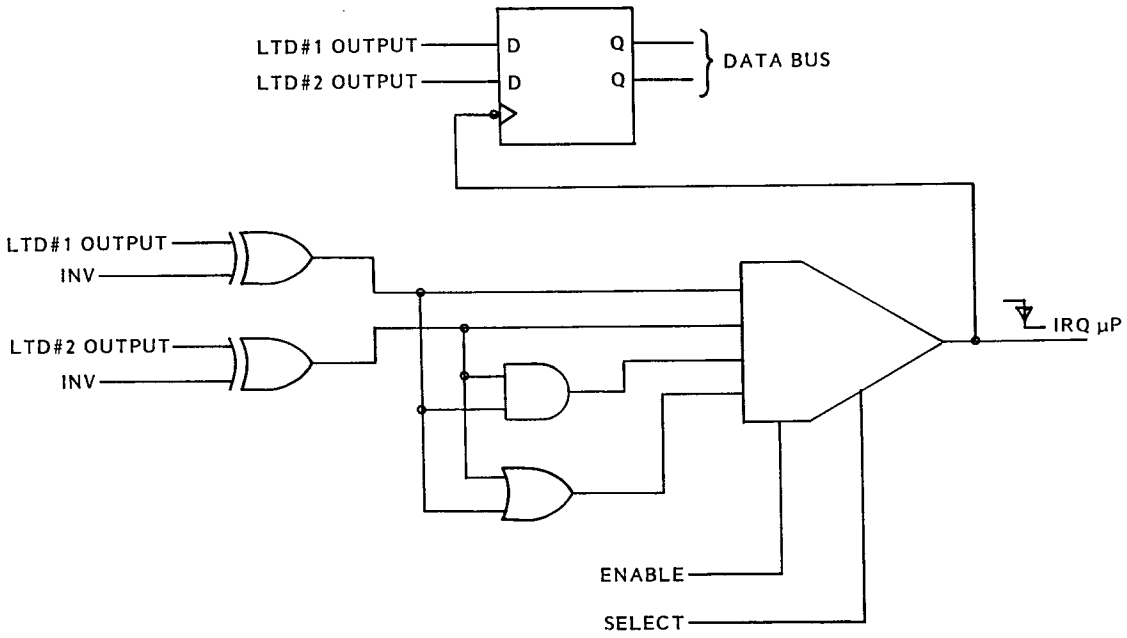


Figure 4-6, Interrupt Logic Block Diagram

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4.2.10.2 At the same time the LTD#1/2 data is latched, the event line is disabled, preventing further interrupts from interrupting the microprocessor. An additional latch is provided to monitor the Interrupt Acknowledge line from the VXIbus Slot 0 Controller. Once an acknowledgement is received, the event line is re-enabled.

4.2.11 Interrupt Logic Block Circuit Description

4.2.11.1 The microprocessor event selection is made through D4 and D5 at U85, and a multiplexer in U63 PLD. Binary code (00) (D5,D4) selects event LTD#1, binary code (01) selects LTD#2, binary code (10) selects (LTD#1 OR LTD#2), and binary code (11) selects (LTD#1 and LTD#2).

4.2.11.2 Phase inversion of the LTD#1 and LTD#2 outputs is possible through D6 and D7 of U85 where a logic high selects inversion. The inversion is performed in U63 PLD.

4.2.11.3 The logical ANDing and ORing of LTD#1 and LTD#2 is performed in U63 PLD.

4.2.11.4 Interrupts are enabled by the IRQEN signal (U124 Pin 16). The interrupt function is level sensitive. Once enabled, an interrupt will occur after an event (e.g., input exceeds the threshold). If the event occurs before the interrupt is enabled and is still true at the enable point, the microprocessor will be interrupted immediately.

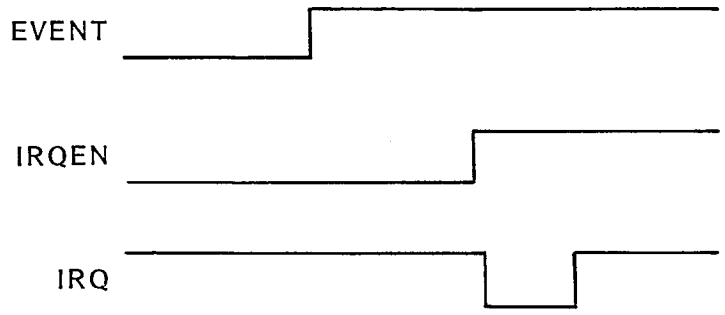


Figure 4.6A, Interrupt Enabled While Event True Causing Immediate IRQ

4.2.11.5 When an event occurs, the output U63 pin 22 clocks the latches U121b, U122a and U122b. On clocking, output U121b pin 8 goes logic low causing an interrupt at the microprocessor, U122a latches the state of LTD#1, and U122b latches the state of LTD#2. The Interrupt line is cleared by the microprocessor writing a logic low and then high to U121b pin 13. This signal is sourced from D6 at U124. This signal also resets the state of latches U122a and U122b.

4.2.11.6 Once an interrupt has occurred and further interrupts have been disabled, the microprocessor checks latch U121a for an interrupt acknowledge. This latch is clocked high via the VXI interface IACK line. The output is read back via D11 U126. The latch is cleared by strobing D5 of U124 low and high.

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4.2.12 Microprocessor Block

4.2.12.1 The Microprocessor Block includes the microprocessor, RAM, ROM, Address Decode Logic, Input/Output Latches and Power-On Reset Circuit. Refer to block diagram Figure 4-7.

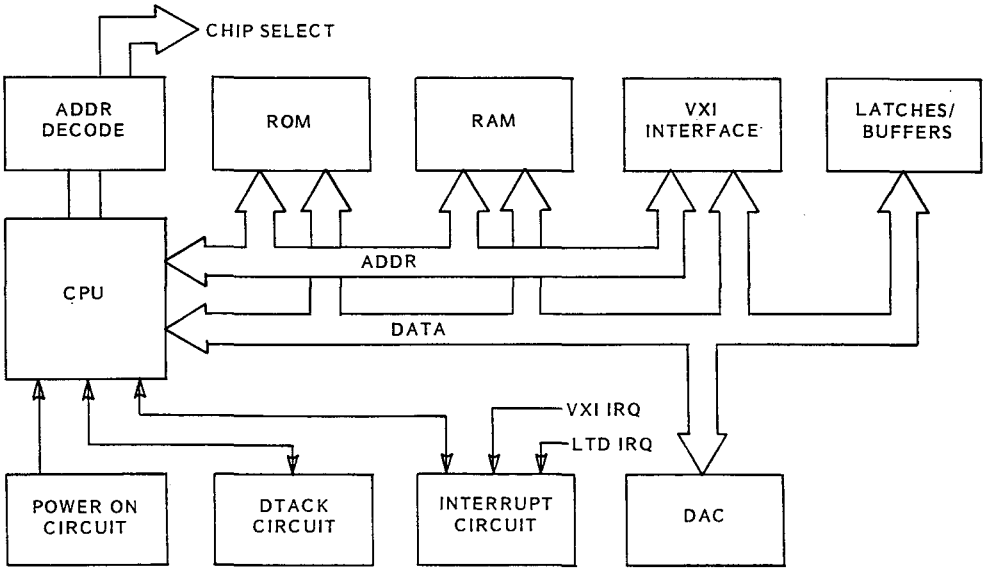


Figure 4-7, Microprocessor Block Diagram

4.2.12.2 The Microprocessor Block's basic function is to convert commands sent from the user (through the VXI interface) into control signals for setting up the instrument.

4.2.12.3 The Microprocessor Block incorporates many components essential to the microprocessor's operation. These include the ROM, RAM, Power-on Reset circuit, DTACK logic and Interrupt circuit. The remaining Microprocessor Block circuitry provides interface to all the other blocks through latches, buffers and address decode logic.

4.2.13 Microprocessor Block Circuit Description

4.2.13.1 The microprocessor (U1) is a 12MHz 68000 with 16-bit data bus and 23-bit address bus. The system firmware is contained in two 64K x 16 ROMs (U6,U7) with two 32K x 8 RAMs (U4,U5) for work area.

4.2.13.2 Address decode logic is contained in U3 PLD allowing access to the ROMs, RAMs, DACs, Latches and VXI Interface.

4.2.13.3 The reset circuit provides a reliable signal to permit an orderly shutdown of the system when power is lost. The circuit consists of a voltage reference, D1, which provides a nominal voltage level of 1.23V, U8b, which senses when the +5V supply drops below 4.5V, and discharges the reset timing capacitor, C1, via Q1. As the +5V is applied to the board, the output U8b is held low until the supply

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reaches a nominal +4.75V, at which time it goes high. This signal is inverted by U8c which in turn drives Q1. As long as the +5V is below +4.75V, the gate of Q1 is held high and prevents C1 from charging. If at any time the +5V supply drops below +4.5V due to the hysteresis provided by Z4a, the gate of Q1 is again pulled high, and the transistor discharges the capacitor C1, restarting the a reset cycle. D2 holds the voltage across the reset timing capacitor C1, and drives the HALT line from which all other reset signals are derived. This comparator also provides hysteresis due to Z4d to prevent oscillation as the capacitor voltage crosses the reference voltage. The HALT signal is hardwired logical OR of two signals. U8D buffers the low +5V sense signal from U8b, and also drives HALT. U36 buffers the reset signal from the VXI backplane, and drives PSFTRST which is the module's internal reset line.

4.2.13.4 The DTACK logic is designed into U3 PLD, and is in the form of a state machine. The DTACK output is on U3 pin 44. The DTACK logic is initially enabled by Data Strobe (DS*) going logic low. Clocked by the 12MHz system clock, the DTACK output stays high for three clock cycles before going low. DTACK returns high when data strobe goes high.

4.2.13.5 The Interrupt circuit processes the interrupts that originate from the VXI Interface Block and the Interrupt Logic Block. The circuit is contained within U3 PLD. The circuit prioritizes the interrupts and outputs the appropriate signals on the IPL0/1/2 lines to the microprocessor. The VXI Interface Block has priority one, and the Interrupt Logic Block priority two.

4.2.13.6 The Latches and Buffers provide control to both the Level Threshold Detector and the Time Constant Filters. They enable the user to configure both circuits to the required setup. The Latches (U79,U80,U81,U84,U85,U124) output logic lows and highs in order to enable/disable relays and route signals through different paths. U79 and U80 are type 74ACT273 which are capable of sourcing the 10mA required to drive the Time Constant Filter solid state relays. U81 drives U75, a high current source driver. The driver is used to operate the on-board 24V relays located in the LTD Block and TCF Block. U84, U85 and U124 provide control logic for the Trigger Source Block and Window Block.

4.2.13.7 Buffers U86 and U126 allow the microprocessor to readback the self-test lines and Interrupt Logic Block state after an Interrupt.

4.2.14 VXI Interface Block

4.2.14.1 The VXI Interface Block consists of the interface circuitry between the VXIbus Slot 0 Controller and the 6056 on-board microprocessor. The Slot 0 Controller sends and receives information to/from the 6056 via this circuit. Refer to Figure 4-8 for block diagram.

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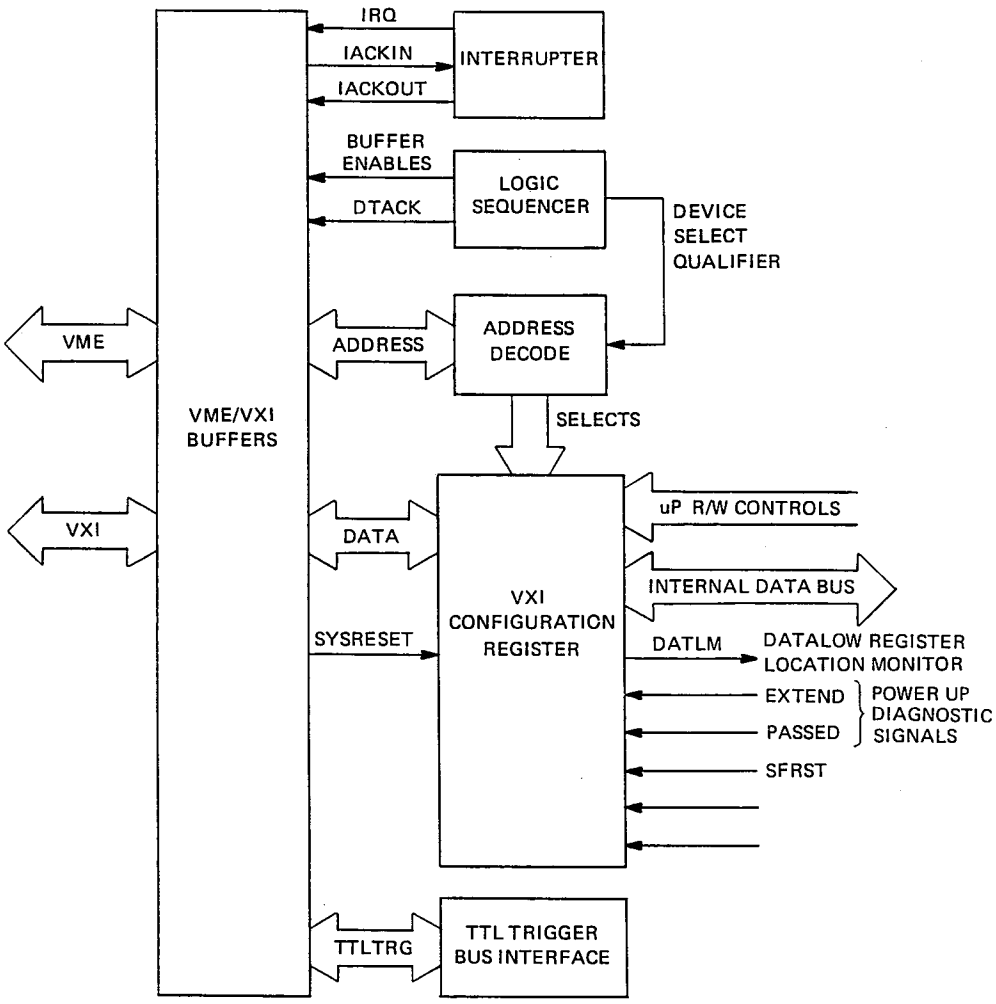


Figure 4-8, VXI Interface Block Diagram

4.2.15 VXI Interface Block Circuit Description

4.2.15.1 Options and Setup

4.2.15.1.1 The block diagram for the VXIbus Interface is shown in Figure 4-8. The interface implements Revision 1.3 of the VXIbus Specification for message-based devices with the following VXIbus optional features:

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a. Selectable dynamic or static configuration.

b. Selectable "Assign Interrupt Line" command support (programmable interrupt level) or manual interrupt level selection.

4.2.15.1.2 Two DIP switches SW1 and SW2 are provided for the selectable features of the VXIbus interface. The functions of the switches are as follows:

SW2 (six positions

Switch 1-3: Interrupt level setting for manual interrupt level mode. Switch 1 is least significant.

Switch 4: Open - Programmable interrupt level supported. Closed - Manual interrupt level.

Switch 5: Unused.

Switch 6: Unused.

SW1 (eight positions)

Switch 1-8: Logical address setting for static configuration. All open - the address is set to 255 and the 6056 responds to auto-configuration. Any other switch setting - the 6056 is now at the selected logical address.

4.2.15.2 VME/VXI P1 Connector Interface

4.2.15.2.1 The VME/VXI address and data bus are buffered with standard TTL buffers as recommended in the VMEbus specification. The VMEbus control signals are buffered with a 74HCT244 in order to meet the low leakage requirement for the MODID line (100µA). The data bus logic is bi-directional and supports D16/D08 communication.

4.2.15.3 Logical Address Register

4.2.15.3.1 The interface supports both dynamic and static logical address configuration. Static configuration is implemented with a DIP switch SW1. Dynamic configuration is implemented with a latch which is reset at power-up, and is written to by the VXIbus controller. The two configurations are selected by setting the DIP switch SW1 to all open for dynamic configuration, or any other setting (see Subsection 4.2.14.1.2) which causes a multiplexer to route the proper register to the logical address comparator.

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4.2.15.3.2 When the Dynamic Configuration mode is selected and the logical address is FF, the instrument can only be selected with the MODID line. Figure 4-9 shows a block diagram of the logical address circuitry.

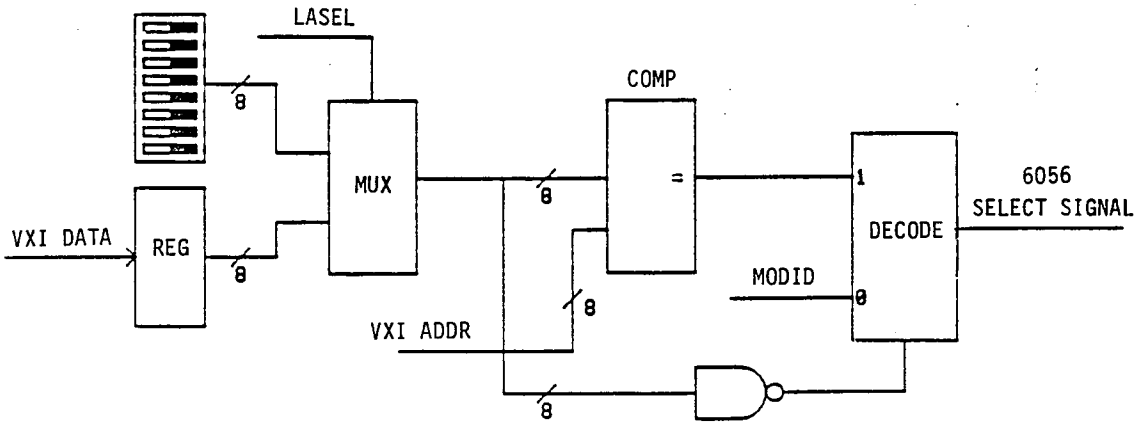


Figure 4-9, Logical Address Select Block Diagram

4.2.15.4 ID, Device Type, Protocol Registers

4.2.15.4.1 These three static, read-only registers are implemented in PROM. The registers are located at the following addresses of the PROM:

Address 00 - ID
01 - Device Type
04 - Protocol

4.2.15.4.2 The ID REGISTER provides the following information:

Device Class = 10 (Message-based)

Address Space = 11 (for A16 only)

Manufacturer ID = Racal-Dana ID number

4.2.15.4.3 The contents of the DEVICE TYPE REGISTER are as follows:

Model Code = 6056 Identifier

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4.2.15.4.4 The PROTOCOL REGISTER contains the following bits:

CMDR*	=	1 (Servant only)
SIGNAL REGISTER*	=	1 (Signal Register not implemented)
MASTER*	=	1 (Not a VMEbus master)
INTERRUPTER	=	1 (Interrupter capability)
FHS*	=	1 (Fast Handshake not implemented)
SHARED MEMORY*	=	1 (Shared Memory not implemented)
RESERVED	=	111111
DEV DEP	=	1111

4.2.15.5 Interrupt Logic

4.2.15.5.1 Because the 6056 does not have bus master capability, the VXIbus specification requires it to have interrupter capability. The interrupt logic is shown on the instrument's schematic. The interrupt logic is divided into three separate functions: 1) Interrupt Level Select, 2) Interrupt Generator, and 3) Interrupt Acknowledge.

4.2.15.6 Interrupt Level Select

4.2.15.6.1 Two methods are provided for the selection of the interrupt level - manual and programmable. In manual mode, the desired interrupt level is set with the first three switches of SW2 while the fourth switch is in the closed position. If the fourth switch is in the open position, the instrument supports the "Assign Interrupt Line command. When the microprocessor receives this command, the desired interrupt level is stored in the interrupt level select register.

4.2.15.7 Interrupt Generator

4.2.15.7.1 The decision to send a VXIbus interrupt is always made by the microprocessor according to information it receives from the "Response Enable" command. To generate an interrupt, the µP simply writes the board's logical address along the appropriate "event" data into the Event Register. This 16-bit word becomes the Status/ID word as defined in the VXIbus specification. The write operation causes the RSPINT+ signal to go high which enables the decoder controlling the VXIbus interrupt lines. The one interrupt line corresponding to the previously selected interrupt level goes low and stays low until an interrupt acknowledge is received.

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4.2.15.8 Interrupt Acknowledge

4.2.15.8.1 The interrupt acknowledge circuitry consists of a comparator, the Event Register, and the VXIbus Control Logic. The comparator determines whether or not the VXIbus master is acknowledging the instrument's interrupt by comparing the RSPINT+ signal with logic-one to see if the instrument is sending out an interrupt at all, and by comparing the interrupt level being broadcast on address lines VBA1-VBA3 with the selected interrupt level of the instrument. If an interrupt acknowledge cycle is taking place but the comparator does not detect a match on these signals, the VXIbus Control PAL activates the IACKOUT signal according to the VMEbus guidelines, and waits for the cycle to end. If the Interrupt Acknowledge is determined to be for this instrument interrupt, the contents of the event register are placed on the VXIbus as the status/ID word, and the active interrupt line is released (Release On Acknowledge protocol). Figure 4-10 shows the flow of an interrupt operation.

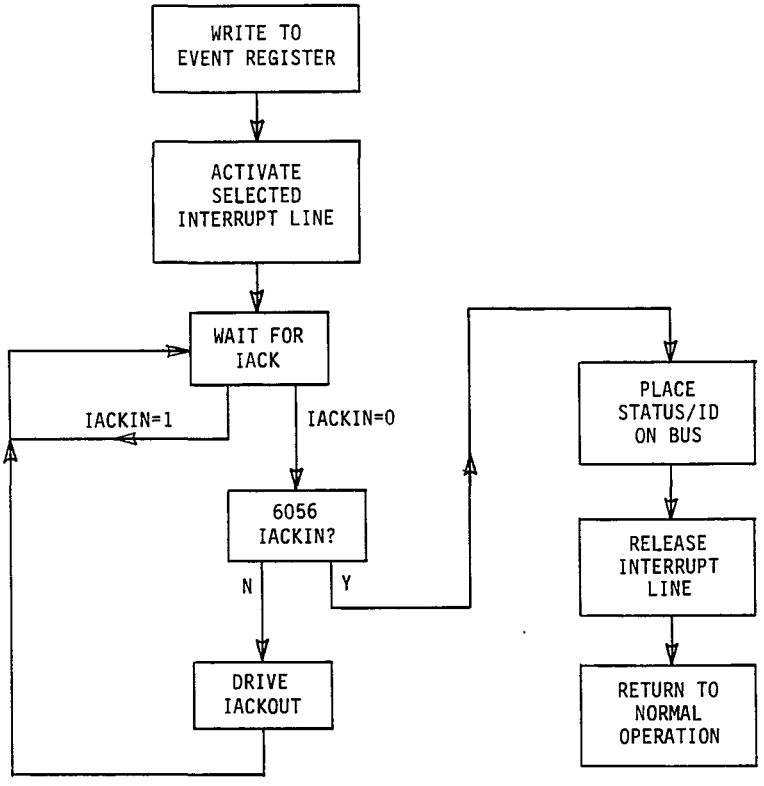


Figure 4-10, Interrupt Acknowledge Cycle

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4.2.15.9 Status, Control, Response Registers

4.2.15.9.1 The Status, Control, and Response registers are implemented in a single 1810 EPLD described below.

BIT #	15	14	13-----4	3	2	1-----0
CONTENTS	A24/A32 ACTIVE	MODID*	DEVICE DEPENDENT	READY	PASSED	DEVICE DEPENDENT
PAL PIN NAME	#ACTIVE	#MOD	NOT USED	#RDY	#PAS	NOT USED

4.2.15.10 Status Register

4.2.15.10.1 The Status Register is a VXIbus read-only register with the following bit designation.

4.2.15.10.2 The #ACTIVE and #MOD bits are accessed by the VXIbus only. The #ACTIVE bit is always low indicating no A24/A32 space. The MODID bit is simply a pass-through of the BMODID signal. The #RDY and #PAS bits are written and read by the µP through the #READY and #PASSED pins.

4.2.15.11 Control Register

4.2.15.11.1 The Control Register is a VXIbus write-only register with the following bit designation:

BIT #	15	14-----2	1	0
CONTENTS	A24/A32 ENABLE	DEVICE DEPENDENT	SYSFAIL INHIBIT	RESET
PAL PIN NAME	#UAEN	NOT USED	#SFINHC	#RST

4.2.15.11.2 Each bit is stored in an internal flip-flop after the VXIbus commander writes to this register. The following actions result from the control bits going active:

#UAEN (Active High): Causes the #ACTIVE bit of the Status Register to go high, unused in this design.

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#SFINHC (Active High): Disables the SYSFAIL signal from going active.

#RST (Active High): Causes the PSFTRST signal to go low which puts the instrument into a soft reset condition.

4.2.15.12 Response Register

4.2.15.12.1 The Response Register is a VXIbus read only register which is also read by the µP. To allow the VXIbus and the µP bus access to these bits, two copies of the register are maintained. The register has the following bit designation:

BIT #	15	14	13	12	11	10	9	8	7	6←0
CONTENTS	0	RESERVED	DOR	DIR	ERR*	READ READY	WRITE READY	FHS ACTIVE*	LOCKED*	DEVICE DEPENDENT
VXI PIN NAME	*ZERO	#RSV	#DOR	#DIR	#ERR	#RDR	#WRR	#FHS	NOT USED	NOT USED
uP PIN NAME	*IZERO	#IRSV	#IDOR	#IDIR	#IERR	#IRDR	#IWRR	#IFHS	NOT USED	NOT USED

4.2.15.12.2 The VXIbus pins and the µP pins are equivalent with the exception of the output enable signals that control them. A change that takes place on the #IDIR pin, for example, will also take place on the #DIR pin. With the exception of the #RDR/#IRDR and WRR/#IWRR pins, all bits are set and reset by writes from the µP. The #WRR bit can only be set by the µP, and the #RDR bit can only be reset by the µP. The states of these bits will also change automatically on the following conditions:

#RDR -> 1: µP write to the Data Low Register
#RDR -> 0: VXIbus read of the Data Low Register
#WRR -> 0: VXIbus write to the Data Low Register

4.2.15.13 Data Low Register

4.2.15.13.1 The Data Low Register is implemented using a registered transceiver which allows the VXIbus commander to write commands without destroying data being output by the 6056.

4.2.15.14 Signal/Event Register

4.2.15.14.1 Another registered transceiver is used to implement the Signal/Event Register. These two registers have no functional relation to each other, but are implemented in the same chip set to conserve board space. The Signal Register allows a VXIbus master to send commands to the 6056 through signals rather than through the word serial format. The Event Register is used to generate VXIbus interrupts.

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By writing the device's logical address and a protocol event into the Event Register, the µP causes the interrupt logic to drive one of the VXIbus interrupt lines active. Upon receipt of an interrupt acknowledge, the contents of the Event Register are placed on the VXIbus data bus as the Status/ID word.

4.2.15.15 TTLTRG* Circuit

4.2.15.15.1 The 6056 allows TTLTRG* signals from the VXIbus backplane to be routed to the Trigger Source Block. Two 8-1 multiplexers, U66 and U67, allow one signal to be routed to Multiplexer 1 and Multiplexer 2. The TTLTRG* signals are selected via latch U84.

4.2.15.15.2 The VXI Interface also allows LTD1/2 and the Window Outputs to be routed to the backplane via driver U65. The signal selected to be output is multiplexed into the driver by U64 PLD. The PLD essentially provides a 4-1 multiplexer for each of the eight driver pins. The fourth signal (aside from LTD#1, LTD#2, and Window) to be input to each multiplexer is logic high which is the inactive state for the open collector TTLTRG* outputs.

4.2.16 Power Supplies

4.2.16.1 DC power is supplied to the 6056 by the VXI backplane. +5V, +12V, -12V and +24V are used. Filtering is provided to help reduce the possibility of circuit noise being passed back to the VXI backplane.

4.2.17 Time Constant Filter Block Theory Of Operation

4.2.17.1 The Time Constant Filter Block consists of two identical circuits (TCF1, TCF2). Only TCF1 will be described below. See block diagram, Figure 4-11.

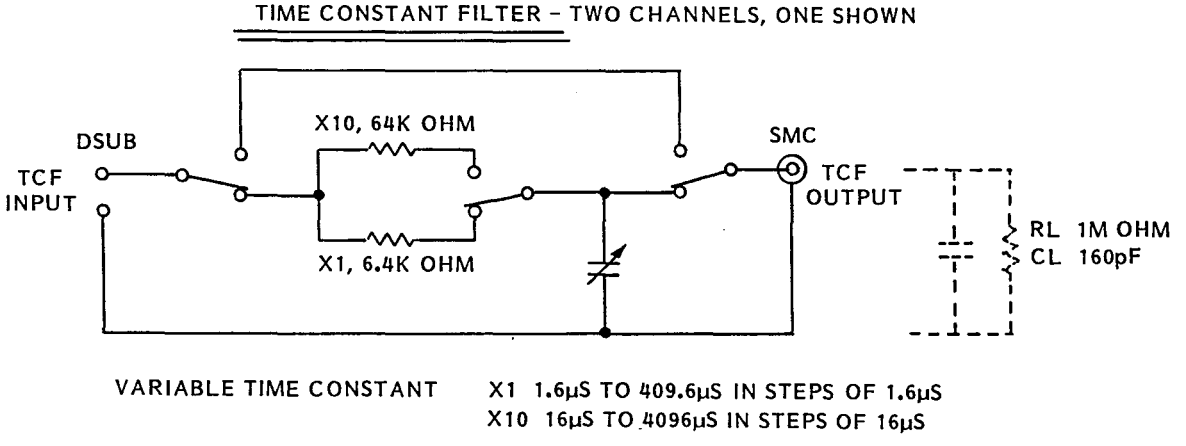


Figure 4-11, Time Constant Block Diagram

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4.2.17.2 Each TCF is a variable time constant, low pass, single pole filter and is isolated from any other part of the instrument. It has two mode settings X1 and X10. The X1 mode time constant can be varied from 0µS to 409.6µS in steps of 1.6µS. The X10 mode time constant can be varied from 0µS to 4096µS in steps of 16µS. The accuracy of the time constant is +/-10%.

4.2.17.3 The design assumes a load of 1Mohm and 160pF.

4.2.18 Time Constant Filter Circuit Description

4.2.18.1 The architecture for the filter is a selectable series resistor with selectable parallel capacitors. The values of the filters and capacitors are selected to meet the time constant requirements.

4.2.18.2 The series resistor is selected from 6.34kohm (X1) and 63.4kohm (X10). Any one or more of eight parallel mica capacitors (250pF, 500pF, 1nF, 2nF, 4nF, 8nF, 16nF and 32nF) are selectable.

4.2.18.3 Two switchable, parallel 220kohm resistors are also connected in parallel with the capacitors. They are used to discharge the capacitors before changing the setup.

4.2.18.4 The time constant is set to zero by disabling the relay K11.

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SECTION 5 MAINTENANCE

5.1 Performance Verification Procedures (PVPs)

5.1.1 Introduction

5.1.1.1 This section provides the procedures necessary to verify conformance of the 6056 to it's published specifications. It is recommended these procedures are carried out at a minimum interval of one year.

5.1.2 Required Test Equipment

Function Generator, HP3325A
DC Voltage Calibrator, Valhalla 2701
Analog Oscilloscope, DC to 350MHz, Tektronix 2465A
Frequency Counter, DC to > 100KHz, Racal Dana 1992
Digital Multimeter, +/-5% Accuracy, DC to 100KHz, Racal Dana 5001

NOTE

In the following procedures, it is recommended all signal levels are measured with the Digital Multimeter, and adjusted to give a level as close to its nominal value as can be achieved before being applied to the 6056.

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5.1.3 LTD#1 Sensitivity Test

5.1.3.1 Connect the HP3325 Function Generator to the LTD#1 input, and the 1992 Frequency Counter to LTD#1 Main Output as shown in Figure 5-1.

5.1.3.2 Set the 6056 LTD#1 trigger threshold to 0V by sending it the command string

VOLT:DC:REF 0.0

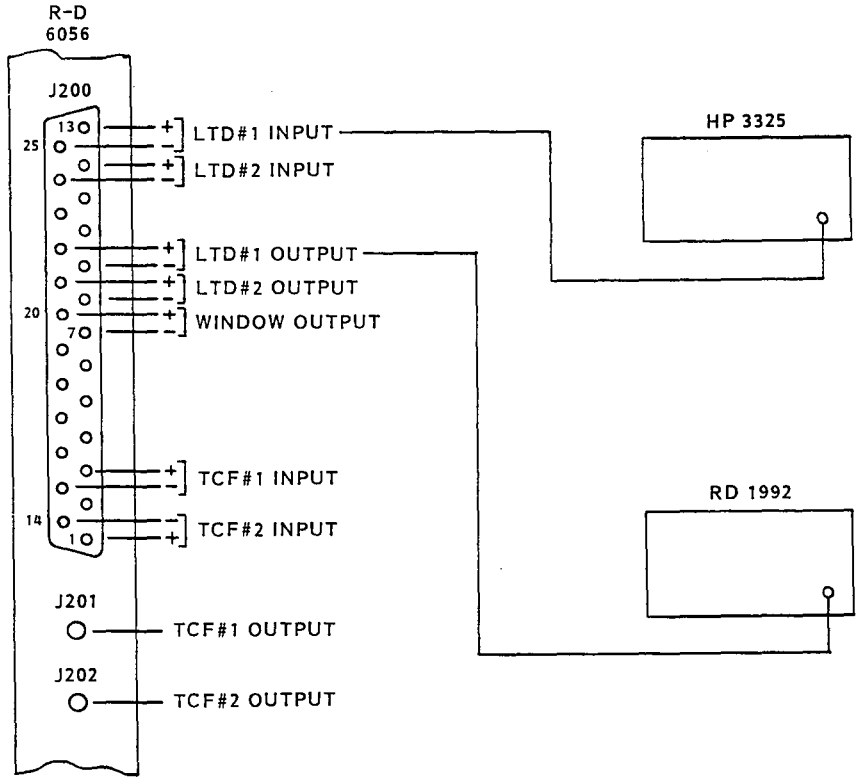


Figure 5-1, Setup For LTD#1 Sensitivity Test

5.1.3.3 Apply the frequencies given in Table 5-1 to the 6056 at a level of 60mVrms. Set up the counter to 50ohms input impedance and measure the period between the rising edges of the output. Verify the 1992 gives a stable reading for the selected frequency.

Table 5-1, LTD#1 Low Frequency Sensitivity Test

Frequency
100Hz
1KHz
10KHz
100KHz

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5.1.4 LTD#2 Sensitivity Test

5.1.4.1 Connect the HP3325 Function Generator to the LTD#2 input, and the 1992 Frequency Counter to LTD#2 Main Output as shown in Figure 5-2 below.

5.1.4.2 Set the 6056 LTD#2 trigger threshold to 0V by sending the following command string:

VOLT:DC:REF2 0.0

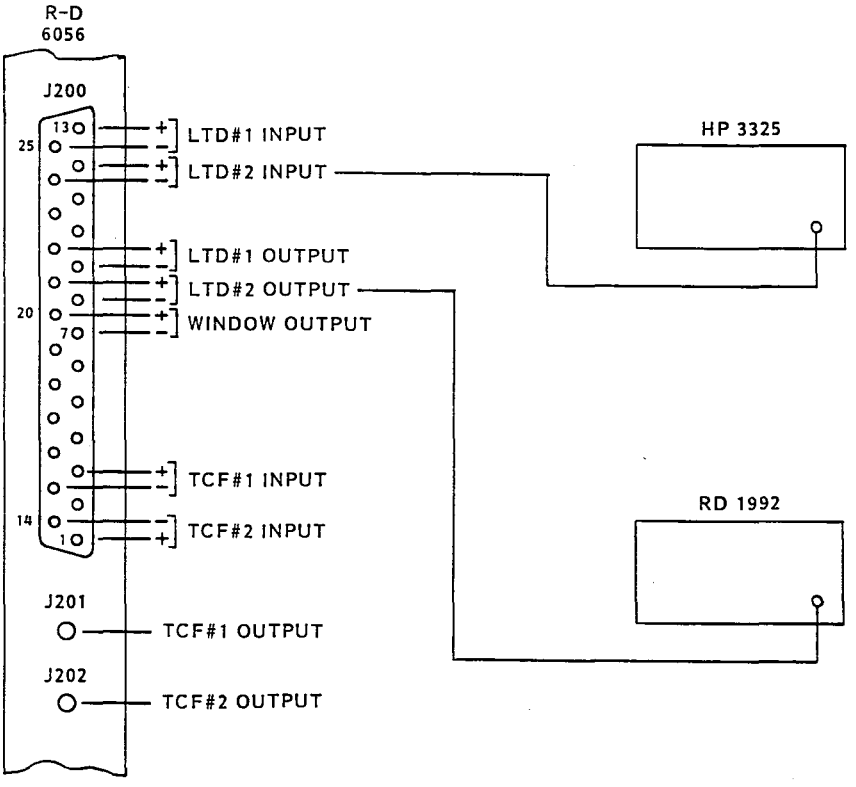


Figure 5-2, Setup For LTD#2 Sensitivity Test

5.1.4.3 Apply the frequencies given in Table 5-2 to the 6056 at a level of 60mVrms. Set up the counter to 50ohms input impedance, and measure the period between the rising edges of the output. Verify the 1992 gives a stable reading for the selected frequency.

Table 5-2, LTD#2 Low Frequency Sensitivity Test

Frequency
100Hz
1KHz
10KHz
100KHz

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5.1.5 LTD#1 Trigger Level Accuracy Test

5.1.5.1 Connect the DC Standard to LTD#1 input, and connect the oscilloscope to the LTD#1 Main Output as shown in Figure 5-3 below.

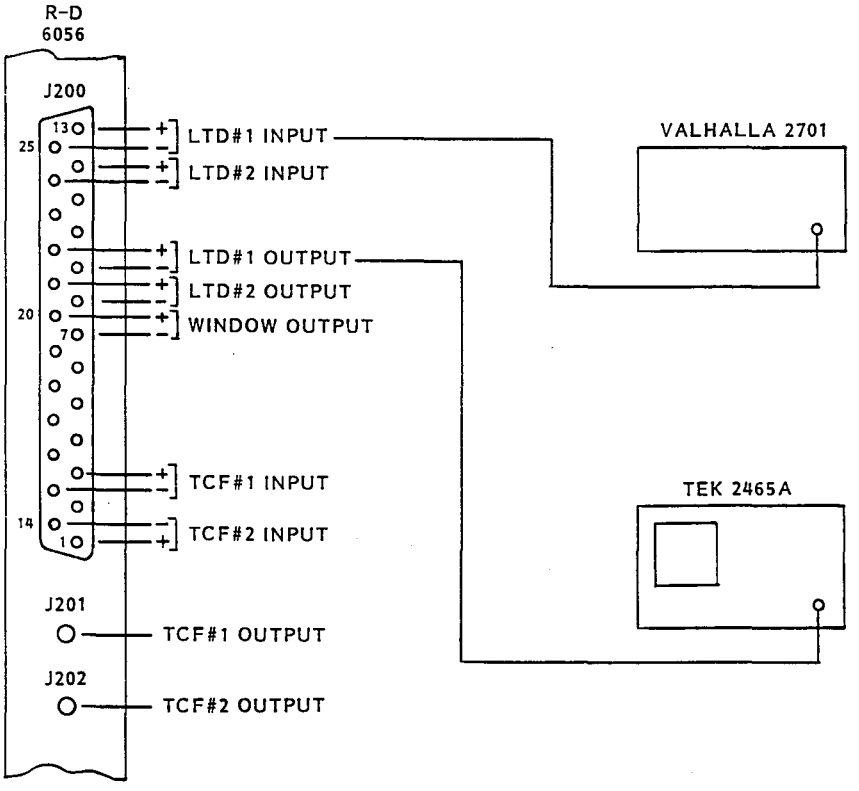


Figure 5-3, Setup For LTD#1 Trigger Level Accuracy Test

5.1.5.2 Set the DC Standard to the voltage levels given in Table 5-3 below using the command string VOLT:DC:REF1 < >. Increase the 6056 trigger level until the Main Output is seen to trigger on the oscilloscope. Verify the trigger level setting is within the tolerance given.

Table 5-3, LTD#1 Trigger Level Accuracy Test

DC Level	Trigger Tolerance
+40V	+40V +/-0.61V
0V	0V +/-0.21V
-40V	-40V /-0.61V

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5.1.6 LTD#2 Trigger Level Accuracy Test

5.1.6.1 Connect the DC Standard to LTD#2 input, and connect the oscilloscope to the LTD#2 Main Output as shown in Figure 5-4 below.

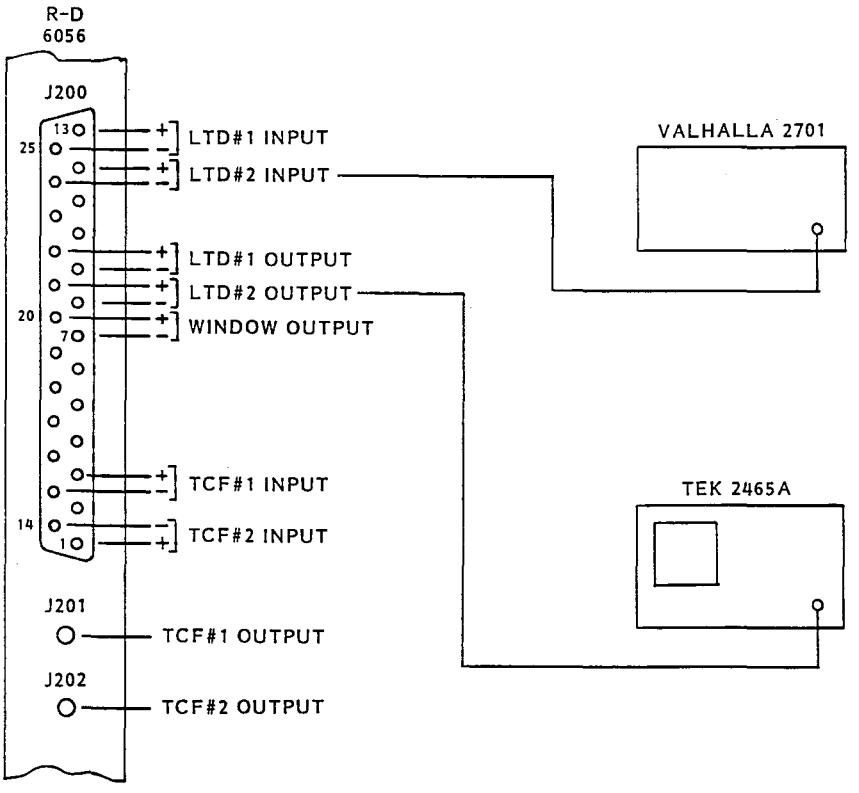


Figure 5-4, Setup For LTD#2 Trigger Level Accuracy Test

5.1.6.2 Set the DC Standard to the voltage levels given in Table 5-4 below using the command string VOLT:DC:REF2 < >. Increase the 6056 trigger level until the Main Output is seen to trigger on the oscilloscope. Verify the trigger level setting is within the tolerance given.

Table 5-4, LTD#2 Trigger Level Accuracy Test

DC Level	Trigger Tolerance
+40V	+40V +/-0.61V
0V	0V +/-0.21V
-40V	-40V /-0.61V

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5.1.7 Main Output Performance Test

5.1.7.1 Connect the HP3325 to LTD#1 input, and LTD#1 Main Output to the oscilloscope as shown in Figure 5-5 below.

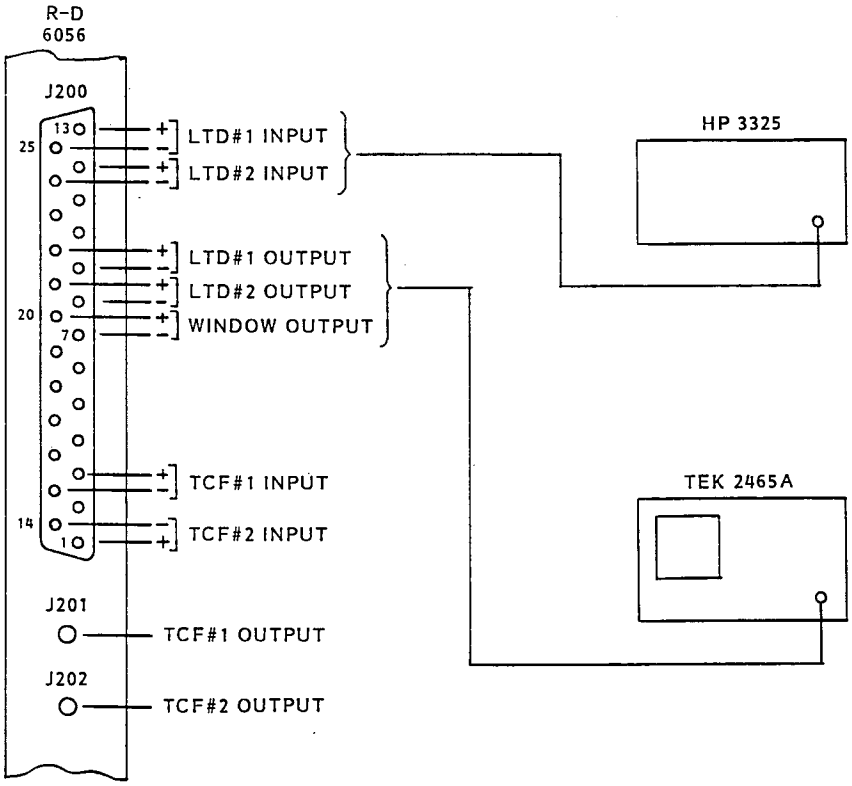


Figure 5-5, Setup For Main Output Performance Test

5.1.7.2 Set LTD#1 and LTD#2 of the 6056 to trigger at 0V using the command string

VOLT:DC:REF1 0.0
VOLT:DC:REF2 0.0

5.1.7.3 Set the HP3325 to output $\pm 2V_{pp}$ at 10KHz (sine). Set the oscilloscope input impedance to 50ohms.

5.1.7.4 Verify the LTD#1 Main Output:

Logic low	< 0.4V
Logic high	> 4.6V
Risetime	< 100nSec
Falltime	< 100nSec

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5.1.7.5 Connect the HP3325 to LTD#2 input, and LTD#2 Main Output to the oscilloscope.

5.1.7.6 Verify the LTD#2 Main Output:

Logic low	< 0.4V
Logic high	> 4.6V
Risetime	< 100nSec
Falltime	< 100nSec

5.1.7.7 Enable the window function to logically OR LTD#1 and LTD#2 using the command string

FUNCTION "A OR B"

5.1.7.8 With the HP3325 still connected to the LTD#2 input, connect the Window Main Output to the oscilloscope.

5.1.7.9 Verify the Window Main Output:

Logic low	< 0.4V
Logic high	> 4.6V
Risetime	< 100nSec
Falltime	< 100nSec

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5.1.8 TCF#1 Time Constant Accuracy

5.1.8.1 Connect the HP3325 Function Generator to the TCF#1 input and the Tektronix 2465A slope to the output as shown in Figure 5-6 below.

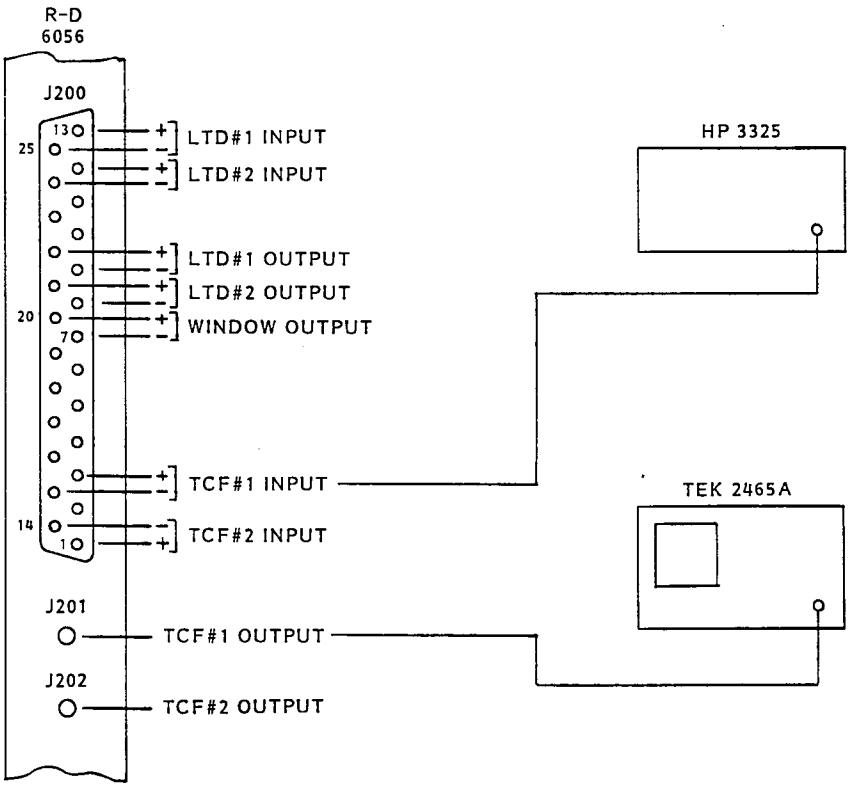


Figure 5-6, Setup For TCF#1 Time Constant Accuracy Test

5.1.8.2 Set the 6056 TCF#1 time constant to the values shown in Table 5-5 using command string:

INPUT:FILT1:TIME < >

5.1.8.3 Set the HP3325 to square wave at $5V_{pp}$ at the frequencies shown below in Table 5-5. Set the scope to 1MOhm input impedance, DC coupled. Monitor the waveform on the display and, using the vertical calibration, adjust the signal peaks to the 0% and 100% marks. Set the voltage level markers to the 0% and 63% points. Adjust the timebase to measure the 63% risetime. Verify the risetime is within the tolerance as below:

Table 5-5, TCF#1 Time Constant Accuracy

Test Frequency	Time Constant	Tolerance
5KHz	3.2µS	±3.2µS
1KHz	16µS	±3.2µS
250Hz	409.6µS	±40.96µS
250Hz	416µS	±41.6µS
20Hz	4096µS	±409.6µS

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5.1.9 TCF#2 Time Constant Accuracy

5.1.9.1 Connect the HP3325 Function Generator to the TCF#2 input, and the Tektronix 2465A oscilloscope to the output as shown in Figure 5-7 below.

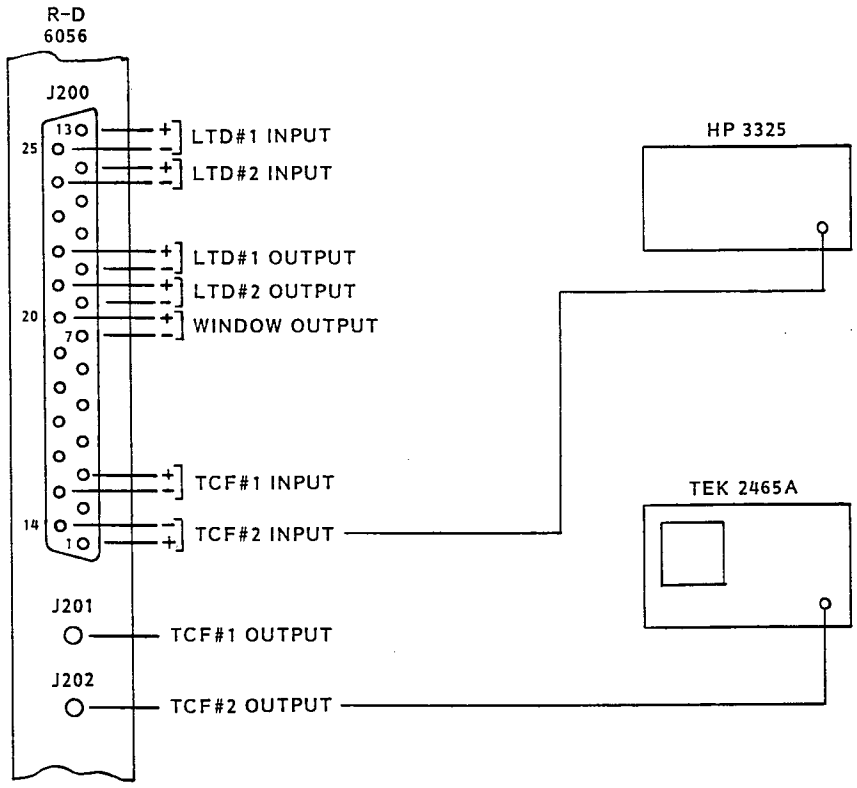


Figure 5-7, Setup For TCF#2 Time Constant Accuracy Test

5.1.9.2 Set the 6056 TCF#2 time constant to the values shown in Table 5-6 using command string

INPUT:FILT2:TIME < >

5.1.9.3 Set the HP3325 to square wave at $5V_{pp}$ at the frequencies shown below in Table 5-6. Set the scope to 1MOhm input impedance, DC coupled. Monitor the waveform on the display and, using the vertical calibration, adjust the signal peaks to the 0% and 100% marks. Set the voltage level markers to the 0% and 63% points. Adjust the timebase to measure the 63% risetime. Verify the risetime is within the tolerance as below in Table 5-6.

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Table 5-6, TCF#2 Time Constant Accuracy

Test Frequency	Time Constant	Tolerance
5KHz	3.2µS	±3.2µS
1KHz	16µS	±3.2µS
250Hz	409.6µS	±40.96µS
250Hz	416µS	±41.6µS
20Hz	4096µS	±409.6µS

5.2 Calibration

5.2.1 Introduction

5.2.1.1 This section provides the necessary information for calibrating the Model 6056. Calibration should be performed on a yearly basis. There are four calibration procedures; LTD#1 DAC offset and gain, LTD#2 DAC offset and gain, LTD#1 comparator offset and LTD#2 comparator offset.

5.2.2 Equipment Needed:

Function Generator, DC to 10KHz, HP3325
Digital Multimeter, +/-5% Accuracy, DC to 100KHz, Racal Dana 5001
VXI Extender Cards
Analog Oscilloscope, DC to 350MHz, Tektronix 2465A

5.2.3 LTD#1 DAC Offset and Gain Adjustment

5.2.3.1 Remove the right hand side cover from the 6056, and insert the unit into the VXIbus chassis via the extender cards.

5.2.3.2 Connect the Digital Multimeter to test points TP32 (+) and TP19 (-). Set the 6056 trigger level to +40V using command string VOLT:DC:REF1 40.0, and adjust the offset pot R25 so the voltage reading is -10V.

5.2.3.3 Set the 6056 trigger level to -40V using command string VOLT:DC:REF1 -40.0, and adjust the gain pot R24 so the voltage reading is +9.9997V.

5.2.4 LTD#2 DAC Offset and Gain Adjustment

5.2.4.1 Connect the Digital Multimeter to test points TP34 (+) and TP13 (-). Set the 6056 trigger level to +40V using command string VOLT:DC:REF1 +40.0, and adjust the offset pot R41 so the voltage reading is -10V.

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5.2.4.2 Set the 6056 trigger level to -40V using command string VOLT:DC:REF2 -40.0, and adjust the gain pot R40 so the voltage reading is +9.9997V.

5.2.5 **LTD#1 Comparator Offset Calibration**

5.2.5.1 With the 6056 still on the extender cards, set LTD#1 trigger level to 0V using command string VOLT:DC:REF1 0.0.

5.2.5.2 Connect the HP3325 Function Generator to LTD#1 input and to the 2465A oscilloscope channel 1. Connect Channel 2 of the 2465A oscilloscope to Test Point TP33 using a X10 probe with probe ground to TP19, as shown in Figure 5-8 below.

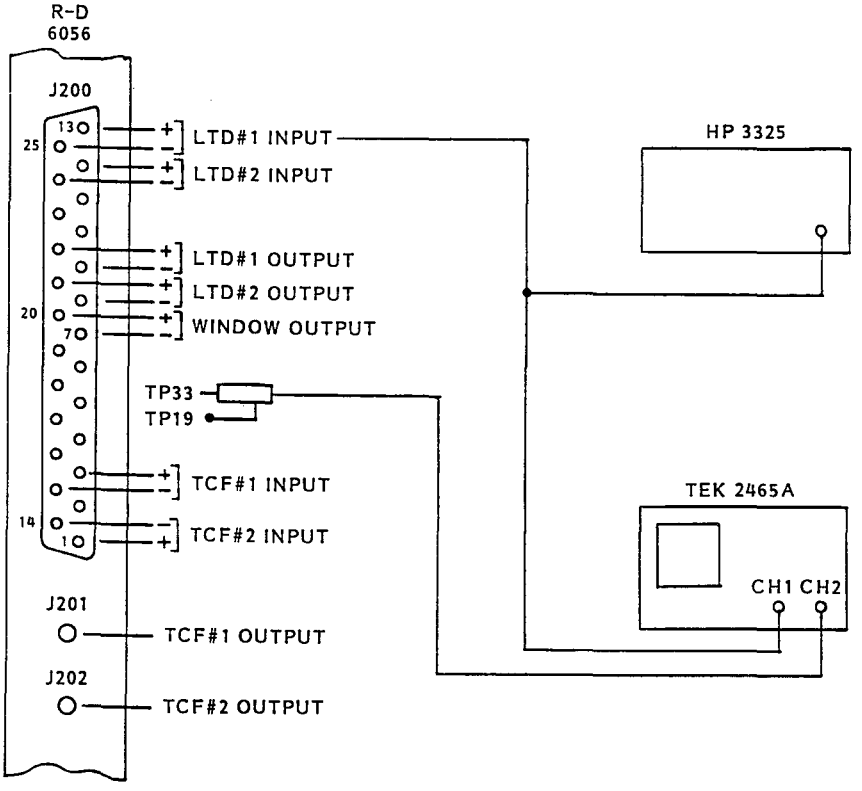


Figure 5-8, Setup For LTD#1 Comparator Offset Calibration

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5.2.5.3 Set the HP3325 to triangle wave output at a level of $1V_{pp}$ at 1KHz. Set the 2465A oscilloscope to XY mode.

5.2.5.4 Observe the hysteresis window on the oscilloscope screen. Adjust R14 to bring the center of the hysteresis window to the center of the screen.

5.2.6 LTD#2 Comparator Offset Calibration

5.2.6.1 With the 6056 still on the extender cards, set LTD#2 trigger level to 0V using command string VOLT:DC:REF2 0.0.

5.2.6.2 Connect the HP3325 Function Generator to LTD#2 input and to the 2465A oscilloscope channel 1. Connect channel 2 of the 2465A oscilloscope to Test Point TP35 using a X10 probe with ground to TP13, as shown in Figure 5-9 below.

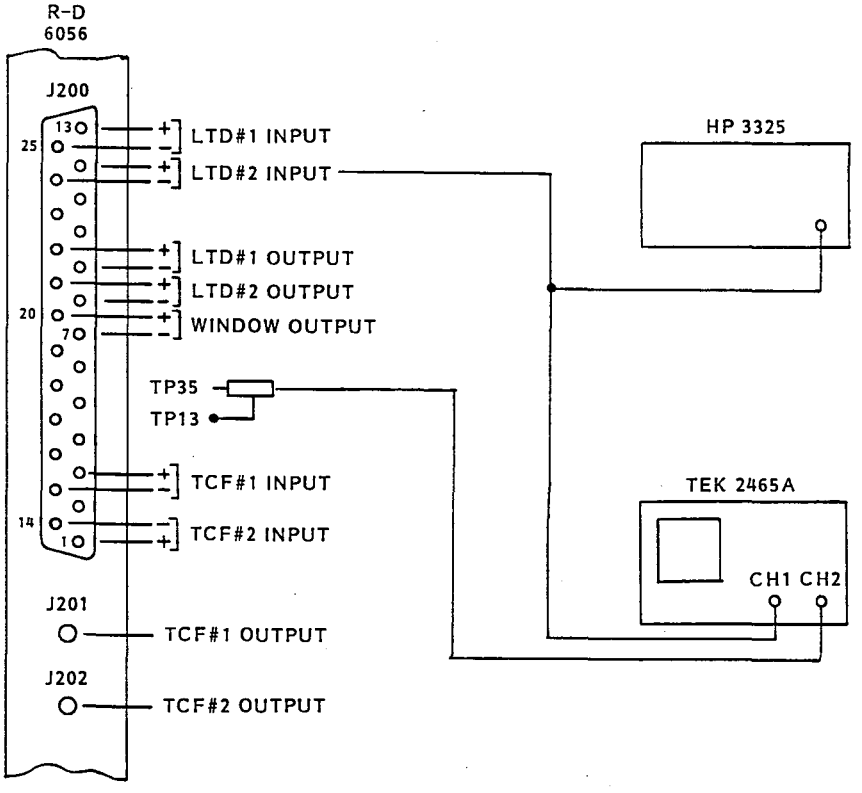


Figure 5-9, Setup For LTD#2 Comparator Offset Calibration

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5.2.6.3 Set the HP3325 to triangle wave output at a level of $1V_{pp}$ at 1KHz. Set the 2465A oscilloscope to XY mode.

5.2.6.4 Observe the hysteresis window on the oscilloscope screen. Adjust R30 to bring the center of the hysteresis window to the center of the screen.

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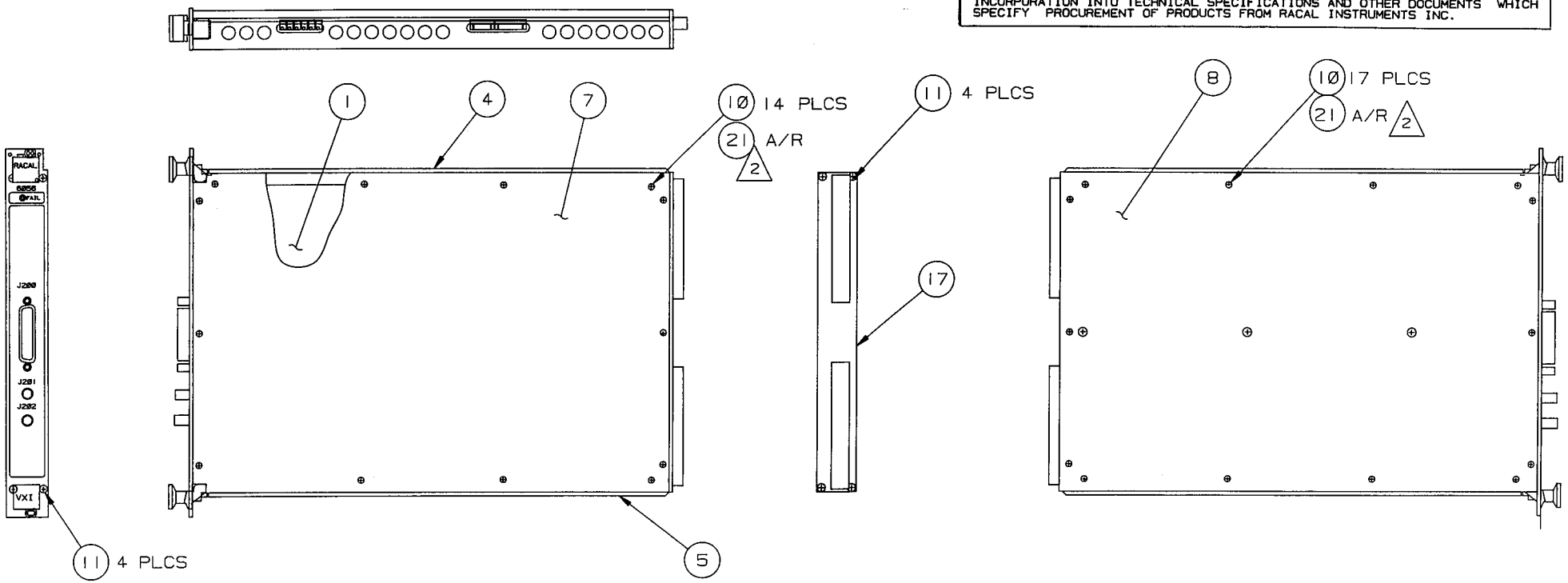
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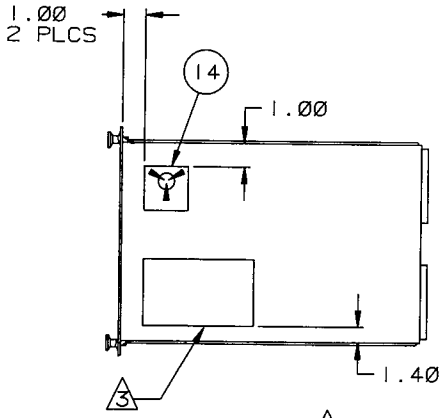
407144-003	Final Assembly, 6056	6-2
405062-003	PCB Assy, 6056	6-3
435062	Schematic, 6056	6-5

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DETAIL B (1)

LABEL POSITIONS
SCALE 1/2

NOTES:

(3) LOCATE APPROPRIATE VXI LABEL WHERE SHOWN. REFERENCE 921410 FOR SPECIFIC LABEL INFORMATION.

(2) APPLY LOCTITE 242 (ITEM 21) TO ALL SCREWS THAT DO NOT USE MECHANICAL LOCKING HARDWARE.

(1) LOCATE LABEL AS SHOWN IN DETAIL B.

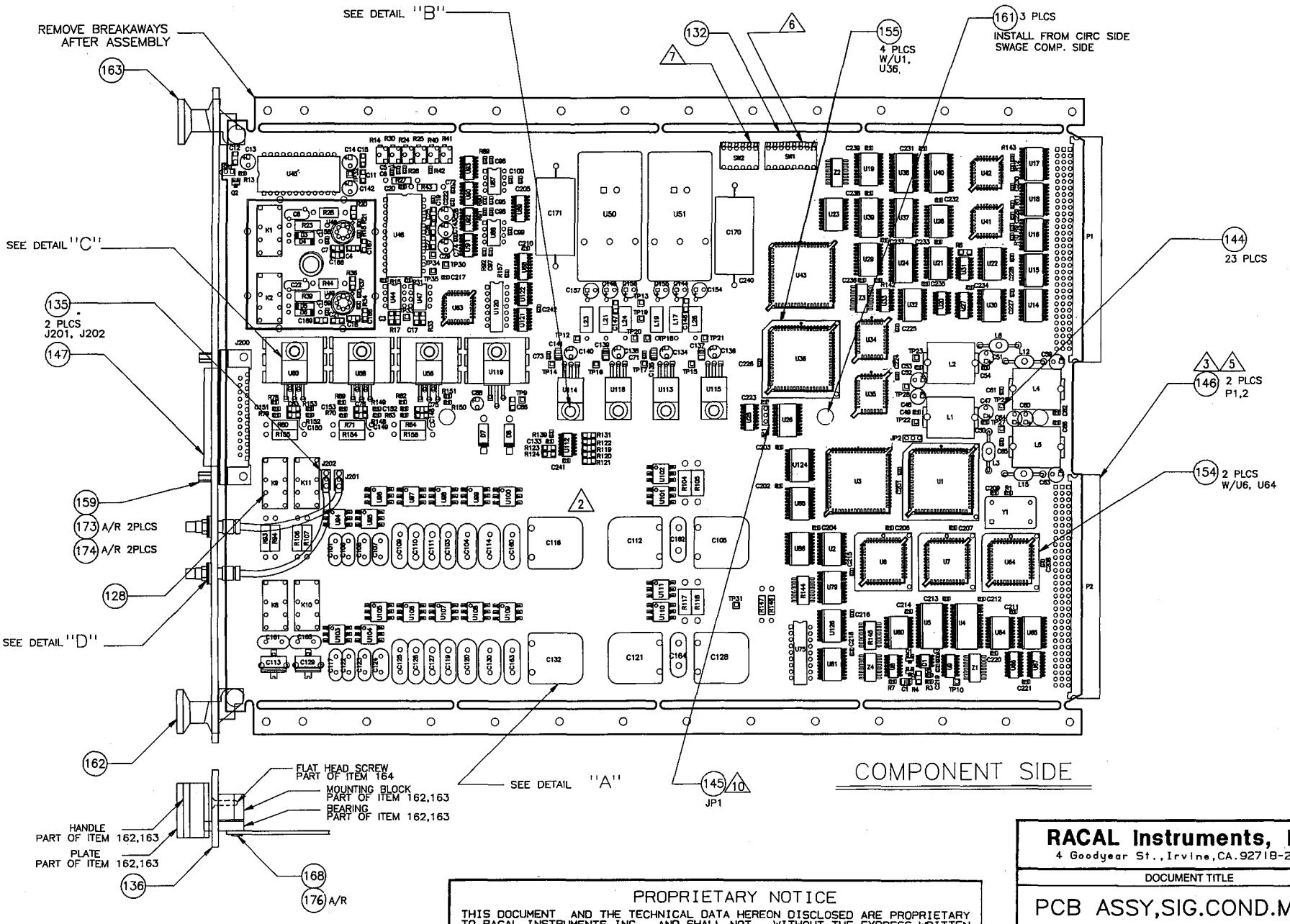
RACAL Instruments, Inc.
4 Goodyear St., Irvine, CA. 92718-2002

TITLE
FINAL ASSY, 6056

SIZE	CAGE CODE	DWG NO.	REV.
D	21793	407144-003	A

SCALE 1:2 | CALC. WT | ACT. WT | SHEET 1 OF 2

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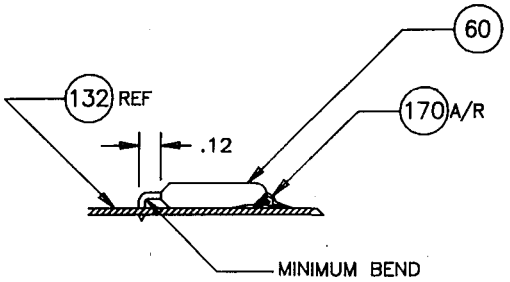


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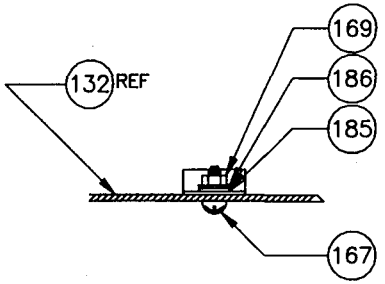
RACAL Instruments, Inc.			
4 Goodyear St., Irvine, CA. 92718-2002			
DOCUMENT TITLE			
PCB ASSY,SIG.COND.MOD			
SIZE	CODE IDENT NO.	DOCUMENT NO.	REV.
D	21793	405062-003	A
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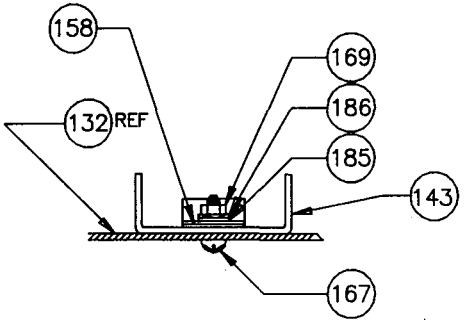
DETAIL "A"

SCALE: NONE
6 PLCS
C105,C112,C116,
C121,C128,C132.



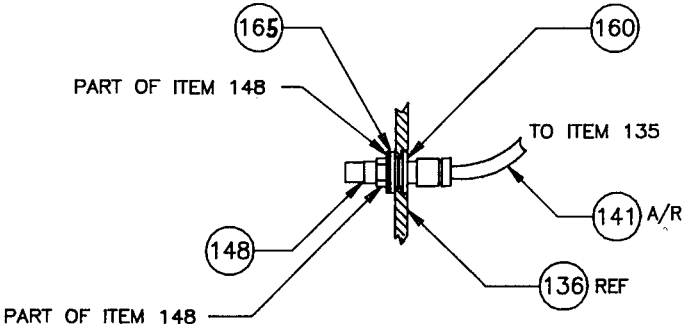
DETAIL "B"

SCALE: NONE
4 PLCS



DETAIL "C"

SCALE: NONE
4 PLCS



DETAIL "D"

SCALE: NONE
2 PLCS

10. INSTALL (ITEM 145) WITH SHORT PINS IN PCB (ITEM 132).

8. COMPONENTS NOT INSTALLED ON THIS ASSEMBLY:
C161, C165, C113, C129, TP1, TP29, U7(IC & SOCKET),
JP2, C6, C20, C158, C159

7. ALL POSITIONS ON SW2 (ITEM 150) SHOULD BE SET OFF EXCEPT FOR POSITIONS No 1 AND 3 (ON) . DO NOT WAVE SOLDER.

6. ALL POSITIONS ON SW1 (ITEM 149) SHOULD BE SET ON EXCEPT FOR POSITIONS No 1 AND 2 (OFF) . DO NOT WAVE SOLDER.

5. P1 AND P2 MUST BE INSTALLED FLUSH AT RIGHT ANGLE TO PCB.

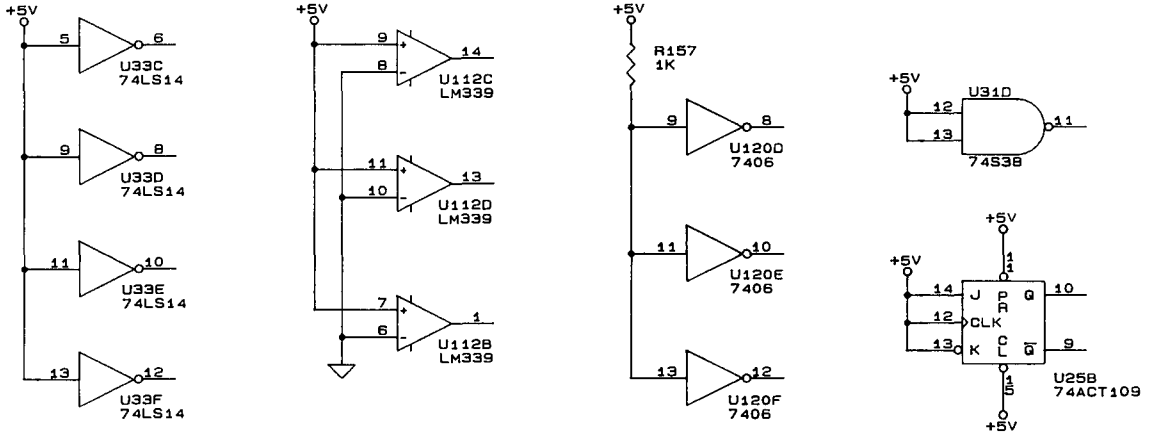
3. SOLDER TAILS ON CIRCUIT SIDE OF PCB FOR P1 AND P2 (ITEM 146) TO BE TRIMMED TO A MAXIMUM HEIGHT OF .045.

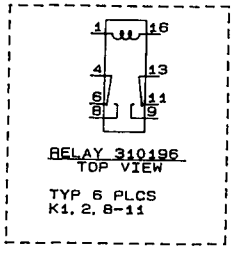
2. INK STAMP SERIAL NUMBER AND CURRENT REVISION ON COMPONENT SIDE APPROX. WHERE SHOWN.

1. REFERENCE SCHEMATIC 435062.

SIZE	CODE IDENT NO.	DOCUMENT NO.	REV.
D	21793	405062-003	A
SCALE		SHEET 1 OF 5	

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5. RELAYS SHOWN IN DE-ENERGIZED POSITION.

4. CAPACITOR VALUES ARE IN MICROFARADS, 50V, +/-10% UNLESS OTHERWISE SPECIFIED.

3. RESISTOR VALUES ARE IN OHMS, 1/16W, +/-5% UNLESS OTHERWISE SPECIFIED.

2. RESISTOR NETWORKS ARE IN OHMS, +/-2%.

1. PARTS NOT INSTALLED.

NOTES: UNLESS OTHERWISE SPECIFIED

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B	21793	435062	C

SCALE _____ SHEET 1 OF 21

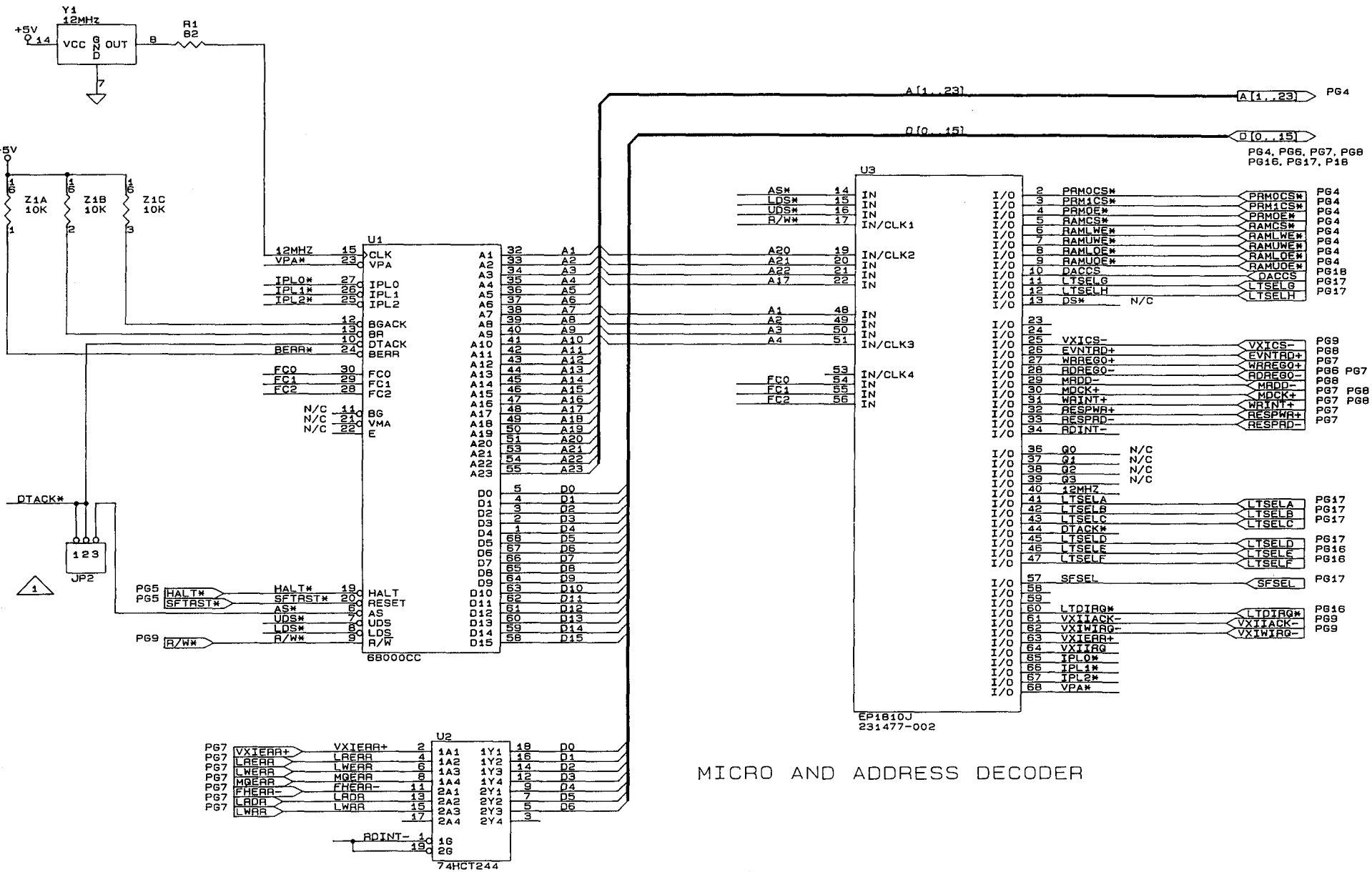
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IC POWER CONNECTIONS							
REFERENCE DESIGNATOR	IC TYPE	+5V PIN NO	GND PIN NO	+5VA	GND1	5VB	GND2
U1	68000	14, 52	15, 17, 56, 57				
U2 U22 U86 U126	74HCT244	20	10				
U3 231477-002	1810	18, 52	1, 35				
U4	4256-10	28	14				
U5	4256-10	28	14				
U6	27210	44	12, 34				
U7 231476-002 (NOT INSTALLED)	27210	44	12, 34				
U14 U15 U16 U19 U28 U32	74LS244	20	10				
U17 U18	74ALS645A-1	20	10				
U20	74LS30	14	7				
U21 U29	74F521	20	10				
U23	74ACT373	20	10				
U24 U37 U38 U39 U40	74HCT652	24	12				
U25	74ACT109	16	8				
U26	74LS273	20	10				
U27	74LS138	16	8				
U30 U65	74LS641-1	20	10				
U31	74S38	14	7				
U33	74LS14	14	7				
U34 231476-003	27C64	32	16				
U35 231476-004	27C64	32	16				
U36	1810	18, 52	1, 35				
U41 231477-001	22V10	28	14				
U42 231477-005	20RA10	28	15				
U43 231477-004	1810	18, 52	1, 35				
U120	7406	14	7				
U121 U122	74HCT74	14	7				
U63 231477-007	26V12	7	21				
U64 231477-006	7032	3, 15, 23, 35	10, 22, 30, 42				
U66 U67 U68	74F151	16	8				
U81 U84 U85 U124	74HCT273	20	10				
U79 U80	74ACT273	20	10				
U89	74LS175	16	8				
U90 U93	74HCT164			14	7		
U91 U92	74HCT164					14	7

HIGHEST REFERENCE DESIGNATOR
C242
CR1
D8
J202
JP2
K11
L26
P3
Q2
R157
SW2
TP35
U126
Y1
Z4

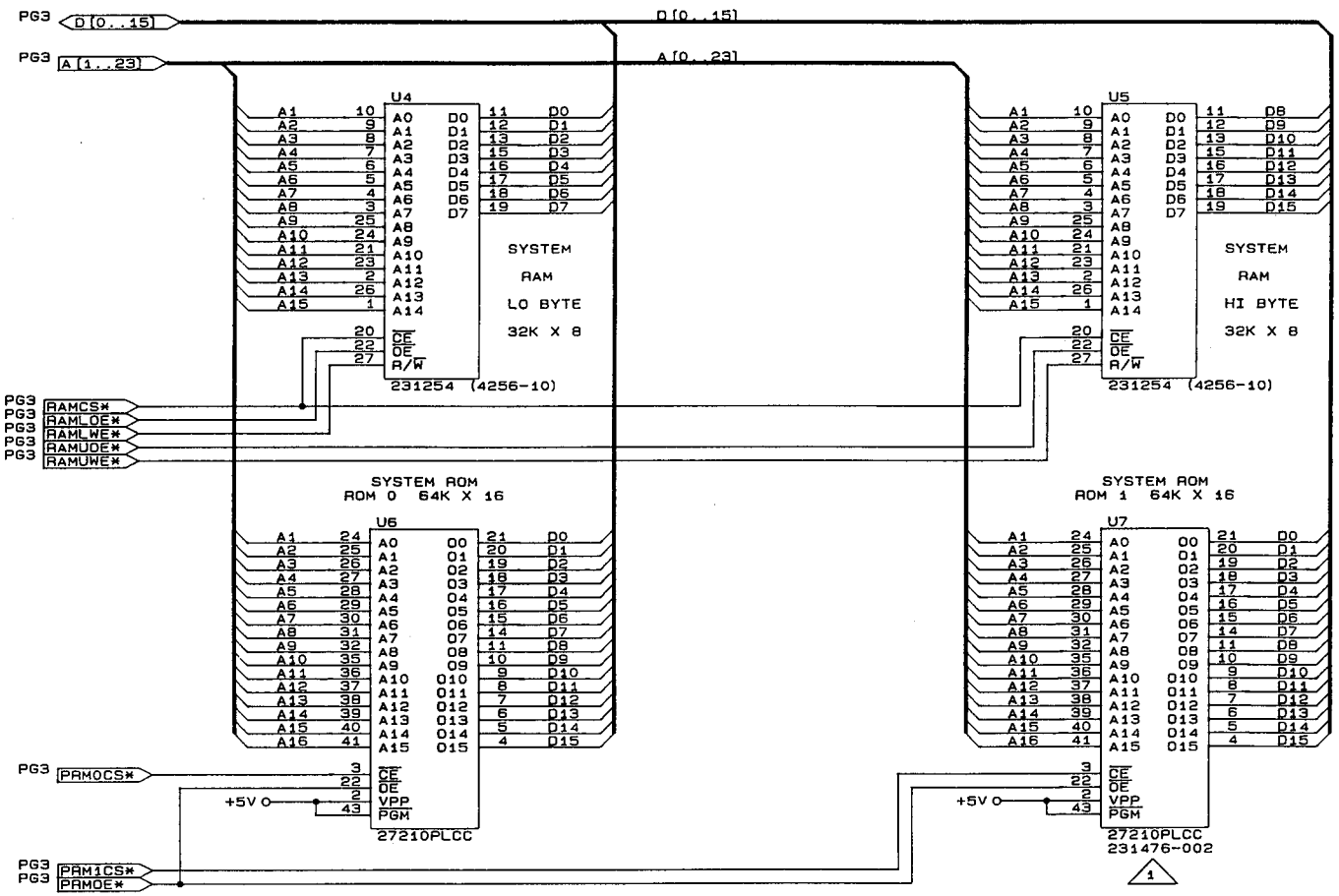
SIZE	CAGE CODE	DOCUMENT NO.	REV.
B	21793	435062	C
SCALE ———		SHEET 2	OF 21

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SIZE	CAGE CODE	DOCUMENT NO.	REV.
B	21793	435062	C
SCALE		SHEET 3 OF 21	

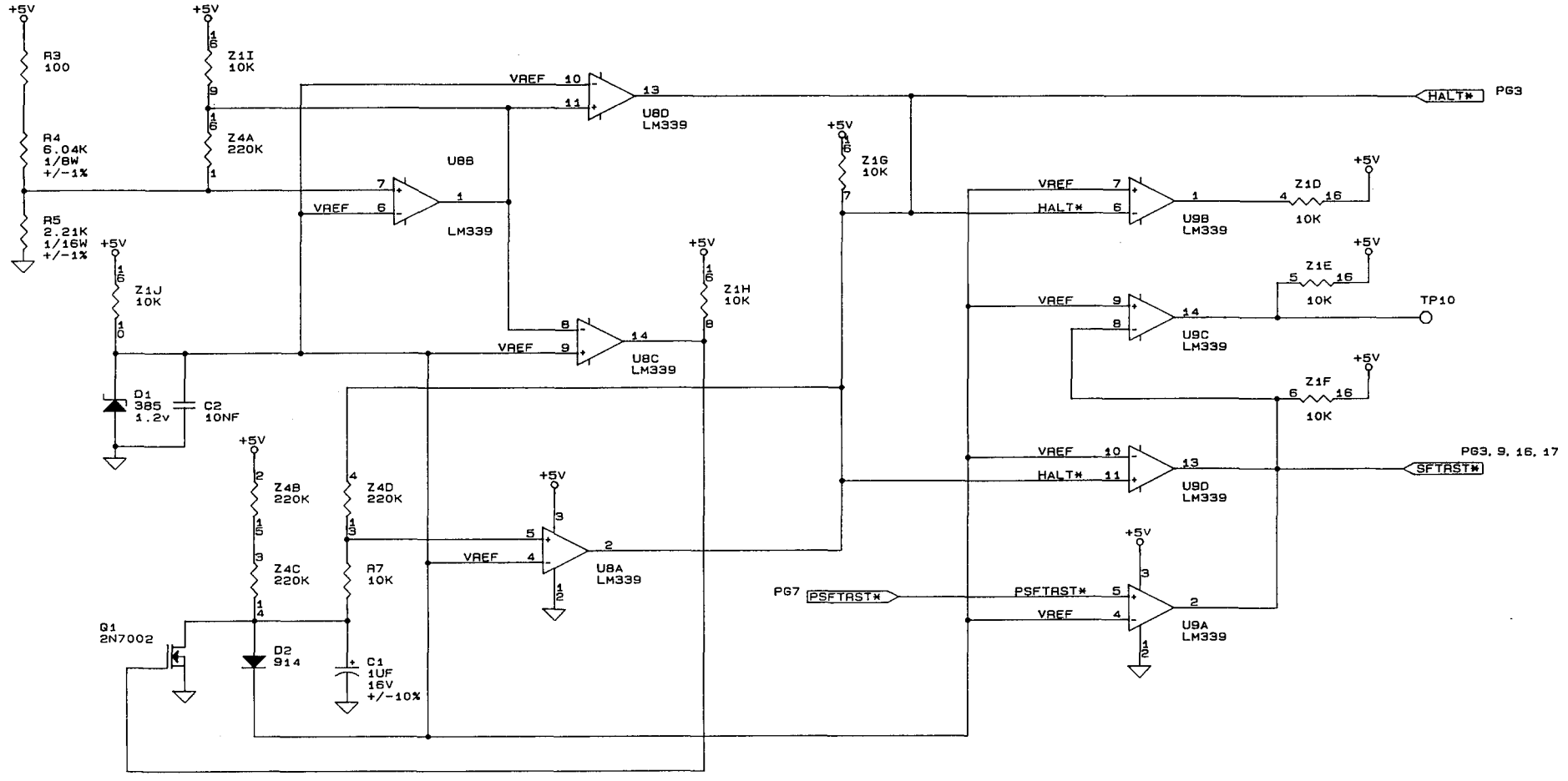
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ROM AND RAM

SIZE	CAGE CODE	DOCUMENT NO.	REV.
B	21793	435062	C
SCALE ———		SHEET 4 OF 21	

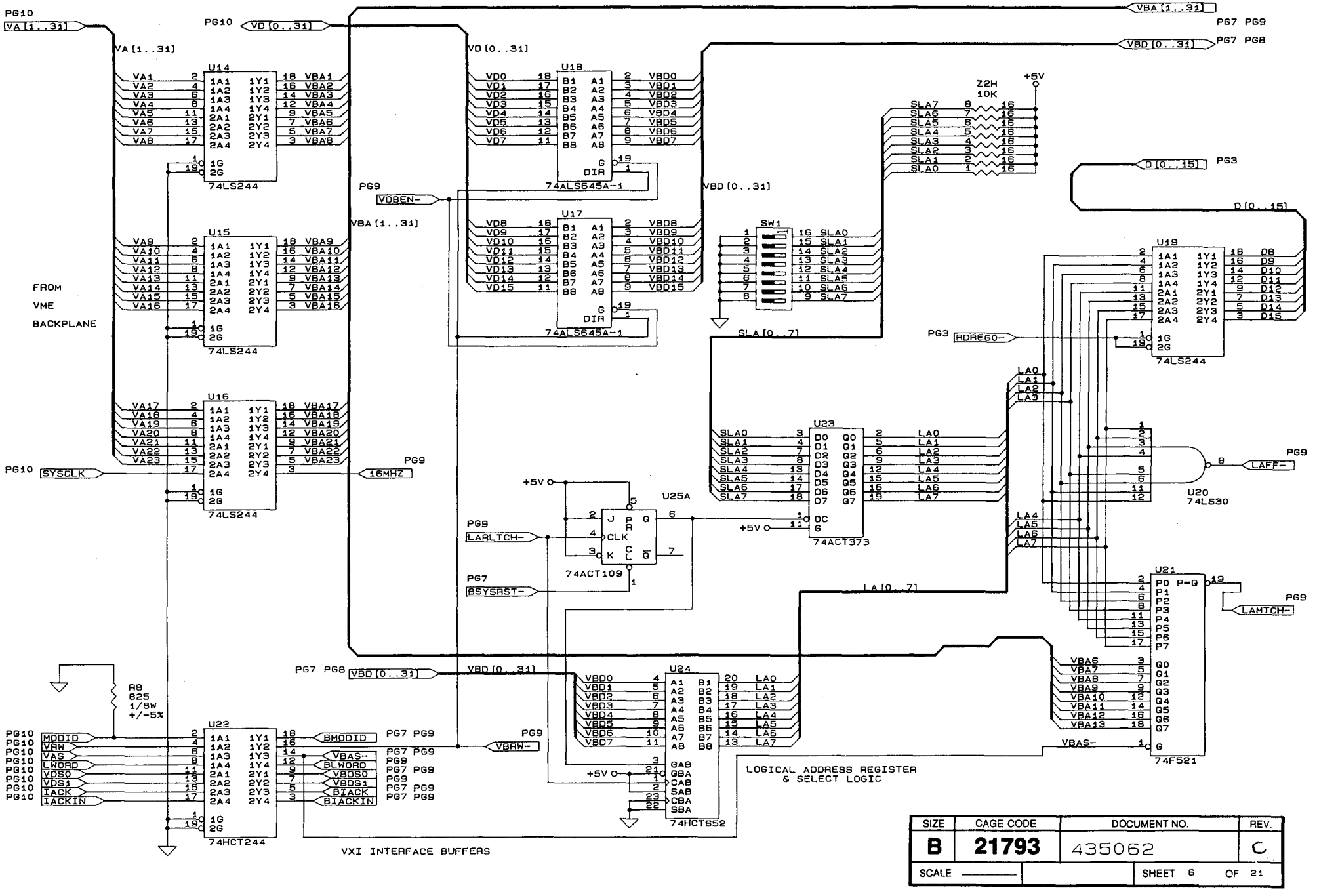
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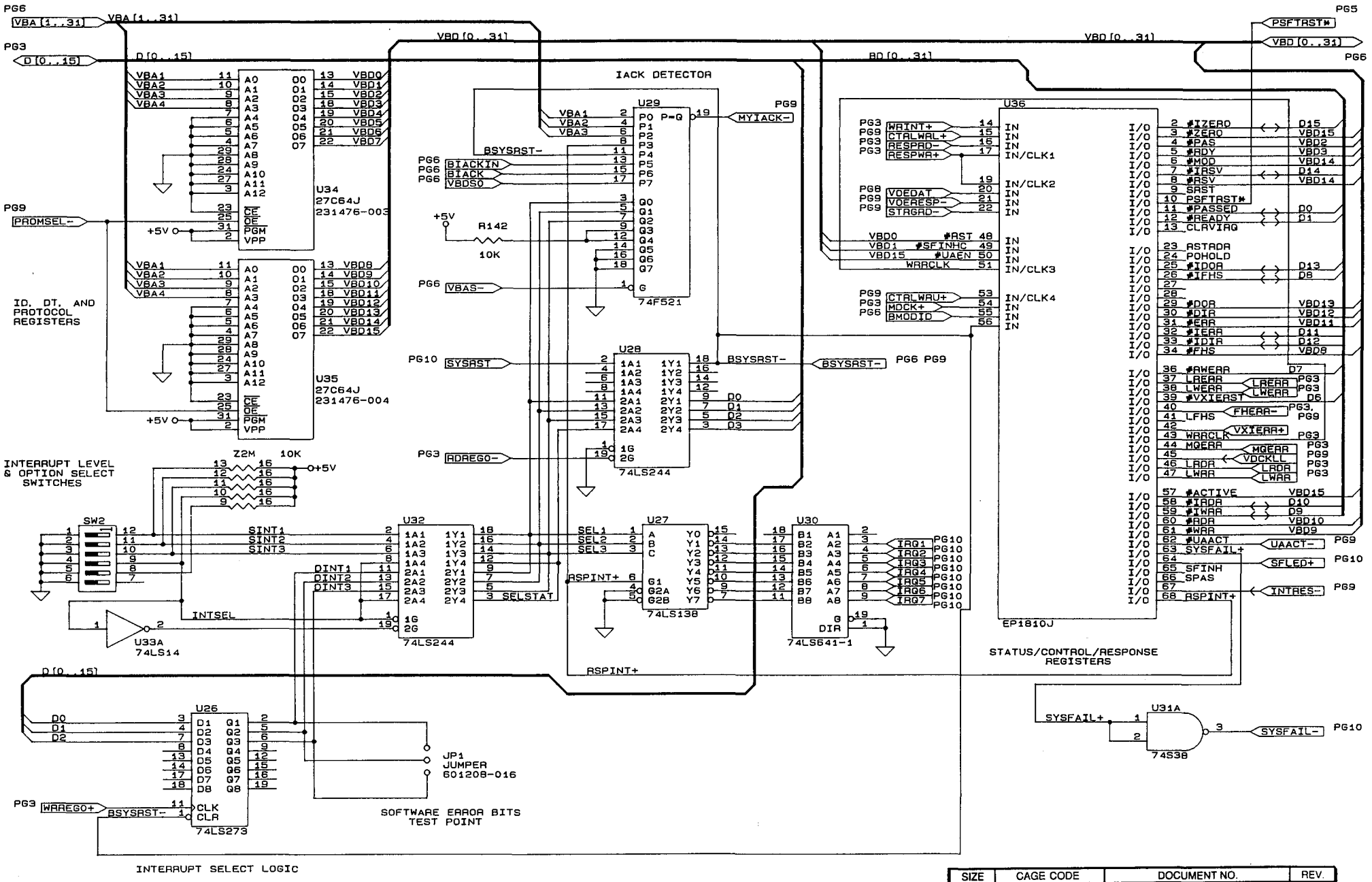
POWER ON RESET CIRCUIT

SIZE	CAGE CODE	DOCUMENT NO.	REV.
B	21793	435062	C
SCALE		SHEET 5 OF 21	

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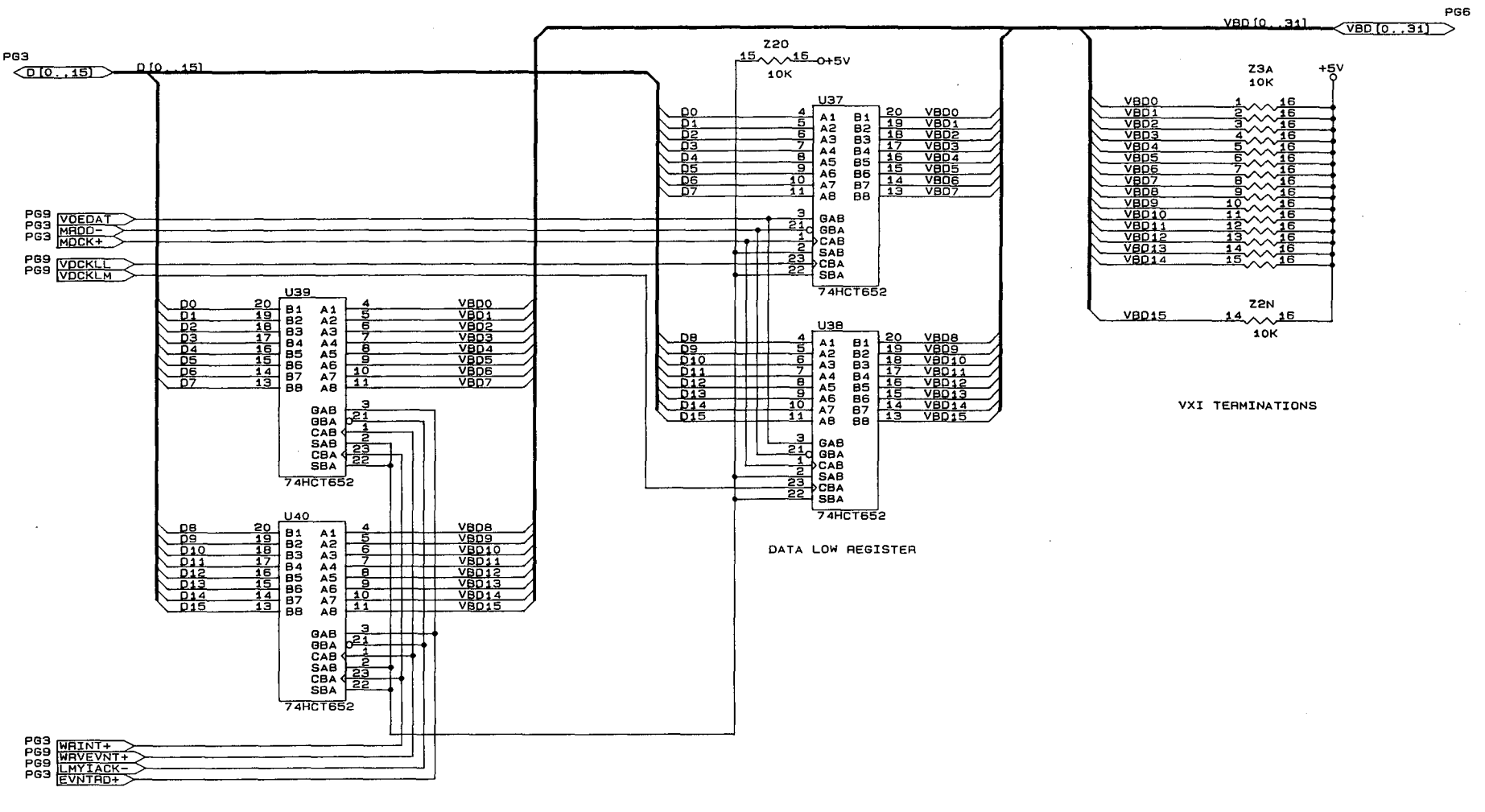


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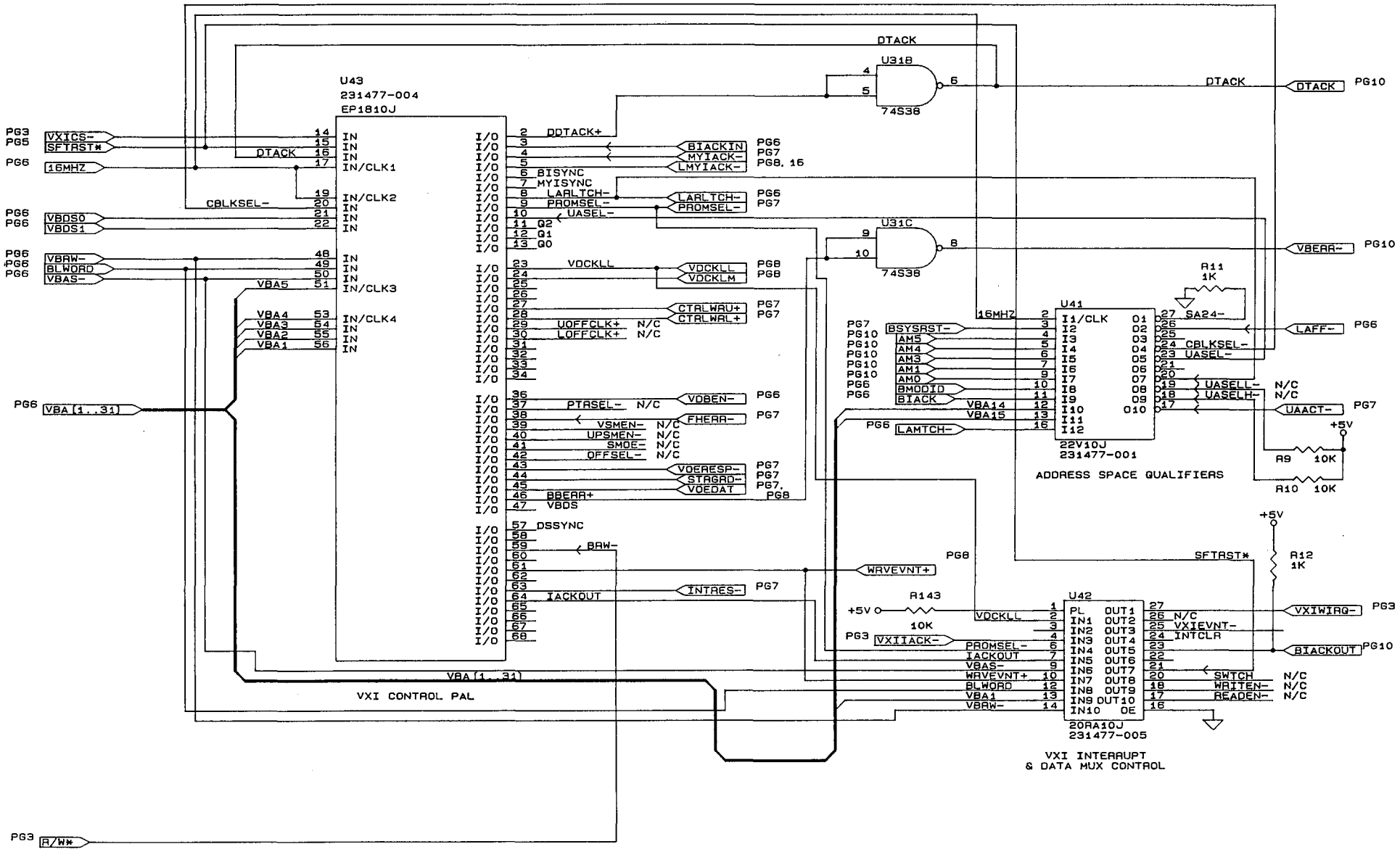
SIZE	CAGE CODE	DOCUMENT NO.	REV.
B	21793	435062	C
SCALE		SHEET 7	OF 21

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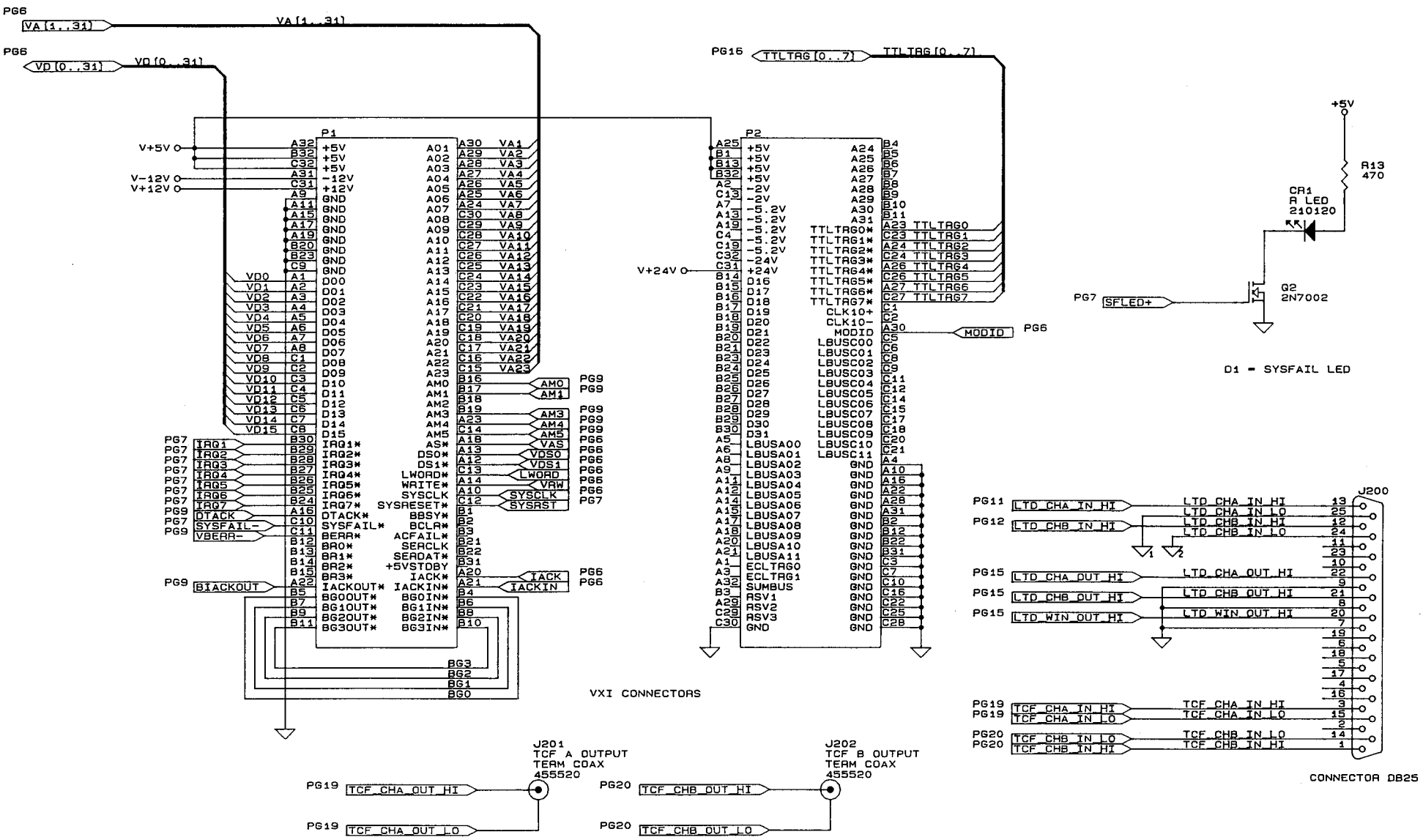
SIZE	CAGE CODE	DOCUMENT NO.	REV.
B	21793	435062	C
SCALE		SHEET 8 OF 21	

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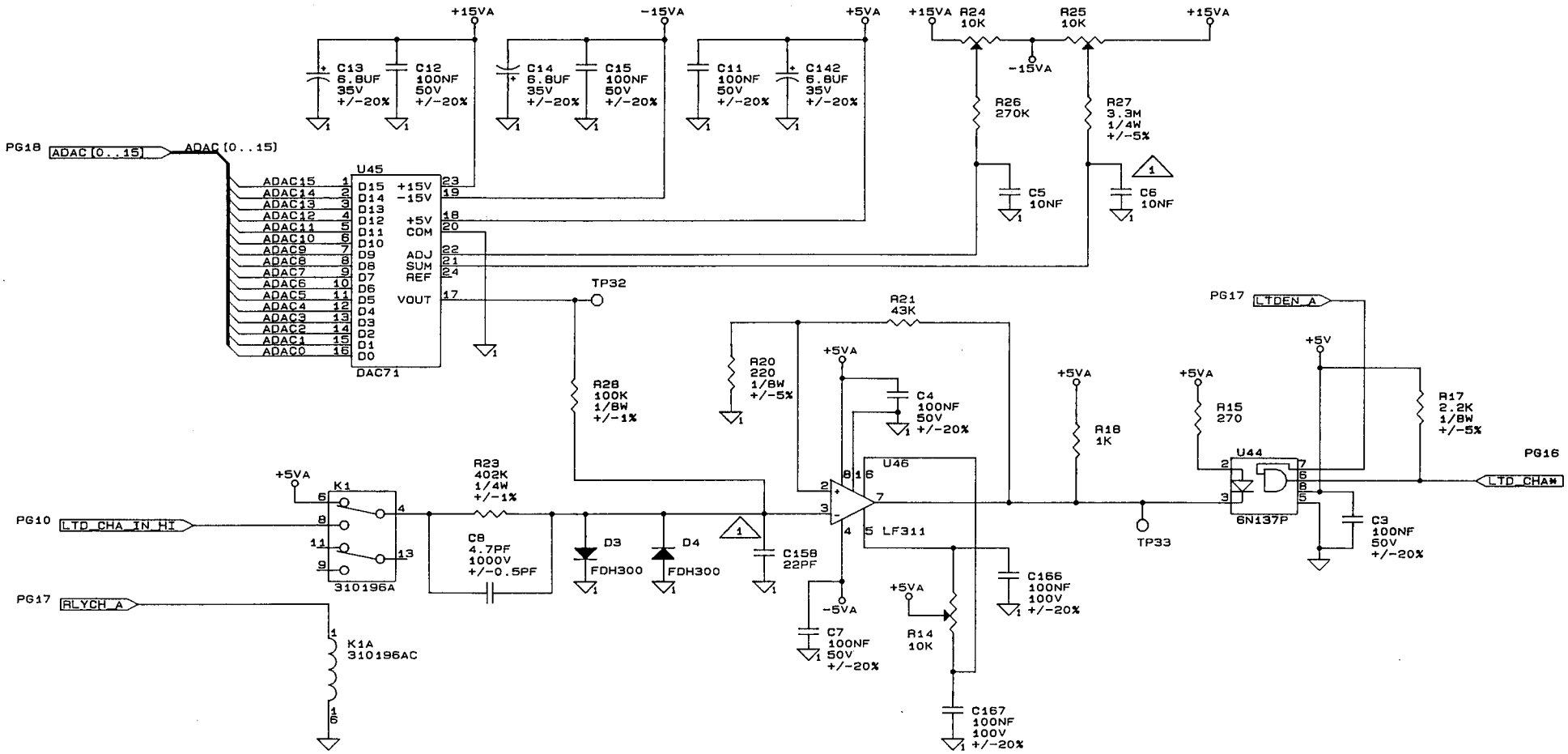
SIZE	CAGE CODE	DOCUMENT NO.	REV.
B	21793	435062	C
SCALE		SHEET 9 OF 21	

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SIZE	CAGE CODE	DOCUMENT NO.	REV.
B	21793	435062	C
SCALE		SHEET 10 OF 21	

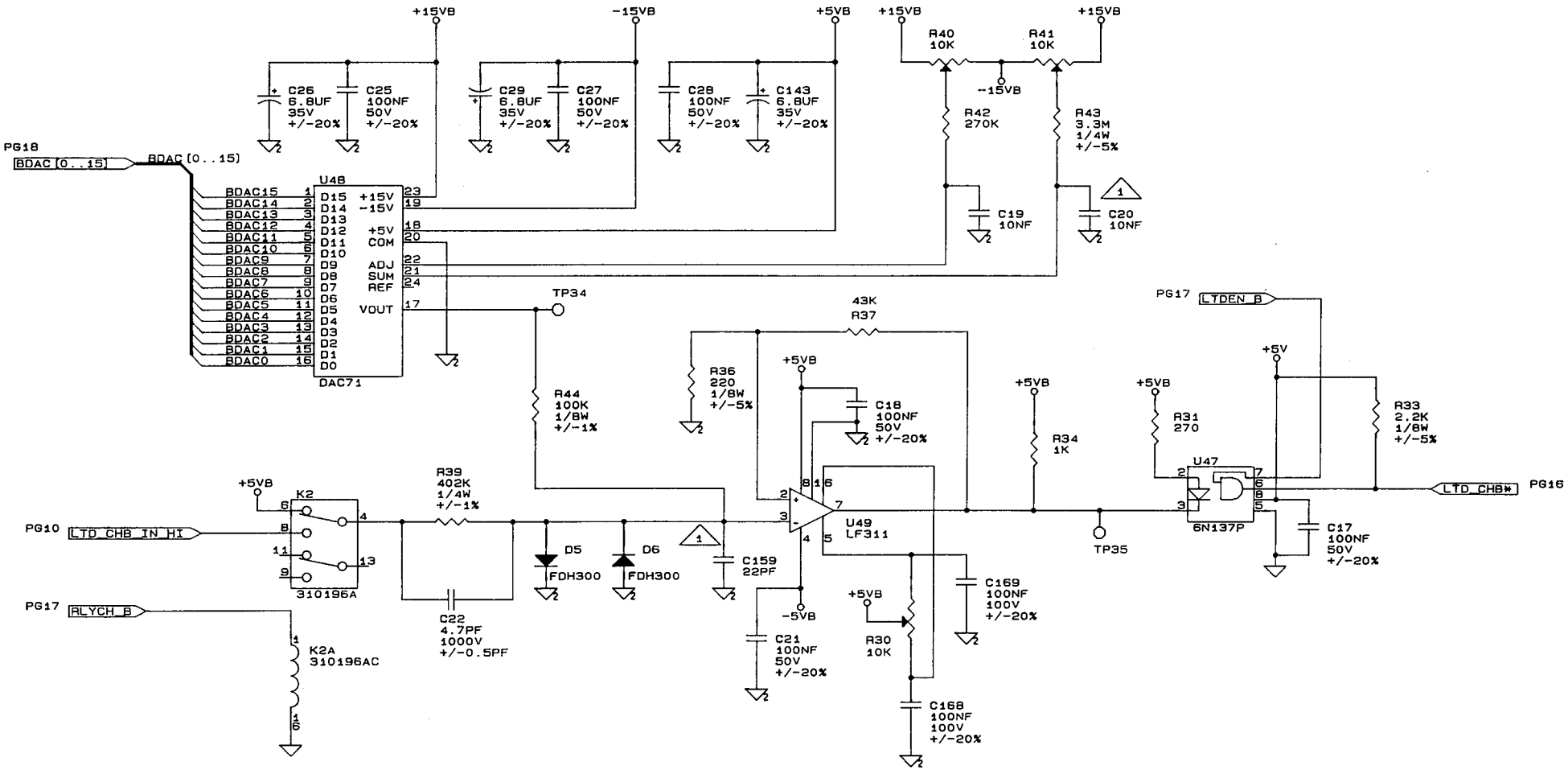
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CHANNEL A THRESHOLD DETECTOR

SIZE	CAGE CODE	DOCUMENT NO.	REV.
B	21793	435062	C
SCALE		SHEET 11 OF 21	

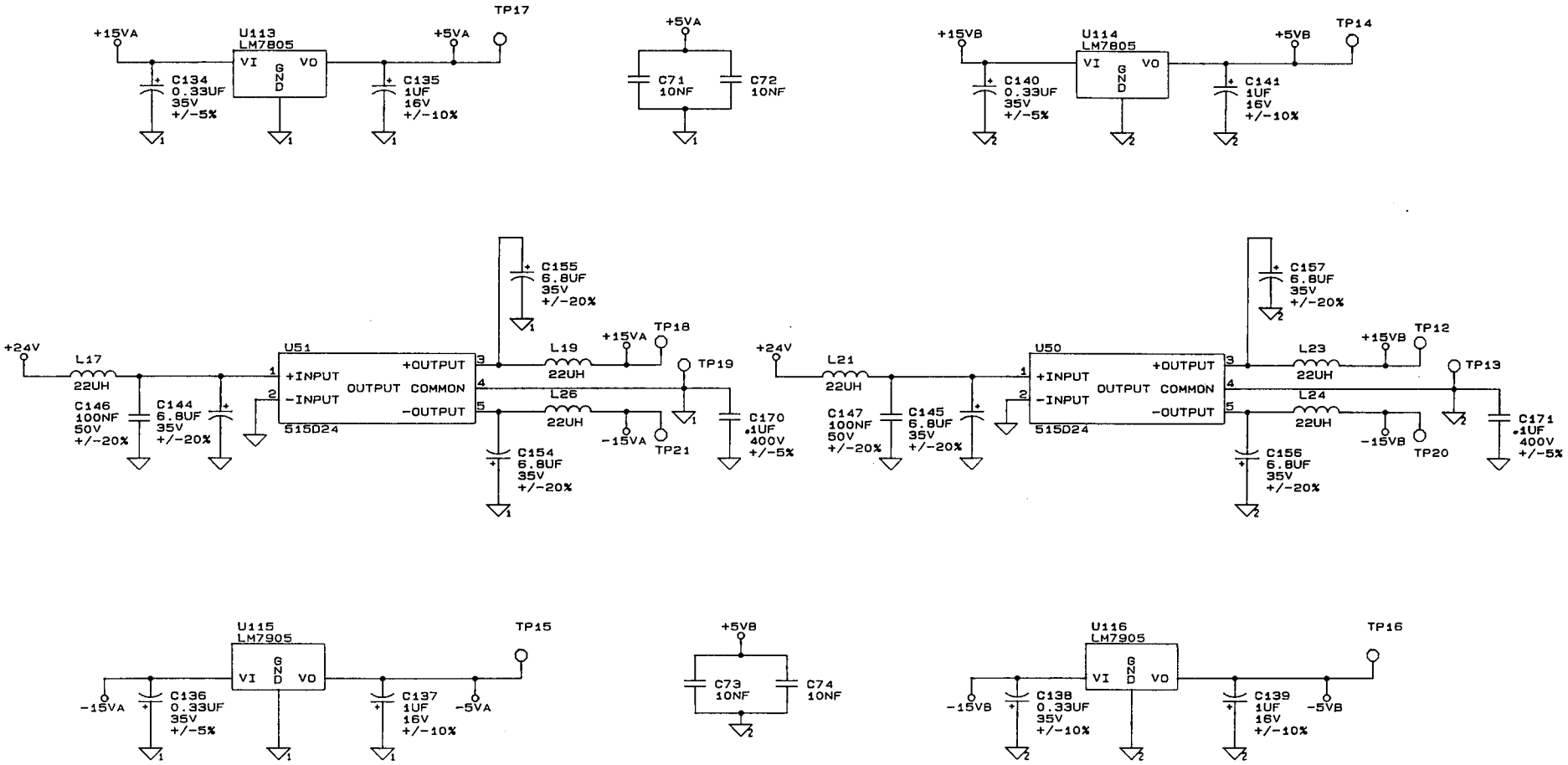
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CHANNEL B THRESHOLD DETECTOR

SIZE	CAGE CODE	DOCUMENT NO.	REV.
B	21793	435062	C
SCALE		SHEET 12 OF 21	

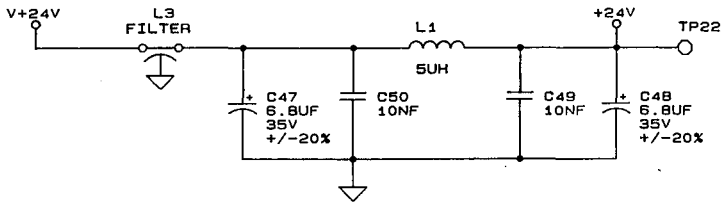
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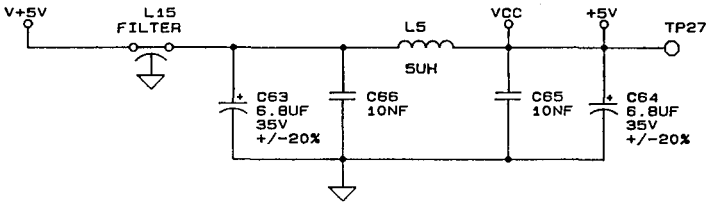


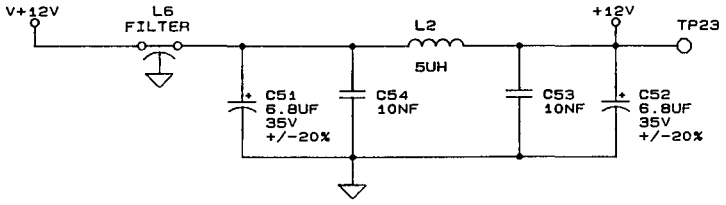
DC - DC CONVERTORS AND REGULATOR CIRCUITS

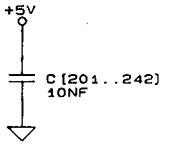
SIZE	CAGE CODE	DOCUMENT NO.	REV.
B	21793	435062	C
SCALE ———		SHEET 13 OF 21	

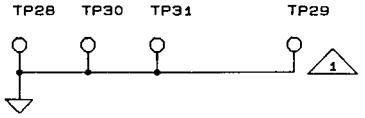
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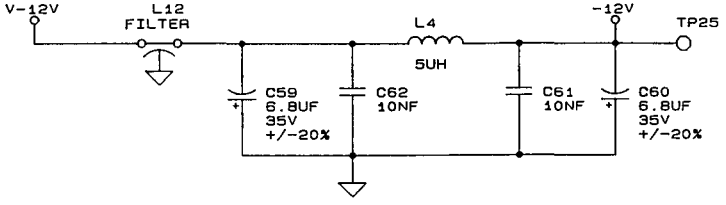






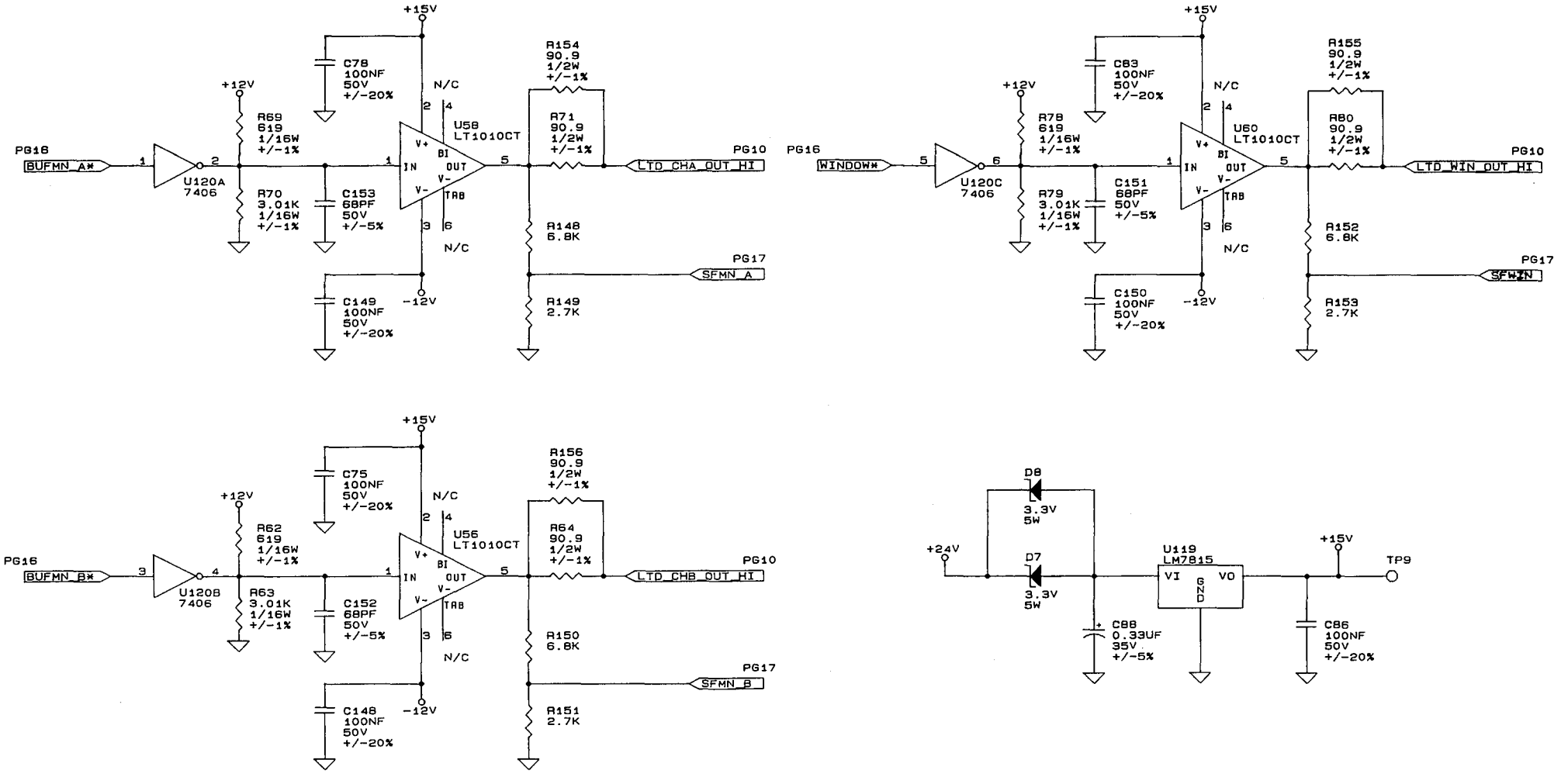






SIZE	CAGE CODE	DOCUMENT NO.	REV.
B	21793	435062	C
SCALE ———		SHEET 14 OF 21	

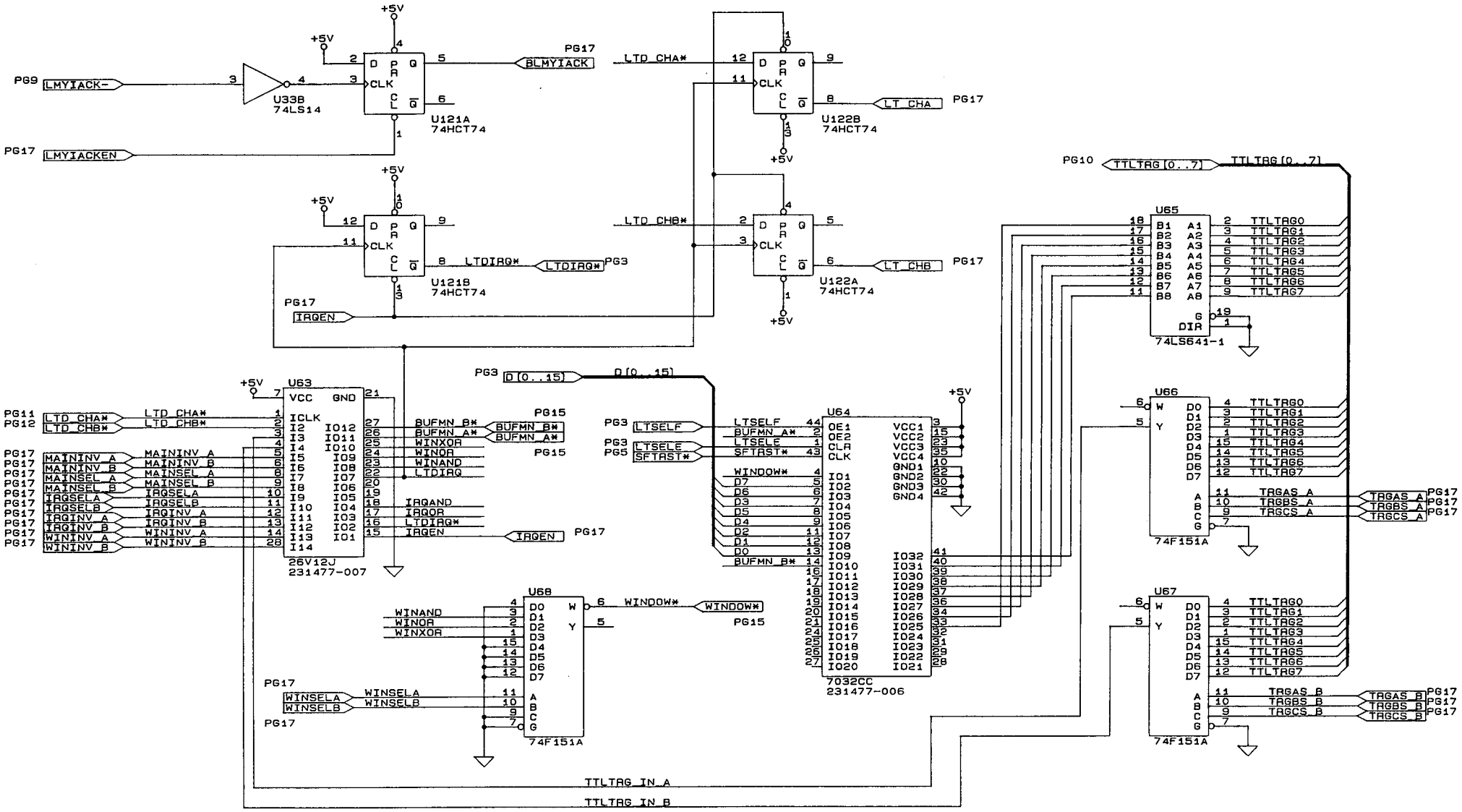
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CHAN A, CHAN B AND WINDOW OUTPUTS

SIZE	CAGE CODE	DOCUMENT NO.	REV.
B	21793	435062	C
SCALE		SHEET 15 OF 21	

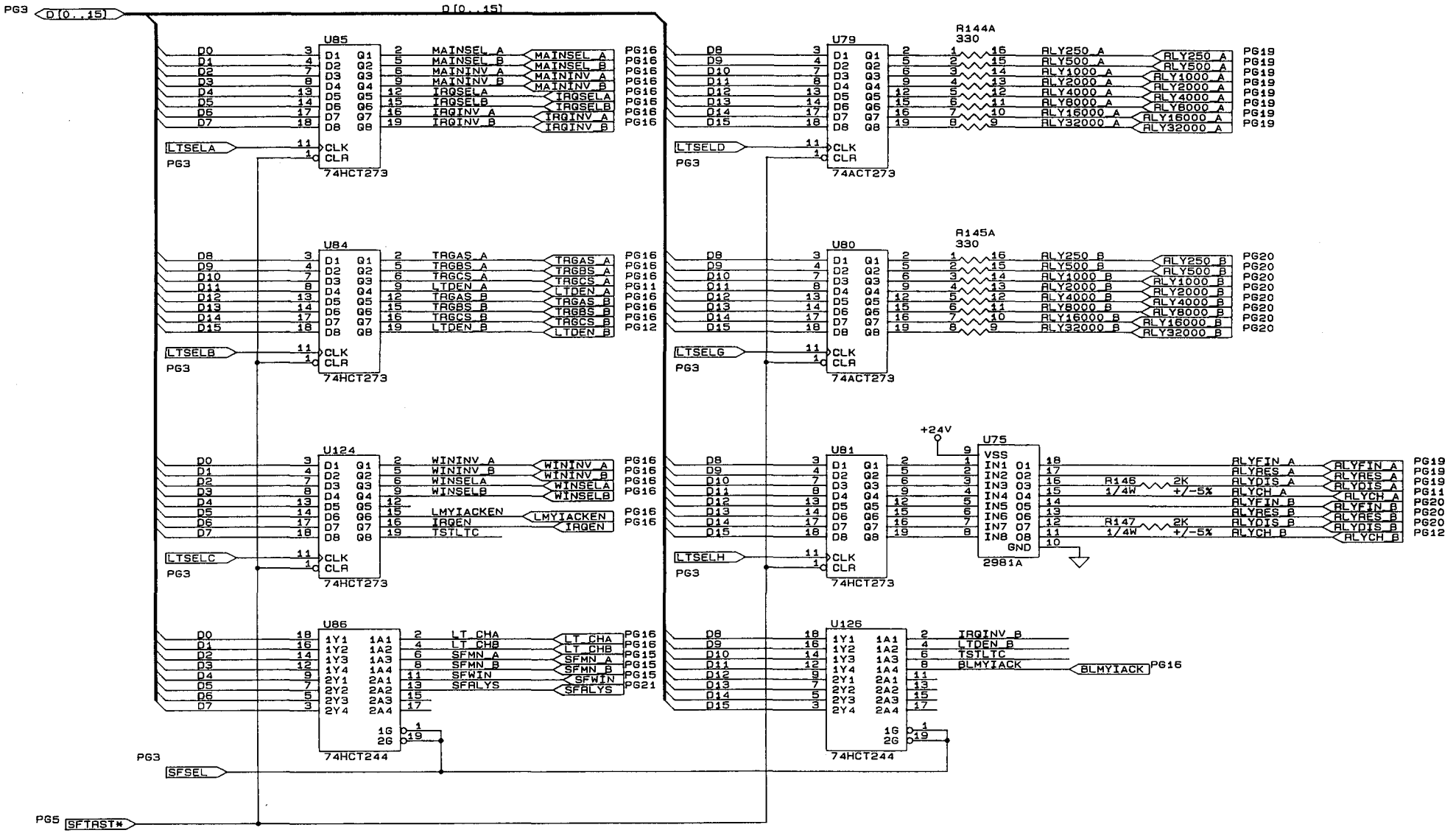
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WINDOW LOGIC

SIZE	CAGE CODE	DOCUMENT NO.	REV.
B	21793	435062	C
SCALE		SHEET 16 OF 21	

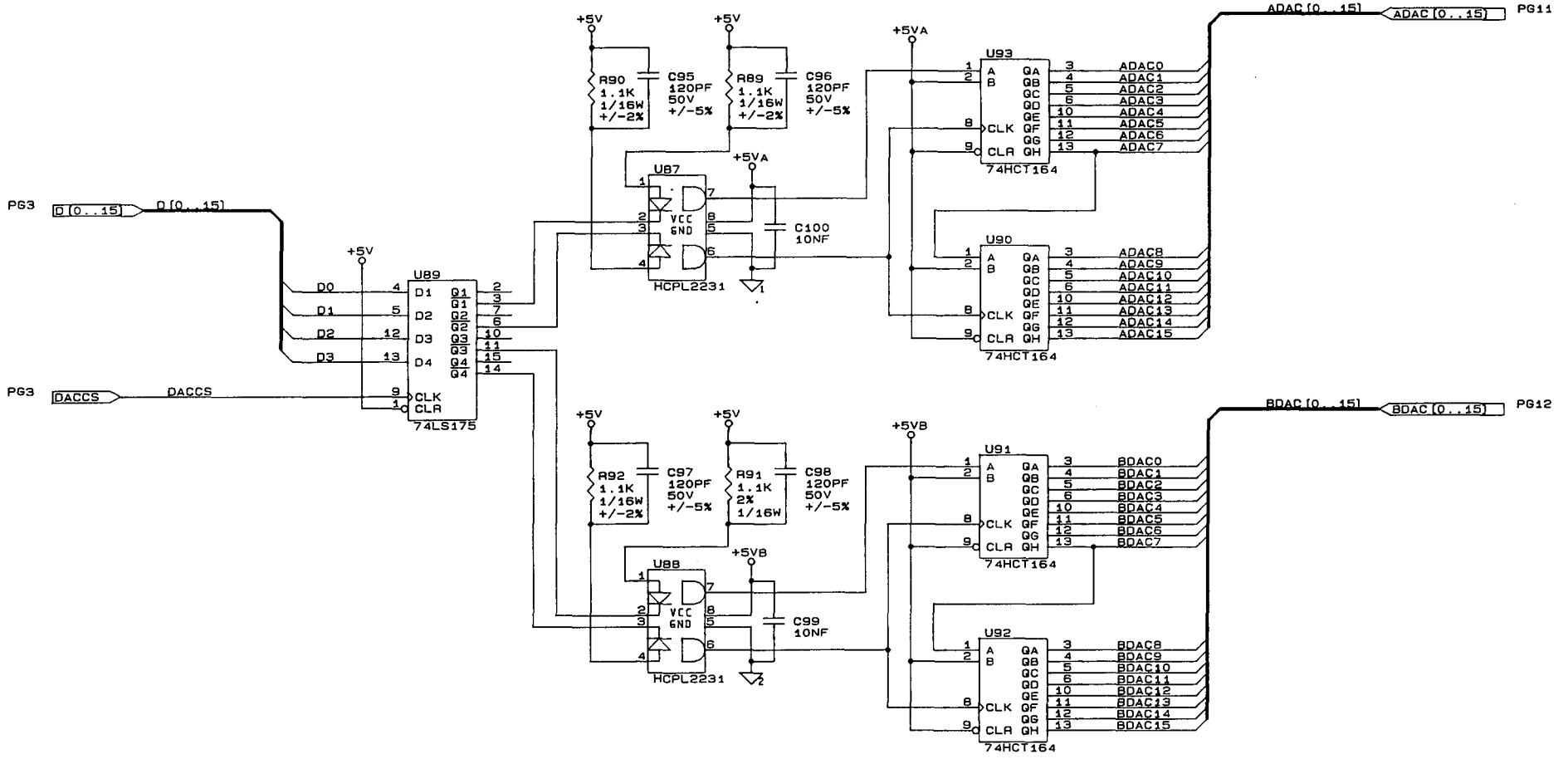
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CONTROL LATCHES AND SELFTEST BUFFER

SIZE	CAGE CODE	DOCUMENT NO.	REV.
B	21793	435062	C
SCALE ———		SHEET 17 OF 21	

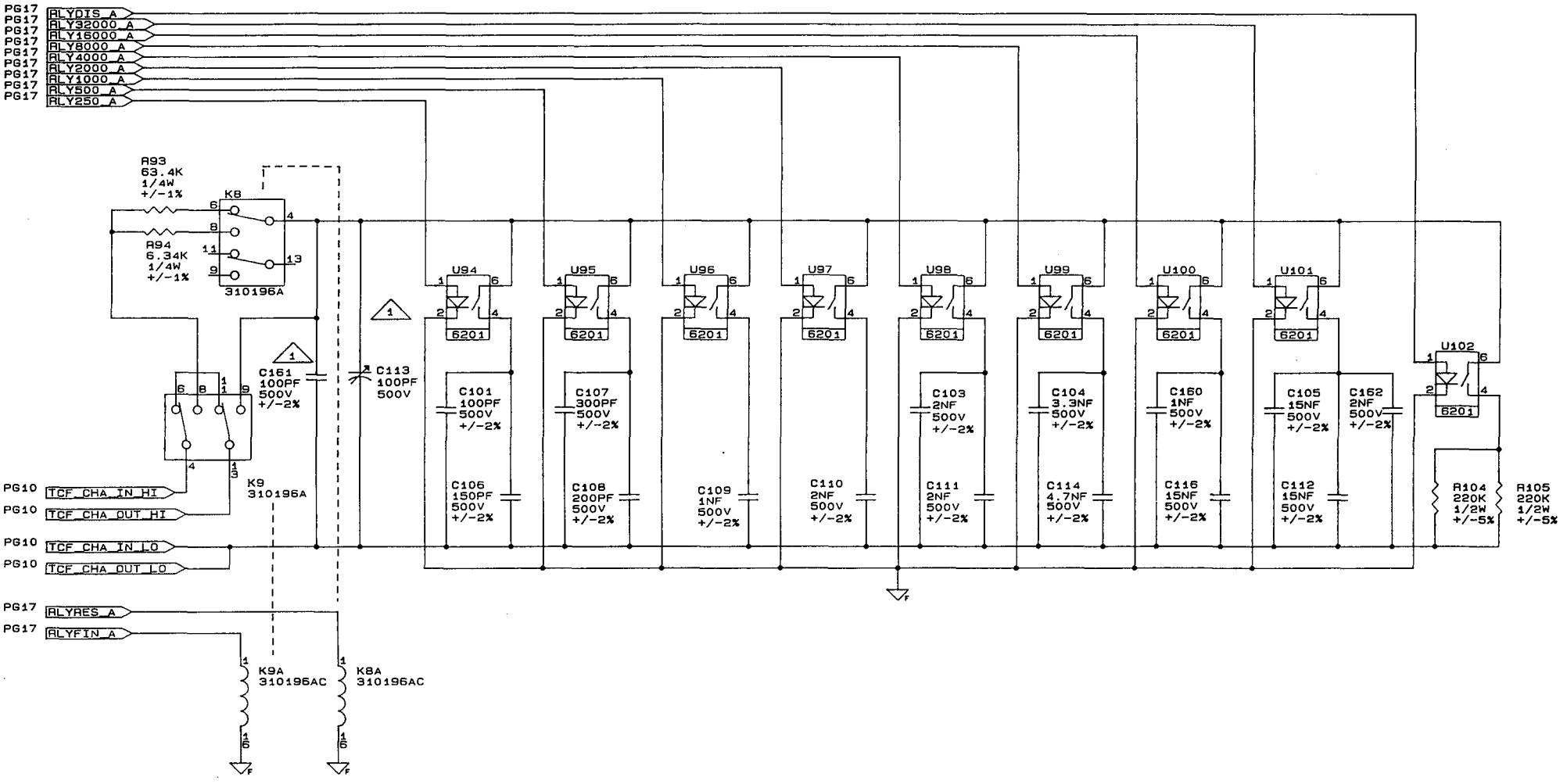
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DAC INTERFACE

SIZE	CAGE CODE	DOCUMENT NO.	REV.
B	21793	435072	C
SCALE		SHEET 18 OF 21	

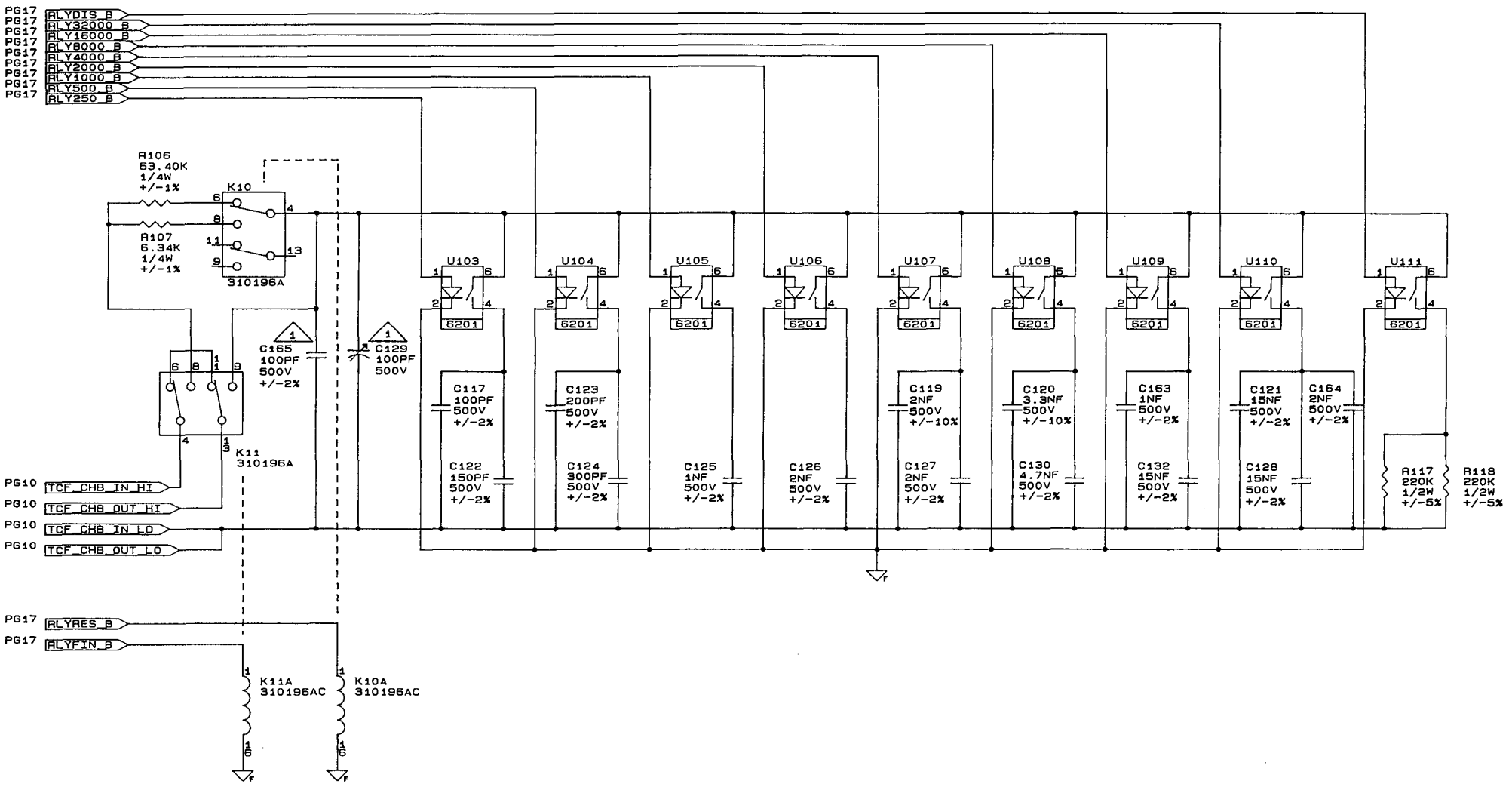
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CHANNEL A TIME CONSTANT FILTER

SIZE	CAGE CODE	DOCUMENT NO.	REV.
B	21793	435062	C
SCALE		SHEET 19 OF 21	

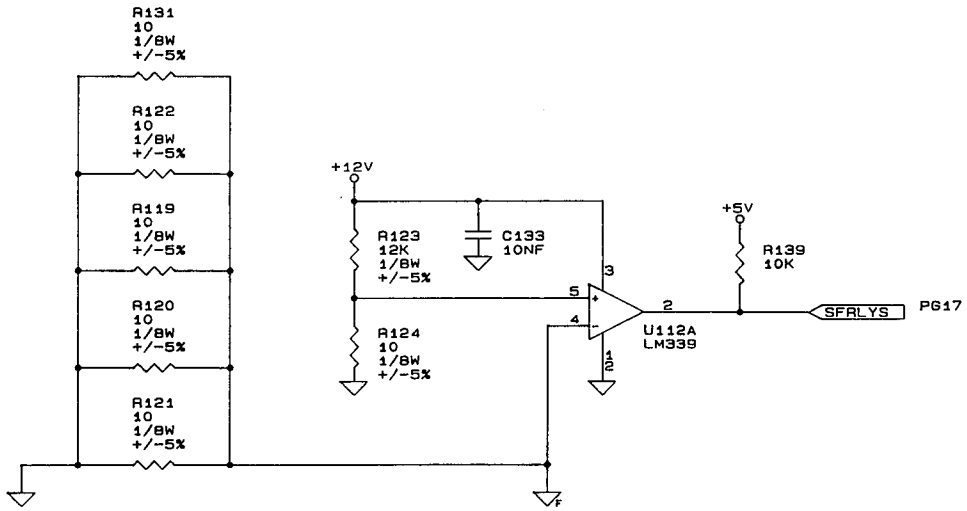
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CHANNEL B TIME CONSTANT FILTER

SIZE	CAGE CODE	DOCUMENT NO.	REV.
B	21793	435062	C
SCALE ———		SHEET 20 OF 21	

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RELAY SELFTEST COMPARATORS

SIZE	CAGE CODE	DOCUMENT NO.	REV.
B	21793	435062	C
SCALE ———		SHEET 21 OF 21	

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407144-003 Final Assembly, 6056 7-4

405062-003 PCB Assy, 6056 7-5

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FSC	SUPPLIER
00779	AMP, INC. HARRISBURG, PA
01139	GENERAL ELECTRIC CO. (SILICONE PRODUCTS) WATERFORD, NY
01295	TEXAS INSTRUMENTS, INC. DALLAS, TX
04713	MOTOROLA, INC. (SEMICONDUCTOR PRODUCTS DIV.) PHOENIX, AZ
05397	UNION CARBIDE CORP. (MATERIALS SYSTEMS DIV.) CLEVELAND, OH
05972	LOCTITE CORP. HARTFORD, CT
06540	AMATOM ELECTRONIC HARDWARE NEW ROCHELLE, NY
07263	FAIRCHILD (SEMICONDUCTOR DIV.) MOUNTAIN VIEW, CA
09023	CORNELL-DUBILIER ELECTRONICS SANFORD, NC
11236	CTS OF BERNE, INC. BERNE, IN
13103	THERMALLOY, INC. DALLAS, TX
17856	SILICONIX, INC. SANTA CLARA, CA
18324	SIGNETICS, INC. SUNNYVALE, CA
18565	CHOMERICS, INC. WOBURN, MA
1CJ86	BOSSARD BROOKFIELD, CT
21793	RACAL INSTRUMENTS INC. IRVINE, CA
24355	ANALOG DEVICES NORWOOD, MA
27014	NATIONAL SEMI-CONDUCTOR CORP. SANTA CLARA, CA
27556	IMB ELECTRONIC PRODUCTS INC. SANTA FE SPRINGS, CA
29005	STORM PRODUCTS CO. LOS ANGELES, CA
50434	HEWLETT-PACKARD CO. (HPA DIV.) PALO ALTO, CA
52072	CIRCUIT ASSY. CORP. COSTA MESA, CA
55322	SAMTEC, INC NEW ALBANY, IN
56235	PRECISION STDS CORP. (BIRTCHER SEMI-CONDUCTOR DIV.) SANTA ANA, CA
56289	SPAGUE ELECTRIC CO. N. ADAMS, MA
61441	SARONIX PALO ALTO, CA
61529	AROMAT CORP. CUPERTINO, CA
62559	SCHROFF, INC. WARWICK, RI
64155	LINEAR TECHNOLOGY CORP. MILPITAS, CA
65940	ROHM CORP. IRVINE, CA
71707	COTO-COIL CO., INC. PROVIDENCE, RI
72982	ERIE TECHNOLOGICAL PRODUCTS, INC. ERIE, PA
80294	BOURNS INSTRUMENTS INC. RIVERSIDE, CA
81349	MILITARY SPECIFICATION
86928	SEASTROM MFG. CO. GLENDALE, CA
91637	DALE ELECTRONICS, INC. COLUMBUS, NE
91802	INDUSTRIAL DEVICES INC. EDGEWATER, NJ
92194	ALPHA WIRE ELIZABETH, NJ
95146	ALCO ELECTRONIC PRODUCTS INC. NORTH ANDOVER, MA

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List of Suppliers continued

FSC	SUPPLIER
95275	VITRAMON, INC. BRIDGEPORT, CT
98291	SEALECTRO CORP. MAMARONECK, NY
99800	AMERICAN PRECISION INDUSTRIES, INC. (DELEVAN DIV.) EAST AURORA, NY
K1935	JERMYN MANUFACTURING KENT, ENGLAND
MATSU	MATSUO ELECTRONICS HUNTINGTON BEACH, CA
OAK51	CONVERSION DEVICES BROCKTON, MA

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407144-003 - 6056, SIGNAL CONDITIONER

REF DESIG	RACAL INST P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
{1}1	405062-003	PCB ASSY., 6056	21793	405062-003
{4}1	456108	PANEL, TOP, 6056	21793	456108
{5}1	455784-002	PANEL, VXI BOTTOM	21793	455784-002
{7}1	455779	PANEL, SIDE	21793	455779
{8}1	455779-001	PANEL, STD SIDE, 3SCR, LEFT	21793	455779-001
{10}31	615539	SCREW, PFH, 4-40X. 125	-	-
{11}8	616480	SCREW, PFH, 4-40 X .375	-	-
{14}1	921059	LABEL, CAUTION, STATIC	21793	921059
{16}1	980727	INSTRUCTION MANUAL, 6056	21793	980727
{17}1	455781	PANEL, REAR, SINGLE	21793	455781
{21}A/R	920962	LOCTITE, 242, MED STR.	05972	272

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405062-003 - PCB ASSY., SIGNAL CONDITIONER MOD.

REF DESIG	RACAL INST P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
C1	110244	CAP TANTA 1.0 MF, 16V, 10 PCT	MATSU	267M1602105K
C2	100152-103	CAP,CHIP, 10NF, 50V, 10PCT	95275	VJ0805Y103KXAAT
C3	R-21-1802	CAP, CHIP, 100 NF	95275	VJ1206Y104MF
C4	R-21-1802	CAP, CHIP, 100 NF	95275	VJ1206Y104MF
C5	100152-103	CAP,CHIP, 10NF, 50V, 10PCT	95275	VJ0805Y103KXAAT
C7	R-21-1802	CAP, CHIP, 100 NF	95275	VJ1206Y104MF
C8	100081	CAP, CERAM, 4.7PF, 1000V, 5PCT	56289	C030B102E4R7D
C11	R-21-1802	CAP, CHIP, 100 NF	95275	VJ1206Y104MF
C12	R-21-1802	CAP, CHIP, 100 NF	95275	VJ1206Y104MF
C13	110126	CAP, TANTA, 6.8UF, 35V, 20 PERCENT	05397	T355F685M035A5
C14	110126	CAP, TANTA, 6.8UF, 35V, 20 PERCENT	05397	T355F685M035A5
C15	R-21-1802	CAP, CHIP, 100 NF	95275	VJ1206Y104MF
C17	R-21-1802	CAP, CHIP, 100 NF	95275	VJ1206Y104MF
C18	R-21-1802	CAP, CHIP, 100 NF	95275	VJ1206Y104MF
C19	100152-103	CAP,CHIP, 10NF, 50V, 10PCT	95275	VJ0805Y103KXAAT
C21	R-21-1802	CAP, CHIP, 100 NF	95275	VJ1206Y104MF
C22	100081	CAP, CERAM, 4.7PF, 1000V, 5PCT	56289	C030B102E4R7D
C25	R-21-1802	CAP, CHIP, 100 NF	95275	VJ1206Y104MF
C26	110126	CAP, TANTA, 6.8UF, 35V, 20 PERCENT	05397	T355F685M035A5
C27	R-21-1802	CAP, CHIP, 100 NF	95275	VJ1206Y104MF
C28	R-21-1802	CAP, CHIP, 100 NF	95275	VJ1206Y104MF
C29	110126	CAP, TANTA, 6.8UF, 35V, 20 PERCENT	05397	T355F685M035A5
C47	110126	CAP, TANTA, 6.8UF, 35V, 20 PERCENT	05397	T355F685M035A5
C48	110126	CAP, TANTA, 6.8UF, 35V, 20 PERCENT	05397	T355F685M035A5
C49	100152-103	CAP,CHIP, 10NF, 50V, 10PCT	95275	VJ0805Y103KXAAT
C50	100152-103	CAP,CHIP, 10NF, 50V, 10PCT	95275	VJ0805Y103KXAAT
C51	110126	CAP, TANTA, 6.8UF, 35V, 20 PERCENT	05397	T355F685M035A5
C52	110126	CAP, TANTA, 6.8UF, 35V, 20 PERCENT	05397	T355F685M035A5
C53	100152-103	CAP,CHIP, 10NF, 50V, 10PCT	95275	VJ0805Y103KXAAT
C54	100152-103	CAP,CHIP, 10NF, 50V, 10PCT	95275	VJ0805Y103KXAAT
C59	110126	CAP, TANTA, 6.8UF, 35V, 20 PERCENT	05397	T355F685M035A5
C60	110126	CAP, TANTA, 6.8UF, 35V, 20 PERCENT	05397	T355F685M035A5
C61	100152-103	CAP,CHIP, 10NF, 50V, 10PCT	95275	VJ0805Y103KXAAT
C62	100152-103	CAP,CHIP, 10NF, 50V, 10PCT	95275	VJ0805Y103KXAAT
C63	110126	CAP, TANTA, 6.8UF, 35V, 20 PERCENT	05397	T355F685M035A5
C64	110126	CAP, TANTA, 6.8UF, 35V, 20 PERCENT	05397	T355F685M035A5
C65	100152-103	CAP,CHIP, 10NF, 50V, 10PCT	95275	VJ0805Y103KXAAT
C66	100152-103	CAP,CHIP, 10NF, 50V, 10PCT	95275	VJ0805Y103KXAAT
C71-C74	100152-103	CAP,CHIP, 10NF, 50V, 10PCT	95275	VJ0805Y103KXAAT
C75	R-21-1802	CAP, CHIP, 100 NF	95275	VJ1206Y104MF
C78	R-21-1802	CAP, CHIP, 100 NF	95275	VJ1206Y104MF
C83	R-21-1802	CAP, CHIP, 100 NF	95275	VJ1206Y104MF
C86	R-21-1802	CAP, CHIP, 100 NF	95275	VJ1206Y104MF
C88	110162	CAP, TANTA, .33 UF, 35V, 10 PERCENT	05397	T368A334J035AS
C95-C98	100154-121	CAP, CHIP, 120PF, 50V, 5PCT	95275	VJ0805A121JXAAT
C99	100152-103	CAP,CHIP, 10NF, 50V, 10PCT	95275	VJ0805Y103KXAAT
C100	100152-103	CAP,CHIP, 10NF, 50V, 10PCT	95275	VJ0805Y103KXAAT
C101	130190-001	CAP, MICA, 100PF, 500V, 2PCT	09023	CM05FD101G03
C103	130190-012	CAP, MICA, 2000PF, 500V, 2PCT	09023	CM07FD202G03
C104	130190-008	CAP, MICA, 3300PF, 500V, 2PCT	09023	CM06FD332G03
C105	130190-011	CAP, MICA, 15NF, 500V, 2PCT	09023	CM07FD153G03
C106	130190-002	CAP, MICA, 150PF, 500V, 2PCT	09023	CM05FD151G03
C107	130190-004	CAP, MICA, 300PF, 500V, 2PCT	09023	CM05FD301G03
C108	130190-003	CAP, MICA, 200PF, 500V, 2PCT	09023	CM05FD201G03
C109	130190-005	CAP, MICA, 1000PF, 500V, 2PCT	09023	CM06FD102G03
C110	130190-012	CAP, MICA, 2000PF, 500V, 2PCT	09023	CM07FD202G03
C111	130190-012	CAP, MICA, 2000PF, 500V, 2PCT	09023	CM07FD202G03
C112	130190-011	CAP, MICA, 15NF, 500V, 2PCT	09023	CM07FD153G03
C114	130190-009	CAP, MICA, 4700PF, 500V, 2PCT	09023	CM06FD472G03

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405062-003 - PCB ASSY., SIGNAL CONDITIONER MOD.

REF DESIG	RACAL INST P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
C116	130190-011	CAP, MICA, 15NF, 500V, 2PCT	09023	CM07FD153G03
C117	130190-001	CAP, MICA, 100PF, 500V, 2PCT	09023	CM05FD101G03
C119	130190-012	CAP, MICA, 2000PF, 500V, 2PCT	09023	CM07FD202G03
C120	130190-008	CAP, MICA, 3300PF, 500V, 2PCT	09023	CM06FD332G03
C121	130190-011	CAP, MICA, 15NF, 500V, 2PCT	09023	CM07FD153G03
C122	130190-002	CAP, MICA, 150PF, 500V, 2PCT	09023	CM05FD151G03
C123	130190-003	CAP, MICA, 200PF, 500V, 2PCT	09023	CM05FD201G03
C124	130190-004	CAP, MICA, 300PF, 500V, 2PCT	09023	CM05FD301G03
C125	130190-005	CAP, MICA, 1000PF, 500V, 2PCT	09023	CM06FD102G03
C126	130190-012	CAP, MICA, 2000PF, 500V, 2PCT	09023	CM07FD202G03
C127	130190-012	CAP, MICA, 2000PF, 500V, 2PCT	09023	CM07FD202G03
C128	130190-011	CAP, MICA, 15NF, 500V, 2PCT	09023	CM07FD153G03
C130	130190-009	CAP, MICA, 4700PF, 500V, 2PCT	09023	CM06FD472G03
C132	130190-011	CAP, MICA, 15NF, 500V, 2PCT	09023	CM07FD153G03
C133	100152-103	CAP,CHIP, 10NF, 50V, 10PCT	95275	VJ0805Y103KXAAT
C134	110162	CAP, TANTA, .33 UF, 35V, 10 PERCENT	05397	T368A334J035AS
C135	110244	CAP TANTA 1.0 MF, 16V, 10 PCT	MATSU	267M1602105K
C136	110162	CAP, TANTA, .33 UF, 35V, 10 PERCENT	05397	T368A334J035AS
C137	110244	CAP TANTA 1.0 MF, 16V, 10 PCT	MATSU	267M1602105K
C138	110162	CAP, TANTA, .33 UF, 35V, 10 PERCENT	05397	T368A334J035AS
C139	110244	CAP TANTA 1.0 MF, 16V, 10 PCT	MATSU	267M1602105K
C140	110162	CAP, TANTA, .33 UF, 35V, 10 PERCENT	05397	T368A334J035AS
C141	110244	CAP TANTA 1.0 MF, 16V, 10 PCT	MATSU	267M1602105K
C142-C145	110126	CAP, TANTA, 6.8UF, 35V, 20 PERCENT	05397	T355F685M035A5
C146-C150	R-21-1802	CAP, CHIP, 100 NF	95275	VJ1206Y104MF
C151-C153	100154-680	CAP, CHIP, 68PF, 50V, 5PCT	95275	VJ0805A680JXAAT
C154-C157	110126	CAP, TANTA, 6.8UF, 35V, 20 PERCENT	05397	T355F685M035A5
C160	130190-005	CAP, MICA, 1000PF, 500V, 2PCT	09023	CM06FD102G03
C162	130190-012	CAP, MICA, 2000PF, 500V, 2PCT	09023	CM07FD202G03
C163	130190-005	CAP, MICA, 1000PF, 500V, 2PCT	09023	CM06FD102G03
C164	130190-012	CAP, MICA, 2000PF, 500V, 2PCT	09023	CM07FD202G03
C166-C169	R-21-1802	CAP, CHIP, 100 NF	95275	VJ1206Y104MF
C170	120210	CAP, MYLAR, 1MF, 400V, 5PCT	27556	ZA2E105J
C171	120210	CAP, MYLAR, 1MF, 400V, 5PCT	27556	ZA2E105J
C201-C242	100152-103	CAP,CHIP, 10NF, 50V, 10PCT	95275	VJ0805Y103KXAAT
CR1	210120	DIODE, LIGHT EMITTING, RED	91802	5350T1LC
D1	230951	IC, 1.2V MICRO PWR V REF DIODE	27014	LM385BM-1.2
D2	210115	DIODE, HIGH SPEED SWITCHING	04713	MMBD914(TA)
D3-D6	210036	DIODE, HIGH COND, LO LEAKAGE	07263	FDH300
D7	210137	DIODE, ZENER, 3.3V, 5W, 5PCT	04713	1N5333B
D8	210137	DIODE, ZENER, 3.3V, 5W, 5PCT	04713	1N5333B
J200	601726	CONNECTOR, D-SUB, RECEPT., 25-PIN	00779	745783-4
J201	455520	COAX TERMINAL, PCB MOUNT	21793	455520
J202	455520	COAX TERMINAL, PCB MOUNT	21793	455520
JP1	601208-016	CONNECTOR, PCB, PLUG, 3-PIN	52072	CA-S03-23B-43
K1	310196	RELAY, 2FORM C	61529	DS2YE-S-DC24V
K2	310196	RELAY, 2FORM C	61529	DS2YE-S-DC24V
K8-K11	310196	RELAY, 2FORM C	61529	DS2YE-S-DC24V
L1	310193	CHOKE, SHIELDED, 5UH	91637	IH-5-5-10
L2	310193	CHOKE, SHIELDED, 5UH	91637	IH-5-5-10
L3	100164	CAP, FEED-THRU,800PF, 50V	00779	842448-2
L4	310193	CHOKE, SHIELDED, 5UH	91637	IH-5-5-10
L5	310193	CHOKE, SHIELDED, 5UH	91637	IH-5-5-10
L6	100164	CAP, FEED-THRU,800PF, 50V	00779	842448-2
L12	100164	CAP, FEED-THRU,800PF, 50V	00779	842448-2
L15	100164	CAP, FEED-THRU,800PF, 50V	00779	842448-2
L17	310239	CHOKE, 22UH, 10PCT	99800	1641-223
L19	310239	CHOKE, 22UH, 10PCT	99800	1641-223
L21	310239	CHOKE, 22UH, 10PCT	99800	1641-223

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405062-003 - PCB ASSY., SIGNAL CONDITIONER MOD.

REF DESIG	RACAL INST P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
L23	310239	CHOKE, 22UH, 10PCT	99800	1641-223
L24	310239	CHOKE, 22UH, 10PCT	99800	1641-223
L26	310239	CHOKE, 22UH, 10PCT	99800	1641-223
P1	601675-001	CONNECTOR, EUROCARD, 96 PIN MOD.	21793	601675-001
P2	601675-001	CONNECTOR, EUROCARD, 96 PIN MOD.	21793	601675-001
Q1	200330	TRANSISTOR, MOSFET, N CH	17856	2N7002
Q2	200330	TRANSISTOR, MOSFET, N CH	17856	2N7002
R1	050000-820	RES, CHIP, 82 OHM, .06W, 5PCT	91637	CRCW0805SERIES
R3	050000-101	RES, CHIP, 100OHM .06W, 5PCT	91637	CRCW0805SERIES
R4	050040	RES, CHIP, 6.04K, 1/8W, 1PCT	65940	MCR186.04KFW
R5	050047	RES, CHIP, 2.21K, .06W, 1PCT	56235	50705CPX2211F30
R7	050000-103	RES, CHIP, 10K, .06W, 5PCT	91637	CRCW08051002J
R8	050038	RES, CHIP, 825 OHM, 1/8W, 5PCT	65940	MCR18825J
R9	050000-103	RES, CHIP, 10K, .06W, 5PCT	91637	CRCW08051002J
R10	050000-103	RES, CHIP, 10K, .06W, 5PCT	91637	CRCW08051002J
R11	050000-102	RES, CHIP, 1K, .06W, 5PCT	91637	CRCW-0805SERIES
R12	050000-102	RES, CHIP, 1K, .06W, 5PCT	91637	CRCW-0805SERIES
R13	050000-471	RES, CHIP, 470 OHM, .06W, 5PCT	91637	CRCW08054700J
R14	040330	POT, CERAM METAL, 10K, SIDE ADJ	80294	3266X-1-103
R15	050000-271	RES, CHIP, 270 OHM, .06W, 5PCT	91637	0805SERIES
R17	R-20-5796	RES, CHIP, 2.2K, 1/8W, 5 PCT, 200V	65940	MCR18-2.2K-5 PCT
R18	050000-102	RES, CHIP, 1K, .06W, 5PCT	91637	CRCW-0805SERIES
R20	R-20-5785	RES, CHIP, 220 OHM,1/8W,5 PCT,200V	65940	MCR18-220 OHM-5 PCT
R21	050000-433	RES, CHIP, 43K, .06W, 5PCT	91637	CRCW0805 SERIES
R23	010384	RES, METAL FILM, 402K, 1/4W, 1PCT	81349	RN60D4023F
R24	040330	POT, CERAM METAL, 10K, SIDE ADJ	80294	3266X-1-103
R25	040330	POT, CERAM METAL, 10K, SIDE ADJ	80294	3266X-1-103
R26	050000-274	RES, CHIP, 270K, .06W, 5PCT	91637	0805SERIES
R27	000335	RES, FIXED COMP	81349	RC07GF335J
R28	010542	RES, METAL FILM, 100K, 1/8W, 1PCT	81349	FRN55E1003F
R30	040330	POT, CERAM METAL, 10K, SIDE ADJ	80294	3266X-1-103
R31	050000-271	RES, CHIP, 270 OHM, .06W, 5PCT	91637	0805SERIES
R33	R-20-5796	RES, CHIP, 2.2K, 1/8W, 5 PCT, 200V	65940	MCR18-2.2K-5 PCT
R34	050000-102	RES, CHIP, 1K, .06W, 5PCT	91637	CRCW-0805SERIES
R36	R-20-5785	RES, CHIP, 220 OHM,1/8W,5 PCT,200V	65940	MCR18-220 OHM-5 PCT
R37	050000-433	RES, CHIP, 43K, .06W, 5PCT	91637	CRCW0805 SERIES
R39	010384	RES, METAL FILM, 402K, 1/4W, 1PCT	81349	RN60D4023F
R40	040330	POT, CERAM METAL, 10K, SIDE ADJ	80294	3266X-1-103
R41	040330	POT, CERAM METAL, 10K, SIDE ADJ	80294	3266X-1-103
R42	050000-274	RES, CHIP, 270K, .06W, 5PCT	91637	0805SERIES
R43	000335	RES, FIXED COMP	81349	RC07GF335J
R44	010542	RES, METAL FILM, 100K, 1/8W, 1PCT	81349	FRN55E1003F
R62	012177	RES, CHIP, 619 OHM, .06W, 1PCT	91637	CRCW0805-6190F
R63	050017	RES, CHIP, 3.01K, .06W, 1PCT	91637	CRCW08053011F
R64	012176	RES, METAL FILM, 90.9 OHM, 1/2W, 1PCT	91637	RN60D90R9F
R69	012177	RES, CHIP, 619 OHM, .06W, 1PCT	91637	CRCW0805-6190F
R70	050017	RES, CHIP, 3.01K, .06W, 1PCT	91637	CRCW08053011F
R71	012176	RES, METAL FILM, 90.9 OHM, 1/2W, 1PCT	91637	RN60D90R9F
R78	012177	RES, CHIP, 619 OHM, .06W, 1PCT	91637	CRCW0805-6190F
R79	050017	RES, CHIP, 3.01K, .06W, 1PCT	91637	CRCW08053011F
R80	012176	RES, METAL FILM, 90.9 OHM, 1/2W, 1PCT	91637	RN60D90R9F
R89-R92	050031-112	RES, CHIP, 1.10K, .06W, 2PCT	91637	CRCW08051101G
R93	010015	RES, METAL FILM, 63.4K, 1/4W, 1PCT	81349	RN60C6342F
R94	010218	RES, METAL FILM, 6.34K, 1/4W, 1PCT	81349	RN60D6341F
R104	001766	RES, CARBON, 220K, 1/2W, 5PCT	81349	RC20GF224J
R105	001766	RES, CARBON, 220K, 1/2W, 5PCT	81349	RC20GF224J
R106	010015	RES, METAL FILM, 63.4K, 1/4W, 1PCT	81349	RN60C6342F
R107	010218	RES, METAL FILM, 6.34K, 1/4W, 1PCT	81349	RN60D6341F
R117	001766	RES, CARBON, 220K, 1/2W, 5PCT	81349	RC20GF224J

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REF DESIG	RACAL INST P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
R118	001766	RES, CARBON, 220K, 1/2W, 5PCT	81349	RC20GF224J
R119-R122	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5 PCT,200V	65940	MCR18-10 OHM-5 PCT
R123	R-20-5802	RES,CHIP,12K,1/8W,5 PCT	65940	MCR18-12K-5 PCT
R124	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5 PCT,200V	65940	MCR18-10 OHM-5 PCT
R131	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5 PCT,200V	65940	MCR18-10 OHM-5 PCT
R139	050000-103	RES, CHIP, 10K, .06W, 5PCT	91637	CRCW08051002J
R142	050000-103	RES, CHIP, 10K, .06W, 5PCT	91637	CRCW08051002J
R143	050000-103	RES, CHIP, 10K, .06W, 5PCT	91637	CRCW08051002J
R144	080161	RES NETWORK, 330 OHM, 16P8R	91637	50MC-16-03-331J
R145	080161	RES NETWORK, 330 OHM, 16P8R	91637	50MC-16-03-331J
R146	000202	RES, CARBON, 2K, 1/4W, 5 PERCENT	81349	RC07GF202J
R147	000202	RES, CARBON, 2K, 1/4W, 5 PERCENT	81349	RC07GF202J
R148	050000-682	RES, CHIP, 6.8K, .06W, 5PCT	91637	CRCW0805SERIES
R149	050000-272	RESISTOR, CHIP, 150K, .06W 5PCT	91637	CRCW0805SERIES
R150	050000-682	RES, CHIP, 6.8K, .06W, 5PCT	91637	CRCW0805SERIES
R151	050000-272	RESISTOR, CHIP, 150K, .06W 5PCT	91637	CRCW0805SERIES
R152	050000-682	RES, CHIP, 6.8K, .06W, 5PCT	91637	CRCW0805SERIES
R153	050000-272	RESISTOR, CHIP, 150K, .06W 5PCT	91637	CRCW0805SERIES
R154-R156	012176	RES, METAL FILM, 90.9 OHM, 1/2W, 1PCT	91637	RN60D90R9F
R157	050000-102	RES, CHIP, 1K, .06W, 5PCT	91637	CRCW-0805SERIES
SW1	601949	SWITCH, DIP 8 POSITION	95146	ADP-08
SW2	601950	SWITCH, DIP 6 POSITION	95146	ADP-06
U1	231396	IC, MIC, 68000, 16MHZ, PLCL	04713	MC68000FN12F
U2	231236	IC, DIGITAL BUFFER SCIC	04713	MC74HCT244DW
U3	231477-002	IC, PLA	21793	231477-002
U4	231254	IC, MEMORY CMOS	21793	231254
U5	231254	IC, MEMORY CMOS	21793	231254
U6	231553-002	IC MEMORY	21793	231553-002
U8	231093	IC, QUAD COMPARATOR	04713	LM339D
U9	231093	IC, QUAD COMPARATOR	04713	LM339D
U14-U16	231092	IC, TRI-STATE BUFFER	18324	74LS244D
U17	231129	IC, OCTAL BUS TRANSCEIVERS	18324	N74LS645-1D
U18	231129	IC, OCTAL BUS TRANSCEIVERS	18324	N74LS645-1D
U19	231092	IC, TRI-STATE BUFFER	18324	74LS244D
U20	231409	IC, DIGITAL, SMD	27014	DM74LS30M
U21	230986	IC,8-BIT COMPARATOR	07263	74F521SC
U22	231236	IC, DIGITAL BUFFER SCIC	04713	MC74HCT244DW
U23	230988	IC,OCTAL LATCH W/3-STATE OUTPUTS	07263	74ACT373SC
U24	231318	IC, DIGITAL SMD	01295	74HCT652DW
U25	231326	IC, DIGITAL, SMD	27014	74ACT109SC
U26	231466	IC, 8-BIT REGISTER W/CLR	27014	DM74LS273M
U27	231094	IC, DEMUX DECODER	18324	N74LS138D
U28	231092	IC, TRI-STATE BUFFER	18324	74LS244D
U29	230986	IC,8-BIT COMPARATOR	07263	74F521SC
U30	231122	IC, SOIC	01295	SN74LS641-1DW
U31	231126	IC, NAND GATE	18324	74S38D
U32	231092	IC, TRI-STATE BUFFER	18324	74LS244D
U33	231387	HEX INVERTER	27014	DM74LS14M
U34	231476-003	IC, MEMORY	21793	231476-003
U35	231476-004	IC, MEMORY	21793	231476-004
U36	231554-002	IC MEMORY	21793	231554-002
U37-U40	231318	IC, DIGITAL SMD	01295	74HCT652DW
U41	231477-001	IC, PLA	21793	231477-001
U42	231477-005	IC, PLA	21793	231477-005
U43	231477-004	IC, PLA	21793	231477-004
U44	250008	OCI, FAST TTL OPTICALLY COUPLED	50434	6N137-5082-4360
U45	231475	IC, MONOLITHIC 16-BIT D/A CONV	24355	DAC71-C0B-V
U46	231474	IC, VOLTAGE COMPARATOR	27014	LF311H
U47	250008	OCI, FAST TTL OPTICALLY COUPLED	50434	6N137-5082-4360

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REF DESIG	RACAL INST P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
U48	231475	IC, MONOLITHIC 16-BIT D/A CONV	24355	DAC71-C0B-V
U49	231474	IC, VOLTAGE COMPARATOR	27014	LF311H
U50	921281	MODULE, DC-DC CONVERTER	OAK51	515D24
U51	921281	MODULE, DC-DC CONVERTER	OAK51	515D24
U56	231471	IC, FAST + - 150MA PWR BUFFER	64155	LT1010CT-FLOW 30
U58	231471	IC, FAST + - 150MA PWR BUFFER	64155	LT1010CT-FLOW 30
U60	231471	IC, FAST + - 150MA PWR BUFFER	64155	LT1010CT-FLOW 30
U63	231477-007	IC, PLA	21793	231477-007
U64	231477-006	IC, PLA	21793	231477-006
U65	231122	IC, SOIC	01295	SN74LS641-1DW
U66-U68	231465	IC, 1 OF 8 DATA SEL/MUX	27014	74F151AS
U75	230483	IC, DRIVER	56289	UDN-2981A
U79	231481	IC, DIGITAL, SOIC	04713	MC74ACT273DW
U80	231481	IC, DIGITAL, SOIC	04713	MC74ACT273DW
U81	231095	IC, D-TYPE FLIP-FLOP	18324	74HCT273D
U84	231095	IC, D-TYPE FLIP-FLOP	18324	74HCT273D
U85	231095	IC, D-TYPE FLIP-FLOP	18324	74HCT273D
U86	231236	IC, DIGITAL BUFFER SCIC	04713	MC74HCT244DW
U87	250017	OPTO-COUPLER, DUAL	50434	HCPL-2231
U88	250017	OPTO-COUPLER, DUAL	50434	HCPL-2231
U89	231462	IC, HEX/QUAD D F-F	27014	DM74LS175M
U90-U93	231131	IC, DIGITAL, SHIFT REGISTER	18324	PC74HCT164D
U94-U111	310238	RELAY, SOLID STATE, 400V	71707	6201A-1
U112	231093	IC, QUAD COMPARATOR	04713	LM339D
U113	230275	IC, LINEAR	04713	MC7805CT
U114	230275	IC, LINEAR	04713	MC7805CT
U115	231458	IC, 3-TERMINAL REGULATORS	27014	LM790SCT
U116	231458	IC, 3-TERMINAL REGULATORS	27014	LM790SCT
U119	230373-051	IC, VOLTAGE REGULATOR	21793	23073-051
U120	230609	IC, HEX INVERTER	01295	SN7406N
U121	231436	IC, HIGH SPEED CMOS	18324	74HCT74D
U122	231436	IC, HIGH SPEED CMOS	18324	74HCT74D
U124	231095	IC, D-TYPE FLIP-FLOP	18324	74HCT273D
U126	231236	IC, DIGITAL BUFFER SCIC	04713	MC74HCT244DW
Y1	921248	OSCILLATOR, 12MHZ, TTL	61441	S1100-12.00
Z1-Z3	080120	RES NETWORK, 10K	11236	767-161R10K
Z4	080119	RES NETWORK, 220K	91637	SOMC-1603-224K
1152	100164	CAP, FEED-THRU,800PF, 50V	00779	842448-2
{132}1	415062	PCB, SIGNAL CONDITIONER (UNLOADED)	21793	415062
{136}1	456109	PANEL, FRONT, 6056	21793	456109
{139}A/R	501376	TUBING, TEFLON, 20 GA, THIN WALL	29005	TW20GA
{140}A/R	500009	TUBING, SHRINK,. 12 ID, BLK	29005	RNF-100-1-1/8
{141}1	500254	CABLE, COAXIAL, 50 OHM	92194	9178B
{143}4	601106	HEATSINK, TO 220	13103	61078-14
{144}22	601197	POST, TEST, .025 SQ	00779	6-87022-6
{148}2	601944	CONNECTOR, RECEPTACLE, PANEL MOUNT SMC	98291	50-010-3196
{152}3	602068-028	CONNECTOR, SOCKET, 28 PIN	55322	PLCC-28-T-A
{153}2	602068-032	CONNECTOR, SOCKET, 32 PIN	55322	PLCC-32-T-A
{154}2	602068-044	IC SOCKET, 44-PIN, SMD	55322	PLCC-44-T-A
{155}4	602068-068	CONNECTOR RECEPTACLE 68 PIN	55322	PLCC-68-T-A
{158}4	610851	INSULATOR, TO-220	18565	60-11-5791-1674
{159}1	611092	HARDWARE KIT, D-SUB, 4-40 THD, FEMALE	00779	205817-3
{160}4	611257	WASHER, SHOULDER #10	86928	5607-98
{161}3	611258-001	STANDOFF, SWAGE 4-40 X .170	06540	8091-11B-B-440-28
{162}1	611264	HANDLE, EXTRACTOR, BOTTOM	62559	20817-327
{163}1	611265	HANDLE, EXTRACTOR, TOP	62559	20817-328
{164}.5	611266	MOUNTING HARDWARE, HANDLE	62559	21100-745
{167}8	616316	SCREW, PPH, M3X8	1CJ86	7985-A-M2.5X14MM
{168}2	616405	SCREW, PFH, M2.5-.45 X 12	-	-

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{169}8	617042	NUT, HEX, M3	1CJ86	DIN934-M3
{170}A/R	920450	ADHESIVE/SEALANT	01139	RTV-108
{171}1	921148	LABEL SET, VXI-VME	21793	921148
{173}A/R	921279	LOCQUIC, PRIMER	05972	74756
{174}A/R	921280	LOCTITE, HIGH STRENGTH	05972	27121
{185}8	R-23-9148	INSULATING BUSH, M3	K1935	J22-5006
{186}8	R-24-2801	WASHER, CRINKLE, M3	21793	R-24-2801

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