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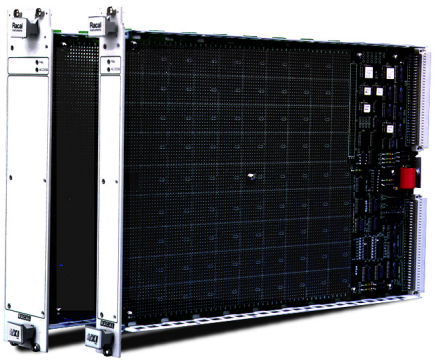
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Racal Instruments™ 7064M

Message-Based Prototyping Modules

The Racal Instruments™ 7064M Series of C-sized, message-based prototyping modules simplifies your task of developing VXIbus-based products.

The 7064M combines 96 digital I/O lines, an IEEE-488.2 compliant message-based interface, shared memory, and master/slave expansion capability to simplify the task of interfacing to the VXIbus. These features give you the opportunity to concentrate on product and/or circuit design.

Key Features

- **Message-based interface supports IEEE-488.2 Instrument protocol**
- **Multiple slot widths with local bus support**
- **96 buffered digital I/O control lines**
- **On-board 68000 CPU bus directly accessible to you**
- **VXI*plug&play* install disk included (based on the Microsoft Windows® operating system)**
- **85 in² of prototyping space**

Product Information

The "master" message-based 7064M includes a 68000-based daughter board that provides a simple interface between the VXIbus and the user's prototype circuitry.

If a system requires more than one 7064M, up to eleven more "slave" 7064M's can be added which maybe controlled by the "master" via the VXI local bus. Either type of 7064M includes 82 square inches of development area which can accommodate Dual-Inline Packages (DIPs), Pin Grid Arrays (PGAs), Plastic Leaded Chip Carriers (PLCCs) and Small Outline (SO) surface mount packages.

The Message-Based Daughter Board

The message-based interface (Opt 05, included with "master" modules) is a daughter board that plugs into the prototyping board. This interface allows control of user circuitry via the 96 digital I/O lines or via the microprocessor's local bus (available only on the master version). The upper half of the 68000's address space is available for the user to interface with memory-mapped devices.

The lower half is reserved for the 7064M's I/O ports, on-board memory, and VXIbus registers. All VXIbus registers are implemented including the VXIbus user-definable registers. The message-based interface supports the local bus on the VXIbus backplane, which can either be used for proprietary signals or for expansion by adding up to eleven "slave" 7064M's.

When to Use the Message-based 7064M

The message-based 7064M should be used in situations where a user-friendly interface and built-in I/O ports are required to speed prototype development. Software features in the 7064M such as channel scanning, the soft front panel, or native language drivers can also speed the prototyping process.

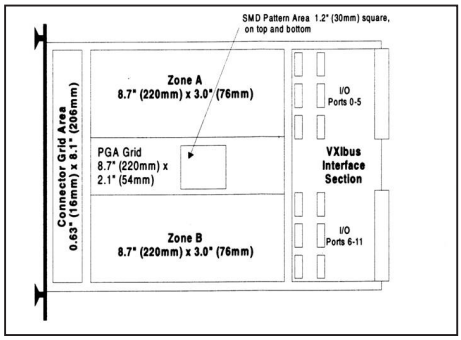
If maximum throughput across the VXIbus interface is critical, consider using the 7064R, Register-based prototyping module.

Development Area

Eighty-two square inches of prototyping space are available to the user along with all the appropriate VXIbus backplane signals. The user circuitry in the breadboard area is controlled through twelve 8-bit individually configurable ports.

The user circuitry can also be controlled through the message-based module's 68000 micro-processor directly. The upper half of the 68000 address space is available for this purpose.

As shown below, the 7064M's prototyping area is divided into five prototyping zones



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Product Information

continued

for maximum flexibility. The Connector Grid Area is a 0.1" (2.54mm) x 0.1" (2.54mm) grid designated for user I/O connectors. Holes may be cut in the 7064M's front panel to facilitate connection to the "outside world."

Zones A and B are identical areas for locating circuitry utilizing Dual-Inline Packages (DIPs). Both zones have six rows for DIP IC's or sockets, including locations for bypass capacitors (to +5 V and the "B" and "T" user-selectable power planes) for each chip.

The PGA Grid area contains a 0.1" (2.54 mm) x 0.1" (2.54 mm) grid with access to +5 V and ground along the edges. The area can be used to mount Pin Grid Array (PGA) style packages or discrete components.

The SMD Pattern Area is a general-purpose surface-mount area which allows component mounting on both the top and bottom sides of the prototyping card. Various combinations of PLCC packages from 20 to 68 pins and 20 pin SO packages can be accommodated.

All pins are brought out to pads located at the edges of the area with +5 V and ground available at the four corners.

All seven VXIbus supply lines are available to the user and are fused, reducing the risk of damage to the backplane.

The 7064M module also provides the EMI power filtering required by the VXIbus specifications, removing the need for the user to design this circuitry.

Digital Control

The 7064M message-based prototyping module, provides 96 buffered TTL control lines, programmable in either binary, octal, decimal or hex. These 96 I/O lines can also be accessed in bit, byte or word format.

Automatic Channel Scanning

The 7064M includes a Scanlist feature which allows the user to set up an on-board memory buffer to write to or read from the 7064M's 96 TTL I/O lines. I/O ports can be updated and read automatically at programmable rates up to 100 kHz using the Scanlist Internal Delay Timer feature. This feature effectively turns the 7064M into a 100 kHz digital pattern generator. As an alternative, 7064M Scanlists can be advanced using a trigger. Breakpoints can be added to Scanlists to facilitate hardware trouble-shooting. Scanlist input masks can be specified to filter out unwanted data bits.

Specifications

Note: The EADS North America Test and Services policy is one of continuous development and improvement. Consequently, the equipment may vary in detail from the description and specifications in this publication.

CPU Configuration

Type

- 16 MHz MC68000

Memory

RAM	ROM	Non-vol	Shared RAM
64 k	128 k	16 k	64 k

Digital I/O Ports

- 12 Eight-bit ports

Digital I/O Modes

- Clocked Input: Input data latched with external clock
- Buffered Input: Input data sampled during VXIbus read
- Latched Output: Output data is latched (with readback capability)
- Scanlist Input/Output: To/From a User-Defined Buffer
- Scanlist Advance Source: Internal Delay or Trigger
- Scanlist Internal Delay Range: to 100 kHz
- Scanlist Internal Delay Resolution 1 µs

Software Features

- Bit and Byte Access, Scanlists, Breakpoints, Internal Scan Delay, Trigger I/O Support (TTLTRG0-7), IEEE-488.2 Command Set

Prototyping Features

Buffered I/O

- 96 Channels, TTL levels

I/O Drive Current

- Sink: 64 mA @ 0.55 V max
- Source: 15 mA @ 2.4 V min

User Current (fused)

	I_{user} (A)
+24 V	1.0
+12 V	1.0
+5 V	7.0
–2 V	2.0
-5.2 V	7.0
–12 V	1.0
–24 V	1.0

I/O Port Reset State

- 0 or 1, jumper selectable

Breadboarding Space

- 82 sq in

Prototyping Area Clearances

Type	Ckt. Side	Comp. Side
1-slot	0.13" (3.3 mm)	0.75" (19 mm)
2-slot	1.30" (33 mm)	0.75" (19 mm)
3-slot	1.30" (33 mm)	1.95" (49.5 mm)

VXI Local Bus Access

- A single "master" 7064M can control itself plus up to eleven "slave" 7064M's via the VXI local bus.

CPU Interface

- Shared Memory Access: D16, A24 (user supplied shared memory) CPU Local Bus: D16, A24 and control lines

Interface

(Message-based, VXIbus Rev. 1.4 compliant)

Software Compliance

- IEEE-488.2

VXI*plug&play*

- VXI*plug&play* support for frameworks based on Microsoft Win32® application programming interface

Shared Memory

- A 4, 64 k

Status Lights

- Red: Failed Self-Test
- Green: Access

Backplane Signal Support

- TTLTRG0-7, LBUS, ACFAIL, SERCLK, SERDAT, CLK10, SUMBUS, BERR, +5VSTDBY, SYSRESET, SYSCLK (buffered)

Trigger Support

- TTLTRG lines

Peak Current & Power Consumption

(excluding circuitry)

- Total Power: 6.25 W

	+5
I_{PM} (A)	0.25
I_{DM} (mA)	10.0

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Specifications
continued

Environmental

Temperature
- Operating: 0º C to +55º C
- Storage: -40º C to +71º C

Humidity (non-condensing)
- 11º C to 30º C: 95% ±5%
- 31º C to 40º C: 75% ±5%
- 41º C to 55º C: 45% ±5%

Altitude
- Operating: 10,000 ft
- Storage: 15,000 ft

Vibration (non-operating)
- 0.013 in: double amplitude, 5 to 55 Hz

EMC (Council Directive 89/336/EEC)
- EN55011, Group 1, Class A
- EN50082-1, IEC 801-2,3,4

Safety (Low Voltage Directive 73/23/EEC)
- EN6010-1, IEC1010-1

Mechanical

Weight
- 7064M-100: 1 kg (2.2 lbs)
- 7064M-200: 1.13 kg (2.5 lbs)
- 7064M-Opt 95: 0.3 kg (0.65 lbs)

Cooling (10º C Rise)
- 0.5 l/s @ 0.04 mm H_2O

CE The CE Mark indicates that the product has completed and passed rigorous testing in the area of RF Emissions and Immunity to Electromagnetic Disturbances, and complies with European electrical safety standards.

Ordering Information

407620-100 : Racal Instruments™ 7064M
Single Slot, Message-Based Prototyping Module (Master)

407620-200 : Racal Instruments™ 7064M-200
Double Slot Message-Based Prototyping Module (Master)

407620-Opt 95 : Racal Instruments™ 7064M-Opt 95
Source Code for Message-Based Interface w/Manual

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