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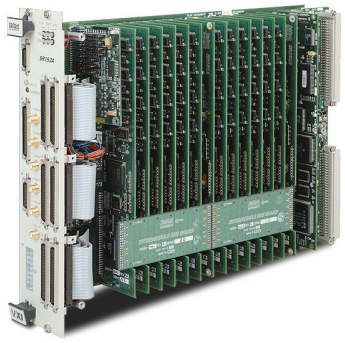
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Talon Instruments™ SR192A

OBSOLETE

50 MHz Digital Module

The Talon Instruments™ SR192A Digital Module provides up to 192 high-performance digital I/O channels in a space-saving double-wide VXI module. The SR192A operates at data rates up to 50 MHz with 5 ns edge placement and channel-to-channel skew.

Key Features

- **50 MHz digital stimulus and response with 5 ns edge placement resolution**
- **Supports Digital Test for Parallel and Serial Digital applications**
- **Data Import tools available for importing LSRTAP files**
- **Includes a Graphical User Interface to speed test development**
- **Scalable design supports digital test systems from 8 to 192 channels**
- **High-speed data sequencer provides control of stimulus/response patterns**

Product Information

Bus-Emulation Meets Stimulus/Response

For years, the test engineer faced less than desirable alternatives when selecting a digital resource. Early digital products were basic stimulus/response architectures, were expensive, consumed abundant real-estate, and were power-hungry. They also required extensive programming to emulate a relatively simple digital interface.

In the mid ’80s, Talon Instruments (now Astronics Test Systems) developed the first digital bus emulator product with the introduction of the Model 6000 Digital Test System.

In the early ‘90s, we introduced bus emulation in a VXI format with the BE64. For many applications, these bus emulation products significantly reduced cost, real-estate, power, and programming requirements. However, the BE64 posed another question for the test engineer: Does the test system require bus emulation or a traditional stimulus/response digital resource?

The Talon Instruments™ SR192A solves this dilemma by integrating both bus-emulation and stimulus/response architectures into a single resource for the VXIbus.

Versatile Architecture

When in bus-emulation mode, channels are grouped in 8-Pin groups. For example, fields are 8, 16, 24, 32, 40, etc. bits long. When in stimulus/response mode, each channel can be either input or output on a per-pin basis.

Density and Modularity

Because space in a VXI mainframe is at a premium, the SR192A was designed to pack the most dynamic digital capability into the smallest possible space. As many as 192 I/O channels, plus 20 timing and control channels, are housed in a dual-slot VXI module.

Additionally, to meet specific system requirements, the SR192A can be configured with I/O modules that can be chosen to meet specific system needs.

An SR192A system can grow to meet changing requirements by adding more and different types of I/O channels. Multiple SR192As can be synchronized, yielding a system with up to 1152 I/O channels.

Programmability

The SR192A can be configured with a variety of fixed and programmable I/O channels including TTL, RS-485, ECL, LVDS, and variable voltage.

The optional WCEM for PAWS® Run Time Software (RTS) provides an interface to the SR192A from the IEEE-standard ATLAS test language and eases integration into legacy systems.

This interface, which utilizes the PAWS® RTS, one of the most popular independent implementations of the ATLAS language, provides the capability for the SR192A to support both legacy and modern system implementations that take advantage of the higher-order, signal-oriented features of IEEE ATLAS.

There’s no need to know the nuances of the SR192A, as the ATLAS language provides the higher-order interface to the hardware.

ASTRONICS TEST SYSTEMS

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Product Information

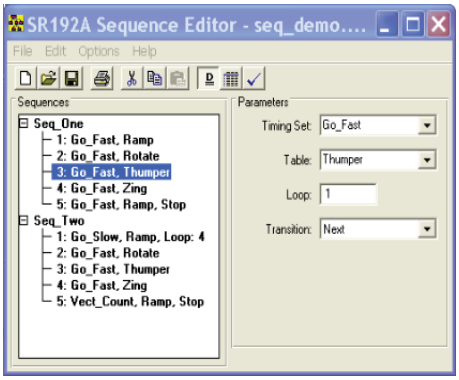
continued

Scalable Design

Built-in scalability and modular design enable configurations from 8 to 192 Single-Ended (SE) channels in 8-channel increments. Each SR192A can hold up to 12 modules of 16 SE channels each. Stimulus/response module types can be intermixed to match the signal requirements of the test system. Using master/slave mode, multiple modules can be linked for larger systems.

High-Speed Data Sequencer

The high-speed data sequencer provides intricate control over digital test patterns. Each SR192A contains up to two SR101A timing modules, each containing a data sequencer that can operate independently or synchronously for timing, memory, and control of up to six front-end modules. Sequencer logic supports full UUT handshaking and controls timing, format, pattern data, looping, and conditional testing. The sequencer includes definable standby and idle sequences.



Triggering and Synchronization

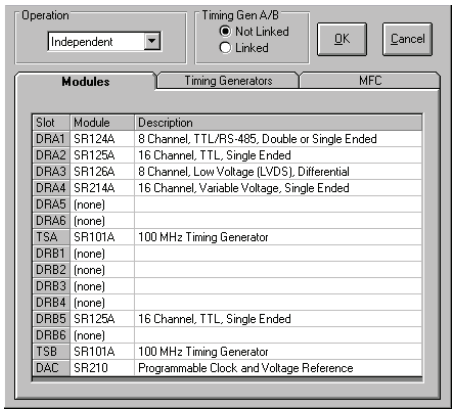
The SR192A features extensive control over digital testing to synchronize the SR192A with other test instruments and to control digital test sequencing. The SR192A accepts triggers from the VXI TTL Trigger Bus, VXI ECL Trigger Bus, Front Panel Auxiliary Inputs, or from any channel. Triggers can be used to synchronize the SR192A with other instruments and to act as a test input for test sequence control. Sync outputs can be offset to the start of a test sequence or step.

SR214A: Variable Voltage Stimulus/ Response

SR214A stimulus/response modules can be intermixed with LVDS, TTL, and RS-485 module types to provide a complete digital test system. Refer to Product Specifications and Ordering Information for details.

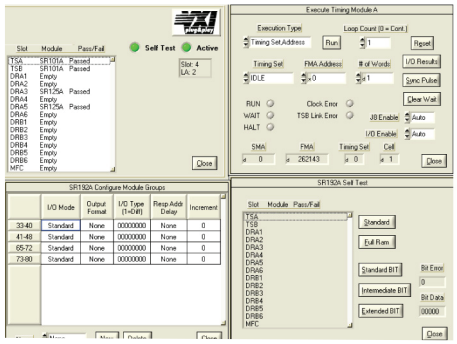
SR214A features:

- Voltage range of -5 V to +7 V with an output swing of up to 12 V
- Full drive current on all channels simultaneously
- Output slew rate greater than 1 V/ns
- 50 Ω output impedance



SR192A Soft Front Panel

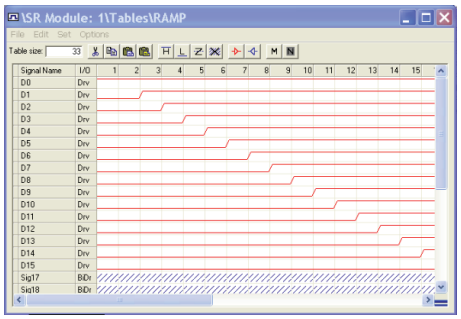
The soft front panel provides interactive control. The easy-to-use graphical interface enables setup and configuration, calibration, and sequencer control. Channels may be setup either individually or in user-defined groups.



SR192A Development System

The SR192A Development System is a tool for visually defining timing and table information. The SR192A Development System's advanced user interface design streamlines the process of creating digital tests. This 32-bit Microsoft Windows® application defines digital test data and timing without cumbersome and arcane programming. A fully functional evaluation copy is available for downloading.

Digital designs are increasing in complexity while time-to-market is decreasing. A test developer can no longer afford to spend



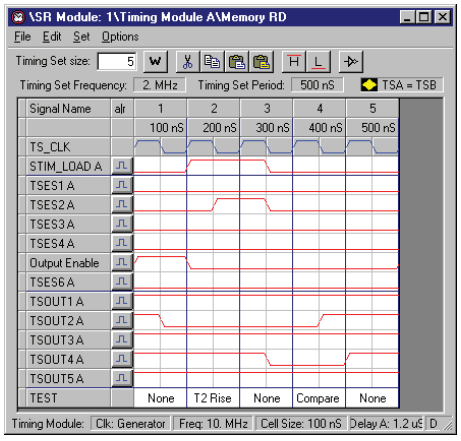
time learning the idiosyncrasies of his test equipment.

The SR192A Development System removes the burden of low-level details while still providing access to the full capability of the instrument. This is achieved with a cleanly structured point-and-click interface that minimizes effort and maximizes user feedback. The intuitive operations are aided by drag-and-drop, toolbars, pop-up menus, tooltips, flexible editing, and helpful wizards for more complex entry.

Digital data patterns are defined visually via a logic analyzer view. Within this view, digital data is set, moved, copied, labeled and highlighted. Carefully selected colors and graphics denote level, direction, and mask states. Finally, a test developer can edit all the attributes of a digital signal on one waveform display.

Timing cycles are defined through a simulated logic analyzer. This allows the important relationships between timing signals to be readily apparent. The length of a timing cycle can now be specified by period or frequency.

The SR192A Development System has external utilities and drivers for interfacing with an SR192A, including both an import utility for existing data sets and an automatic hardware configuration extractor.



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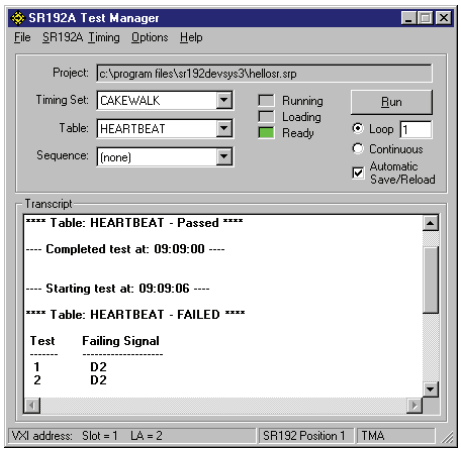
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Product Information
continued

A stand-alone ActiveX driver (DLL) is provided to load and execute an SR192A project from a variety of programming languages and test environments.

SR192A Test Manager

The SR192A Test Manager allows interactive execution of stored SR192A projects.



LASAR Translation Tools

Optional LASAR Translation Tools allow the import of these files into an SR192A project.

Specifications

Note: The Astronics Test Systems policy is one of continuous development and improvement. Consequently, the equipment may vary in detail from the description and specifications in this publication.

Timing Characteristics (Per SR101A)

SR101A per System
- 1 or 2

Timing Sets
- SR101A per system: 1 or 2
- Range: 1 to 16 per SR101A
- Cells per Timing Set: 2 to 256
- User Signals: TSOUT (6)
- Control Signals: Assert/Return, Output Enable/Input Strobe (6), Pattern Increment

Test Input Wait Conditions
- Inputs: TEST (2)
- Conditions: TESTn Low/High, Rising/Falling Edge, Delay A/B, Error, Compare, None

Wait Timeout
- 1 to 256 (selectable per Seq. Step)

Pause/Pattern Clutch
- Phases and Windows are frozen when asserted.

Halt/System Clutch
- All Phases will complete their action for the current Pattern.

Word Generation

Sequence
- Dynamic, Static

Sequence Steps
- Force: lo, hi, tri-state
- Format: NR, RT, R0, R1, RC, Complement Surround. Output the Phase or its complement (used to output Waveforms on channels).

Sequence Step Conditionals
- Mask
- Opening edge of window
- Closing edge of window
- Window (input data must match “expect” for the entire duration of the window).

Timing/Sequence Clock
- Size: 256 k words
- Expect: Good 1, Good 0, OK , between or mask
- Keep last
- Toggle last
- Accumulate a CRC16 (based on a Good 1 only)

SR124A/SR125A

Digital I/O Type
- SR124A: Single-ended TTL
- SR127A: Differential RS-422, RS-485

Number of Channels
- SR124A: 8
- SR125A: 16

Differential Driver/Receivers
- V_{OH} (Unloaded): 5V max
- V_{OH} (Loaded RS-485): 1.5 V min
- V_{OH} (Loaded RS-422): 2 V min
- Receiver Threshold: ±0.2 V max
- Receiver Hysteresis: 60 mV typ
- Receiver common mode range: -7 V to +12 V
- Input/Output Impedance: 100 Ω

Single Ended TTL Driver/Receivers
- V_{OH}: 2.4 V min
- High-Level Source Current: 50 mA
- VOL: 0.4 V min
- Low Level Sink Current: 50 mA
- Output Impedance: 55 Ω typ
- Short Circuit Protected: Yes
- High Input Threshold: 2.0 V
- Low Input Threshold: 0.8 V
- Input Impedance: >10 kΩ

Memories
- Stimulus: Output, Tristate
- Response: Expect, Mask, Record

Data Format
- Hold, RTZ, RTO, RTC, RTT

Increment Channel Mode
- 1 to 65, 536

Data Shift Channel Modes
- Serial Mode: Shift by one
- Multiplexed Mode: Shift by eight

Memory Depth per Channel
- Standard/Increment Modes: 256 k
- Multiplexed Mode: 512 k
- Serial Mode: 4 M

Stimulus/Response Data Rate (max)
- 50 MHz

Output Enable Source
- Internal: 8
- External: 2

Output Enable/Response Strobe Resolution
- ½ TS_CLK

Output Enable/Response Strobe Placement
- Range: 0 to 20 ns
- Resolution: 1 ns

Response Strobe Source
- Internal: 6
- External: 2

SR126A/SR127A

Digital I/O Type
- SR126A: Differential LVDS
- SR127A: Differential ECL

Number of Channels
- 8

Output Voltage Swing (SR126A)
- 100 Ω Terminator: 650 mV
- 50 Ω Terminator: 350 mV

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Specifications
continued

Output Voltage Swing (SR127A)
- V_{OH}/V_{IH}: -1.1 V min/-1.13 V max
- V_{OL}/V_{IL}: -2.0 V max/-1.48 V max
- High Level Source Current: 80 mA max
- Tri-stated V_O: -2.0 V typ
- Tri-stated V_I (for a true): <-1.5 V typ

Input/Output Termination
- SR126A: 100 Ω
- SR127A: 50 Ω to -2 V

Memories
- Stimulus: Output, Tristate
- Response: Expect, Mask, Record

Data Format
- Hold, RTZ, RTO, RTC, RTT

Increment Channel Mode
- 1 to 65,536

Data Shift Channel Modes
- Serial Mode: Shift by one
- Multiplexed Mode: Shift by eight

Memory Depth per Channel
- Standard/Increment Modes: 256 k
- Multiplexed Mode: 512 k
- Serial Mode: 4 M

Stimulus/Response Data Rate (max)
- 50 MHz

Output Enable Source
- Internal: 8
- External: 2

Output Enable/Response Strobe Resolution
- ½ TS_CLK

Output Enable/Response Strobe Placement
- Range: 0 to 20 ns
- Resolution: 1 ns

Response Strobe Source
- Internal: 6
- External: 2

SR214A

Signal Type
- Variable Voltage: -5 V to +7 V

Operating Modes
- Parallel, Serial, Increment, Multiplex

Number of Channels
- 16 (Single-ended)

Memories
- Stimulus: Output, Tristate
- Response: Expect, Mask, Record

Data Format
- Hold, RTZ, RTO, RTC, RTT

Increment Channel Mode
- 1 to 65,536

Data Shift Channel Modes
- Shift by one: Serial
- Shift by eight: Multiplex

Memory Depth per Channel
- Standard/Increment Modes: 256 k
- Multiplexed Mode: 512 k
- Serial Mode: 4 M

Stimulus/Response Data Rate (max)
- 50 MHz

Output Enable Source
- Internal: 8
- External: 2

Internal Output Enable Resolution
- ½ TS_CLK

Output Enable Placement
- Range: 0 to 20 ns
- Resolution: 1 ns

Response Strobe Source
- Internal: 6
- External: 2

Internal Response Strobe Resolution
- ½ TS_CLK

Response Strobe Placement
- Range: 0 to 20 ns
- Resolution: 1 ns

Input/Output References

Reference Groups
- V_{OH}: A or B
- V_{OL}: A or B
- V_{IH}: A or B
- V_{IL}: A or B

Output High Range (V_{OH})
- V_{OL} to +7 V

Output Low Range (V_{OL})
- -5 V to V_{OH}

Input High Range (V_{IH})
- V_{IL} to +7 V

Input Low Range (V_{IL})
- -5 V to V_{IH}

Reference Resolution
- 5 mV

Reference Accuracy
- ±20 mV

Channel Voltage Measurement
- Resolution: 4 mV
- Accuracy: ±50 mV

Drivers/Receivers
- V_{OH}/V_{IH}: -5 V to +7 V
- V_{OL}/V_{IL}: -5 V to +7 V
- Source/Sink Current: 25 mA
- Output Impedance: 50 Ω typ
- Output Slew Rate: >1 V/ns
- Output Protection: 0 V, short circuit
- Input Impedance: >500 kΩ

Front Panel I/O

System Indicators
- Fail/ID:
  Off = normal operation
  Green = VXI modid line asserted
  Flashing Red = command/module error
  Solid Red = CPU power-up self-test failure
  Amber = Both FAIL and MODID are asserted
- Overdrive: A variable voltage driver was over-driven and shut off

Timing Set Indicators (for each SR101A)
- Run:
  Off = cycle not active
  Green = cycle is active
  Red = Sequence cycles are executing
- Wait:
  Off = no timeouts
  Green = awaiting test cell completion
  Red = a test cell timed out
- Halt:
  Off = cycle not active
  Green = cycle is active
  Red = Sequence cycles are executing

Digital I/O
- J1-J6: 32 Channels per connector (68 pin, mates with 3M P50-68-MDS-TG)
- J7: Master/Slave daisy chain connector (20 pin, mates with 3M P50-20-MDS-TG)
- J8: Timing Signal connector (60-Pin, mates with 3M P50-60-MDS-TG)
- J9: Probe/Reference connector (28-Pin, mates with 3M P50-28-MDS-TG)
- J10: External Power connector (mates with Molex 39-01-2160)

User Signals (SMA)
- Clock Out (2): One for each SR101A
- Clock Ref: Programmable reference input to the SR210 (when installed)
- Programmable Clock (2): Delayed programmable output clocks from SR210 (when installed)
- Variable Voltage Clock: Programmable clock from SR210 (when installed)

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Specifications
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Software

Native Language
- Registers with some SCPI

Driver Support
- VXI*plug&play* Driver, Microsoft Win32® programming software

Test Executive/GUI
- SR192A GUI for Microsoft Win32®

Environmental

Humidity (non-condensing)
- 0° C to +10° C: Not controlled
- +10° C to +30° C: 5 to 95 ±5% RH
- +30° C to +40° C: 5 to 75 ±5% RH
- +40° C to +50° C: 5 to 55 ±5% RH

Temperature
- Operating: 0° C to 45° C
- Storage: -40° C to 70° C

Altitude
- 10,000 ft

EMC (Council Directive 89/336/EEC)
- Emission: EN61326-1: 2006, Class A
- Immunity: EN61326-1: 2006, Table 1

Safety (Low Voltage Directive 73/23/EEC)
- BS EN 61010-1: 2001

Mechanical

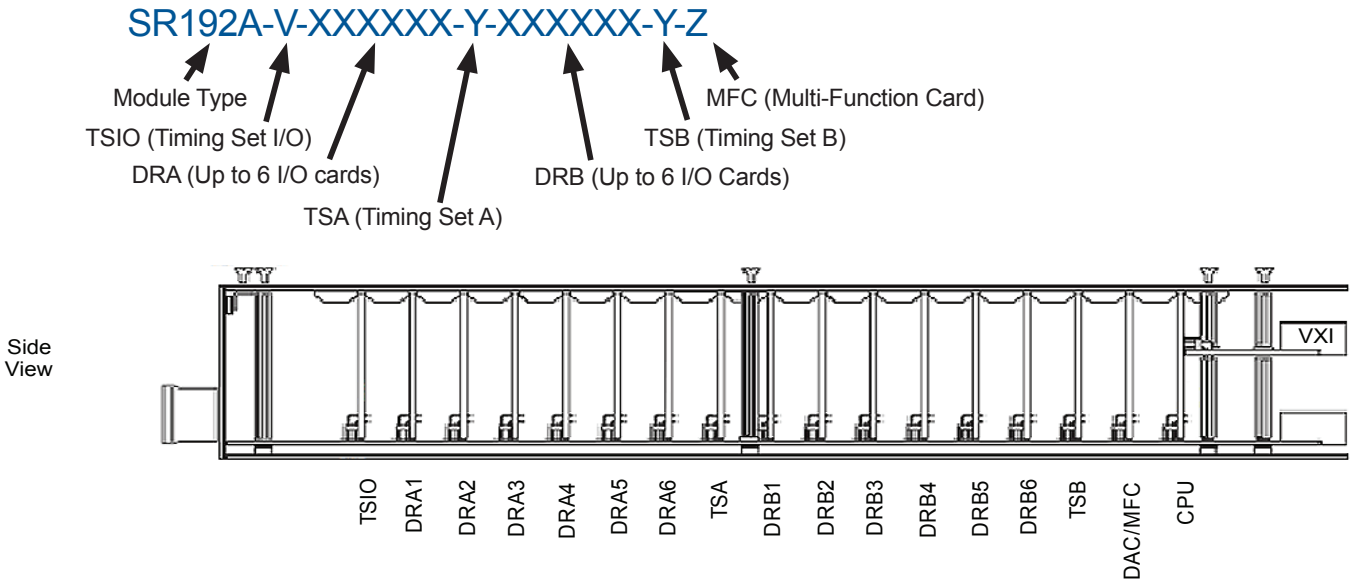
Dimensions
- Dual-slot, C-size VXI module 10.2” H x 13.8” W x 2.4” D (260 mm x 350 mm x 60 mm)

Weight
- 4 lb 4 oz

Ordering Information

SR192A-V-XXXXXX-Y-XXXXXX-Y-Z : Talon Instruments™ SR192A (Obsolete)

50 MHz Digital Module



Construct the SR192A model/part number by substituting the position code from the table below for the appropriate letter position in the appropriate section of the part number below.

Position Code (-V), (-X), (-Y), (-Z)	Position Code Description	Spares Part #
0	Empty Position	n/a
TSIO (Timing Set I/O) — Position “V”		
1	TSIOA (TTL/Differential I/O)	n/a
DRA and DRB I/O Cards — Position “X”		
A	SR107 (16 TTL I/O, static)	10780
B	SR124A (8 TTL or RS485-RS422 Differential I/O, 50 MHz), source termination	20570-004
C	SR125A (16 TTL I/O, 50 MHz), source termination	20570-005
D	SR214A (16 +7 to -5 VDC I/O, 50 MHz)	20700
E	SR126A (8 LVDS I/O, 50 MHz), source termination	20570-006
F	SR127A (8 ECL I/O, 50 MHz)	20710
G	SR124A (8 TTL or RS485-RS422 Differential I/O, 50 MHz), no termination	20570-001

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Ordering Information
continued

Position Code (-V), (-X), (-Y), (-Z)	Position Code Description	Spares Part #
H	SR125A (16 TTL I/O, 50 MHz), no termination	20570-002
I	SR126A (8 LVDS I/O, 50 MHz), no termination	20570-003
TSA and TSB — Position "Y"		
1	SR101A (4 k sequence memory); Timing Set Module, 4096 sequence memory, conditional jumping, sub-routing and looping. includes programmable clock generator (up to 50 MHz), 8 strobe/ enable signals, and half cycle resolution of 50 MHz.	20560-100
Multi-Function DAC — Position "Z"		
1	SR210 (2 programmable clocks and level clock + external references); Accessory Card; provides an internal 0 to 50 MHz programmable clock source, voltage reference control for the variable voltage clock outputs and control signals to/from the SR211 probe (Note: not needed unless the SR211 probe will be used.)	10560

Part Number Ordering Examples:

SR192A-1-DDDD00-1-000000-0-0	SR192A with a TSIO (1), one SR101A (1), and four SR214A (D)
SR192A-1-BBBB00-1-EEEE00-1-0	SR192A with a TSIO (1), two SR101A (1), four SR124A (B), and four SR126A (E)

Additional Ordering Information

SR192A-3E50-3E50 : Talon Instruments™ SR192A
Digital Channel Module (Variable Voltage, -5 V to +15 V, 64 channels)

SR192A-1400 : Talon Instruments™ SR192A-DR14
Digital Utility Module (Probe I/O, Clocks/Clutches, Meter, Counter, 32 Utility I/O channels)

405387 : Talon Instruments™ SR192A Base Digital Resource Module (no DR modules installed)

408002 : DR3e Driver/Receiver Type 3e–Variable Voltage, -5 V to +15 V, 32 Channels

408xxx : UM14 Utility Module Type 14–Probe I/O, Clocks/Clutches, Meter, Counter, 32 Utility I/O Channels

408177 : Racal Instruments™ 1263 High-power VXI Mainframe

Accessories

SR/300-00X : Flat Ribbon Cable X' long (68-Pin I/O Connector to two 34-Pin Headers) for J1-J6, where X = 1-6

SR/300-T-00X : Twisted Pair Ribbon Cable X' long (68-Pin I/O Connector to two 34-Pin Headers) for J1-J6, where X = 1-6

SR/301 : Connector Kit (includes Mating Connectors for J1-J6, J8, J9 and J10)

SR/302-00X : Flat Ribbon Cable X' long (60-Pin I/O Connector to two 34-Pin Headers) for J8, where X = 1-6

SR/302-T-00X : Twisted Pair Ribbon Cable X' long (60-Pin I/O Connector to two 34-Pin Headers) for J8, where X = 1-6

SR/303-00X : Flat Ribbon Cable X' long (28-Pin Voltage Reference Connector to two 34-Pin Headers) for J9, where X = 1-6

SR/304-00X : 16-gauge wire X' long (16-Pin Power Connector open ended) for J10, where X = 1-6

SR/305 : SR192A J1-J6 Connectors (quantity of 2)

SR/306/N : SR192A Master Slave Cable for Multiple SR192 Systems ("N" denotes number of systems connecting together; values for "N" can range from 2 to 12)

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