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Ball Corporation
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INSTALLATION AND OPERATION, PROGRAMMING, AND DIAGNOSTIC MANUAL

MODEL

VRFS

VXIbus Rubidium Frequency Standard
(For Use with VXIbus System Mainframes)

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Ball Corporation
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September 12, 1994

TECHNICAL NOTICE

EFRATOM VRFS - P/N 101790-008

The VRFS is a VXI module offered in several hardware configurations. The software of the module, with the exceptions noted below, functions identically for all hardware configurations.

The -008 configuration provides the following front panel outputs:

J1 = 10 MHz sine output

J2 = 10 MHz sine output

J3 = 10 MHz sine output

J4 = 10 MHz sine output

J5 = 10 MHz sine output

J6 = 10 MHz sine output

J7 = 10 MHz sine output

J8 = 10 MHz sine output

FRONT PANEL INDICATORS

Front panel LEDs include:

- POWER ON = green
- MODID = green
- RUBIDIUM LOCK = green
- ADJUST CRYSTAL = yellow
- OUTPUT FAULT = red

SOFTWARE MODIFICATIONS

All high level VXI commands function as described in this manual, with the exception of the :DELay<nn> and :DELay? commands, which are used only with 1 PPS inputs and outputs, a feature not incorporated in this configuration. Use of these commands will result in an error message being initiated.

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May 10, 1994

TECHNICAL NOTICE

EFRATOM VRFS - P/N 101790-007

The VRFS is a VXI module offered in several hardware configurations. The software of the module, with some exceptions noted below, functions identically for all hardware configurations.

The -007 configuration provides the following front panel outputs:

J1 = 10 MHz sine output

J2 = 10 MHz sine output

J3 = 10 MHz sine output

J4 = 10 MHz sine output

J5, which can be used as a 1 PPS synch input, has been deleted.

SOFTWARE MODIFICATIONS

All high level VXI commands function as described in this manual, with the exception of the :DELay<nn> and :DELay? commands, which are used only with 1 PPS inputs and outputs, a feature not incorporated in this configuration. Use of these commands will result in an error message being initiated.

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May 10, 1994

TECHNICAL NOTICE

EFRATOM VRFS - P/N 101790-006

The VRFS is a VXI module offered in several hardware configurations. The software of the module, with the exceptions noted below, functions identically for all hardware configurations.

The -006 configuration provides the following front panel outputs:

J1 = 10 MHz sine output

J2 = 10 MHz sine output

J3 = 10 MHz sine output

J4 = 10 MHz sine output

J5 = 10 MHz sine output

J6 = 10 MHz TTL output

J7 = 10 MHz TTL output

J8 = 10 MHz TTL output

J9 = 10 MHz Calibration Input

FRONT PANEL INDICATORS

Front panel LEDs include:

CAL OK = green	RUBIDIUM LOCK = green
POWER ON = green	ADJUST CRYSTAL = yellow
MODID = green	OUTPUT FAULT = red

SOFTWARE MODIFICATIONS

All high level VXI commands function as described in this manual, with the exception of the :DELay<nn> and :DELay? commands, which are used only with 1 PPS inputs and outputs, a feature not incorporated in this configuration. Use of these commands will result in an error message being initiated.

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Ball Efratom Division

TECHNICAL NOTICE

July 21, 1993

EFRATOM VRFS-MC - P/N 101790-005

The VRFS-MC is a VXI module currently offered in several configurations. The software of the module, with some exceptions noted below in this accompanying tech note, functions identically for all output configurations. The -005 configuration, as shipped with this manual, provides the following front panel outputs:

J1 through J4:	10 MHz TTL
J5 through J8:	10 MHz Sine

J9, which can be used as a 1 PPS synch input, has been deleted.

The isolation between outputs is ≤65 db

Refer to Appendix B for a final assembly drawing of the -005 configuration.

Software Modifications

All High level VXI commands function as described, with the exception of the `:DELay<nn>` and `:DELay?` commands, which are used only with 1 PPS inputs and outputs, a feature not included in this configuration. These commands will cause an error message to be generated if they are used.

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VRFS INSTALLATION, & OPERATION, PROGRAMMING, & DIAGNOSTIC MANUAL

TABLE OF CONTENTS

PARAGRAPH		PAGE
I	INSTALLATION & OPERATION	
1.1	Description	1
1.2	VRFS Module Specifications	1
1.3	Shipping & Receiving Info.	7
1.4	Installation	8
1.5	Operation	8
II	PROGRAMMING THE VRFS	
2.1	Description	1
2.2	Common VXIbus/ VRFS Command Definitions	1
2.3	VRFS Command Definitions	8
2.4	Programming of Interrupt Events	8
III	DIAGNOSTICS AND MAINTENANCE	
3.1	Description	1
3.2	Troubleshooting Guidelines	1
3.3	Module Disassembly	2
3.4	LED Indicators	2
3.5	Frequency Adjust	4

APPENDIX A:

Drawing, Schematic, and Parts List	A1
VRFS Final Assembly	A2
Parts List, VRFS Final Assembly	A3
———	A4
———	A5
———	A6
Schematic, VRFS Control Board	A7
———	A8
———	A9
———	A10
Board Assembly, VRFS	A11

APPENDIX B:

Special Configuration Drawings	B1
VRFS Final Assembly	B2, 3

LIST OF ILLUSTRATIONS

FIGURE		PAGE
1-1	High Level Command Tree for Model VRFS	5
1-2	VXIbus Rubidium Frequency Standard	6
1-3	Setting the Logical Address of VRFS	9
2-1	Structure of Event & Event Enable Registers	10
2-2	Voltage Event & Voltage Summary Bit Registers	13
2-3	VRFS Status Data Structure	14
2-4	FRS Event & Frequency Summary Bit Registers	15
3-1	Frequency Monitor Cutout & Module Address Set Cutout Locations	1

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SECTION I

INSTALLATION & OPERATION

1.1 Description

The Efratom model VRFS is an ultra-stable miniature atomic oscillator suitable for use as a VXIbus system clock housed in a module that is designed to be installed in a C-size mainframe configured in accordance with the VXIbus Specification. This module is a message-based device that offers timing accuracy of ± 1 ppb over its specified operating temperature at the VXIbus system clock frequency of 10 MHz and can provide up to eight outputs (1 PPS, 1 MHz sine, 10 MHz sine, and 10 MHz TTL) and, as an option, a 1 PPS input from an external source.

1.2 VRFS Module Specifications

1.2.1 Electrical

	Number	*Frequency*	*Waveform*
• Outputs*:	1 each	1 MHz	Sine
	1 each	1 PPS	Pulse
	4 each	10 MHz	Sine
	2 each	10 MHz	TTL

- 1 PPS Output Characteristics:

Rise Time:	25 nS
Fall Time:	100 nS
Pulse Width:	16µS ± 1 µS

- Output Level Load:

Sine Output:	1-2V P-P into 50 ohms
TTL Output:	TTL Compatible into 50 ohms
1 PPS Option:	10V ± 10% into 50 ohms
	5V option - CMOS Compatible

*Outputs must be programmed at the factory with various combinations of frequencies and waveshapes. The frequencies available are 1 Hz (1 PPS output), and 0.1, 1, 5, and 10 MHz (sine, TTL). The total number of outputs available is 8.

- Input (available as an option):

1 PPS:	V_{OH}	=	2.5V to 11V
	V_{OLmax}	=	0.8V
	Pulse Width	=	1 µS min

- Short Term Stability:

1.0 Second (Allan Variance)	=	1E-10
10 Second (Allan Variance)	=	3E-11
100 Second (Allan Variance)	=	1E-11

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- 1-Day Stability: 1E-10 @ 25°C ± 3°C
- Frequency Drift Per Month: 5E-11 (After 1 month of continuous operation)
- Frequency Accuracy at Shipment: ± 5E-11 (25°C)
- Frequency Trim Range: ± 1E-9 Minimum
- Setting Resolution: 1E-11
- Isolation Between Outputs: ≥ 80 dB
- Frequency Retrace: 5E-11
  (After 1 hour power ON @ 25°C
  and up to 25 hours power OFF)
- Phase Noise:
  1 Hz from Carrier: -70 dBc/ Hz
  100 Hz from Carrier: -110 dBc/ Hz
  1000 Hz from Carrier: -130 dBc/ Hz
- Harmonic/Non-Harmonic Distortion
  (Sine Wave Output): -34 dBc/-70 dBc
- Power Required:

Voltage	*No. of Pins Used*	*dc-Peak Current*	*Dynamic Current*
+5	P1-3, P2-4	2.5A	2.5A
+12	P1-1	0.5A	0.5A
+24	P2-1	2A @ 0°C (for ≤ 5 minutes)	0.5A

- Current at Turn On (0°C): 2.0A Peak +24 Vdc
- Input Voltage Sensitivity: < 5E-11 (for ± 10% Vdc Delta)
- Warm-up Times:
  Time to Lock (25°C): ≤ 4 minutes
  Minutes/Frequency (25°C): 6 minutes/1E-9
- Output Protection: Short Circuit Proof

1.2.2 VXI Bus Interfaces

- Manufacturer ID: 3938 (Using only the lower 12 bits)
  65,280 (If all 16 bits are used)
- Model Code: 3840
- Protocols: EG, I, I4 (EG = Event Generation,
  I = VXIbus Instrument,
  I4 = VXIbus 488.2 Instrument)

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- Device Type: Message Based Servant
- Address Space: A16 only
- 8 bit Logical Address Switch
- Static Configuration
- Programmable Interrupter
- Status/ID Register

1.2.3 Commands

- *High level Commands:*

`:STATus:VERBose?` - The response for this command has the following format:

Rb Lock/Unlock
Xtal Adj. Status
RF Output Status
Output #1 Pass/Fail
. . . . . .
Output #8 Pass/Fail

`:DELAy <nn>` This command sets the time delay between the input 1 PPS and the output 1 PPS. Delay is in seconds and the resolution is 100 nS.

`:DELAy?` The response for this command returns the Delay value in seconds (50 nS accuracy). At power ON the 1 PPS output delay is set to within 100 nS of the 1 PPS input.

Common and High Level Commands to write and read event enable and event registers:

Standard Events Register commands

`*ESR?`	Standard Event Status Enable query
`*ESE <n>`	Standard Event Status Enable <bit number>
`*ESE?`	Standard Event Status Enable query
`*CLS`	Clear Status Command (clears all registers)

Status Byte register commands

`*STB?`	Queries Status Byte

Service Request Enable Register

`*SRE <n>`	Service Request Enable command <bit number>
`*SRE?`	Service Request Enable query
`*WAI`	Wait-to-Continue Command

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Questionable Status register commands

`:STATus:QUEStionable:EVENt?`	Returns content of Voltage Summary Bit
`:STATus:QUEStionable?`	Sums contents of Voltage Summary Bit

Questionable Enable Events register commands

`:STATus:QUEStionable:ENABle <n>`	Returns content of bit <n>
`:STATus:QUEStionable:ENABle?`	Sums contents of register

Output Enable Events register commands

`:STATus:QUEStionable:VOLTage:ENABle?`	Enables contents of register
`:STATus:QUEStionable:VOLTage:ENABle <n>`	Enables only bit <n>

Output Events register commands

`:STATus:QUEStionable:VOLTage:EVENt?`	Returns "Hi" event bits
`:STATus:QUEStionable:VOLTage?`	Sums contents of register

FRS Events register commands

`:STATus:QUEStionable:FREQuency:EVENt?`	Returns "Hi" event bits
`:STATus:QUEStionable:FREQency?`	Sums contents of register

FRS Events Enable register commands

`:STATus:QUEStionable:FREQuency:ENABle?`	Enables contents of register
`:STATus:QUEStionable:FREQency:ENABle <n>`	Enables only bit <n>

Figure 1-1 shows the tree structure of the High Level Commands used by the VRFS.

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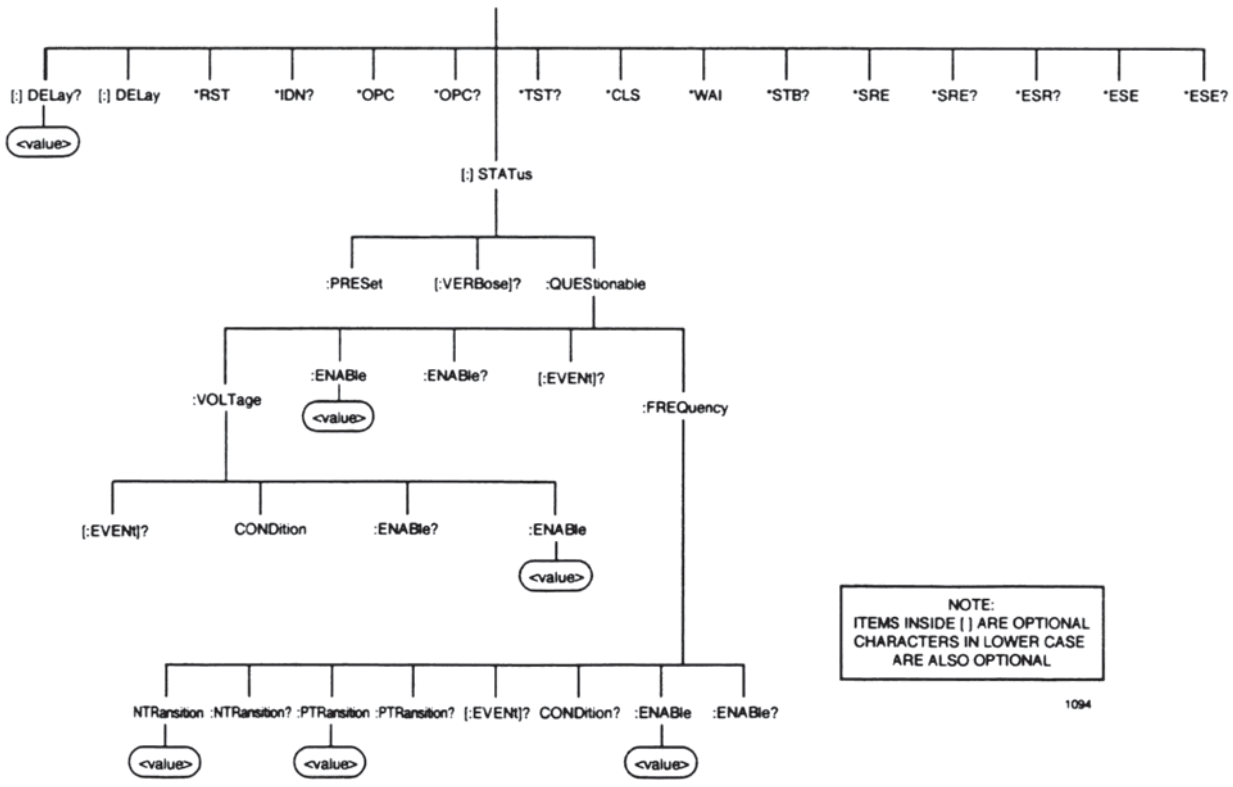


Figure 1-1. High Level Command Tree for Model VRFS-MC

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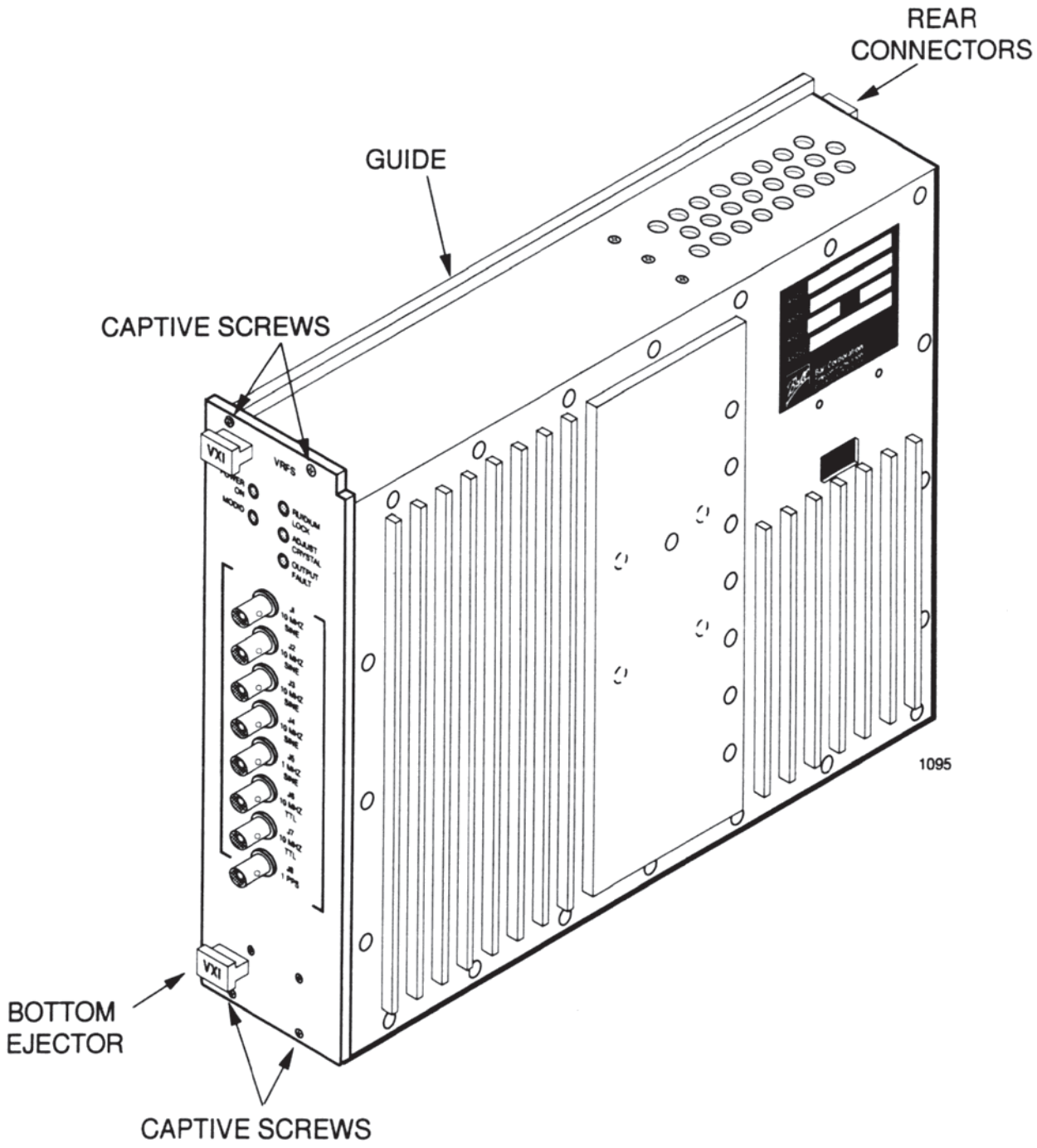


Figure 1-2. VXIbus Rubidium Frequency Standard (Model VRFS-MC)

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1.2.3 Mechanical Specifications

- Size: Two-Slot Wide, C-Size Module (shown in Figure 1-1).
  In accordance with (IAW) VXIbus Specification

- Connections: P1 and P2 IAW VXIbus Specifications
  8 each, Front Panel BNC Output Connectors
  1 each, Front Panel BNC Input Connector

- Front Panel LEDs:

RUBIDIUM LOCK	(GRN - Rb locked)
ADJUST CRYSTAL	(YEL - Xtal voltage out of range)
OUTPUT FAULT	(RED - fault condition)
MODID Line	(GRN - module on line)
POWER ON	(GRN - module is powered)

- Cooling Requirements:
  Watts/Slot: 16
  Airflow/Slot: 6 Liter/sec @ .05 mmH_2O for 5°C Rise

1.2.4 Environmental Specifications

- Operating Temperature Range: 0°C/+50°C (Ambient)
- Change in frequency Offset over Temp. range: 3E-10
- Storage Temperature: -40°C to +75°C
- Magnetic Field Sensitivity: <4E-13/AM-1 (worst case)
  (3E-11/Gauss)
- Relative Humidity: 95%
- EMC: IAW VXIbus Specification

1.3 Shipping and Receiving Information

The Model VRFS is packaged and shipped in a foam-packed container. The unit was inspected mechanically and electrically prior to shipment. Upon receipt of the unit, a thorough inspection should be made to ensure that no damage has occurred during shipping. If any damage is discovered, contact Ball Corporation, Efratom Division, 3 Parker, Irvine, CA. 92718-1605. Telephone (714) 770-5000; FAX (714) 770-2463; Telex 685-635. European customers should contact Ball Efratom Elektronic GmbH, Fichtenstrasse 25, 85649 Hofolding, West Germany, telephone 08104/90 40. If reshipment of the unit is necessary, the original container and packing should be used. If the original container is not available, a suitable container with foam-packing is recommended.

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1.4 Installation

The VRFS has been designed to be installed into a C-size VXI mainframe, using any slot except slot 0 (zero), which is reserved for the resource manager. It is recommended to place the module in the right-most slot so that the FRS Rb crystal oscillator voltage loop can be calibrated while powered (by removing the right side panel of the VXIbus mainframe to reveal the right rf shield of the VRFS module). After setting the Rubidium Frequency Standard address on the eight position DIP switch accessible through a cut-out on the right side cover of the module (refer to Section 1.5.3) slide the VRFS into the mainframe until it stops against the backplane. At this point rock the module gently back and forth to seat the VRFS connectors into the backplane receptacles. The unit ejectors will be at right angles to the VRFS front panel when the instrument is properly seated in the backplane. Once the module is seated in the backplane, tighten the two captive screws above and below the ejectors to secure the VRFS into the VXI chassis.

1.4.1 Installing Interrupt Jumpers

The VRFS is an interrupting device and uses the IACKIN* and IACKOUT* signals. Make certain that installation of IACK* jumpers is according to the chassis manufacturer's guidelines. If the jumpers are not installed properly either the VRFS will not generate an interrupt (IACK* - signal disconnected), and/or the interrupt acknowledge line is not propagated down the chain.

1.4.2 Electrical Check-out

The VRFS powers up automatically once it is seated in the backplane of the VXI chassis. Check to see that the expected outputs are present on the front panel BNC connectors using an oscilloscope probe.

1.5 Operation

1.5.1 Introduction

The VRFS is a two-wide "C" size VXI module that has two connections to the VXI backplane, P1 and P2, where it receives commands and data, responds to queries, and receives necessary power. The VRFS front panel supports nine BNC connectors consisting of one input (J9), and eight outputs (J1 through J8).

The module resides in a VXI chassis and is subject to all of the benefits and restrictions of such an environment. All power is supplied through the VXI chassis. Access to the VRFS is by means of high level ASCII commands sent through the VXI controller.

1.5.2 Controls, Connectors, Indicators, and Tests

All control of the module is through the VXI mainframe. The VXI controller can be prompted by the operator to send queries to the module to obtain the status of the device from the status byte. These responses consist of the statuses of the eight outputs, the status of the rubidium lock condition, and the status of the crystal oscillator's control voltage. In addition to these status indications, the VXI controller can also set and query the value of the delay.

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There are also five general Light Emitting Diode (LED) status indicators located on the front panel of the module:

OUTPUT FAULT
RUBIDIUM LOCK
CRYSTAL ADJUST
MODID
POWER ON

The POWER ON indicator illuminates when all three power supplies (5V, 12V, and 24V) are present.

The RF Output Status indicator illuminates and alerts the operator when any of the eight outputs has failed.

The Rb lock indicator illuminates when the Rb oscillator is locked.

The MODID indicator flashes at power-up when the mainframe microprocessor indicates that a module is located in the VXI chassis at the VRFS position.

The CRYSTAL ADJUST indicator illuminates when the crystal voltage of the Rb Oscillator is out of range.

1.5.3 Logical Address Selection

The address of the VRFS can be set by means of the eight position DIP switch accessible on the side panel of the VRFS side panel. Figure 1-3 provides a view of its location on the module.

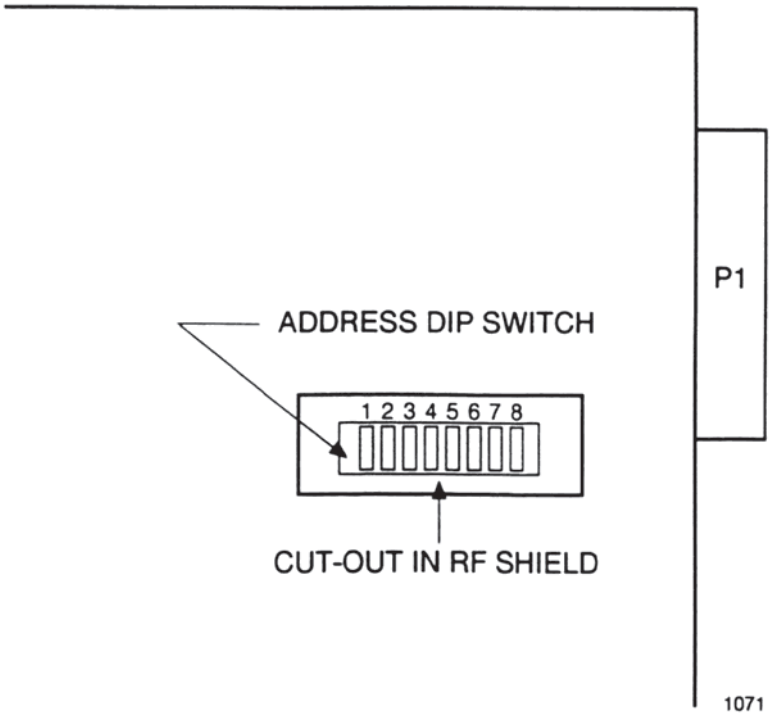


Figure 1-3. Setting the Logical Address of the VRFS

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All 256 addresses can be set, however, there are two unique addresses that cannot be used: Address "0" is reserved for the VXI mainframe slot zero resource manager, and address 255 is reserved for dynamically configurable instruments. The design is such that there is active low logic at the switch. To generate a logical 1, the switch must be turned OFF. Switch position 1 is the least significant bit. The VRFS is shipped with address 16 set up on the DIP switch. The VRFS is shipped with a label specifying the address set at the factory, the power consumption of the module, and the interrupt level.

1.5.4 Interrupter

In addition to serving as the frequency source, the VRFS is a programmable interrupter. This means that the VRFS, when enabled, sends Events as interrupts to the commander in the VXI chassis. These interrupts are the fault indications discussed above, and in Section II. Programming.

The following is a brief explanation of how the interrupt mechanism in the VRFS works. The example given is based on the National Instruments GPIB-VXI card being used as the Slot 0 Resource Manager.

The interrupt in the VXI-GPIB system involves two buses, the VXIbus and the GPIB bus. The VRFS is connected to the VXIbus and the NI GPIB-VXI resource manager is connected to both the GPIB and the VXIbus. This kind of setup allows the operator to treat a VXIbus instrument as a GPIB instrument.

1.5.4.1 Configuration

There are seven interrupt lines IRQ1 - IRQ7 in the VXIbus. When the power is applied the VRFS is not connected to this interrupt line. IRQ7 has the highest priority. Once the self test is passed, the VRFS enters the CONFIGURE sub-state. During the CONFIGURE sub-state the resource manager sends the Assign Interrupter Line command to the VRFS. When this command is successfully executed the oscillator is assigned to one of the seven interrupt lines.

1.5.4.2 Interrupts

Once the VRFS is assigned an interrupt line, it waits for an event to happen before it can pull the assigned interrupt line low. The event can occur in the analog as well as the digital section of the VRFS.

1.5.4.3 Events

A device may have several events that cause interrupts. In the VRFS there are three major analog events that can cause interrupts: failure of one of the eight rf outputs; the crystal voltage exceeds the limits, or the Rb oscillator is not locked.

The microprocessor in the VRFS monitors the condition of these signals at a regular interval of 1 second. When an abnormal condition occurs, the processor proceeds to pull the interrupt line, providing it has been enabled to do so.

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Events originate in the digital section through programming errors such as syntax errors, unidentified commands, out of range parameter values, etc, and can cause interrupts when enabled.

1.5.4.4 Enabling Events

Events can be enabled and disabled globally, as well as individually. The VXI standard has three pre-defined events: No Cause Given, Request True, and Request False. In addition to these three pre-defined events the VXIbus standard allows user defined events also. These events can be enabled or disabled individually using the high level commands

.

1.5.4.5 Global Event Control

The EVENT Enable* bit 2 of AMC (Asynchronous Mode Control) command allows the operator to globally enable or disable all the events of a device. This is a very handy mechanism to quickly enable/disable all the events of a device and eliminates the need to deal with individual events one at a time. EVENT Enable* bit (b2), when set to 1, disables the interrupt and enables the interrupt when it is set to zero. At Power On the global event, request true, request false events are automatically enabled.

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SECTION II

PROGRAMMING THE VRFS

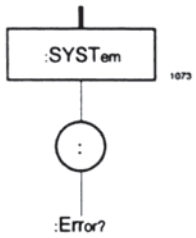
2.1 Description

The VRFS has been designed both for accuracy and ease of use. The command set allows the operator to read the lock status of the Rb oscillator, the control voltage of the crystal adjust circuit, and other parameters necessary to ensure that the device is operating properly before a test sequence is initated on the VXIbus mainframe. Status byte and event registers can be selectively read by the operator, allowing hardware faults in the VRFS to be identified through software.

2.2 Common VXIbus/VRFS Command Definitions

All operator commands are typed in at a keyboard interfaced to a PC-compatible VXIbus computer and the VXI message-based commander in the computer interrogates the VRFS status byte register. Of the ten VXIbus specified commands, the VRFS recognizes and uses seven:

2.2.1 System Subsystem



The System subsystem returns the error number and description of the errors in the error queue. The numbers range from -32768 to -32767 with the negative numbers specified by SCPI and the positive numbers Oscillator dependent. When there are no errors, a zero code is returned as follows:

```
0,  "No error".
```

The error queue is a first in first out. Only one error is displayed for each query. When all errors have been read from the queue, the zero error code will be returned. If the queue has overflowed, the last error code returned will be:

```
-350, "Queue overflow".
```

The queue is cleared at Power On, upon reading the last item from the queue, and upon receiving *CLS command. For list of the VFRS-MC error codes, refer to Appendix B.

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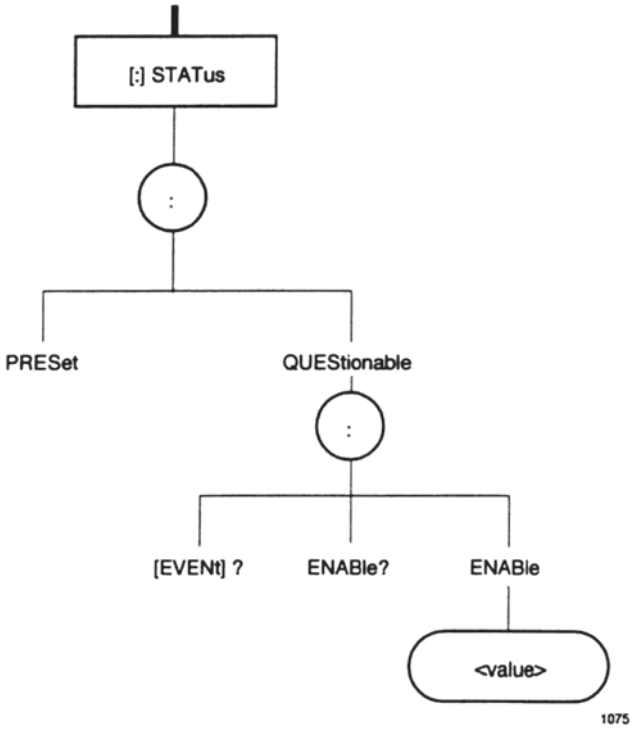
The response to this query will always take the following format:



For example, a return may appear as follows:

-112, "Program mnemonic too long"

2.2.2 Status Subsystem



This subsystem contains the Status reporting registers. The Preset command allows the user to preset certain event registers to a known value, as shown in the table below.

Event Enable Register	Preset Value
ESE - Std. Event Enable Register	0
FRS - Event Enable Register	7
Voltage Event Enable Register	255

In general, a status register fits into a 16 bit integer with the most significant bit always being zero (positive logic). Unused or "don't care" bits in masks and registers always be read back as zero when queried.

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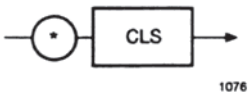
2.2.3 Common and Low Level Commands

2.2.3.1 Common Commands

The VRFS responds to all of the mandatory Common commands (refer to IEEE 488.2-1987). But there are many Common commands that have limited meaning in this device and hence it will accept those Common command for compatibility, but does not do anything with them.

***CLS** **Clear Status** Command

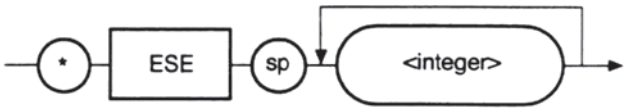
The Clear Status command clears all the Event Registers summarized in the status byte. In addition to the event registers the output queue is also emptied. The value of the Status Byte will be zero immediately after the execution of this command, provided there is no other condition existing that will cause the immediate generation of an interrupt.



1076

***ESE** **Standard Event Status Enable** Command

The Standard Event Status Enable command sets the Standard Event Status Enable Register as follows:



1077

The <integer> can range from 0 through 255 and is the mask enable value, eg. a value of "3" will enable bits 0 and 1. Even though any value between 0 and 255 is accepted, only two events are enabled in the VRFS. The two events that are meaningful in this oscillator are:

a. EXE: Execution error caused when value of a parameter is out of range and
b. CME: Command error due to Syntax error, or when unimplemented or invalid commands are received.

The rest of the bits are always set to zero even if they are enabled by the command.

***ESE? Standard Event Status Enable Query**

The Standard Event Status Enable query allows the programmer to determine the current contents of the Standard Event Status Enable Register.



1078

The response to the query will be an integer between the range of 0 and 255 representing the value of the 8 bits in the event status register.

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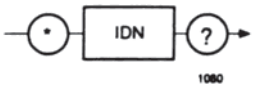
*ESR? Standard Event Status Register Query

The Standard Event Status Register query allows the programmer to determine the current contents of the Standard Event Status Register. Reading the Standard Event Status Register clears it.



*IDN? Identification Query

The intent of the Identification query is to identify unique devices over the system interface.

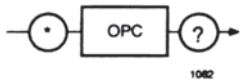


The response is organized into four fields separated by commas and will be:

BALL EFRATOM,3840,<serial number>,<firmware revision level>
The serial number returned will always be zero.

*OPC Operation Complete Command

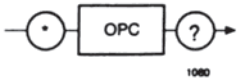
The Operation Complete command normally causes a device to generate the operation complete message in the Standard Event Status Register when all pending selected operations have been finished. The VRFS accepts this command, but the command has no meaning to this device. Neither an error or an action is generated based on this command.



*OPC? Operation Complete Query

The Operation Complete query places an ASCII character 1 into the device's Output Queue when all pending selected device operations have been finished.

The response will be:



1

*RST Reset Command

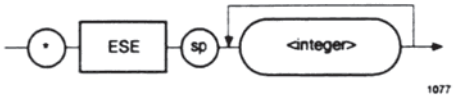
This reset command initializes device-specific functions within a device. Since the VRFS has only one device specific function - *the delay*. Upon receiving this command the delay will be cleared to zero.



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***SRE** **Service Request Enable Command**

The Service Request Enable command sets the Service Request Enable Register bits permitting the programmer to select which messages in the Status Byte Register may cause service requests.



1077

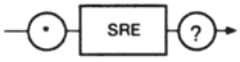
The integer can range between 0 and 255. The mask value of bit 6 will be ignored; it is a fixed logical 0. Even though any value between 0 and 255 is accepted, only three events are enabled in the VRFS. The three events that are meaningful in this oscillator are:

a. QUES: Questionable summary bit to detect the voltage and frequency status of the VRFS.
b. MAV: Message Available bit.
c. ESB: Event status bit to detect command and execution errors.

The remainder of the bits are always set to zero even if they are enabled by the command.

***SRE?** **Service Request Enable Query**

The Service Request Enable query allows the programmer to determine the current contents of the Service Request Enable Register.

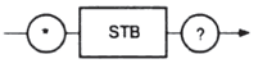


1080

The response will be the mask value from 0 through 63, or 128 through 191.

***STB?** **Read Status Byte Query**

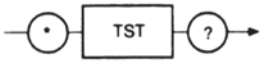
The Read Status Byte query allows the programmer to read the Status byte and the Master Summary Status bit.



1086

***TST?** **Self-Test Query**

The Self-Test query causes an internal self-test that tests both the EPROM and the static RAM. If both memories pass the self test, then the response will be "Self Test Passed". If failure occurs in either memory there will be no response from the unit. Upon successful completion of *TST, the device settings will be restored to their values prior to the *TST?.



1088

***WAI** **Wait-to-Continue Command**

The VRFS will accept this command, but the command has no meaning to this device. Neither an error or an action is generated based on this command.



1088

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2.2.3.2 Low Level VXIbus Commands

Low level commands are the VXIbus Word Serial Commands and require complex bit and byte manipulations. However, they are transparent to the message based device user and a through knowledge of these commands is not necessary to program the VRFS. Since the VRFS is a message based device, the user may skip this section, if desired, and concentrate on the High level programming section and Command Command section.

ANO **Abort Normal Operation:**
This command causes the VRFS to cease its normal operation as fast as possible. It stops processing incoming signals and resets the **ready** bit in the Status register to 0 (zero) (C.2.4.7.3). The interrupt generation is also disabled (C.2.91) and if an interrupt operation is pending it will be reset. The unit is reconfigured to the default state; the power-up memory test is NOT performed. Both DIR and DOR bits in the response register are set to zero. The unit goes into CONFIGURE Sub-state and waits for the BNO (Begin Normal Operation) command. This command is usually issued by the VXI slot zero resource manager.

BNO **Begin Normal Operation:**
This commands the VRFS to begin normal operation. The **ready** bit in the Status register is set to 1. Generation of an interrupt is enabled upon receiving this command. BNO is usually issued by the VXI slot zero resource manager.

ENO **End Normal Operation:**
This command orders the VRFS to end its normal operation in an orderly manner without any time limit restraints. Incoming signals are no longer processed. All of the event registers are cleared. Both the DIR and the DOR bits in the response register are set to zero. The unit goes into CONFIGURE Sub-state and waits for the BNO command to be issued by the VXI slot zero resource manager.

CLR **Clear:**
Upon receiving the clear command, the VRFS removes all output data in the VXI Data Low register. The VRFS will discard all data due for output from operations currently in progress and become ready to receive a new command. The **read ready** bit in the Response register will be reset to 0. Both DIR and DOR bits in the response register are set to zero. The unit stays in the NORMAL OPERATION Sub-state and waits for the BNO command. The Ready bit in the status register is not cleared but the Error bit in the response register is cleared. Both the input and output buffers are cleared. The DIR bit is set and the DOR bit is reset to zero. The VRFS is waiting for a new command. The **Err*** bit of the Response register will be de-asserted and any pending **read protocol** error command responses will be cancelled.

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AMC **Asynchronous Mode Control**
This command allows the VRFS to generate interrupts through the Global event bit. Upon Power On, this bit is automatically set, which allows the interrupt generation. This command is rarely used since there are so many other easy to use high level commands in the system that allows the user to enable and/or disable interrupts.

Control Event: This command allows the VRFS to generate interrupts through the *request true* and *request false* events. Upon Power On, these two events are automatically set, which allows the interrupt generation. These two commands are rarely used since there are many easy to use high level commands in the system that allow the user to enable and/or disable interrupts.

The *request true* and *request false* events are useful in a VXI-GPIB system. The VRFS sends a request true interrupt to assert the SRQ line through the Slot 0 resource manager that has the capability. It also sends the *request false* event (to deassert the SRQ line) once the device is polled.

Read STB: This command is equivalent to the Common command ***STB?**. This command returns the value of the Status byte and the Master Summary Status bit.

Read Protocol: This command reads the Protocol register. The VRFS supports Event Generation, VXIbus Instrument and IEEE 488.2 protocols.

Read Protocol Error: This command is used when the Error bit in the response register of the VRFS unit is set. Upon receiving this command the unit resets the Error bit and returns a value that indicates the type of protocol protection.

Miscellaneous Word Serial Commands:

Byte Available and **Byte Request**: these two commands are atomic commands that are used by the Commander and the device as part of the *word serial byte transfer protocol.*

Assign Interrupter Line, **Read Interrupter Line**, and **Read Interrupters**: These commands are used by the interrupt handlers (usually the Slot 0 resource manager) to configure the interrupt mechanism during the power-up sequence. The VRFS will return a value 1 to the **Read Interrupters** command. For further information on these commands, refer to the VXIbus standard and the Slot 0 resource manager's user manual.

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2.2.3.3 VRFS Command Set

The VFRS-MC specific command set: `:STATus:VERBose?`, `DELAy nn`, and `DELAy?`, and the parameters of these unique commands are described below.

2.3 VRFS Command Definitions

The programming of the VFRS-MC is directed at monitoring the health and accuracy of the Rb oscillator that is the frequency source for all outputs. The following commands allow the operator to sample the health of the module, to set the time delay between the 1 PPS input and the 1 PPS output, and obtain the current delay in effect. The syntax of the commands is as shown.

2.3.1 `:STATus : VERBose?`

This command returns a long string as a response in the following format:

RB Lock/Unlock
Xtal Adj. Status
RF Output Status
Output #1 Pass/Fail
....
Output #8 Pass/Fail

The response indicates if the Rb oscillator is unlocked or locked, shows whether the current voltage for the crystal adjust loop is out of the specified range, and RF Output Status indicates which, if any, of the eight outputs of the module has failed (Output #1 through Output #8).

2.3.2 `:DELAy <nn>`

This command allows the operator to set the time delay between the Input 1 PPS and the Output 1 PPS. The delay is in seconds and the resolution is 100 nS. An application for this feature is to allow synchronization to an external reference for time keeping.

2.3.3 `:DELAy?`

Entering this command allows the operator to determine the current delay value (shown in seconds). At POWER ON the delay value is set to 0 (zero).

2.4 Programming of Interrupt Events

There are three major analog events that cause interrupts to be sent to the VXIbus commander:

1. The failure of one or more of the eight rf outputs.
2. The Crystal Adjust voltage feedback loop for the Rb oscillator exceeding its limits.
3. The Rb oscillator losing lock.

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The VRFS microprocessor monitors each of these conditions at regular 1 second intervals. When an abnormal condition occurs the processor will cause the appropriate status bit to go from a logic low (0) to a logic high (1) state, provided it has been enabled to do so by the operator.

2.4.1 Status Reporting

In a VXIbus System a controller (usually a computer) and one or more instruments are tied together to perform several tasks, such as measuring power, generating voltages of different wave-forms and/or frequencies, or calibration of standards, etc. During the execution of these tasks, instruments typically must display event and status information, or must report to the controller. There are different types of displays, CRTs, LEDs, and other visual means that indicate the present status of critical parameters in an instrument. But displays are geared to the human interface and cannot be used with computer interfaces. The interrupt event and status reporting mechanism, with the required hardware, are used to report these events to the controller in charge.

2.4.1.1 Events

An event can be a short circuited output voltage, out of spec output current, over-temperature reading for the device, Rb oscillator falling out of lock, and so on. When an event is detected by the processor, it sets the corresponding event bit to true (logical 1). In the VRFS, there are eleven events that can be monitored by the commander. These consist of eight output voltage events (one for each output) checking whether the output is short-circuited, one crystal adjust event determining if the crystal voltage is above or below the operating range, and two events signifying that the Rb oscillator is "in lock" or has fallen "out of lock".

2.4.1.2 Status Information

Typical status information deals with operations, i.e., whether an instrument is idle, busy measuring, waiting for trigger, etc.

2.4.2 Status Data Structure

The format of the Status Data Structure of the VRFS is based on two industry standards, the IEEE 488.2 and the Standard Commands for Programmable Instruments (SCPI). As per these standards, events are stored by the module (instrument) in the event register, while event enable bits are saved in the event enable register. These two registers are compared and the result is stored in a summary bit. The basic structure (as illustrated in Figure 2-1) and it consists of:

1. an optional condition register
2. an optional transition register
3. a pair of registers called the event register and the event enable register
4. ANDing of the outputs of these two registers, and
5. a summary bit that summarizes the result using OR logic, as shown in Figure 2-1.

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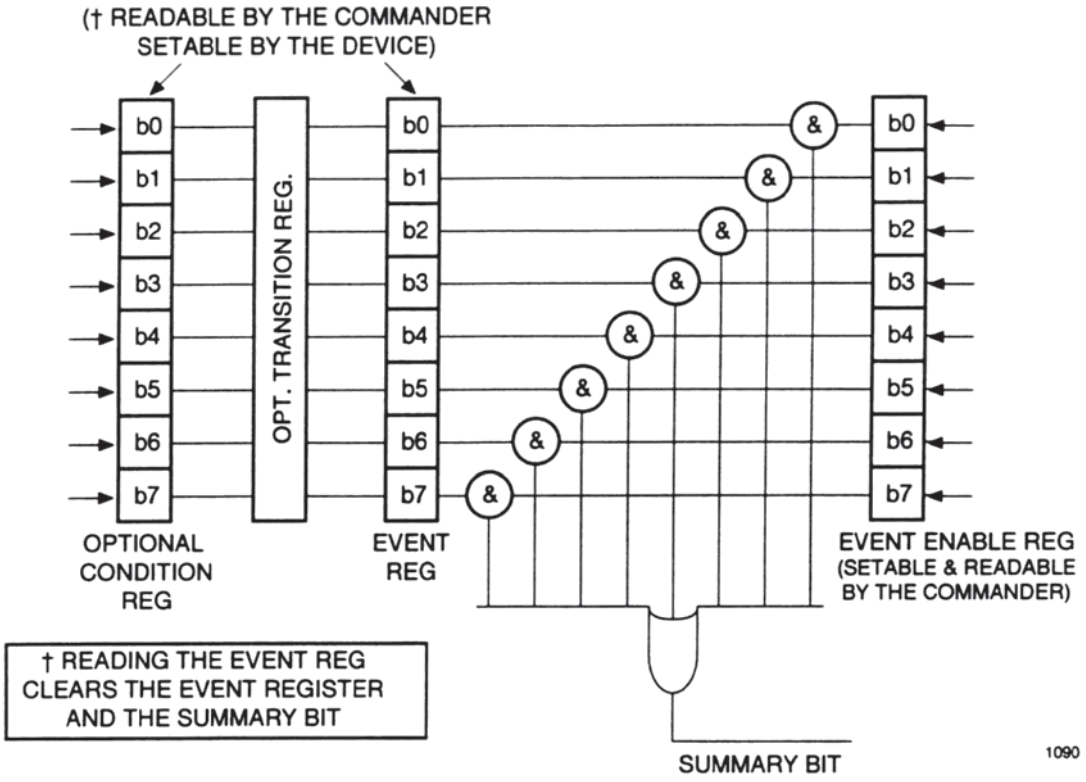


Figure 2-1. Structure of Event and Event Enable Registers

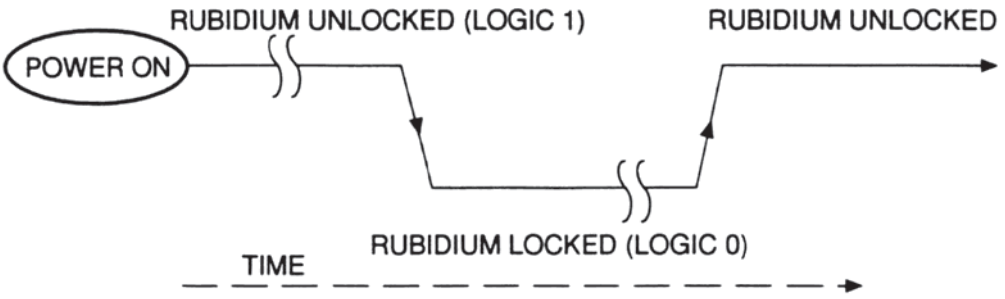
2.4.2.1 The Condition Register

A condition register is an optional register that reflects the current status of the device. In the VRFS VXIbus oscillator there are two condition registers - one for the voltage related events and one for the frequency related events. The condition register is constantly updated at regular intervals - that is the bits in this register are set or reset to reflect the current condition of the register. If the Commander did not read the condition register at regular intervals it might not detect any transient conditions that may have occured for only a brief moment. Of course, as explained below, the event register, when enabled, always catches any transient events that might have come and gone.

2.4.2.2 The Transition Filter Register

Transition filters are used when more flexibility is desired in controlling the event reporting. Typically the events are reported as in either a true or false state - where the normal conditions are represented by a true state and abnormal conditions by a false state. The true state is represented by setting the corresponding bit to zero and the abnormal state by setting the bit to 1. However, in some cases the state of the event bit is less important than the actual transition to either state.

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For example, in the VRFS the output frequency is not locked to the internal phase locked loop until the oscillator is warmed up and has reached the right operating conditions. So it is important to know when the oscillator went into lock as well as when it went out of lock, as shown above, meaning that the user is interested in the transition to both states.

2.4.2.3 The Event Register

The event register in a device does not reflect the current condition of the device, rather it reflects an event that occured in the past. For example, a short in the output of a channel may be permanent or transient. But the event register, when and if that short circuit occurs, always remembers that event by saving it in its event register. This register is not cleared even if the short circuit at the output no longer exists. The event register is cleared only by the Commander when it reads that register, or clears it with a `*CLS` command. So a condition register is added to the status data structure to save the current status of the device.

2.4.2.4 The Status Byte

The IEEE 488.2 standard requires each instrument to have a Status Byte that is made up of seven summary bits and one master summary bit. The seven summary bits (b0 - b5 & b7) in the Status Byte are summarized and saved as the master summary bit (MSS - bit b6) in the Status Byte. These summary bits of the Status Byte quickly indicate the overall status of the VRFS module. Each summary bit in the Status Byte can be further expanded as shown in Figure 2-3 to accomodate the status requirements of the instrument.

Status registers are paired: i.e., an *event register* and an *event enable register*. Interrupt events will be stored in the registers as they occur, but will go onto the interrupt line only if so requested by the operator. By requesting attention, the operator can select which event will go on the interrupt line.

The operator can change the masking at will by reprogramming the status of the Enable registers monitoring either the voltage or frequency of the Rb oscillator.

The VRFS implements only two of the seven possible summary bits. These are the Questionable summary bit (b3) and the IEEE 488.2 mandated standard Event Status bit (b5). All other bits except the master summary bit are set to zero all the time

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2.4.2.2 Reading the Status Byte

The Status Byte can be read using two commands. One is the VXIbus word serial command:

```
Read STB
```

The other command is the IEEE 488.2 common command

```
*STB?
```

Reading the Status Byte does not clear it.

2.4.2.3 Clearing the Status Byte

The Status Byte can be cleared by reading the fan-out summary event registers.

NOTE:
The *CLS command clears all the event registers in the device.

2.4.2.4 Reading the Questionable Events Register

Reading this register can tell the operator the summary of the output voltage and FRS events.

The command to read this register is:

```
:STATus:QUEStionable?
```

This will return the value of the Questionable Event register value. It will be one of the possible four values 0, 1, 16, and 17.

Value	Description
0	No events occured
1	Voltage Summary bit set - one or more output has a short circuit
16	Freq. Sumry bit is set - Rub. lock/unlock or Xtal voltage needs adj.
17	Both Voltage and Frequency summary bits are set.

Reading this register will automatically clear this register and will also set the Questionable summary bit (b3) in the Status Byte to zero. The IEEE 488.2 common command:

```
*CLS
```

also clears this event register. Reading either the Voltage Event register or the FRS Event register, whichever caused the summary bit to be set, will also clear this register. The sections below describes the method of reading these two event registers.

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2.4.2.4 Enabling the Questionable Events

The Questionable Enable Events register can be written into using the following command:

```
:STATus:QUEStionable:ENABle <n>
```

The value should be 0, 1, 16, or 17, which will either disable or enable selectively the desired event to enable the interrupt. For example, if one wants to enable only the FRS events to generate an interrupt, then the command will be:

```
:STATus:QUEStionable:ENABle 16
```

The current value of the Questionable Enable Events register can be read back by the commander using the following command:

```
:STATus:QUEStionable?
```

2.4.2.5 Voltage Event Register and Voltage Summary Bit Register

The VRFS has eight outputs that can deliver sine-wave, TTL, and one pulse per second (1 PPS) wave-forms. These outputs are monitored constantly by a short circuit detection circuit. When and if an output is short circuited, the processor detects this event and stores it into the voltage event register, as shown in Figure 2-2. If the events are enabled, then the voltage summary bit will be set true.

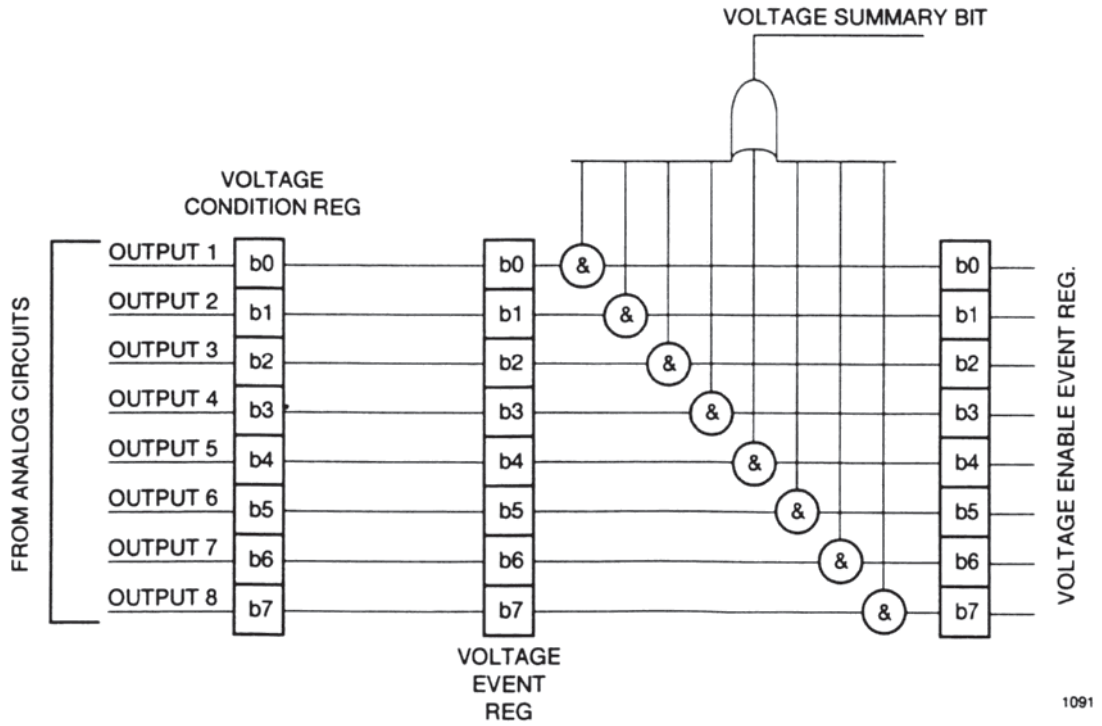


Figure 2-2. Voltage Event and Voltage Summary Bit Registers

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PROGRAMMING

MODEL 3840 STATUS DATA STRUCTURE

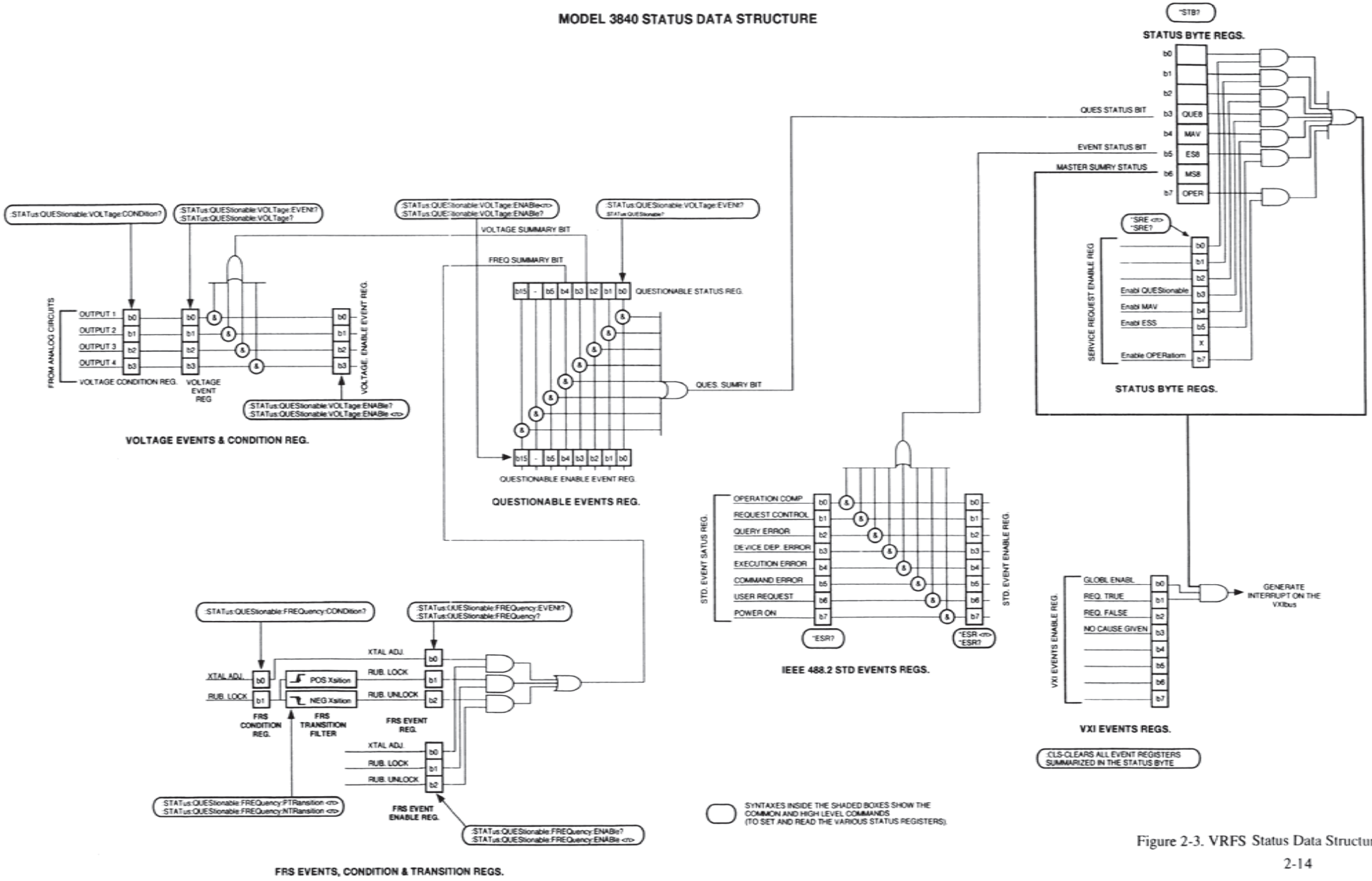


Figure 2-3. VRFS Status Data Structure

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2.4.2.6. Reading and Clearing the Voltage Event Register

Once an event bit is set in the voltage event register, it can be cleared by one of two methods. By reading the event register using the command:

```
:STATus:QUEStionable:VOLTage?
```

Which will return the value of the Voltage Event register. The value will be between 0 and 255. The other method of reading the register is by sending the common command:

```
*CLS
```

2.4.2.7 FRS Event and Frequency Summary Bit Registers

The VRFS has a highly stable Rb oscillator. There are three events in the oscillator that can indicate the stability of the frequency output. The crystal voltage and the lock, or unlocked, condition of the rubidium oscillator. At Power On, the unit needs several minutes of warm-up before the Rb oscillator is locked and stable. These events are constantly monitored by the microprocessor in the Rb oscillator at a one second interval. Changes are detected and saved in the FRS event register and its data structure is shown in Figure 2-4.

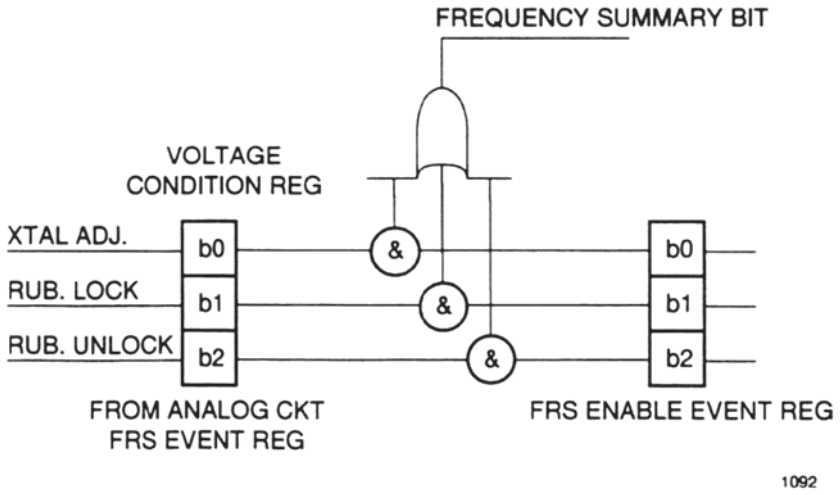


Figure 2-4. FRS Event and Frequency Summary Bit Registers

2.4.2.8 Reading and Clearing the FRS Event Register

Once an event bit is set in the FRS Event register, it can be cleared by one of two methods, first, by using the command:

```
:STATus:QUEStionable:FREQuency?
```

Which will return the value of the FRS Event register. The value will be between 0 and 7. The other method is by sending the common command:

```
*CLS
```


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2.4.2.9 Interrupt Generation

When an event occurs, its corresponding event in the event register is set to 1 and this propagates through the status data structure (see Figure 2-2), which causes its corresponding summary bit/bits to be set to one. Finally, this causes the MSS bit in the Status Byte to be set to one. Once the MSS bit is set to one, then an interrupt request procedure starts.

The procedure first verifies that the Global Enable Bit (set through VXIbus word serial Asynchronous Mode Control command) is true and then verifies that the Req. True event is also true. if both of them are enabled, then the assigned IRQ line is pulled low. The commander then starts an interrupt acknowledge cycle during which the status/ID register content is sent to the controller. The ID part consisits of the logical address of the module and the status part as the event, which will always be *Request True Event.*

Following the interrupt acknowledge cycle the controller reads the *Status Byte*. The controller then examines the *Status Byte* and determines which summary bit was set. In the VRFS's status byte, only two summary bits are used. They are the Questionable and Std. Events Status bits. Reading the *Status Byte* will not clear its contents and thus it can be read as many times as needed. The Commander then, based on which summary bit is set, will read the corresponding event register/registers. Once an event register is read, its contents and its summary bit will be cleared (set to zero).

2.4.3 Power On Conditions

Event registers: At Power On, all the event register bits and summary bits are cleared (set to zero).

Event Enable registers: There are two sets of event enable registers, IEEE 488.2 enable registers and SCPI enable registers. IEEE 488.2 enable registers are SRE and ESE and these two event enable registers are cleared at Power On. There is only one SCPI defined enable register in the VRFS, the Questionable Enable register. This is also cleared at Power On.

Device Dependent Enable Registers: There are two device dependent enable register. The Output Enable register associated with the Voltage summary bit and the FRS Enable register associated with the Frequency summary bit. These two registers will be set to all ones (logical 1) at Power On so these events are enabled to interrupt.

NOTE

When an application program is written by the operator, make sure the following sequency of commands are sent at Power Up (pp. 18-4 of SCPI):

```
*CLS
*SRE 0
*ESE 0
:STATUS:PRESet
```


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2.4.3.1 Clearing Event Registers

Once a bit in the event register is set, it stays set until it is cleared. This is called a "sticky" bit. The event registers can be cleared in one of two ways. *CLS, the Clear Status common command clears all the event registers in the VRFS. This action in turn clears all the summary bits and eventually the master summary bit.

The second method to clear the events register is to read the actual register. This will not only return the value of the event register to the commander, but also clears all the event registers that have just been read.

2.4.3.2 Clearing the Summary Bit

There are seven possible summary bits in the status byte. None of these summary bits can be cleared by reading the status byte. Summary bits can be cleared by reading the actual event registers that set the summary bits.

The commands specific to handing interrupts as shown in Figure 2-1 linked to their registers, and described below (syntax is as shown in capital letters and brackets), allow the user to selectively interrogate the contents of the various registers of the module.

Standard Events Register commands

***ESR?**	Standard Event Status Enable query
***ESE <n>**	Standard Event Status Enable <bit number>
***ESE?**	Standard Event Status Enable query
***CLS**	Clear Status Command (clears all registers)

Status Byte register commands

***STB?**	Queries Status Byte

Service Request Enable Register

***SRE <n>**	Service Request Enable command <bit number>
***SRE?**	Service Request Enable query

Questionable Status register commands

:STATus:QUEStionable:EVENt?	Returns content of Voltage Summary Bit
:STATus:QUEStionable?	Sums contents of Voltage Summary Bit

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Questionable Enable Events register commands

`:STATus:QUEStionable:ENABle <n>`	Returns content of bit <n>
`:STATus:QUEStionable:ENABle?`	Sums contents of register

Output Enable Events register commands

`:STATus:QUEStionable:VOLTage:ENABle?`	Enables contents of register
`:STATus:QUEStionable:VOLTage:ENABle <n>`	Enables only bit <n>

Output Events register commands

`:STATus:QUEStionable:VOLTage:EVENt?`	Returns "Hi" event bits
`:STATus:QUEStionable:VOLTage?`	Sums contents of register

FRS Events register commands

`:STATus:QUEStionable:FREQuency:EVENt?`	Returns "Hi" event bits
`:STATus:QUEStionable:FREQency?`	Sums contents of register

FRS Events Enable register commands

`:STATus:QUEStionable:FREQuency:ENABle?`	Enables contents of register
`:STATus:QUEStionable:FREQency:ENABle <n>`	Enables only bit <n>

2.4.3.3 Handling Interrupts

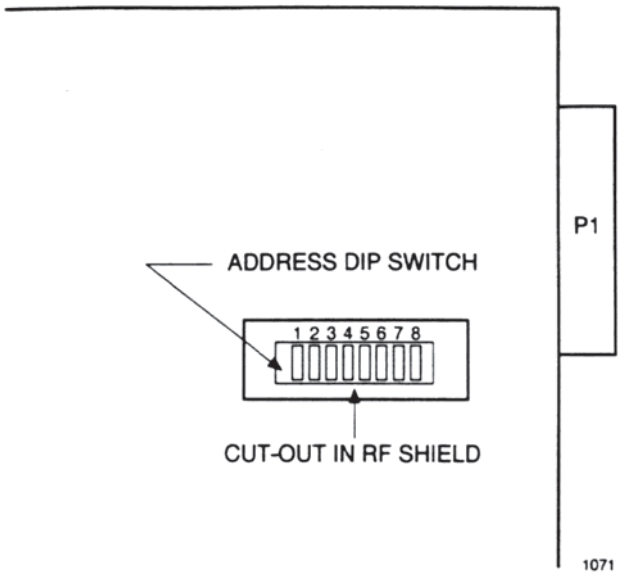
When an event occurs its corresponding event bit is set to 1 and this propagates through the status data structure, which causes its corresponding summary bit/bits to be set to one. This, in turn, causes the MSS bit to be set to one. Once the MSS bit is set to one an interrupt request procedure starts.

The processor verifies that the Global Enable Bit (set through VXI-Asynchronous Mode Control) and Req. True events are true. If both bits are enables, then the assigned IRQ line is pulled low. The controller then starts an interrupt acknowledge cycle during which the status/ID register's contents is sent to the controller. The ID part consists of the logical address of the device and the status part indicates the event (it will always be *request true event*).

Following the interrupt acknowledge cycle, the controller then reads the Status Byte and determines which summary bit has been set. In the VRFS, only two summary bits are used: the Questionable bit and the Std. Events Status bit. Both bits follow the formats specified by IEEE 488.2 and SCPI for the Status Data Structure.

Following the interrupt acknowledge cycle, the controller reads the Status Byte. The controller then examines the Status Byte and determines which summary bit got set. In the VRFSs status byte, only two summary bits are used. They are Questionable and Std. Events Status Bits. Reading the Status

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Byte will n ot clear its contents and hence it can be read as many times as needed. The commander then, based on which summary bit is set, will read the corresponding event register/registers. Once an event register is read, its contents and its summary bit will be cleared (set to zero).
Questionable Status Register: a 16 bit register holding SCPI defined summary bits. The VRFS uses only two of these bits, the Voltage Summary bit and the Frequency Summary bit.

Voltage Summary bit: The eight outputs of the VRFS are monitored constantly by a short circuit detection circuit. When and if an output is short circuited the processor detects the event and stores it into the voltage event register.

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SECTION III

DIAGNOSTICS AND MAINTENANCE

3.1 Description

The Efratom VXIbus module VRFS has been designed to be quickly swapped out with a spare unit, preventing downtime on the VXIbus mainframe. Software diagnostics allow troubleshooting to the failed rf output. Because the module is sealed to prevent the escape of rf into the VXIbus mainframe, disassembly and reassembly of the rf shields should be done only when absolutely necessary.

3.2 Troubleshooting Guidelines

If a module should fail under warranty, the module should be returned to Ball Efratom for repair. If the module fails out of warranty, major replaceable items would consist of the FRS unit, the main circuit board, connectors P1 and P2, the five LEDs, and nine BNC connectors on the front panel. The following sections provide adjustment guidelines and troubleshooting information. Disassembly of the FRS is not recommended, but a FRS manual has been included for reference.

Setting the module address at installation can be performed **without** removing the rf shields. Figure 3-1 shows the panel cutouts for the VRFS module.

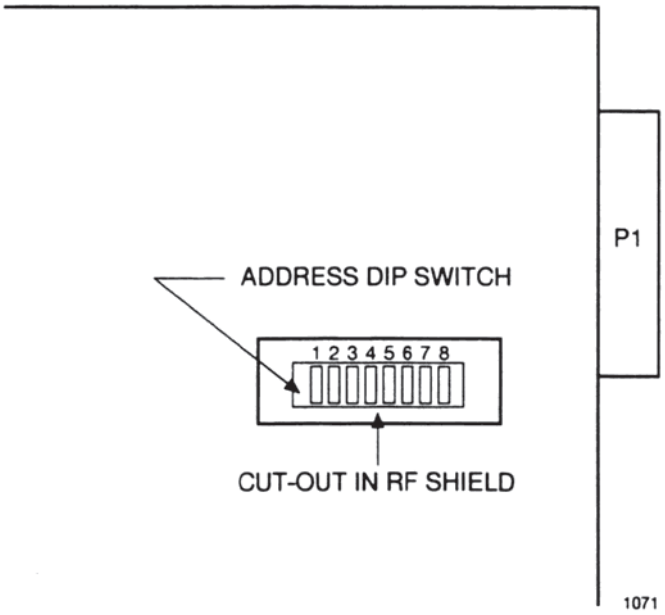


Figure 3-1. Frequency Monitor Cutout and Module Address Set Cutout Locations

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3.3 Module Disassembly

To troubleshoot and repair connectors, the right rf shield must be removed from the module. Twenty-six screws fasten the left and right shield side panels to the board. Remove all screws, placing them so they can be relocated after repairs and reinstalled (failure to replace one or more screws can result in rf leakage from the module), and lift away the right rf shield. This reveals the VRFS circuit board, the two rear connectors (P1 and P2), the FRS component attached to its finned heat shield, and the buffer logic interconnect on the board. Each BNC connector is routed to its own buffer section, with the exception of the 1 PPS input BNC connector.

3.4 LED Indicators

The five Light Emitting Diode (LED) status indicators located on the front panel of the module provide diagnostic information as well as information on the operational status of the Rb oscillator in the VRFS module. These LED indicators consist of:

OUTPUT FAULT	(RED)
RUBIDIUM LOCK	(GREEN)
ADJUST CRYSTAL	(YELLOW)
MODID	(GREEN)
POWER ON	(GREEN)

When illuminated, the OUTPUT FAULT, RUBIDIUM LOCK, ADJUST CRYSTAL, and POWER ON LEDs signify a diagnostic step, which may be followed by further action. The MODID Line LED provides a status indication.

3.4.1 LED Diagnostics

POWER ON LED

The POWER ON indicator illuminates when all three power supplies (5V, 12V, and 24V) are within specified ranges. If the indicator goes dark one of the power supplies has failed or is no longer within output specifications. The module power input lines at P1 and P2 must be checked with a voltmeter to determining if it is functioning properly. The pins to be checked are listed below, (both connectors, P1 and P2 adhere to the VXIbus format):

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	P1			P2		
	row a	row b	row c	row a	row b	row c
pin 1					+5 Vdc	
pin 2				-2 Vdc		
pin 4						-5.2 Vdc
pin 7				-5.2 Vdc		
pin 13				-5.2 Vdc	+5 Vdc	-2 Vdc
pin 19				-5.2 Vdc		-5.2 Vdc
pin 22				GND	GND	GND
pin 25				+5 Vdc		GND
pin 28				GND		GND
pin 31	-12 Vdc	+5 V STDBY	+12 Vdc	GND	GND	+24 Vdc
pin 32	+5 Vdc	+5 Vdc	+5 Vdc	SUMBUS	+5 Vdc	-24 Vdc

OUTPUT FAULT LED

The OUTPUT FAULT Status indicator illuminates and alerts the operator when any of the eight outputs has failed. There are two methods of investigating this fault. The first is through the status firmware of the module (refer to Section II, Programming); the second method is to troubleshoot the hardware. Check each BNC connector with a scope probe to determine which of the connectors lacks output. After removing the module from the VXIbus mainframe, remove the right rf shield and check the "failed" connector for shorts or opens. If there is no output from the buffer section, the associated buffer circuit has a fault and the VRFS module should be returned to the factory.

RUBIDIUM LOCK LED

The Rb Lock indicator illuminates when the Rb oscillator is in lock. If the Rb oscillator loses lock, the LED will go dark. This fault can be caused by several things: a loss of power to the FRS component mounted on the VRFS buffer board, or by a malfunction in the FRS. The loss of lock can also be a momentary effect as the Rb oscillator sweeps. Hook the FRS output up to a frequency counter (Fluke 1910A - 5 MHz to 125 MHz, or equivalent). If the frequency is stable, open the rf shield and check the input voltage at the connector to the FRS. If the voltage input is within specifications, the FRS has failed and should be replaced, or returned with the VRFS module.

MODID

The MODID indicator flashes at power-up when the mainframe microprocessor indicates that a module is located in the VXI chassis at the Rubidium Frequency Standard position. This is a status indication only.

CRYSTAL ADJUST

The CRYSTAL ADJUST indicator illuminates when the crystal voltage of the Rb Oscillator is out of range. This indicator should not illuminate when the RUBIDIUM LOCK indicator is dark. If the CRYSTAL ADJUST indicator lights, return the module to the factory. Crystal adjustment for the VRFS cannot be done in the field.

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3.5 Frequency Adjust

The frequency adjustment accessable through the cutout on the rf shielf of the VRFS is used only to modify the output frequency of the FRS in special circumstances. This is not a trouble-shooting feature.

If you wish to use this feature, call Efratom Customer Support for guidance first. An external frequency reference and an Efratom FMS-200 (or FMS-300) frequency measurement system will be required to make this adjustment.

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APPENDIX A

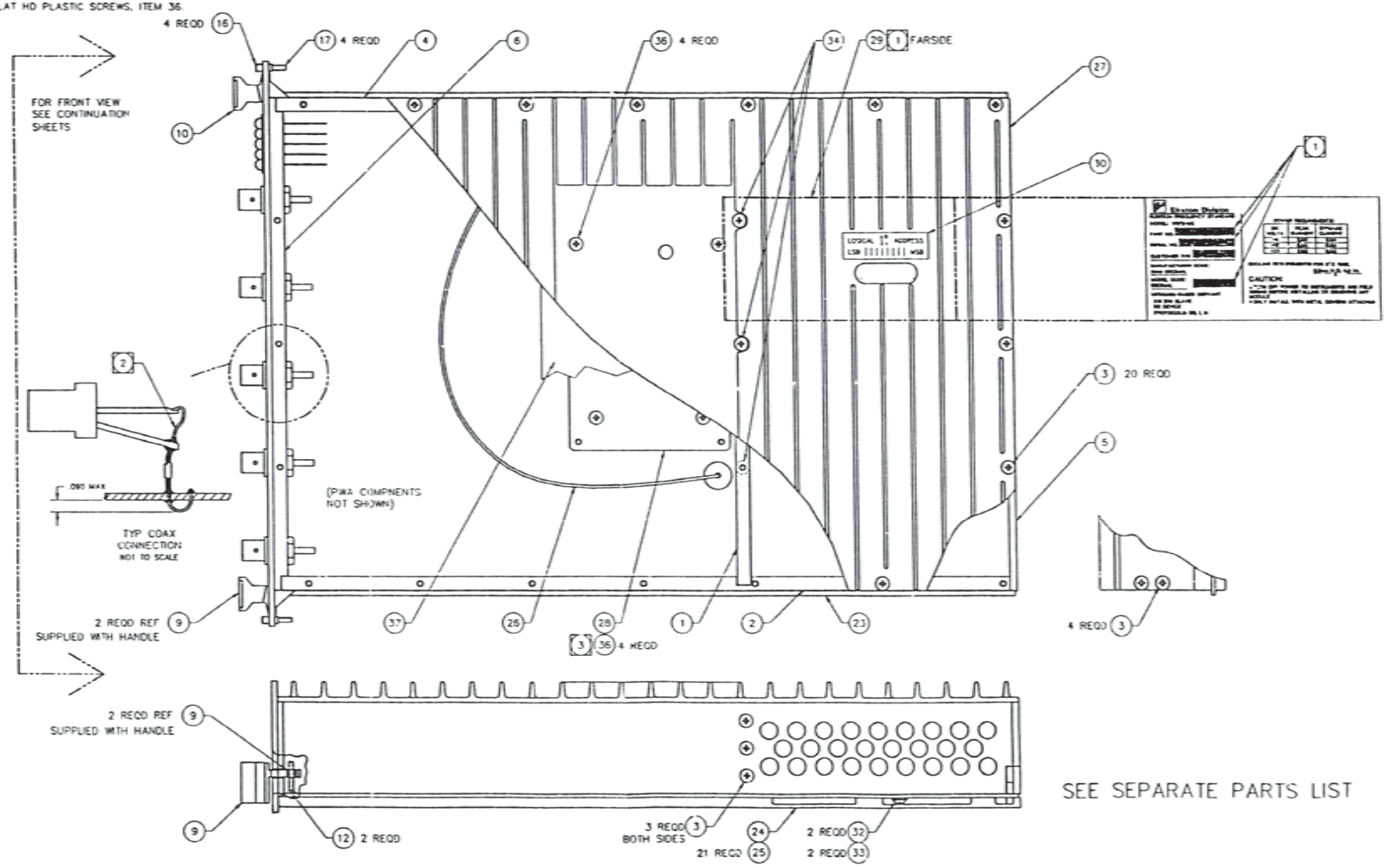
ASSEMBLY DRAWINGS, SCHEMATICS, AND PARTS LISTS

DRAWING NUMBER	DESCRIPTION	PAGE NUMBER
101790	VRFS - FINAL ASSEMBLY	A2-A5
PL101790	PARTS LIST, VRFS FINAL ASSEMBLY	A6-A19
101176	SCHEMATIC - VRFS CONTROL BOARD	A20-A24
101179	CIRCUIT CARD ASSEMBLY - VRFS	A25-26
101727	SCHEMATIC - PLL TRACK/HOLD	A27
101725	CIRCUIT CARD ASSEMBLY - PLL	A28-A29

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NOTES: UNLESS OTHERWISE SPECIFIED

1. MARK IDENTIFICATION PLATE WITH APPROPRIATE PART NUMBER, MODEL CODE AND SERIAL NO. SEE TABULATION ON SHEET 3.
2. MAKE SURE SHIELD DOES NOT TOUCH BNC PIN AND THAT THE INNER CONDUCTOR OF THE COAX IS NOT BENT SO TIGHT AS TO CAUSE IT TO CRACK.
3. REMOVE 4 TOP SCREWS FROM FRS AND REPLACE WITH 4 FLAT HD PLASTIC SCREWS, ITEM 36.

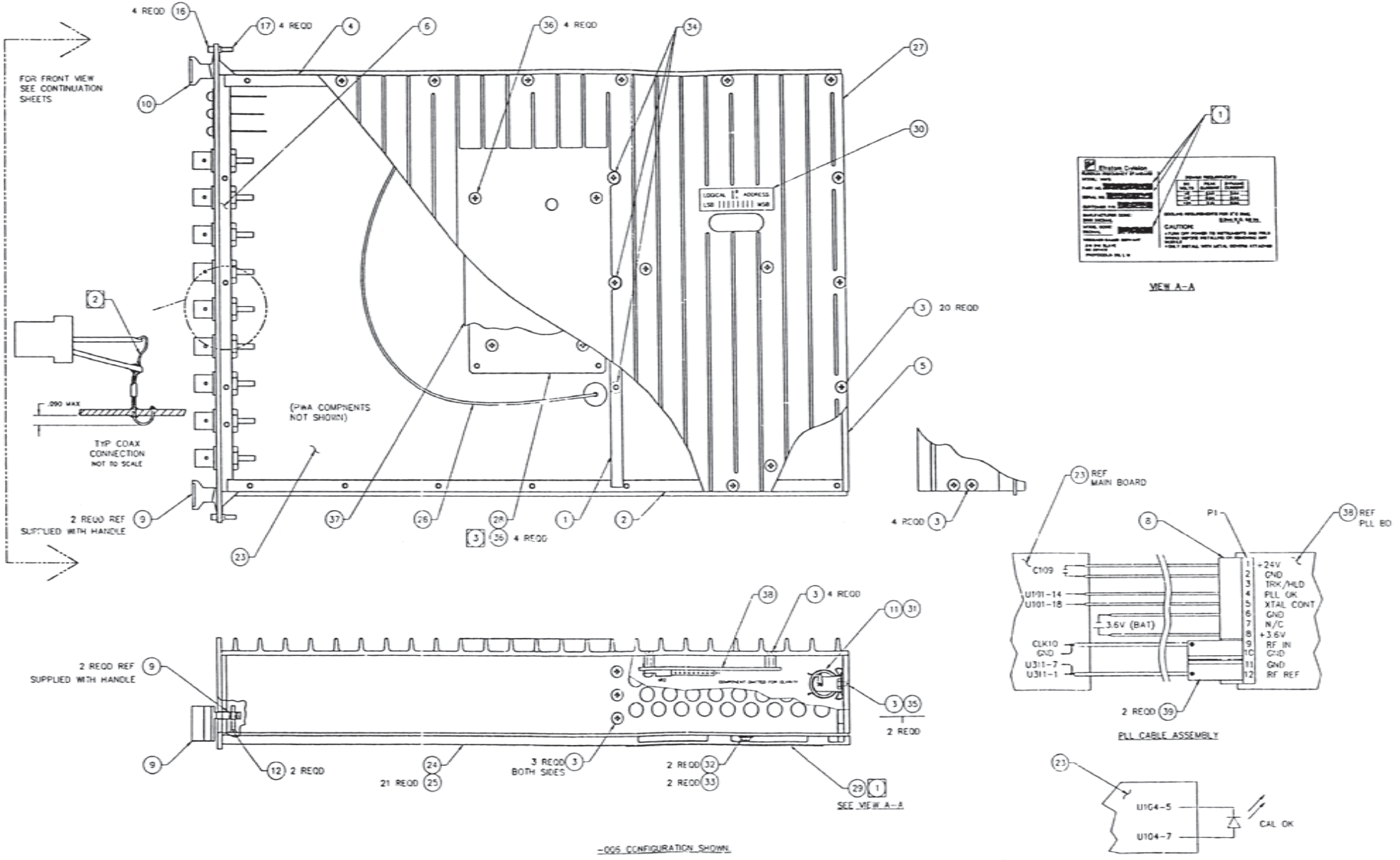


SEE SEPARATE PARTS LIST

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A	A	A	A
SHT 1	SHT 2	SHT 3	SHT 4
REVISION STATUS OF SHEETS			

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-005 CONFIGURATION SHOWN

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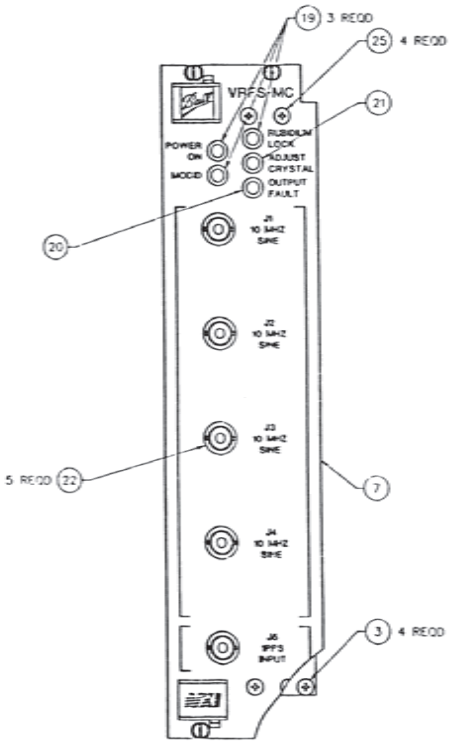
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CONFIGURATION TABULATION

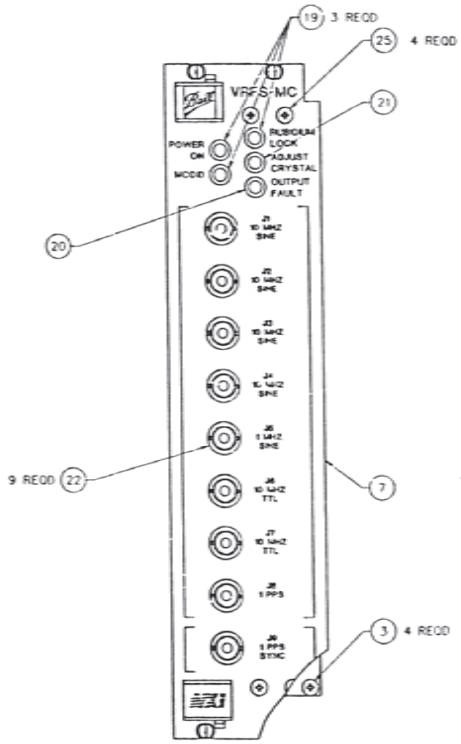
CONFIGURATION		-001	-002	-003	-004	-005	-006	-007
BNC COAX LIST	FROM FRONT PANEL	TO PWA						
	J1	BNC1	BNC1	BNC1	BNC1	BNC1	BNC1	BNC1
	J2	BNC3	BNC2	BNC2	BNC3	BNC2	BNC2	BNC3
	J3	BNC5	BNC3	BNC3	BNC5	BNC3	BNC3	BNC5
	J4	BNC7	BNC4	BNC4	BNC7	BNC4	BNC4	BNC7
	J5	J1-J1GRD	BNC5	BNC5	J1-J1GRD	BNC5	BNC5	NONE
	J6	NONE	BNC6	BNC6	NONE	BNC6	BNC6	NONE
	J7	NONE	BNC7	BNC7	NONE	BNC7	BNC7	NONE
	J8	NONE	BNC8	BNC8	NONE	BNC8	BNC8	NONE
	J9	NONE	J1-J1GRD	J1-J1GRD	NONE	NONE	J1-J1GRD	NONE
IDENT LABEL MARKING	P/N	101790-001	101790-002	101790-003	101790-004	101790-005	101790-006	101790-007
	CODE	3840	3840	3840	3840	3840	3840	3840

LED WIRE LIST

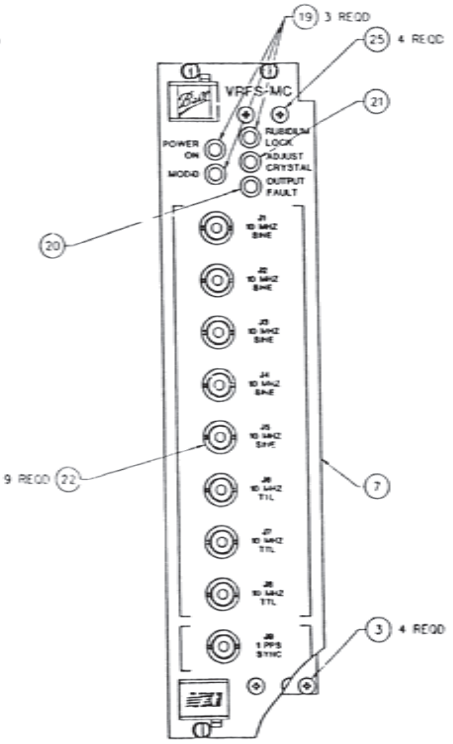
FROM FRONT PANEL		TO PWA	GAUGE	COLOR	
POWER ON	ANODE	E1	24AWG	GRN	
	CATHODE	E2	24AWG	BLK	
OUTPUT FAULT	ANODE	E4	24AWG	RED	
	CATHODE	E3	24AWG	BLK	
ADJ XTAL	ANODE	E6	24AWG	AMB	
	CATHODE	E5	24AWG	BLK	
RB LOCK	ANODE	E8	24AWG	GRN	
	CATHODE	E7	24AWG	BLK	
MODID	ANODE	E10	24AWG	GRN	
	CATHODE	E9	24AWG	BLK	
CAL OK	ANODE	U104-7	24AWG	GRN	} FOR -006 ONLY.
	CATHODE	U104-5	24AWG	BLK	



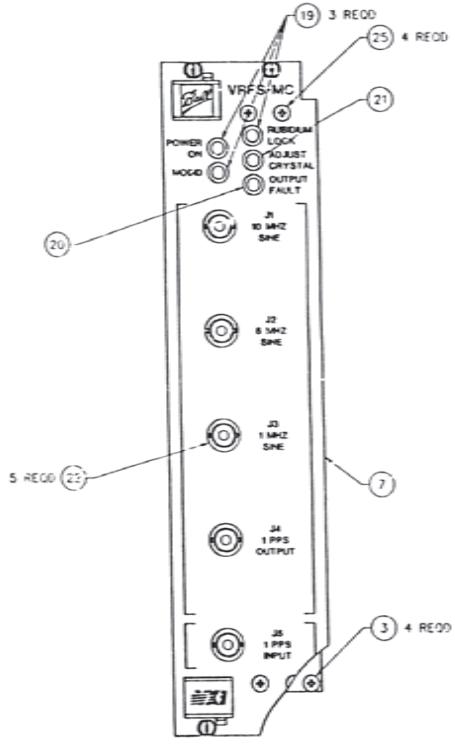
-001 CONFIGURATION



-002 CONFIGURATION

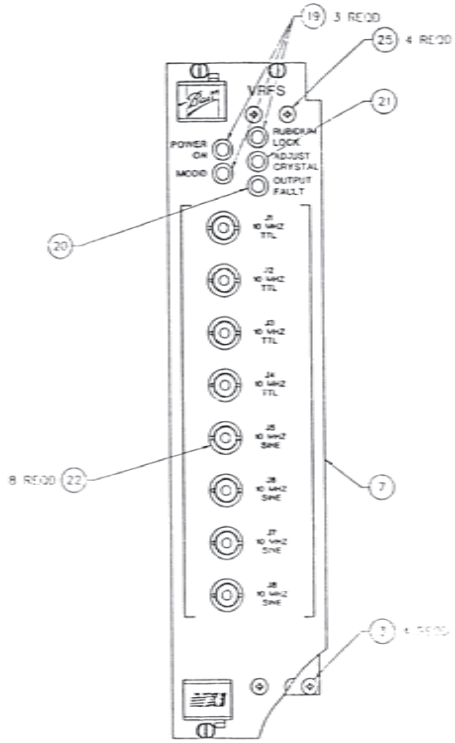


-003 CONFIGURATION

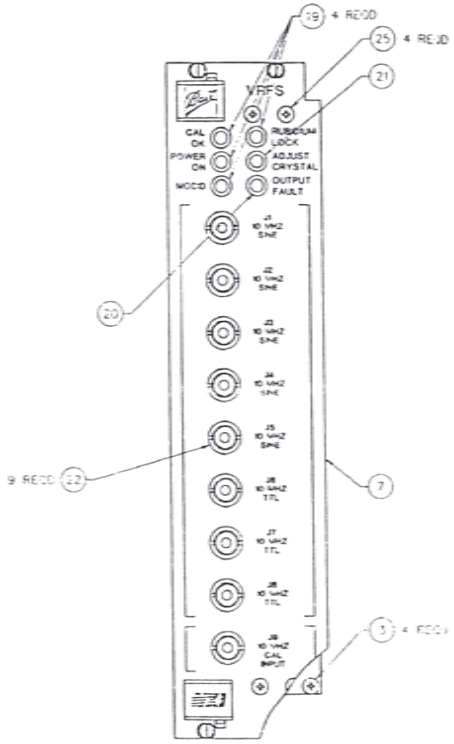


-004 CONFIGURATION

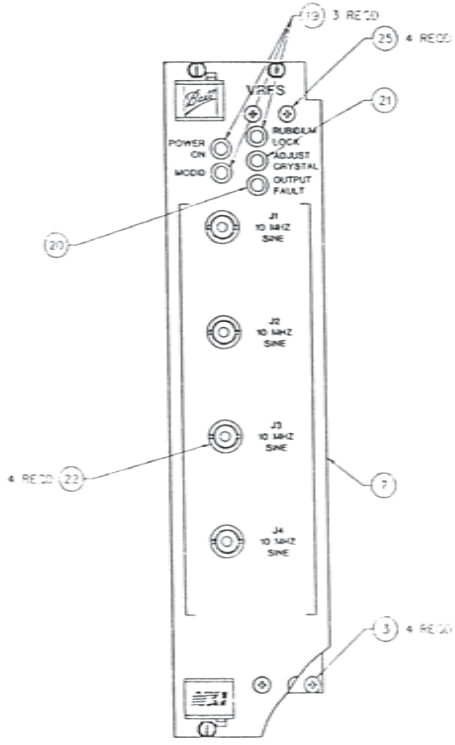
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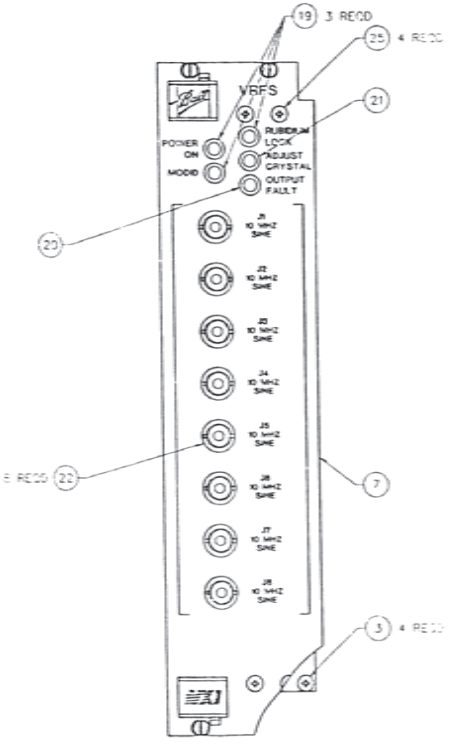
–005 CONFIGURATION



–006 CONFIGURATION



–007 CONFIGURATION



–008 CONFIGURATION

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OCUMENT NO.: PL101790 BALL, EFRATOM DIVISION REVISION DATE: 94/05/10
ITLE: PARTS LIST, FINAL ASSY,VXIBUS-FRS REVISION LETTER: A
HANGE CONTROL NO.: E04342 CAGE CODE 55761 CONTRACT NUMBER: SHEET 1 OF 14
'ARTS LIST OF ASSY NO. 101790-001 INC. DATE: 94/05/11 ORIG. DATE: 92/07/16

FIND NO.	QTY REQ	CAGE CODE	PART OR IDENTIFYING NO.	SPEC. OR MANUFACTURER	NOMENCLATURE OR DESCR.	HCI CODE	REFERENCE DESIGNATOR
1	1		101856-001	101856	DIVIDER,ENCLOSURE,VRFS		
2	1		101854-002	101854	SHIELD,BOTTOM,VRFS		
3	38		MS24693C2	FF-S-92	SCREW,FLAT HEAD,4-40X1/4		
4	1		101854-001	101854	SHIELD,TOP,VRFS		
5	1		101857-001	101857	SHIELD,REAR,VRFS		
6	1		101855-001	101855	SHIELD,FRONT VRFS		
7	1		101863-001	101863	PANEL,FRONT,VRFS		
8					NOT USED		
9	1		103254-001	103254	HANDLE,EXTRACTOR,TOP,SCREENED		
10	1		103253-001	103253	HANDLE,EXTRACTOR,BOTTOM,SCREEN		
11					DELETED		
12	2		AN505C2-10		SCREW,FLAT HEAD,2-56X5/8,82DEG		
13					DELETED		
14					DELETED		
15					DELETED		
16	4		21100-464	SCHROFF	SLEEVE,RETAINING		
17	4		21100-379	SCHROFF	SCREW,COLLAR		
18					DELETED		
19	3		024005-006	024005	LIGHT,LED,PANEL,SNAP-IN,EXT R, GRN,565nm,12mcd@20mA,30mA		
20	1		024005-002	024005	LIGHT,LED,PANEL,SNAP-IN,EXT R, RED,635nm,12mcd@20mA,30mA		
21	1		024005-004	024005	LIGHT,LED,PANEL,SNAP-IN,EXT R, AMB,585nm,7mcd@20mA,20mA		
22	5		KC-79-302-M06	KINGS	CONNECTOR,BNC,ISOLATED		
23	1		101179-002	101179	CIRCUIT CARD ASSY,VRFS		
24	1		101847-001	101847	SHIELD,MACHINING,SOLDER SIDE, VRFS		
25	25		MS24693C4	FF-S-92	SCREW,FLAT HEAD,4-40X3/8		
26	1		101184-001	101184	HARNESS ASSY,VRFS		

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TITLE:	PARTS LIST, FINAL ASSY,VXIBUS-FRS		REVISION LETTER: A
CHANGE CONTROL NO.:	E04342	CAGE CODE 55761 CONTRACT NUMBER:	SHEET 2
PARTS LIST OF ASSY NO.	101790-001	INC. DATE: 94/05/11	ORIG. DATE: 92/07/16

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27	1		101845-001	101845	SHIELD,MACHINING,CMPNT SIDE, VRFS		
28	1		100318-001	100318	FINAL ASSY,FRS,SINE,10MHZ		
29	1		101877-001	101877	LABEL,IDENTIFICATION,VRFS		
30	1		101878-001	101878	LABEL,LOGICAL ADDRESS		
31					DELETED		
32	2		MS35335-62	FF-W-100	WASHER,LOCK,EXT TOOTH,5/16		
33	2		MS51957-14	MS51957	SCREW,PAN HEAD,4-40X5/16		
34	3		MS24693C6		SCREW,FLAT HEAD,4-40X1/2		
35					NOT USED		
36	4		MS18211-31C	MS18211	SCREW,MACH,FLH,SLTD,NYL,4-40X, 3/8,100 DEGREE		
37	1		100294-001	100294	TAPE,THERMAL		
38					NOT USED		
39					NOT USED		
	REF			101166	OUTLINE AND MOUNTING,VRFS		
	REF			101165	SPECIFICATION		
	REF			101162	ACCEPTANCE TEST PROCEDURE		

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TITLE: PARTS LIST, FINAL ASSY,VXIBUS-FRS REVISION LETTER: A
CHANGE CONTROL NO.: E04342 CAGE CODE 55761 CONTRACT NUMBER: SHEET 3
PARTS LIST OF ASSY NO. 101790-002 INC. DATE: 94/05/11 ORIG. DATE: 92/07/16

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1	1		101856-001	101856	DIVIDER,ENCLOSURE,VRFS		
2	1		101854-002	101854	SHIELD,BOTTOM,VRFS		
3	38		MS24693C2	FF-S-92	SCREW,FLAT HEAD,4-40X1/4		
4	1		101854-001	101854	SHIELD,TOP,VRFS		
5	1		101857-001	101857	SHIELD,REAR,VRFS		
6	1		101855-001	101855	SHIELD,FRONT VRFS		
7	1		101863-002	101863	PANEL,FRONT,VRFS		
8					NOT USED		
9	1		103254-001	103254	HANDLE,EXTRACTOR,TOP,SCREENED		
10	1		103253-001	103253	HANDLE,EXTRACTOR,BOTTOM,SCREEN		
11					DELETED		
12	2		AN505C2-10		SCREW,FLAT HEAD,2-56X5/8,82DEG		
13					DELETED		
14					DELETED		
15					DELETED		
16	4		21100-464	SCHROFF	SLEEVE,RETAINING		
17	4		21100-379	SCHROFF	SCREW,COLLAR		
18					DELETED		
19	3		024005-006	024005	LIGHT,LED,PANEL,SNAP-IN,EXT R, GRN,565nm,12mcd@20mA,30mA		
20	1		024005-002	024005	LIGHT,LED,PANEL,SNAP-IN,EXT R, RED,635nm,12mcd@20mA,30mA		
21	1		024005-004	024005	LIGHT,LED,PANEL,SNAP-IN,EXT R, AMB,585nm,7mcd@20mA,20mA		
22	9		KC-79-302-M06	KINGS	CONNECTOR,BNC,ISOLATED		
23	1		101179-001	101179	CIRCUIT CARD ASSY,VRFS		
24	1		101847-001	101847	SHIELD,MACHINING,SOLDER SIDE, VRFS		
25	25		MS24693C4	FF-S-92	SCREW,FLAT HEAD,4-40X3/8		
26	1		101184-001	101184	HARNESS ASSY,VRFS		

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DOCUMENT NO.:	PL101790	BALL, EFRATOM DIVISION	REVISION DATE: 94/05/10
TITLE: PARTS LIST, FINAL ASSY,VXIBUS-FRS			REVISION LETTER: A
CHANGE CONTROL NO.:	E04342	CAGE CODE 55761 CONTRACT NUMBER:	SHEET 4
PARTS LIST OF ASSY NO. 101790-002		INC. DATE: 94/05/11	ORIG. DATE: 92/07/16

FIND NO.	QTY REQ	CAGE CODE	PART OR IDENTIFYING NO.	SPEC. OR MANUFACTURER	NOMENCLATURE OR DESCR.	HCI CODE	REFERENCE DESIGNATOR
27	1		101845-001	101845	SHIELD,MACHINING,CMPNT SIDE, VRFS		
28	1		100318-001	100318	FINAL ASSY,FRS,SINE,10MHZ		
29	1		101877-001	101877	LABEL,IDENTIFICATION,VRFS		
30	1		101878-001	101878	LABEL,LOGICAL ADDRESS		
31					DELETED		
32	2		MS35335-62	FF-W-100	WASHER,LOCK,EXT TOOTH,5/16		
33	2		MS51957-14	MS51957	SCREW,PAN HEAD,4-40X5/16		
34	3		MS24693C6		SCREW,FLAT HEAD,4-40X1/2		
35					NOT USED		
36	4		MS18211-31C	MS18211	SCREW,MACH,FLH,SLTD,NYL,4-40X, 3/8,100 DEGREE		
37	1		100294-001	100294	TAPE,THERMAL		
38					NOT USED		
39					NOT USED		
REF				101166	OUTLINE AND MOUNTING,VRFS		
REF				101165	SPECIFICATION		
REF				101162	ACCEPTANCE TEST PROCEDURE		

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DOCUMENT NO.: PL101790	BALL, EFRATOM DIVISION	REVISION DATE:	94/05/10
TITLE: PARTS LIST, FINAL ASSY,VXIBUS-FRS		REVISION LETTER:	A
CHANGE CONTROL NO.: E04342	CAGE CODE 55761 CONTRACT NUMBER:	SHEET	5
PARTS LIST OF ASSY NO. 101790-003	INC. DATE: 94/05/11	ORIG. DATE:	92/07/16

FIND NO.	QTY REQ	CAGE CODE	PART OR IDENTIFYING NO.	SPEC. OR MANUFACTURER	NOMENCLATURE OR DESCR.	HCI CODE	REFERENCE DESIGNATOR
1	1		101856-001	101856	DIVIDER,ENCLOSURE,VRFS		
2	1		101854-002	101854	SHIELD,BOTTOM,VRFS		
3	38		MS24693C2	FF-S-92	SCREW,FLAT HEAD,4-40X1/4		
4	1		101854-001	101854	SHIELD,TOP,VRFS		
5	1		101857-001	101857	SHIELD,REAR,VRFS		
6	1		101855-001	101855	SHIELD,FRONT VRFS		
7	1		101863-003	101863	PANEL,FRONT,VRFS		
8					NOT USED		
9	1		103254-001	103254	HANDLE,EXTRACTOR,TOP,SCREENED		
10	1		103253-001	103253	HANDLE,EXTRACTOR,BOTTOM,SCREEN		
11					DELETED		
12	2		AN505C2-10		SCREW,FLAT HEAD,2-56X5/8,82DEG		
13					DELETED		
14					DELETED		
15					DELETED		
16	4		21100-464	SCHROFF	SLEEVE,RETAINING		
17	4		21100-379	SCHROFF	SCREW,COLLAR		
18					DELETED		
19	3		024005-006	024005	LIGHT,LED,PANEL,SNAP-IN,EXT R, GRN,565nm,12mcd@20mA,30mA		
20	1		024005-002	024005	LIGHT,LED,PANEL,SNAP-IN,EXT R, RED,635nm,12mcd@20mA,30mA		
21	1		024005-004	024005	LIGHT,LED,PANEL,SNAP-IN,EXT R, AMB,585nm,7mcd@20mA,20mA		
22	7		KC-79-302-M06	KINGS	CONNECTOR,BNC,ISOLATED		
23	1		101179-003	101179	CIRCUIT CARD ASSY,VRFS		
24	1		101847-001	101847	SHIELD,MACHINING,SOLDER SIDE, VRFS		
25	25		MS24693C4	FF-S-92	SCREW,FLAT HEAD,4-40X3/8		
26	1		101184-001	101184	HARNESS ASSY,VRFS		

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DOCUMENT NO.: PL101790 BALL, EFRATOM DIVISION REVISION DATE: 94/05/10
TITLE: PARTS LIST, FINAL ASSY,VXIBUS-FRS REVISION LETTER: A
CHANGE CONTROL NO.: E04342 CAGE CODE 55761 CONTRACT NUMBER: SHEET 6
PARTS LIST OF ASSY NO. 101790-003 INC. DATE: 94/05/11 ORIG. DATE: 92/07/16

FIND NO.	QTY REQ	CAGE CODE	PART OR IDENTIFYING NO.	SPEC. OR MANUFACTURER	NOMENCLATURE OR DESCR.	HCI CODE	REFERENCE DESIGNATOR
27	1		101845-001	101845	SHIELD,MACHINING,CMPNT SIDE, VRFS		
28	1		100318-001	100318	FINAL ASSY,FRS,SINE,10MHZ		
29	1		101877-001	101877	LABEL,IDENTIFICATION,VRFS		
30	1		101878-001	101878	LABEL,LOGICAL ADDRESS		
31					DELETED		
32	2		MS35335-62	FF-W-100	WASHER,LOCK,EXT TOOTH,5/16		
33	2		MS51957-14	MS51957	SCREW,PAN HEAD,4-40X5/16		
34	3		MS24693C6		SCREW,FLAT HEAD,4-40X1/2		
35					NOT USED		
36	4		MS18211-31C	MS18211	SCREW,MACH,FLH,SLTD,NYL,4-40X, 3/8,100 DEGREE		
37	1		100294-001	100294	TAPE,THERMAL		
38					NOT USED		
39					NOT USED		
REF				101166	OUTLINE AND MOUNTING,VRFS		
REF				101165	SPECIFICATION		
REF				101162	ACCEPTANCE TEST PROCEDURE		

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DOCUMENT NO.: PL101790 BALL, EFRATOM DIVISION REVISION DATE: 94/05/10
TITLE: PARTS LIST, FINAL ASSY,VXIBUS-FRS REVISION LETTER: A
CHANGE CONTROL NO.: E04342 CAGE CODE 55761 CONTRACT NUMBER: SHEET 7
PARTS LIST OF ASSY NO. 101790-004 INC. DATE: 94/05/11 ORIG. DATE: 92/07/16

FIND NO.	QTY REQ	CAGE CODE	PART OR IDENTIFYING NO.	SPEC. OR MANUFACTURER	NOMENCLATURE OR DESCR.	HCI CODE	REFERENCE DESIGNATOR
1	1		101856-001	101856	DIVIDER,ENCLOSURE,VRFS		
2	1		101854-002	101854	SHIELD,BOTTOM,VRFS		
3	38		MS24693C2	FF-S-92	SCREW,FLAT HEAD,4-40X1/4		
4	1		101854-001	101854	SHIELD,TOP,VRFS		
5	1		101857-001	101857	SHIELD,REAR,VRFS		
6	1		101855-001	101855	SHIELD,FRONT VRFS		
7	1		101863-004	101863	PANEL,FRONT,VRFS		
8					NOT USED		
9	1		103254-001	103254	HANDLE,EXTRACTOR,TOP,SCREENED		
10	1		103253-001	103253	HANDLE,EXTRACTOR,BOTTOM,SCREEN		
11					NOT USED		
12	2		AN505C2-10		SCREW,FLAT HEAD,2-56X5/8,82DEG		
13					NOT USED		
14					DELETED		
15					DELETED		
16	4		21100-464	SCHROFF	SLEEVE,RETAINING		
17	4		21100-379	SCHROFF	SCREW,COLLAR		
18					DELETED		
19	3		024005-006	024005	LIGHT,LED,PANEL,SNAP-IN,EXT R, GRN,565nm,12mcd@20mA,30mA		
20	1		024005-002	024005	LIGHT,LED,PANEL,SNAP-IN,EXT R, RED,635nm,12mcd@20mA,30mA		
21	1		024005-004	024005	LIGHT,LED,PANEL,SNAP-IN,EXT R, AMB,585nm,7mcd@20mA,20mA		
22	9		KC-79-302-M06	KINGS	CONNECTOR,BNC,ISOLATED		
23	1		101179-004	101179	CIRCUIT CARD ASSY,VRFS		
24	1		101847-001	101847	SHIELD,MACHINING,SOLDER SIDE, VRFS		
25	25		MS24693C4	FF-S-92	SCREW,FLAT HEAD,4-40X3/8		
26	1		101184-001	101184	HARNESS ASSY,VRFS		

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DOCUMENT NO.: PL101790 BALL, EFRATOM DIVISION REVISION DATE: 94/05/10
TITLE: PARTS LIST, FINAL ASSY,VXIBUS-FRS REVISION LETTER: A
CHANGE CONTROL NO.: E04342 CAGE CODE 55761 CONTRACT NUMBER: SHEET 8
PARTS LIST OF ASSY NO. 101790-004 INC. DATE: 94/05/11 ORIG. DATE: 92/07/16

FIND NO.	QTY REQ	CAGE CODE	PART OR IDENTIFYING NO.	SPEC. OR MANUFACTURER	NOMENCLATURE OR DESCR.	HCI CODE	REFERENCE DESIGNATOR
27	1		101845-001	101845	SHIELD,MACHINING,CMPNT SIDE, VRFS		
28	1		100318-001	100318	FINAL ASSY,FRS,SINE,10MHZ		
29	1		101877-001	101877	LABEL,IDENTIFICATION,VRFS		
30	1		101878-001	101878	LABEL,LOGICAL ADDRESS		
31					NOT USED		
32	2		MS35335-62	FF-W-100	WASHER,LOCK,EXT TOOTH,5/16		
33	2		MS51957-14	MS51957	SCREW,PAN HEAD,4-40X5/16		
34	3		MS24693C6		SCREW,FLAT HEAD,4-40X1/2		
35					NOT USED		
36	4		MS18211-31C	MS18211	SCREW,MACH,FLH,SLTD,NYL,4-40X, 3/8,100 DEGREE		
37	1		100294-001	100294	TAPE,THERMAL		
38					NOT USED		
39					NOT USED		
	REF			101166	OUTLINE AND MOUNTING,VRFS		
	REF			101165	SPECIFICATION		
	REF			101162	ACCEPTANCE TEST PROCEDURE		

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DOCUMENT NO.: PL101790 BALL, EFRATOM DIVISION REVISION DATE: 94/05/10
TITLE: PARTS LIST, FINAL ASSY,VXIBUS-FRS REVISION LETTER: A
CHANGE CONTROL NO.: E04342 CAGE CODE 55761 CONTRACT NUMBER: SHEET 9
PARTS LIST OF ASSY NO. 101790-005 INC. DATE: 94/05/11 ORIG. DATE: 92/07/16

FIND NO.	QTY REQ	CAGE CODE	PART OR IDENTIFYING NO.	SPEC. OR MANUFACTURER	NOMENCLATURE OR DESCR.	HCI CODE	REFERENCE DESIGNATOR
1	1		101856-001	101856	DIVIDER,ENCLOSURE,VRFS		
2	1		101854-002	101854	SHIELD,BOTTOM,VRFS		
3	38		MS24693C2	FF-S-92	SCREW,FLAT HEAD,4-40X1/4		
4	1		101854-001	101854	SHIELD,TOP,VRFS		
5	1		101857-001	101857	SHIELD,REAR,VRFS		
6	1		101855-001	101855	SHIELD,FRONT VRFS		
7	1		101863-005	101863	PANEL,FRONT,VRFS		
8					NOT USED		
9	1		103254-001	103254	HANDLE,EXTRACTOR,TOP,SCREENED		
10	1		103253-001	103253	HANDLE,EXTRACTOR,BOTTOM,SCREEN		
11					NOT USED		
12	2		AN505C2-10		SCREW,FLAT HEAD,2-56X5/8,82DEG		
13					NOT USED		
14					NOT USED		
15					NOT USED		
16	4		21100-464	SCHROFF	SLEEVE,RETAINING		
17	4		21100-379	SCHROFF	SCREW,COLLAR		
18					DELETED		
19	3		024005-006	024005	LIGHT,LED,PANEL,SNAP-IN,EXT R, GRN,565nm,12mcd@20mA,30mA		
20	1		024005-002	024005	LIGHT,LED,PANEL,SNAP-IN,EXT R, RED,635nm,12mcd@20mA,30mA		
21	1		024005-004	024005	LIGHT,LED,PANEL,SNAP-IN,EXT R, AMB,585nm,7mcd@20mA,20mA		
22	8		KC-79-302-M06	KINGS	CONNECTOR,BNC,ISOLATED		
23	1		101179-005	101179	CIRCUIT CARD ASSY,VRFS		
24	1		101847-001	101847	SHIELD,MACHINING,SOLDER SIDE, VRFS		
25	25		MS24693C4	FF-S-92	SCREW,FLAT HEAD,4-40X3/8		
26	1		101184-001	101184	HARNESS ASSY,VRFS		

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DOCUMENT NO.: PL101790	BALL, EFRATOM DIVISION		REVISION DATE: 94/05/10
TITLE: PARTS LIST, FINAL ASSY,VXIBUS-FRS			REVISION LETTER: A
CHANGE CONTROL NO.: E04342	CAGE CODE 55761	CONTRACT NUMBER:	SHEET 10
PARTS LIST OF ASSY NO. 101790-005	INC. DATE: 94/05/11		ORIG. DATE: 92/07/16

FIND NO.	QTY REQ	CAGE CODE	PART OR IDENTIFYING NO.	SPEC. OR MANUFACTURER	NOMENCLATURE OR DESCR.	HCI CODE	REFERENCE DESIGNATOR
27	1		101845-001	101845	SHIELD,MACHINING,CMPNT SIDE, VRFS		
28	1		100318-001	100318	FINAL ASSY,FRS,SINE,10MHZ		
29	1		101877-001	101877	LABEL,IDENTIFICATION,VRFS		
30	1		101878-001	101878	LABEL,LOGICAL ADDRESS		
31					NOT USED		
32	2		MS35335-62	FF-W-100	WASHER,LOCK,EXT TOOTH,5/16		
33	2		MS51957-14	MS51957	SCREW,PAN HEAD,4-40X5/16		
34	3		MS24693C6		SCREW,FLAT HEAD,4-40X1/2		
35					NOT USED		
36	4		MS18211-31C	MS18211	SCREW,MACH,FLH,SLTD,NYL,4-40X, 3/8,100 DEGREE		
37	1		100294-001	100294	TAPE,THERMAL		
38					NOT USED		
39					NOT USED		
REF				101166	OUTLINE AND MOUNTING,VRFS		
REF				101165	SPECIFICATION		
REF				101162	ACCEPTANCE TEST PROCEDURE		

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DOCUMENT NO.: PL101790 BALL, EFRATOM DIVISION REVISION DATE: 94/05/10
TITLE: PARTS LIST, FINAL ASSY,VXIBUS,FRS-102 REVISION LETTER: A
CHANGE CONTROL NO.: E04342 CAGE CODE 55761 CONTRACT NUMBER: SHEET 11
PARTS LIST OF ASSY NO. 101790-006 INC. DATE: 94/05/11 ORIG. DATE: 92/07/16

FIND NO.	QTY REQ	CAGE CODE	PART OR IDENTIFYING NO.	SPEC. OR MANUFACTURER	NOMENCLATURE OR DESCR.	HCI CODE	REFERENCE DESIGNATOR
1	1		101856-001	101856	DIVIDER,ENCLOSURE,VRFS		
2	1		101854-002	101854	SHIELD,BOTTOM,VRFS		
3	40		MS24693C2	FF-S-92	SCREW,FLAT HEAD,4-40X1/4		
4	1		101854-001	101854	SHIELD,TOP,VRFS		
5	1		101857-001	101857	SHIELD,REAR,VRFS		
6	1		103698-001	103698	SHIELD,FRONT,VRFS-102		
7	1		103694-001	103694	PANEL,FRONT,VRFS-102		
8	1		060014-008	060014	CABLE ASSY,.100 IN IDC,8 PIN		
9	1		103254-001	103254	HANDLE,EXTRACTOR,TOP,SCREENED		
10	1		103253-001	103253	HANDLE,EXTRACTOR,BOTTOM,SCREEN		
11	1		039000-001	039000	BATTERY,LITHIUM,3.6V,1.9AH,AA, RADIAL LEAD		
12	2		AN505C2-10		SCREW,FLAT HEAD,2-56X5/8,82DEG		
13	2		060001-015	060001	CABLE ASSY,COAX,SH INTEGD SKT, 50 OHM 15 IN LONG		
14					NOT USED		
15					NOT USED		
16	4		21100-464	SCHROFF	SLEEVE,RETAINING		
17	4		21100-379	SCHROFF	SCREW,COLLAR		
18					NOT USED		
19	4		024005-006	024005	LIGHT,LED,PANEL,SNAP-IN,EXT R, GRN,565nm,12mcd@20mA,30mA		
20	1		024005-002	024005	LIGHT,LED,PANEL,SNAP-IN,EXT R, RED,635nm,12mcd@20mA,30mA		
21	1		024005-004	024005	LIGHT,LED,PANEL,SNAP-IN,EXT R, AMB,585nm,7mcd@20mA,20mA		
22	9		KC-79-302-M06	KINGS	CONNECTOR,BNC,ISOLATED		
23	1		103696-001	103696	CIRCUIT CARD ASSY,VRFS-102		
24	1		101847-001	101847	SHIELD,MACHINING,SOLDER SIDE, VRFS		

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DOCUMENT NO.: PL101790	BALL, EFRATOM DIVISION	REVISION DATE:	94/05/10
TITLE: PARTS LIST, FINAL ASSY,VXIBUS,FRS-102		REVISION LETTER:	A
CHANGE CONTROL NO.: E04342	CAGE CODE 55761 CONTRACT NUMBER:	SHEET	12
PARTS LIST OF ASSY NO. 101790-006	INC. DATE: 94/05/11	ORIG. DATE:	92/07/16

FIND NO.	QTY REQ	CAGE CODE	PART OR IDENTIFYING NO.	SPEC. OR MANUFACTURER	NOMENCLATURE OR DESCR.	HCI CODE	REFERENCE DESIGNATOR
25	25		MS24693C4	FF-S-92	SCREW,FLAT HEAD,4-40X3/8		
26	1		101184-001	101184	HARNESS ASSY,VRFS		
27	1		101845-001	101845	SHIELD,MACHINING,CMPNT SIDE, VRFS		
28	1		100318-001	100318	FINAL ASSY,FRS,SINE,10MHZ		
29	1		101877-002	101877	LABEL,IDENTIFICATION,VRFS-102		
30	1		101878-001	101878	LABEL,LOGICAL ADDRESS		
31	1		025040-006	025040	HOLDER,BATTERY,AA,INSUL,CRES		
32	2		MS35335-62	FF-W-100	WASHER,LOCK,EXT TOOTH,5/16		
33	2		MS51957-14	MS51957	SCREW,PAN HEAD,4-40X5/16		
34	3		MS24693C6		SCREW,FLAT HEAD,4-40X1/2		
35	2		NAS671C4	FF-N-836	NUT,HEX #4		
36	8		MS18211-31C	MS18211	SCREW,MACH,FLH,SLTD,NYL,4-40X, 3/8,100 DEGREE		
37	1		100294-001	100294	TAPE,THERMAL		
38	1		101725-003	101725	CIRCUIT CARD ASSY,TRK/HOLD, PLL		
39	2		060001-015	060001	CABLE ASSY,COAX,SH INTEGD SKT, 50 OHM,15 IN LONG		
REF				101166	OUTLINE AND MOUNTING,VRFS		
REF				101165	SPECIFICATION		
REF				101162	ACCEPTANCE TEST PROCEDURE		

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DOCUMENT NO.: PL101790 BALL, EFRATOM DIVISION REVISION DATE: 94/05/10
TITLE: PARTS LIST, FINAL ASSY,VXIBUS,FRS-103 REVISION LETTER: A
CHANGE CONTROL NO.: E04342 CAGE CODE 55761 CONTRACT NUMBER: SHEET 13
PARTS LIST OF ASSY NO. 101790-007 INC. DATE: 94/05/11 ORIG. DATE: 92/07/16

FIND NO.	QTY REQ	CAGE CODE	PART OR IDENTIFYING NO.	SPEC. OR MANUFACTURER	NOMENCLATURE OR DESCR.	HCI CODE	REFERENCE DESIGNATOR
1	1		101856-001	101856	DIVIDER,ENCLOSURE,VRFS		
2	1		101854-002	101854	SHIELD,BOTTOM,VRFS		
3	34		MS24693C2	FF-S-92	SCREW,FLAT HEAD,4-40X1/4		
4	1		101854-001	101854	SHIELD,TOP,VRFS		
5	1		101857-001	101857	SHIELD,REAR,VRFS		
6	1		101855-001	101855	SHIELD,FRONT VRFS		
7	1		101863-006	101863	PANEL,FRONT,VRFS		
8					NOT USED		
9	1		103254-001	103254	HANDLE,EXTRACTOR,TOP,SCREENED		
10	1		103253-001	103253	HANDLE,EXTRACTOR,BOTTOM,SCREEN		
11					NOT USEL		
12	2		AN505C2-10		SCREW,FLAT HEAD,2-56X5/8,82DEG		
13					NOT USED		
14					NOT USED		
15					NOT USED		
16	4		21100-464	SCHROFF	SLEEVE,RETAINING		
17	4		21100-379	SCHROFF	SCREW,COLLAR		
18					NOT USED		
19	3		024005-006	024005	LIGHT,LED,PANEL,SNAP-IN,EXT R, GRN,565nm,12mcd@20mA,30mA		
20	1		024005-002	024005	LIGHT,LED,PANEL,SNAP-IN,EXT R, RED,635nm,12mcd@20mA,30mA		
21	1		024005-004	024005	LIGHT,LED,PANEL,SNAP-IN,EXT R, AMB,585nm,7mcd@20mA,20mA		
22	4		KC-79-302-M06	KINGS	CONNECTOR,BNC,ISOLATED		
23	1		101179-002	101179	CIRCUIT CARD ASSY,VRFS		
24	1		101847-001	101847	SHIELD,MACHINING,SOLDER SIDE, VRFS		
25	25		MS24693C4	FF-S-92	SCREW,FLAT HEAD,4-40X3/8		
26	1		101184-001	101184	HARNESS ASSY,VRFS		

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DOCUMENT NO.: PL101790 BALL, EFRATOM DIVISION REVISION DATE: 94/05/10
TITLE: PARTS LIST, FINAL ASSY,VXIBUS,FRS-103 REVISION LETTER: A
CHANGE CONTROL NO.: E04342 CAGE CODE 55761 CONTRACT NUMBER: SHEET 14
PARTS LIST OF ASSY NO. 101790-007 INC. DATE: 94/05/11 ORIG. DATE: 92/07/16

FIND NO.	QTY REQ	CAGE CODE	PART OR IDENTIFYING NO.	SPEC. OR MANUFACTURER	NOMENCLATURE OR DESCR.	HCI CODE	REFERENCE DESIGNATOR
27	1		101845-001	101845	SHIELD,MACHINING,CMPNT SIDE, VRFS		
28	1		100318-001	100318	FINAL ASSY,FRS,SINE,10MHZ		
29	1		101877-003	101877	LABEL,IDENTIFICATION,VRFS-103		
30	1		101878-001	101878	LABEL,LOGICAL ADDRESS		
31					NOT USED		
32	2		MS35335-62	FF-W-100	WASHER,LOCK,EXT TOOTH,5/16		
33	2		MS51957-14	MS51957	SCREW,PAN HEAD,4-40X5/16		
34	3		MS24693C6		SCREW,FLAT HEAD,4-40X1/2		
35					NOT USED		
36	8		MS18211-31C	MS18211	SCREW,MACH,FLH,SLTD,NYL,4-40X, 3/8,100 DEGREE		
37	1		100294-001	100294	TAPE,THERMAL		
38					NOT USED		
39					NOT USED		
	REF			101166	OUTLINE AND MOUNTING,VRFS		
	REF			101165	SPECIFICATION		
	REF			101162	ACCEPTANCE TEST PROCEDURE		

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NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTORS ARE 1/4W, 1%, VALUES ARE IN OHMS.
2. CAPACITORS ARE 5%, 50V, VALUES ARE IN MICROFARADS.

POWER CHART

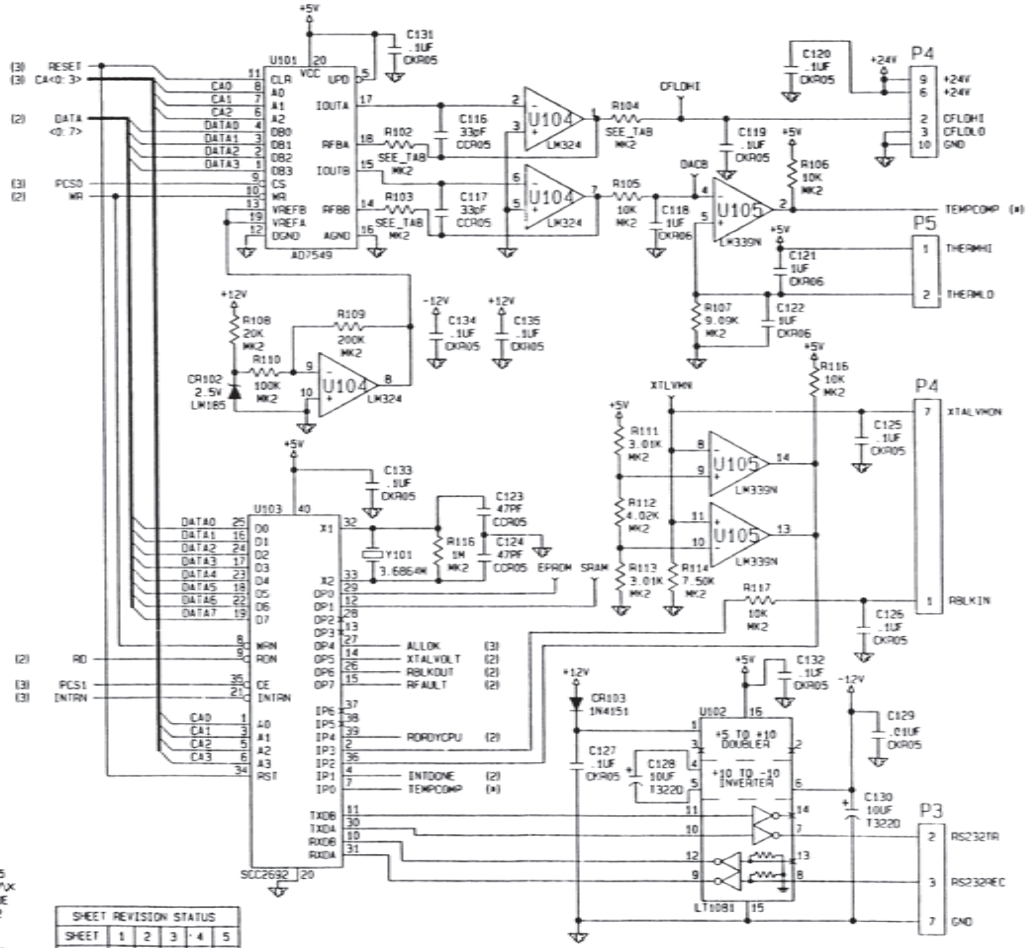
	+5V	+5VREG	+12V	-12V	GND	BYPASS CAP .1UF
U101	20				12, 16	C131
U102	16				15	C132
U103	40				20	C133
U104			4	11		C134, C135
U105			3		11	
U201	20				10	
U202	20				10	C201
U203	20				10	C202
U204	40				20	C203
U205	20				10	C204
U206	20				10	C205
U207	24				12	
U208	24				12	C206
U209	16				8	C207, C208
U210	20				10	C209
U211	18, 52				1, 35	C210, C211
U212	20				10	C212, C213
U301	20				10	C312
U302	20				10	C313
U303	28				14	C314
U304	28				14	C315
U305	9, 43				26, 50	C319, C320
U306	20				10	C321
U307	20				10	C322
U308	24				12	C316
U309	20				10	C323
U310	18				9	C324
U311	14				7	C325
U312	40				20	C326
U314		1			4, 5, 6	C303
U313		24			12	
U315	1				4, 5, 6	C304
U315	14				7	C327
U317			3		11	C328
U318	14				7	C329
U401			3		11	
U501			3		11	

TABULATION

REF DES	SINE 10MHZ	SINE 5MHZ	SINE 1MHZ	SINE 100KHZ	TTL	1PPS +12V	1PPS +5V
C4	47PF	100PF	1000PF	.01UF	NOT USED	NOT USED	NOT USED
C5	240PF NOM	240PF NOM	240PF NOM	100PF NOM	NOT USED	NOT USED	NOT USED
C6	1000PF NOM	3300PF NOM	5600PF NOM	.082UF NOM	NOT USED	NOT USED	NOT USED
C7	1000PF	1000PF	.01UF	.1UF	NOT USED	NOT USED	NOT USED
C8	INSTALL	INSTALL	INSTALL	INSTALL	NOT USED	NOT USED	NOT USED
C9	INSTALL	INSTALL	INSTALL	INSTALL	INSTALL	NOT USED	NOT USED
C10	3.3PF	3.3PF	3.3PF	3.3PF	NOT USED	NOT USED	NOT USED
C11	.1UF	.1UF	.1UF	.1UF	JUMPER	NOT USED	NOT USED
C12	6800PF	6800PF	6800PF	6800PF	6800PF	JUMPER	JUMPER
C13	.1UF	.1UF	.1UF	.1UF	.1UF	10UF	10UF
C15	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	INSTALL	INSTALL
C16	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	INSTALL	INSTALL
C17	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	INSTALL	INSTALL
CR2	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	INSTALL	INSTALL
CR3	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	INSTALL	INSTALL
JP2	NOT USED	NOT USED	NOT USED	NOT USED	JUMPER	NOT USED	NOT USED
L2	.47UH	1.2UH	6.8UH	56UH	NOT USED	NOT USED	NOT USED
Q1	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	INSTALL	INSTALL
Q2	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	INSTALL	INSTALL
R1	909 OHM	909 OHM	909 OHM	909 OHM	909 OHM	NOT USED	NOT USED
R2	10K OHM	10K OHM	10K OHM	10K OHM	27.4K OHM	NOT USED	NOT USED
R3	INSTALL	INSTALL	INSTALL	INSTALL	INSTALL	NOT USED	NOT USED
R4	INSTALL	INSTALL	INSTALL	INSTALL	INSTALL	NOT USED	NOT USED
R5	INSTALL	INSTALL	INSTALL	INSTALL	INSTALL	NOT USED	NOT USED
R6	4.64K NOM	4.64K NOM	4.64K NOM	4.64K NOM	NOT USED	NOT USED	NOT USED
R7	INSTALL	INSTALL	INSTALL	INSTALL	INSTALL	NOT USED	NOT USED
R8	INSTALL	INSTALL	INSTALL	INSTALL	INSTALL	NOT USED	NOT USED
R9	56.2 OHM	56.2 OHM	56.2 OHM	56.2 OHM	90.9 OHM	NOT USED	NOT USED
R10	1K OHM	1K OHM	1K OHM	1K OHM	6.19K OHM	133 OHM	133 OHM
R11	475K OHM	475K OHM	475K OHM	475K OHM	475K OHM	1M OHM	1M OHM
R12	NOT USED	NOT USED	NOT USED	NOT USED	182 OHM	1K OHM	1K OHM
R13	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	INSTALL	INSTALL
R14	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	INSTALL	INSTALL
R15	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	INSTALL	INSTALL
R16	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	INSTALL	INSTALL
R17	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	INSTALL	NOT USED
U1	INSTALL	INSTALL	INSTALL	INSTALL	INSTALL	NOT USED	NOT USED

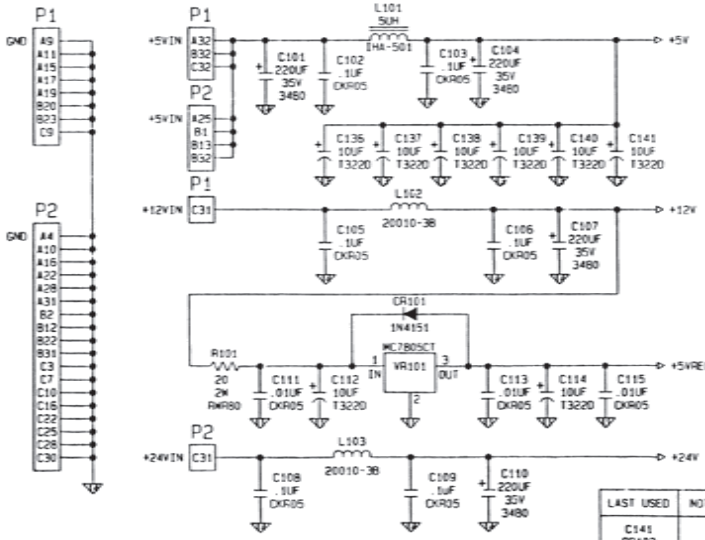
TABULATION

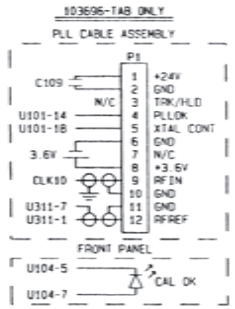
	R102	R103	R104	NOT INSTALLED	JUMPER
101179-XXX	47.5	47.5	2.21K		
103696-XXX	JUMPER	332	JUMPER	U101, U104, U307, U309, U310, U311, R105, C109, C116, C117	U316-4 TO U316-7



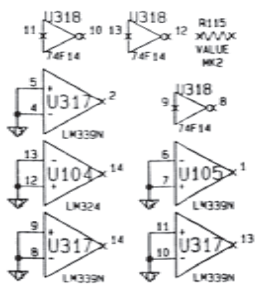
SHEET REVISION STATUS

SHEET	1	2	3	4	5
REV	A	A	A	A	A





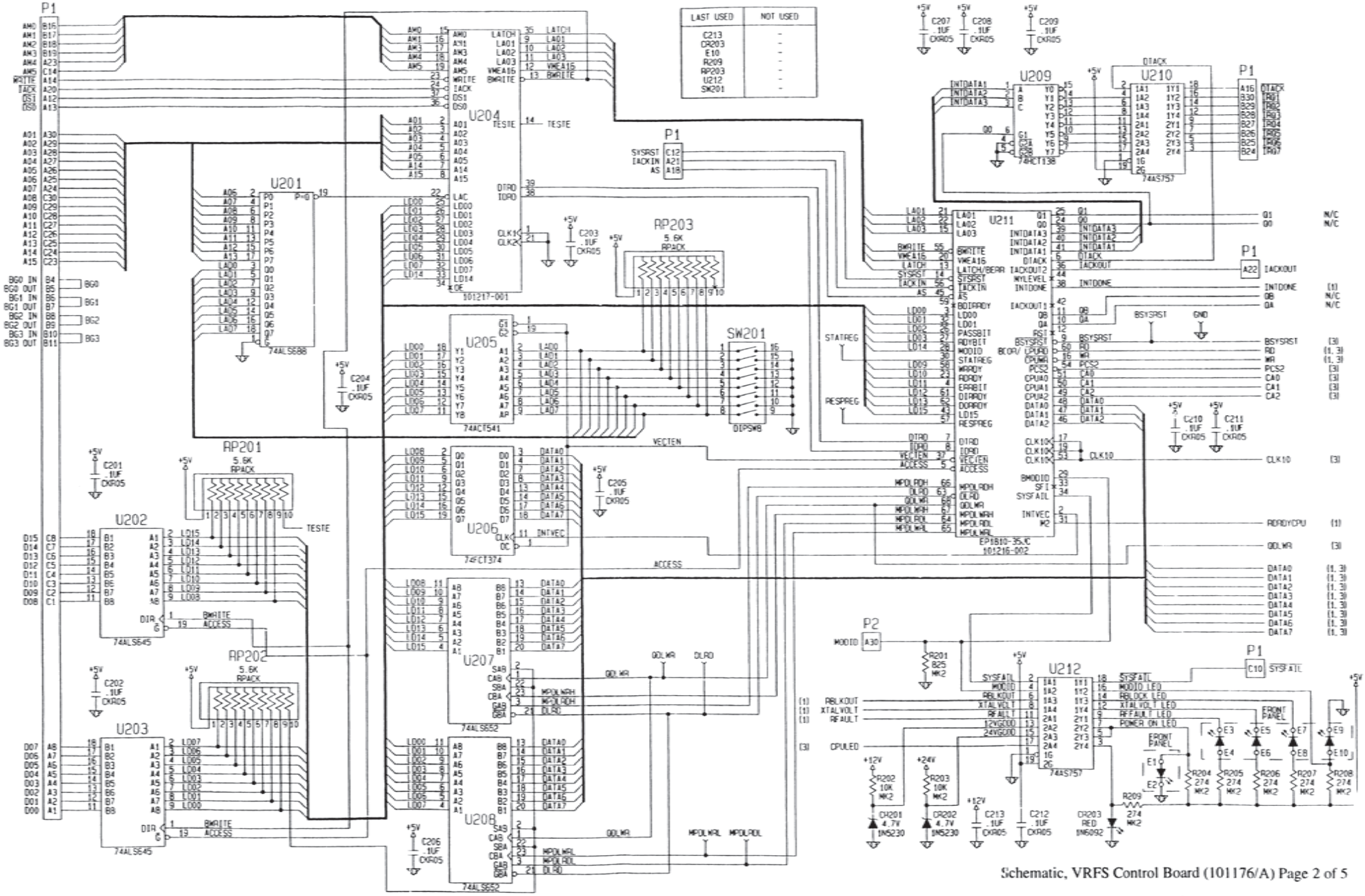
SPARES



LAST USED	NOT USED
C141	-
CR103	-
L103	-
R118	-
U105	-
VR101	-
Y101	-

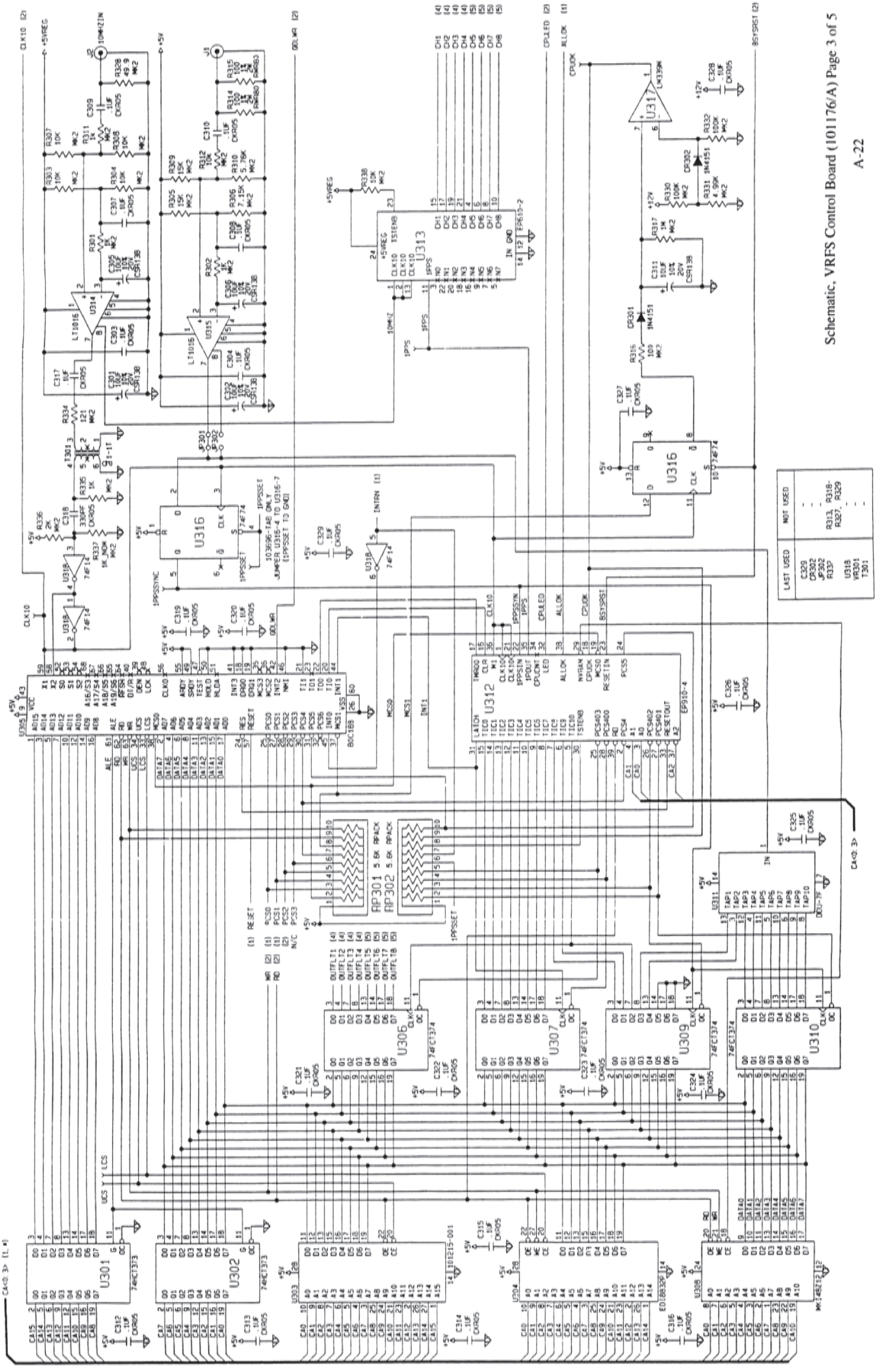
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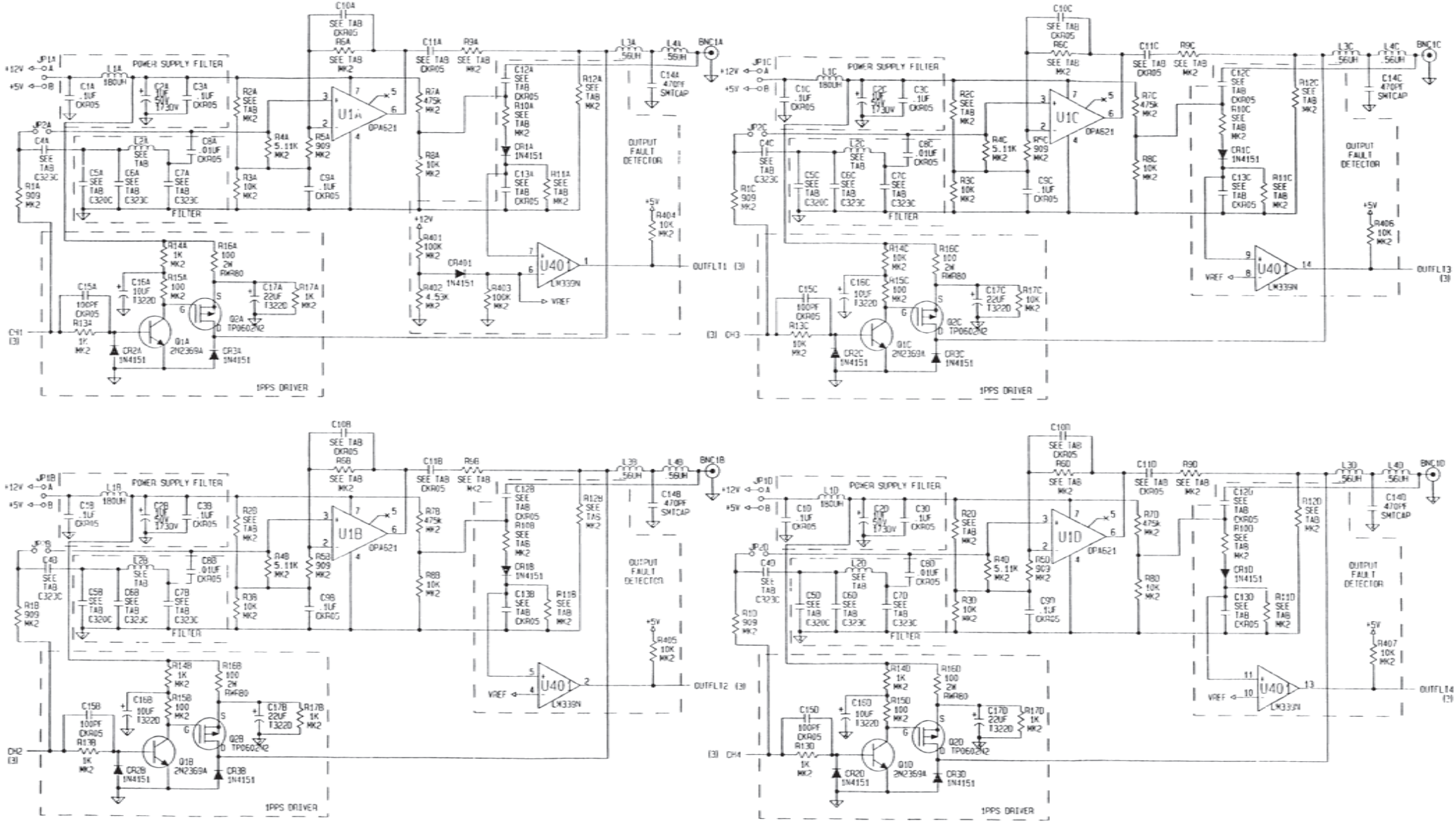
Schematic, VRFS Control Board (101176/A) Page 2 of 5

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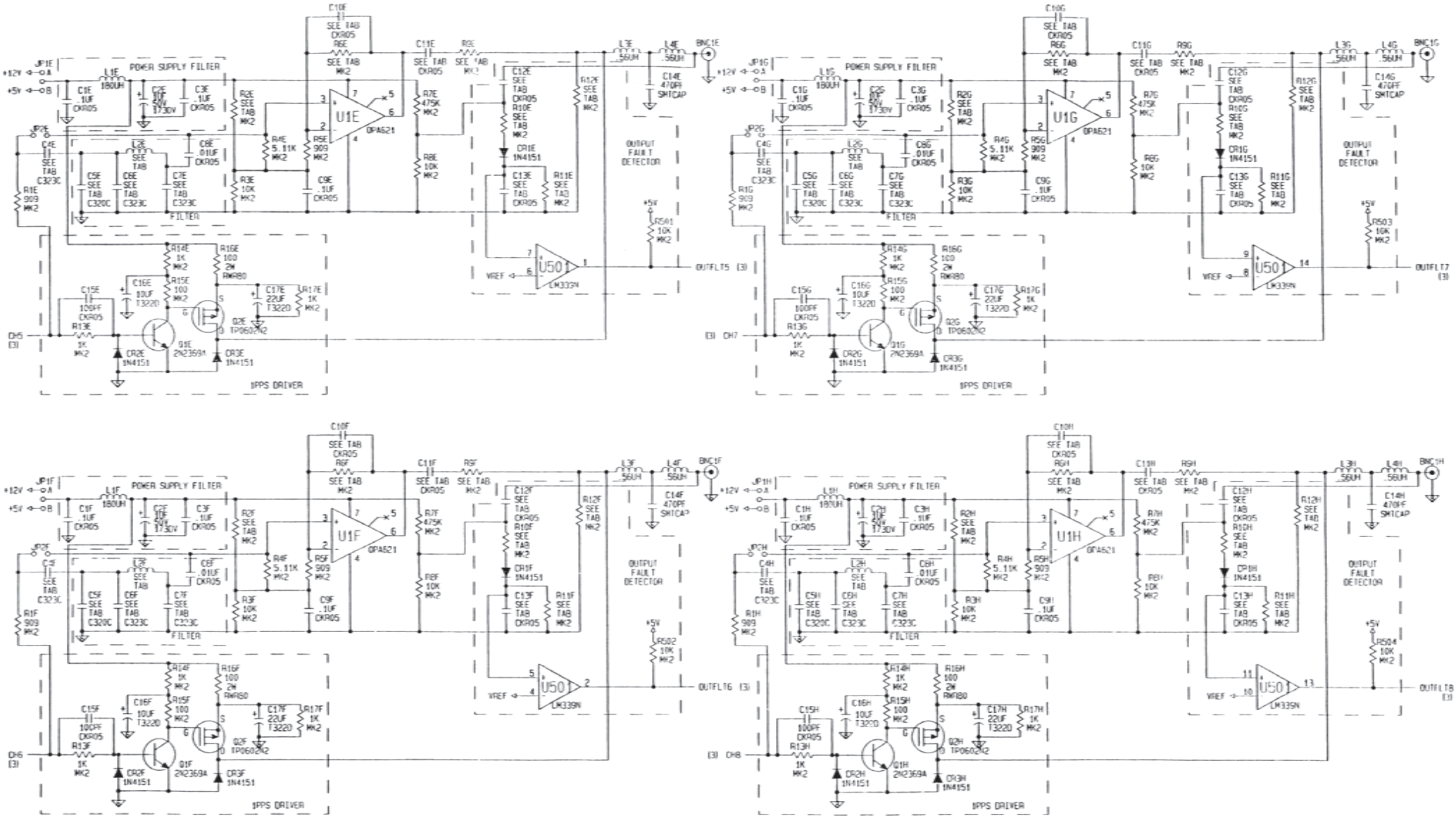


Schematic, VRFS Control Board (101176/A) Page 3 of 5

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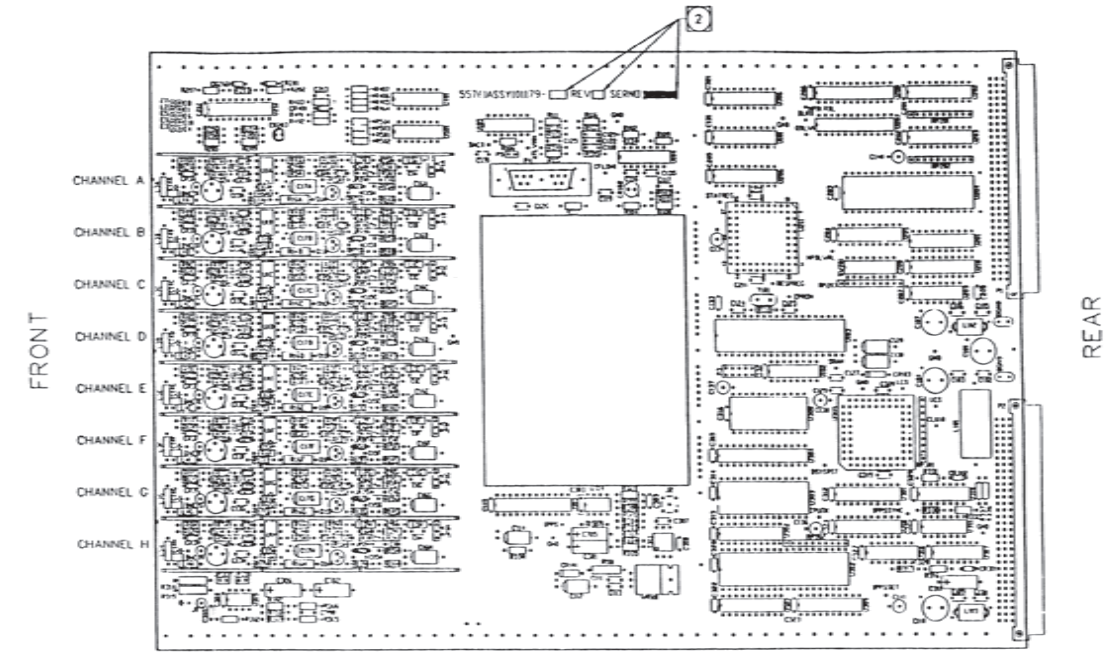
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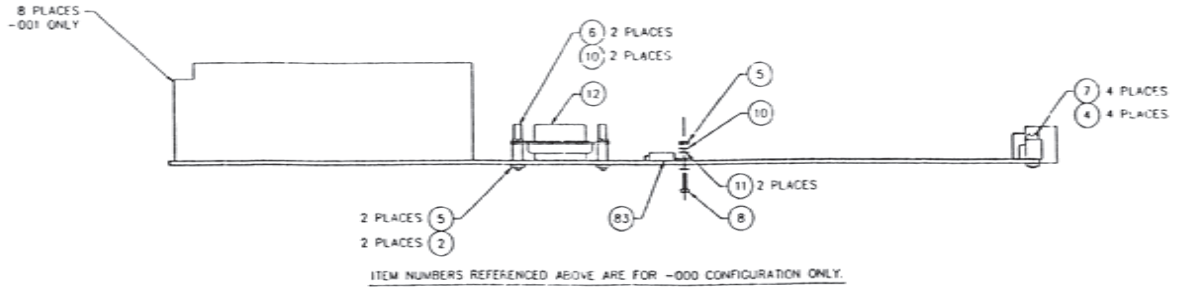


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NOTES: UNLESS OTHERWISE SPECIFIED

1. PART ATTACHMENT, WIRING, SOLDERING, CLEANING AND WORKMANSHIP SHALL BE IN ACCORDANCE WITH IPC-S-815 CLASS III.
2. IDENTIFY WITH ASSEMBLY NUMBER, APPLICABLE DASH NUMBER, REVISION LETTER, AND SERIAL NUMBER PER MIL-STD-130.
3. DELETED
4. DELETED
5. SEE PARTS LIST FOR REFERENCE DOCUMENTS PERTINENT TO THE PRODUCTION OF THIS ASSEMBLY.
6. MAXIMUM TEMPERATURE NOT TO EXCEED 85°C ON BODY OF PART. (U308 TO BE HAND SOLDERED.) APPLIES TO -001 CONFIGURATION ONLY.

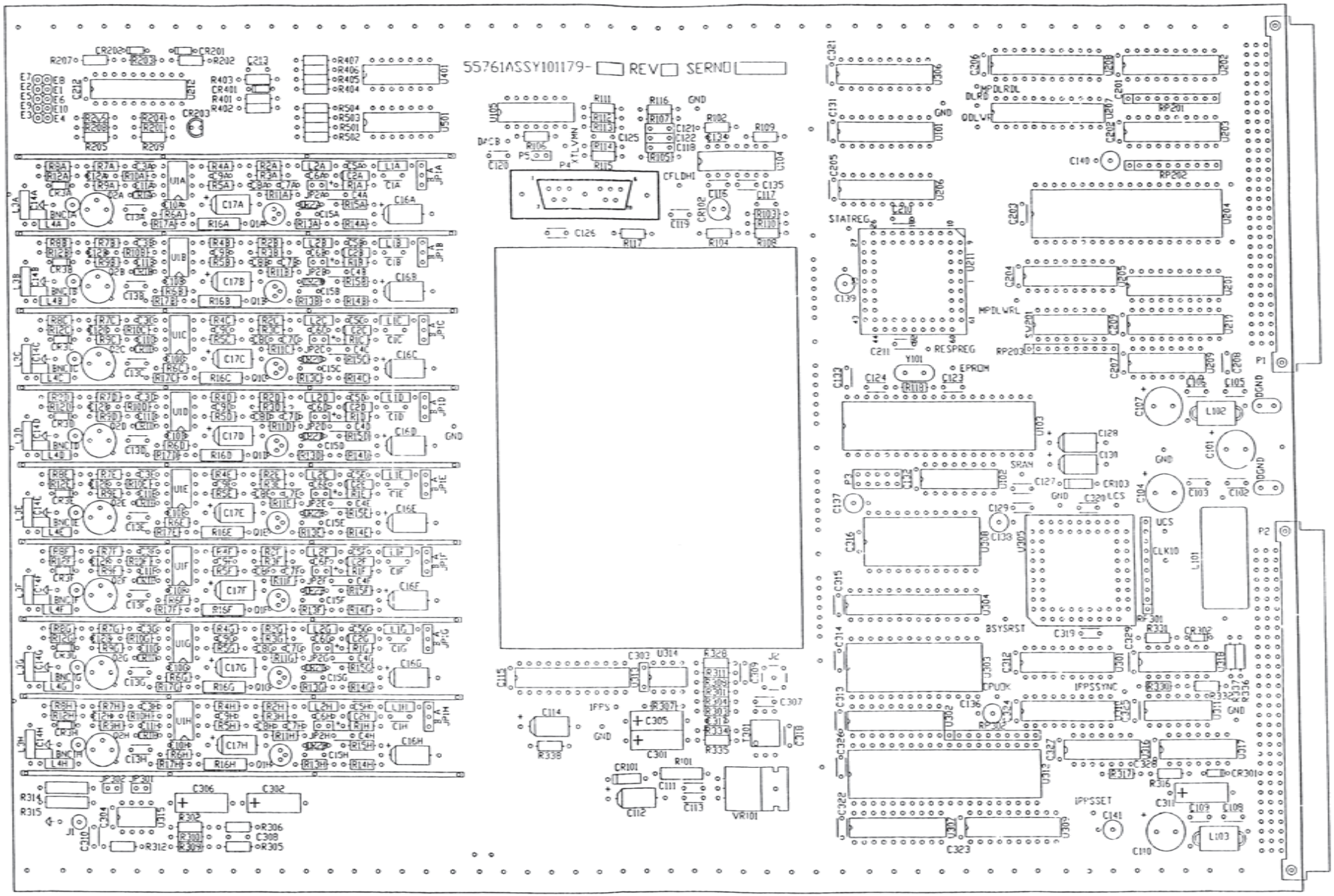




ITEM NUMBERS REFERENCED ABOVE ARE FOR -000 CONFIGURATION ONLY.

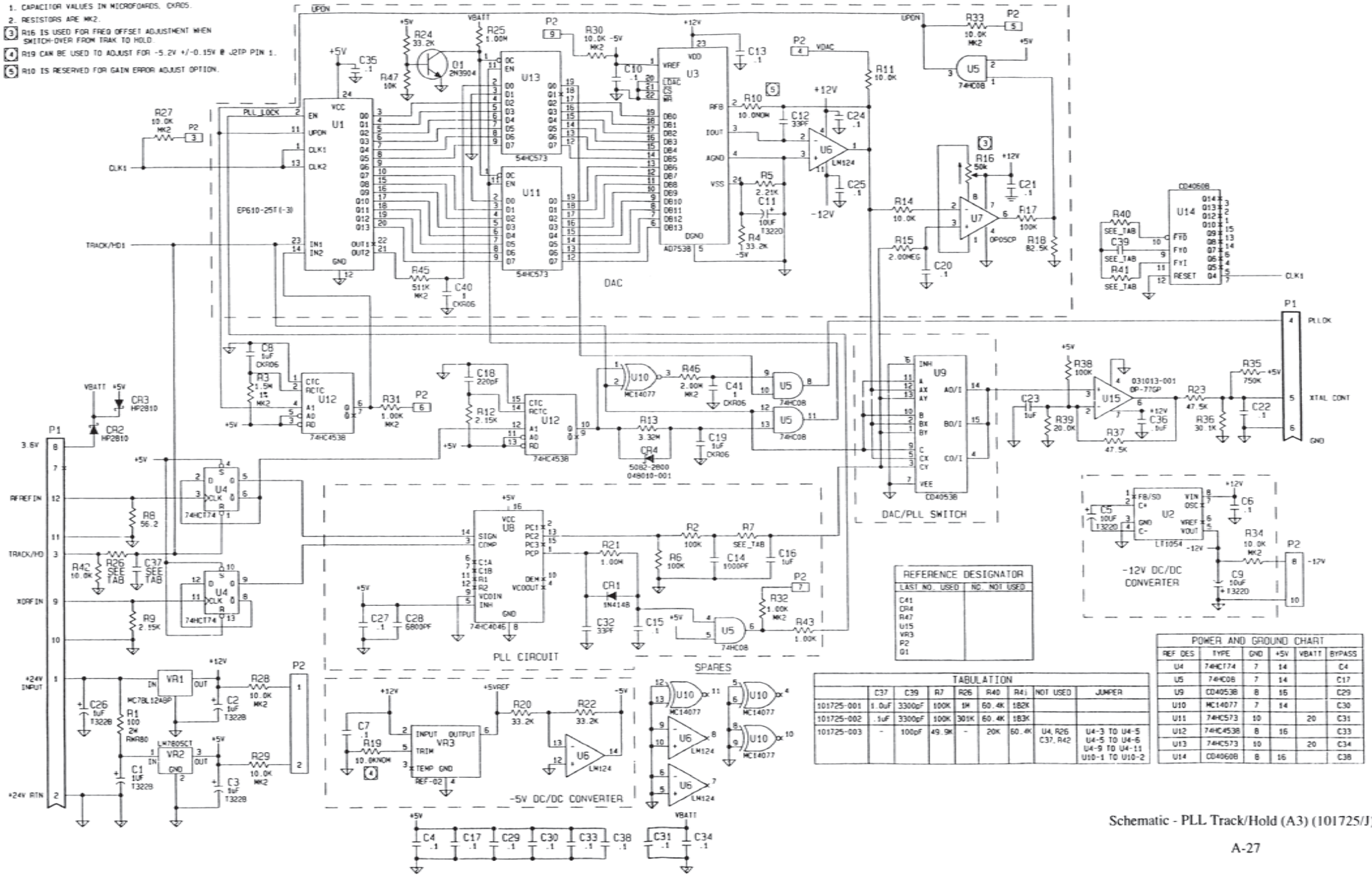
-	5
SHT 1	SHT 2
REV STATUS OF SHEETS	

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Circuit Card Assembly, VRFS (101179/-) Page 2 of 2

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Schematic - PLL Track/Hold (A3) (101725/J)

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NOTES: UNLESS OTHERWISE SPECIFIED

1. SEE PARTS LIST FOR ALL DOCUMENTS PERTINENT TO THE PRODUCTION OF THIS ASSEMBLY

(2) IDENTIFY WITH APPLICABLE DASH NUMBER, REVISION LETTER, AND SERIAL NUMBER AS REQUIRED.

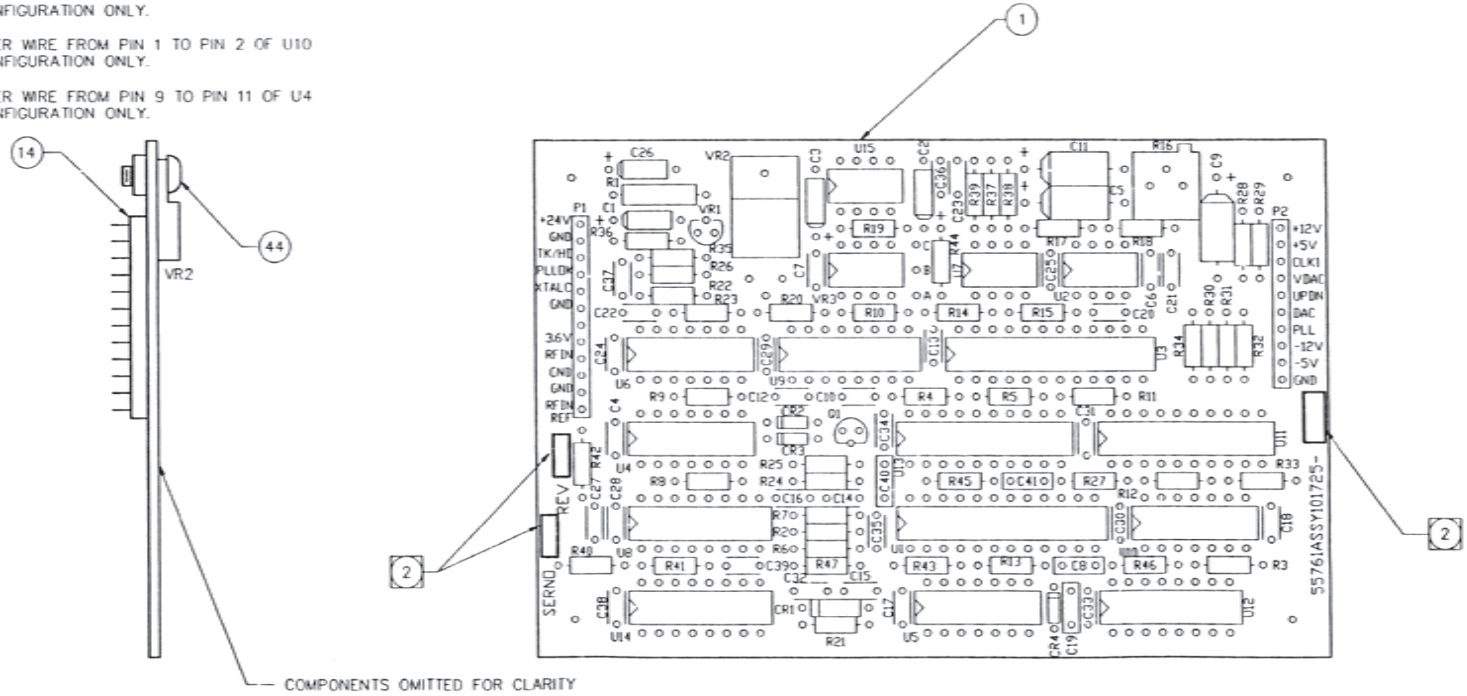
3. PART ATTACHMENT, WIRING, SOLDERING, CLEANING AND WORKMANSHIP SHALL BE IN ACCORDANCE WITH IPC-S-815, CLASS II

(4) INSTALL JUMPER WIRE FROM PIN 3 TO PIN 5 OF U4 FOR -003 CONFIGURATION ONLY.

(5) INSTALL JUMPER WIRE FROM PIN 5 TO PIN 6 OF U4 FOR -003 CONFIGURATION ONLY.

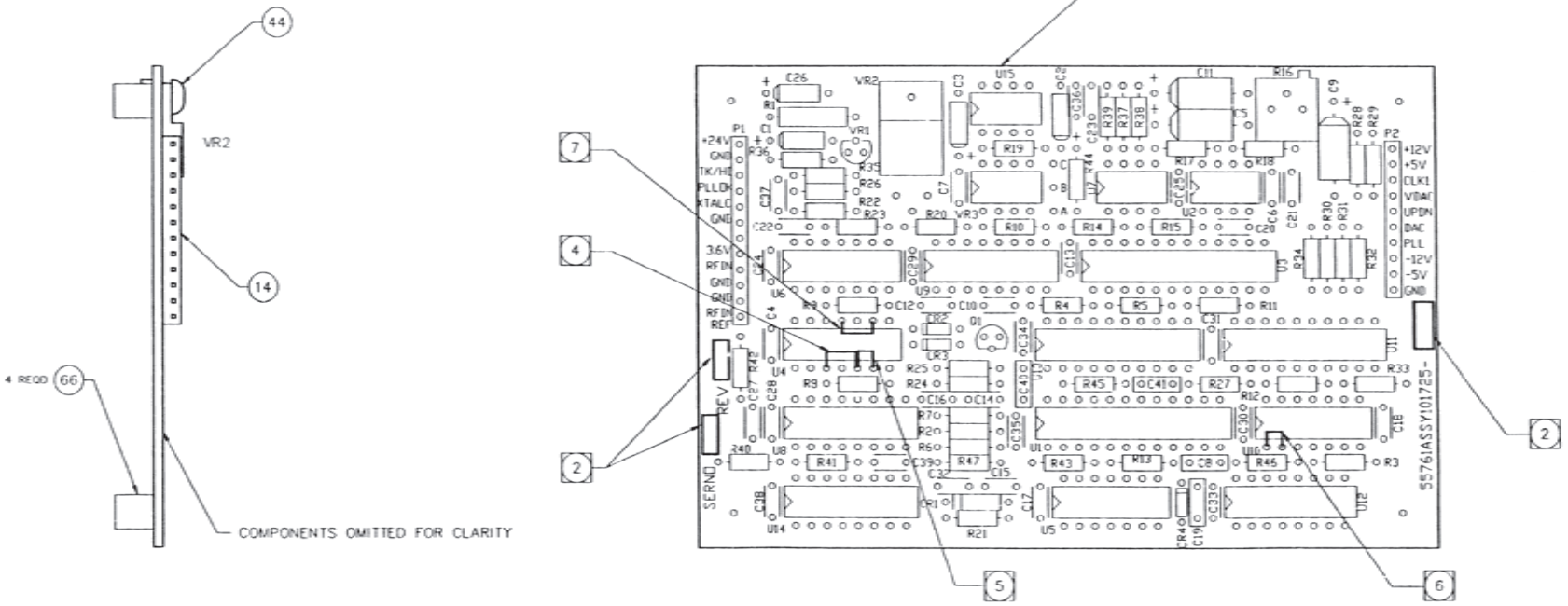
(6) INSTALL JUMPER WIRE FROM PIN 1 TO PIN 2 OF U10 FOR -003 CONFIGURATION ONLY.

(7) INSTALL JUMPER WIRE FROM PIN 9 TO PIN 11 OF U4 FOR -003 CONFIGURATION ONLY.



-001 & -002 CONFIGURATION.

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-003 CONFIGURATION

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