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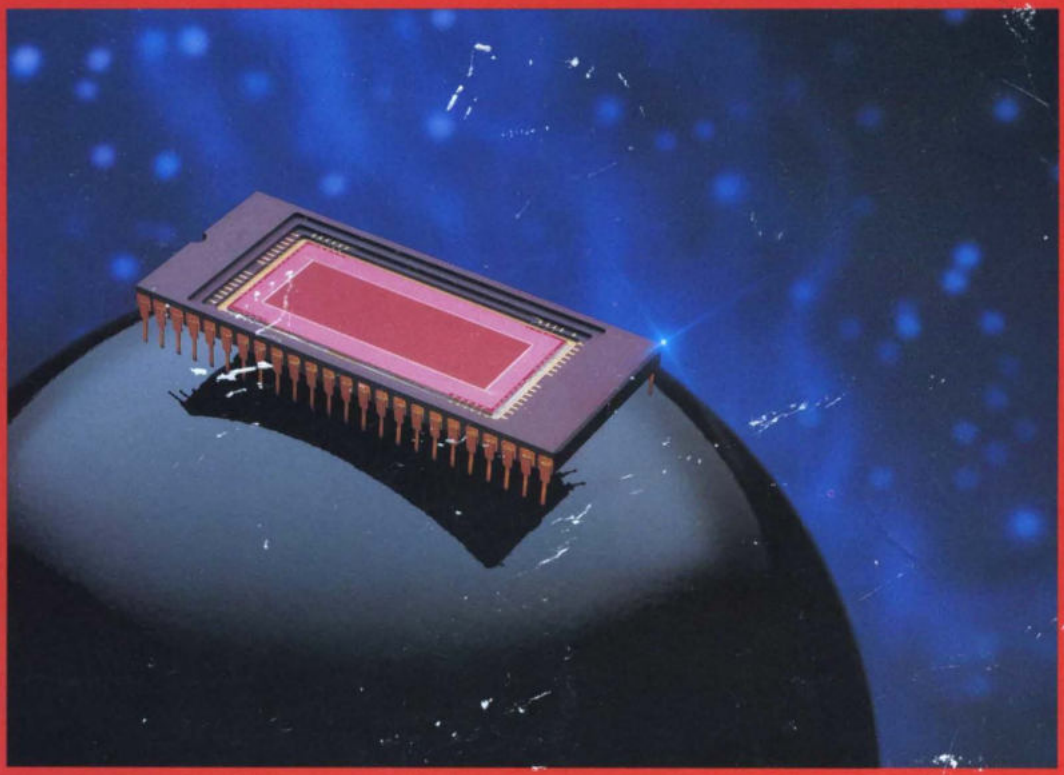
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Image Sensing Products 1992/1993



EG&G RETICON
WHERE VISION AND TECHNOLOGY MEET

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Linear Arrays

D Series Linear
D Series Tapped
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EG&G RETICON

D Series Linear Family
Charge-Coupled Photodiode Array

EG&G Reticon's D Series image sensors are high-speed, self-scanned, charge-coupled photodiode (CCPD) arrays. The D Series Family, consisting of the STANDARD-D, VALUE-D, FAST-D, and LOLIGHT-D image sensors, allows the designer to select just the right device for a particular application. Typical applications include optical character recognition, document scanning, inspection, pattern recognition, noncontact measurement, and other applications requiring high quality, broad spectral response image acquisition.

Key Features

- Antiblooming
- Video data rates up to 30 MHz
- High photo sensitivity
- Wide dynamic range
- 256, 512, 1024, and 2048 elements
- 13 µm x 13 µm and 13 µm x 26 µm picture elements
- Low power consumption
- Wide spectral response (UV to near IR)

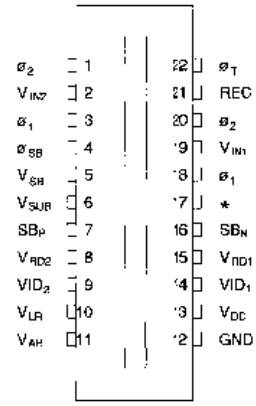


Figure 1. Pinout Configuration
*** (Pin 17 is N/C for RL0256D, V_{SUB} for all other D Series devices)**

General Description

The D series family of image sensors features the CCPD architecture which combines the best features of CCD and photodiode technology. The CCD read-out structure allows very high speed, low noise operation. The photodiode sensing elements provide superior light sensitivity, especially in the blue and near-UV portion of the spectrum.

The STANDARD-D device is the nominal component of the D series family. It operates at data rates up to 20 MHz, has 13 µm x 13 µm pixels, and features very high dynamic range. The VALUE-D device is a lower cost version with all the same features as the STANDARD-D, but has a maximum data rate of 10 MHz and slightly reduced dynamic range. The FAST-D device is specified for operation at data rates up to 30 MHz. The LOLIGHT-D device is a wide aperture version featuring 13µ x 26µ pixels for higher photo sensitivity.

Functional Description

The sensing elements for the D Series Linear CCPDs are a row of diffused p-n junction photodiodes spaced on 13 µm centers and interdigitated into a sensing aperture 13 µm wide (26 µm for LOLIGHT-D). The photodiode sensing elements provide very broad spectral response while the CCD readout registers and output buffer amplifiers allow very low-noise signal extraction. Figure 1 shows the pinout configuration and Figure 2 is a simplified schematic diagram. Figure 3 shows the aperture response function and sensor geometry. The dimensions shown in Figure 3 are as follows: the photodiode diffusion width *a* is 7 µm, the center-to-center spacing *b* is 13 µm and the aperture width *c* is 13 µm or 26 µm. Note that the entire 13 µm (dimension *b*) produces photocurrent which divides between the two diffusions, with most of the charge going to the pixel nearest the site of the photon absorption.

In addition, D Series Linear devices contain an antiblooming gate which can be used to either suppress blooming or to set the integration period independent of the line rate. That allows these devices to be used over the widest possible range of lighting conditions.

Light incident on the sensing aperture generates a photocurrent which is integrated and stored as a charge on the capacitance of each of the photodiodes. If the charge accumulated on any diode exceeds a saturation value, the excess is shunted to V_{AB} through the antiblooming gates, controlled by V_{LR}, to control blooming effects. Refer to Figure 2.

The antiblooming gate is biased at a DC potential which is below that of the junction barrier and transfer gate $ø_T$ "low" barrier. When the signal charge reaches the level set by the antiblooming gate, the excess will be sunk into V_{AB}, thus preventing blooming.

At the end of each integration period, the charges on all the diodes are simultaneously switched through transfer gates, $ø_1$, into one of two CCD analog shift registers for readout. The odd numbered diodes are switched into one register and the even diodes into the other. Immediately after this parallel transfer, a new integration period begins.

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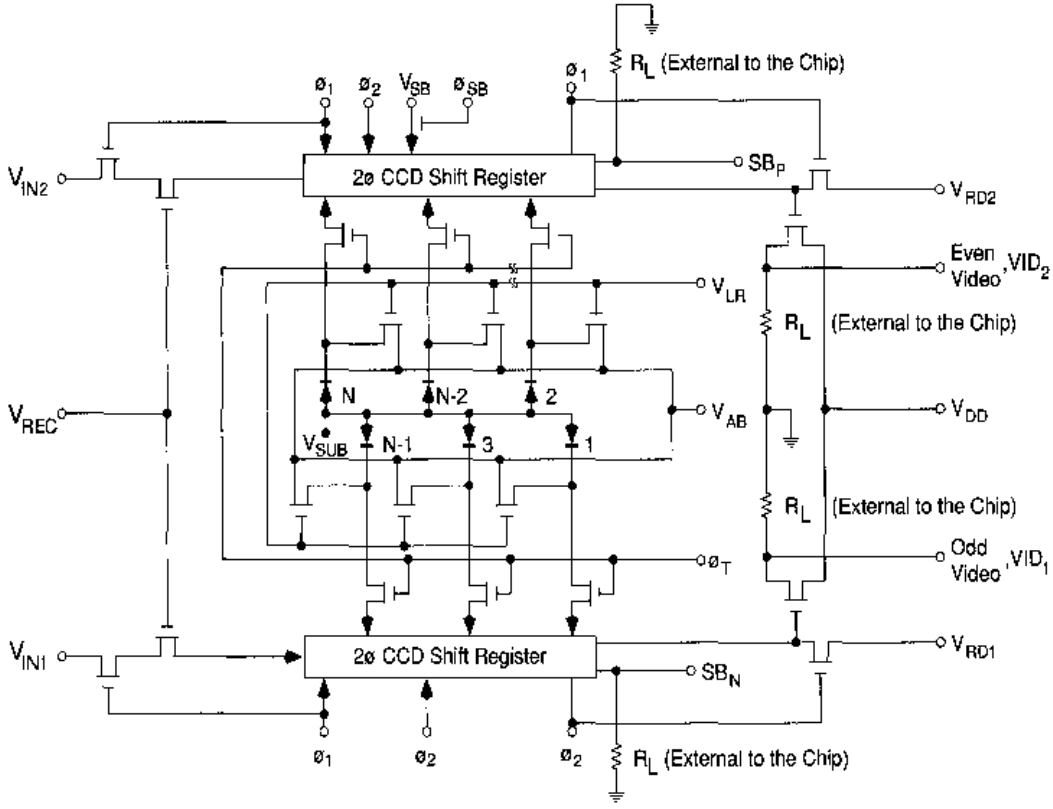


Figure 2. Schematic of D Series Linear Devices

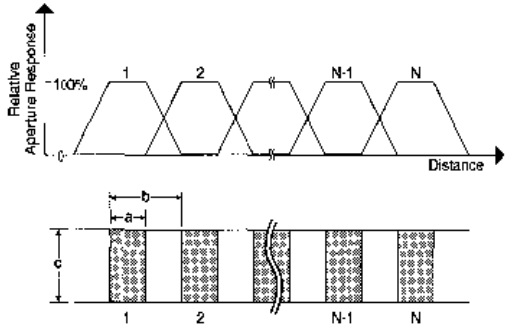


Figure 3. Sensor Geometry and Idealized Aperture

Readout is accomplished by clocking the CCD shift registers so that the charge packets are delivered sequentially into two on-chip charge-detection circuits. The registers deliver the charge packets to their outputs on alternate clock phases, allowing the inactive charge detector to be reset to a fixed level, V_{RD}, while the opposite detector is active. The outputs of the two detectors may then be multiplexed off-chip if a single continuous video output is desired. Each video signal is developed accross a 2-5KΩ resistive load, R_L.

Operation

D Series devices require two complimentary shift register clocks, ϕ_1 and ϕ_2, and a transfer gate pulse, ϕ_T, for normal operation. An additional transfer pulse, ϕ_{SB}, is required if a scan buffer output is desired. The clocks and their timing relationships are shown in Figure 4. The video output and scan buffer output, SB_P, are also shown in Figure 4.

The scan buffer output provides two marker bits; the first pulse coincides with the first video element, and the second with the last video element. The scan buffer output is obtained by differencing SB_P and SB_N through a differential amplifier. The circuit shown in Figure 6 will provide the required interface between the device's scan buffer output and its peripheral TTL circuit. Use of the scan buffer at higher speeds is not recommended. It may be defeated by applying 0V to ϕ_{SB}.

The transfer pulse should swing between -3 and +5V and must have a width greater than 0.2 µsec. In order to transfer the charge from the photodiodes into the CCD register, the ϕ_T clock must remain high during the blanking and transfer interval (see Figure 4). The odd and even video

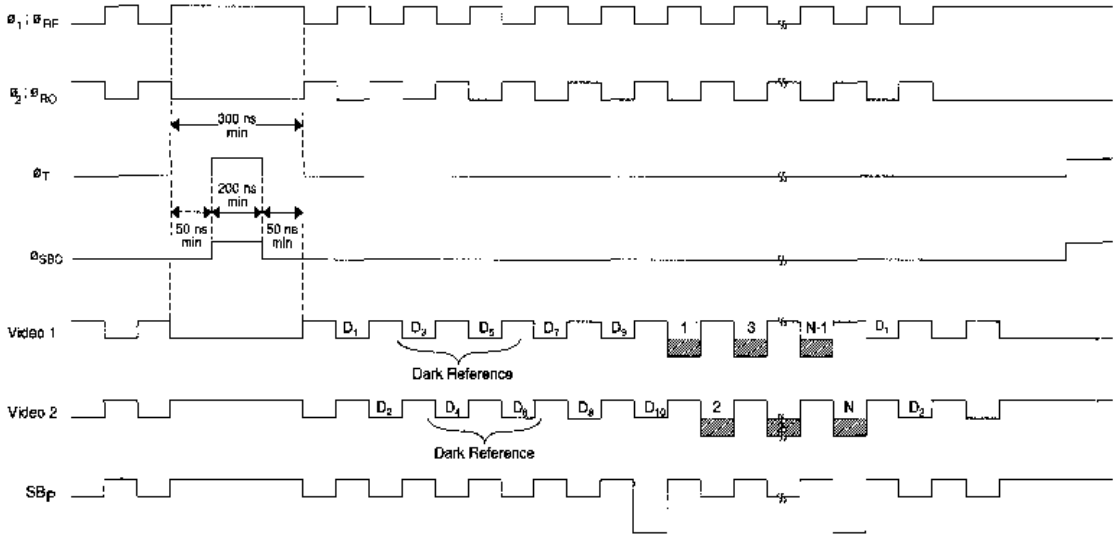


Figure 4. Timing Relationship of the Array's Clock Signals and Output

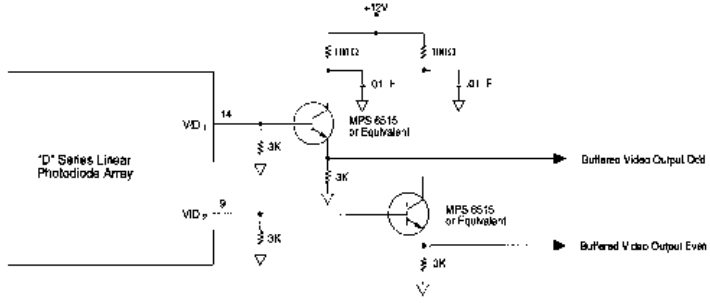
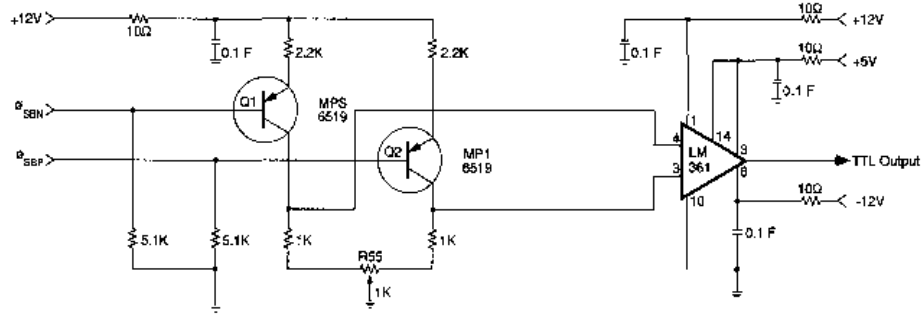


Figure 5. Recommended Output Circuit



Scan Buffer Output Circuit

Figure 6. Recommended Buffer Output Circuit

outputs are also shown in Figure 4. The odd and even output reset clocks, $ø_{RO}$ and $ø_{RE}$, are derived from the same sources as $ø_1$ and $ø_2$ and are nominally synchronous with them. Figure 10 shows the schematic of a typical voltage drive circuit for the D Series.

Antiblooming and line reset operation may be accomplished by applying a small positive voltage to the antiblooming gate, V_{LR}. The actual bias values vary from device to device. Antiblooming requires a DC bias of typically 1 - 3V. Line reset requires V_{LR} to be clocked to typically 2.5 - 4.5V for approximately 1 µs. Using line reset may significantly increase nonuniformity.

Figure 9 shows typical video output waveforms as measured across a 3KΩ load resistor. Relative timing is indicated in relation to $ø_1$ and $ø_2$ clocks. The rise and fall times indicated are relative since they are affected by capacitive loading, including oscilloscope probe capacitance.

A high speed amplifier output circuit such as shown in Figure 5 is not required but is recommended to reduce the loading effects of external circuit capacitance. This will result in video rise and fall times of 50 ns or less.

Performance

Spectral response of D Series devices covers the range from UV to the near IR. A ground and polished glass window is provided on the STANDARD-D, VALUE-D, and FAST-D devices. A quartz window is provided on LOLIGHT-D devices. Relative spectral response is shown as a function of wavelength in Figure 7.

Since most applications for these devices (OCR, machine vision, etc.) use visible light, the responsivity and uniformity of response are specified using a light source with the spectral distribution shown by the dotted line in Figure 7. This spectral distribution is produced by filtering a 2870°K tungsten source with a Fish-Schurman HA-11 heat absorbing 1 mm thick filter.

Transfer characteristics showing the noise level and saturation output voltage can be seen in Figure 8. Since Reticon line scan devices operate in the charge-storage mode, the charge output of each diode (below saturation) is proportional to exposure; i.e., the irradiance or light intensity multiplied by the integration time or the time interval between successive transfer pulses. Thus, there is a trade-off between scanning speed and required light intensity. Light intensity in watts needed to saturate a pixel at a particular integration time can be obtained by dividing saturation exposure by integration time. Thus, longer integration times may be used to detect lower light levels. However, this approach is ultimately limited by dark leakage current which is integrated along with the photocurrent. At room temperature, dark current will typically contribute less than 0.1% of a saturated signal for an integration time of 5 msec.

Drive Circuit

The circuit shown in Figure 10 will interface a TTL level control circuit to D Series CCPD devices. It will ensure that the $ø_1$ and $ø_2$ clock transitions cross at or above the midpoint; i.e., 50% clock crossing or higher. The supply

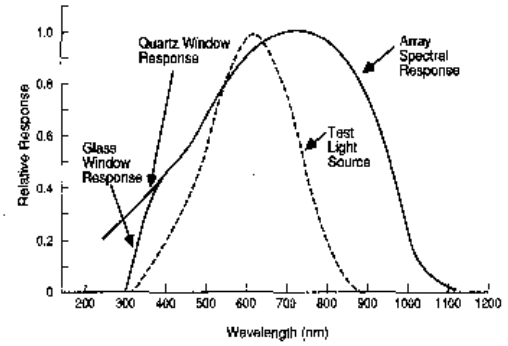


Figure 7. Relative Spectral Response as a Function of Wavelength

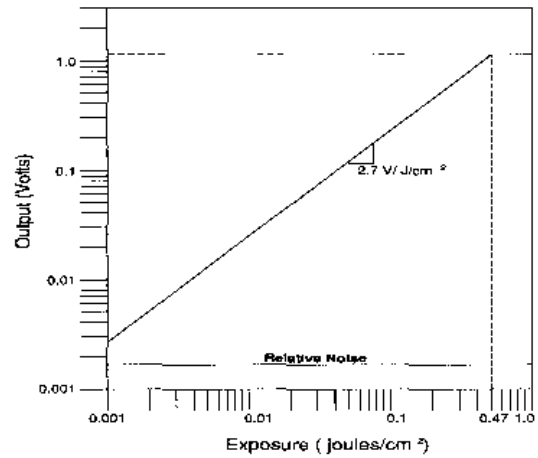


Figure 8. Typical Transfer Characteristics

voltages to the $ø_1$ and $ø_2$ clock drivers, devices 3 and 4, are as follows: V_{SS} = 0V or ground and V_{DD} = +12V.

The clock drivers, devices 1A and 1B, will provide voltage swings consistent with those given in the specification table. The supply voltages to device 1A are V_{DD} = +5V, pin 6 and V_{SS} = -4V. The supply voltages to device 2A are V_{DD} = +12V, pin 6, and V_{SS} = +5V. (Note: Both supply pins are positive to keep the minimum swing to +5V.)

Evaluation Board

A complete evaluation circuit board (RC0730LNN) is available for the D Series and is recommended for first-time evaluation. The board contains all required logic and drive circuitry and has buffered outputs capable of operating at data rates up to 20 MHz.

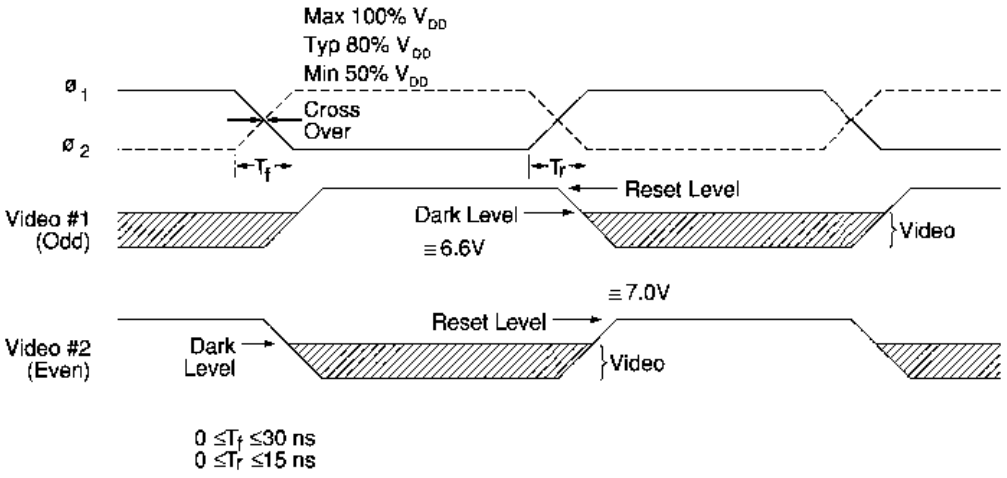


Figure 9. Clock Crossing and Video Output Relationship

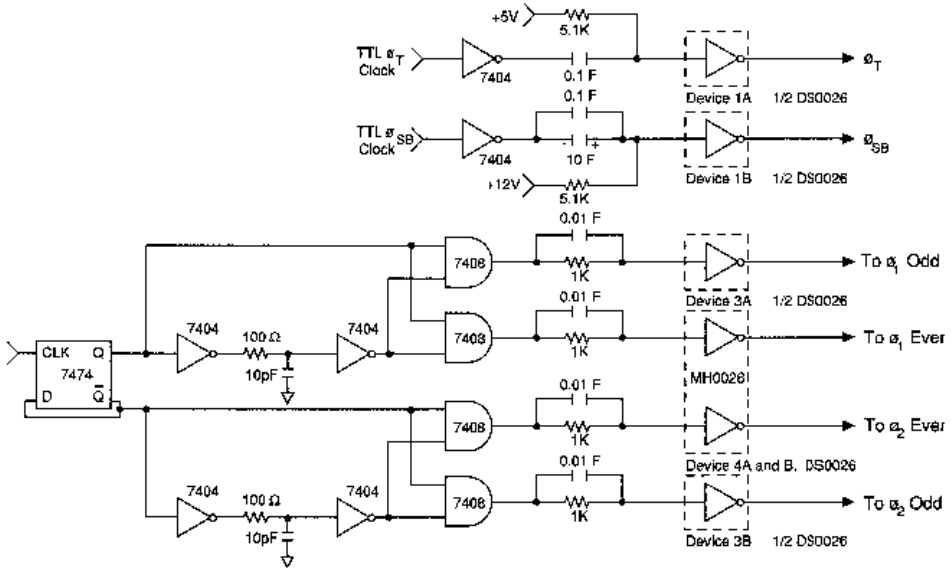


Figure 10. Drive Circuit for D Series Linear Devices

Table 1. Array Bias and Clock Level Requirements

Symbol	Parameter	Min	Typ	Max	Units
V_{RD}	Reset drain bias	+11	+12	+13	V
V_{DD}	Output drain bias	+11	+12	+13	V
V_{IN}	Input bias	+11	+12	+13	V
V_{AB}	Antiblooming drain	+11	+12	+13	V
V_{LR}	Antiblooming gate				
	Disabled	-1	0	+1	V
	Antiblooming active	+1	+1.7	+2.5	V
	Line reset active	+2.5	+3.5	+4.5	V
V_{SUB}	Substrate bias	-6	-5	-4	V
$ø_1$, $ø_2$	CCD transport clock				
	High	+11	+12	+13	V
	Low	-1	0	+1	V
$ø_T$	Transfer clock				
	High	+4	+5	+6	V
	Low	-4	-3	-2	V
$ø_{SB}$	Transfer clock scan buffer				
	High	+11	+12	+13	V
	Low	+4	+5	+6	V
V_{REC}	Receiving gate	-1	0	+1	V
V_{SB}	DC input scanning	+11	+12	+13	V

"Min and Max values shown represent the allowable tolerance to maintain normal operation and are not absolute min and max values".

Table 2. Absolute Maximum Ratings
(Above Which Useful Life May Be Impaired)

Storage temperature	-25°C to 85°C
Operating temperature	-25°C to 55°C
Voltage on any pin with respect to substrate	-0.3V to 22V

Table 3. Linear D Series Array Capacitance Values [1]

		Typical Capacitance (pF)			
Pin No.	**Symbol**	**RL2048D**	**RL1024D**	**RL0512D**	**RL0256D**
1, 20	$ø_7$	280	135	80	40
3, 18	$ø_1$	280	135	80	40
4	$ø_{SB}$	25	13	8	6
7, 16	SB_P, SB_N	5	4	4	3
9, 14	VID_2, VID_1	5	4	4	3
10	V_{LR}	14	14	14	14
22	$ø_T$	65	31	18	12

Notes:

[1] Measured with respect to device substrate (pin 6) with a DC. bias voltage of +12V

Table 4. Array Performance Characteristics

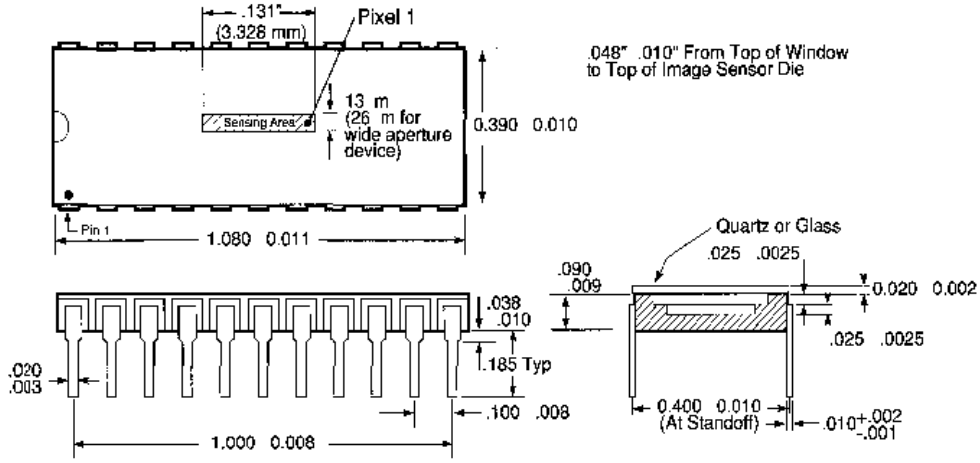
CONDITIONS: (unless otherwise specified)
T_a = 25°C, f_{data} = 400 KHz, t_{ex} = 10 ms, R_L (at video output) = 3KΩ, V_{AB} = 2V, Light Source = 2870°K + Fish Schurman HA-11, 1 mm filter. All other operating voltages are nominal, as specified in Array Electrical Characteristics
First and last pixels of each video output are ignored

Symbol	Parameter	Min	Typ	Max	Units
DR_{p-p}	Dynamic range [1]				
	Standard-D, LoLight-D		2600:1	-	-
	Value-D, Fast-D		2000:1	-	-
DR_{rms}	Dynamic range [1]				
	Standard-D, LoLight-D	-	13000:1	-	-
	Value-D, Fast-D	-	10000:1	-	
E_{NF}	P-to-P noise equivalent exposure	-	.18	-	nj/cm²
	LoLight-D		.09		nj/cm²
E_{SAT}	Saturation exposure	.30	.47	.63	µj/cm²
	LoLight-D	.15	.24	.32	µj/cm²
R	Responsivity	2.0	2.7	3.3	V/µj/cm²
	LoLight-D	4.0	5.4	6.6	V/µj/cm²
PRNU	Photoresponse nonuniformity [4,5]				
0256	[2]	-	3	8	±%
0512	[2]	-	3	8	±%
1024	[2]	-	3	10	±%
2048	[2]	-	5	12	±%
V_{dk}	Average dark signal [3,5]	-	.03	.25	%
V_{dm}	Maximum dark signal [4,5]	-	.06	.5	%
V_{SAT}	Saturation output voltage	0.8	1.3	1.6	V
P	DC Power dissipation [5]	-	126	-	mW
N_{p-p}	Peak-to-peak noise	-	0.5	-	mV
V_{RGR}	Output DC reset level [5]	-	7.0	-	V
V_{DCO}	Output DC dark level [5]	-	6.7	-	V
Z_{out}	Output impedance [6]	-	2	-	kΩ
V_{bal}	Video output balance [9]	-	30	80	mV
	Output DC drift [10]	-	10	-	mV/°C
f_{data}	Maximum guaranteed video data rate [7]				
	Value-D	10	-	-	MHz
	Standard-D and LoLight-D	20	-	-	MHz
	Fast-D	30	-	-	MHz

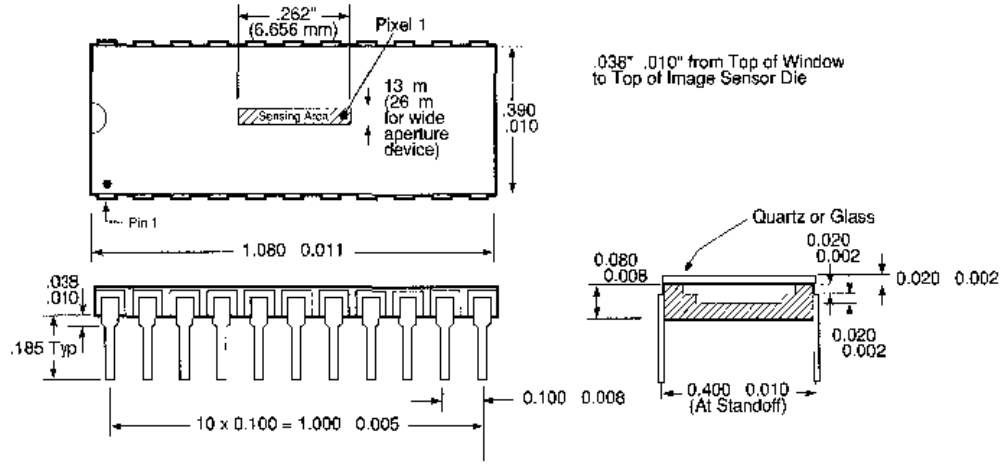
Notes:

1. Dynamic range is defined as V_{SAT}/N_{P-P}. RMS noise is approximately $N_{P-P}/5$
2. Measured at an exposure level of approximately $V_{SAT}/2$. PRNU is defined as 100*[(V_{max}-V_{min})/V_{avg}] where V_{max} is output of highest pixel (toward V_{sat}). V_{min} is output of lowest pixel (towards dark) and V_{avg} is the numerical average of all the pixels in the video line
3. Measured at ambient temperatures Ta = 25°C, t_{int} = 2.5 ms. Defined as 100* (V_d/V_{sat}) where V_d is the numerical average of the output of all pixels in dark and V_{sat} is the numerical average of all pixels in saturation.
4. Measured at ambient temperature T_a = 25°C, t_{int} = 2.5 ms. Defined as 100* (V_m/V_{sat}) where V_m is the pixel with the maximum output of all pixels in dark and V_{sat} is the numerical average of all of pixels in saturation
5. Measured with device in the dark
6. Measured with output current of 2 mA
7. f_{data} is defined as 2 times f_{clock} where f_{clock} is the frequency of the $ø_1$ or $ø_2$ clock. The minimum frequency is limited by increases in dark signal.
8. Dark signal approximately doubles for each 7-10°C increase in temperature
9. Defined as the difference in dc dark level output (D_{dc}) between the two video outputs

Package Dimensions RL0256D



Package Dimensions RL0512D



Package Dimensions RL1024D

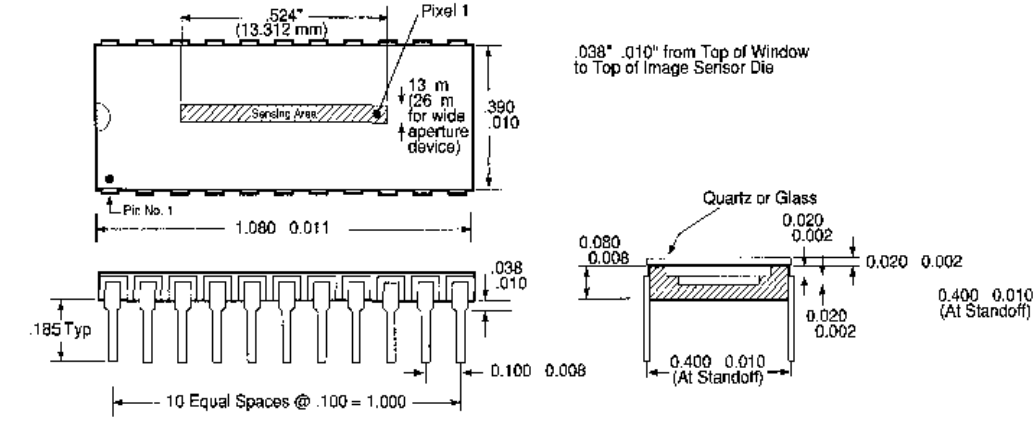
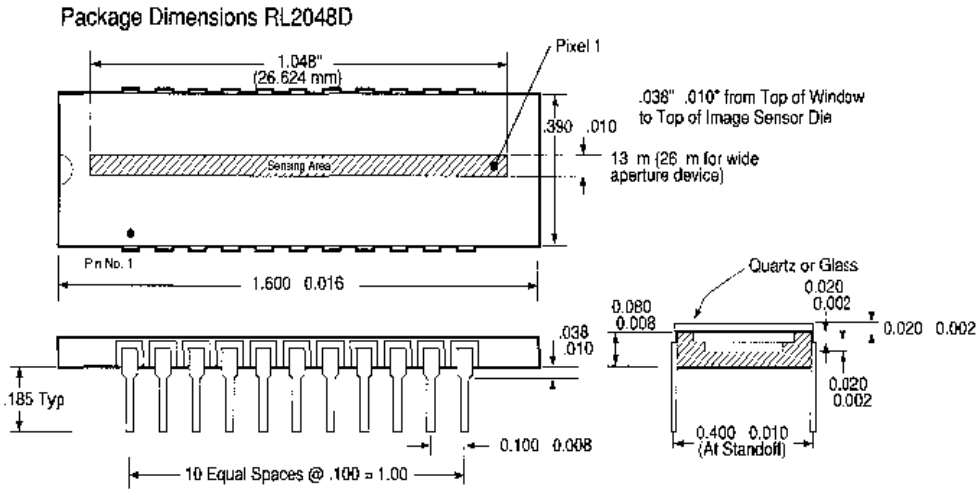


Figure 11. Package Dimensions

Figure 11. Package Dimensions (cont'd)



Ordering Information

Standard-D	Value-D	Fast-D	LoLight-D	Evaluation Board
RL0256DAG-011	RL0256DAG-020	RL0256DAG-021	RL0256DKQ-011	RC0730LNN-011
RL0512DAG-011	RL0512DAG-020	RL0512DAG-021	RL0512DKQ-011	RC0730LNN-011
RL1024DAG-011	RL1024DAG-020	RL1024DAG-021	RL1024DKQ-011	RC0730LNN-011
RL2048DAG-011	RL2048DAG-020	N/A	RL2048DKQ-011	RC0730LNN-011

The quartz window supplied standard on LoLight-D devices is available as an option for all D Series devices. For options, consult EG&G Reticon.

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Introduction

EG&G Reticon's RL1282D, RL1284D and RL1288D are ultra-high-speed, self-scanned charge-coupled linear arrays with video output taps every 128 diodes. The RL1282D has two sections and a resolution of 256, the RL1284D has four sections and a resolution of 512, and the RL1288D has eight sections with 1024 resolution.

Applications for these arrays include optical character recognition, high-speed document scanning, pattern recognition, noncontact measurement, or any process requiring a high-speed linear array.

Key Features

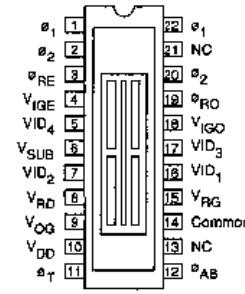
- 256, 512 or 1024 elements
- 18 µm x 18 µm picture elements
- Low power requirements
- +15 and -5V supplies
- On-chip preamplifier
- Wide dynamic range
- Low noise equivalent exposure
- Video sampling rates up to 15 MHz per output channel
- Effective data rates to 240 MHz
- 4.2 µs line scan time
- Wide spectral response, near UV to near IR
- Antiblooming circuitry
- Line reset feature

Functional Description

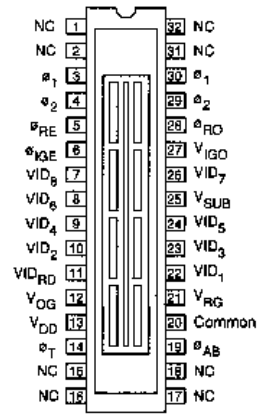
The RL1282D, RL1284D, and RL1288D have 256, 512 and 1024 contiguous diodes respectively, divided into sections of 128 pixels. Each block of 128 pixels has two shift registers for readout, one for odd-numbered pixels within a section (odd video channel), the other for even-numbered pixels within a section (even video channel). The RL1282D, RL1284D, and RL1288D have, respectively, 4, 8, and 16 CCD analog shift registers and the same number of video output lines. Each video output has a preamplifier and can obtain pixel rates up to 15 MHz. Pin configurations are shown in Figure 1. Figure 2 is a simplified schematic diagram.

The sensing elements consist of a row of diffused p-n junction photodiodes spaced on 18 µm centers and interdigitated into a sensing aperture 18 µm wide. Figure 3 gives the aperture response function and sensor geometry where a = 11 µm photodiode diffusion width, b = 18 µm center-to-center spacing, and c = 18 µm aperture width. Light incident on the sensing aperture generates photocurrent which is integrated and stored as a charge on the capacitance of each of the photodiodes. If the charge accumulated on any diode exceeds a saturation value, the antiblooming gates ϕ_{AB} turn on, shunting the excess to the reset drain V_{RD} (see Figure 2) thus reducing blooming effects.

RL 1282D



RL 1284D



RL 1288D

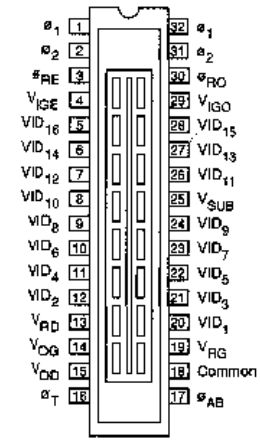


Figure 1. Pinout Configurations

At the end of each integration period, the charges on all the diodes are simultaneously switched through transfer gates, ϕ_T, into CCD analog shift registers for readout. The photodiodes of each 128 element section are divided, with the 64 odd diodes switched into one register and the 64 even diodes into the other. Immediately after this parallel line transfer, a new integration period begins.

Readout for each block is accomplished by clocking the CCD shift registers so that the charge packets are delivered sequentially into two on-chip charge-detection circuits (refer to Figure 5 for timing). The registers deliver the charge packets alternately, allowing the inactive charge detector to be reset to a fixed level of ϕ_{RE} or ϕ_{RO} while the opposite detector is active. The outputs of the two detectors may then be multiplexed off-chip to obtain a stepwise-continuous video signal.

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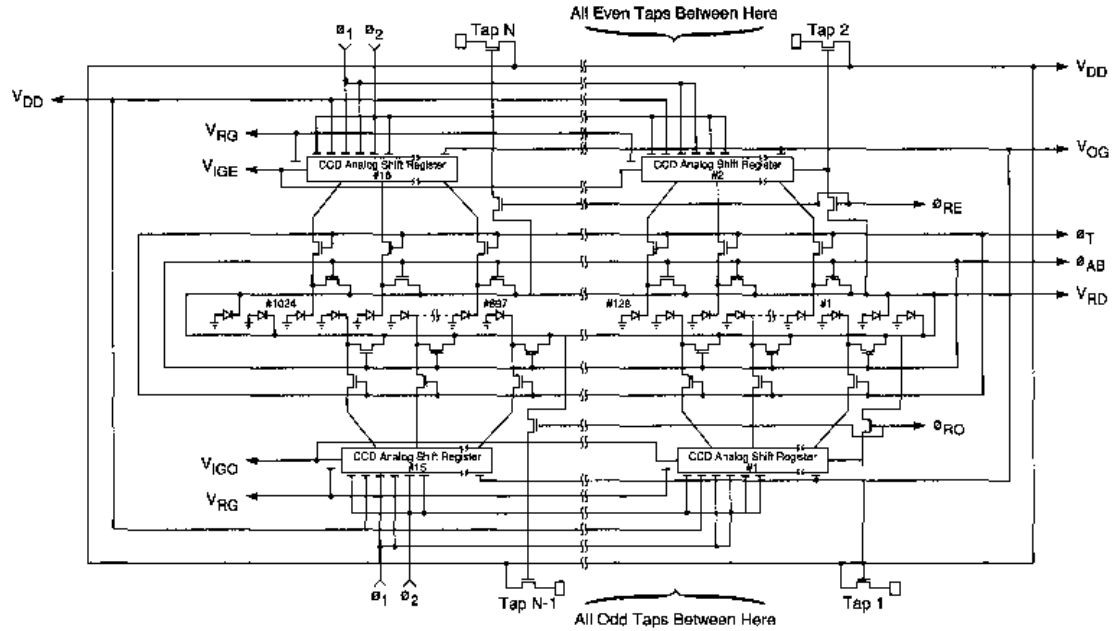


Figure 2. Schematic Diagram

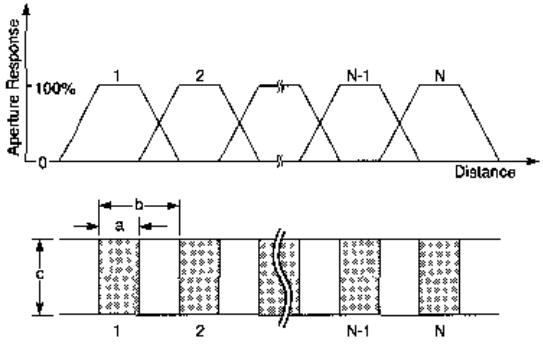


Figure 3. Sensor Geometry and Idealized Aperture Response

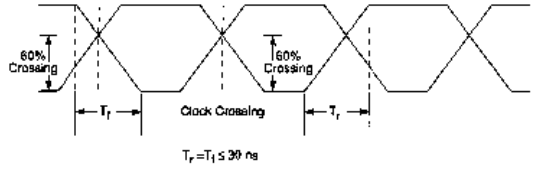


Figure 4. Two-Phase Clocks

Operation

The D Series Tapped arrays require two clock phases, ϕ_1 and ϕ_2, a transfer gate pulse, ϕ_T, and several bias inputs (all voltage references are to common or ground level). The ϕ_1 and ϕ_2 clock waveforms should swing between 0 and +15V. The two-phase clock waveforms are depicted in Figure 4 with waveforms crossing at the 60% amplitude level. The clock crossings must occur at or above 60% (see Figure 4). The ϕ_1 and ϕ_2 clock crossings must occur at or above 60% (see Figure 4). Likewise, the ϕ_1/ϕ_{RO} and ϕ_2/ϕ_{RE} clock crossings must occur at or below 50% for maximum performance. For high-speed operation, the rise and fall should be less than 30 nanoseconds, with no over- or under-shooting on the clock edges.

The transfer pulse, ϕ_T, should swing between -3 and +5V and have a width greater than 0.5 µsec. In order to transfer the charge from the photodiodes into the CCD register, the ϕ_1 clock must remain high during the blanking and transfer interval, as shown in Figure 5. This same figure also shows ϕ_{RE}, the even reset clock, and its relationship to ϕ_1 and ϕ_2 clocks, as well as the odd and even video outputs. The output reset clock, ϕ_{RO}, can be derived from ϕ_2 and the even reset clock, ϕ_{RE}, can be derived from ϕ_1, provided the clock crossing requirements described above are met.

A bias charge level is required in the CCD registers to obtain operation. This charge is supplied by biasing the V_{IGE} and V_{IGO} inputs to the registers with a positive voltage which is nominally set at 8.5V. Also, in order to balance the dc output levels of the two registers, one input level can be adjusted relative to the other. Resistive dividers (potentiometers) may be used since very little current is required.

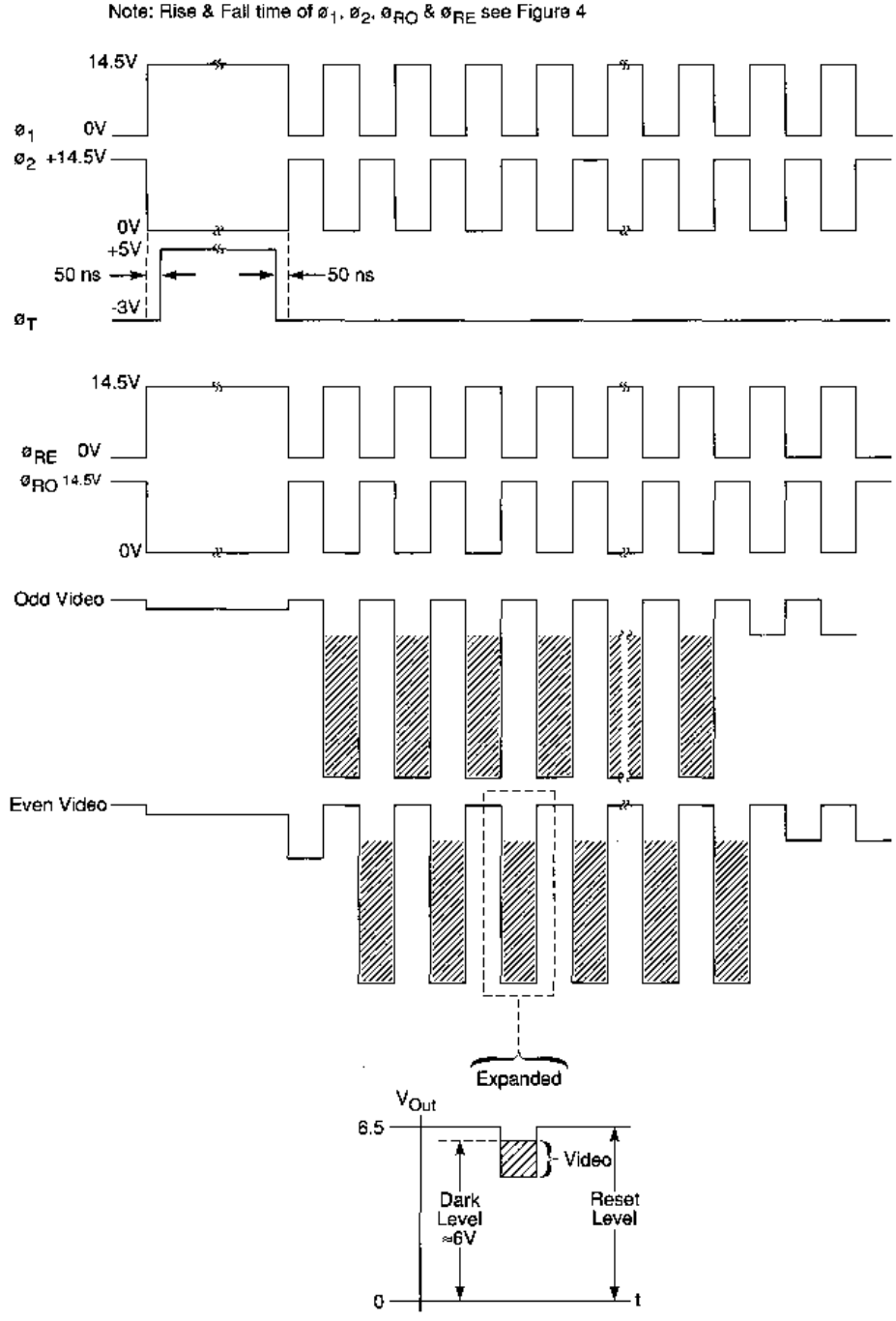


Figure 5. Timing Relationship of the Array's Clocks and Output

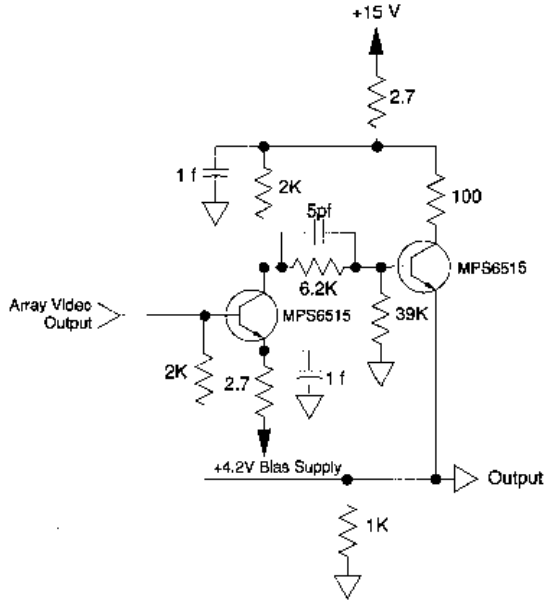


Figure 6. High-speed Video Output Buffer

The optimum output gate bias voltage, V_{OG}, is between 4V and 8.5V and varies from device to device. Since the output gate draws negligible current, it may be biased using a simple resistive voltage divider.

The substrate, V_{SUB}, is held at -5V, the common reference and the antiblooming gate, ϕ_{AB} (if not used), are at ground, and the output amplifier drain, V_{DD}, is at +15V. The V_{RG} gate is used for test purposes at the factory and is normally set at +10V during operation.

The reset drain, V_{RD}, normally is set to 2.5V below V_{DD} (see Table 3). In some applications, it may be desirable to define an integration period shorter than the readout time. This may be accomplished by resetting the diodes with the antiblooming gate. At the desired reset time, ϕ_{AB} is pulsed to +3.5V nominal (2.5 - 4.5V) for at least one µsec and then back to ground. The integration period is then the time between the trailing edge of the ϕ_{AB} pulse and the trailing edge of the next ϕ_T pulse. At low voltages (typically 2-3V), ϕ_{AB} drains off saturation charges. This can be used to eliminate blooming effects. With the output at saturation, ϕ_{AB} is increased from ground until the output voltage begins to decrease. At this point, charge in excess of saturation is shunted to V_{RD}.

A suitable high-speed video output circuit is shown in Figure 6. This circuit is preferable to a 3KΩ load resistor because it reduces the current demand while maintaining speed capabilities.

Performance

Spectral response of the D Series Tapped arrays is similar to that of other high-quality silicon photodetectors, covering the range from near UV to near IR. A quartz window is standard. Relative spectral response is shown as a function of wavelength in Figure 7.

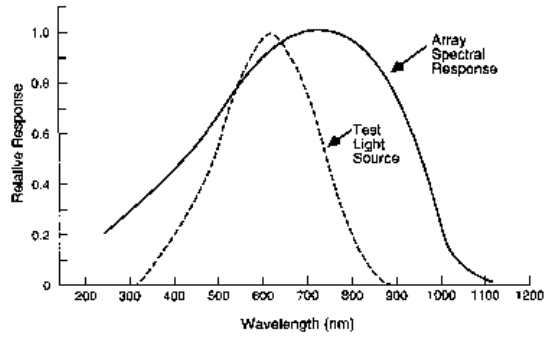


Figure 7. Relative Spectral Response as a Function of Wavelength

As most applications for these devices (OCR, machine vision, etc.) use visible light, the responsivity and uniformity of response are specified using a source with the spectral distribution shown by the dotted line in Figure 7. This spectral distribution is produced by filtering a 2870°K tungsten source with a Fish-Schurman HA-11 heat-absorbing 1 mm thick filter.

Transfer characteristics showing the saturation output voltage can be seen in Figure 8. Since Reticon line scanners operate in the charge-storage mode, the charge output of each diode (below saturation) is proportional to exposure, i.e., the irradiance or light intensity multiplied by the integration time or the time interval between successive transfer pulses.

There is a trade-off between scanning speed and the required light intensity. Light intensity (watts), needed to saturate a pixel at a particular integration time, can be obtained by dividing saturation exposure by integration time. Longer integration times may be used to detect lower light levels. However, this approach is ultimately limited by dark leakage current which is integrated along with the photocurrent.

Video Output waveforms shown in Figure 5 typify video output performance as measured across a 3K load resistor. The rise and fall times are relative since they are affected by capacitive loading, including oscilloscope probe capacitance. For data rates greater than 3 MHz, an output circuit such as Figure 6 is recommended and video rise and fall times of 50 ns or less are typical.

Circuits

A complete evaluation circuit board is available for the D Series Tapped arrays (RL1284 and RL1288, only) and is recommended for first-time evaluation. The RC0716 Board contains all required drive circuitry and has buffered outputs capable of speeds to 10 MHz/tap.

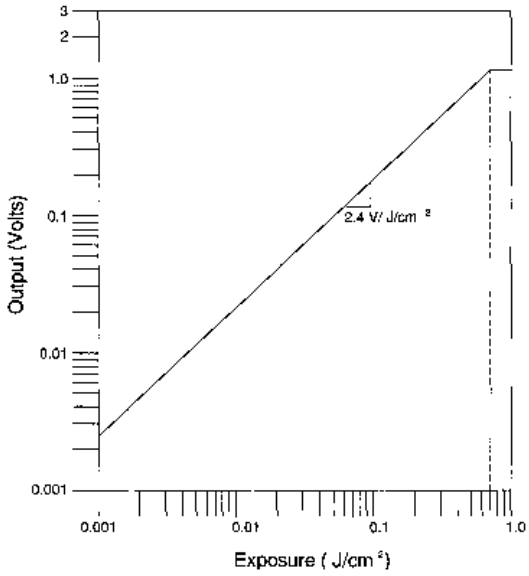


Figure 8. Typical Transfer Characteristic

Table 1. Absolute Maximum Ratings
(Above Which Useful Life May be Impaired)

Storage temperature	-25°C to 100°C
Operating temperature	-25°C to 55°C
Voltage on any pin with respect to substrate	-0.3V to 22V

Table 2. Typical Clock Capacitance *

Clock	Capacitance (pF)		
	RL1282	RL1284	RL1288
$ø_1$	65	137	186
$ø_2$	64	143	183
$ø_2$	65	155	187
$ø_1$	65	120	194
$ø_T$	19	42	56
$ø_{RO}$	7	11	18
$ø_{AB}$	19	19	19
$ø_{RE}$	9	13	19

* Measured with 10V applied to the terminal

Table 3. Drive and Voltage Requirements [1]

Sym	Parameter		Min	Typ	Max	Units
V_{RD}	Reset drain bias [2]		11.5	12.5	13	V
V_{DD}	Output drain bias		14.5	1.5	15.5	V
V_{OG}	Output gate bias [3]		4.0	6.5	8.5	V
V_{IG}	Input gate bias [4]		6	7.8	9	V
$ø_{AB}$	Antiblooming gate [5]		-	0	-	V
V_{SUB}	Substrate bias		-5.25	-5	-4.75	V
$ø_1$, $ø_2$	CCD transport clocks	High	14.5	15	15.5	V
		Low	-0.3	0	+0.5	V
$ø_T$	Transfer clock	High	5	7	15	V
		Low	-5	-3	-2	V
$ø_{RE}$, $ø_{RO}$	Reset - High		14.5	15	15.5	V
$ø_{RE}$, $ø_{RO}$	Clocks - Low		-0.3	0	+0.5	V
V_{RG}	Receive gate		9.5	10	10.5	V
f_{clock}	Video sampling rate [6]			-	15	MHz

Notes:
1. All voltage referenced to COMMON. Use typical values for best performance.
2. Optimum device performance is achieved when V_{RD} is set to 2.5V below V_{DD}.
3. The optimum bias level for V_{OG} varies from device to device.
4. The odd and even input gate biases may be adjusted differentially to achieve an odd/even balance in the video output.
5. See text.
6. Maximum effective array data rate is as follows (15 MHz per video output); RL1282D = 60 MHz; RL1284D = 120 MHz; RL1288D = 240 MHz.

Table 4. Array Performance Characteristics (@ 200 kHz, 25°C)
(Use Typical Voltages shown in Table 3)

Sym	Parameter	Min	Typ	Max	Units
DRFPN	Dynamic range FPN [1,6]	240	1500		-
DRTN	Dynamic range thermal noise [2]	1200	7500		
E_{NE}	Peak-to-peak noise equivalent exposure [3]	-	.0004		$\mu j/cm^2$
E_{SAT}	Saturation exposure [3]	0.45	0.7		$\mu j/cm^2$
	Spectral response range limits	-	0.2-1.1	-	µm
R	Responsivity [3,4]	2.0	2.4	-	V per $\mu j/cm^2$
	Photoresponse nonuniformity:				
	Individual output [3,5,8]		5	10	±%
	Match across array [3,5,7,9]		7	15	%
V_{Dark}	Average dark signal [6]	-	0.5	4	mV
FPN	Fixed pattern noise [6]	-	1	5	mV
V_{Sat}	Saturation output voltage	1.2	1.5	-	V
P	Power dissipation DC [4]	-	600	-	mW
R_O	Output impedance	-	1500	-	Ω
N_{PP}	Peak-to-peak noise [2]		1	5	mV
	Dark level DC mismatch (output to output)		150	400	mV
	Dark level [7]		8.0		V
CTE	Charge transfer efficiency		.99995		

Notes:

1 Dynamic range defined as V_{Sat}/p-p fixed pattern noise

2 Dynamic range defined as V_{Sat}/single pixel rms thermal noise; rms noise is defined as 1/5 of p-p noise

3 Measured using 2870°K light source of Figure 7. Filtered with Fish-Schurman HA-11 heat absorbing filter

4 3KΩ load resistors and V_{DD} = 14.5V

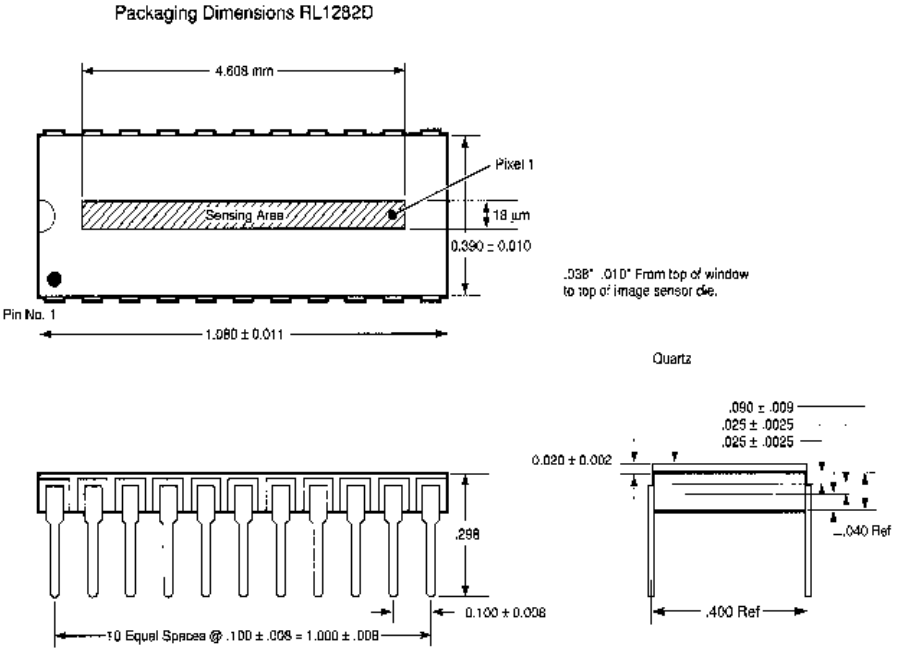
5 Measured with uniform illumination at approximately 50% of saturation

6 At 20°C with 1 msec integration time. Dark signal and dark signal nonuniformity are proportional to integration time, and approximately double for every 7°C increase in temperature

7 See Figure 6 for output schematic

8 Calculated as: + % NU = (Max Diode - Avg./Avg.) x 100
- % NU = (Avg. - Min. Diode/Avg.) x 100

9 Calculated as: X - Y/X where X and Y are the average outputs of any two taps of the array, and X is the output of greater amplitude, output is defined as the difference between the diode dark level and the diode level in the light.



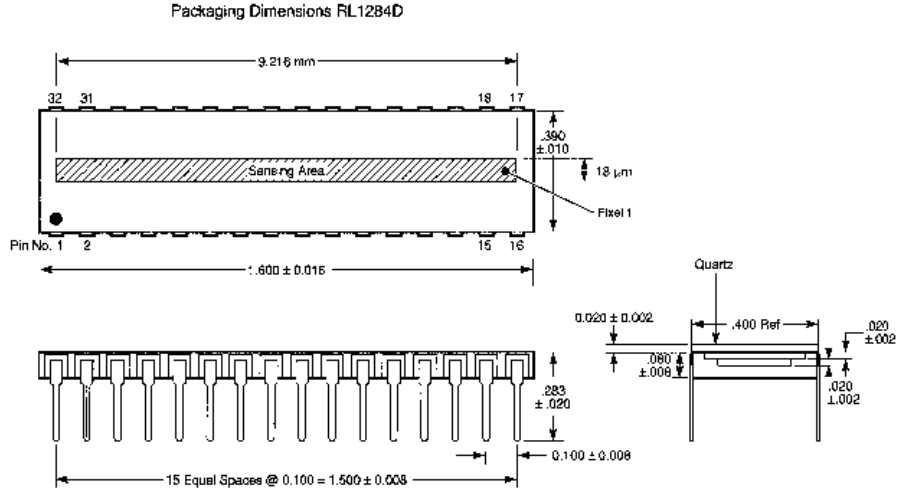


Figure 9. Package Dimensions

Packaging Dimensions RL1288D

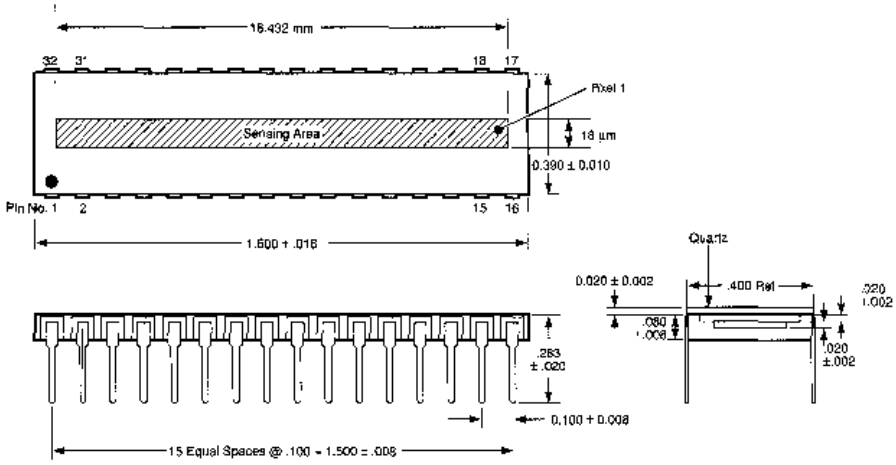


Figure 9. Package Dimensions (Continued)

Ordering Information *

Part Number	Evaluation Board
RL1282DAQ-111	No Board Available
RL1284DAQ-111	RC0716LNB-020
RL1288DAQ-111	RC0716LNB-011

* Includes standard devices. For options, consult EG&G Reticon sales offices.

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Introduction

EG&G Reticon's G Series solid state line scanners are optimized for second-generation solid state image sensor applications. Devices in this series contain 128, 256, 512 or 1024 photodiodes on 25 µm centers (the RL0128G, RL0256G, RL0512G, and RL1024G, respectively). Applications include optical character recognition, pattern recognition, facsimile and noncontact measurement.

Key Features

- On-chip driver and parts of video processing circuit
- Simplicity of use – single-phase TTL clock (open collector TTL or CMOS 5V)
- Several units can be directly cascaded for higher resolution
- Differential output for on-chip noise cancellation
- Charge storage mode operation for high sensitivity
- Standard dual-inline ceramic package with optical window

General Description

The Reticon G series is a family of monolithic self-scanning linear photodiode arrays. The devices in this series consist of a row of silicon photodiodes, each with an associated junction capacitance on which to integrate photocurrent and multiplex switch for periodic readout via an integrated shift register scanning circuit. The shift register clock driver is also integrated so that only a single-phase TTL clock is required for scanning. A row of dummy diodes is read out differentially with the photodiodes to allow cancellation of multiplex switching transients, and to provide a clean video signal with a minimum of external circuitry. The 512 and 1024 devices are designed for low-cost facsimile applications and can easily be cascaded for extremely high resolution by optically dividing the field of view between two or more devices. The 128 and 256 element devices are well suited for OCR applications. Any of these devices may be used for noncontact measurement and inspection depending on the required resolution. Pinout configurations are shown in Figure 1.

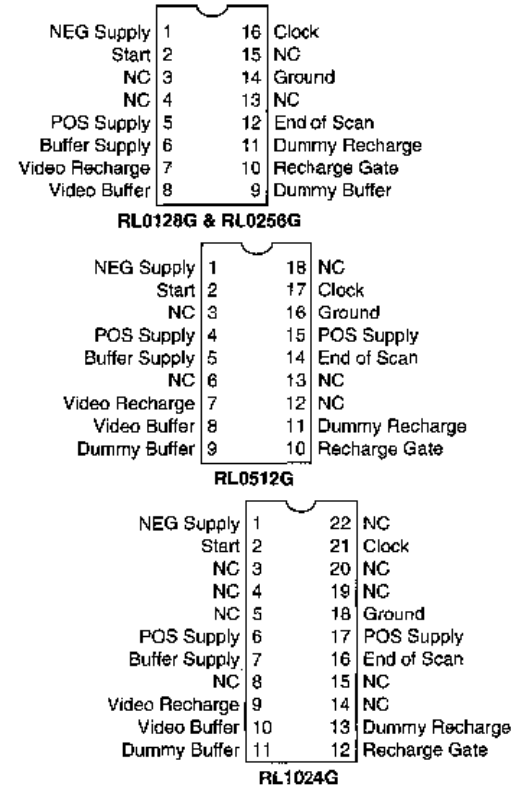


Figure 1. Pinout Configurations

Equivalent Circuit

A greatly simplified equivalent circuit of a G series line scanner is shown in Figure 2 *. Each cell consists of a photodiode and a dummy diode, both with an associated junction capacitance. These diodes are connected through MOS multiplex switches to video and dummy recharge lines which are common to all the cells. The switches are sequentially closed for one clock period by the shift register scanning circuit, thereby recharging each cell to 5V and storing a charge of approximately 3 pC on its capacitance. The scanning circuit is driven by a single-phase TTL clock with a periodic TTL start pulse introduced to initiate each scan. The cell-to-cell sampling rate is the clock frequency, and the total time between line scans is the interval between start pulses. During this line time, the charge stored on each photodiode is gradually removed by photocurrent. The photocurrent is the product of the diode sensitivity and the light intensity or irradiance. The total charge removed from each cell is the product of the photocurrent and the line time. This charge must be replaced through the video line when the diode is sampled and reset once each scan.

* In the schematic diagram of Figure 2, the block labeled "shift register scanning circuit" consists of two two-phase dynamic shift registers and a drive circuit which generates four clock phases and two properly timed start pulses to load the two registers. The individual cells are actually interdigitated with the odd elements being sampled by one register, and the even numbered cells by the other register.

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The part number (RL0128G, etc) indicates the number of diodes in the various devices. The diodes are on 25 µm centers in all cases. The devices are packaged in 16, 18, or 22-pin dual-inline integrated circuit packages with ground and polished optical windows.

In addition to the signal charge, switching transients are capacitively coupled into the video line by multiplex switches. Similar transients are introduced into the dummy line and, therefore, they can be reduced and a cleaner signal recovered by reading out the video and dummy lines differentially.

In many applications, the recharge gate is biased to the negative supply potential and an output signal is obtained simply by differentially amplifying the recharge pulses on the video and dummy recharge lines. However, internal buffer amplifiers are also provided which may be used as part of a sample-and-hold video output circuit.

Sensor Geometry

In G line scanners the light-sensing area is a long, narrow rectangular region defined by an aperture in an opaque mask. Bar-shaped photodiodes extend across the aperture and are connected to the multiplex switches buried under the mask. The entire aperture is photosensitive. Photocurrent generated by light incident between photodiodes will be collected by the nearest diode. Figure 3 shows the aperture geometry along with an idealized response function which would be obtained by scanning a point source of visible light along the length of the aperture.

The dimensions *a*, *b* and *c* indicated in Figure 3 are as follows: the photodiode width *a* is 15 µm, the center-to-center spacing *b* is 25 µm, and the aperture width *c* is 26 µm.

Sensitivity and Spectral Response

The spectral response of the G series devices is similar to that of other high-quality silicon photodetectors, covering the range from the near UV to the near IR. A glass window is standard; however, an optional quartz window is available. Relative spectral response is shown as a function of wavelength in Figure 4. Note that relatively high sensitivity is maintained even in the blue end of the spectrum because there is no interfering structure covering the diode. As most applications for these devices (OCR, fax, etc.) utilize visible light, the sensitivity and uniformity of response are specified using a source with the spectral distribution shown by the dotted line in Figure 4. This spectral distribution is produced by filtering a 2870°K tungsten source with a Fish-Schurman HA-11 heat absorbing filter 1 mm thick.

Since Reticon line scanners operate in the charge storage mode, the charge output of each diode (below saturation) is proportional to exposure, i.e., the irradiance or light intensity multiplied by the integration time or the time interval between successive start pulses. Thus, there is an obvious trade-off between scanning speed and the required light intensity. A plot of charge output versus exposure is shown in Figure 5 for the light source of Figure 4.

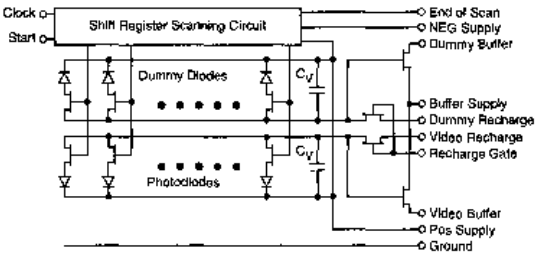


Figure 2. Simplified Equivalent Circuit

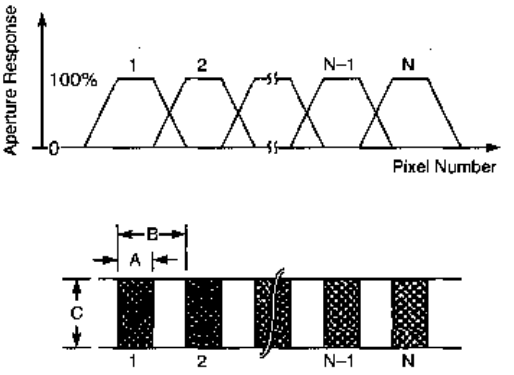


Figure 3. Sensor Geometry and Idealized Aperture Response Function

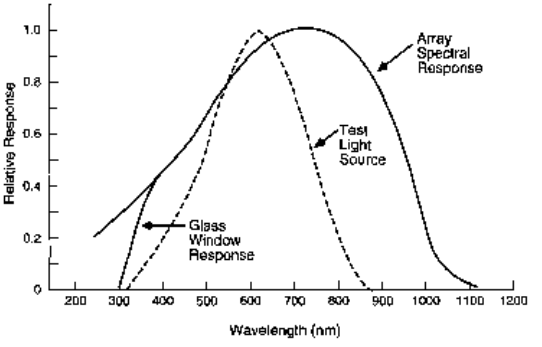


Figure 4. Relative Spectral Response as a Function of Wavelength. Dotted line shows spectral distribution of light source used for sensitivity measurements. Quartz and glass windows have similar response except the glass window will fall off at approximately 300 nm as shown above

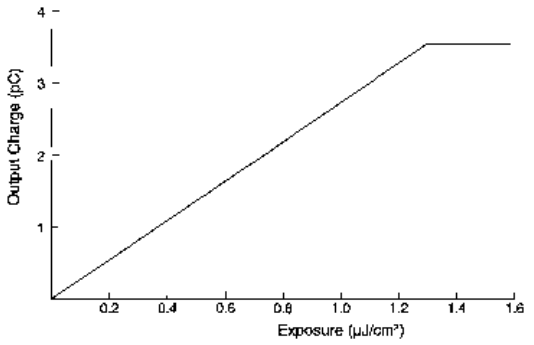


Figure 5. Signal Charge per Cell as a Function of Exposure (Light Intensity x Line Scan Time)

Uniformity of response along the length of a photodiode array is a function of wavelength. Devices tend to be less uniform at long wavelengths (IR) and more uniform at short wavelengths (visible). The nonuniformity specifications of the G series are based on the light source of Figure 4.

Dark Response and Dynamic Range

There are three components to the dark output signal from a Reticon line scanner: (1) the integrated dark leakage current, (2) the fixed pattern noise caused by incomplete cancellation of clock switching transients which are capacitively coupled into the video line, and (3) the random pixel noise.

The dark leakage current will vary from element to element but is typically less than 2 pA at room temperature. Assuming this value, leakage current would contribute an output charge of 2 pC with a 1 sec line time or .08 pC with a 40 ms line time. Thus, since the saturation charge is typically 4 pC, dark current will contribute about 2% of the saturated output signal for t_L = 40 ms, 0.2% for t_L = 4 ms, and so on. The dark current is a very strong function of temperature, approximately doubling for every 7°C increase of photodiode temperature. Thus, the maximum allowable line time becomes correspondingly shorter at high temperatures, and longer at low temperatures. An important feature of the G device design is low power dissipation which means that self-heating is negligible. Dark current does not become a limiting factor in the dynamic range unless very long integration times or highly elevated temperatures are used.

The switching noise appears as a fixed pattern which is spatially random except that it may have a slight 1, 2, 3, 4 pattern because alternate diodes are sampled on different phases of an internally-generated, four-phase clock. Fixed pattern noise is largely removed by differential readout; its residual amplitude will typically be 1% of the saturation level.

Pixel noise is the random, nonrepetitive fluctuations which are superimposed on the dark level and is the ultimate limiting noise which cannot be removed by signal processing. Its rms value will generally be amplifier limited at a value less than about 0.1% of the saturation level, depending on the noise bandwidth and preamplifier used.

The dynamic range that can be achieved depends on circuit complexity and layout techniques. Care must be exercised in circuit layout to provide for adequate ground plane, circuit decoupling, and avoidance of electrostatic pickup.

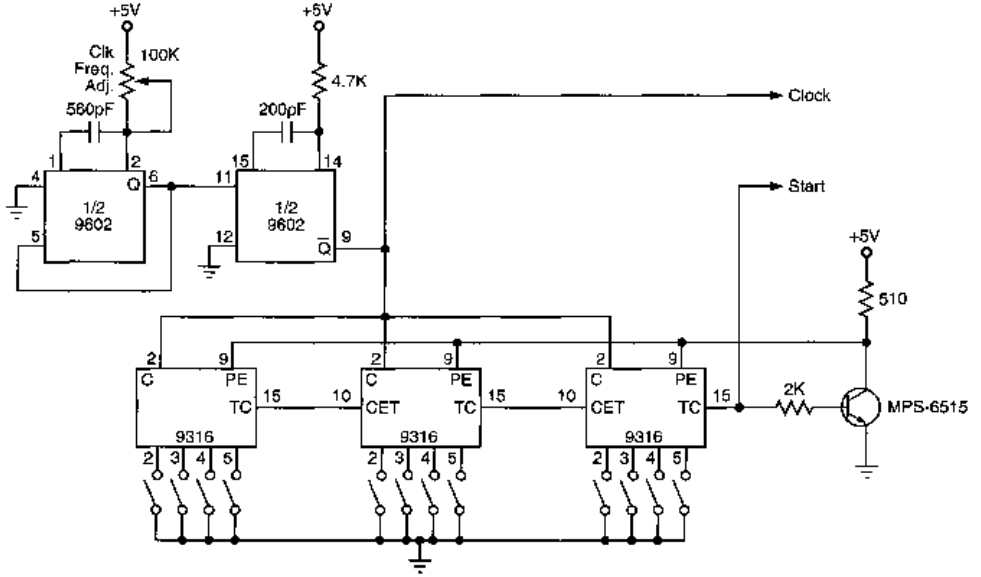


Figure 6. Clock and Counter Circuit Suitable for Generating TTL Clock and Start Pulses. The number of clock periods between start pulses may be set at any value up to 4096 by setting the switches

Drive Requirements

Two power supplies to the array are required—nominally +5 and -10V. The clock and start timing signals may be at TTL level, and may be supplied from other parts of the system or generated by using a simple circuit such as that shown in Figure 6. In this circuit, the start pulse is obtained by counting clock pulses. By setting the appropriate switches, the number of clock periods, n, between start pulses may be set at any desired value greater than or equal to N, the number of elements in the array. However, the total time between start pulses $t_L = n/f_S$ should not exceed approximately 40 ms (at room temperature) to prevent integrated dark current from making a significant contribution to the output charge.

A timing diagram showing the relationship between the clock and start pulses and the video and end-of-line outputs is shown in Figure 7.

Signal Extraction

The video output of the G devices is a train of N charge pulses flowing onto the video recharge line and dummy recharge line capacitances during each scan, with timing as shown in Figure 7. The pulses on the dummy line contain switching transients only; those on the video line contain switching transients plus the video signal. An output circuit is required which is capable of differentially amplifying these pulses to a useable voltage level. Two types of amplifier circuits are in common use: (1) a simple differential current amplifier, and (2) a video line integration, sample-and-hold circuit. The former has a pulse output while the latter has a boxcar output waveform.

Current Amplifier

A simple differential current amplifier circuit is shown in Figure 8. The same circuit can be used on all G series devices. In this mode of operation, the recharge gate is biased ON by connecting it to the negative supply and the signal is obtained through the video dummy and recharge lines. The unused buffer amplifiers are biased OFF by connecting all pins to the positive supply. An example of the video output of the circuit of Figure 8 is shown in the oscilloscope photograph of Figure 9.

Integrate, Sample-and-Hold Amplifier

A simple buffer mode operation circuit and its associated timing diagram are shown in Figure 10a and 10b. This alternative signal processing scheme makes use of the internal buffer amplifiers and recharge switches. Immediately after the multiplex switch is closed to sample a diode, the voltage change on the video line is sensed through the buffer amplifier, and sampled and held. The recharge gate is then pulsed negative to reset the video line before the next diode is sampled. The result is a sampled-and-held boxcar video signal such as that shown in Figure 11.

End-of-Scan

An output pulse is provided when the next-to-last element is sampled by the shift register scanning circuit. This end-of-scan output is provided primarily for test purposes. When not in use, it should be connected to the positive supply to avoid introduction of unwanted "glitches" into the video. In some applications, however, it may be desirable to use the end-of-scan output. In these cases, it is recommended that the voltage excursion on the end-of-scan terminal be minimized by using a circuit such as that shown in Figure 12. This figure shows a common application in which the end-of-scan output of one array is used to generate the start pulse for a second array. The timing is such that the last element of the first array and the first element of the second array are sampled on successive clock pulses.

Circuit Cards

Printed circuit cards containing all required drive and amplifier circuitry for operating G series self-scanning photodiode arrays are available from Reticon. These circuits are highly recommended for first-time array evaluation. In many cases they are also useful for design into final equipment.

Two families of circuit cards are available, corresponding to the two amplifier configurations described earlier. Both circuits are complete except for power supplies and have the flexibility to operate over a wide range of scan rates and integration times.

RC0300 Series. These boards incorporate the clock and counter circuit of Figure 6 and the amplifier circuit of Figure 8. They provide a pulse type output such as that shown in Figure 9 and give good performance at lowest cost. The boards are 3 inches square and have mounting holes in each corner on 2.6-inch centers.

RC0100 Series. These circuits provide an integrated, sampled-and-held boxcar output such as that shown in Figure 11. They are recommended for high-performance applications which require this type of output waveform. Each circuit is divided into two boards—a standard "motherboard", which contains most of the circuitry, and a small "array board", which contains only those components which must be located close to the array. The array board may be plugged directly into the motherboard or can be extended up to 30 inches away via an optional ribbon cable.

The motherboard (RC0100LNB) is 4.5 x 6.4 inches in size and is terminated by a standard 22-pin edge connector. The array boards (RC0104L) are 3 inches square and have mounting holes in each corner on 2.6-inch centers. A different array board is required for each array type.

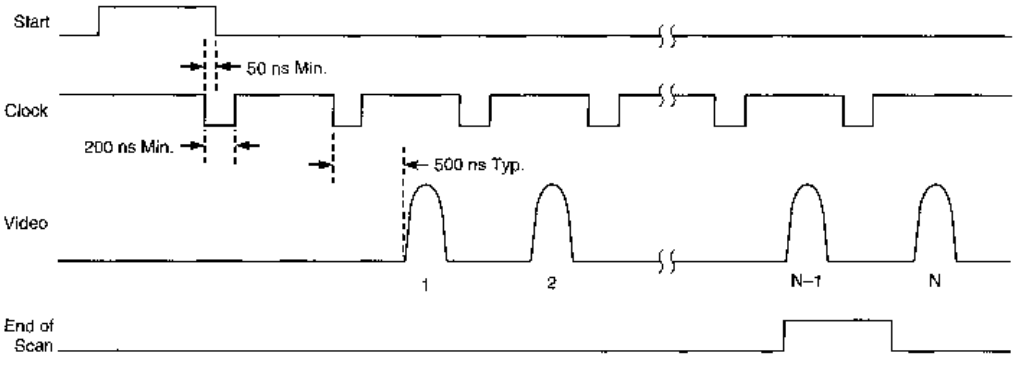


Figure 7. Timing Diagram Showing Relationship of Clock and Start Inputs to Video and End-of-Scan Outputs

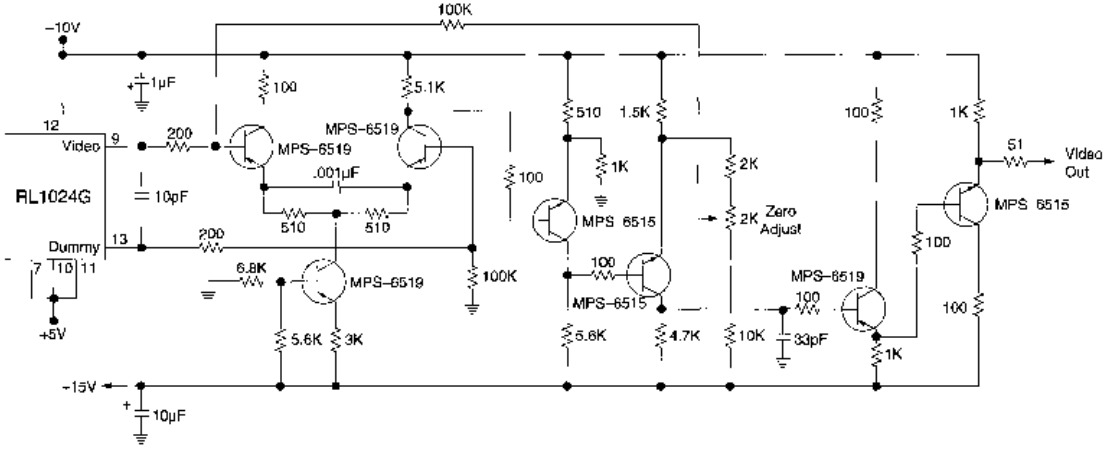


Figure 8. Differential Current Amplifier Circuit for RL1024G

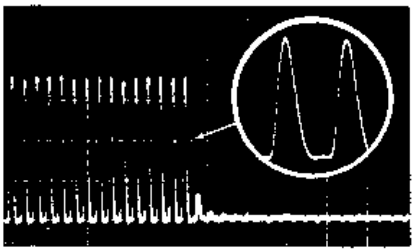


Figure 9. Oscilloscope Photograph Showing Video Output of Circuit of Figure 8

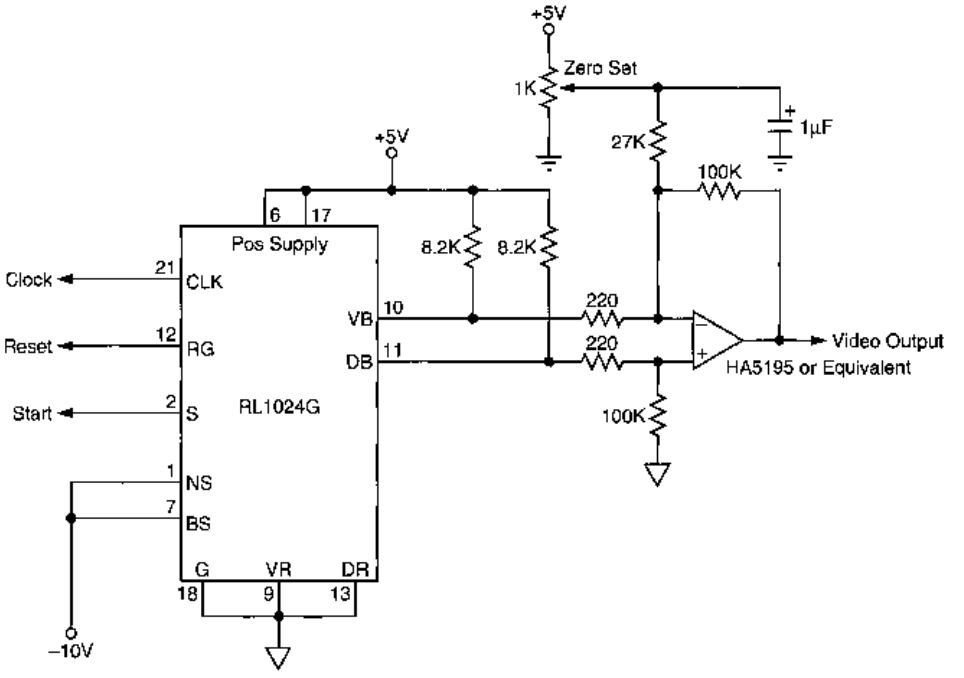


Figure 10a. Buffer Mode Operation Simplified Diagram

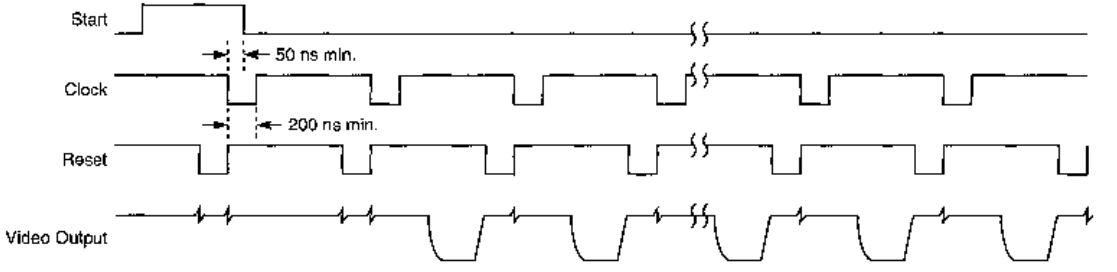


Figure 10b. Buffer Mode Timing Diagram



Figure 11. Oscilloscope Photograph Showing Video Output of Integrate, Sample-and-Hold Amplifier

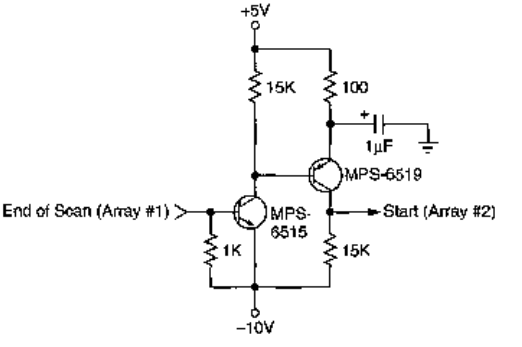


Figure 12. End-of-Scan Output Circuit Suitable for Generating Start Pulse for a Second Array

Table 1. Electrical Characteristics (25°C)

	Min	Typ	Max	Units
Positive supply voltage V_P [1]	+4.5	+5	+5.5	V
Negative supply voltage V_n	-10.5	-10	-9.5	V
Clock voltage low V_{CL}	-10.5	0	+1	V
Clock voltage high V_{CH}	V_P-1	+5	V_P	V
Start voltage low V_{SL}	-10.5	0	+1	V
Start voltage high V_{SH}	V_P-1	+5	V_P	V
Recharge gate voltage low V_{RL}	-10.5	-10	-9.5	V
Recharge gate voltage high V_{RH}	V_P-1	+5	V_P	V
Clock pulse width	0.2	-	-	µs
Start pulse width	See Figure 7			
Clock frequency f_c	-	-	1	MHz
Integration time t_i [3]	-	-	40	ms
Clock input capacitance C_{C_2} [2]	-	4	-	pF
Start input capacitance C_S [2]	-	4	-	pF
Video line capacitance C_V [2]				
RL0128G	-	8	-	pF
RL0256G	-	12	-	pF
RL0512G	-	20	-	pF
RL1024G	-	30	-	pF
End-of-scan output resistance	-	5	-	KΩ
DC power dissipation [4]	-	45	-	mW

Test Conditions:

A. Typical supply parameters used
B. Light source of Figure 4
C. Clock frequency = 500 kHz
D. RC0100L series circuit used

Notes:
1 No terminal should ever be allowed to go more positive than V_P
2 Measured with nominal power supply voltages
3 Integration time can be longer if the array is cooled and/or if the application can tolerate a larger percentage of dark signal
4 Mostly due to use of on-chip buffers. When recharge mode is used (buffers biased off), power dissipation is on the order of 1 mW

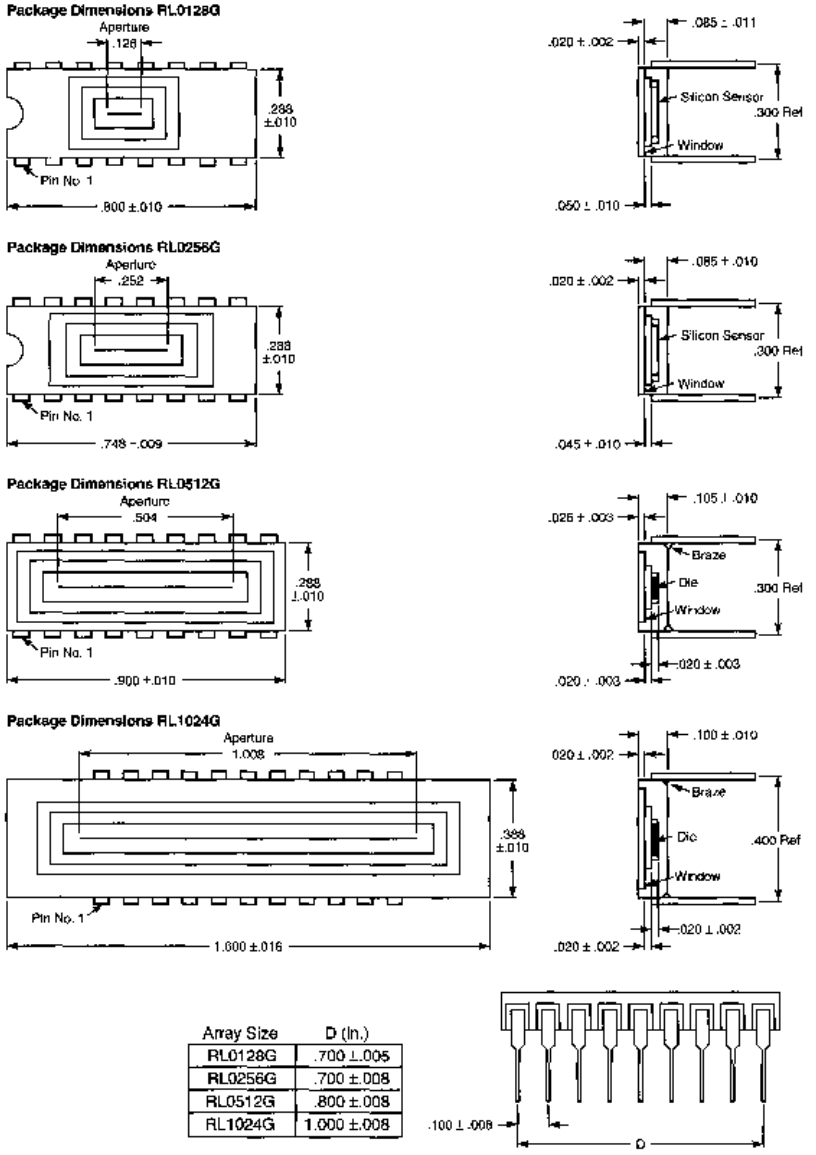
Table 2. Electro-Optical Characteristics (25°C)

	Min	Typ	Max	Units
Diode center-to-center spacing	-	25	-	µm
Diode aperture width	-	26	-	µm
Photodiode sensitivity [1]	-	2.5	-	pC/µJ/cm^2
Nonuniformity of sensitivity [1]				
RL0128G	-	7	10	±%
RL0256G	-	7	10	±%
RL0512G	-	9	11	±%
RL1024G	-	12	14	±%
Saturation exposure [1]	-	1.8	-	µJ/cm^2
Saturation charge	-	4	-	pC

Note:
1 Measured using light source of Figure 4 neglecting first 2 and last 2 diodes

Absolute Maximum Ratings

	Min	Max	Units
Voltage on any terminal	V_P-20	V_P	V
Storage temperature	-55	+125	°C
Temperature under bias	-55	+85	°C



Array Size	D (in.)
RL0128G	.700 ±.005
RL0256G	.700 ±.008
RL0512G	.800 ±.008
RL1024G	1.000 ±.008

Figure 13. Package Dimensions

Ordering Information *

Ordering No.	Current Amplifier	Evaluation Circuit Integrate, S/H Amplifier
RL0128GAG-011	RC0301LNN	RC0100LNB-011/RC0104LNN-011
RL0256GAG-011	RC0301LNN	RC0100LNB-011/RC0104LNN-011
RL0512GAG-011	RC0302LNN	RC0100LNB-011/RC0105LNN-011
RL1024GAG-011	RC0303LNN	RC0100LNB-011/RC0106LNN-011

* Includes standard devices. For options, consult your local sales offices.

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The Reticon H Series devices are high-resolution solid state image sensors designed specifically for facsimile and related applications. These monolithic silicon integrated circuits contain a row of 1024, 1728 or 2048 photodiodes on 15 µm centers, together with shift register scanning circuits for sequential readout. The RL1728H and RL2048H allow high-resolution facsimile using only a single device to read a full 8.5-inch page width. The RL1024H may be used for lower resolution requirements.

Key Features:

- High resolution–up to 2048 elements on 15 µm centers
- Internal scanning for serial video output
- Differential output to reduce fixed-pattern noise
- Charge storage mode operation for high sensitivity
- Requires only simple external circuitry using standard components
- Standard dual-inline package with optical window

General Description

The Reticon H series is a family of monolithic self-scanning linear photodiode arrays. The devices in this series consist of a row of silicon photodiodes, each with an associated junction capacitance and multiplex switch for periodic readout via an integrated shift register scanning circuit. The part number of each device indicates the number of elements in the array (e.g., 1024 or 1728). H series devices have elements on 15 µm (0.59 mil) centers. The sensing area is defined by an aperture which is 16 µm wide and runs the full length of the array.

The devices are packaged in 18- or 22-lead dual-inline integrated circuit packages with ground and polished optical windows. Pin configurations for the H devices are shown in Figure 1 and package dimensions are shown in Figure 12.

Equivalent Circuit

A simplified equivalent circuit of an H series line scanner is shown in Figure 2. Each cell consists of a photosensor and is connected through an MOS transistor switch to a common video output line. The switches are turned on and off in sequence by the shift register multiplexing circuits, thereby periodically recharging each cell to 5V and storing approximately 2.2 pC on its intrinsic junction capacitance. The multiplexing circuits are driven by six clock phases which are easily generated from a TTL master clock which sets the cell-to-cell sampling rate. During the line scan time, the charge on each junction capacitance is gradually removed by the reverse current flowing in the photodiode.

The reverse current is made up of two components: the photocurrent and the dark leakage current. The photocurrent is proportional to the light intensity or irradiance. During a line scan time, the charge removed from each cell is the product of the photocurrent and the line time. This charge must be replaced through the video line when the diode is sampled once each scan. Thus, the output signal obtained from each scan of an N element array is a train of N charge pulses each proportional to the light exposure on the corresponding photodiode.

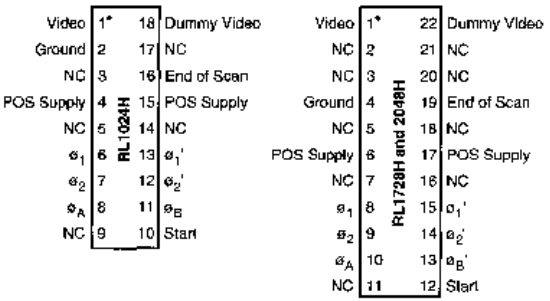


Figure 1. Pin Configuration

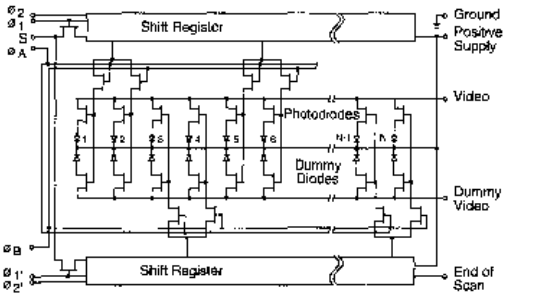


Figure 2. Equivalent Circuit

The H series devices also contain a row of dark dummy diodes which are in one-to-one correspondence with the sensing diodes. By sampling the sensing diodes and the dark diodes differentially, switching transients associated with the multiplex switches are reduced. This gives a high quality video signal with a minimum of external circuitry.

Sensor Geometry

In the H series line scanners the light sensing area is a long, narrow rectangular region defined by an aperture in an opaque mask. Bar-shaped photodiodes extend across the aperture and are connected to the multiplex switches buried under the mask. The entire aperture is photosensitive; photocurrent generated by light incident between the photodiodes will be collected by the nearest diode. Figure 3 shows the aperture geometry and an idealized response function which would be obtained by scanning a point source of visible light along the length of the aperture.

The dimensions *a*, *b*, and *c* indicated in Figure 3 are as follows: the photodiode width *a* is 7 µm, the photodiode spacing *b* is 15 µm and the aperture width *c* is 16 µm. Wide aperture H Series devices with dimensions *c* = 300 µm are available in 1024 and 2048 elements. They are the RL1024HDQ and RL2048HDQ, respectively.

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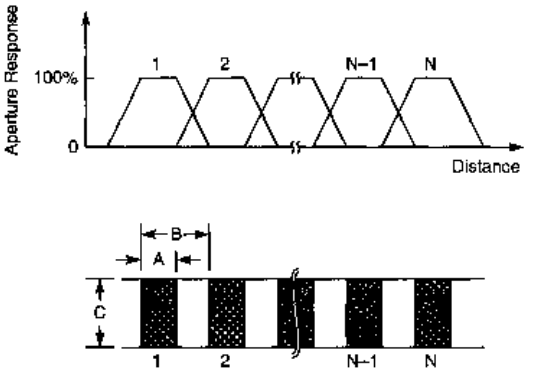


Figure 3. Sensor Geometry and Idealized Aperture Response Function

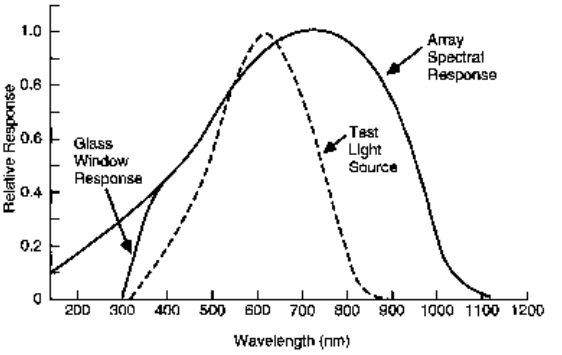


Figure 4. Relative Spectral Response as a Function of Wavelength. Dotted Line Shows Spectral Distribution of Light Source Used for Sensitivity Measurements. Quartz and Glass Windows Have Similar Response Except the Glass Window will Fall Off at Approximately 300 nm as Shown Above.

Sensitivity and Spectral Response

The spectral response of the H series devices is similar to that of other high quality silicon photodetectors, covering the range from the near UV to the near IR. A glass window is standard for arrays with a 16 µm aperture while arrays with the 300 µm aperture have a quartz window. Relative spectral response is shown as a function of wavelength in Figure 4. Note that relatively high responsivity is maintained even in the blue end of the spectrum because there is no interfering structure covering the diode. As most facsimile related applications for these devices use visible light, sensitivity and uniformity of response are specified using a source with the spectral distribution shown in the dotted line of Figure 4. This spectral distribution is produced by filtering a 2870°K tungsten source with a Fish Schurman HA-11 heat absorbing, 1 mm thick filter.

Since Reticon line scanners operate in the charge storage mode, the charge output of each diode (below saturation) is proportional to exposure, i.e., the irradiance or light intensity multiplied by the integration time or the time interval between successive start pulses. Thus there is an obvious trade-off between scanning speed and the required light intensity. Plots of charge output versus exposure are shown in Figure 5 for the light source of Figure 4 and the amplifier circuit of Figure 8.

Uniformity of response along the length of a photodiode array is a function of wavelength. Devices tend to be less uniform at long wavelengths (IR) and more uniform at short wavelengths (visible). The nonuniformity specifications of the H series are based on the light source of Figure 4.

Dark Response and Dynamic Range

There are three components to the dark output signal from a Reticon H series line scanner: (1) the integrated dark leakage current, (2) the fixed pattern caused by incomplete cancellation of clock switching transients between the sensing and dummy diodes, and (3) the random pixel noise.

The dark leakage current will vary significantly from element to element but is typically 1.0 pA per diode at room temperature. Thus, dark current will contribute about 2% of the saturated output signal for t_L = 40 msec, 0.2% for t_L = 4 msec, and so on.

The dark current is a very strong function of temperature, approximately doubling every 7°C. Thus, the maximum allowable line time becomes correspondingly shorter at high temperatures and longer at low temperatures. An important feature of these devices is the low power dissipation, which means that self-heating is negligible.

The switching transients are very nearly cancelled by the differential output. Residual uncancelled transients will result in a fixed pattern which is about 1% of the saturated output signal for unprocessed video.

Pixel noise is the random, nonrepetitive fluctuations which are superimposed on the dark level, and is the ultimate limiting noise which cannot be removed by signal processing. Its rms value will generally be amplifier limited at a value less than 0.1% of the saturation level, depending on the noise bandwidth and preamplifier used.

The dynamic range that can be achieved is circuit dependent. Care must be exercised in circuit layout to provide for adequate ground plane, circuit decoupling, and avoidance of electrostatic pickup. The typical dynamic range for the RL1728H array operating in the RC1728H/LN low noise evaluation circuit is 375:1 when measured as a ratio of the saturation output to the peak to peak dark fixed pattern. The typical dynamic range is 3000:1 when the saturation level is compared to the rms noise on each pixel.

Drive Requirements

Six clock phases are required to drive the H series devices and a properly timed start pulse is required to initiate each scan. Figure 6 shows the proper timing of the input clock and start signals. Note that ϕ_1 and ϕ_2, and ϕ'_1 and ϕ'_2 are two pairs of complementary square waves. The ϕ_A and ϕ_B clocks are complementary, but are not square waves. Diodes are sampled on the negative going transitions of ϕ_2, ϕ_B, ϕ'_2, ϕ_B, ϕ_1, ϕ_B, ϕ'_1. The start pulse timing is noncritical except that it must be negative for one positive going transition of ϕ_1 and the following positive going transition of ϕ'_1. The number of master clock periods n between start pulses is arbitrary except that it must be equal to or greater than N when N is the number of elements in the array.

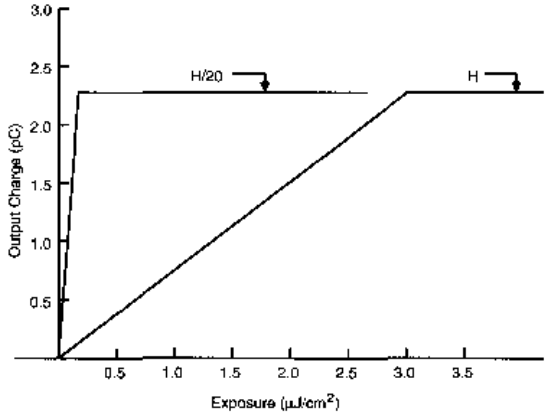


Figure 5. Signal Charge Per Cell as a Function of Exposure for Light Source of Figure 4

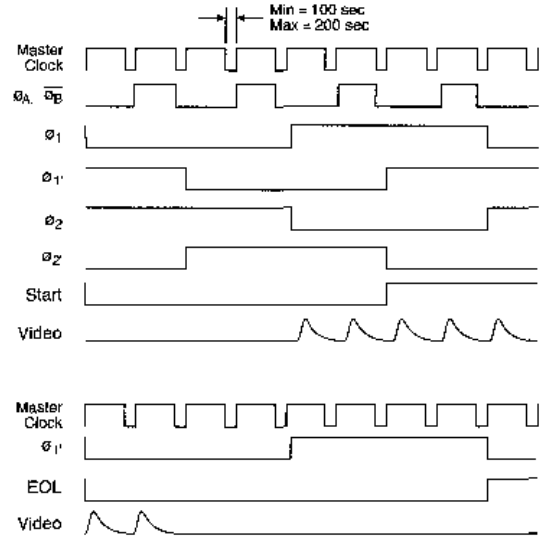


Figure 6. Timing Diagram

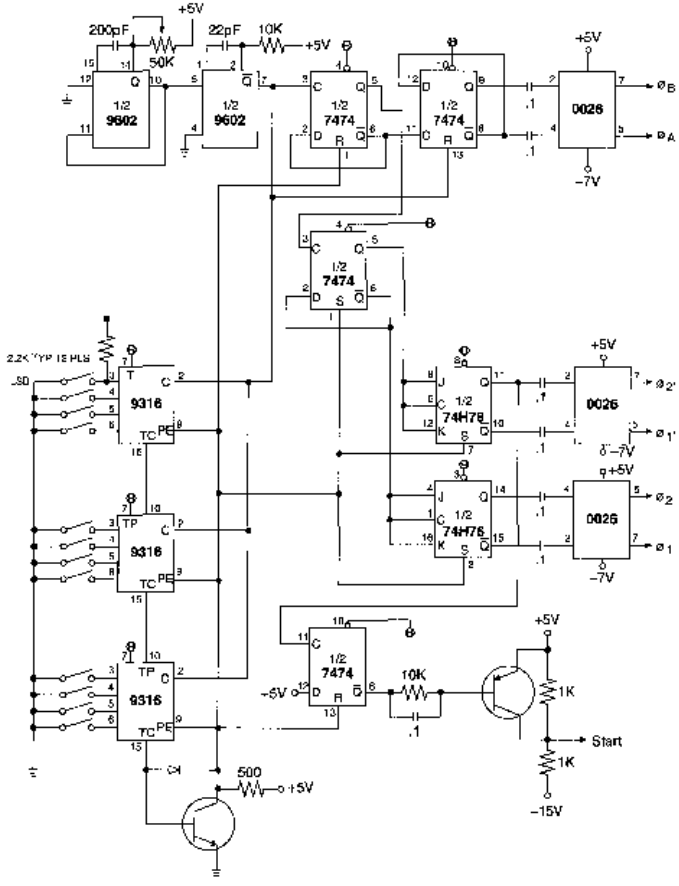


Figure 7. Suggested Drive Circuit

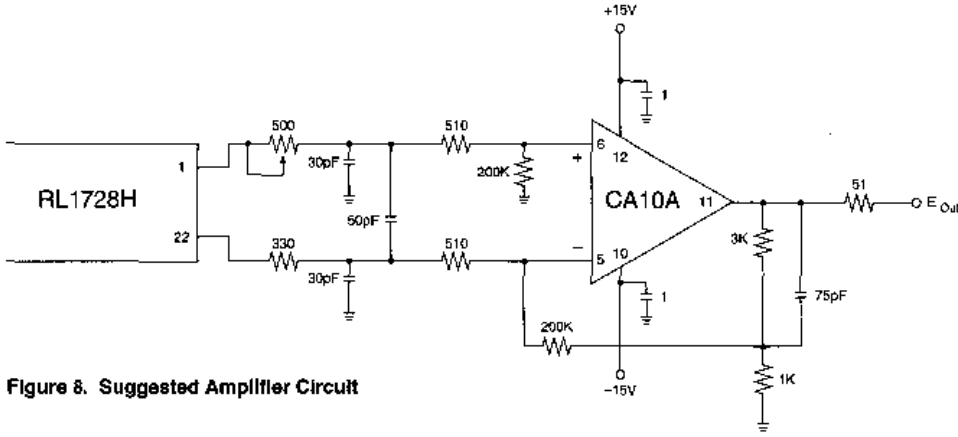


Figure 8. Suggested Amplifier Circuit

A suitable drive circuit for the H series devices is shown in Figure 7. The start count n may be set at any value up to 4096 by closing the appropriate set of switches on the 9316 counters.

Signal Extraction

The video output of the H series devices is a train of N charge pulses flowing onto the video line capacitance during each scan with timing as shown in Figure 6. Superimposed on the video signal are periodic switching transients which are introduced by the multiplex circuitry. Since similar transients also appear without the signal on the dummy video line, the two outputs may be amplified differentially to obtain a cleaner video signal. Two types of amplifier circuits are in common use: (1) a simple differential current amplifier; and (2) a video line integration, sample-and-hold circuit. The former has a pulse output while the latter has a boxcar output with greater signal to noise ratio.

Current Amplifier–Circuit Card RC1024L and RC1728L

These circuit boards, available from Reticon, incorporate the drive of Figure 7 and the amplifier circuit as shown in Figure 8 (using the Reticon CA10A op amp connected as a differential amplifier). They provide a pulse type video output as shown in the oscilloscope photograph of Figure 9.

Integrate, Sample-and-Hold Amplifier–Circuit Card RC0100L Series

In this alternative signal processing scheme, the output charge pulses are integrated on the video and dummy line capacitances. The voltage change on these output lines is then amplified differentially, and sampled-and-held for one master clock period. After sampling, the output lines are reset to integrate the next charge pulse. The result is a sampled-and-held-boxcar video signal such as that shown in Figure 10.

The RC0100L circuit cards are recommended for high performance applications which require this output waveform.

Circuit cards are highly recommended for first-time array evaluation. In many cases they are also useful for design into final equipment. They contain all required drive and amplification circuitry for operation of the H arrays. These circuits, complete except for power supplies, have the flexibility to operate over a wide range of scan rates and integration times.

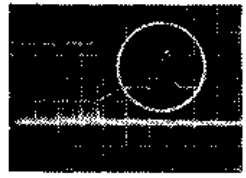


Figure 9. Oscilloscope Photograph showing Video Output of Figure 8



Figure 10. Oscilloscope Photograph showing Sampled-and-Held Boxcar Video Signal

End-of-Scan Output

An end-of-scan output pulse is provided when the last two diodes are sampled. This end-of-scan output is provided primarily for test purposes and, if not in use, it should be shorted externally to the +5V supply. In those cases where the end-of-scan pulse is used, the voltage excursion of the end-of-scan pin should be minimized by using a circuit such as that shown in Figure 11. The timing of the end-of-scan output is shown in Figure 6.

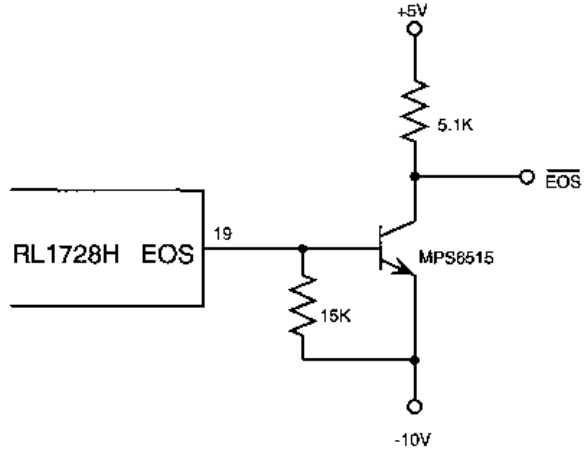


Figure 11. Suggested End-of-Scan Output Circuit

Table 1. Electrical Characteristics (25°C)

	Min	Typ	Max	Units
Positive supply voltage V_P [1]	4.5	5	5.5	V
Clock voltage high V_{CH}	V_P-1	5	V_P	V
Clock voltage low V_{CL}	-7.5	-7	-6.5	V
Start voltage high V_{SH}	V_P-1	5	V_P	V
Start voltage low V_{SL}	-7.5	-7	-5	V
Sample frequency f_S			3	MHz
Clock input capacitance [2] (Phases 1, 1', 2, 2')				
RL2048H		65		pF
RL1728H		60		pF
RL1024H		35		pF
Clock input capacitance [2] (Phases A, B)				
RL2048H		140		pF
RL1728H		125		pF
RL1024H		75		pF
Video line capacitance C_V [2] (Active and dummy)				
RL2048H		70		pF
RL1728H		60		pF
RL1024H		35		pF
End-of-scan output resistance		5		KΩ

Additional test conditions: drive and amplifier circuits as shown in Figures 7 and 8 at 600 kHz sample rate

Notes:
1 No terminal should ever be allowed to go more positive than Vp
2 Capacitance measured at 5V bias

Table 2. Electro-optional Characteristics (25°C)

	Typ	Max	Units
Number of sensors			
RL1024H, H/20	1024		
RL1728H	1728		
RL2048H, H/20	2048		
Center-to-center spacing	15		µm
Aperture length			
RL1024H, H/20	1.536		cm
RL1728H	2.592		cm
RL2048H, H/20	3.072		cm
Aperture width			
H	16		µm
H/20	300		µm
Sensitivity [1]			
H	.8		pA/µW/cm^2
H/20	12.0		pA/µW/cm^2
Nonuniformity of sensitivity *[1,2,4,5]			
H, H/20	10	15	±%
Saturation exposure [1]			
H	3.0		µJ/cm^2
H/20	.2		µJ/cm^2
Saturation charge			
H, H/20	2.2		pC
Dynamic range [3]			
H, H/20	375		
Average dark leakage [2,4]		4	%

* Nonuniformity is ±11% maximum on 1024 arrays, ±15% maximum on all others.

Additional test conditions: drive and amplifier circuits as shown in Figures 7 and 8 at 600 kHz sample rate

Notes:
1 Specified for light source of Figure 4
2 Neglecting first 4 and last 4 diodes
3 RL1728H measured in RC1728H/LN circuit board at 1 MHz scan rate neglecting first 4 and last 4 diodes. Dynamic range is defined as the ratio of saturation signal to peak fixed pattern noise in the dark.
4 % of saturated output at 40 ms integration time at 25°C
5 Clock crossing 75%, rise and fall time 10 ns to 100 ns

Absolute Maximum Ratings

	Min	Max	Units
Voltage on any terminal	V_P-20	V_P	V
Storage temperature	-55	+125	°C
Temperature under bias	-55	+85	°C

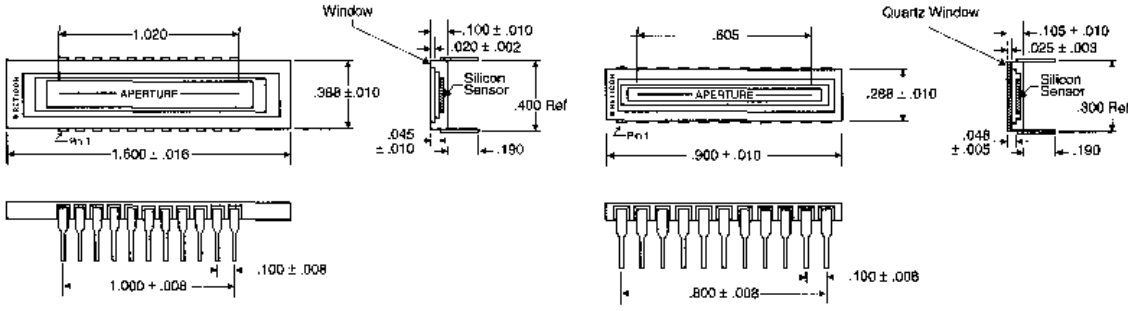


Figure 12. Packaging Dimensions of RL1728H (Left) and RL1024H (Right). The RL2048H is similar to the RL1728H except the Aperture is 1.209 and the Overall Package Length is 1.8 rather than 1.6.

Ordering Information *

Ordering Number	Evaluation Board	
	Current Amplifier	Integrate, S/H Amplifier
RL1024HAG-011	RC1024LNN-011	RC0100LNB-011/RC0107LNN-011
RL1024HDQ-011	RC1024LNN-011	RC0100LNB-011/RC0107LNN-011
RL1728HAG-011	RC1728LNN-011	RC0100LNB-011/RC0108LNN-011
RL2048HAG-011	RC1728LNN-011	RC0100LNB-011/RC0108LNN-011
RL2048HDQ-011	RC1728LNN-011	RC0100LNB-011/RC0108LNN-011

* Includes standard devices. For options, consult your local sales office.

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Introduction

The EG&G Reticon K Series linear photodiode arrays are designed for applications that require higher sensitivity and wider dynamic range than is available with square element geometries. Devices in this series contain 128, 256, 512 or 1024 photodiodes on 25 µm centers. Typical applications include HPLC, conventional spectroscopy, and noncontact measurement in robotics and factory automation.

Key Features

- 128, 256, 512 or 1024 elements
- Wide 250 µm aperture for higher sensitivity
- Single-phase TTL clock (open collector TTL or 5V CMOS)
- On-chip driver
- Differential output for on-chip noise cancellation

Packaging

Devices are packaged in 16, 18 or 22-pin dual-inline IC packages with ground and polished quartz windows. The pinout configurations are shown in Figure 1 and package dimensions are shown in Figure 11.

General Description

The devices consist of a row of silicon photodiodes, each with an associated junction capacitance on which to integrate photocurrent, and a multiplex switch for periodic readout via an integrated shift register scanning circuit. The shift register clock driver is also integrated so that only a single-phase TTL clock is required for scanning. A row of dummy diodes is read out differentially with the active photodiodes to allow cancellation of multiplex switching transients and to provide a clean video signal with a minimum of external circuitry.

A simplified equivalent circuit of a K Series photodiode array is shown in Figure 2.

Each cell consists of an active photodiode and a dummy photodiode, both with an associated junction capacitance. These diodes are connected through MOS multiplex switches to active video and dummy video recharge lines that are common to all the cells. The switches are sequentially closed for one clock period by the shift register scanning circuit, thereby recharging each cell to 5V and storing a charge of approximately 4 pC on its capacitance. The scanning circuit is driven by a single-phase dynamic shift register (actually two registers in parallel, one for even-numbered diodes and the other for odd-numbered diodes) and a drive circuit which generates four clock phases and two properly-timed start pulses to load the two registers. The individual cells are actually interdigitated with the odd elements being sampled by one register and the even-numbered cells by the other register.

NEG Supply	1	16	Clock
Start	2	15	NC
NC	3	14	Ground
NC	4	13	NC
POS Supply	5	12	End of Scan
Buffer Supply	6	11	Dummy Recharge
Video Recharge	7	10	Recharge Gate
Video Buffer	8	9	Dummy Buffer

RL0128K & RL0256K

NEG Supply	1	18	NC
Start	2	17	Clock
NC	3	16	Ground
POS Supply	4	15	POS Supply
Buffer Supply	5	14	End of Scan
NC	6	13	NC
Video Recharge	7	12	NC
Video Buffer	8	11	Dummy Recharge
Dummy Buffer	9	10	Recharge Gate

RL0512K

NEG Supply	1	22	NC
Start	2	21	Clock
NC	3	20	NC
NC	4	19	NC
NC	5	18	Ground
POS Supply	6	17	POS Supply
Buffer Supply	7	16	End of Scan
NC	8	15	NC
Video Recharge	9	14	NC
Video Buffer	10	13	Dummy Recharge
Dummy Buffer	11	12	Recharge Gate

RL1024K

Figure 1. Pinout Configurations

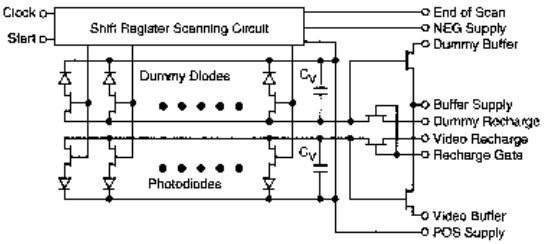


Figure 2. Simplified Equivalent Circuit

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The cell-to-cell sampling rate is the clock frequency, and the integration time is the interval between start pulses. During this line time, this charge stored on each photodiode is gradually removed by photocurrent. The photocurrent is the product of the diode sensitivity and the light intensity or irradiance. The total charge removed from each cell is the product of the photocurrent and the line time. This charge must be replaced through the video line when the diode is sampled and reset once each scan.

In addition to the signal charge, switching transients are capacitively coupled into the active video line by the multiplex switches. Similar transients are introduced into the dummy video line and therefore can be reduced (and a cleaner signal recovered) by reading out the active video and dummy video lines differentially.

In many applications, the recharge gate is biased to the negative supply potential and an output signal is obtained simply by differentially amplifying the recharge pulses on the active video and dummy video recharge lines. However, internal buffer amplifiers that are also provided may be used as part of a sample-and-hold video output circuit.

Sensor Geometry

In the K line scanners, the light-sensing area is a long, narrow rectangular region defined by an aperture in an opaque mask. Bar-shaped photodiodes extend across the aperture and are connected to the multiplex switches buried under the mask. The entire aperture is photosensitive; photocurrent generated by light incident between the photodiodes will be collected by the nearest diode. Figure 3 shows the aperture geometry along with an idealized response function that would be obtained by scanning a point source of visible light along the length of the aperture. The dimensions *a*, *b*, and *c* in Figure 3 are as follows: the photodiode width *a* is 15 µm, the center-to-center spacing *b* is 25 µm, and the aperture width *c* is 250 µm.

Sensitivity and Spectral Response

The spectral response of the K Series devices is similar to that of other high quality silicon photodetectors, covering the range from near UV to the near IR. A standard quartz window assures a full spectral bandwidth. Relative spectral response is shown as a function of wavelength in Figure 4. Note that a smooth spectral response down to the UV is maintained, unlike CCDs, which use a polysilicon layer over the photosite and thus have no response in the UV.

Since Reticon photodiode arrays operate in the charge storage mode, the charge output of each diode (below saturation) is proportional to exposure; i.e., the irradiance or light intensity multiplied by the integration time or the time interval between successive start pulses. Thus, there is an obvious trade-off between scanning speed and the required light intensity. A plot of charge output versus exposure is shown in Figure 5.

Uniformity of response along the length of a photodiode array is a function of wavelength. Devices tend to be less uniform at long wavelengths (IR) and more uniform at short wavelengths (visible).

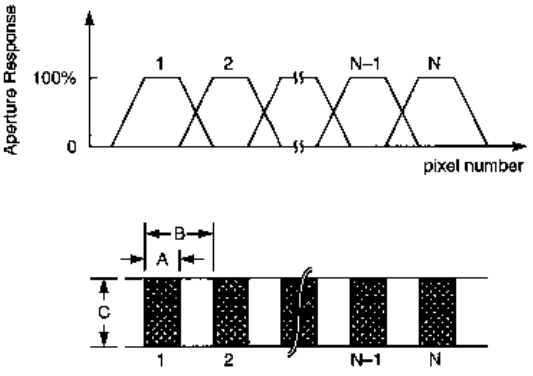


Figure 3. Sensor Geometry and Idealized Aperture Response Function

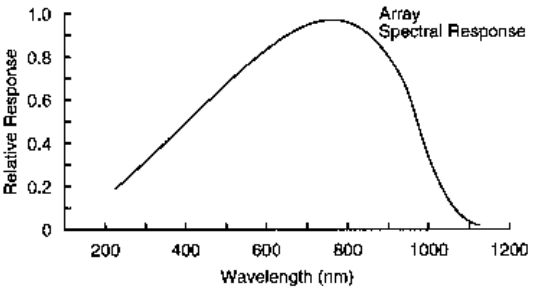


Figure 4. Relative Spectral Response as a Function of Wavelength

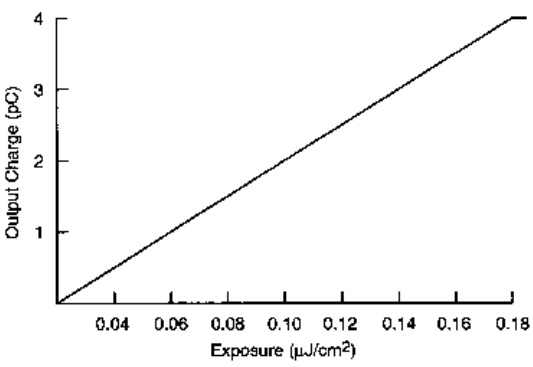


Figure 5. Signal Charge Per Cell as a Function of Exposure (Light Intensity x Line Scan Time)

Dark Response and Dynamic Range

There are three components in the dark output signal from a Reticon line scanner: (1) the integrated dark leakage current; (2) the fixed pattern noise caused by incomplete cancellation of clock switching transients which are capacitively coupled into the video line, and (3) the random pixel noise.

The dark leakage current will vary from element to element but is typically less than 2 pA at room temperature. Assuming this value, leakage current would contribute an output charge of 2 pC with a 1 sec line time, or .08 pC with a 40 ms line time. Thus, since the saturation charge is typically 4 pC, dark current will contribute about 2% of the saturated output signal for t_L = 40 ms, 0.2% for t_L = 4 ms, and so on. The dark current is a very strong function of temperature, approximately doubling for every 7°C increase of photodiode temperature. Thus, the maximum allowable line time becomes correspondingly shorter at high temperatures, and longer at low temperatures. An important feature of the K device design is its low power dissipation, which means that self-heating is negligible. Dark current does not become a limiting factor in the dynamic range unless very long integration times or highly elevated temperature are used.

The switching noise appears as a fixed pattern which is spatially random except that it may have a slight 1, 2, 3, 4 pattern because alternate diodes are sampled on different phases of an internally-generated, four-phase clock. Fixed pattern noise is largely removed by differential readout; its residual amplitude will typically be 1% of the saturation level at a 40 ms integration time.

Pixel noise is the random, nonrepetitive fluctuations superimposed on the dark level and is the ultimate limiting noise that cannot be removed by signal processing. Its rms value will generally be amplifier-limited at a value less than about 0.1% of the saturation level, depending on the noise bandwidth and preamplifier used.

The dynamic range that can be achieved depends on circuit complexity and layout techniques. Care must be exercised in circuit layout to provide for adequate ground plane, circuit decoupling, and avoidance of electrostatic pickup.

Drive Requirements

Two power supplies to the array are required—nominally +5 and -10V. The clock and start timing signals may be at TTL level, and may be supplied from other parts of the system or generated by using a simple circuit such as that shown on Figure 6. In this circuit, the start pulse is obtained by counting clock pulses. By setting the appropriate switches, the number of clock periods, n, between start pulses may be set at any desired value greater than or equal to N, the number of elements in the array. However, the total time between start pulses $t_L = n/f_S$ should not exceed approximately 40 ms (at room temperature) to prevent integrated dark current from making a significant contribution to the output charge.

A timing diagram showing the relationship between the clock and start pulses and the video and end-of-line outputs is shown in Figure 7.

Signal Extraction

The video output of the K devices is a train of N charge pulses flowing onto the video recharge line and dummy recharge line capacitances during each scan, with timing as shown in Figure 7. The pulses on the dummy line contain switching transients only; those on the video line contain switching transients plus the video signal. An output circuit is required which is capable of differentially amplifying these pulses to a useable voltage level.

An integrated sample-and-hold amplifier similar to the type used on Reticon's evaluation board is recommended for the best signal-to-noise ratio performance.

The signal processing scheme makes use of the internal buffer amplifiers and recharge switches. Immediately after the multiplex switch is closed to sample a diode, the voltage change on the video line is sensed through the buffer amplifier, and sampled and held. The recharge gate is then pulsed negative to reset the video line before the next diode is sampled. The result is a sampled and held boxcar video signal such as that shown in Figure 8. Timing and circuitry for this mode is shown in Figures 9A and 9B.

End-of-Scan

An output pulse is provided when the next-to-last element is sampled by the shift register scanning circuit. This end-of-scan output is provided primarily for test purposes. When not in use, it should be connected to the positive supply to avoid introduction of unwanted "glitches" into the video. In some applications, however, it may be desirable to use the end-of-scan output. In these cases, it is recommended that the voltage excursion on the end-of-scan terminal be minimized by using a circuit such as that shown in Figure 10.

Evaluation Boards

Evaluation circuitry containing all the required drive and amplifier circuitry for the operation of the K Series is available from Reticon. These circuits are highly recommended for first-time array evaluation. In many cases, they are also useful for design into final equipment.

RC0100B Series

These circuits provide an integrated, sampled-and-hold-boxcar output as shown in Figure 8. Each circuit is divided into two boards—a standard "motherboard" which contains most of the circuitry, and a small "array board" which contains only those components which must be located close to the array. The array board may be plugged directly into the motherboard or can be extended up to 30 inches away via an optional ribbon cable.

The motherboard (RC0100LNB) is 4.5 x 6.5 inches in size and is terminated by a standard 22-pin edge connector. The array boards (RC0104N, etc.) are 3 inches square and have mounting holes in each corner on 2.6-inch centers. A different array board is required for each array type.

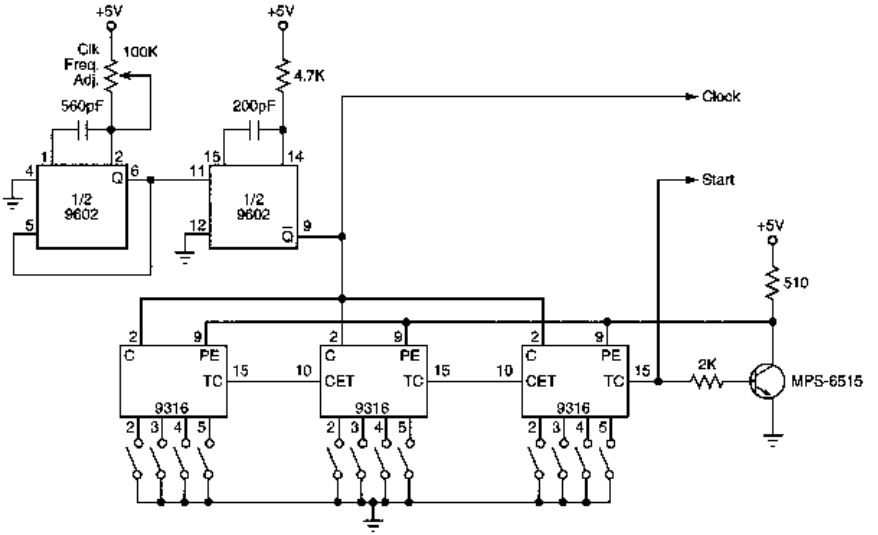


Figure 6. Clock and Counter Circuit Suitable for Generating TTL Clock and Start Pulses

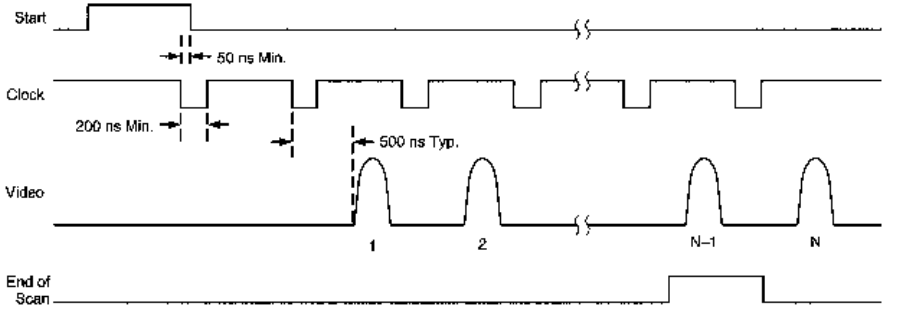


Figure 7. Recharge Mode Timing Diagram

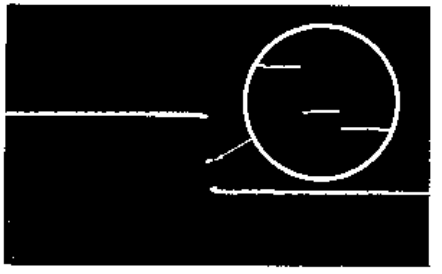


Figure 8. Oscilloscope Photograph Showing Video Output of Integrate, Sample-and-Hold Amplifier

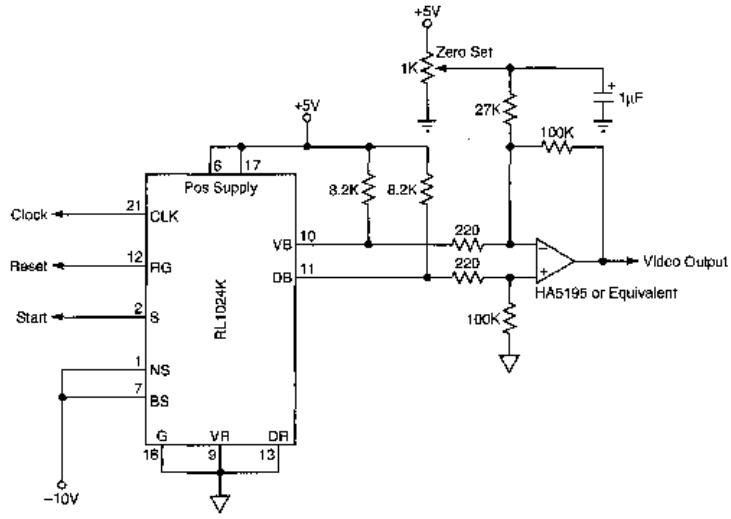


Figure 9A. Buffer Mode Operation Simplified Diagram

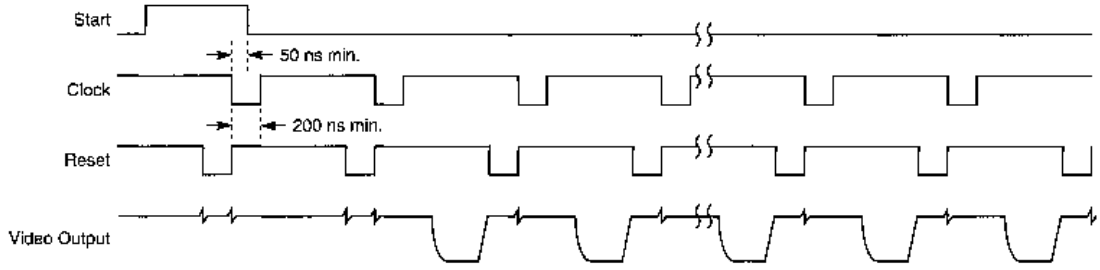


Figure 9B. Buffer Mode Timing Diagram

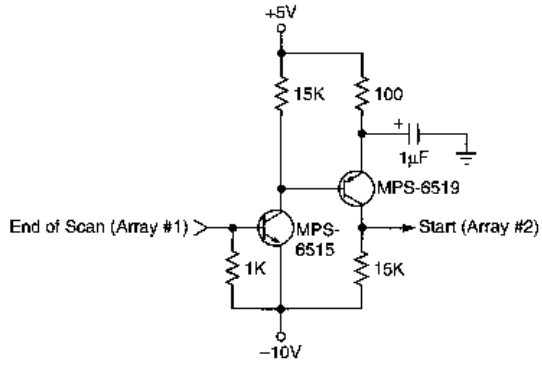


Figure 10. End-of-Scan Output Circuit Suitable for Generating Start Pulse for a Second Array

Table 1. Electrical Characteristics (25°C)

	Min	Typ	Max	Units
Positive supply voltage V_P [1]	+4.5	+5	+5.5	V
Negative supply voltage V_N	-10.5	-10	-9.5	V
Clock voltage low V_{CL}	-10.5	0	+1	V
Clock voltage high V_{CH}	V_P-1	+5	V_P	V
Start voltage low V_{SL}	-10.5	0	+1	V
Start voltage high V_{SH}	V_P-1	+5	V_P	V
Recharge gate voltage low V_{RL}	-10.5	-10	-9.5	V
Recharge gate voltage high V_{RH}	V_P-1	+5	V_P	V
Clock pulse width	0.2	-	-	µs
Start pulse width		See Figure 7		
Clock frequency f_c	-	-	1	MHz
Integration time t_i [3]	-	-	40	ms
Clock input capacitance C_c [2]	-	4	-	pF
Start input capacitance C_s [2]	-	4	-	pF
Video line capacitance C_v [2]				
RL0128K	-	8	-	pF
RL0256K	-	12	-	pF
RL0512K	-	20	-	pF
RL1024K	-	30	-	pF
End-of-scan output resistance	-	5	-	KΩ
DC power dissipation [4]	-	45	-	mW

Notes:

1 No terminal should ever be allowed to go more positive than V_P
2 Measured with nominal power supply voltages
3 Integration time can be longer if the array is cooled and/or if the application can tolerate a larger percentage of dark signal.
4 Mostly due to use of on-chip buffers. When recharge mode is used (buffers biased off), power dissipation is on the order of 1 mW.

Table 2. Electro-Optical Characteristics (25°C)

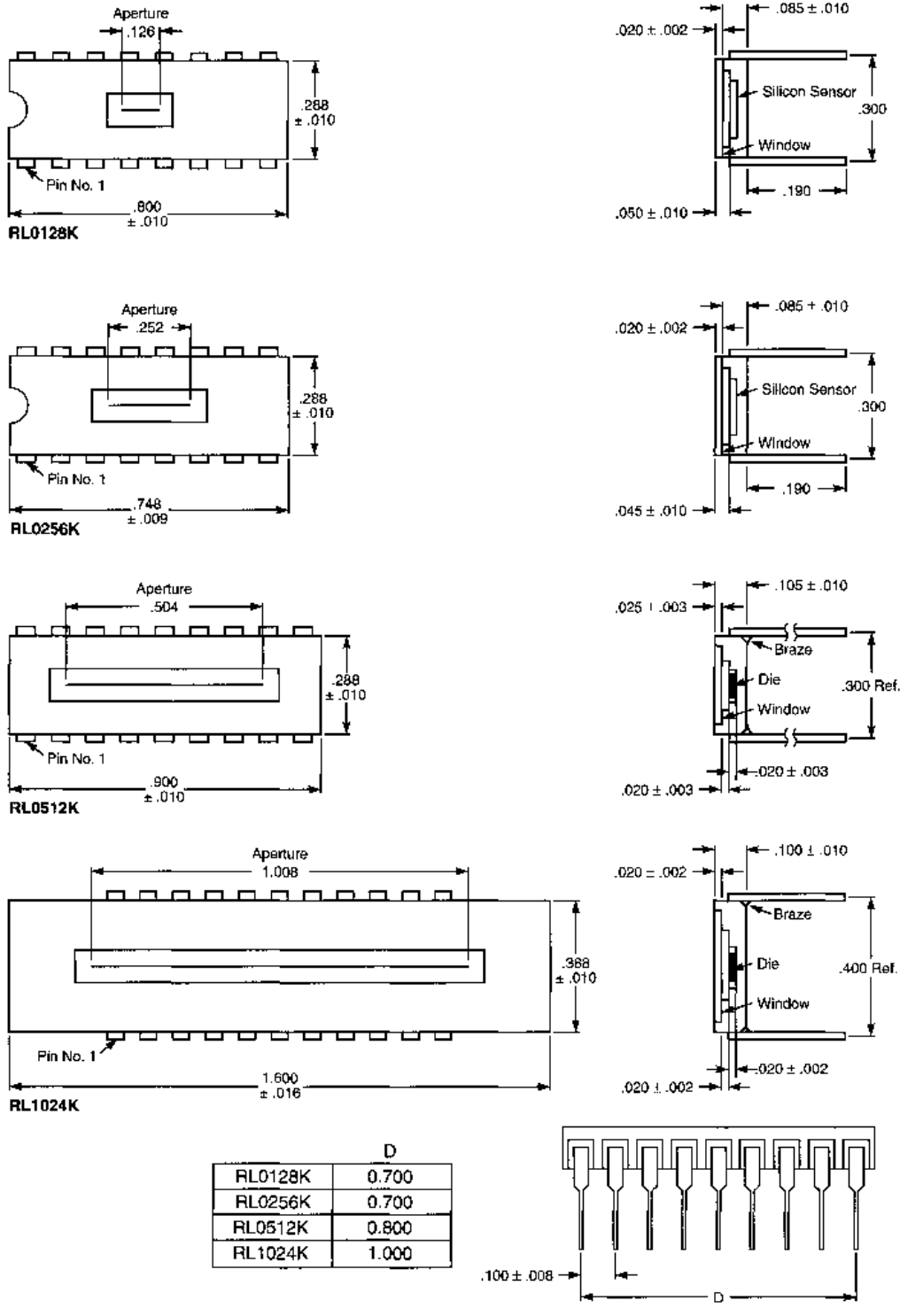
	Min	Typ	Max	Units
Diode center-to-center spacing	-	25	-	µm
Diode aperture width	-	250	-	µm
Photodiode sensitivity [1]	-	25	-	pC/µJ/cm^2
Nonuniformity of sensitivity [1]				
RL0128K	-	7	10	±%
RL0256K	-	7	10	±%
RL0512K	-	9	11	±%
RL1024K	-	12	14	±%
Saturation charge	-	4	-	pC
Saturation exposure		0.18		µJ/cm^2

Note:

1 Measured using a 2870°K broadband light source filtered with a Fish-Schurman HA-11 heat absorbing filter. The first 2 and the last 2 diodes are neglected

Absolute Maximum Ratings

	Min	Max	Units
Voltage on any terminal	V_P-20	V_P	V
Storage temperature	-55	+125	°C
Temperature under bias	-55	+85	°C



	D
RL0128K	0.700
RL0256K	0.700
RL0512K	0.800
RL1024K	1.000

Figure 11. Package Dimensions

Ordering Information *

Part Number	Evaluation Circuit	
	Current Amplifier	Integrate, S/H Amplifier
RL0128KAQ-011	RC0301LNN-011	RC0100LNB-011/RC0104LNN-011
RL0256KAQ-011	RC0301LNN-011	RC0100LNB-011/RC0104LNN-011
RL0512KAQ-011	RC0302LNN-011	RC0100LNB-011/RC0105LNN-011
RL1024KAQ-011	RC0303LNN-011	RC0100LNB-011/RC0106LNN-011

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General Description

The EG&G Reticon R Series (RL0512R and RL1024R) combines two S Series devices on a single, monolithic substrate. They are positioned in parallel to each other. They operate completely independently, allowing simultaneous readout, sequential readout (first one side and then the other), or any number of other user-defined formats. Each R Series device comes in a 34-pin ceramic side-brazed DIP. Two kinds of windows are available: a ground and polished quartz window, or a fiber-optic window.

The R Series has virtually all the advantages of the standard RL0512S. Refer to the S Series data sheet for information on internal scanning circuitry, timing, electrical characteristics, dark signal and noise characteristics, and amplifier requirements.

The R Series is ideal for applications such as dual-beam spectroscopy (sample and reference beam), time-resolved spectroscopy of a single beam (by delaying the start of one of the arrays), or other instrumentation requiring parallel arrays in perfect registration.

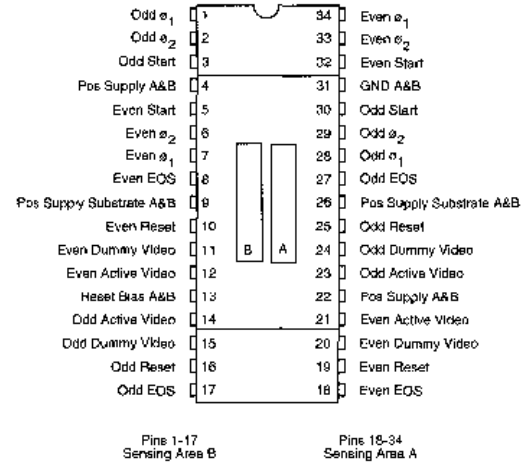


Figure 1. Pinout Configuration

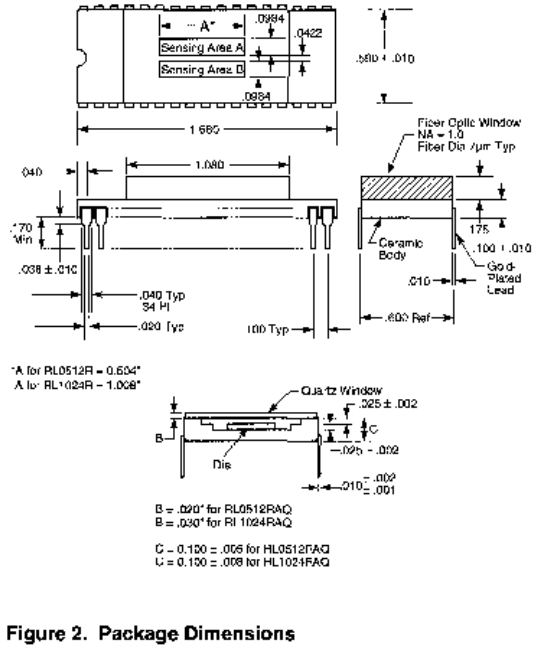


Figure 2. Package Dimensions

Ordering Information

Array	Part Number
RL0512R with Quartz Window	RL0512RAQ-011
RL0512R with Fiber Optic Faceplate	RL0512RAF-011
RL1024R with Quartz Window	RL1024RAQ-011
RL1024R with Fiber Optic Faceplate	RL1024RAF-011

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General Description

The Reticon S series is a family of monolithic self-scanning linear photodiode arrays optimized for application in spectroscopy. The devices in this series consist of a row of silicon photodiodes, each with an associated junction capacitance in which to integrate photocurrent and a multiplex switch for periodic readout via an integrated shift register scanning circuit. The part number of each device indicates the number of elements in the array (e.g., 128, 256, 512 or 1024).

The S series devices are mounted in ceramic side-brazed dual-inline packages which mate with standard 22-pin integrated circuit sockets. The pinout configuration is shown in Figure 1. Package dimensions are shown in the outline drawing of Figure 11. Standard S series devices are sealed with a ground and polished quartz window. However, the optional fiber optic faceplate version shown in Figure 11 is also available. The fiber optic faceplate has 6 µm diameter fibers and a numerical aperture of 1.0.

Key Features

- Simultaneous integration on 128, 256, 512 or 1024 photodiode sensor elements with 25 µm center-to-center spacing
- Each sensor element has a 100:1 aspect ratio (25 µm x 2.5 mm)
- Integration times as short as 64 µsec or as long as 0.3 sec are possible at room temperature. Integration times of minutes or even hours without sensors saturating can be achieved by cooling.
- Low power dissipation (less than 1 mwatt) to facilitate cooling
- Clock controlled sequential readout at arbitrary total effective data rates up to 5 MHz (f_C =1.25 MHz max)
- Differential output to cancel clock switching transients and fixed patterns
- Low output capacitance for low noise
- High saturation signal charge (14 pcoul) for wide dynamic range
- Wide spectral response (200 - 1000 nm)
- Choice of quartz window or fiber optic faceplate
- Standard 22 lead dual-inline integrated circuit package

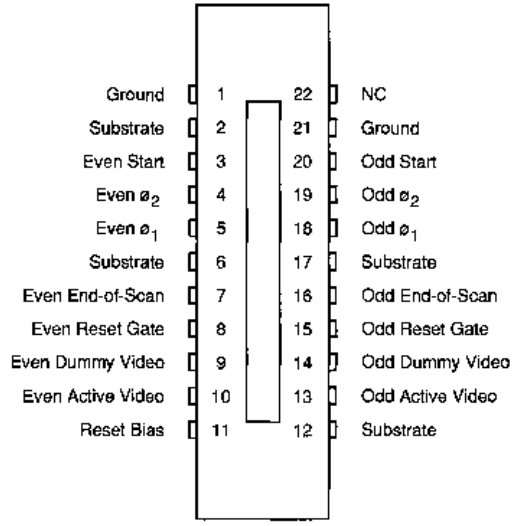


Figure 1. Pinout Configuration

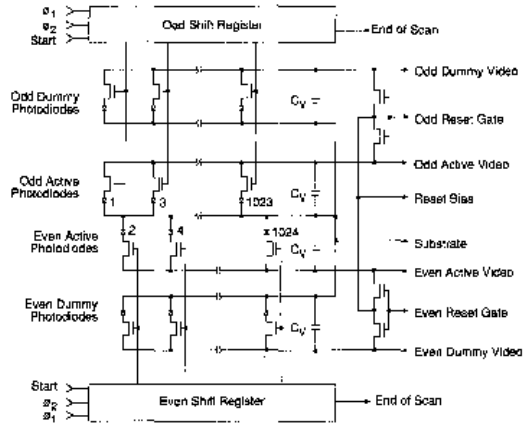


Figure 2. Equivalent Circuit

Sensor Characteristics

The Reticon S series self-scanning photodiode arrays contain 128, 256, 512 or 1024 silicon diode sensor elements on 25 µm centers corresponding to a density of 40 diodes/mm and an overall aperture length of 3.2, 6.4, 12.8 or 25.6 mm. The height of the sensor elements is 2.5 mm giving each element a slit-like geometry with 100:1 aspect ratio suitable for coupling to monochromators or spectrographs. The sensor geometry is shown in Figure 3.

Charge generated by light incident on the n-type surface between two p-regions will divide between the adjacent diodes to produce the response function shown in Figure 3.

Figure 4 shows typical output charge as a function of exposure at 750 nm wavelength. Exposure in njoules/cm^2 is calculated by multiplying the light intensity in µwatt/cm^2 by the integration time in msec. Note that the response is linear with exposure up to a saturation charge of 14 pcoul at a saturation exposure of 50 njoules/cm^2. The sensitivity is defined as the ratio of saturation charge to saturation exposure and is 2.8 x 10^{-4} pcoul/joule/cm^2 (at 750 nm). Typical sensitivity as a function of wavelength is shown in Figure 5. Quantum efficiency can be obtained by dividing the sensitivity by the area of a sensor element (6.25 x 10^{-4} cm^2) and multiplying by the energy per photon in eV. Peak quantum efficiency is about 80% at 650 nm. The dark current of an S series device is typically about 2 pA per diode at 25°C and is a strong func-

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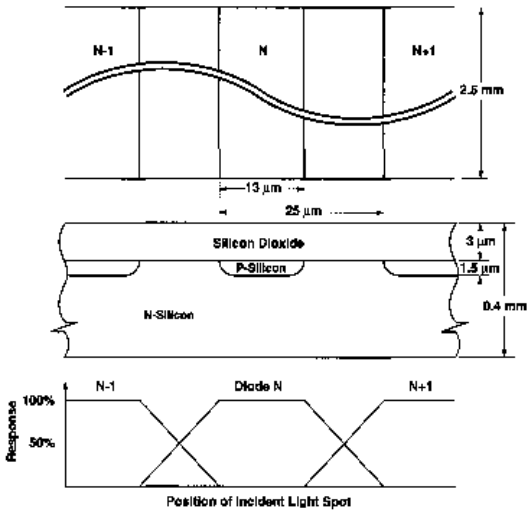


Figure 3. Sensor Geometry and Aperture Response Function

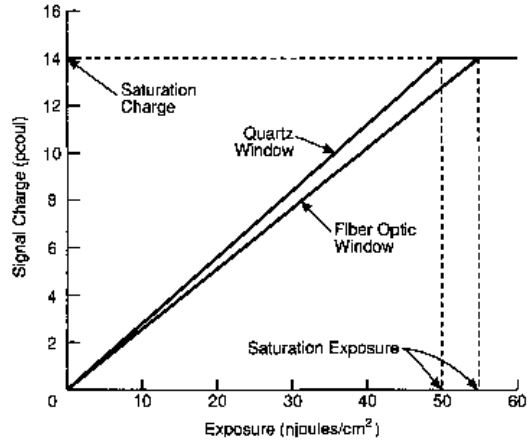


Figure 4. Signal Charge Versus Exposure at 750 nm Wavelength

tion of temperature as shown in Figure 6. The dark signal charge is given by the dark current multiplied by the integration time.

Scanning Circuit

A simplified equivalent circuit of an RL1024S photodiode array is shown in Figure 2. Each cell consists of a photodiode and a dummy diode, both with an associated junction capacitance. These diodes are connected through MOS multiplex switches to video and dummy recharge lines. One pair of recharge lines is common to all the odd elements and another pair is common to all the even elements. The shift registers are driven by multiphase clocks with periodic start pulses being introduced to initiate each scan. The cell-to-cell sampling rate is determined by the clock frequency.

The integration time is the interval between start pulses. The output signal obtained from each scan of an N element array is a train of N charge pulses, each proportional to the light exposure on the corresponding photodiode. By properly phasing the clock drives to the two shift registers, all of the diodes can be sampled in proper sequence. The two video lines can then be connected together to provide a continuous train of output charge pulses. In addition to the signal charge, switching transients are capacitively coupled into the video lines by the multiplex switches. Similar transients are introduced into the dummy lines and therefore can be reduced and a cleaner signal recovered by reading out the video and dummy lines differentially.

Clock and Voltage Requirements

Scanning is by means of two independent integrated shift registers, one to address the odd-numbered diodes, and the other to address the even-numbered diodes. Each shift register is driven by two-phase clocks. The clocks may be complementary square waves, or they may have shorter negative duty cycle. In no case should ϕ_1 and ϕ_2 be negative simultaneously, as this will cause the scan to be terminated.

The same pair of clocks and the same start pulse may be applied to both registers, but this will result in diode pairs 1 and 2, 3 and 4, etc., being sampled simultaneously. Figure 7 shows a simple two-phase clock drive circuit for this mode of operation and its related timing diagram. Alternatively, four-phase clocking may be used in which the two phases which drive the even register are delayed with respect to the two phases which drive the odd register. This results in all the diodes being sampled in proper sequence. Four-phase clocking is used in the Reticon RC1000/RC1001 board set evaluation circuit (described below).

In the specifications, all voltages are expressed with respect to the substrate. However, for compatibility with TTL clocks and ease of signal extraction, it is recommended that the substrate be run at +5V. The clock phases should then swing between +5 and −7V nominal. The start pulse should overlap one positive going transition of ϕ_1 as shown in Figure 7.

End of Scan

Output pulses, useful primarily for test purposes, are provided when the last odd and even elements are sampled by the shift register scanning circuit. When not used, they should be shorted externally to the array substrate to avoid introduction of unwanted "glitches" into the video. The voltage excursion on the end-of-scan terminals (when used), should be minimized by using a circuit such as that shown in Figure 8.

Amplifier Requirements

Two types of amplifier circuits are in common use with Reticon photodiode arrays. These are (1) a simple current amplifier, and (2) a video line integration, sample-and-hold circuit. A current amplifier holds the video line at virtual ground and senses the current pulses flowing into the video line to recharge the diodes through their respective multiplex switches as they are sampled in sequence. These current

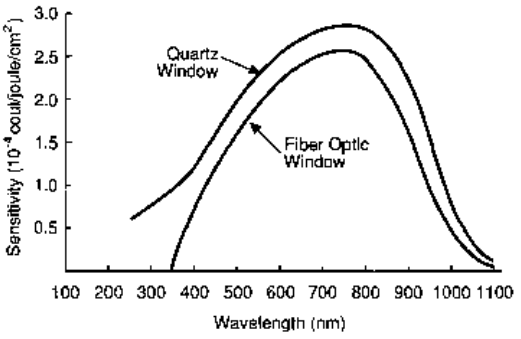


Figure 5. Typical Spectral Response

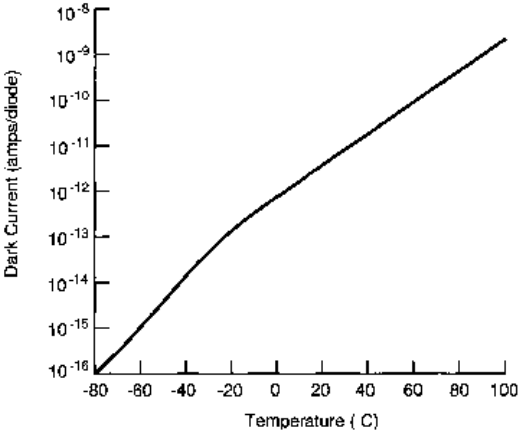


Figure 6. Temperature Dependence of Dark Current

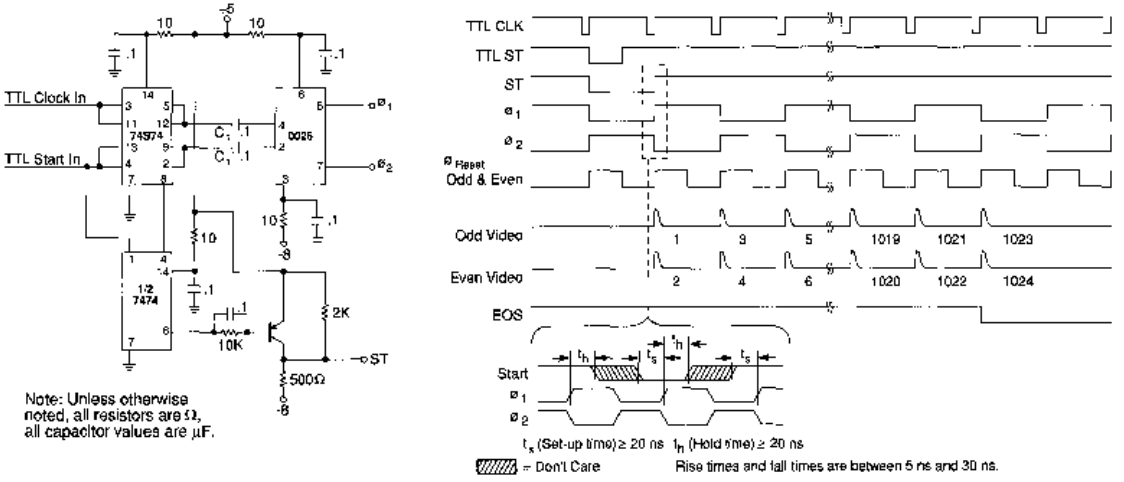


Figure 7. Simple Two-phase Clock Drive Circuit and Related Timing Diagram

pulses, which contain a charge up to 14 pcoul at saturation, are converted by the amplifier to a train of voltage pulses corresponding to the light intensity on the various diodes.

With a video line integration sample-and-hold circuit, the video line is reset to ground prior to closing the multiplex switch to each diode. When the switch is closed, charge divides between the diode and the video line and the resulting change in video line voltage is sampled and held. The video line and diode are then reset to ground prior to opening the multiplex switch to the next diode. The result is a boxcar output waveform.

Dark Signal and Noise

There are two components to the dark fixed pattern signal from the S series arrays. These are due to (1) spatial variations in the switching transients coupled into the video line through the clocks and the internal multiplex switches, and (2) the integrated dark current. A portion of the switching transient effect will be spatially random and a portion will have the periodicity of the clocks. The latter portion can be minimized by matching the clock amplitudes and rise and fall times and by good circuit layout to minimize capacitance between clocks and video lines. The peak-to-peak fixed pattern due to all switching transient effects should be less than 1% of the saturated signal. The fixed pattern due to dark current is the dark current multiplied by the integration time. It can be arbitrarily reduced by lowering the temperature (see Figure 6) or by reducing the integration time.

There are three identifiable sources of readout noise: (1) reset noise, (2) shot noise, and (3) amplifier noise. Reset noise or kTC noise is associated with resetting the diode

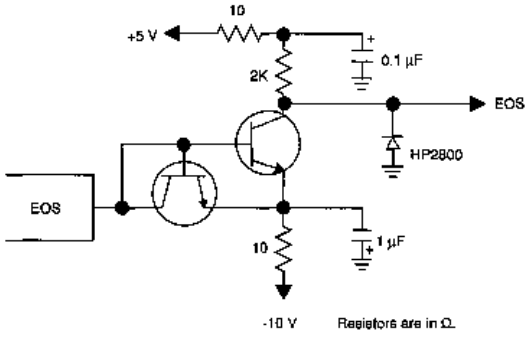


Figure 8. End-of-Scan Circuit

capacitance to a fixed voltage. Its rms value is given by $\sqrt{kTC}/q$ where k is Boltzmann's constant, T is the absolute temperature, q is the electronic charge, and C is the total capacitance of the photodiode (approximately 2 pF), the video line it connects to, and the capacitance of the external circuitry. At room temperature, the kTC noise for the 1024S array is approximately 2000 electrons. It can be reduced somewhat by cooling. The rms dark current shot noise is the square root of the number of electrons in the dark signal charge. For example, with a room temperature dark current of 5 pA and 10 msec integration time, the rms dark current shot noise is approximately 560 electrons. Because of the exponential temperature dependence of dark current, shot noise can be reduced dramatically with a moderate amount of cooling. Amplifier noise depends on the amplifier circuit used. In general, the low video output capacitance of the S series makes it easier to achieve low amplifier noise, and values below 2200 electrons are possible.

Evaluation Circuit

A complete evaluation circuit for the S series arrays is available from Reticon. The RC1000/RC1001 evaluation boardset provides the user an easy means to evaluate the operation of the S series photodiode arrays.

The RC1000/1001 has a sample-and-held video output with a typical dynamic range of 4000:1. Provision for cooling the array using a thermo-electric cooler is provided by means of an access hole located directly beneath the array.

The boardset requires +5 and ±15V supplies and can be adjusted for pixel rates up to 250 kHz.

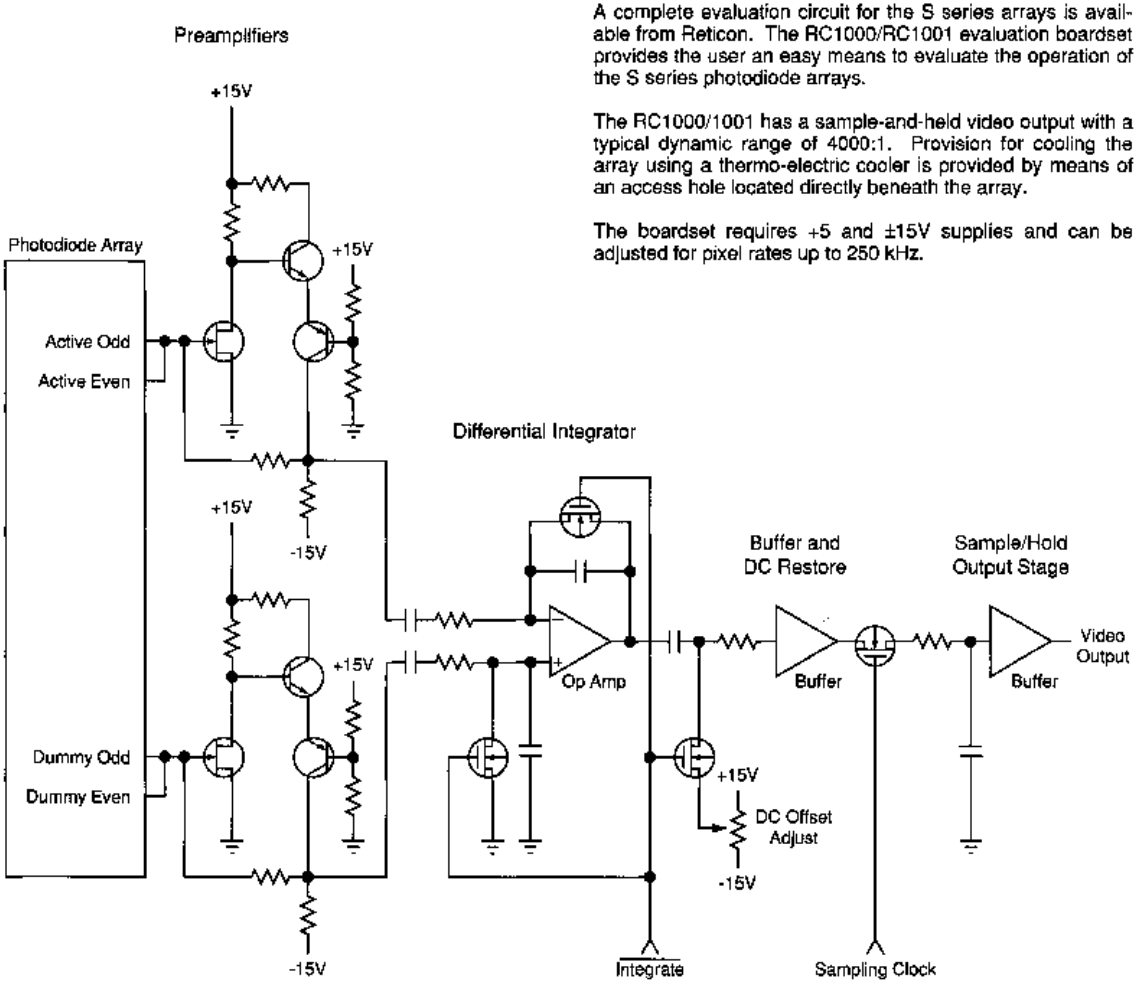


Figure 9. Simplified RC1000/RC1001 Evaluation Board Output Circuit

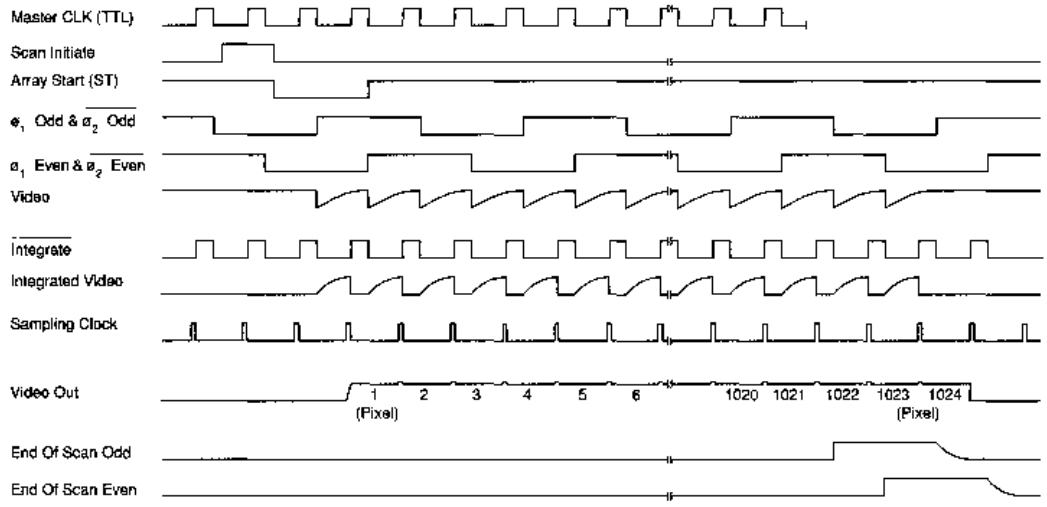


Figure 10. Timing Diagram of RC1000/RC1001 Evaluation Board

Table 1. Electrical Characteristics (25°C)

	Min	Typ	Max	Units
Video line bias [1]	-4	-5	-6	V
Clock amplitude [1]	-11	-12	-15	V
Start pulse amplitude [1]	-11	-12	-15	V
Substrate bias	+4.5	+5	+5.5	V DC
Total effective pixel output rate			5	MHz
Clock frequency			1.25	MHz
Capacitance of each clock line (@ 5V bias) [3]				
RL0128S		8		pF
RL0256S		23		pF
RL0512S		30		pF
RL1024S		60		pF
Capacitance of each video line (@ 5V bias) [3]				
RL0128S		3		pF
RL0256S		9		pF
RL0512S		12		pF
RL1024S		24		pF
Capacitance of each photodiode (@ 5V bias) [3]		2		pF
End of scan output resistance [3]		5		KΩ
DC power dissipation [2]		1		mwatt

Notes:

1 Measured with respect to substrate. Substrate is normally run at +5V for compatibility with TTL clock circuits.

2 The AC power is given by $2C_cV_c^2f_s$ where C_c is the capacitance of each clock line, V_c is the clock voltage, and f_s is the scan frequency.

3 Calculated typicals - not measured.

Table 2. Electro-Optical Characteristics (25°C)

	Typ	Max	Units
Center-to-center spacing	25		µm
Aperture width	2.5		mm
Sensitivity [1,3,6]	2.8×10^{-4}		coul/joul/cm^2
Nonuniformity of response [2,6]	5	10	±%
Saturation exposure [1,3,6]	50		njoules/cm^2
Saturation charge	14		pcoul
Average dark current [5,6]	2	5	pamp
Quantum efficiency [1,3]	75		%
Spectral response peak [3]	750		nm
Spectral response range [3,4]	200-1000		nm

Notes:

1 Peak, typical at 750 nm, quartz window.

2 Measured at 50% V_{sat} with 2870°K incandescent tungsten lamp filtered with a Fish Schurman HA-11 heat-absorbing filter.

3 Fiber optic faceplate will modify sensitivity as shown in Figure 5.

4 From 250-1000 nm sensitivity ≥20% of its peak value.

5 Max dark leakage ≤1.5 x average dark leakage. Measured at 40 milliseconds integration at 25°C.

6 All specifications ignore first two and last two diodes.

Absolute Maximum Ratings

	Min	Max	Units
Voltage applied to any terminal with respect to common	0	-20	V
Storage or operating temperature			
Quartz windowed (SAQ)	-78	+85	°C
Fiber optic (SAF)	-40	+85	°C

Ordering Information

Part Number	Evaluation Circuit
Quartz Window	
RL0128SAQ-011	RC1000LNN-011/RC1001LNN-011
RL0256SAQ-011	RC1000LNN-011/RC1001LNN-011
RL0512SAQ-011	RC1000LNN-011/RC1001LNN-011
RL1024SAQ-011	RC1000LNN-011/RC1001LNN-011
Fiber Optic Window	
RL0128SAF-011	RC1000LNN-011/RC1001LNN-011
RL0256SAF-011	RC1000LNN-011/RC1001LNN-011
RL0512SAF-011	RC1000LNN-011/RC1001LNN-011
RL1024SAF-011	RC1000LNN-011/RC1001LNN-011

Custom modifications to the S series devices are also possible, i.e., minimum thickness (1 µm) protective oxide layer for use in soft x-ray detection.

	A	B
RL0128S	1.080±.011	3.2 mm
RL0256S	1.080±.011	6.4 mm
RL0512S	1.080±.011	12.8 mm
RL1024S	1.600±.016	25.6 mm

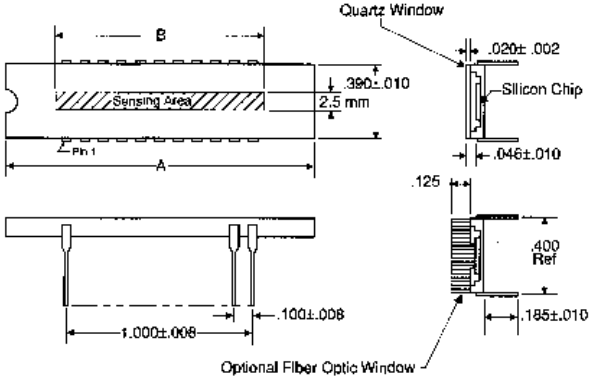


Figure 11. Package Dimensions. Dimensions are in Inches Except Where Millimeters (mm) are Indicated.

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SAX Series
X-Ray Sensitive
Solid State Line Scanners

General Description

The SAX is a custom modification of the S series solid state line scanner with the fiber optic face plate option. Resolutions available are 128, 512, and 1024 elements. The modification consists of adding an X-ray phosphor to the input side of the fiber optic face plate. This provides spectral sensitivity to X-rays in the range of 10 to 75 keV. The fiber optic face plate acts as an interface between the phosphor and the diode array and protects the array from X-ray damage as well (See Figures 5 and 6). For detection of soft X-rays (1.2 to 12 keV) see reference No. 2.

Optical alignment of the SAX device is possible because the X-ray phosphor has approximately 50% transmission to visible light. During operation, X-rays striking the phosphor are converted to green light. The green light is transmitted through the fiber optic face plate to the silicon photodiodes where the light is converted to an electronic charge. The resulting charge is integrated on each photodiode so that after a period of time each photosite has collected a charge proportional to the local flux of the X-ray beam. When the array circuitry scans the diodes, the charge packets are sequentially converted to a voltage level which, when displayed on an oscilloscope, reproduces a spatially resolved one-dimensional X-ray image. Integration times of .026 to 500 msec are possible at room temperature. Cooling the array can extend integration time to minutes or hours by reducing the dark current.

The SAX series has all the advantages of the S series arrays. Refer to the S series data sheet for detailed information on the internal scanning circuitry, the package and pin configuration, electrical characteristics, dark signal and noise characteristics, amplifier requirements and evaluation circuit.

References

1. John McGinnis, "An X-Ray Sensitive Photodiode Array", Industrial Research and Development, March 1980.
2. Reticon Application Note 101, "Application of Reticon Photodiode Arrays as Electron and X-Ray Detectors".
3. Louis N. Koppel, "An Active-Recording X-Ray Crystal Spectrometer For Laser-Induced Plasmas", Review of Scientific Instruments, 47, 9 (Sept. 1976).
4. R. D. Bleach & D. J. Nagel, "X-Ray Applications of Self-Scanning Silicon Diode Arrays", Applied Optics, Vol. 16, March 1977.
5. John McGinnis, Ronald K. Hopwood and Louis N. Koppel, "X-Ray Applications of Self-Scanned Photo-diode Arrays", Advances in Nondestructive Testing, 1980 Volume.

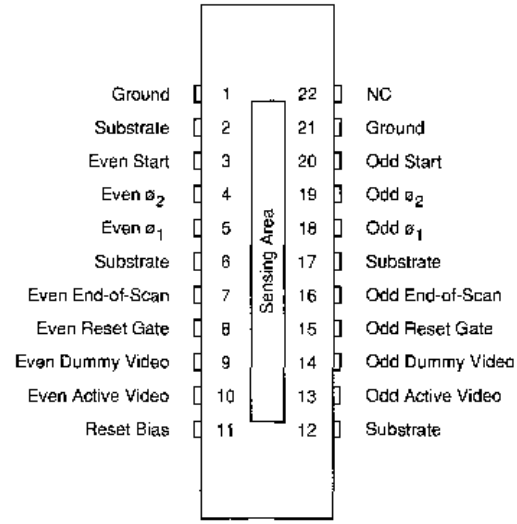


Figure 1. Pinout Configuration

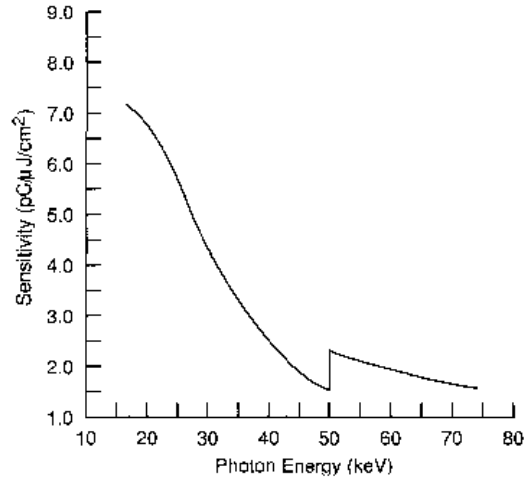


Figure 2. Typical Spectral Response

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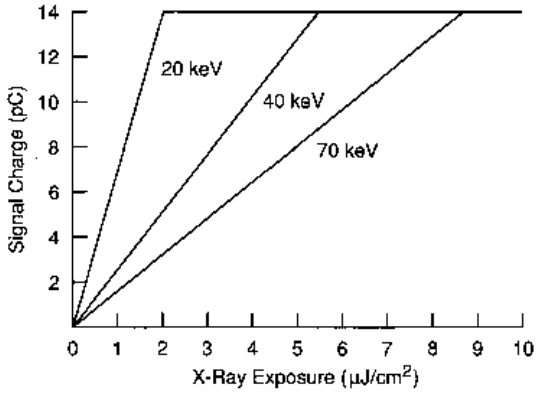


Figure 3. Signal Charge Versus X-Ray Exposure for 20 keV, 40 keV, and 70 keV

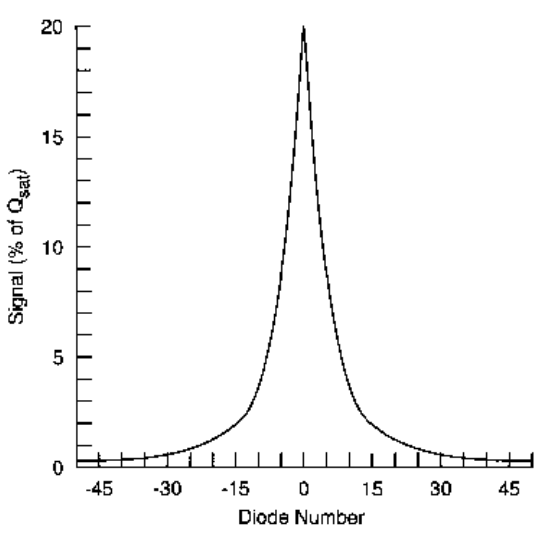


Figure 4. Typical Resolution, 0.05 mm Lead Slit

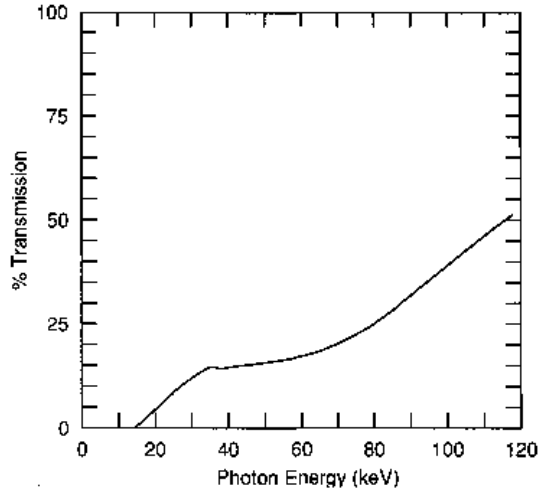


Figure 5. X-Ray Transmission of a 1/8" Thick Fiber Optic Plate (Barium Lanthanum Glass)

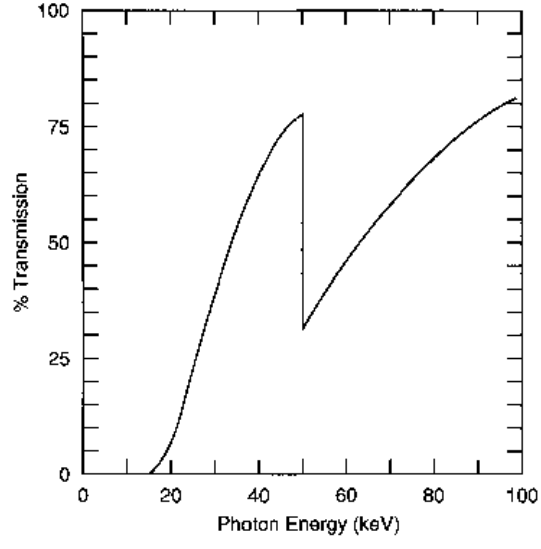
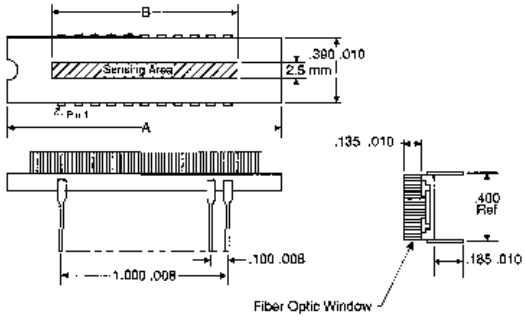


Figure 6. X-Ray Transmission Scintillator Screen

Table 1. Electro-Radiological Characteristics (25°C)

Parameter	Typ	Units
Center-to-center spacing	25	µm
Aperture width	2.5	mm
Sensitivity [1]	2.5	pC/µJ/cm²
Nonuniformity of response	10	±%
Saturation exposure [1]	5.6	µJ/cm²
Saturation charge	14	pC
Average dark current	5	pA
Spectral response range	10-75	keV

Note:
[1] 40 keV monochromatic x-ray source



	A	B
RL0128S	1.080 .011	3.2 mm
RL0512S	1.080 .011	12.8 mm
RL1024S	1.600 .016	25.6 mm

Figure 7. Packaging Dimensions

Ordering Information *

Part Number	Evaluation Circuit
RL0128SAX-011	RC1000LNN-011/RC1001LNN-011
RL0512SAX-011	RC1000LNN-011/RC1001LNN-011
RL1024SAX-011	RC1000LNN-011/RC1001LNN-011

*Includes standard devices. For all options, consult your local sales office.

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General Description

The RL2048S is a monolithic self-scanning linear photodiode array optimized for spectroscopy applications. The device consists of a row of silicon photodiodes, each with an associated junction capacitance on which to integrate photo current and a multiplex switch for periodic readout via four independent integrated shift registers. The device is an addition to Reticon's S Series family of arrays, and offers the same operational and performance characteristics.

The array die is bonded in a 32-pin DIP with dimensions of 2.75" length by 0.6" width and sealed with a choice of a polished and ground quartz window or a fiber optic faceplate as shown in Figure 1. The fiber optic faceplate has 6 µm diameter fibers and a numerical aperture of 1.

Key Features

- Simultaneous integration on 2048 photodiode sensor elements with 25 µm center-to-center spacing
- Each sensor element has a 100:1 aspect ratio (25 µm x 2.5 mm)
- Integration times as short as 1 ms or as long as 0.3 sec are possible at room temperature. Integration times of minutes or even hours can be achieved by cooling.
- Low power dissipation (less than 1 mW) to facilitate cooling
- Clock controlled sequential readout at arbitrary total effective data rates up to 5 MHz (f_c = 625 kHz, max)
- Differential output to cancel clock switching transients and fixed patterns
- Low output capacitance for low noise
- High saturation signal charge (14 pC) for wide dynamic range
- Wide spectral response (200 - 1000 nm)
- Choice of quartz or fiber optic window
- 32 lead dual-inline integrated circuit package

Sensor Characteristics

This addition to the Reticon S Series self-scanning photodiode arrays contains 2048 silicon diode sensor elements on 25 µm centers, corresponding to a density of 40 diodes/mm and an overall length of 52 mm. The height of the sensor elements is 2.5 mm giving each element a slit-like geometry with 100:1 aspect ratio suitable for coupling to monochromators or spectrographs. The sensor geometry is shown in Figure 2.

Charge generated by light incident on the n-type surface between two p-regions will divide between the adjacent diodes to produce the response shown in Figure 2.

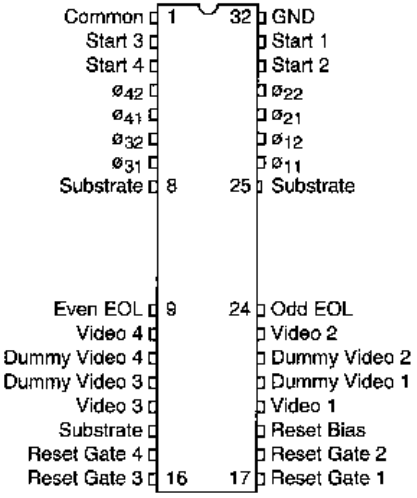


Figure 1. Pin Configuration

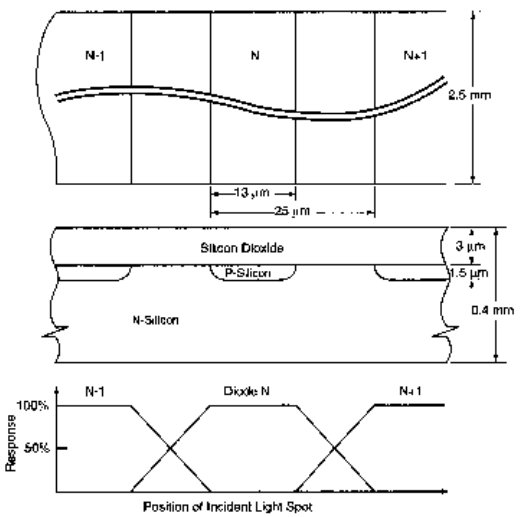


Figure 2. Sensor Geometry and Aperture Response Function

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Figure 3 shows typical output charge as a function of exposure at 750 nm wavelength. Exposure in nJ/cm^2 is calculated by multiplying the light intensity in µW/cm^2 by the integration time in ms. Note that the response is linear with exposure up to a saturation charge of 14 pC. A saturation exposure is typically 50 nJ/cm^2. The sensitivity is defined as the ratio of saturation charge to saturation exposure and is 2.8 x 10^{-4} C/J/cm^2 (at 750 nm). Typical sensitivity as a function of wavelength is shown in Figure 4. Quantum efficiency can be obtained by dividing the sensitivity by the area of a sensor element (6.25 x 10^{-4} cm^2) and multiplying by the energy per photon in eV. Peak quantum efficiency is about 80% at 650 nm. The dark current of an S Series device is typically about 2 pA per diode at 25°C and is a strong function of temperature as shown in Figure 5. The dark signal charge is given by the dark current multiplied by the integration time.

Device Structure

The device structure provides a variety of readout options. See Figure 6 for a simplified equivalent circuit of the RL2048S. Each of the four independent registers are connected to a set of 512 active photodiodes and 512 dummy diodes. The diodes are connected to their respective active and dummy video lines through multiplex switches. A reset switch is connected from each of the video lines to an external pin connection.

As shown in Figure 6, two registers control readout of the first block of 1024 diodes; 512 odd diodes and 512 even diodes, respectively. The remaining 2 registers control readout of the next block of 1024 diodes.

Operational Description

With a bias of approximately 5V between the substrate and both dummy and active video lines, a charge of 5V is placed on the diode's depletion capacitance each time its multiplexing switch is closed. When the switch is opened, the photon-generated charges are allowed to integrate on the photodiode's capacitance during the integration time, which is the time between switch closures. These charges are removed when the diodes are recharged to 5V. The charge, which is proportional to the impinging light energy, can be read with a current pulse detector during the diode recharge period. Figure 7 is an example of a transconductance amplifier which is used to detect the impulse current of the signal charge.

As the shift register clocks a bit sequentially through its output lines, it opens and closes the multiplexing switches. Hence, the switch closure rate of a given diode will equal the scan rate or the integration time for the light exposure.

Since the gate of the multiplexing switches of the active diode and its corresponding dummy diode are connected in parallel to each output of the shift register, the active as well as the dummy lines will be read out together. Because the charges which are introduced in the dummy diodes are anomalies such as fixed pattern noises generated by the clocks, they can be reduced through a differential summation of the charges from the dummy and the active signals, leaving only the signal component. An example of the differential detection circuit is shown in Figure 8. First, the pixel charges from the active and dummy video lines are preamplified with a transconductance amplifier, then these amplified signals are applied to a differential integrator where the dummy signals are subtracted from the active signals. Leaving the integrator, the difference signal can then be sampled and held.

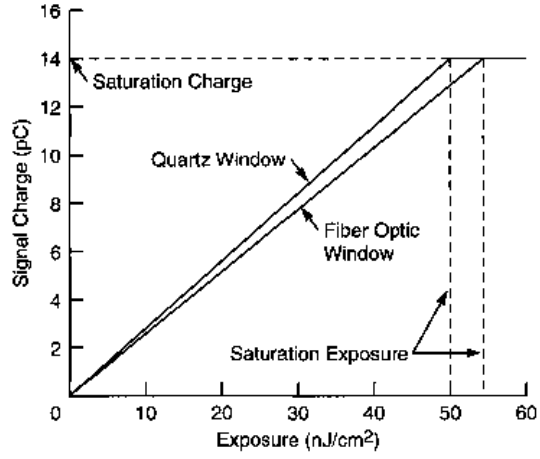


Figure 3. Signal Charge Versus Exposure at 750 nm Wavelength

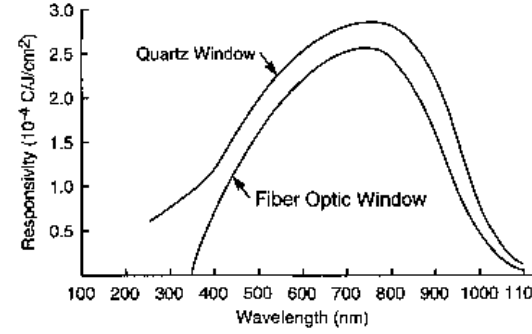


Figure 4. Typical Spectral Response

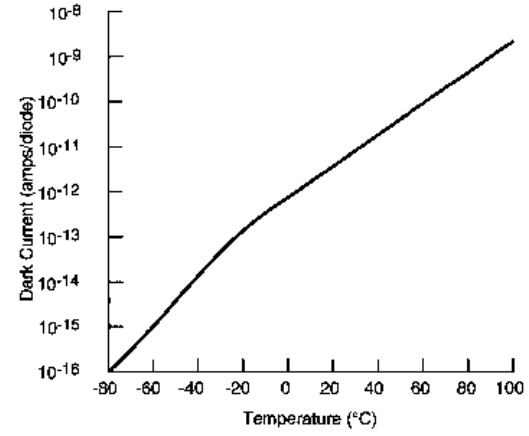


Figure 5. Temperature Dependence of Dark Current

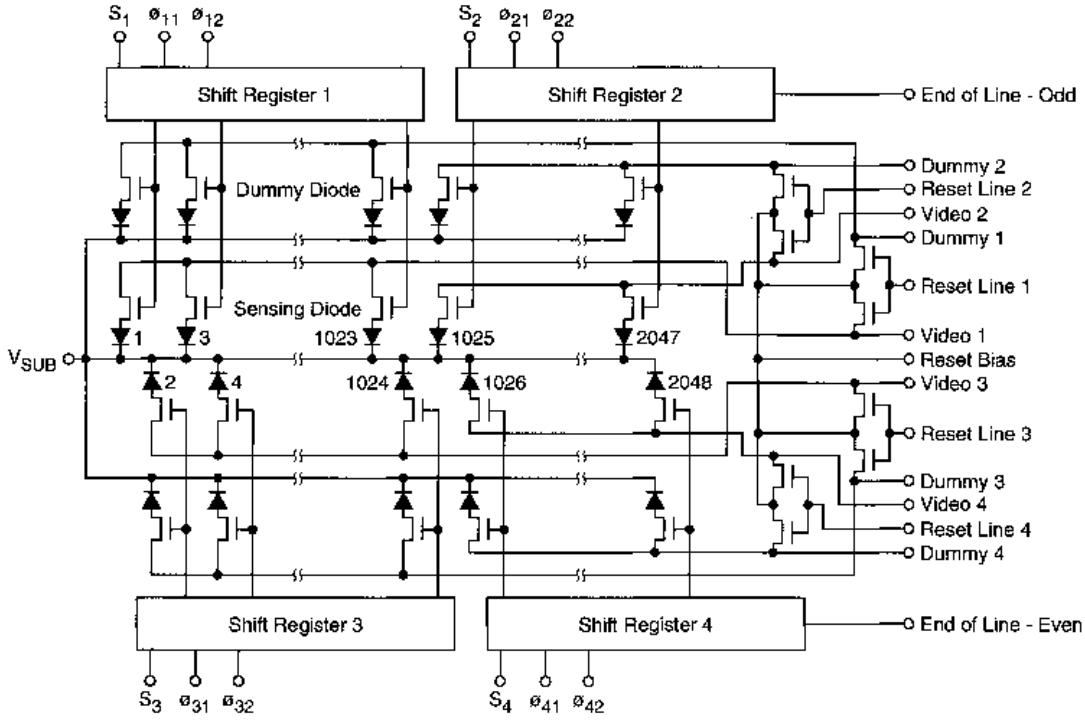


Figure 6. Simplified Diagram of Device Structure

Clock Drive and Voltage Requirements

Since the four shift registers are independent, the clock operational description for any one applies to the others. Figure 9 is a timing diagram of a shift register's operation. It is driven with complementary clocks $ø_1$ and $ø_2$. The scanning process is initiated when the start pulse is loaded into the register. The start pulse is locked into the register with the rising edge of $ø_1$ as noted in the timing diagram. Figure 9 also shows a simplified diagram of the two-phase clock generator and its start pulse. The start pulse should be low for a minimum setup time of 20 ns prior to the rising edge of $ø_1$ and for a minimum hold time of 20 ns after the edge. The start pulse should not overlap two ø1 edges going high, otherwise it will load multiple start pulses into the register in succession, one for every ø1 rising edge.

As the shift register shifts a bit down the register, the multiplexing switches are sequentially clocked and the photodiode to which the switch is connected produces an impulse signal current proportional to the photo exposure on the diode site. These video pulses are sensed at the output terminal of the video line.

In reference to the substrate, the clock amplitude should be a maximum of -11V to a minimum of -15V with the typical at -12V. For all clocks, the minimum rise and fall times are 10 ns and the maximum rise and fall times are 200 ns. It is recommended that the clock rise and fall be as symmetrical as possible. The complementary clocks should have their clock crossing between 50% to 100%. See Figure 10, which illustrates the definition of the clock crossing.

Modes of Operation

Taking advantage of the devices's four independent registers, the designer is given flexiblity in matching the various types of readout modes to suit the application. Some of the basic modes will be described.

Mode 1 - Serial Readout. Figure 11 depicts the clock timing diagram for sequential readout. The registers controlling the odd-number diodes are clocked by one complementary phase while the other clocks the shift register with even-numbered diodes. The start pulses are staggered to scan in a two-part sequence, one for the first 1024 diodes and the other for the last 1024 diodes. The integration time is the interval between start pulses on the same start line.

The signals can be combined by tying all four active lines together and the four dummy lines together and processing through a single differential preamplifier. Alternately, each line may be processed separately; the choice depends upon the noise requirements. If the limiting noise is the kTC noise of the video line capacitances, then an amplifier must terminate each video line separately. Otherwise, the video lines can be combined in parallel.

Mode 2 - Parallel Readout. The parallel clocking mode is for high-speed scanning applications, where for any pixel rate, the readout rate is two times that of the serial mode. The timing diagram is shown in Figure 12, for a single scan. In this case, all four registers are clocked in parallel; i.e., a common complementary set of clocks and a common start pulse are used on all registers. For the video processing, a preamplifier is required for each video line.

Other Modes - A variety of different operational modes can be implemented by combining the serial and parallel clocking modes. The adjacent pixels could be read on the odd and even video lines and directly subtracted from each other, thus providing direct and real time signal differencing operations.

End of Scan

The end of scan output pulses, useful primarily for test purposes, are provided when the last odd and even elements are sampled by the shift register scanning circuit. When not used, they should be shorted externally to the array substrate to avoid introduction of unwanted "glitches" into the video. When using the end-of-scan terminals, a circuit such as that shown in Figure 13 is recommended.

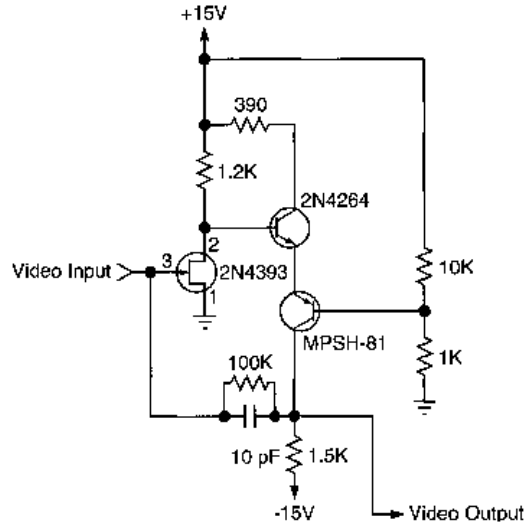


Figure 7. Simplified Diagram of Transconductance Amplifier

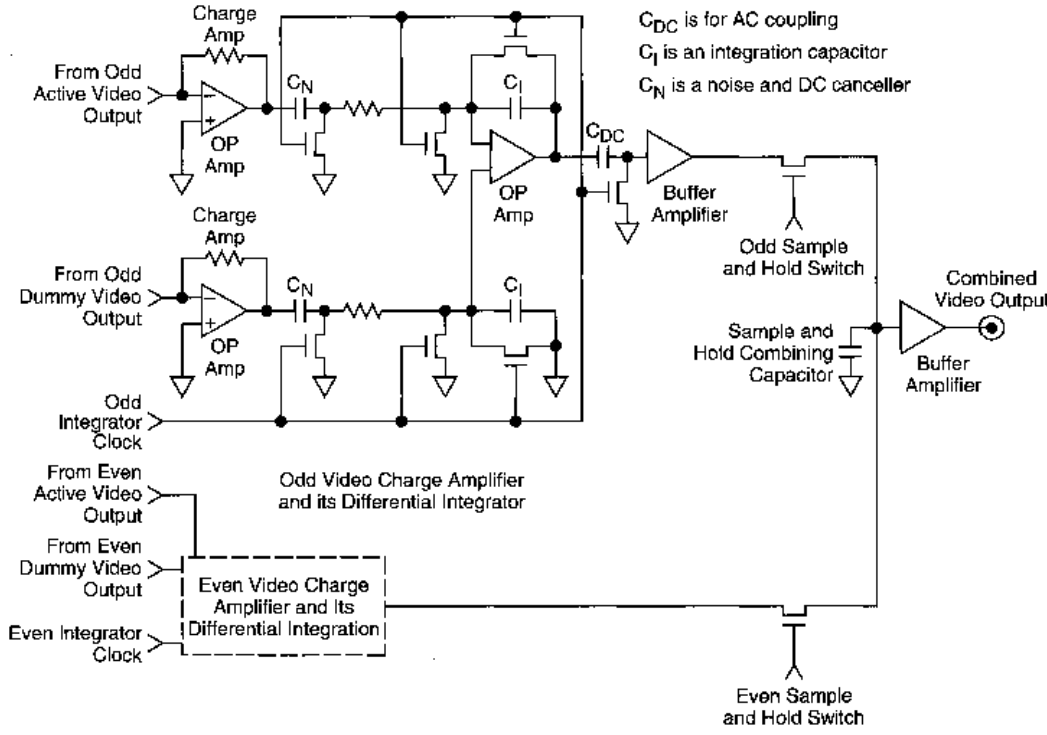


Figure 8. Simplified Differential Integration

Dark Signal and Noise

There are two components to the dark signal from the S Series self-scanning photodiode arrays. These are due to: (1) switching transients coupled into the video line through the clocks and the internal multiplex switches, and (2) the integrated dark current. A portion of the switching transient effect will be spatially random and a portion will have the periodicity of the clocks. The latter portion can be reduced by matching the clock amplitudes and rise and fall times and by good circuit layout to minimize capacitance between clocks and video lines. The peak-to-peak fixed pattern due to all switching transient effects should be less than 1% of the saturated signal. The signal due to dark current is just the dark current multiplied by the integration time. It can be arbitrarily reduced by lowering the temperature (see Figure 6) or by reducing the integration time.

There are three identifiable sources of readout noise: (1) reset noise, (2) shot noise, and (3) amplifier noise. Reset noise or kTC noise is associated with resetting the diode capacitance to a fixed voltage. Its rms value is given by (kTC)1/2/q where k is Boltmann's constant, T is the absolute temperature, q is the electronic charge, and C is the total capacitance of the photodiode (approximately 2 pF), the video line it connects to, and the capacitance of the external circuitry. At room temperature, the rms kTC noise is approximately 2400 electrons. It can be reduced somewhat by cooling. The rms dark current shot noise is the square root of the number of electrons in the dark signal charge. For example, with a room temperature dark current of 5 pA and 10 ms integration time, the rms dark current shot noise is approximately 560 electrons. Because of the exponential temperature dependence of dark current, shot noise can be reduced dramatically with a moderate amount of cooling. Amplifier noise depends on the amplifier circuit used. In general, the low video output capacitance of the S Series facilitates low amplifier noise circuits. Noise values below 2500 electrons are possible.

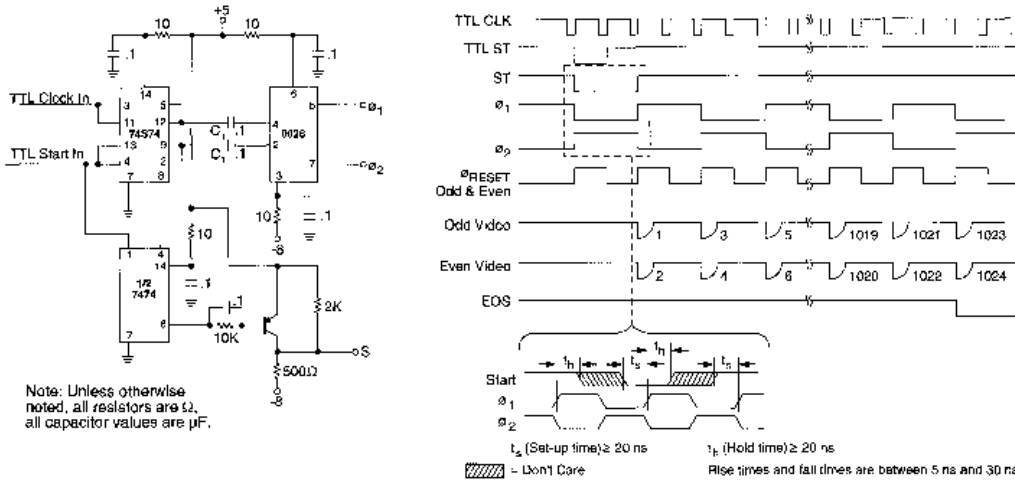


Figure 9. Simplified Diagram at a Two-phase Clock Generator and its Timing Diagram

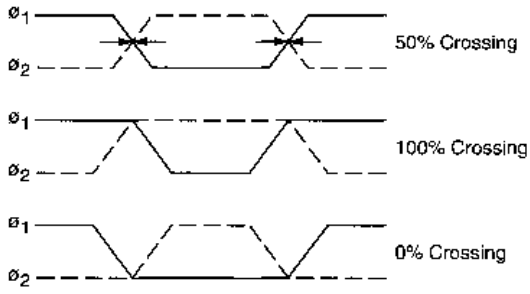


Figure 10. Clock % Crossing Definition

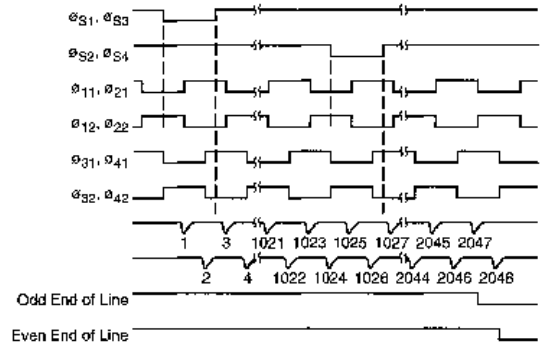


Figure 11. Timing Diagram of the Serial Mode

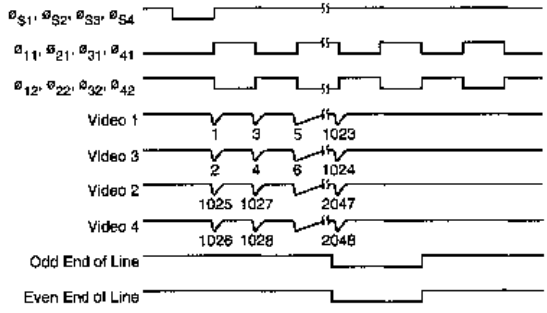


Figure 12. Timing Diagram of the Parallel Mode

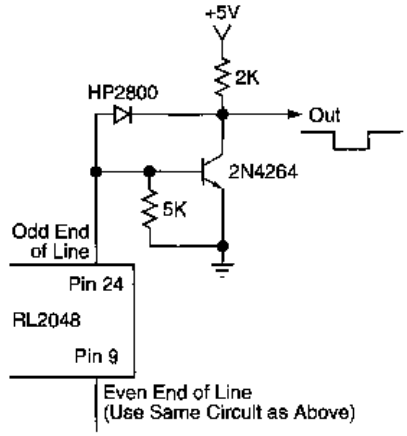


Figure 13. End-of-Scan Circuit

Table 1. Electrical Characteristics (25°C)

Parameter	Min	Typ	Max	Units
Video line bias [1]	- 4	- 5	-6	V
Clock amplitude [1]	-11	-12	-15	V
Start pulse amplitude [1]	-11	-12	-15	V
Total effective pixel output rate			5	MHz
Clock frequency			625	kHz
Capacitance of each video line (at 5V bias)				
Active video 1		35		pF
Active video 2		35		pF
Active video 3		35		pF
Active video 4		35		pF
Dummy video 1		47		pF
Dummy video 2		47		pF
Dummy video 3		47		pF
Dummy video 4		47		pF
Capacitance of each clock line (at 5V bias)				
Clock 11		95		pF
Clock 12		95		pF
Clock 21		105		pF
Clock 22		105		pF
Clock 31		95		pF
Clock 32		95		pF
Clock 41		105		pF
Clock 42		105		pF
Capacitance of each photodiode (at 5V bias)		2		pF
End of scan output resistance		5		KΩ
DC power dissipation [2]		1		mW

Notes:

1 Measured with respect to substrate. Substrate is normally run at +5V for compatibility with TTL clock circuits.

2 The AC power is given by $2C_cV_c^2f_s$ where C_c is the capacitance of each clock line, V_c is the clock voltage, and f_s is the scan frequency.

Table 2. Electro-Optical Characteristics (25°C)

Parameter	Typ	Units
Center-to-center spacing	25	µm
Aperture width	2.5	mm
Sensitivity [3]	2.8×10^{-4}	$C/J/cm^2$
Nonuniformity of response	10	±%
Saturation exposure [3]	50	nJ/cm^2
Saturation charge	14	pC
Average dark current	5	pA
Quantum efficiency [1, 3]	75	%
Spectral response peak [3]	750	nm
Spectral response range [2, 3]	250 - 1000	nm

Notes:

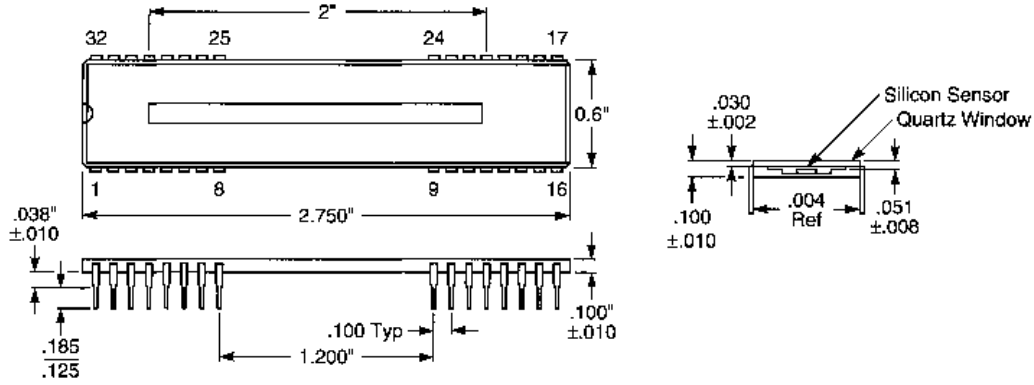
1 Typical value specified at 750 nm wavelength.

2 Sensitivity within this range is typically at least 20% of peak sensitivity.

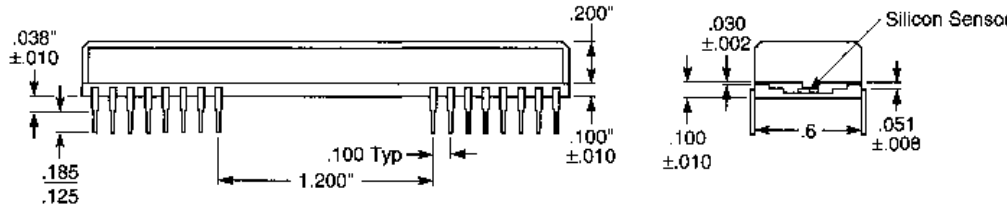
3 Specified for quartz windowed devices. Fiber optic faceplate will modify response characteristics as shown in Figure 4.

Absolute Maximum Ratings

Parameter	Min	Max	Units
Voltage applied to any terminal with respect to common	0	-20	V
Storage or operating temperature			
Quartz windowed (SAQ)	-78	+85	°C
Fiber optic (SAF)	-40	+85	°C



A. Package with Quartz Window



B. Package with Fiberoptic Window

Figure 14. Package Dimensions. Dimensions are in inches except where millimeters (mm) are indicated

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General Description

The EG&G Reticon SB series is a family of monolithic self-scanning linear photodiode arrays optimized for application in spectroscopy. The devices in this series consist of a row of silicon photodiodes, each with an associated junction capacitance on which to integrate photocurrent and a multiplex switch for periodic readout via an integrated shift register scanning circuit. The part number of each device indicates the number of elements in the array (example, 128, 256, 512, and 1024).

The SB series devices are mounted in ceramic side-brazed dual-inline packages which mate with standard 22-pin integrated circuit sockets. The 256-element array is also available in a ceramic LCC package. Pinout configurations are shown in Figure 1. Package dimensions are shown in the outline drawings of Figure 9. Standard SB devices are sealed with a ground and polished quartz window. However, an optional fiber optic faceplate version is also available in side-brazed packages. The fiber optic faceplate has 6 µm diameter fibers and a numerical aperture of 1.

Key Features

- Simultaneous integration of 128, 256, 512, or 1024 photodiode elements with 25 µm center-to-center spacing
- Each sensor element has a 100:1 aspect ratio (25 µm x 2.5 mm)
- Extremely low dark leakage current for longer integration times
- Low power dissipation to facilitate cooling
- Clock-controlled sequential readout at rates up to 10 MHz
- Single-supply operation with HCMOS-compatible inputs
- Single shift register design for simplified clocking requirements
- Differential video output to cancel clock switching transients and Fixed Pattern Noise (FPN)
- Low output capacitance for low noise
- High saturation charge for wide dynamic range
- Antiblooming function for high-contrast images
- Line Reset Mode for simultaneous reset of all photodiodes
- Wide spectral response
- Choice of quartz window or fiber optic faceplate (LCC package has only quartz window)
- On-chip diodes (two) for temperature monitoring

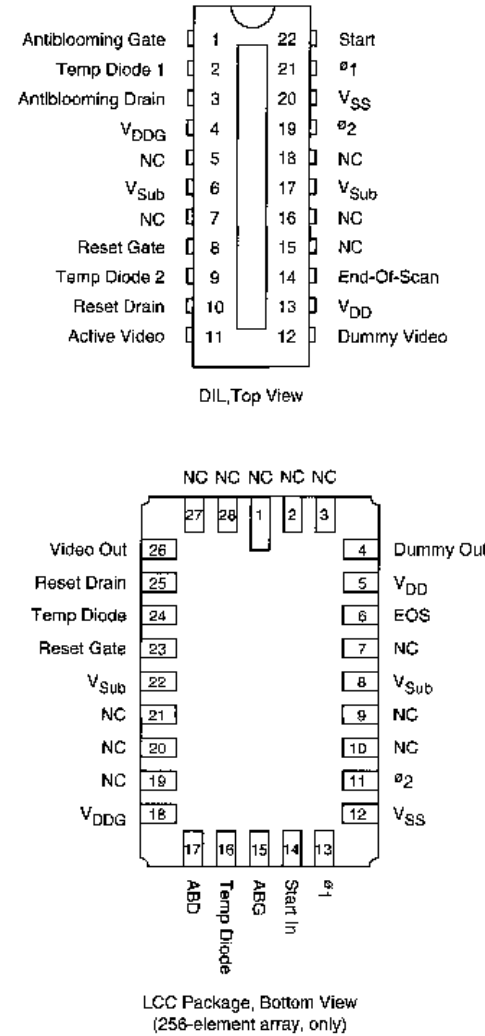


Figure 1. Pinout Configurations

Sensor Characteristics

The SB series self-scanning photodiode arrays contain 128, 256, 512, or 1024 elements (LCC package: 256 elements, only) on 25 µm centers corresponding to a density of 40 diodes/mm and an overall length of 3.2, 6.4, 12.8, or 25.6 mm. The height of the sensor elements is 2.5 mm giving each element a slit-like geometry with 100:1 aspect ratio suitable for coupling to monochromators or spectrographs. The sensor geometry is shown in Figure 3.

Charge generated by light incident on the p-type surface between two n-regions will divide between the adjacent diodes to produce the response function shown in Figure 3.

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Figure 4 shows the typical output charge as a function of exposure at 750 nm wavelength. Exposure in nJ/cm^2 is calculated by multiplying the light intensity in µW/cm^2 by the integration time in ms. Note that the response is linear with exposure up to a saturation charge of 10 pC at a saturation exposure of 35 nJ/cm^2. The sensitivity is defined as the ratio of saturation charge to saturation exposure and is 2.9 x 10^{-4} C/J/cm^2 (at 750 nm). Typical relative sensitivity as a function of wavelength is shown in Figure 5. Quantum efficiency can be obtained by dividing the sensitivity by the area of a sensor element (6.25 x 10^{-4} cm^2) and multiplying by the energy per photon in eV. Peak quantum efficiency is about 80% at 650 nm. The dark current of an SB series device is typically .20 pA at 25°C and is a strong function of temperature, approximately doubling for every 7°C increase in temperature. The dark signal charge is given by the dark current multiplied by the integration time. See Table 2 for Electro-optical Characteristics.

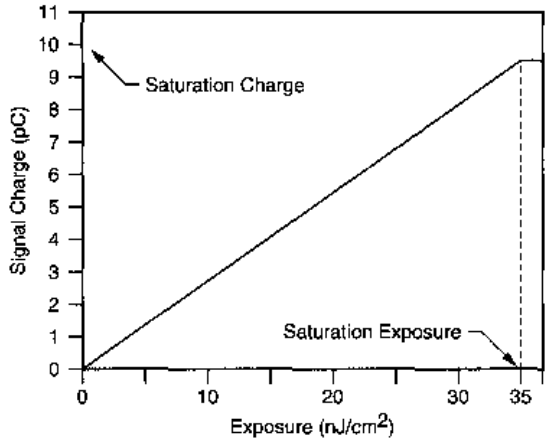


Figure 4. Typical Signal Charge versus Exposure at 750 nm Wavelength

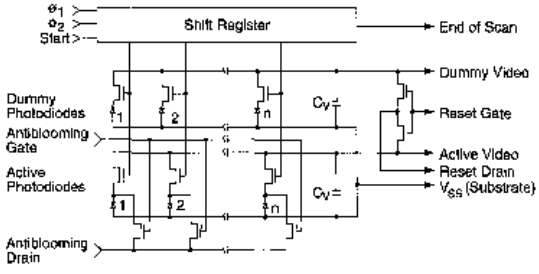


Figure 2. Equivalent Circuit

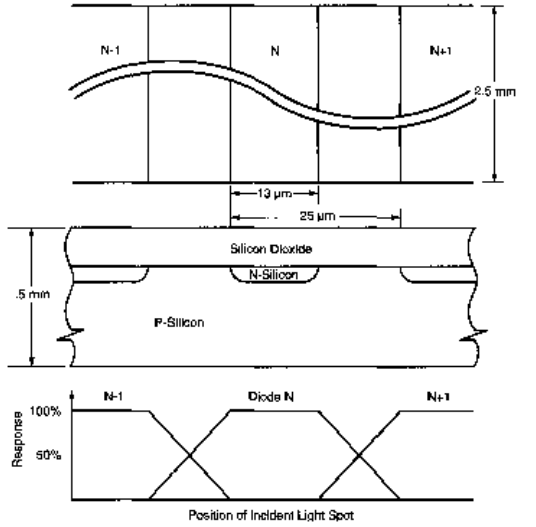


Figure 3. Sensor Geometry and Aperture Response Function

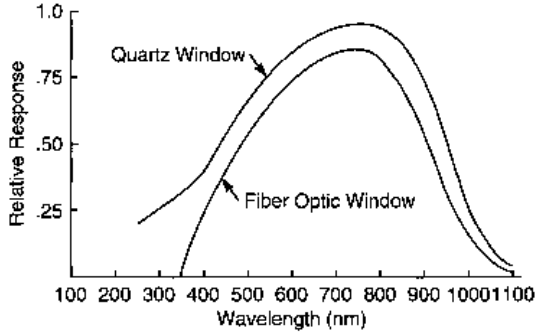


Figure 5. Typical Spectral Response

Scanning Circuit

The simplified equivalent circuit of an SB series photodiode array is shown in Figure 2. Each cell consists of an active photodiode and a dummy photodiode, both with an associated junction capacitance. These diodes are connected through MOS multiplex switches to active and dummy video lines. The shift register is driven by complementary square wave clocks with periodic start pulses being introduced to initiate each scan. The pixel sampling rate is determined by the clock frequency. Integration time is the interval between start pulses. The output signal obtained from each scan of an N-element array is a train of N charge pulses, each proportional to the light exposure on the corresponding photodiode. In addition to the signal charge, switching transients are capacitively coupled into the active video lines by the multiplex switches. Similar transients are introduced into the dummy video lines and, therefore, can be reduced and a cleaner signal recovered by reading out the video and dummy lines differentially.

Clock and Voltage Requirements

Scanning is achieved by means of an integrated shift register. The shift register is driven by complementary square wave clocks, ϕ_1 and ϕ_2. Table I gives rise and fall times and crossover points for these clock waveforms. The clock amplitude should be equal to V_{DD} - V_{SS}. With V_{DD} = 5V and V_{SS} = 0V, the clock inputs will be HCMOS-compatible. Since each photodiode is read out on a negative transition of ϕ_2 (see Figure 6), the frequency of the clock signal should be set equal to the desired video data rate.

The start pulse of similar amplitude to the clocks is required to load the shift register and initiate each readout period (each scan of the array). The start pulse is loaded when ϕ_2 is high; the start signal is pulsed high for a minimum of 10 ns during one and only one ϕ_2 clock high cycle. A timing diagram for the start and clock signals is shown in Figure 6. Caution: ϕ_1 and ϕ_2 clocks need to be continuously applied to the device. The integration period should be controlled by varying the time between start pulses.

For optimum performance and minimum switching noise, it is important that the clocks are exact complements and that their rise and fall times comply with Table 1. A recommended circuit for generating these clocks is shown in Figure 7.

End of Scan

An output pulse useful primarily for test purposes is provided two clock cycles after the last photodiode is sampled by the shift register scanning circuit. The timing of the EOS output is shown in Figure 6. The voltage levels on the EOS output will be determined by the V_{DD} and V_{SS} voltage levels supplied to the photodiode array. When V_{DD} is at +5V and V_{SS} is operated at 0V, the EOS output will be compatible with the HCMOS family of logic devices.

Amplifier Requirements

The recommended amplifier circuit for use with the SB devices is a simple current amplifier. A current amplifier

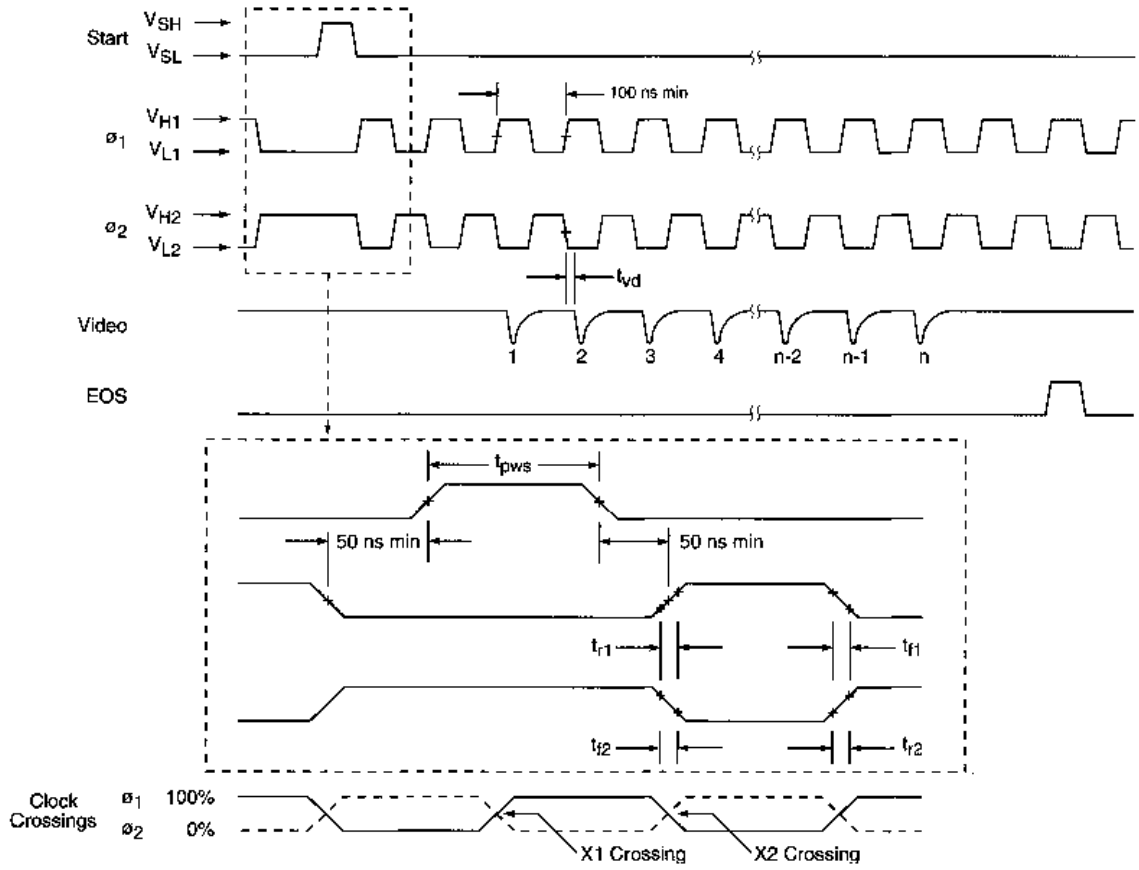


Figure 6. Timing Diagram

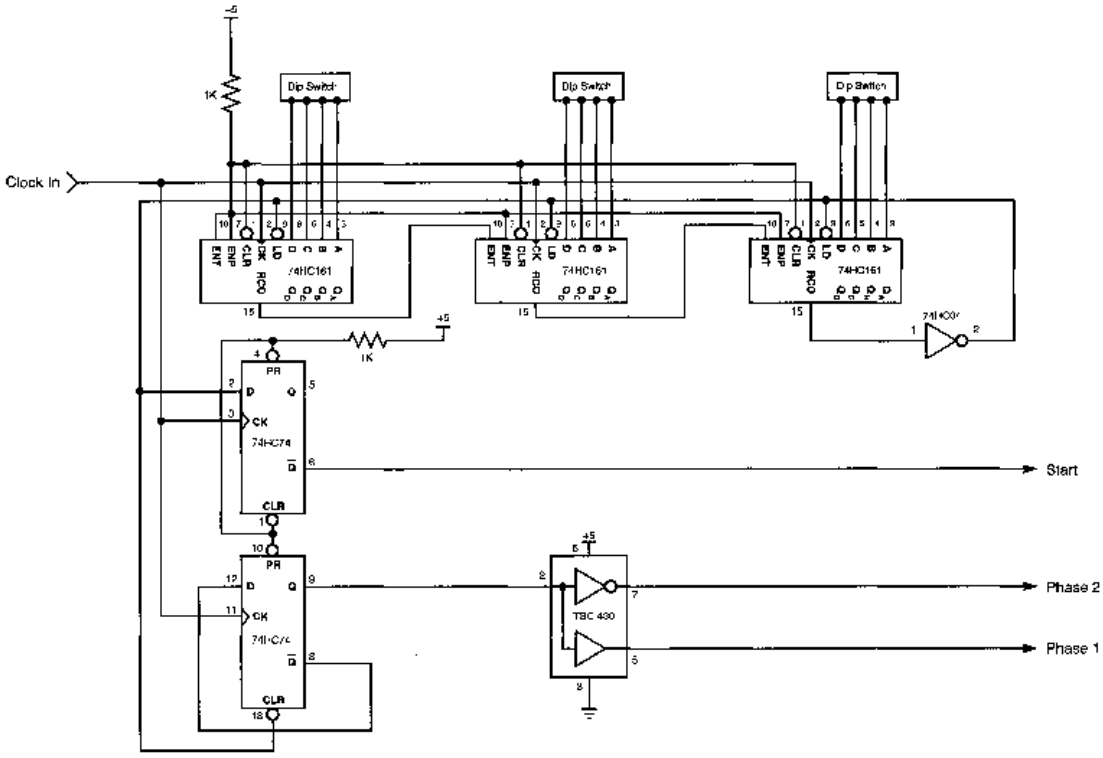


Figure 7. Two-Phase Drive Circuit

holds the video line at a virtual ground and senses the current pulses flowing into the video line to recharge the diodes through their respective multiplex switches as they are sampled in sequence. These current pulses, which each contain a charge of up to 10 pC at saturation, are converted to a train of voltage pulses corresponding to the light intensity on the various diodes. In this mode of operation, the current amplifier must provide a positive bias voltage to the video line since the photodiode anode (the p-substrate) is biased to 0V (V_{SS}). Figure 8 shows a differential recharge amplifier suitable for use with SB series devices.

Line Reset/Antiblooming Control

Under certain operating conditions, it may be desirable to control integration time independent of the line scan time (time between start pulses). This can be accomplished by the use of the Antiblooming Gate control input. When the Antiblooming Gate is held at V_{DD}, all photodiodes are simultaneously reset to the bias voltage on the antiblooming drain (typically $V_{DD}/2$). Conversely, when the antiblooming gate is held at V_{SS}, the antiblooming transistor is off and the photodiodes can then integrate photocurrent. Thus, when an active high pulse is applied to V_{ABG}, the integration time for diode 'N' then becomes the time between the negative-going transition of the antiblooming gate to the time in which diode 'N' is read out through the diode multiplex switch.

Under normal operating conditions, SB series devices do not require any blooming control due to their excellent antiblooming characteristics. However, under extremely high contrast conditions, blooming control can be implemented to further enhance this performance. In this mode of operation, a bias voltage (the same voltage as the video line bias, typically $V_{DD}/2$) is required on the antiblooming drain. The antiblooming gate is then biased to 1-3V. By adjusting the bias level on the antiblooming gate, excess charge present on the video line is shunted to the antiblooming drain.

Dark Signal and Noise

There are two components of the dark signal from the SB series. These are due to: (1) spatial variations in the switching transients coupled into the video line through the clocks and internal multiplex switches, and (2) the integrated dark current. A portion of the switching transient effect will be spatially random and a portion will have the periodicity of the clocks. The latter portion can be minimized by matching the clock amplitudes and rise and fall times and by good circuit layout to minimize capacitance between clocks and video lines. The peak-to-peak fixed pattern due to all switching transient effects should be less than 1% of the saturated signal. The dark signal due to dark current is the dark current multiplied by the integration time. It can be arbitrarily reduced by lowering the temperature or by reducing the integration time.

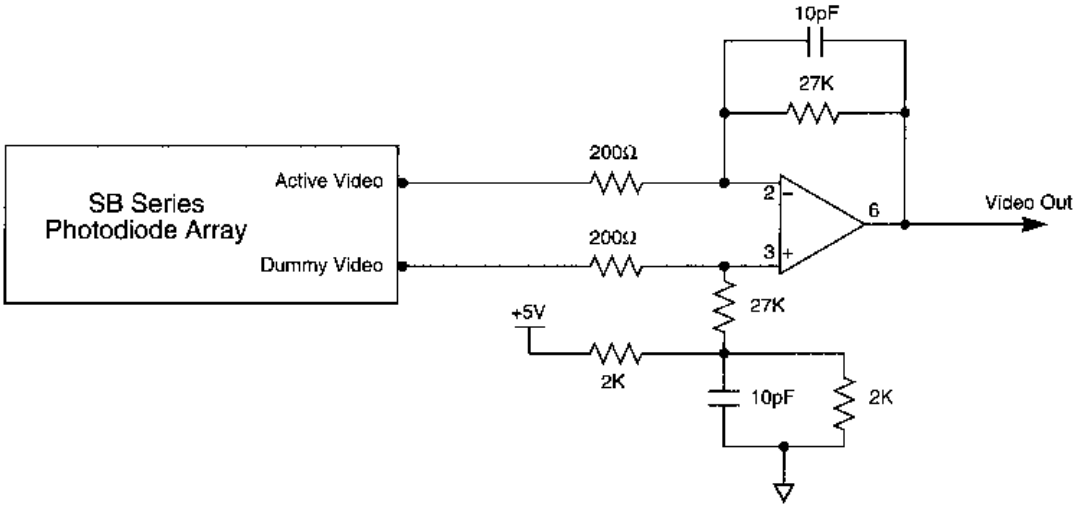


Figure 8. Differential Recharge Mode Video Amplifier

There are three identifiable sources of readout noise: (1) reset noise, (2) shot noise, and (3) amplifier noise. Reset noise is associated with resetting the diode capacitance to a fixed voltage. Its root mean square value is given by $(kTC)^{1/2}/q$ where k is Boltzmann's constant, T is the absolute temperature, q is the electronic charge and C is the total capacitance of the photodiode (approximately 4 pF), the video line it connects to, and the capacitance of the external circuitry. At room temperature, kTC noise is approximately 1500 electrons rms. It can be reduced somewhat by cooling. The rms value of the dark shot noise is the square root of the number of electrons in the dark signal charge. For example, with a room temperature dark current of .25 pA and 10 ms integration time, the rms dark current shot noise is approximately 125 electrons. Because of the exponential temperature dependence of dark current, shot noise can be reduced dramatically with a moderate amount of cooling. Amplifier noise depends on the amplifier circuit used. In general, the low video output capacitance of the SB series makes it easy to achieve low amplifier noise and values below 2000 electrons are possible.

Temperature Diodes

The SB Series arrays each have 2 on-chip diodes for sensing array temperature. The standard method of use is to force a fixed forward current (normally 10 μA) through the diodes and measure the forward diode voltage drop. For details, please refer to Application Note 127, *How to Use Reticon Temperature Diodes.*

Evaluation Circuit

A complete evaluation circuit for the SB series is available from Reticon (side-brazed package, only). The RC1030 board provides the user with an easy means of evaluating operation. The RC1030 uses an alternative circuit to that shown in Figure 7.

The RC1030 has a sample-and-held video output with a typical dynamic range of 4000:1. Provision for cooling the array using a thermal-electric cooler is provided by means of an access hole located directly beneath the array.

The board requires +5 and ±15V supplies and can be adjusted for pixel rates up to 50 kHz.

Table 1. Electrical Characteristics (25°C)
(All voltages measured with respect to V_{Sub})

Signal	Sym		Min	Typ	Max	Units
V_{DD}	V_{DD}		4.5	5	5.5	V
V_{DD} guard	V_{DDG}			V_{DD}		V
V_{SS}	V_{SS}			0		V
Antiblooming drain	V_{ABD}			V_{SS}		V
Start	V_{SH}	High	V_{DD} - .1		V_{DD}	V
	V_{SL}	Low	V_{SS}		V_{SS} + .4	V
Clock $ø_1$, $ø_2$	V_{H1}, V_{H2}	High	V_{DD} - .1		V_{DD}	V
	V_{L1}, V_{L2}	Low	V_{SS}		V_{SS} + .4	V
Reset gate	V_{HRG}	High	V_{DD} - .1		V_{DD}	V
	V_{LRG}	Low	V_{SS}		V_{SS} + .4	V
Antiblooming gate	V_{HABG}	High	V_{DD} - .1		V_{DD}	V
	V_{LABG}	Low	VSS		V_{SS} + .4	V
Video bias	V_V		2	$V_{DD}/2$	V_{DD} - 2	V
Reset drain	V_{RD}		2	$V_{DD}/2$	V_{DD}- 2	V
Clock rate			.001		10	MHz
Start rise time	t_{rs}			10	50	ns
Start fall time	t_{fs}			10	50	ns
Start pulse width	t_{pws}		10			ns
$ø_1$ Rise time	t_{r1}			10	20	ns
$ø_1$ Fall time	t_{f1}			10	20	ns
$ø_2$ Rise time	t_{r2}			10	20	ns
$ø_2$ Fall time	t_{f2}			10	20	ns
Video delay time	t_{VD}			20		ns
Clock crossings	X_1		0		50	%
	X_2		0		50	%
Capacitance $ø_1$, $ø_2$ at 5V bias [1]	C_c					
RL0128SB				26		pF
RL0256SB				27		pF
RL0512SB				31		pF
RL1024SB				35		pF
Capacitance, each video line at 2.5V bias	C_V					
RL0128SB				5		pF
RL0256SB				6		pF
RL0512SB				10		pF
RL1024SB				18		pF

Note:
1 Calculated typicals - not measured.

Table 2. Electro-Optical Characteristics (25°C)

Conditions:
Alt voltage levels set to typical values shown in Table 1
Light source is 2870°K tungsten filtered with a 750 nm bandpass filter
Video data rate = 250 kHz

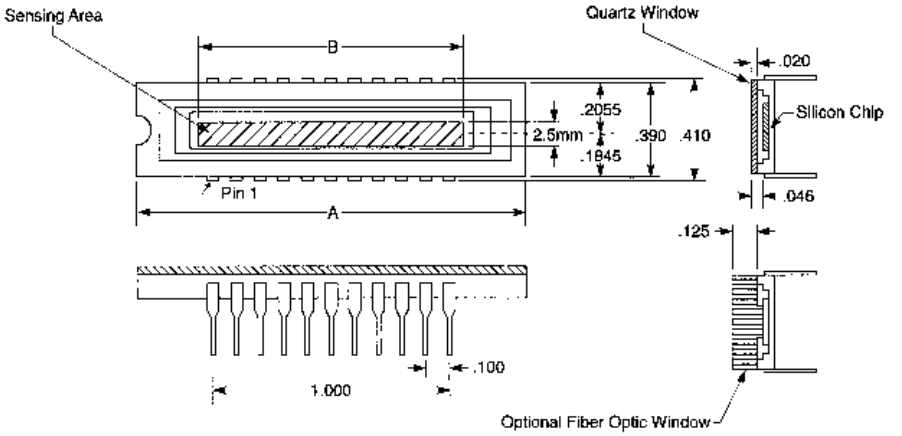
Characteristics	Typ	Max	Units
Center-to-center spacing	25		µm
Aperture width	2.5		mm
Sensitivity [1,2,3]	2.9×10^{-4}		C/J/cm²
Nonuniformity of response			
RL0128SB [2,4,5]	5	10	±%
RL0256SB [2,4,5]	5	10	±%
RL0512SB [2,4,5]	5	10	±%
RL1024SB [2,4,5]	5	10	±%
Saturation exposure (E_{SAT}) [1,2,3]	35		nJ/cm²
Saturation charge (Q_{SAT})	10		pC
Dynamic range ($Q_{sat}/Q_{noise\ (rms)}$)	31,250		
Average dark current [6]	0.20	.50	pA
Spectral response peak	750		nm
Spectral response range [5,7]	200-1000		nm

Notes:

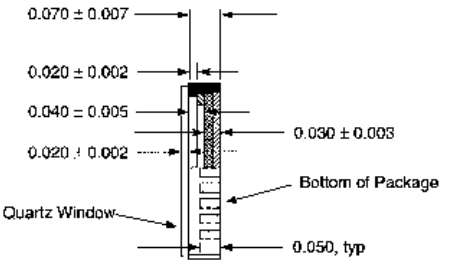
1 Measured at 2.5V video line bias
2 Peak, typical at 750 nm
3 Fiber optic faceplate will modify sensitivity as shown in Figure 5
4 +% PRNU is defined as $[(V_{max} - V_{avg})/V_{avg}] \times 100\%$ and -% PRNU is defined as $(V_{avg} - V_{min})/V_{avg}] \times 100\%$, where
V_{max} is the output of the pixel closest to saturation level,
V_{min} is the output of the pixel closest to dark level,
V_{avg} is the numerical average of all the array pixels.
The first and last pixels are not counted in this measurement.
5 Measured at an exposure level of $E_{SAT}/2$
6 Maximum dark current ≤1.5 x average dark current
7 From 250 - 1000 nm, sensitivity is typically at least 20% of its peak value.

Absolute Maximum Ratings

	Min	Max	Units
Voltage applied to any terminal with respect to substrate (V_{SS})	0	+10	V
Storage of operating temperature			
Quartz window	-78	+85	°C
Fiber optic	-40	+85	°C

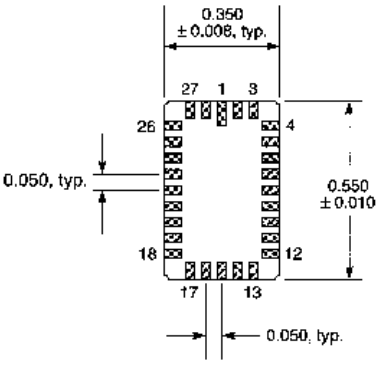


Device	A	B
RL0128SB	1.080	.1260 (3.2 mm)
RL0256SB	1.080	.2520 (6.4 mm)
RL0512SB	1.080	.5039 (12.8 mm)
RL1024SB	1.600	1.008 (25.6 mm)



LCC Package, Side View

Note: Sensing aperture in LCC is centered with respect to cavity edges



LCC Package, Bottom View

Figure 9. Package Dimensions (all dimensions are typical and in inches unless otherwise specified)

Ordering Information

Part Number	Evaluation Circuit
Quartz Window	
RL0128SBQ-011	RC1030LNN-011
RL0256SBQ-011	RC1030LNN-011
RL0512SBQ-011	RC1030LNN-011
RL1024SBQ-011	RC1030LNN-011
Fiber Optic Window	
RL0128SBF-011	RC1030LNN-011
RL0256SBF-011	RC1030LNN-011
RL0512SBF-011	RC1030LNN-011
RL1024SBF-011	RC1030LNN-011
Quartz Window, LCC Package	
RL0256SBQ-111	none

055-0264
March 1992

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General Description

The SR Series is a unique family of monolithic linear image arrays with randomly-accessible photodiode sensors. The photodiodes are accessed via 5V binary address lines. Like the Reticon S Series, the SR sensors are 25 µm by 2500 µm for the high sensitivity required in spectroscopy and scientific applications.

The SR Series devices are mounted in 34 pin, .6" wide, side-brazed ceramic dual-inline packages as shown in Figure 8. Pin descriptions are shown in Table 3.

Key Features

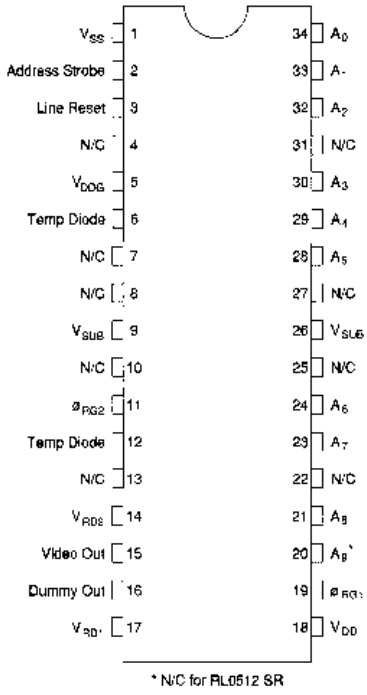
- Randomly accessible photodiode sensors - easily accessed with 5V binary-encoded MOS-level address lines
- Sensor structure based on Reticon's S Series arrays – sensor spacing 25 µm center-to-center with aspect ratio of 100:1 (25 µm by 2500 µm)
- 512 and 1024 element versions
- Very low dark leakage current for longer integration times
- Low power dissipation
- Address clock rates up to 1 MHz
- Very low output capacitance for low noise
- High saturation charge for high dynamic range
- Choice of quartz window or fiberoptic faceplate

Sensor Characteristics

The family of SR Series devices consists of 512 and 1024 photodiode sensing elements on 25 µm centers corresponding to a density of 40 diodes/mm and an overall length of approximately 12.8 and 25.6 mm, respectively. The height of the sensor elements is 2.5 mm, giving each sensor a slit-like geometry with a 100:1 aspect ratio suitable for coupling to monochromators or spectrographs. The equivalent circuit is shown in Figure 2 and sensor geometry in Figure 3.

Charge generated by light incident on the p-type surface between two n-regions will divide between the adjacent diodes to produce the response function shown in Figure 3. The photo response profile as shown is a function not only of the silicon geometry, but also of the wavelength. See Reprint #IA-6, *Design Considerations for a Solid-State Image Sensing System*, available from EG&G Reticon. Typical relative response as a function of wavelength is shown in Figure 4.

A typical optical-to-electrical transfer function at 750 nm wavelength is shown in Figure 5. Exposure in njoules/cm^2 is calculated by multiplying the irradiance (µwatt/cm^2) by the integration time (msec). Note that the response is linear with exposure up to the saturation charge of 10 pcoul at a saturation exposure of 40 njoules/cm^2. The sensitivity is defined as the ratio of the saturation charge to the saturation exposure and is 2.5 x 10^{-4} coul/joule/cm^2 (at 750 nm). Quantum efficiency can be obtained by dividing the sensitivity by the area of a sensor element (6.25 x 10^{-4} cm^2) and multiplying by the energy per photon in eV. Peak quantum efficiency is about 80% at 650 nm.



* N/C for RL0512 SR

Figure 1. Pinout Configuration

The dark current of the SR Series device is typically 0.5 pA per diode at 25°C and is a strong function of temperature. The general "rule of thumb" is that the current doubles with every 7°C. The dark signal charge is given by the dark current multiplied by the integration time.

Device Operation

The equivalent circuit of the SR Series is shown in Figure 2. It is composed of five sections: (1) an address decoder; (2) an address strobe; (3) a line reset; (4) an array of active photodiodes and an array of dummy photodiodes; and (5) two video lines (one for the active diodes and the other for the dummy diodes), each with an associated reset switch.

A single sensor or photosite is selected by the address lines via the address decoder. When the multiplexing gate is activated by the address strobe, the photo-converted charge in the active diode is placed on the video line and sensed at the output. The addressed photodiode is automatically reset by the readout operation and will start integrating charge for the next scan after it is deselected.

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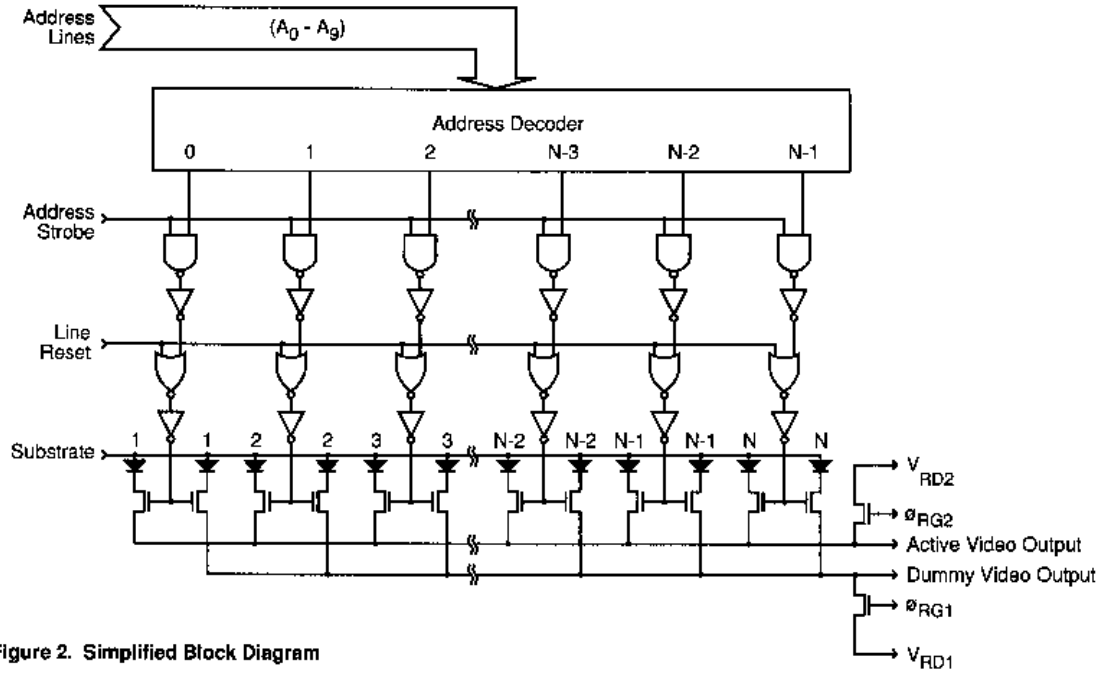


Figure 2. Simplified Block Diagram

The line reset input is used to simultaneously reset all of the diodes. When this input is activated, all of the diodes are recharged and, if exposed, will start integrating the photo converted charges simultaneously. Otherwise, this reset function can serve to recharge the diodes for shutter operation or flash exposures. A line reset pulse (positive-going to +5V) should last at least 2 µsec, with 10 - 15 µsec preferred for more complete resetting.

The dummy diodes serve to differentially cancel most of the fixed-pattern noise generated from the clocks. When a diode is selected, both the active and the dummy diodes are simultaneously connected to their respective video lines. The resulting charges are read simultaneously, and can be differentially subtracted by an external differencing amplifier.

Signal Extraction Circuits

Figure 6 shows a simplified example of two charge sensing amplifiers with their outputs differentially connected to a resettable integrator along with its associated timing diagram. The voltage levels at the output of the integrator, representing the integrated charges, can then be sampled and held.

In applications where noise performance is not the limiting criteria, a simpler circuit can be implemented. The accessed signal charges from a selected diode can be deposited directly on the video line and then discharged just prior to accessing the next photodiode. The video lines are discharged with the active and dummy reset switches. Figure 7 shows a typical method and timing diagram for buffering the video line and using it as a holding capacitor. In this mode, the video line exhibits the characteristics of a MOS capacitor. The active and dummy outputs can be differentially processed, if desired. In cases where fixed pattern noise can be ignored, the dummy line can be tied to a potential equal to the active video line.

Clock Requirements

All of the clock input levels are designed to operate with 5V CMOS levels. The decoder requires binary encoded addresses. The pin out diagram of Figure 1 shows the address inputs starting with A_0 as the least significant bit. The selected diode site is clocked out with the address strobe. The signal charges appear at the output of the video line with the rising edge of the address strobe.

Temperature Reference Diode

There are two temperature diodes, one at each end of the SR devices for temperature monitoring. The diodes are forward biased by applying a negative potential to the input pin with respect to the substrate (V_{SUB}). The anode of each temperature diode is internally connected to the substrate (V_{SUB}). Since there are several methods which can be used to monitor temperature with the diodes, and since each will require device as well as circuit calibration, the terminals of the diodes are provided for the user to calibrate and to use as desired. Examples of the different methods are as follows: (1) One method is to measure the open circuit junction voltage as a function of temperature. This method will require calibration of an external buffer amplifier, which is used to isolate the diode terminal from the external circuit. (2) Another method is to reverse bias the diode and measure the leakage current as a function of temperature. This method will require calibration of the leakage current. (3) Another method is to measure the forward diode drop as a function of temperature. This method not only requires the calibration of forward voltage drop as a function of temperature, but it requires drawing current through the substrate which will degrade performance as well as cause localized heating in the substrate. Charge injected into the substrate will diffuse into nearby pixels. If this method is used, forward biasing should

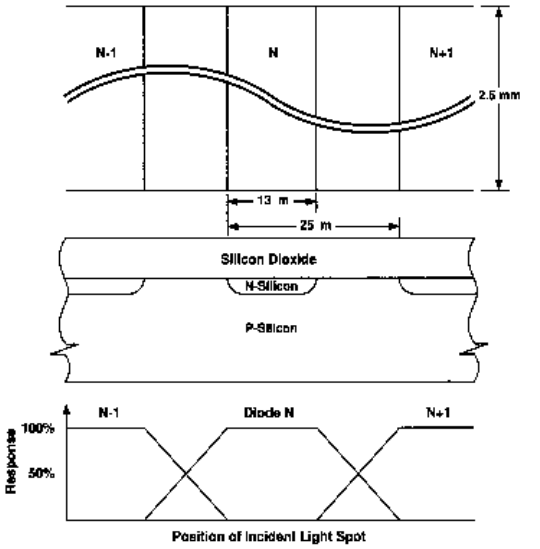


Figure 3. Sensor Geometry and Aperture Response Function

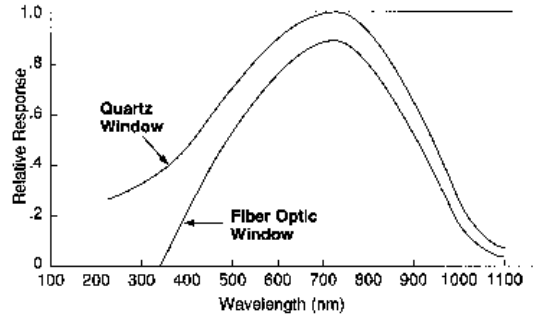


Figure 4. Typical Spectral Response

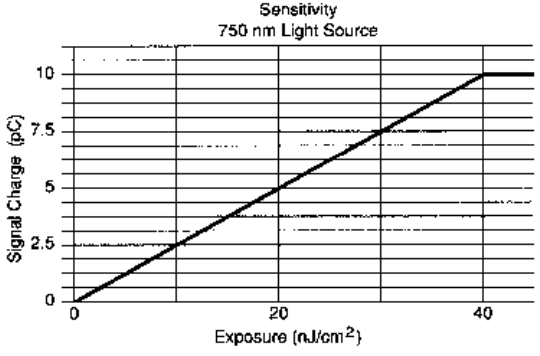


Figure 5. Optical-electrical Transfer Function

only occur during output scans that can be discarded. Moreover, a few scans should occur after the temperature diodes are turned off to "clean out" the substrate. If the temperature diodes are not used, these pins should be tied to ground.

Dark Signal and Noise

There are two components of the dark signal from the SR Series random access arrays. These are due to: (1) Spatial variations in the switching transients coupled into the video line through the clocks, and (2) the integrated dark current. A portion of the switching transient effect will be spatially random. Keeping the clock transient effects to a minimum requires strict observation of good layout techniques, such as splitting of grounds between the digital and analog circuits. The dark current leakage can be controlled by the integration time or by cooling the device. The dark current can also be mostly cancelled if the integration time of the given photo site is kept constant between readouts, because its leakage value can be stored and subtracted from each of the succeeding scans.

Evaluation Circuit

A complete evaluation circuit for the SR Series arrays is available from EG&G Reticon. The RC1010/RC1011 boardset provides the user with an easy means of evaluating the operation and performance of the SR devices. The board set allows the user to address the devices via an on-board EPROM or inputting the address through a 25-pin D-type connector. It requires +5 and ±15V supplies, and has a sample-and-held video output with a typical dynamic range of 2000:1. Provisions for cooling the array using a thermoelectric cooler are provided by means of an access hole located directly beneath the array.

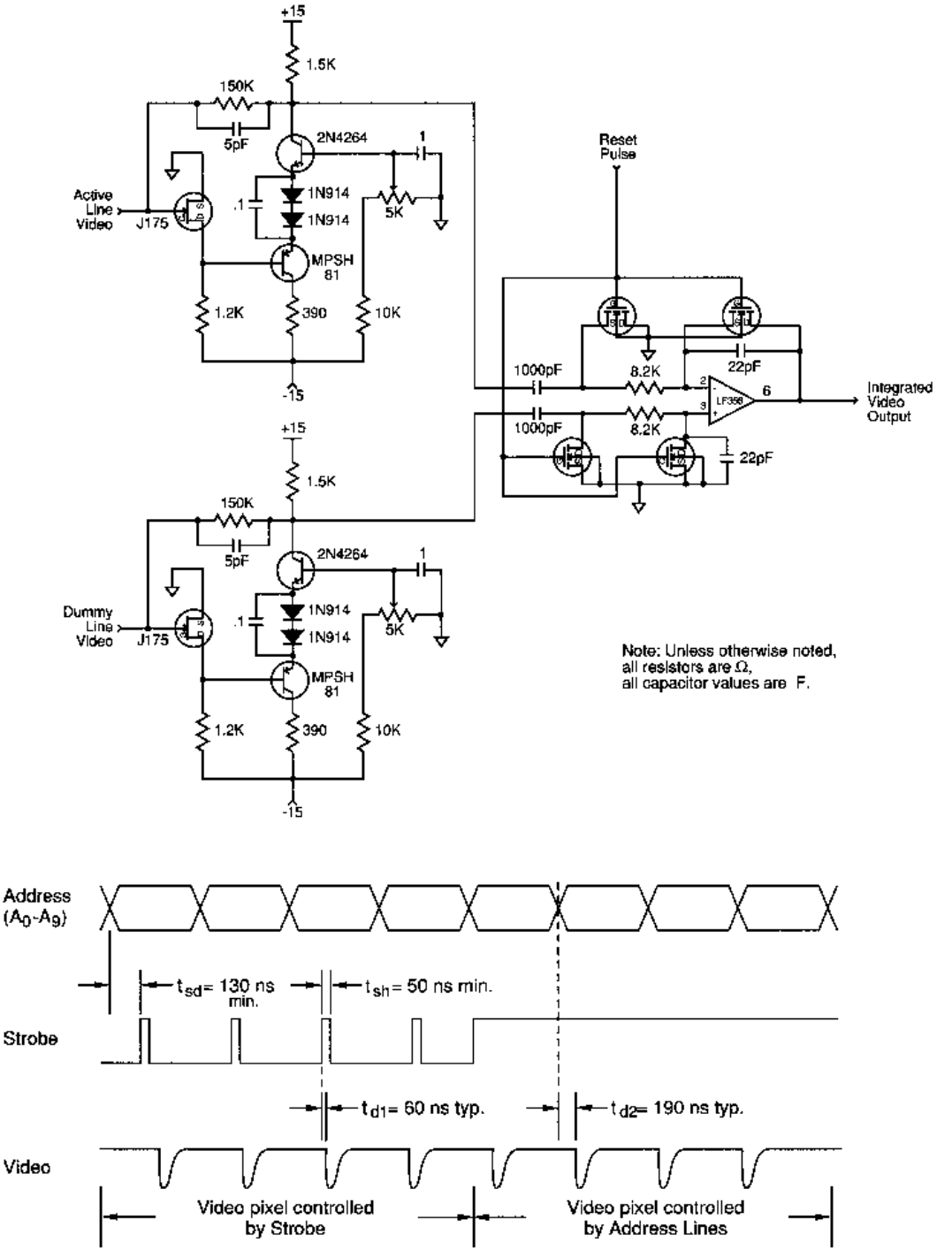
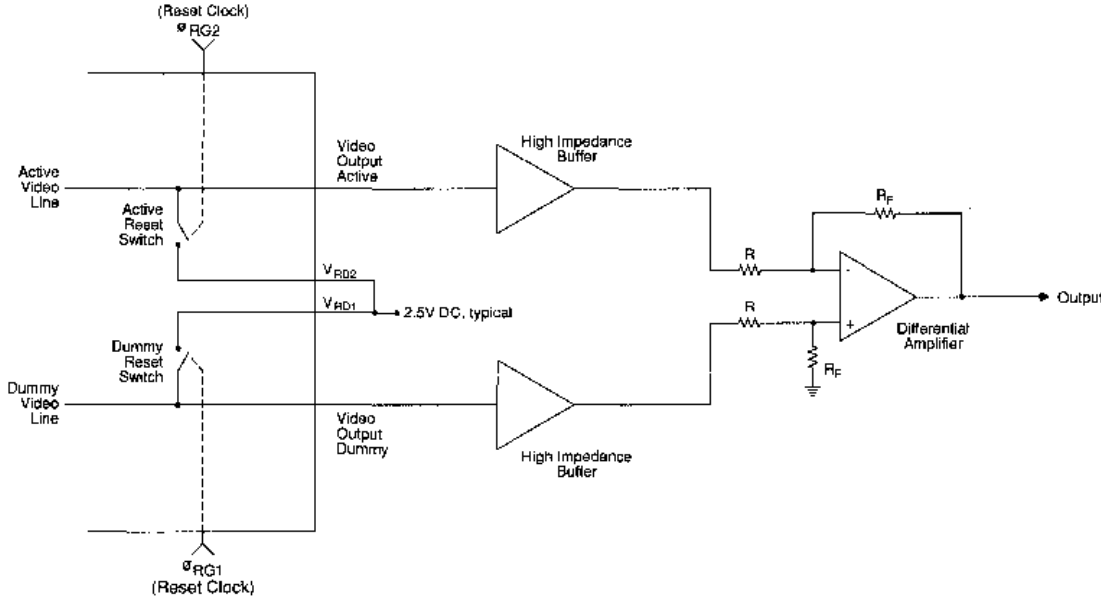


Figure 6. Charge-Sensing Amplifiers with Differential Integrator and Associated Timing Diagram



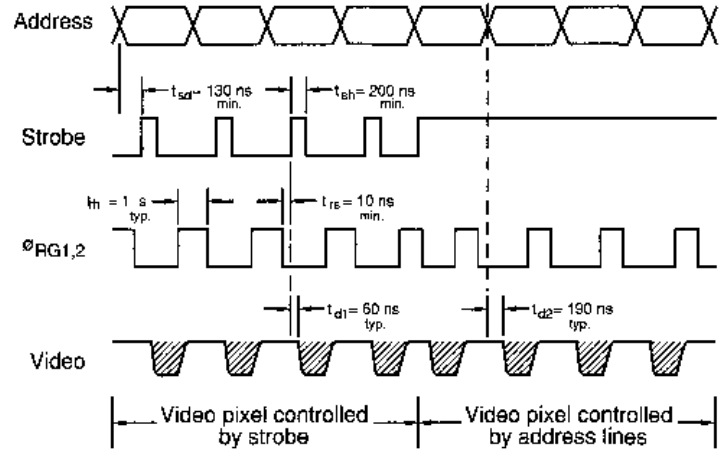


Figure 7. Simplified Circuit for Buffered Video Line Reset Operation and Associated Timing Diagram

Table 1. Electrical Characteristics (25°C)

	Min	Typ	Max	Units
V_{DD}	4.5	5.0	5.5	V
V_{DDG}	4.5	5.0	5.5	V
V_{SS}		0		
Video line bias	+2	$V_{DD/2}$	$V_{DD/2}$	V
Clock and address lines amplitude	V_{DD}-.5	+5	V_{DD}	V
Clock repetition rate			1	MHz
Capacitance of each clock line (@ 5V bias)				
RL0512SR		10		pF
RL1024SR		15		pF
Capacitance of each video line (@ 2.5V bias)				
RL0512SR		12		pF
RL1024SR		20		pF
Capacitance of each photodiode (@ 2.5V bias) [1]		4		pF
DC power dissipation		1		mW

Notes:
[1] Calculated typicals, not measured

Table 2. Electro-Optical Characteristics (25°C) [5]

	Typ	Units
Center-to-center spacing	25	µm
Aperture width	2.5	mm
Sensitivity [3,6]	2.5×10^{-4}	coul/joule/cm^2
Nonuniformity of response [4,5]	10	±%
Saturation exposure [3]	40	nJ/cm^2
Saturation charge	10	pC
Average dark current	0.5	pA
Quantum efficiency [1,3]	80	%
Spectral response peak	750	nm
Spectral response range [2,3]	200-1000	nm

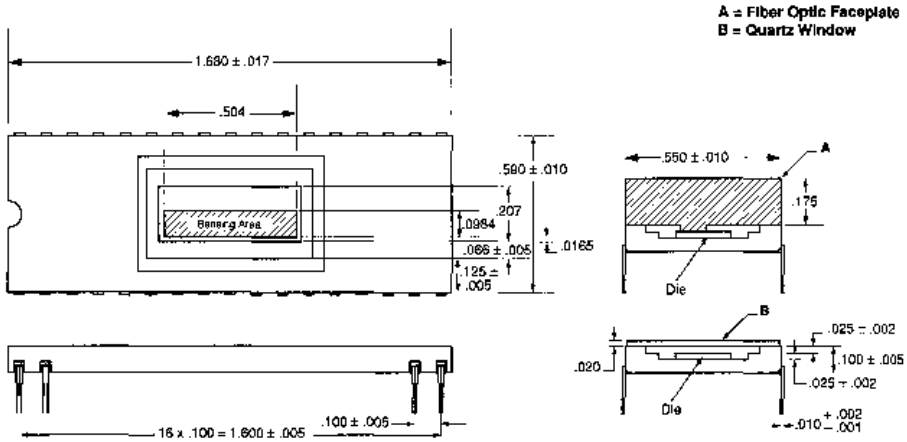
Notes:
[1] Typical value specified at 750 nm wavelength.
[2] From 250-1000 nm sensitivity ≥20% of peak value.
[3] Specified for quartz windowed devices. Fiber optic faceplate will modify response characteristics as shown in Figure 6.
[4] Measured at 50% V_{SAT} with a 2870°K incandescent tungsten source filtered with a Fish-Schurman HA-11 heat absorbing filter. First and last diodes are ignored.
[5] Data rate = 100 kHz. Device operated in serial readout mode. $V_{DD} = V_{DDG} = +5V$.
[6] At 750 nm.

Table 3. Pin Descriptions of Figure 2

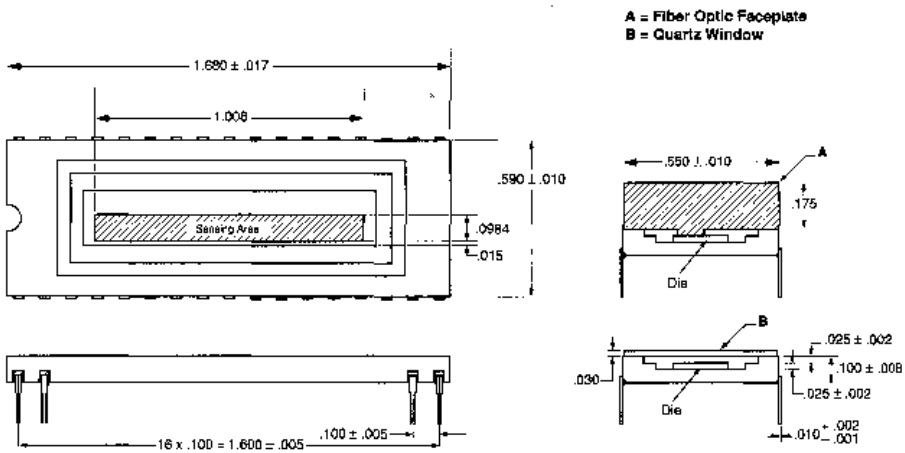
Pin Number	Description
1	V_{SS} - negative supply (GND)
2	Address strobe - latches address bits. Video clocked out on rising edge of strobe
3	Line reset - simultaneous reset of all diodes
5	V_{DDG} - same potential as V_{DD}
6, 12	Temperature diodes - one on each end of die for temperature measurements
9, 26	V_{SUB} - substrate (GND)
11, 19	ϕ_{RG2}, ϕ_{RG1} - active and dummy video line reset gates
14, 17	V_{RD2}, V_{RD1} - active and dummy video line reset drains (+2.5V)
15	Active video output
16	Dummy video output
18	V_{DD} - positive supply (+5V)
34, 33, 32, 30, 29, 28, 24, 23, 21, 20	A0-A9 - address bits. Open collector TTL or CMOS levels (GND to +5V)
All other pins	No connection (should be tied to GND for best noise immunity)

Absolute Maximum Ratings

	Min	Max	Units
Voltage applied to any terminal with respect to common	0	7	V
Storage or operating temperature			
Quartz windowed	−70	+85	° C
Fiber optic faceplate	−40	+85	° C



512SR



1024 SR

Figure 8. Package Dimensions

Ordering Information

Part Number	Window	Evaluation Circuit
RL0512SRQ-011	Quartz	RC1010LNN-011/ RC1011LNN-011
RL1024SRQ-011	Quartz	RC1010LNN-011/ RC1011LNN-011
RL0512SRF-011	Fiber optic	RC1010LNN-011/ RC1011LNN-011
RL1024SRF-011	Fiber optic	RC1010LNN-011/ RC1011LNN-011

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General Description

The Reticon T series is a family of monolithic self-scanning linear photodiode arrays optimized for application in spectroscopy. The devices in this series consist of a row of silicon photodiodes, each with an associated junction capacitance in which to integrate photocurrent and a multiplex switch for periodic readout via an integrated shift register scanning circuit. The part number of each device indicates the number of elements in the array (e.g., 64, 128, 256, 512).

The T series devices are mounted in ceramic side-brazed dual-inline packages which mate with standard 22-pin integrated circuit sockets. The pinout configuration is shown in Figure 1. Package dimensions are shown in the outline drawing of Figure 11. Standard T series devices are sealed with a ground and polished quartz window. However, the optional fiber optic faceplate version shown in Figure 11 is also available. The fiber optic faceplate has 6 µm diameter fibers and a numerical aperture of 1.0.

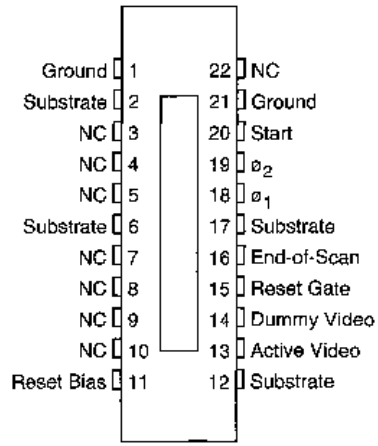


Figure 1. Pinout Configuration

Key Features

- Simultaneous integration on 64, 128, 256, or 512 photodiode sensor elements with 50 µm center-to-center spacing
- Each sensor element has a 50:1 aspect ratio (50 µm x 2.5 mm)
- Integration times as short as 64 µsec or as long as 0.3 sec are possible at room temperature. Integration times of minutes or even hours without sensors saturating can be achieved by cooling.
- Low power dissipation (less than 1 mW) to facilitate cooling
- Clock controlled sequential readout at arbitrary total effective data rates up to 2.5 MHz (f_C = 1.25 MHz max.)
- Differential output to cancel clock switching transients and fixed patterns
- Low output capacitance for low noise
- High saturation signal charge (28 pC) for wide dynamic range
- Wide spectral response (200-1000 nm)
- Choice of quartz window or fiber optic faceplate
- Standard 22-lead dual-inline integrated circuit package

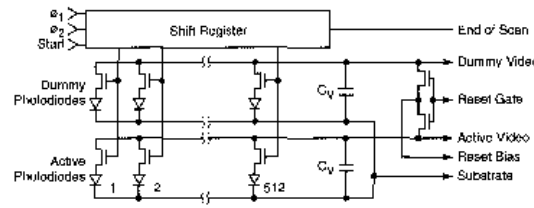


Figure 2. Equivalent Circuit

Sensor Characteristics

The Reticon T series self-scanning photodiode arrays contain 64, 128, 256, or 512 silicon diode sensor elements on 50 µm centers corresponding to a density of 20 diodes/mm and an overall length of 3.2, 6.4, 12.8, or 25.6 mm. The height of the sensor elements is 2.5 mm, giving each element a slit-like geometry with 50:1 aspect ratio suitable for coupling to monochromators or spectrographs. The sensor geometry is shown in Figure 3.

Charge generated by light incident on the n-type surface between two p-regions will divide between the adjacent diodes to produce the response function shown in Figure 3.

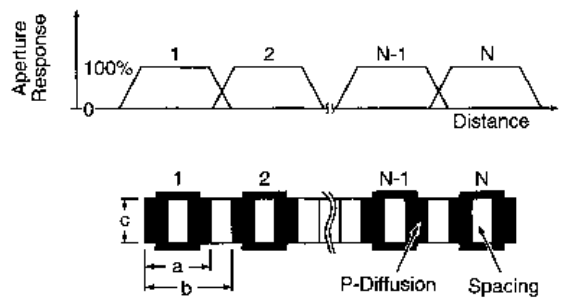


Figure 3. Sensor Geometry and Aperture Response Function

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Figure 4 shows typical output charge as a function of exposure at 750 nm wavelength. Exposure in nJ/cm^2 is calculated by multiplying the light intensity in µW/cm^2 by the integration time in msec. Note that the response is linear with exposure up to a saturation charge of 28 pC at a saturation exposure of 50 nJ/cm^2. The sensitivity is defined as the ratio of saturation charge to saturation exposure and is 4.4 x 10^{-4} C/J/cm^2 (at 750 nm). Typical sensitivity as a function of wavelength is shown in Figure 5. Quantum efficiency can be obtained by dividing the sensitivity by the area of a sensor element (6.25 x 10^{-4} cm^2) and multiplying by the energy per photon in eV. Peak quantum efficiency is about 80% at 650 nm. The dark current of a T series device is typically about 4 pA per diode at 25°C and is a strong function of temperature as shown in Figure 6. The dark signal charge is given by the dark current multiplied by the integration time.

Scanning Circuit

A simplified equivalent circuit of an RL0512T photodiode array is shown in Figure 2. Each cell consists of a photodiode and a dummy diode, both with an associated junction capacitance. These diodes are connected through MOS multiplex switches to video and dummy recharge lines. The shift register is driven by two-phase clocks with periodic start pulses being introduced to initiate each scan. The cell-to-cell sampling rate is determined by the clock frequency.

The integration time is the interval between the start pulses. The output signal obtained from each scan of an N element array is a train of N charge pulses, each proportional to the light exposure on the corresponding photodiode. In addition to the signal charge, switching transients are capacitively coupled into the video line by the multiplex switches. Similar transients are introduced into the dummy line and, therefore, can be reduced and a cleaner signal recovered by reading out the video and dummy lines differentially.

Clock and Voltage Requirements

Scanning is by means of an integrated shift register. The shift register is driven by a two-phase clock. The clock phases may be complementary square waves, or they may have a shorter negative duty cycle. In no case should ϕ_1 and ϕ_2 be negative simultaneously, as this will cause the scan to be terminated. Figure 7 shows a simple two-phase clock drive circuit and its related timing diagram.

In the specifications all voltages are expressed with respect to the substrate. However, for compatibility with TTL clocks and ease of signal extraction, it is recommended that the substrate be run at +5V. The clock phases should then swing between +5 and -7V nominal. The start pulse should overlap one positive going transition of ϕ_1 with appropriate set-up and hold times as shown in Figure 7.

End of Scan

An output pulse, useful primarily for test purposes, is provided when the last element is sampled by the shift register scanning circuit. When not used, it should be shorted externally to the array substrate to avoid introduction of unwanted "glitches" into the video. The voltage excursion on the end-of-scan terminal (when used) should be minimized by using a circuit such as that shown in Figure 8.

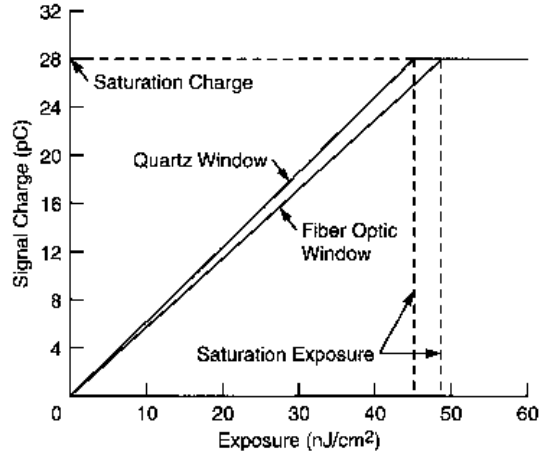


Figure 4. Signal Charge Versus Exposure at 750 nm Wavelength

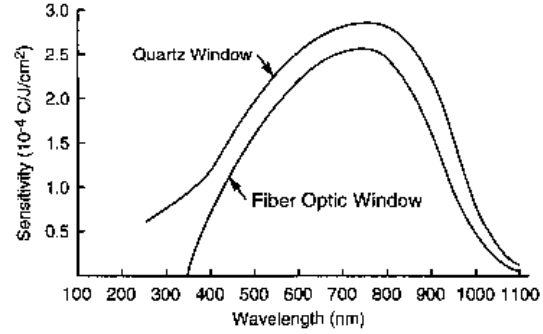


Figure 5. Typical Spectral Response

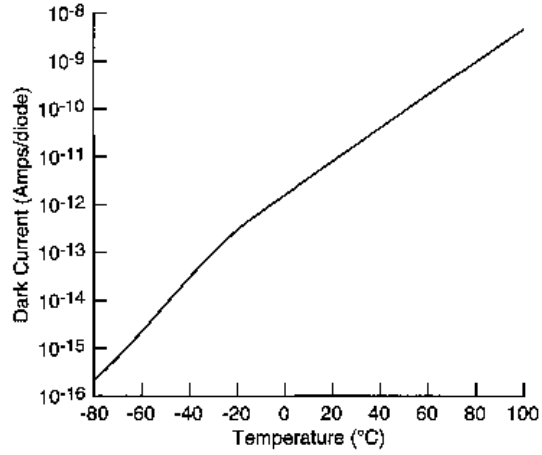


Figure 6. Temperature Dependence of Dark Current

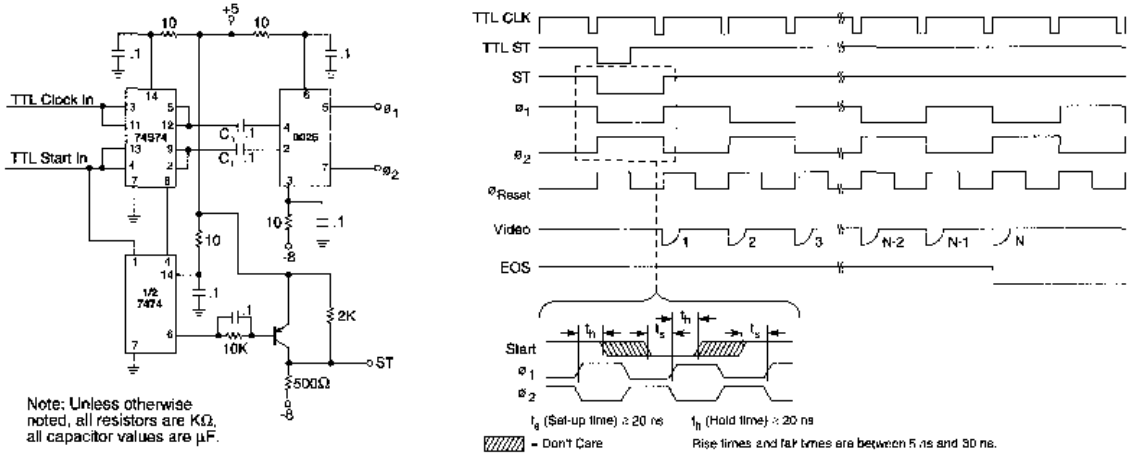


Figure 7. Simple Two-Phase Clock Drive Circuit and Related Timing Diagram

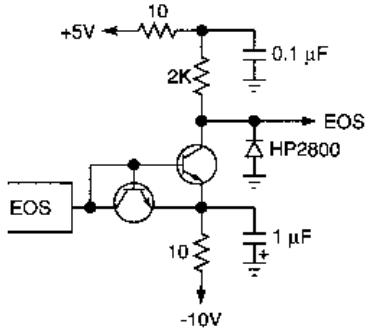


Figure 8. End-of-Scan Circuit

Amplifier Requirements

Two types of amplifier circuits are in common use with Reticon photodiode arrays. These include: (1) a simple current amplifier, and (2) a video line integration, sample-and-hold circuit. A current amplifier holds the video line at virtual ground and senses the current pulses flowing into the video line to recharge the diodes through their respective multiplex switches as they are sampled in sequence. These current pulses, each containing a charge of up to 28 pC at saturation, are converted by the amplifier to a train of voltage pulses whose level corresponds to the exposure on the various diodes.

With a video line integration, sample-and-hold circuit, the video line is reset to ground prior to closing the multiplex switch to each diode. When the switch is closed, charge divides between the diode and the video line and the resulting change in video line voltage is sampled and held. The video line and diode are then reset to ground prior to opening the multiplex switch to the next diode. The result is a boxcar output waveform.

Dark Signal and Noise

There are two components to the dark fixed pattern signal from the T series arrays. These are due to: 1) spatial variations in the switching transients coupled into the video line through the clocks and the internal multiplex switches, and 2) variation in the integrated dark current. A portion of the switching transient effect will be spatially random and a portion will have the periodicity of the clocks. The latter portion can be minimized by matching the clock amplitudes and rise and fall times and by good circuit layout to minimize capacitance between clocks and video lines. The peak-to-peak fixed pattern due to all switching transient effects should be less than 1% of the saturated signal. The fixed pattern due to dark current is just the variation in dark current multiplied by the integration time. It can be arbitrarily reduced by lowering the temperature or by reducing the integration time. This is not to be confused with the average dark current as shown in Figure 6.

There are three identifiable sources of readout noise: 1) reset noise, 2) shot noise, and 3) amplifier noise. Reset noise or kTC noise is associated with resetting the diode capacitance to a fixed voltage. Its rms value is given by $(kTC)^{1/2}/q$ where k is Boltzmann's constant, T is the absolute temperature, q is the electronic charge, and C is the total capacitance of the photodiode (approximately 4 pF), the video line, and the capacitance of the external circuitry. At room temperature, the kTC noise of the 512T is approximately 2100 electrons. It can be reduced somewhat by cooling. The rms dark current shot noise is the square root of the number of electrons in the dark signal charge. For example, with a room temperature dark current of 5 pA and 10 msec integration time, the rms value of the shot noise is approximately 560 electrons. Because of the exponential temperature dependence of dark current, shot noise can be reduced dramatically with a moderate amount of cooling. Amplifier noise depends on the amplifier circuit used. In general, the low video output capacitance of the T series makes it easier to achieve low amplifier noise and values below 2200 electrons are possible.

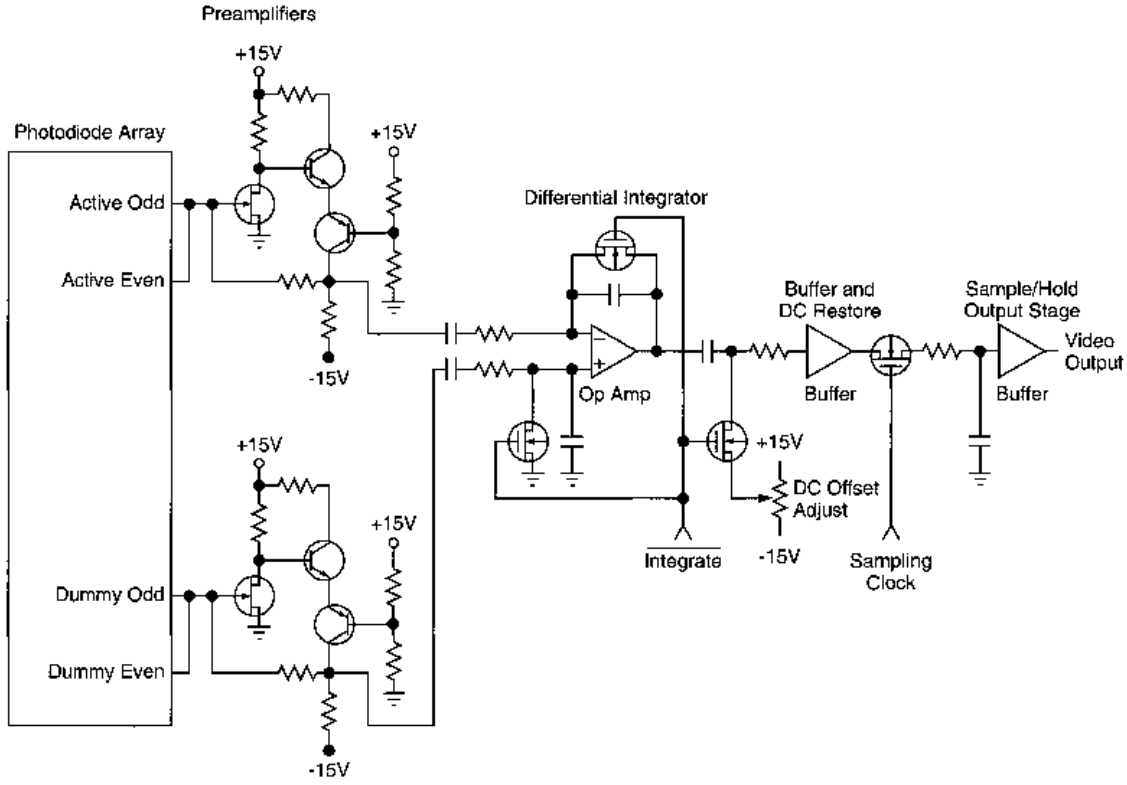


Figure 9. Simplified RC1000/RC1001 Evaluation Board Output Circuit

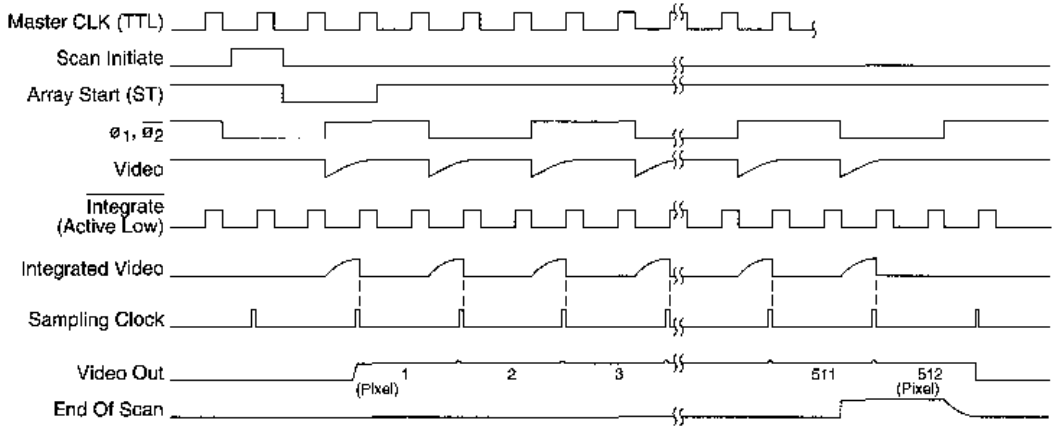


Figure 10. Timing Diagram of RC1000/1001 Evaluation Board

Evaluation Circuit

A complete evaluation circuit for the T series arrays is available from Reticon. The RC1000/RC1001 evaluation boardset provides the user an easy means to evaluate the operation of the T series photodiode arrays.

The RC1000/RC1001 has a sample-and-held video output with a typical dynamic range of 4000:1. Provision for cooling the array using a thermo-electric cooler is provided by means of an access hole located directly beneath the array.

The boardset requires +5 and ±15V supplies and can be adjusted for pixel rates up to 250 kHz.

Table 1. Electrical Characteristics (25°C)

	Min	Typ	Max	Units
Video line bias [1]	-4	-5	-6	V
Substrate bias	+4.5V	+5	+5.5	V DC
Clock amplitude [1]	-11	-12	-15	V
Start pulse amplitude [1]	-11	-12	-15	V
Total effective pixel output rate			2.5	MHz
Clock frequency			1.25	MHz
Capacitance of each clock line (@ 5V bias) [2]				
RL0064T		8		pF
RL0128T		23		pF
RL0256T		30		pF
RL0512T		60		pF
Capacitance of each video line (@ 5V bias) [2]				
RL0064T		3		pF
RL0128T		9		pF
RL0256T		12		pF
RL0512T		24		pF
Capacitance of each photodiode (@ 5V bias) [2]		4		pF
End of scan output resistance [2]		5		KΩ
DC power dissipation [3]		1		mW

Notes:

1 Measured with respect to substrate. Substrate is normally run at +5V for compatibility with TTL clock circuits.

2 Calculated typicals—not measured.

3 The AC power is given by $2C_cV_c^2f_s$ where C_c is the capacitance of each clock line, V_c is the clock voltage, and f_s is the scan frequency.

Table 2. Electro-Optical Characteristics (25°C)

	Typ	Max	Units
Center-to-center spacing	50		µm
Aperture width	2.5		mm
Sensitivity [1,3,6]	4.4×10^{-4}		C/J/cm²
Nonuniformity of response [2,6]	5	10	±%
Saturation exposure [3]	50		nJ/cm²
Saturation charge	28		pC
Average dark current [5,6]	4	10	pA
Quantum efficiency [1,3]	75		%
Spectral response peak [3]	750		nm
Spectral response range [3,4]	200-1000		nm

Notes:

1 Peak, typical @ 750 nm, quartz window.

2 Measured at 50% V_{sat} with 2870°K incandescent tungsten lamp filtered with a Fish-Schurman HA-11 heat absorbing filter.

3 Fiber optic faceplate will modify sensitivity as shown in Figure 5.

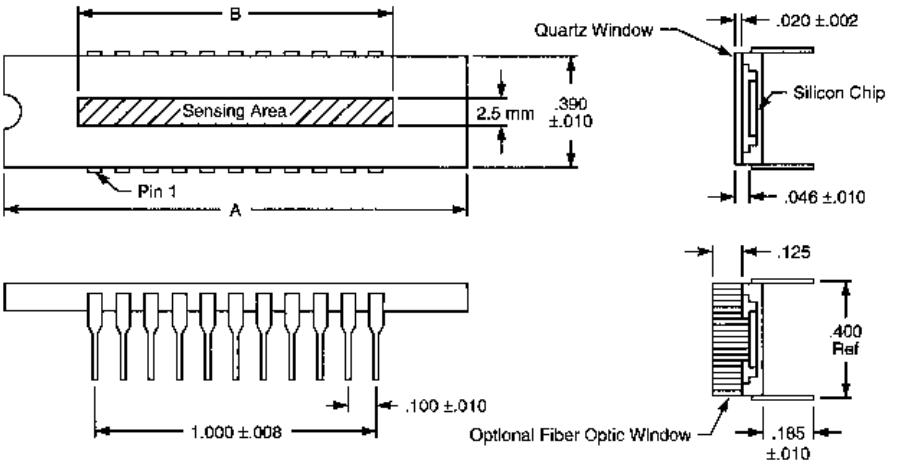
4 From 250-1000 nm sensitivity ≥20% of its peak value.

5 Max dark leakage ≤1.5 x avg dark leakage measured at 40 msec integration @ 25°C.

6 All specifications ignore first two and last two diodes.

Absolute Maximum Ratings

	Min	Max	Units
Voltage applied to any terminal with respect to substrate	0	-20	V
Storage or operating temperature			
Quartz windowed (TAQ)	-78	+85	°C
Fiber optic (TAF)	-40	+85	°C



	A	B
RL0064T	1.070 ±.010	3.2 mm
RL0128T	1.080 ±.011	6.4 mm
RL0256T	1.080 ±.011	12.8 mm
RL0512T	1.600 ±.016	25.6 mm

Figure 11. Package Dimensions. Dimensions are in inches except where millimeters (mm) are indicated.

Ordering Information

Part Number	Evaluation Circuit
Quartz Window	
RL0064TAQ-011	RC1000LNN-020/RC1001LNN-011
RL0128TAQ-011	RC1000LNN-020/RC1001LNN-011
RL0256TAQ-011	RC1000LNN-020/RC1001LNN-011
RL0512TAQ-011	RC1000LNN-020/RC1001LNN-011
Fiber Optic Window	
RL0064TAF-011	RC1000LNN-020/RC1001LNN-011
RL0128TAF-011	RC1000LNN-020/RC1001LNN-011
RL0256TAF-011	RC1000LNN-020/RC1001LNN-011
RL0512TAF-011	RC1000LNN-020/RC1001LNN-011

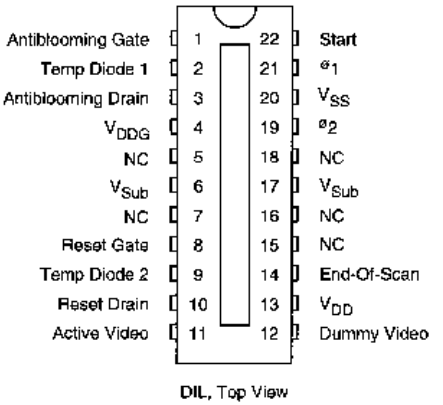
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January 1992

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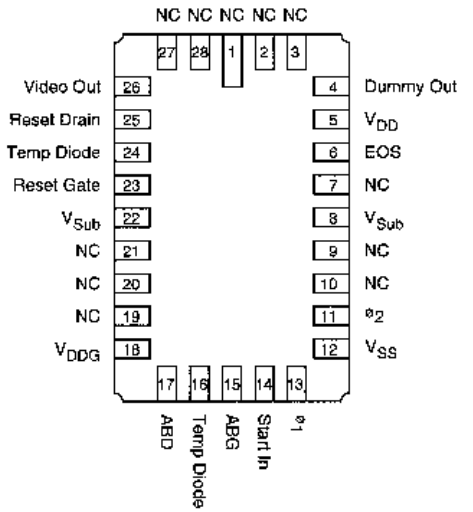
General Description

The EG&G Reticon TB series is a family of monolithic self-scanning linear photodiode arrays optimized for application in spectroscopy. The devices in this series consist of a row of silicon photodiodes, each with an associated junction capacitance on which to integrate photocurrent and a multiplex switch for periodic readout via an integrated shift register scanning circuit. The part number of each device indicates the number of elements in the array (example, 128, 256, and 512).

The TB series devices are mounted in ceramic side-brazed dual-inline packages which mate with standard 22-pin integrated circuit sockets. The 128-element array is also available in a ceramic LCC package. Pinout configurations are shown in Figure 1. Package dimensions are shown in the outline drawings of Figure 9. Standard TB devices are sealed with a ground and polished quartz window. However, an optional fiber optic faceplate version is also available for side-brazed packages. The fiber optic faceplate has 6 µm diameter fibers and a numerical aperture of 1.



DIL, Top View



LCC Package, Bottom View
(128-element array, only)

Figure 1. Pinout Configurations

Key Features

- Simultaneous integration of 128, 256, or 512 photodiode elements with 50 µm center-to-center spacing
- Each sensor element has a 50:1 aspect ratio (50 µm x 2.5 mm)
- Extremely low dark current for longer integration times
- Low power dissipation to facilitate cooling
- Clock-controlled sequential readout at rates up to 10 MHz
- Single-supply operation with HCMOS-compatible inputs
- Single shift register design for simplified clocking requirements
- Differential video output to cancel clock switching transients and fixed pattern noise (FPN)
- Low output capacitance for low noise
- High saturation charge for wide dynamic range
- Antiblooming function for high-contrast images
- Line Reset Mode for simultaneous reset of all photodiodes
- Wide spectral response
- Choice of quartz window or fiber optic faceplate (LCC package has quartz window, only)
- On-chip diodes (two) for temperature monitoring

Sensor Characteristics

The TB series self-scanning photodiode arrays contain 128, 256, or 512 elements (LCC package: 128 elements, only) on 50 µm centers corresponding to a density of 20 diodes/mm and an overall length of 6.4, 12.8, or 25.6 mm. The height of the sensor elements is 2.5 mm giving each element a slit-like geometry with 50:1 aspect ratio suitable for coupling to monochromators or spectrographs. The sensor geometry is shown in Figure 3.

Charge generated by light incident on the p-type surface between two n-regions will divide between the adjacent diodes to produce the response function shown in Figure 3.

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Figure 4 shows the typical output charge as a function of exposure at 750 nm wavelength. Exposure in nJ/cm^2 is calculated by multiplying the light intensity in µW/cm^2 by the integration time in ms. Note that the response is linear with exposure up to a saturation charge of 20 pC at a saturation exposure of 34 nJ/cm^2. The sensitivity is defined as the ratio of saturation charge to saturation exposure and is 5.4 x 10^{-4} C/J/cm^2 (at 750 nm). Typical relative sensitivity as a function of wavelength is shown in Figure 5. Quantum efficiency can be obtained by dividing the sensitivity by the area of a sensor element (12.5 x 10^{-4} cm^2) and multiplying by the energy per photon in eV. Peak quantum efficiency is about 80% at 650 nm. The dark current of a TB series device is typically .5 pA at 25°C and is a strong function of temperature, approximately doubling for every 7°C increase in temperature. The dark signal charge is given by the dark current multiplied by the integration time. See Table 2 for Electro-optical Characteristics.

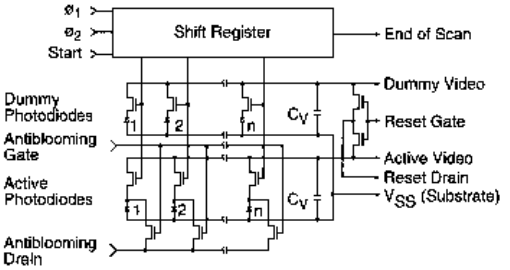


Figure 2. Equivalent Circuit

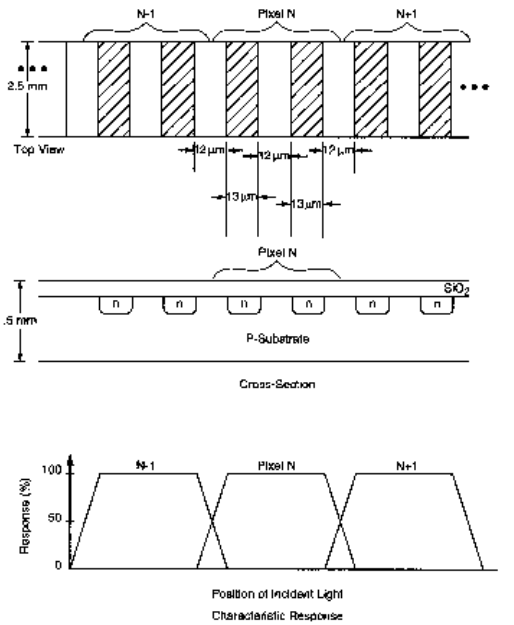


Figure 3. Sensor Geometry and Aperture Response Function

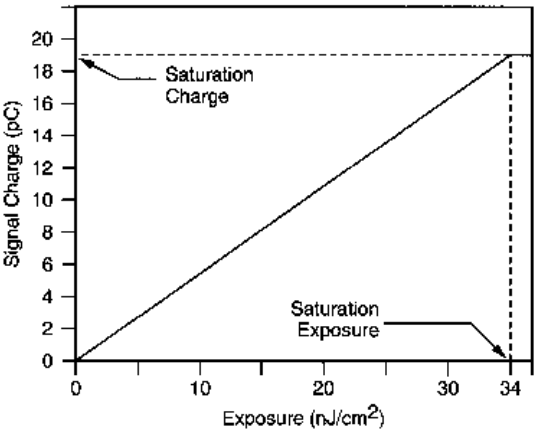


Figure 4. Typical Signal Charge versus Exposure at 750 nm Wavelength

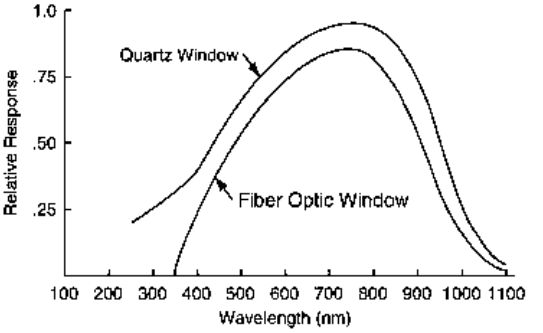


Figure 5. Typical Spectral Response

Scanning Circuit

The simplified equivalent circuit of a TB series photodiode array is shown in Figure 2. Each cell consists of an active photodiode and a dummy photodiode, both with an associated junction capacitance. These diodes are connected through MOS multiplex switches to active video and dummy video lines. The shift register is driven by complementary square wave clocks with periodic start pulses being introduced to initiate each scan. The pixel sampling rate is determined by the clock frequency. The integration time is the interval between start pulses. The output signal obtained from each scan of an N-element array is a train of N charge pulses, each proportional to the light exposure on the corresponding photodiode. In addition to the signal charge, switching transients are capacitively coupled into the active video lines by the multiplex switches. Similar transients are introduced into the dummy video lines and, therefore, can be reduced and a cleaner signal recovered by reading out the video and dummy lines differentially.

Clock and Voltage Requirements

Scanning is achieved by means of an integrated shift register. The shift register is driven by complementary square wave clocks, $ø_1$ and $ø_2$. Table 1 gives rise and fall times and crossover points for these clock waveforms. The clock amplitude should be equal to V_{DD} - V_{SS}. With V_{DD} = 5V and V_{SS} = 0V, the clock inputs will be HCMOS-compatible. Since each photodiode is read out on a negative transition of $ø_2$ (see Figure 6), the frequency of the clock signal should be set equal to the desired video data rate.

The start pulse of similar amplitude to the clocks is required to load the shift register and initiate each readout period (each scan of the array). The start pulse is loaded when $ø_2$ is high; the start signal is pulsed high for a minimum of 10 ns during one and only one $ø_2$ clock high cycle. A timing diagram for the start and clock signals is shown in Figure 6. Caution: $ø_1$ and $ø_2$ clocks need to be continuously applied to the device. The integration period should be controlled by varying the time between start pulses.

For optimum performance and minimum switching noise, it is important that the clocks are exact complements and that their rise and fall times comply with Table 1. A recommended circuit for generating these clocks is shown in Figure 7.

End of Scan

An output pulse useful primarily for test purposes is provided two clock cycles after the last photodiode is sampled by the shift register scanning circuit. The timing of the EOS output is shown in Figure 6. The voltage levels on the EOS output will be determined by the V_{DD} and V_{SS} voltage levels supplied to the photodiode array. When V_{DD} is at +5V and V_{SS} is operated at 0V, the EOS output will be compatible with the HCMOS family of logic devices.

Amplifier Requirements

The recommended amplifier for use with the TB devices is a simple current amplifier. A current amplifier holds the video line at a virtual ground and senses the current pulses flowing

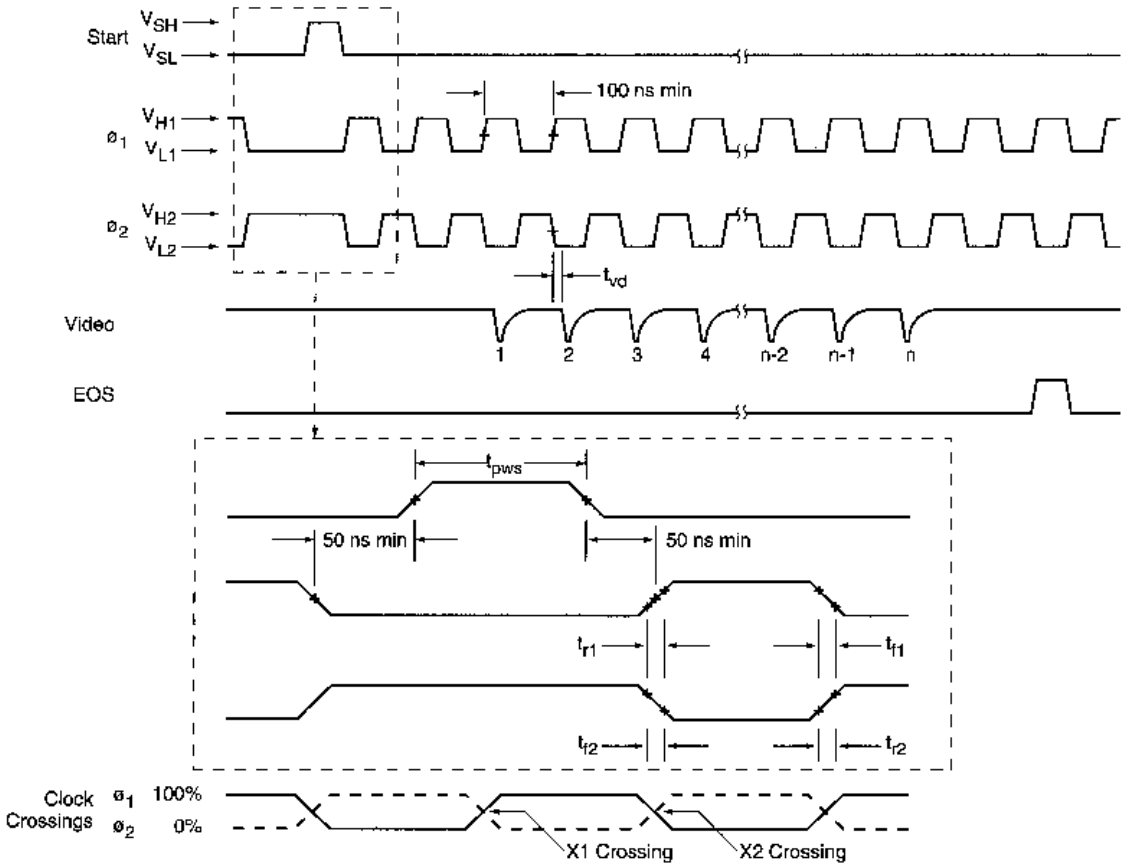


Figure 6. Timing Diagram

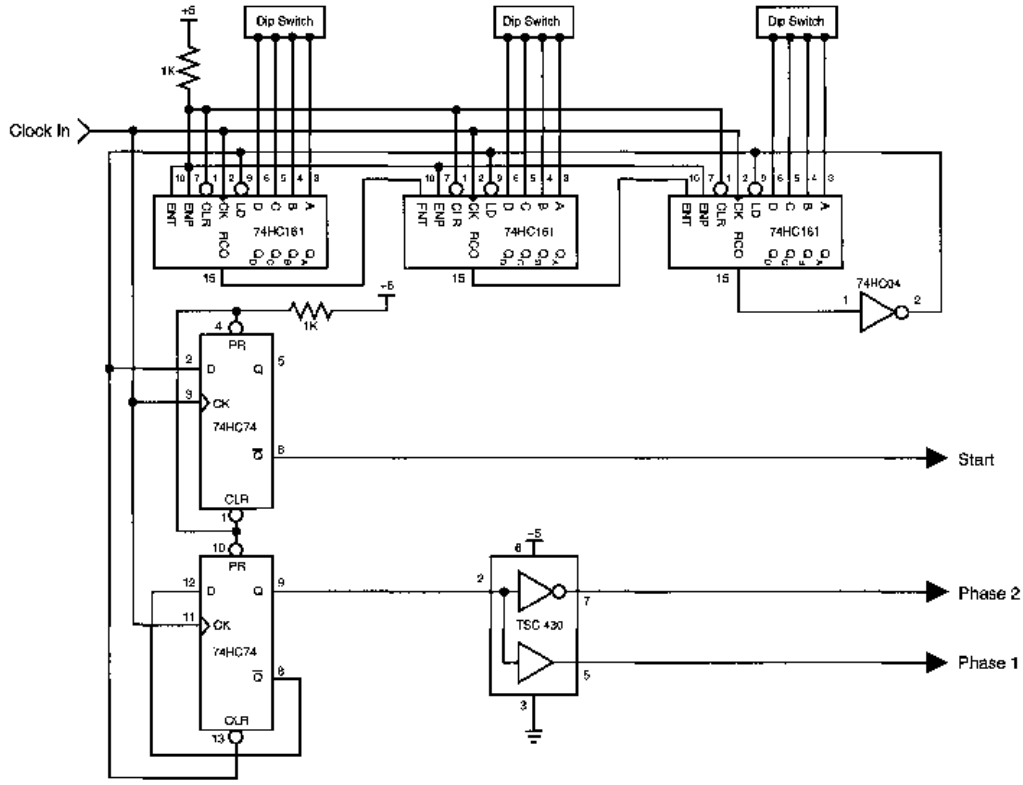


Figure 7. Two-Phase Drive Circuit

into the video line to recharge the diodes through their respective multiplex switches as they are sampled in sequence. These current pulses, which each contain a charge of up to 20 pC at saturation, are converted to a train of voltage pulses corresponding to the light intensity on the various diodes. In this mode of operation, the current amplifier must provide a positive bias voltage to the video line since the photodiode anode (the p-substrate) is biased to 0V (V_{SS}). Figure 8 shows a differential recharge amplifier suitable for use with TB series devices.

Line Reset/Antiblooming Control

Under certain operating conditions, it may be desirable to control integration time independent of the line scan time (time between start pulses). This can be accomplished by the use of the Antiblooming Gate control input. When the Antiblooming Gate is held at V_{DD}, all photodiodes are simultaneously reset to the bias voltage on the antiblooming drain (the same voltage as the video line bias, typically $V_{DD}/2$). Conversely, when the antiblooming gate is held at V_{SS}, the antiblooming transistor is off and the photodiodes can then integrate photocurrent. Thus, when an active high pulse is applied to V_{ABG}, the integration time for diode 'N' then becomes the time between the negative-going transition of the antiblooming gate input to the time in which diode 'N' is read out through the diode multiplex switch.

Under normal operating conditions, TB series devices do not require any blooming control due to their excellent antiblooming characteristics. However, under extremely high contrast conditions, blooming control can be implemented to further enhance this performance. In this mode of operation, a bias voltage (the same voltage as the video line bias, typically $V_{DD}/2$) is required on the antiblooming drain. The antiblooming gate is then biased to 1-3V. By adjusting the bias level on the antiblooming gate, excess charge present on the video line is shunted to the antiblooming drain.

Dark Signal and Noise

There are two components of the dark signal from the TB series. These are due to: (1) spatial variations in the switching transients coupled into the video line through the clocks and internal multiplex switches, and (2) the integrated dark current. A portion of the switching transient effect will be spatially random and a portion will have the periodicity of the clocks. The latter portion can be minimized by matching the clock amplitudes and rise and fall times and by good circuit layout to minimize capacitance between clocks and video lines. The peak-to-peak fixed pattern due to all switching transient effects should be less than 1% of the saturated signal. The dark signal due to dark current is the dark current multiplied by the integration time. It can be arbitrarily reduced by lowering the temperature or by reducing the integration time.

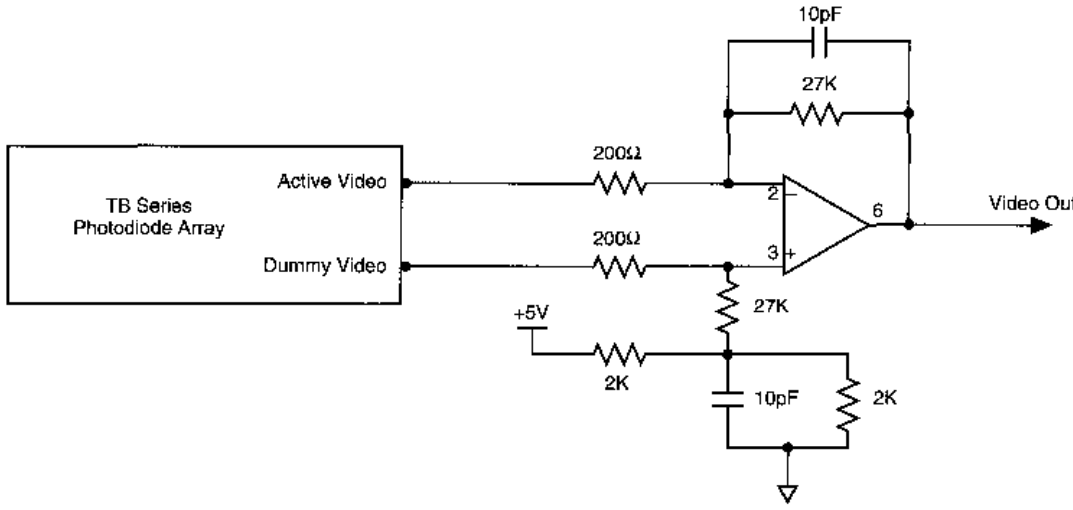


Figure 8. Differential Recharge Mode Video Amplifier

There are three identifiable sources of readout noise: (1) reset noise, (2) shot noise, and (3) amplifier noise. Reset noise is associated with resetting the diode capacitance to a fixed voltage. Its rms value is given by $(kTC)^{1/2}/q$ where k is Boltzmann's constant, T is the absolute temperature, q is the electronic charge and C is the total capacitance of the photodiode (approximately 7 pF), the video line it connects to, and the capacitance of the external circuitry. At room temperature, kTC noise is approximately 1700 electrons rms. It can be reduced somewhat by cooling. The rms value of the dark shot noise is the square root of the number of electrons in the dark signal charge. For example, with a room temperature dark current of .75 pA and 10 ms integration time, the rms dark current shot noise is approximately 210 electrons. Because of the exponential temperature dependence of dark current, shot noise can be reduced dramatically with a moderate amount of cooling. Amplifier noise depends on the amplifier circuit used. In general, the low video output capacitance of the TB series makes it easy to achieve low amplifier noise and values below 2200 electrons are possible.

Temperature Diodes

The TB Series arrays each have 2 on-chip diodes for sensing array temperature. The standard method of use is to force a fixed forward current (normally 10 μA) through the diodes and measure the forward diode voltage drop. For details, please refer to Application Note 127, *How to Use Reticon Temperature Diodes*.

Evaluation Circuit

A complete evaluation circuit for the TB series is available from Reticon (side-brazed packages, only). The RC1030 board provides the user with an easy means of evaluating operation. The RC1030 uses an alternative circuit to that shown in Figure 7.

The RC1030 has a sample-and-held video output with a typical dynamic range of 8,000:1. Provision for cooling the array using a thermal-electric cooler is provided by means of an access hole located directly beneath the array.

The board requires +5 and ±15V supplies and can be adjusted for pixel rates up to 50 kHz.

Table 1. Electrical Characteristics (25°C)
(All voltages measured with respect to V_{Sub})

Signal	Sym		Min	Typ	Max	Units
V_{DD}	V_{DD}		4.5	5	9	V
V_{DD} guard	V_{DDG}			V_{DD}		V
V_{SS}	V_{SS}			0		V
Antiblooming drain	V_{ABD}			V_{SS}		V
Start	V_{SH}	High	V_{DD} - .1		V_{DD}	V
	V_{SL}	Low	V_{SS}		V_{SS} + .4	V
Clock $ø_1$, $ø_2$	V_{H1}, V_{H2}	High	V_{DD} - .1		V_{DD}	V
	V_{L1}, V_{L2}	Low	V_{SS}		V_{SS} + .4	V
Reset gate	V_{HRG}	High	V_{DD} - .1		V_{DD}	V
	V_{LRG}	Low	V_{SS}		V_{SS}+ .4	V
Antiblooming gate	V_{HABG}	High	V_{DD} - .1		V_{DD}	V
	V_{LABG}	Low	V_{SS}		V_{SS}+ .4	V
Video bias	V_V		2	$V_{DD}/2$	V_{DD} - 2	V
Reset drain	V_{RD}		2	$V_{DD}/2$	V_{DD} - 2	V
Clock rate			.001		10	MHz
Start rise time	t_{rs}			10	50	ns
Start fall time	t_{fs}			10	50	ns
Start pulse width	t_{pws}		10			ns
$ø_1$ rise time	t_{r1}			10	20	ns
$ø_1$ fall time	t_{f1}			10	20	ns
$ø_2$ rise time	t_{r2}			10	20	ns
$ø_2$ fall time	t_{f2}			10	20	ns
Video delay time	t_{VD}			20		ns
Clock crossings	X_1		0		50	%
	X_2		0		50	%
Capacitance $ø_1$, $ø_2$ at 5V bias [1]	C_c					
RL0128TB				33		pF
RL0256TB				38		pF
RL0512TB				44		pF
Capacitance, each video at 2.5V bias	C_v					
RL0128TB				6		pF
RL0256TB				9		pF
RL0512TB				16		pF

Note:
1 Calculated typicals - not measured

Table 2. Electro-Optical Characteristics (25°C)

Conditions:
All voltage levels set to typical values shown in Table 1
Light source is 2870°K tungsten filtered with a 750 nm bandpass filter
Video data rate = 250 kHz

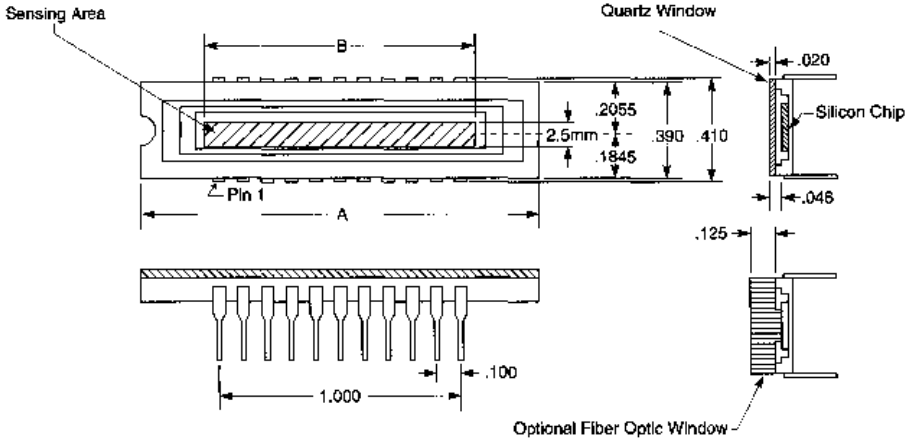
Characteristics	Typ	Max	Units
Center-to-center spacing	50		µm
Aperture width	2.5		mm
Sensitivity (E_{SAT})[1,2,3]	5.4×10^{-4}		$C/J/cm^2$
Nonuniformity of response			
RL0128TB[2,4,5]	5	10	±%
RL0256TB[2,4,5]	5	10	±%
RL0512TB[2,4,5]	5	10	±%
Saturation exposure (E_{SAT})[1,2,3]	34		nJ/cm^2
Saturation charge (Q_{SAT})	19		pC
Dynamic range ($Q_{SAT}/Q_{Noise\ (rms)}$)	54,000		
Average dark current[6]	.5	.75	pA
Spectral response peak	750		nm
Spectral response range[5,7]	200-1000		nm

Notes:

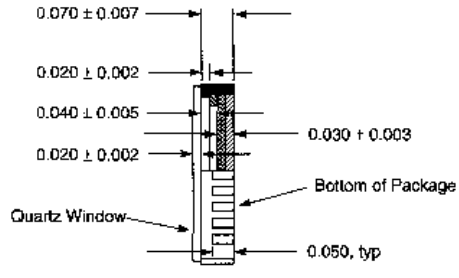
1 Measured at 2.5V video line bias
2 Value specified at 750 nm
3 Fiber optic faceplate will modify sensitivity as shown in Figure 5
4 +% PRNU is defined as $[(V_{max} - V_{avg})/V_{avg}] \times 100\%$ and -% PRNU is defined as $(V_{avg} - V_{min})/V_{avg}] \times 100\%$, where
V_{max} is the output of the pixel closest to saturation level,
V_{min} is the output of the pixel closest to dark level,
V_{avg} is the numerical average of all the array pixels.
The first and last pixels are not counted in this measurement.
5 Measured at an exposure level of $E_{SAT}/2$
6 Maximum dark current ≤1.5 x average dark current
7 From 250 - 1000 nm, sensitivity is typically at least 20% of its peak value.

Absolute Maximum Ratings

	Min	Max	Units
Voltage applied to any terminal with respect to common	0	+10	V
Storage of operating temperature			
Quartz window	-78	+85	°C
Fiber optic	-40	+85	°C

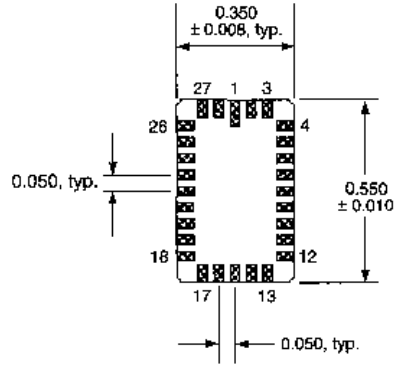


Device	A	B
RL0128TB	1.080	.2520 (6.4 mm)
RL0256TB	1.080	.5039 (12.8 mm)
RL0512TB	1.600	1.008 (25.6 mm)



LCC Package, Side View

Note: Sensing aperture in LCC is centered with respect to cavity edges



LCC Package, Bottom View

Figure 9. Package Dimensions (all dimensions are typical and in inches unless otherwise specified)

Ordering Information

Part Number	Evaluation Circuit
Quartz Window	
RL0128TBQ-011	RC1030LNN-020
RL0256TBQ-011	RC1030LNN-020
RL0512TBQ-011	RC1030LNN-020
Fiber Optic Window	
RL0128TBF-011	RC1030LNN-020
RL0256TBF-011	RC1030LNN-020
RL0512TBF-011	RC1030LNN-020
Quartz Window, LCC Package	
RL0128TBQ-111	none

055-0263
March 1992

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Area Arrays

Photodiodes

RA0100A/RA0128N
RA0256B
RA1441A
RA1662N
RA2568N
RA3812P
RA6464N

CCDs

RA0512J
RA1024J
RA1200J
RA2000J
RA2048J

Description

The Reticon RA0100A and RA0128N are two-dimensional self-scanned optical sensor arrays with optimized characteristics. The discrete photodiodes are geometrically arranged in 100 x 100 and 128 x 128 matrices. In contrast to comparable CCD devices, discrete photodiode sensors require no surface electrodes, so there is no interference pattern or light loss and the full inherent sensitivity of a silicon photodiode is obtainable.

The scanning method permits pixel rates up to 10 MHz. Each line of pixel information is parallel-loaded into two high-speed bucket-brigade (BBD) analog shift registers and sequentially shifted out. The outputs of the registers are then combined externally to reconstruct the line information. All of the 100 or 128 lines may be sequentially accessed to give a single frame, or alternate odd or even lines may be selected to produce one-half of the lines per field in an odd and even pattern. The integration time is normally one frame period, giving maximum sensitivity.

The primary applications of these devices are in industrial and scientific instrumentation systems, such as:

- Noncontact optical measurements
- Pattern recognition
- Inspection and robotic systems
- Industrial process monitoring and control
- Laser profiling

Key Features

- 10,000 or 16,384 light-sensitive elements in a high-resolution 100 x 100 or 128 x 128 matrix, respectively
- 60 µm center-to-center element spacing in both X and Y directions
- Frame storage. Each diode integrates photocurrent for the entire frame.
- Self-scanned in both X and Y directions by high-speed on-chip circuitry, to provide either single frame or interlaced video output
- Variable data rates up to 10 MHz
- Low power dissipation, small size, and solid state reliability
- 24-pin dual-inline package with scratch resistant quartz window or optional fiber optic faceplate

Functional Description

The RA0100A and RA0128N are each packaged in a 24-pin ceramic side-brazed, dual-inline package with a ground and polished window covering the active area. Figure 1 is a pinout configuration of the devices and Figure 11 shows the package dimensions.

The devices are fabricated using a double-poly NMOS process. Each device consists of several functional elements, shown in Figure 2, to control the operation of the device. These elements have been indicated on Figure 2 by dotted lines. They are:

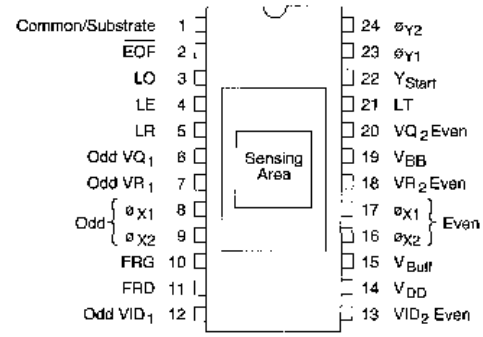


Figure 1. Pinout Configuration

1. Photodiode Array

The first element consists of a 100 x 100 or 128 x 128 diode array matrix, schematically indicated by the columns and rows of individual photodiodes. The diodes in each column are connected one at a time through multiplex switches to a video line, which is common to all diodes in that column. Parallel connection of the multiplex switches simultaneously selects one diode from each column. When a diode is selected by the multiplex switch, the reverse-bias of the diode is reset to a value of V_{GM}-V_{TM}, where V_{GM} (14.5V typical) and V_{TM} (2V typical) are the clock high voltage and threshold voltage of the multiplex switch, respectively. The signal charge removed from the selected diode will be transferred into an analog shift register through the column video line for readout. After the multiplex switch is turned off, the diode starts to integrate photon-generated charge and its reverse-bias decays. The total integration time of each diode is the time between two consecutive readouts of the same diode. Thus, the device operates in a frame storage mode.

2. Digital Dynamic Shift Register (Y Register)

The second element consists of a two phase (2ø) dynamic shift register which controls the multiplex switches. The register turns on each row of diodes in sequence and transfers the corresponding signal charge into the appropriate BBD analog shift register through each column video line. Thus, a complete row of information is loaded at one time. The dynamic shift register is driven by a two-phase clock denoted by $ø_{Y1}$ and $ø_{Y2}$ in Figure 2. It can be self-loaded for sequencing or controlled by an external start pulse Y_{Start}. These functions are performed by a "NOR" circuit. Tied to each output of the shift register (except for the 100th or 128th position) are inputs to a NOR gate which provides for the self-loading feature. When there is an output from any of the 99 (or 127) output positions, the NOR gate keeps the shift register from loading. Once the bit occupies the last position, the NOR gate's output goes high and the shift register loads with the rising edge of $ø_{Y1}$. Note that Y_{Start} is connected to the NOR gate. It can be used to inhibit the register from loading by pulling Y_{Start} to V_{DD}. Odd lines are accessed while $ø_{Y1}$ clock is high, even while $ø_{Y2}$ is high.

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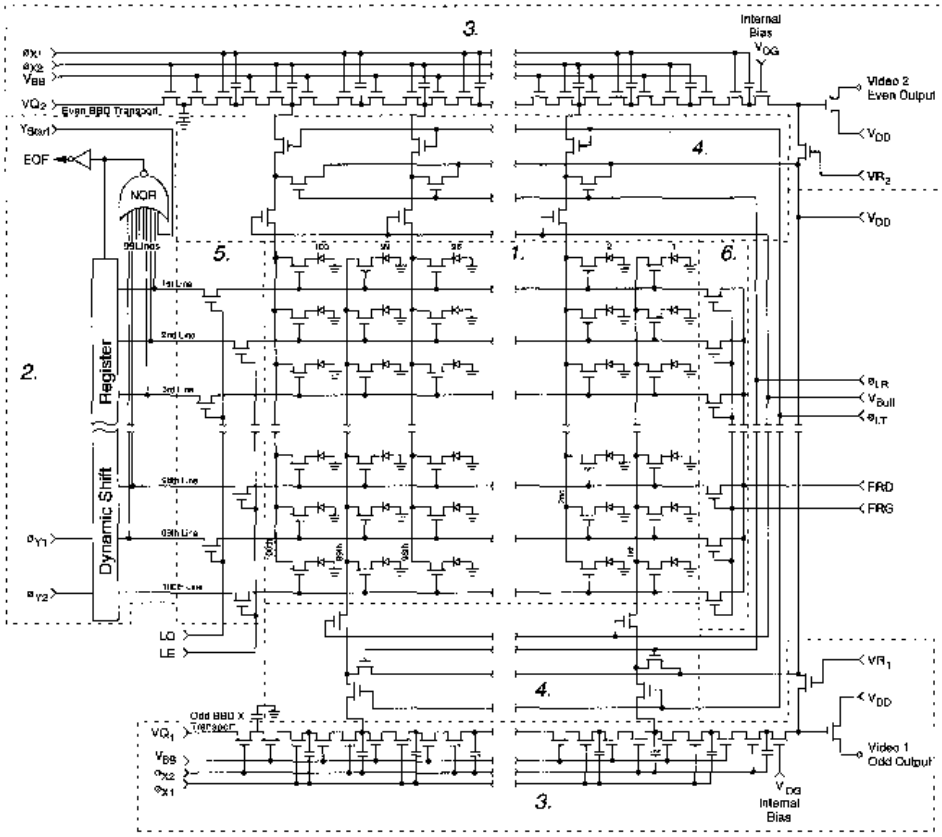


Figure 2. Schematic Diagram RA0100A (the RA0128N has a Similar Format with the Exception of 128 Lines and 128 Pixels Per Line)

The NOR gate output is connected to an external pin, EOF, through an open-drain inverter. This output is normally tied to V_{DD} through an 8.6KΩ resistor; therefore, when there is a bit in any row except the last, or if Y_{Start} is active, EOF will remain high. It goes immediately low on the rising edge of ϕ_{Y2} if Y_{Start} is low, and none of the rows 1-99 (or 1-127) are active.

3. Bucket-Brigade Analog Shift Register

Two tetrode-gate bucket-brigade shift registers, each with a gated charge-integrator output, form the third element. These are the odd and even transport registers which accept pixel information in parallel from their respective odd and even video diode columns and shift the pixel information sequentially to the output amplifier. Each shift register is driven by a two-phase clock, denoted by ϕ_{X1}, and ϕ_{X2} in Figure 2. A "fat zero" input is provided to improve the transfer efficiency of the register. The outputs from both shift registers are multiplexed off-chip to obtain one line of combined video information (refer to the RC0502A Evaluation Circuit).

As shown in Figure 2, there are several other terminals associated with the two BBD registers. V_{BB} is the tetrode-gate bias which is usually set at a DC voltage about 1V below the ϕ_{X1} and ϕ_{X2} high level. V_{Q1} and V_{Q2} are the biases for the "fat zero" input. These inputs control the bias level in the dark. Nominally, these terminals are set to approximately 10V. However, when the odd and even videos are summed together, either input bias voltage may be used to adjust the corresponding dark-level output to remove the odd and even pattern. Figure 3 shows the relationship between output dark signal level and V_{Q1}, V_{Q2} bias voltage. The shaded area represents the optimum bias range.

VR_1 and VR_2 are the reset clocks for the output gated-charge amplifiers. These terminals, shown in Figure 2, provide reset voltages for the gated-charge amplifiers at the outputs of both bucket brigades. On the even side, the signal appears at the gate of the output source follower when ϕ_{X1} drops to a low potential. While ϕ_{X1} is high before the next sample appears, this node is cleared by charging it to the reset voltage, V_{DD}. Thus, reset is accomplished when this terminal is clocked synchronously with ϕ_{X1}. The complementary situation applies to the odd output, with signal appearing while ϕ_{X2} is low and reset while ϕ_{X2} is high. The extra half-stage in the even side allows the alternating sequence desired. Normally, the synchronous relationship is obtained by direct connection of ϕ_{X1} to VR_2 and direct connection of ϕ_{X2} to VR_1.

VID_1 and VID_2 are the respective odd and even video output terminals. The video output is that of a source follower. Normally, the output of each source follower is connected to 2KΩ, which is referenced to ground. This configuration provides the proper bias current for the source follower. Figure

4 shows the output voltage across such a load resistor, showing the relationship of video pixel information relative to the superimposed reset clock amplitude. Figure 5 shows output impedance of the source follower as a function of the bias current. This graph can be used to design an interface circuit with suitable DC bias translation (e.g. an emitter-coupled transistor with the base biased near the video output line potential).

4. Line Transfer (LT), Line Reset (LR), and Buffer Gate (V_{Buff})

The fourth element consists of a video line reset switch, LR; a transfer switch, LT; and a buffer gate, V_{Buff}. The reset switch, LR, provides a reference bias for all video lines while all the sensor diodes are integrating. All charges collected on stray capacitances along the video lines and all excess signal charges leaked from the sensor diodes are drained into the sink voltage, V_{DD}, through the LR gate. Therefore, LR functions as an antiblooming and anticrosstalk gate.

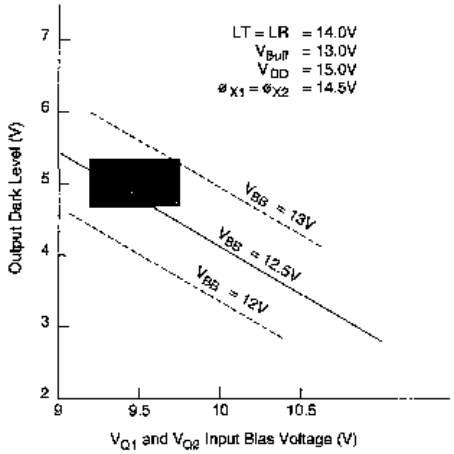


Figure 3. Operation Range of V_{Q1} and V_{Q2} Bias

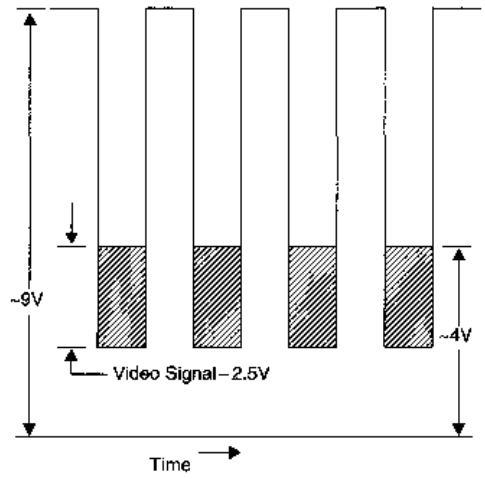


Figure 4. Typical Video Signal Seen Across 2KΩ Load Resistor

Prior to the moment when the dynamic register is to select another row of diodes, the LR gate is turned off and the transfer gate turned on. This makes conditions ready for the signal charge from the next row to be transferred into the BBD registers.

The voltage applied to the LR switch should be equal to or lower than that of LT. This will prevent possible loss of signal charge through LR as a result of threshold voltage mismatch between LR and LT transistors. The effect of different gate potentials on LR and LT results in adding a fixed amount of charge, Q_f, to the video signal, where $Q_f = (\Delta V_G + \Delta V_T)\, C_V$. These quantities ΔV_G and ΔV_T are the gate potential and threshold voltage differences of the LR and LT gates, respectively, and C_V is the capacitance of the video line.

To minimize Q_f a buffer gate V_{Buff} is introduced in front of the LR and LT switches. This buffer gate is biased at a DC potential below the LR and LT "high" potential. The function of this buffer gate is to isolate the video line capacitance C_V from the effect of ΔV_G and ΔV_T. With the introduction of this buffer gate, Q_f becomes $(\Delta V_G + \Delta V_T)\, C_j$, where C_j is the junction capacitance of the n+ diffusion between LR and LT. The capacitance C_j is much smaller than C_V and results in great reduction of Q_f. Normally LR is clocked synchronously

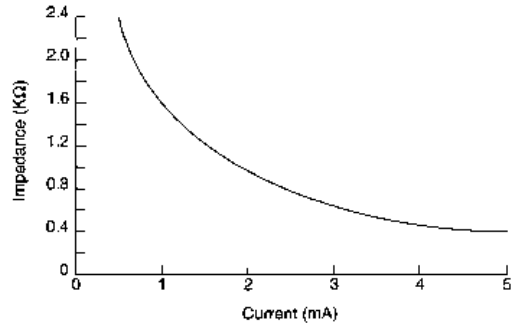
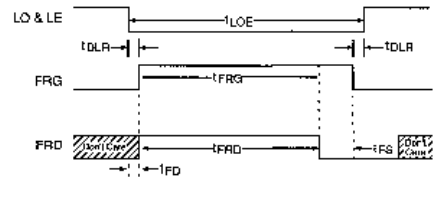


Figure 5. Typical Video Output Impedance Versus Bias Current



	Min	Typ	Max	Remark
t_{DLR}	100 ns			
t_{LOE}				To be consistant with t_{FRG}
t_{FRG}	1.5 ms		2.6 ms	
t_{FRD}	1.5 ms			
t_{FS}	2.50 µs			
t_{FD}	0.1 µs			

Note: Clock rise and fall times are not critical. However it is recommended not to exceed 0.5 µs. While frame reset is active, the reset takes place by performing at least 3 line scans using the BBD registers.

Figure 6. Timing Sequence for Frame Reset

with ϕ_{X1}. However, to avoid crosstalk and to permit adjustment for optimum blooming control, a separate driver is used for LR.

5. Field Select Switches (LO and LE)

The fifth functional element is the field select switches, LO and LE. The LO input terminal controls the gates that switch all the odd-numbered outputs from the Y shift register, and the LE terminal controls the gates that switch the even-numbered outputs. In turn, these Y register outputs control row selection. When the LO line is held at V_{DD}, the odd rows of diodes may be selected by the Y shift register. When the LE line is held at V_{DD}, even rows of diodes may be selected. The selected diodes are connected to the column video lines, which in turn are connected to transport bucket brigades through buffer transistors and the line transfer switches. Typically, the LO or LE, when selected, is switched from a low of 0.4V to a high of V_{DD}. For sequential scan of all lines, both LE and LO are continuously held at V_{DD}.

6. Frame Reset Gate (FRG) and Frame Reset Drain (FRD)

The sixth element consists of the frame reset gate, FRG, and frame reset drain, FRD. This switch provides access to the multiplex switches of all diodes in the matrix and allows the entire frame to be reset simultaneously. Since the diodes in each line are automatically reset when the line is accessed, the frame reset control is not normally used and is held low. However, when a particular exposure is desired, this control may be used to clear the diodes to start a fresh integration cycle by setting the FRG terminal to V_{DD}. When this mode is used, a shutter or pulsed-light input is required because the diodes are sequentially accessed and will thus differ in exposure time if light input is continued during the read-out sequence. With FRG and FRD active, 3 line scans are done to fully recharge both the pixels and video lines through the BBD registers. Depending on the timing or lighting, more line scans may be needed. LR could be used, but a line scan with the BBD registers is then needed to avoid excessive fixed-pattern noise (FPN).

The minimum timing requirements for the frame operation are shown in Figure 6. The longest of the control pulses are LE and LO which are pulsed off during this operation. They should be held negative 200 nanoseconds wider than the frame reset gate, with pulse width overlap as shown in the figure. The FRD can be continuously active, but within and before the trailing edge of FRG, FRD must be pulled to ground to allow the vertical shift register's multiplexing line to discharge. This operation ensures turn-off of the multiplexing switch. Except for FRD, all the clock voltages are set with the low swing at 0.0 +0.25/-0V and at V_{DD} +0/-1V on the high swing. FRD's clock is the same low as called out on the other clocks, but the high end is set to V_{DD} -3 ±0.5V.

Device Operation

Figure 7 shows the timing diagram for the devices in the noninterlaced and continuous mode of operation. It requires two sets of complementary clocks, namely ϕ_{Y1} and ϕ_{Y2} to drive the dynamic shift register, and ϕ_{X1} and ϕ_{X2} to drive the two BBD registers. It also requires an LT clock to control charge transfer from the column video line into the BBD registers. The line reset clock, LR, is the blooming control and has the same timing as ϕ_{X1}. The reset gates, VR_1 and VR_2, are to control the output charge integrators, and are directly tied to ϕ_{X2} and ϕ_{X1}, respectively. The timing relations and rise and fall times of the various clocks are summarized in Table 1.

Before a new row of diodes is selected by the Y shift register, which occurs when ϕ_{Y1} and ϕ_{Y2} change states, the line reset LR should be turned off to prevent signal charge being drained into V_{DD}. The requirement of a certain t_{YD} delay, as shown in Figure 7, warrants this condition. A minimum pulse width of LT is also required to accommodate complete charge transfer from the video line into the BBD register. During the time when the signal charge is being transferred into the BBD register, the clock driving the register must stop at high potential on the buckets receiving charge from the video line. This will cause a deep potential well for the signal charge to flow into. The buckets receiving charge for both the odd and

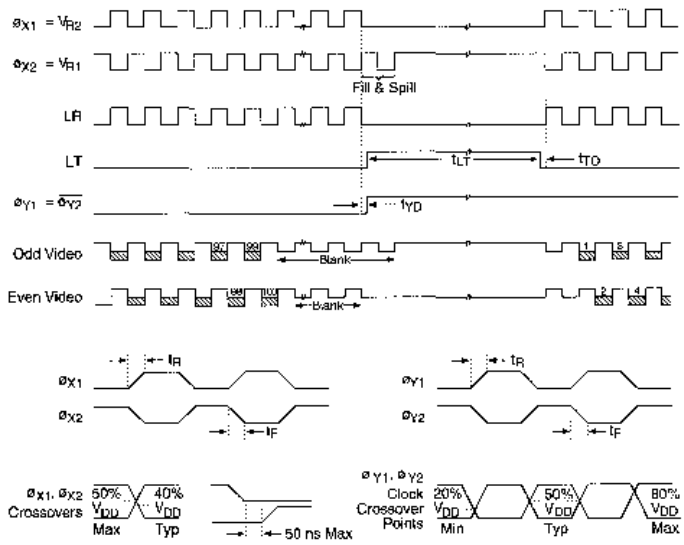


Figure 7. Timing Diagram for RA0100A/RA0128N Noninterlaced Continuous Operation

even transport registers are driven by ϕ_{X2}, and the charge transfer takes place simultaneously for both registers during the time ϕ_{X2} is held high. Note that there is an extra clock of ϕ_{X2} within the LT pulse. The function of this extra clock is to dump the "fat zero" charge of the BBD register into the video line, where it will combine with the signal charge and then spill back together into the BBD register. This "fill and spill" action significantly improves the transfer efficiency of the signal charge.

The LT clock is then shut off before the BBD register shifts the signal charge to the output amplifiers. On the readout, the odd BBD register produces the first pixel. It reads out on the second low-going ϕ_{X2} clock after the transfer period. The second pixel is produced by the even BBD register. Since this even pixel must transfer through an extra half-stage which is controlled by ϕ_{X1}, it is produced when ϕ_{X1} goes low. This provides an easily multiplexed signal by means of a simple external adder-amplifier.

Specifications

Table 1 summarizes the clock timing of Figure 7. Table 2 lists the mechanical specifications of the array. Table 3 and Table 4 are the operating biases and clock amplitudes in accordance with the timing diagram of Figure 7. The capacitances are listed in Table 5. With the exception of supply inputs, such as V_{DD}, the input terminal impedance is essentially capacitive.

Optical Performance

Table 6 lists the optical characteristics and Table 7 summarizes the array output characteristics. The circuit used to obtain the typical performance characteristics is essentially identical to the evaluation circuit offered by Reticon under the designation RC0502A. However, the video processing circuit has not been used. Instead, all measurements have been taken across a 2KΩ load to ground. The optical source for the performance data is a 2870°K tungsten lamp with a Fish-Schurman HA-11 filter. Illumination levels are measured using a detector with a flat response from 370 to 1040 nm.

The spectral response is the standard silicon photodiode response shown in Figure 8. In contrast with CCD detector arrays, no semi-transparent electrode covers the sensors, hence, no interference patterns appear in the pass band and no additional attenuation occurs at short wavelengths.

The transfer function, Figure 9, shows a linear optical-to-electrical relationship with dynamic range exceeding 100:1. This linear relationship depends on application of the proper electrode potentials, especially those for V_{Buff} and the line reset pulse level, LR. Improper potentials can cause substantial nonlinearity.

Antiblooming

Blooming is defined as excess charge integrated on the column video line during a sample period as a result of excess exposure. Blooming is generally less severe in the RA0100A and RA0128N type of structure as compared to typical CCD structures because the sensor elements are separate and distinct p-n junction photodiodes. However, since there are common video lines for each column of diodes, a vertical-blooming effect is observed when some excess charge is collected.

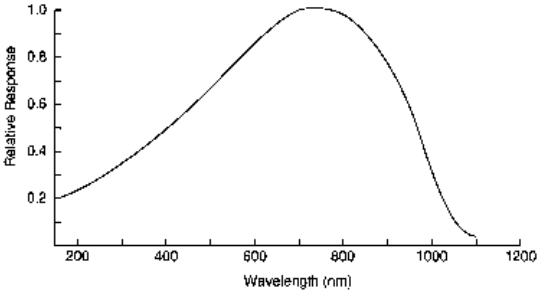


Figure 8. Spectral Response

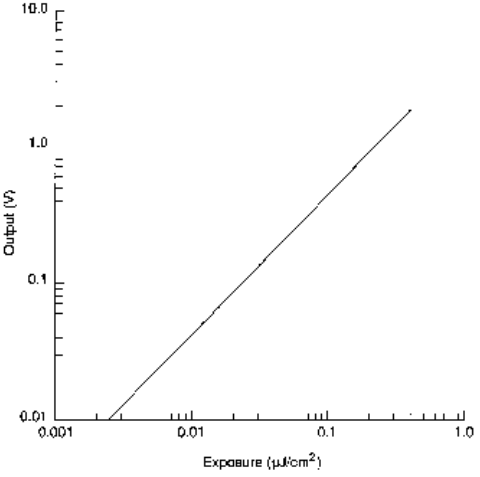


Figure 9. Typical Output Versus Exposure (2870°K Tungsten Lamp with HA-11 Filter)

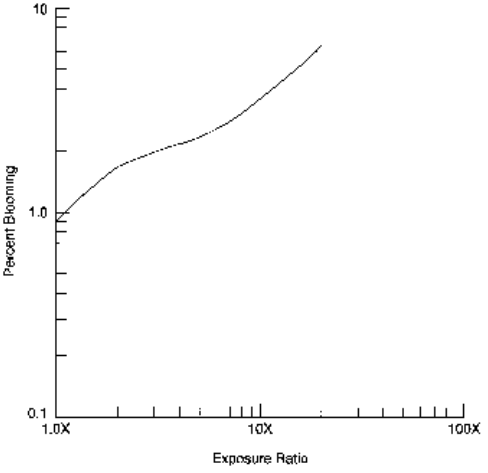


Figure 10. Blooming Ratio

Figure 10 is a curve of this ratio, i.e., points on the horizontal axis represent multiples of saturation exposure and points on the vertical axis represent the output of a nonexposed diode located 15 diodes away from the exposure center sharing the same column video line. The output is normalized to the output voltage of a saturated diode and plotted in percent of the saturation voltage. The exposed area is circular with a diameter of approximately 10 diodes.

Evaluation Circuit Board, RC0502A

The RC0502A evaluation circuit board is available from Reticon. It contains all required drive and amplifier circuitry and is recommended for first-time array evaluation. The circuit board measures approximately 4.5 x 6.5 inches in size and is terminated by a standard dual 22-pin printed circuit board edge connector.

Table 1. Clock and Control Line Timing

Parameters	Sym	Min	Typ	Max	Units
Continuous	t_{LT}	2.5		4	µs
operation	t_{TO}	0	30		ns
	t_{YD}	0	30		ns
$ø_{X1}$, $ø_{X2}$ rise time	t_R	20	60		ns
$ø_{X1}$, $ø_{X2}$ fall time	t_F	20	60		ns
$ø_{Y1}$, $ø_{Y2}$ rise time	t_R	20	60		ns
$ø_{Y1}$, $ø_{Y2}$ fall time	t_F	20	60		ns
Clock crossing $ø_{X1}$, $ø_{X2}$		0*	40	50	% V_{DD}
Clock crossing $ø_{Y1}$, $ø_{Y2}$		20	50	80	% V_{DD}

* Note: Clocks may be nonoverlapping with a maximum of 50 nanoseconds dead time between rising and falling edges.

Table 2. Array Mechanical Specifications

	RA0100A	RA0128N	Units
Number of diodes	10000	16384	
Diode X, Y center-to-center spacing	60/2.36	60/2.36	µm/mils
Diode sensing area	2562	2562	$µm^2$
Package size (24-pin DIP)	.6 x 1.2	.6 x 1.2	inch

Table 3. DC Voltage Requirements

Parameters	Sym	Min	Typ	Max	Units
Supply voltage	V_{DD}	12	15	16	V DC
Quiescent current	I_{DD}	6	8	10	mA
Transport bias	V_{BB}	V_{DD}-2V	V_{DD}-2.0V	V_{DD}-1V	V DC
Isolation gate	V_{Buff}	V_{DD}-2V	V_{DD}-1.5V	V_{DD}	V DC
BBD input	V_{O1},V_{O2}	9.2V	9.5V	10.5	

Note: All voltages are measured with respect to common (ground/substrate)

Table 4. Clock and Control Voltage Requirements

Parameters	Conditions	Sym	Min	Typ	Max	Units
X-Clock	High state	$ø_{X1}$,$ø_{X2}$	V_{DD}-1	V_{DD}-.5	V_{DD}	V DC
	Low state		-.4	.25	.5	V DC
	Capacitance			120		pF
Y-Clock	High state	$ø_{Y1}$, $ø_{Y2}$	V_{DD}-1	V_{DD}-.5	V_{DD}	V DC
	Low state		-.4	.25	.5	V DC
	Capacitance			25		pF
End-of-frame	High state	E_{OF}			V_{DD}	V DC
opendrain	Low state (sync current)				1.5	mA
	Capacitance			5		pF
Line transfer	High state	$ø_{LT}$	V_{DD}-1	V_{DD}-.5	V_{DD}	V DC
	Low state		-.4	.25	.5	V DC
	Capacitance			27		pF
Line reset	High state	$ø_{LR}$	V_{DD}-1	V_{DD}-.5	V_{DD}	V DC
	Low state		-.4	.25	.5	V DC
	Capacitance			27		pF
Video reset	High state	$ø_{VR1}$, $ø_{VR2}$	V_{BB}+1	V_{DD}-.5	V_{DD}	V DC
	Low state		-.4	.25	.5	V DC
	Capacitance			5		pF
Y-Start	High state					
	Low state					
	Capacitance			4		pF

Table 5. Typical Terminal Capacitance with 10V Bias

Pin	Sym	RA0100A	RA0128N	Units
2	EOF	5	5	pF
3	LO	20	22	pF
4	LE	20	22	pF
5	LR	22	27	pF
7	VR_1	5	5	pF
8	$ø_{X1}$	55	60	pF
9	$ø_{X2}$	55	60	pF
10	FR	14	15	pF
12	VID_1	5	5	pF
13	VID_2	5	5	pF
16	$ø_{X2}$	55	60	pF
17	$ø_{X1}$	55	60	pF
18	VR_2	5	5	pF
21	LT	22	27	pF
22	Y_{Start}	4	4	pF
23	$ø_{Y1}$	20	25	pF
24	$ø_{Y2}$	20	25	pF

Table 6. Optical Characteristics

Parameters	Conditions	Sym	Min	Typ	Max	Units
Responsitivity				13.5		$V/\mu J/cm^2$
Saturation exposure [1,2]		E_{SAT}		.155		$\mu J/cm^2$
Noise equivalent exposure	Peak-to-peak	E_{NE}		.0015		$\mu J/cm^2$
Photoresponse nonuniformity [1,2,3]					±10	% V_{SAT}

Notes:
1. Measured with typical clock and voltage requirements
2. Measured using 2870°K light source with HA-11 filter at 20 ms frame period
3. Ignoring first and last columns/first and last lines

Table 7. Output Characteristics

Parameters	Sym	Min	Typ	Max	Units
Impedance	Z_O		2		KΩ
Saturation voltage [1, 2]	V_{SAT}		2.5		V
Pixel rate	F_{SAMP}	0.2		10	MHz
Baseline reference [1, 4]		6		8	V
Fixed pattern noise [1, 4, 5]				20	mV
Average leakage [1, 3]			20	80	mV

Notes:
1. Measured with typical clock and voltage requirements
2. Measured using 2870°K light source with HA-11 filter at 20 ms frame period
3. Measured at 25°C, 40 ms frame period
4. Measured at 20 ms frame period
5. Ignoring first and last columns/first and last lines

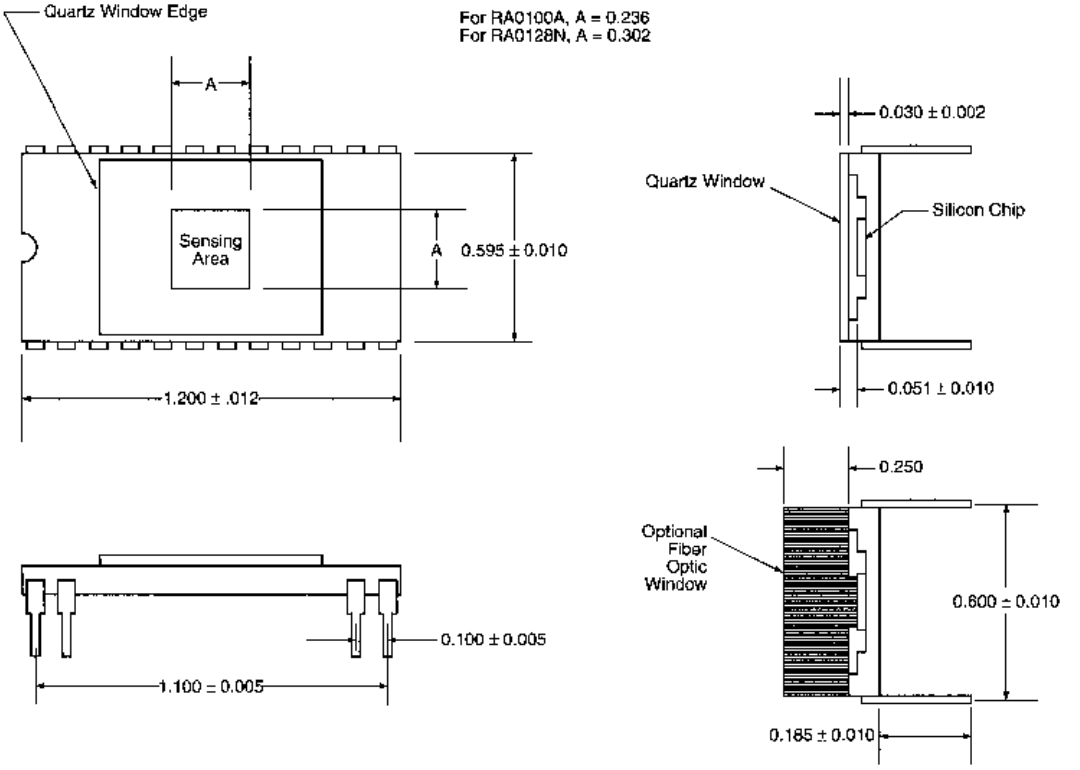


Figure 11. Package Dimensions. Dimensions are in inches except where millimeters (mm) are indicated.

Ordering Information

Array	Ordering Number	Evaluation Circuit
RA0100A (quartz) (0 defects)	RA0100AAQ-011	RC0502ANA-011
RA0100A (quartz) (1-9 defects)	RA0100AAQ-020	RC0502ANA-011
RA0100A (fiber optic) (0 defects)	RA0100AAF-011	RC0502ANA-011
RA0100A (fiber optic) (1-9 defects)	RA0100AAF-020	RC0502ANA-011
RA0128N (quartz) (0 defects)	RA0128NAQ-011	RC0502ANA-020
RA0128N (quartz) (1-9 defects)	RA0128NAQ-020	RC0502ANA-020
RA0128N-011(fiber optic) (0 defects)	RA0128NAF-011	RC0502ANA-020
RA0128N-020 (fiber optic) (1-9 defects)	RA0128NAF-020	RC0502ANA-020

Note: A defect is defined as any diode out of specification.

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Introduction

The EG&G Reticon RA0256B is a two-dimensional self-scanned optical sensor array with perfected characteristics. 65,536 discrete photodiodes are geometrically arranged into 256 x 256 matrix. In contrast to comparable CCD devices, the discrete photodiode sensors require no surface electrode so there is no interference pattern or light loss and the full inherent sensitivity is obtainable.

The scanning method permits pixel rates up to 5 MHz. Each line of pixel information is parallel-loaded into a high-speed bucket-brigade analog shift register and sequentially shifted out. All 256 lines may be sequentially accessed to give a 256-line frame, or alternate odd or even lines may be selected to produce 128 lines per field in an odd and even field pattern. The integration time is nominally one frame period, giving maximum sensitivity.

Features

- 65,536 light-sensitive elements in a high-resolution 256 x 256 matrix
- 40 µm center-to-center element spacing in both X and Y directions
- Frame storage–each diode integrates photocurrent for the entire frame
- Self-scanned in both X and Y directions by high-speed on-chip circuitry to provide either single frame or interlaced odd/even field multiplexed serial video output
- Nonburning sensors
- Solid-state reliability
- Low power dissipation
- 28-pin dual-inline package with scratch-resistant quartz window

General Description

The RA0256B is packaged in a 28-pin dual-inline pin package with a ground and polished window covering the mask-defined active area. Figure 1 is the device's pinout configuration. The device, fabricated on a monolithic silicon chip, contains the matrix diode array with access and reset switches in addition to both the X and Y readout shift registers. Figure 2 is a schematic representation.

A MOS dynamic shift register sequentially selects the diode rows while two bucket brigades connect to each column. Each position of the shift register selects two diode rows through two multiplexing gates, ϕ_A and ϕ_B, one for the odd and the other for the even, providing the user the choice of selecting the odd or even fields.

Together the shift register and the bucket brigade process the signal in the following sequence: The shift register selects two rows, one of which is selected by the ϕ_A or ϕ_B clock. The transfer gates parallel-transfer the selected diode in each column into the bucket brigade.

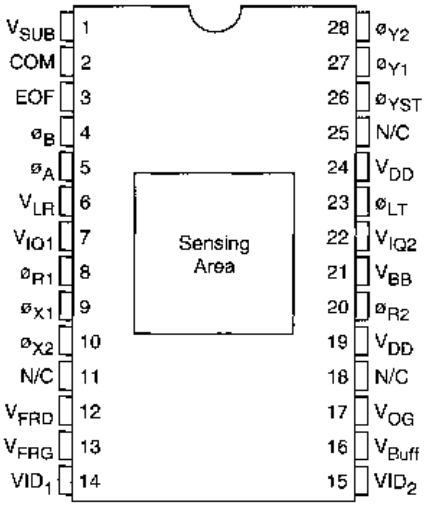


Figure 1. Pinout Configuration

One bucket brigade obtains information from odd and the other from even diode columns and each then shifts that information sequentially to the output. On the output side, there are three extra buckets on the even video transport and two extra buckets on the odd video. Therefore, the even video is delayed an extra 1/2 cycle of the shift frequency, ϕ_{X1}, to obtain the desired time sequence. The alternating odd and even signals are then transferred to corresponding output ports, VID_1 and VID_2.

The integration times are determined by the time interval between accesses for a given diode. This interval can be controlled through the special frame reset clock or through the normal sequential readout. The difference between the two reset processes lies in the integration time for each diode. Frame reset initializes all diodes simultaneously and hence allows each diode to increase the integration time monotonically as the diodes are sequentially read-out–while in the array's normal scanning mode, each diode is accessed periodically with a constant time interval. Hence, in this mode each diode has the same integration time.

Input/Output Definitions and Functional Description

The area array has functional elements which serve to control the timing sequences for diode access, to transport the pixel information to the output, to control integration time, to control the odd and even fields, to provide for interlace, and to buffer each video output. The external circuit provides the timing and the bias to these functional elements as well as clocks to control ϕ_A, ϕ_B, LT, V_{BUFF}, ϕ_{YST}, EOF, FRD, ϕ_{R1}, ϕ_{R2}, V_{IO1},V_{IO2}.

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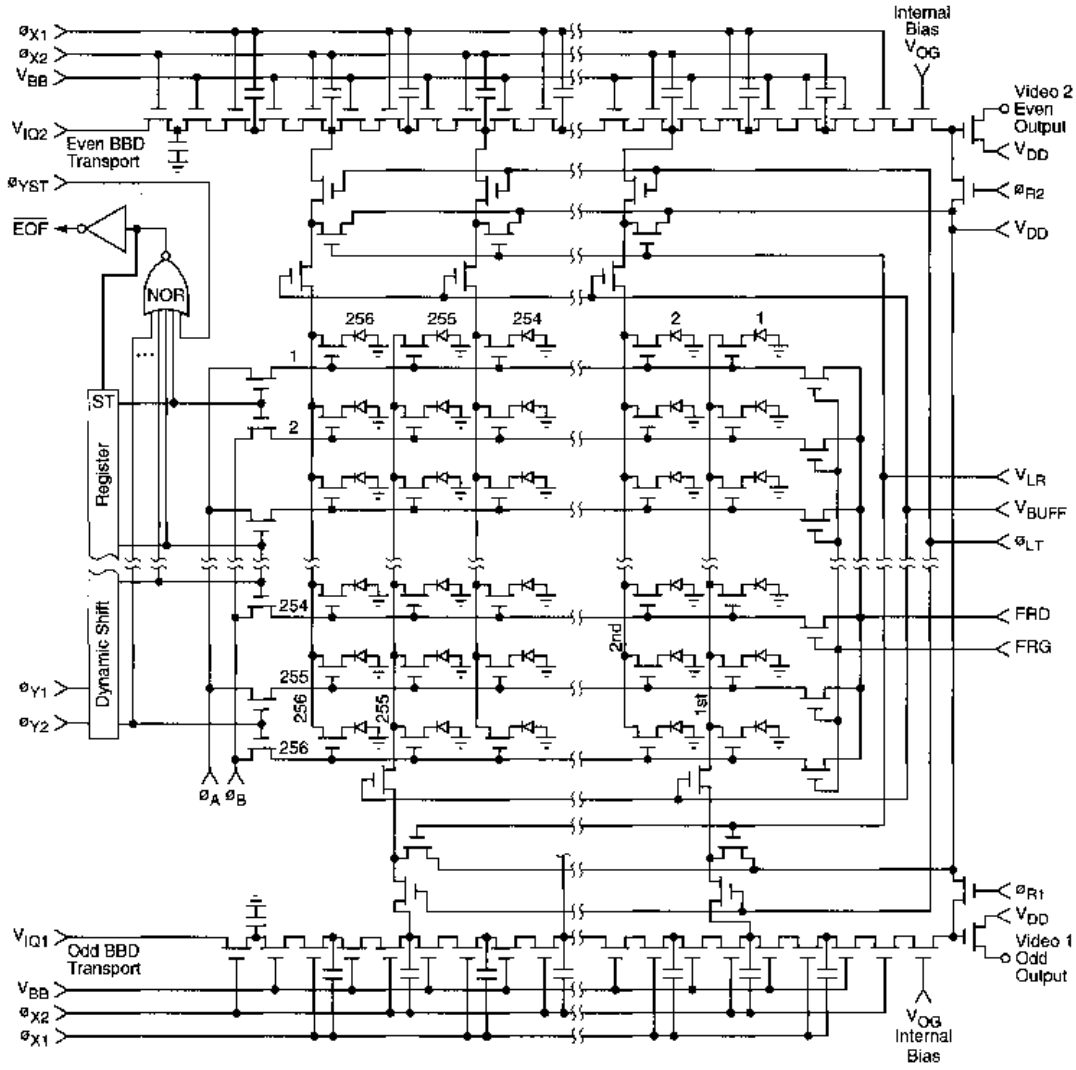


Figure 2. Schematic RA0256B

1. The Odd and Even Bucket Brigade Transports and Their Clocks, ϕ_{X1}-ϕ_{X2}.

Figure 2 shows two bucket brigade analog shift registers located on each side of the device. These are the odd and even transport registers which accept the pixel information in parallel from their respective odd and even video diode columns and shift the pixel information sequentially to the output amplifier. Each bucket brigade must be provided with a two-phase clock as shown in Figure 3. Note: To ensure high transfer efficiency, it is important that the clock waveforms cross at or below the 50% level. The two limits on clock crossing are shown in Figure 3. Normally these clocks swing from a low of 0.4V to a high of 15V.

As evident from Figures 2 and 4, the transfer into both shift registers takes place simultaneously while the ϕ_{X2} is held high. However, the odd bucket brigade produces a pixel first, since it reads out on the second low-going ϕ_{X2} clock after the transfer period. The second pixel is produced by the even shift register. This pixel must transfer through an extra half-stage which is controlled by the ϕ_{X1} clock; thus, even pixels are produced 1/2 cycle out of phase with the odd pixels to provide an easily multiplexed signal by means of a simple adder amplifier.

The multiplexing increases the pixel rate to 2 times the transport clock frequency. See Figure 4 for the clock timing diagram. Figure 5 shows the detailed relationship between ϕ_{X1} and ϕ_{LT}, the line transfer clock. Figure 6 shows the detailed relationship between ϕ_A, and ϕ_B, the vertical multiplexing clocks, and ϕ_Y, the shift register clock.

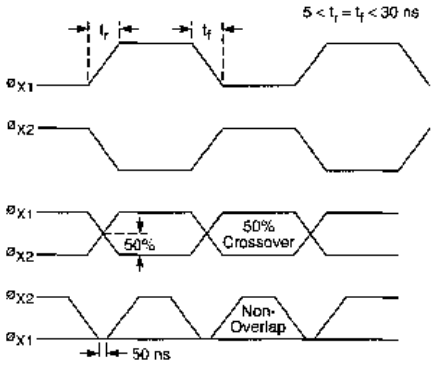


Figure 3. Illustration of $ø_{X1}$ and $ø_{X2}$ Clock Crossover and Time Tolerance

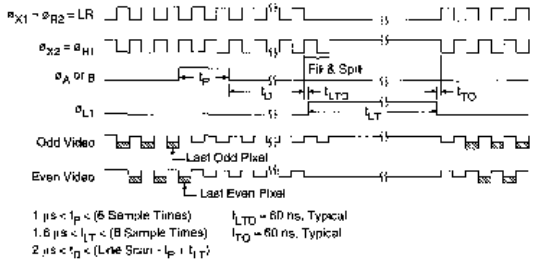
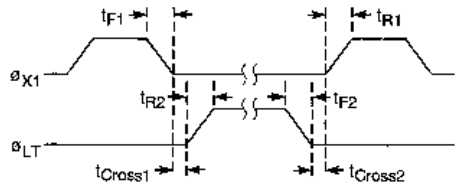


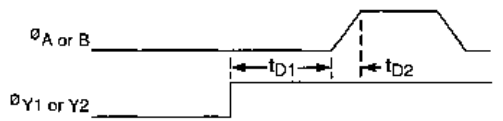
Figure 4. Overall Relationship



0 < t_{F1} < 30 ns
0 < t_{R2} < 30 ns
50% Crossing < $t_{Cross\ 1}$ < 50 ns
$t_{Cross\ 1} = t_{Cross\ 2}$

$t_{F1} = t_{F2}$
$t_{R1} = t_{R2}$

Figure 5. Detailed Timing Between $ø_{X1}$ and $ø_{LT}$



t_{D1} > 1.0 µs
t_{D2} > 10 ns

Figure 6. Detailed Timing Between $ø_A$ or $ø_B$, $ø_{Y1}$ or $ø_{Y2}$

2. The Y Dynamic Shift Register

This shift register is shown in Figure 2 as a block with 128 outputs, each connected to two multiplexing gates plus one extra stage at each end. The gates are connected to two rows of photodiodes and select those rows in accordance to the multiplex clocks, $ø_A$ and $ø_B$. If $ø_A$ and $ø_B$ are alternately clocked, the rows will be sequentially accessed, each selected diode connected to its respective column's video line. Then the photodiode information on each column line is transferred to the bucket brigade. Tied to each stage of the shift register are inputs to a NOR gate which provides for the self-loading feature. When there is a "1" in any of the 130 stages the NOR gate keeps the shift register from loading. Once the bit has been clocked out of the last stage, the NOR gate's output goes high and the shift register loads with the falling edge of $ø_{Y1}$. Note that $ø_{YST}$ is connected to the NOR gate. It can be used to inhibit the register from loading by pulling $ø_{YST}$ to V_{DD}. The register requires a two-phase clock which typically swings from a low of 0.4V to V_{DD}.

Note there are two extra stages, one in the first and another in the last position. The purpose of the stages is to minimize the interference caused by the starting and terminating process of the shift register.

3. Line Select Controls, $ø_A$ and $ø_B$

As evident from the schematic diagram, Figure 2, the $ø_A$ input terminal controls the gates that switch all of the odd-numbered rows from the Y shift register, and the $ø_B$ terminal controls the gates that switch the even-numbered rows. These gates, $ø_A$ and $ø_B$, select the rows of diodes as discussed under Section 2. The time relationship is shown in Figure 6.

4. Line Reset, LR

The LR maintains the potential of the column video line between line transfers by bleeding off the excess charges collected under excess illumination. It will require adjustment when the frame reset function is used. This adjustment is discussed under Optimum Relation Between Clocks and Bias.

5. Line Transfer, LT, and Line Buffer, V_{BUFF}

The LT pulse input controls the period during which the row of diode information is transferred into the bucket-brigade transport registers. This pulse must occur while LR is off (low). Normally this LT input is clocked as seen in Figures 4 and 5 with rise and fall as shown. The line buffer control, V_{BUFF}, is normally held at approximately 0.8 V_{DD} and adjusted to optimize blooming control.

6. Y Shift Register Start, $ø_{YST}$

The $ø_{YST}$ input provides access to one of the inputs to the Y shift register's NOR gate (Figure 2). When this input is held high, the output of the NOR gate is held low and inhibits loading of the shift register; however, when the $ø_{YST}$ input is pulled low, the NOR output rises and a bit is loaded into the register with the falling edge of $ø_{Y1}$ clock. The first two rows are then accessed on the next $ø_{Y1}$ rising edge.

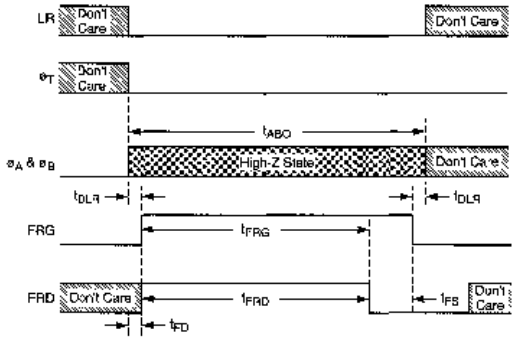
7. End of Frame, EOF

As discussed under ϕ_{YST}, the Y shift register has a NOR gate which provides control for the self-starting feature. The NOR gate output is connected to an external pin through an open-drain inverter. This output is normally tied to V_{DD} through an 8.6 KΩ resistor; therefore, when there is a bit in any row, or if ϕ_{YST} is active, EOF will remain high. It goes immediately low on the rising edge of ϕ_{Y2}, when the bit leaves the last stage of the shift register. This point will sink a maximum of 1.5 ma.

8. Frame Reset, FRG

This input controls access switches to every diode in the matrix and provides simultaneous resetting of all diodes. Since the diodes in each line are automatically reset when the line is accessed, the frame reset control is not normally used, and, as such, is held low. However, when a particular exposure is desired, this control may be used to clear the diodes to start a fresh integration cycle.

The minimum timing requirements for the frame operation are shown in Figure 7. ϕ_A and ϕ_B are held in a high-impedance state during the entire procedure. FRG and FRD are pulsed as shown to connect all photodiodes to their respective video lines. During this connection, the array is taken through at least three line-transfer-and-readout sequences. This resets the video lines and photodiodes through the BBD output registers (the LR function could be used, too, at the expense of



	Min	Typ	Max	Remark
t_{DLR}	200 ns			
t_{ABO}				To be consistant with t_{FRG}
t_{FRG}	2.5 ms		3.5 ms	
t_{FRD}	2.5 ms			
t_{FS}	4.0 µs			
t_{FD}	0.2 µs			

Note: Clock rise and fall times are not critical. However it is recommended not to exceed 0.5 µs. While frame reset is active, the reset takes place by performing at least 3 line scans using the BBD registers. If no bit is in the Y-register (i.e., between frames), ϕ_A and ϕ_B need not be taken to a high-Z state during frame reset.

Figure 7. Timing Sequence for Frame Reset. This is only performed before or after a line transfer sequence.

more fixed-pattern-noise (FPN). This FPN can be reduced by going through one line readout sequence after the line reset is done). After the reset is finished, FRD is taken low to turn off the multiplex switches. It is important to wait the indicated time, t_{FS}, to make sure the multiplex switches are not left with their gates floating "on."

For best performance, the frame reset drain input may require adjustment. The adjustment procedure is described under Optimum Relation Between Clocks and Bias.

9. Reset Clocks for the Gated-Charge Amplifiers, ϕ_{R1} and ϕ_{R2}

These terminals provide reset voltages for the gated-charge amplifiers which are shown in the schematic diagram, Figure 2, at the outputs of both bucket brigades. On the even side, the signal appears at the gate of the output source follower when ϕ_{X1} drops to a low potential. While ϕ_{X1} is high, before the next sample appears, this node is cleared by charging it to a reset voltage. Thus, reset is accomplished when this terminal is clocked synchronously with ϕ_{X1}. The complementary situation applies to the odd output, with signal appearing while ϕ_{X2} is low and reset while ϕ_{X2} is high. The extra half-stage in the even side allows the alternating sequence desired. Normally, the synchronous relationship is obtained by direct connection of ϕ_{X1} to ϕ_{R2}, and direct connection of ϕ_{X2} to ϕ_{R1}. The timing sequence for the output signal is shown in Figure 4 relative to the transfer pulse time.

10. Video Output Terminals, VID_1 and VID_2

The video output is that of a source follower. Normally, the output of each source follower is connected to 1KΩ which is referenced to ground. This configuration provides the proper bias current for the source follower. Figure 8 shows the output voltage across such a load resistor, showing the relationship of the video pixel information relative to the superimposed reset clock amplitude.

Figure 9 shows the output impedance of the source follower as a function of the bias current. This graph can be used to design a desired interface circuit with suitable DC bias translation (e.g., an emitter-coupled transistor with the base biased up near the video output line potential).

11. Input Bias, V_{IQ1} and V_{IQ2}

Bias voltages are connected to the inputs of both bucket-brigade transports: V_{IQ1} to the odd and V_{IQ2} to the even. These inputs control the bias level in the dark. Nominally, these terminals are biased to approximately 10V.

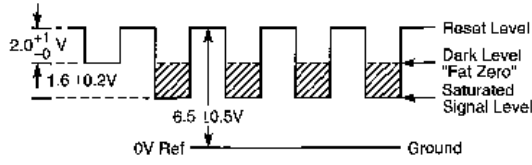


Figure 8. Typical Video Signal Across a 1 KΩ Output Load

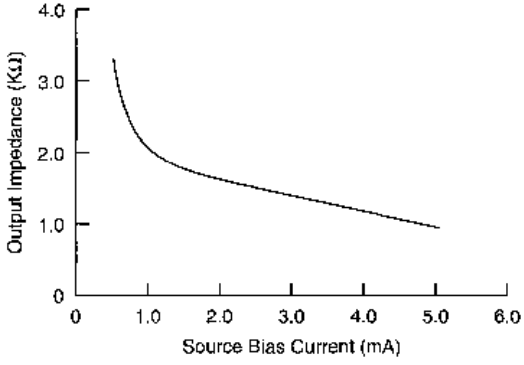


Figure 9. Output Impedance vs. Output Source Current

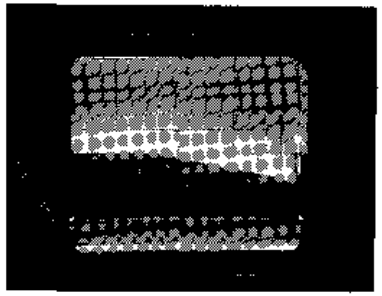


Figure 10a. Scope Output

An example of worst case adjustment. Single frame scan of video output after frame reset. Horizontal 0.5V/div, Vertical 0.002 sec/div.

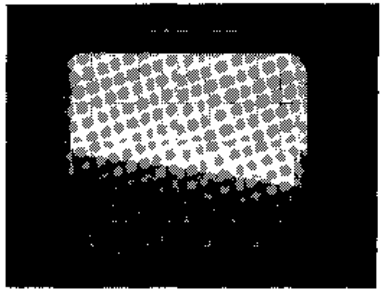


Figure 10b. Scope Output

An example of properly biased output. Single frame scan of video output after frame reset. Horizontal 0.5V/div, Vertical 0.002 sec/div.

Adjustment of V_{IQ1} and V_{IQ2}

Since V_{IQ1} and V_{IQ2} bias the internal operating levels of the bucket brigade, they affect the output signal level. Since there are two bucket brigade outputs, when the two are summed together, an odd and even imbalance may be experienced. One easy method to balance out the odd and even patterns in the summed video is to make one of the V_{IQ} inputs adjustable.

Typically these voltages are set to 10V and they will produce an output bias condition as seen in Figure 8 where the difference between the "fat zero" (or the dark level) and the reset level will maintain a magnitude of approximately 2V. However, when V_{BB} is reduced, the "fat zero" level reduces proportionally. In this case, V_{IQ1} and V_{IQ2} may be reduced to maintain the "fat zero" level. In any case, both V_{IQ} voltages and V_{BB} must be limited according to $7<V_{IQ}<10V$ and $8.5<V_{BB}<V_{DD}-0.5$.

Optimum Relation Between Clocks and Bias

Greatest performance from the device is normally obtained with the ϕ_{X2} and LT clocks interleaved as shown in Figure 4. In this mode of operation the optical to electrical transfer function is given in Figure 11. The dynamic range is in excess of 100:1 with an rms noise-equivalent exposure of less than $.5 \times 10^{-3}$ $\mu J/cm^2$.

The important relationships that must be observed are timing of the clock transitions of ϕ_{X1}, ϕ_{X2}, ϕ_{Y1} and ϕ_{Y2}; the zero level of LT; and the relative timing relationship between LT and ϕ_{X2} (this creates a fill-and-spill phenomenon to improve transfer efficiency). Furthermore, when FR is employed, both the LR and FR voltage level will require adjustment (see Frame Reset Adjustment).

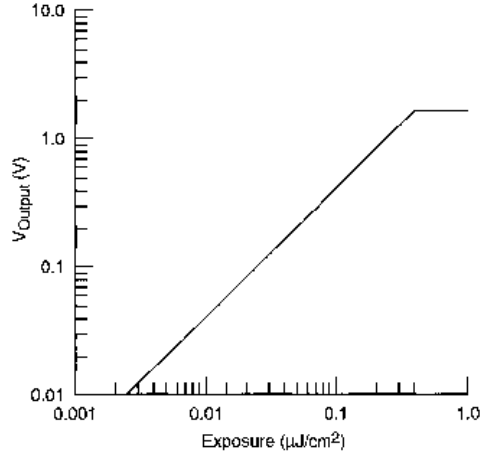


Figure 11. Exposure Chart

ϕ_{X1} and ϕ_{X2} are complementary clocks with crossover of the transition edge taking place at or below 50% of the clock amplitude. Rise and fall times preferably are on the order of 20 nanoseconds. If an MH0026 or equivalent is employed, place a 50Ω resistor in series between the driver output and the clock input pins. This edge control is required to obtain the optimum efficiency from the bucket-brigade transport (refer to Figure 3 for ϕ_X clock shapes).

ϕ_{Y1} and ϕ_{Y2} also are complementary and should cross approximately at the 50% level at the transition edges and should have rise and fall times the same as the ϕ_X clocks. The transition-edge spacing of the interleaving clocks ϕ_{LT} and ϕ_{X2} should be kept as shown in the detailed timing diagram of Figure 4.

Frame Reset Adjustment

When FR is employed, FRD and V_{LR} voltages may require adjustment. With the application of the voltage as given in the specification table, the array will provide operation suitable for most applications. However, to obtain the best balance between low noise, high sensitivity, and antiblooming control, the following adjustment procedure is recommended.

With the array operating with the voltages as specified in the specification table, make the following adjustment: Apply a uniform light across the array surface to provide an output which is approximately 1/4 of the total saturated output. Apply the frame reset clock as specified in Figure 7 and the specification table. Operate the array atapproximately 2 MHz sampling rate. With the Frame Reset pulse synchronized to the scope, the frame scan as shown in Figure 10A will be seen. Lower LR amplitude to approximately 12V then lower FRD voltage towards 10V until a linear output as seen in Figure 10B is achieved.

Transfer Function and Spectral Response

Figure 11 is a transfer function graph which shows a linear optical-to-electrical relationship with dynamic range exceeding 100:1. This linear relationship depends on the proper electrode potentials, especially those for V_{BUFF} and the line reset level, LR. Improper potentials can cause substantial nonlinearity.

The array spectral response is shown in Figure 12.

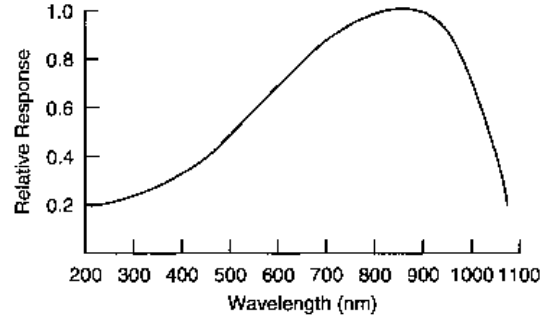


Figure 12. Photodiode Response

Table 1. Array Mechanical Characteristics

		Units
Number of diodes	65,536	
Diode X, Y center-to-center spacing	40/1.57	µm/mils
Diode sensing area	912 µm²	
Package size (28-pin)	0.8 x 1.4	inch

Table 2. Terminal Input Capacitance

Typical Capacitance with 10V Bias		
Pin	**Sym**	**Capacitance (pF)**
3	End of frame	5
4	ϕ_B	21
5	ϕ_A	21
6	V_{LR}	48
7	V_{IQ1}	5
8	V_{R1}	6
9	ϕ_{X1}	150
10	ϕ_{X2}	150
12	ϕ_{FRD}	50
13	ϕ_{FRG}	29
14	VID_1	6
15	VID_2	6
16	V_{BUFF}	64
17	V_{OG}	6
20	V_{R2}	4
21	V_{BB}	101
22	V_{IQ2}	5
23	ϕ_{LT}	43
26	ϕ_{YST}	4
27	ϕ_{Y1}	28
28	ϕ_{Y2}	28

Table 3. Array Performance Characteristics (T_A = 23°C)

Sym	Parameter	Typ	Max	Units
DR	Dynamic range (P-P) [1]	100:1		—
E_{NE}	Peak-to-peak noise equivalent exposure [2]	2.5 x 10^{-3}		$\mu J/cm^2$
E_{Sat}	Saturation exposure [2]	0.4		$\mu J/cm^2$
R	Responsivity [2]	4		$V/(\mu J/cm^2)$
PRNU	Photoresponse nonuniformity [1,2]	±10	±15	%
V_{Dark}	Average dark signal [3]	1	2	%
V_{Sat}	Saturation output voltage [4]	1.6	2	V
R_O	Output impedance [5]	1		KΩ
f_s	Video sample rate [6]		5	MHz

Notes:
1 Ignoring lines 1, 2 and 256 as well as the first and last two diodes of each line
2 2870°K tungsten lamp with a Fish Schurman HA-11 visible spectrum filter was used as the source
3 Integration time 20 ms. Dark signal changes by a factor of 2 every 7°C
4 Voltage measured across 1.5KΩ load resistor
5 See Figure 9
6 Odd and even video outputs combined

Table 4. Electrical Specifications

	Parameter				
Definition	Sym	Min	Typ	Max [3]	Dimension
X-register clock amplitudes [2]	$ø_{X1}$	11.5	14	V_{DD}	V
	$ø_{X2}$	11.5	14	V_{DD}	V
Y-register clock amplitudes [2]	$ø_{Y1}$	11.5	14	V_{DD}	V
	$ø_{Y2}$	11.5	14	V_{DD}	V
Y shift register reset amplitude	$ø_{YST}$	11.5	14	V_{DD}	V
Line transfer amplitude	$ø_{LT}$	11.5	14	V_{DD}	V
Line reset amplitude	V_{LR}	9	12	V_{DD}	V
X-register input bias odd	V_{IQ1}		10		V
X-register input bias even	V_{IQ2}		10		V
Video reset 1 (odd)	VR_1		V_{DD}-0.5	V_{DD}	V
Video reset 2 (even)	VR_2		V_{DD}-0.5	V_{DD}	V
Frame reset gate [1]	FRG		V_{DD}-0.5	V_{DD}	V
Frame reset drain [1]	FRD		10	V_{DD}	V
Isolation gate	V_{Buff}	11	12.75	13	V
DC supply	V_{DD}	11.8	15	16	V
DC current	I_{DD}	6	8	10	mA
X-register tetrode gate bias	V_{BB}	8	12.5	V_{DD}-.5V	V
Multiplex clock amplitude	$ø_A$	11.5	14	V_{DD}	V
Multiplex clock amplitude	$ø_B$	11.5	14	V_{DD}	V
Substrate bias	V_{Sub}	-2.95	-3.3	-3.65	V

Notes:
1 See text
2 All voltages measured with reference to common (ground). See text
3 For optimum performance use typical value. Other in-spec voltages will operate the array but with reduction in performance

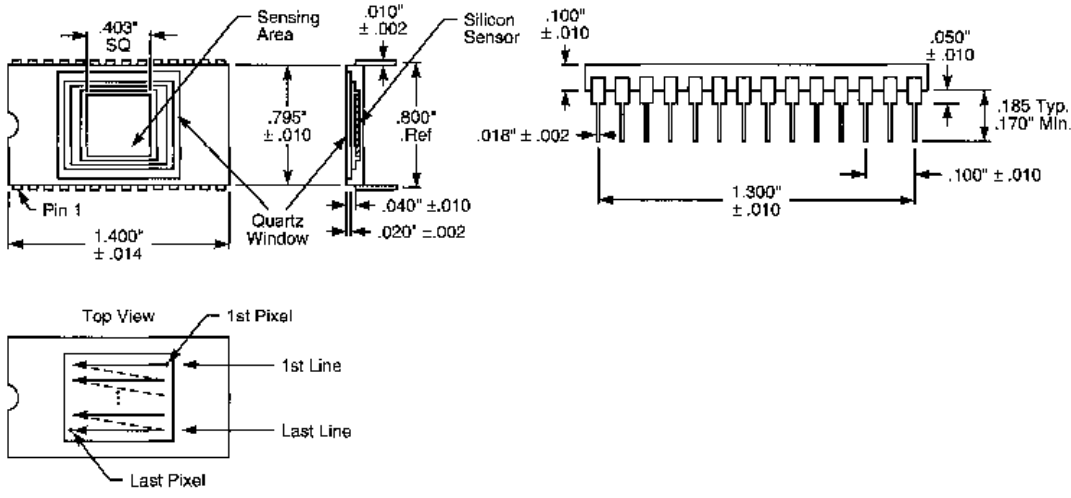


Figure 13. Package Dimensions and Scanning Sequence

Ordering Information

Part Number	Evaluation Circuit (Current Amplifier)	Adjacent Defects Forming a Group
RA0256BAQ-011 (1-12 defects)	RC0503ANC-011	up to 2
RA0256BAQ-020 (13-50 defects)	RC0503ANC-011	up to 4

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General Description

The RA1441A is a self-scanned area photodiode array containing 14 rows of 41 sensing elements each. The center-to-center spacing of the elements along each row is 4.1 mils; the center-to-center spacing between rows is 3.6 mils.

Scanning is accomplished by means of a static shift register which sequentially samples the diodes in each line with all 14 lines being read out in parallel. The shift register is driven by an externally-generated single-phase TTL level Clock which determines the sample frequency. The device is operated in the internal start mode; no additional timing signals are required. There is a "flyback" time of two sample periods between the completion of one scan and the beginning of the next, thus, the readout time is given by $43/f_S$, where f_S is the clock frequency. An EOS output pulse is provided during the flyback time to indicate the completion of each scan.

Package

The RA1441A is packaged in a standard 22-pin ceramic DIP with a ground and polished window. Package dimensions are approximately 0.4 x 1.1 inches. Pinout configuration is shown in Figure 1 and package dimensions are shown in Figure 5.

Performance

A test circuit which provides the clock input, load resistors and biasing is shown in Figure 2. Clock frequency is set by potentiometer R_1 and operation is guaranteed up to 400 kHz.

Typical spectral response is shown in Figure 3.

Equivalent Circuit and Timing

Figure 4 is an equivalent circuit showing a 3 x 3 section of the RA1441A. To accomplish each scan, a sampling pulse is automatically loaded and clocked through the shift register so that each cell is accessed in sequence for one clock period. A source follower on each cell provides a high level boxcar type output across an external load resistor connected between each video line and common. Note that while a cell is being sampled, the previous cell is being reset to the negative supply voltage. Between the time it is reset and the time it is accessed on the next scan, the voltage on a cell will decay by an amount proportional to the exposure on that cell (light intensity times scan time). Thus, the remaining voltage on the cell when it is sampled is a measure of the light intensity. The output becomes more positive with increasing exposure, saturating at 0V (common). The EOS signal is normally obtained across a load resistor connected between the EOS output and V_{DD}.

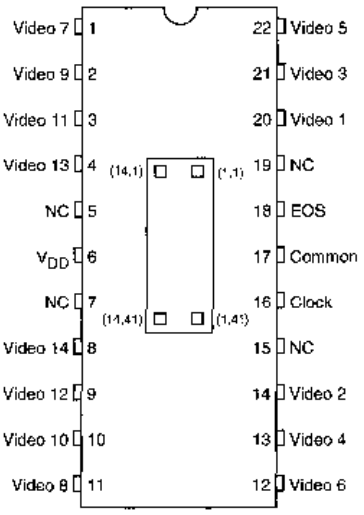


Figure 1. Pinout Configuration

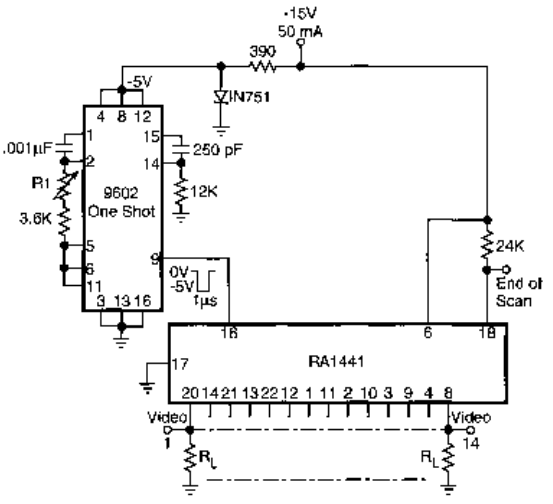


Figure 2. Test Circuit Schematic

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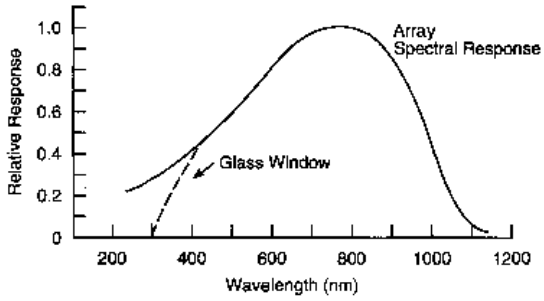


Figure 3. Typical Spectral Response

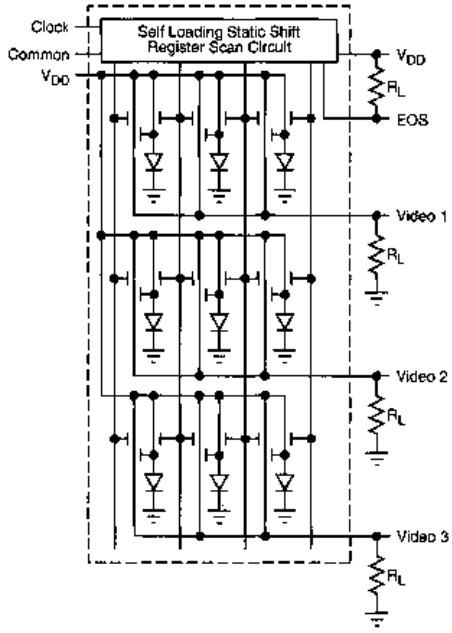


Figure 4. Equivalent Circuit

RC0501A Evaluation Board for RA1441A Photodiode Array

This board, which mates with a standard 22-pin edge connector, provides appropriate interface circuits for evaluating the RA1441A. The circuit requires a single negative supply voltage and provides clock, sync, and all video outputs. As supplied, the clock frequency may be adjusted over the range 50 to 200 kHz using a trim pot. Higher or lower frequency ranges can be obtained by simply changing a capacitor on the board. If desired, an external clock may be used by changing in the INT-EXT jumper to external and connecting the external clock to pin 21.

The video outputs are taken across 51KΩ load resistors suitable for operation up to about 200 kHz. At higher frequencies (up to 400 kHz) lower value load resistors should be used. Output voltage swing (dark to saturation) is proportional to load resistance and V_{DD}, and is about 2V with 50KΩ loads and -17V. V_{DD} can be operated between -12 to -17V. External capacitance should be kept below 50 pF on all outputs. Clock supplied on pin 22 of edge connector is inverted from that supplied to pin 16 of the array.

Table 1. Electrical Characteristics (25°C) [1]
(Voltages with respect to common)

	Min	Typ	Max	Units
Supply voltage (single supply)	-12		-17	V
Clock amplitude (single phase)	-5		-15	V
Maximum scan rate			400	kHz
Average output voltage from saturation to dark (-15V supply, 51KΩ load, 100 kHz scan rate)		-2.0		V
Timing			43	clock cycles per scan

Note:
[1] Test Conditions:
a. V_{DD} = -17V with respect to common
b. Clock swing = -12V with respect to common
c. Clock frequency = 250 kHz
d. Load resistance = 51KΩ
e. 2870°K Tungsten light source
f. Approximate 50% saturation level

Table 2. Electro-Optical Characteristics [1,2]

	Min	Typ	Max	Units
Saturation exposure	.042	.070	.170	$\mu J/cm^2$
Dark level nonuniformity [2]			±10	%
Nonuniformity (per line) at 50% saturation [2]			±12	%
Line-to-line deviation			10	%
Dark level minimum diode	-2.25		-3.25	V

Notes:
[1] Test Conditions:
a. V_{DD} = -17V with respect to common
b. Clock swing = -12V with respect to common
c. Clock frequency = 250 kHz
d. Load resistance = 51KΩ
e. 2870°K Tungsten light source
f. Approximate 50% saturation level
[2] Nonuniformity is defined as the difference in output voltage of the highest and lowest elements in each line divided by the average voltage swing between dark and saturation. The 41st element of each row is not included in nonuniformity measurements.

Table 3. Mechanical Characteristics

	Typ	Units
Number of diodes	574	
Element spacing center-to-center	4.1 along row	mils
	3.6 between rows	mils
22-Pin DIP package size		
Width	0.4	inch
Length	1.080	inch

Absolute Maximum Rating

	Min	Max	Units
Storage temperature	-25	+85	°C
Temperature under bias	0	+70	°C

22-pin Ceramic

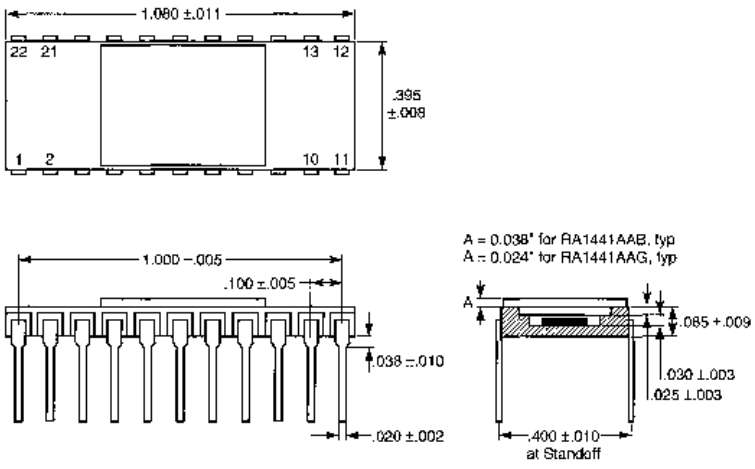


Figure 5. Package Dimensions

Ordering Information *

Part Number	Evaluation Circuit
RA1441AAB-011	RC0501ANN-011

* Includes standard devices. For options, consult your local sales office.

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General Description

The RA1662N is a self-scanned area photodiode array containing 16 rows of 62 sensing elements each. The center-to-center spacing of the elements along each row and between rows is 100 µm.

Scanning is accomplished by means of a static shift register which sequentially samples the diodes in each line, with all 16 lines being read out in parallel. The shift register is driven by an externally generated single phase TTL level Clock which determines the sample frequency. If the device is operated in the internal start mode, no additional timing signals are required and there is a "flyback" time of two sample periods between the completion of one scan and the beginning of the next. Thus, the readout time is given by $64/f_s$, where f is the clock frequency. If desired, the flyback time can be increased arbitrarily by holding the Start Inhibit input negative until it is desired to initiate a scan. An EOS output pulse is provided during the flyback time to indicate the completion of each scan.

Packaging

The RA1662N is packaged in a standard 22-pin ceramic DIP with a ground and polished window. Package dimensions are approximately 0.4 x 1.1 inches. Pin configuration and the direction of scan relative to the package are indicated in Figure 1 and package dimensions are shown in Figure 6.

Performance

A test circuit that provides the clock input, load resistors and biasing is shown in Figure 2. Clock frequency is set by potentiometer R_1 and will operate up to 400 kHz. The array supply voltage V_{Array} may be varied using potentiometer R_2 to adjust the dark output voltage to the desired value. By using this adjustment, V_{Dark} on all arrays may be set at any value over a minimum range of 0 to -2.5V.

Typical spectral response is shown in Figure 3 and typical curves of output voltage versus exposure for 2870° K tungsten light source are shown in Figure 4.

All of the data reported here was taken with 25KΩ load resistors. It should be noted that if the load resistance is too high or if there is capacitive loading, the time required to make a light/dark transition will be increased.

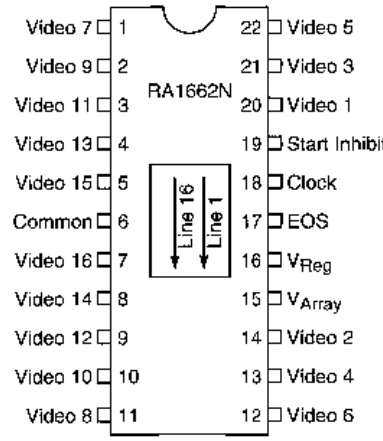


Figure 1. Pinout Configuration

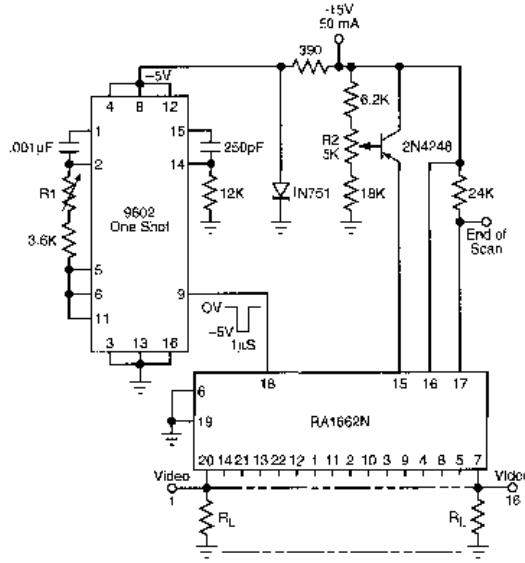


Figure 2. Test Schematic

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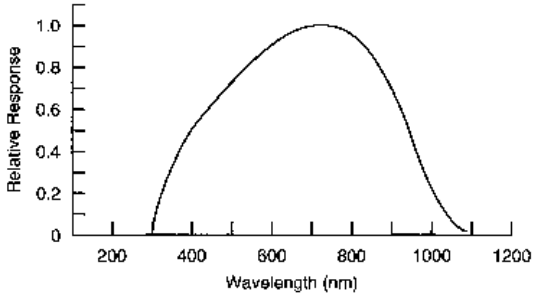


Figure 3. Typical Spectral Response

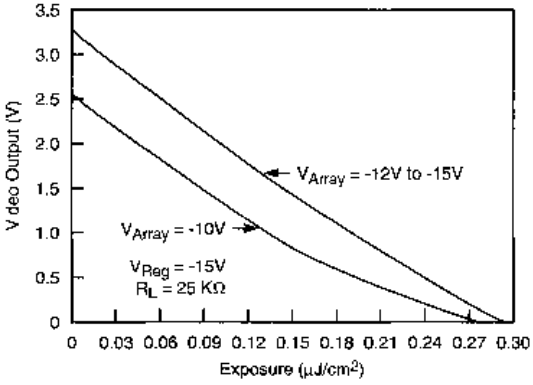


Figure 4. Typical Curves of Output Voltage Versus Exposure

Equivalent Circuit and Timing

Figure 5 is an equivalent circuit showing a 3 x 3 section of the RA1662N. Separate supply voltage inputs V_{Reg} and V_{Array} are provided to the shift register and the diode array, respectively. The shift register supply V_{Reg} is nominally -15V. The array supply may be the same as the register supply or it may be adjusted several volts lower. Reducing V_{Array} reduces the amplitude of the video output.

For operation in the internal start mode, the Start Inhibit input is connected to Common. In this mode a new scan is automatically initiated every 64 clock periods. To accomplish each scan, a sampling pulse is automatically loaded and clocked through the shift register so that each cell is accessed in sequence for one clock period. A source follower on each cell provides a high level boxcar type output across an external load resistor connected between each video line and common. Note that while a cell is being sampled, the previous cell is being reset to the negative supply voltage. Between the time it is reset and the time it is accessed on the next scan, the voltage on a cell will decay by an amount proportional to the exposure on that cell (light intensity times scan time). Thus, the remaining voltage on the cell, when it is sampled, is a measure of the light intensity. The output becomes more positive with increasing exposure, saturating at 0V (common). The EOS signal is normally obtained across a load resistor connected between the EOS output and V_{Reg}.

In the above and all subsequent discussions, it is assumed that the device is operated with the common terminal held at ground and the clock swinging negative with respect to ground. However, for TTL compatibility, it is sometimes desirable to bias the common terminal at +5V and V_{Reg} at -10V. The Clock should then swing from +5V to ground. With this biasing scheme, the video signal is referenced to +5V in saturation and swings negative to about +3V in the dark.

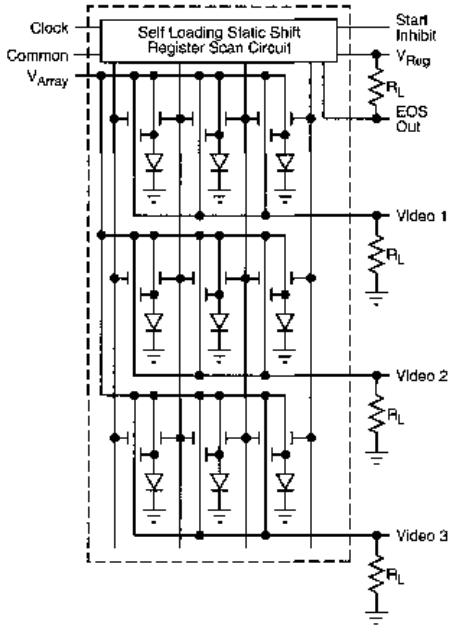


Figure 5. Equivalent Circuit of a 3 x 3 Section of RA1662N

Table 1. Electrical Characteristics (25°C)
(Voltages with respect to common)

	Min	Typ	Max	Units
Supply voltage (single supply)	-12		-17	V
Clock amplitude (single phase)	-5		-15	V
Maximum scan rate			400	kHz
Average output voltage from saturation to dark [1, 2]			-2.25	V
Timing			64	pixels per scan

Notes:
1 A separate pin is provided to bring all array outputs within ±10% using a single potentiometer adjustment.
2 Test conditions:
a. V_{DD} = -15V with respect to common
b. Clock swing = -10V with respect to common
c. Clock frequency = 250 kHz
d. Load resistance = 25KΩ
e. 2870° K tungsten light source
f. Approximate 50% saturation level

Table 2. Electro-optical Characteristics [1]

	Min	Typ	Max	Units
Saturation exposure		0.3		$\mu J/cm^2$
Dark level nonuniformity [2]			±10	%
Nonuniformity (per line) at 50% saturation [2]			±12	%
Line-to-line deviation			±10	%
Dark level minimum diode			-2.25	V

Notes:
1 Test conditions:
a. V_{DD} = -15V with respect to common
b. Clock swing = -10V with respect to common
c. Clock frequency = 250 kHz
d. Load resistance = 25KΩ
e. 2870° K tungsten light source
f. Approximate 50% saturation level
2 Nonuniformity is defined as the difference in output voltage of the highest and lowest elements in each line divided by the average voltage swing between dark and saturation. The 62nd element of each row is not included in nonuniformity measurements.

Table 3. Mechanical Characteristics

	Typ	Units
Number of diodes	992	
Element spacing center-to-center	100 x 100	µm
Package size:		
22-pin DIP, ground and polished window, hermetically sealed	0.4 x 1.1	inches

22-pin Ceramic

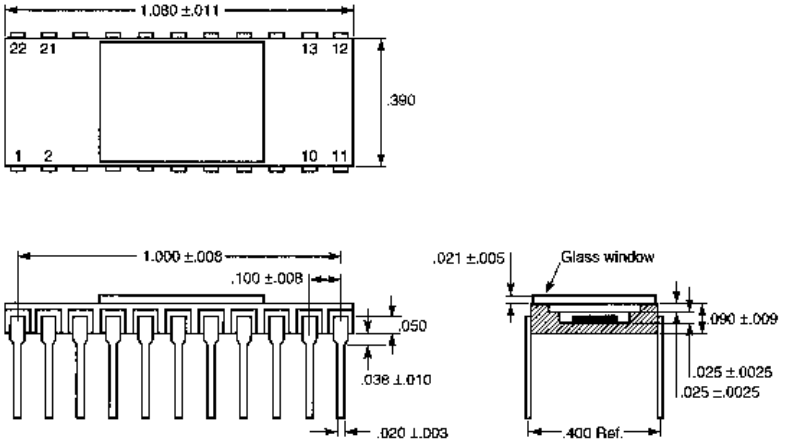


Figure 6. Package Dimensions

Ordering Information*

Part Number	Ordering No.
RA1662N	RA1662NAG-011

* Includes standard devices. For all options, consult your local sales office.

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EG&G RETICON

RA2568N
High-Speed Solid State Image Sensor Array

General Description

The EG&G Reticon RA2568N High Speed Tapped 256 x 256 Array is a two-dimensional scanned optical array with optimized-geometry of 65,536 discrete photodiodes read through eight video output taps providing high frame rate, minimal interference-pattern loss, and the full inherent sensitivity of the photodiode structure.

The RA2568N is available in a 28-pin dual-inline package with a ground and polished quartz window over the active area. Figure 1 shows the pinout configuration. The device, fabricated in monolithic NMOS silicon, contains a diode array matrix with access and reset switches in addition to eight X and a single Y readout register. Figure 2 is a block diagram of the device. The array mechanical specification is given in Table 1.

Key Features

- High frame rate: 500 frames/second
- 40 µm spacing in X and Y directions
- Frame storage: diodes integrate photocurrent for entire frame
- Low power dissipation
- 28-pin dual-inline package
- Frame reset capability

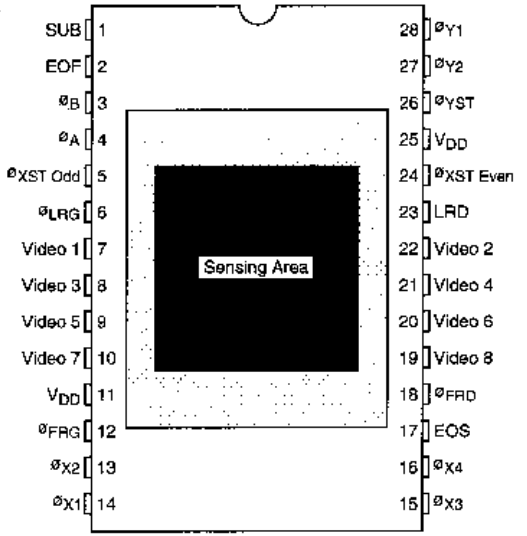


Figure 1. Pinout Configuration

Operation

There are 256 columns and 256 rows of photosensors with center-to-center spacing of 40 µm in both the vertical (Y) and horizontal (X) axis. The individual photosensor is formed by a p-n junction diode with an associated junction capacitance. The photosensors in one column are connected to a common video line through an access switch. All the access switches in one row are connected in parallel and turned on simultaneously by the Y Scanning Shift Register. Photosensors connected to each access switch operate in a charge-integration mode.

When a row of 256 switches are closed by the Y Register, the photodiode charge is placed on each of the column video lines. The horizontal scanning Shift Register switches the charges out in groups of 32 sequential pixels through 8 video output ports. A train of 32 pixels is sequentially scanned by each of eight horizontal shift registers, which divides the array into four sections. Four of the shift registers scan out the odd numbered pixels while the other four scan even numbered pixels.

I/O Functions

Y-Register Clocks

The Y Register is a dynamic shift register driven with complementary clocks ($ø_{Y1}$, $ø_{Y2}$). A Start-Inhibit Pulse ($ø_{YST}$) controls or inhibits the loading of the shift registers. To keep the number of shift register stages to 128 while accessing 256 rows, each shift register position is provided with two multiplexing switches which are clocked by $ø_A$ and $ø_B$. As the shift register is scanned, these switches alternate the bit on each of the register's outputs between two vertical lines, thus accessing two rows of diodes for each of the register positions (256 rows are accessed with 128 stages). There are two additional dummy stages, one at the beginning and one at the end of the register, for a total of 130 shifts for one Y scan. The typical clock waveforms ($ø_{Y1}$, $ø_{Y2}$, $ø_A$, $ø_B$, and $ø_{YST}$) are depicted in Figure 3, and their timing relationship is given in Table 2.

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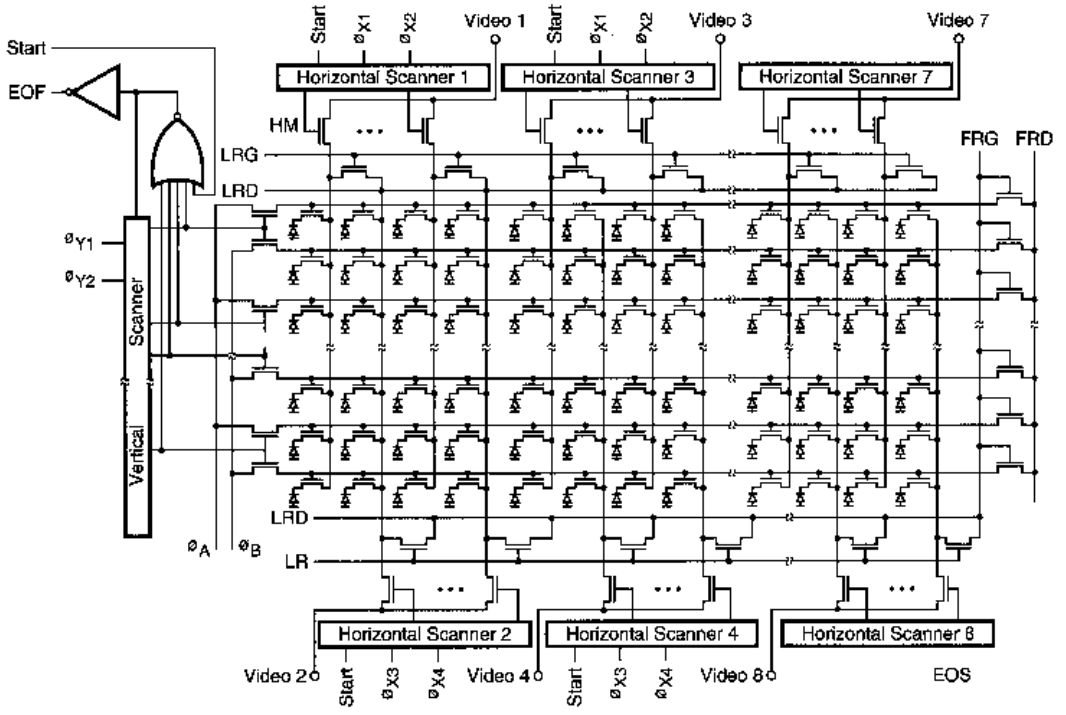


Figure 2. Block Diagram

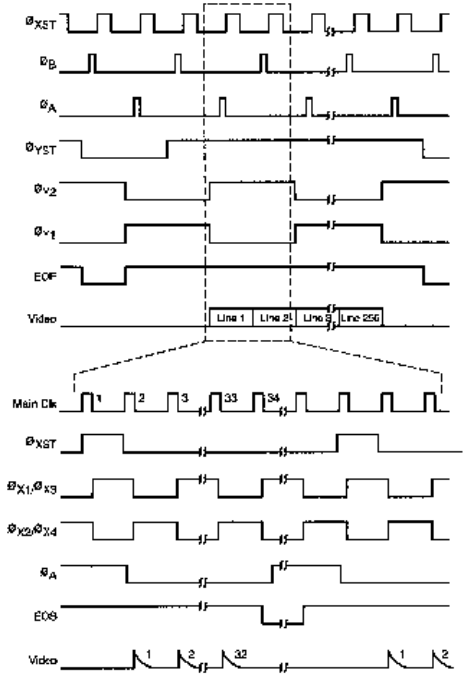


Figure 3. Timing Diagram

X Register Clocks

The eight X Registers are also dynamic shift registers requiring two-phase complementary clocks (ϕ_{X1} and ϕ_{X2} for the odd video scanner and ϕ_{X3} and ϕ_{X4} for the even video scanner). The shift register starts when a start pulse (ϕ_{XST} Odd and ϕ_{XST} Even) is loaded into the register. There are two additional dummy stages other than the required 32 stages, one at each end. The typical clock waveforms are depicted in Figure 4 and relative timing relationship is given in Table 2. As shown on the timing diagrams, the start bit loads into the even (odd) register on the falling edge of the ϕ_4 (ϕ_2) clock.

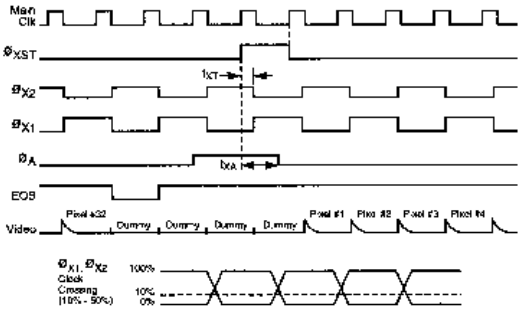


Figure 4. Timing Diagram of X Clock. (Note: ϕ_{XST} Is for reference only)

Line Reset Gate and Drain

Line Reset Gate (LRG) and Line Reset Drain (LRD) are used to reset the charges that accumulated on the video lines and to clamp the video line to a reference voltage just prior to accessing the photodiodes. The drain is normally connected to the same potential as its corresponding video output.

Frame Reset Gate and Drain

The Frame Reset Gate (FRG) and Drain (FRD) are used to recharge the photodiodes prior to the initiation of a frame integration period involving the simultaneous integration of all photodiodes. Both inputs are clocked during the diode-recharging duration. The FRD and FRG must be activated and released as shown in Figure 5, which shows the typical waveforms and timing relationships between Y clocks and the frame reset clocks.

Signal Processing Circuit

The signal output charge is proportional to the photosite exposure. The charges are processed through a circuit (or its equivalent) as depicted in Figure 6. Photo-integrated charges are converted to voltages by the transconductance amplifier and are integrated. The integrated pulses are then sampled and held to provide the zero-order hold signal.

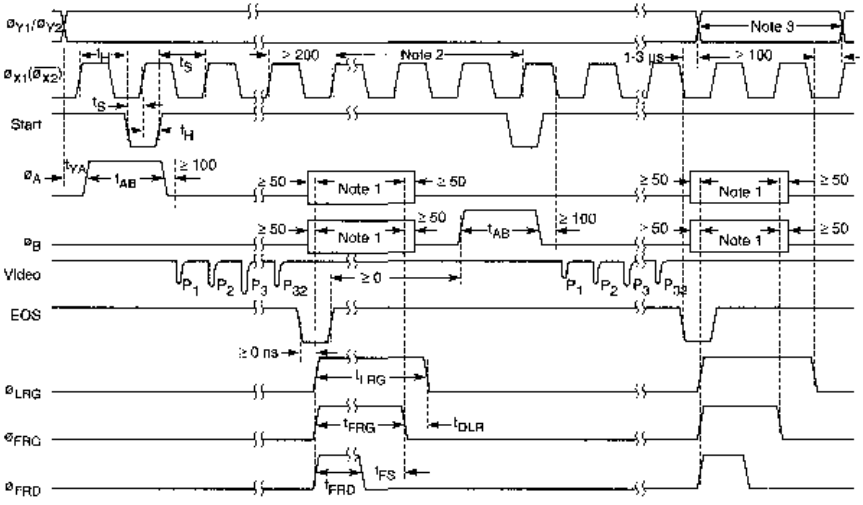
Electrical Specifications

Table 3 lists I/O pins' corresponding symbols, functions, and electrical specifications. Electrical functions are described in the text. Clock waveforms and their respective timing relationships are described under I/O Functions.

Table 4 lists the capacitance of each terminal.

Performance Characteristics

Table 5 lists the optical and electrical signal performance characteristics. The output signal format will depend on the charge-converting circuit; for example, the saturated charge of 0.8 pC can be transformed to current or voltage pulses through a transconductance amplifier, or it can be converted to voltage determined by capacitance through a charge integrator, similar to the integrator in Figure 6.



Note 1: ϕ_A and ϕ_B must be equal to ϕ_{FRD} while ϕ_{FRG} is high, or ϕ_A and ϕ_B can be in a high-impedance state.

Note 2: This time period can last up to several ms.

Note 3: The ϕ_{Y1}/ϕ_{Y2} transition can occur at either of the indicated places, not both.

Note: All measurements are in nanoseconds unless otherwise indicated.

Figure 5. Timing Diagram of Resets

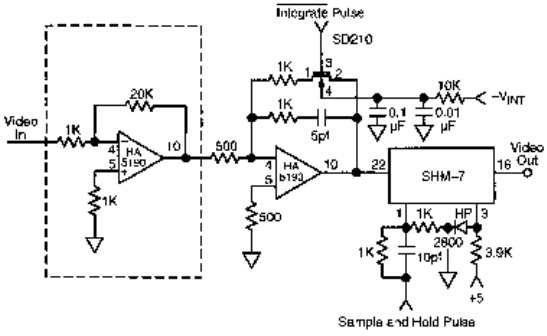


Figure 6. Signal Processing Circuit

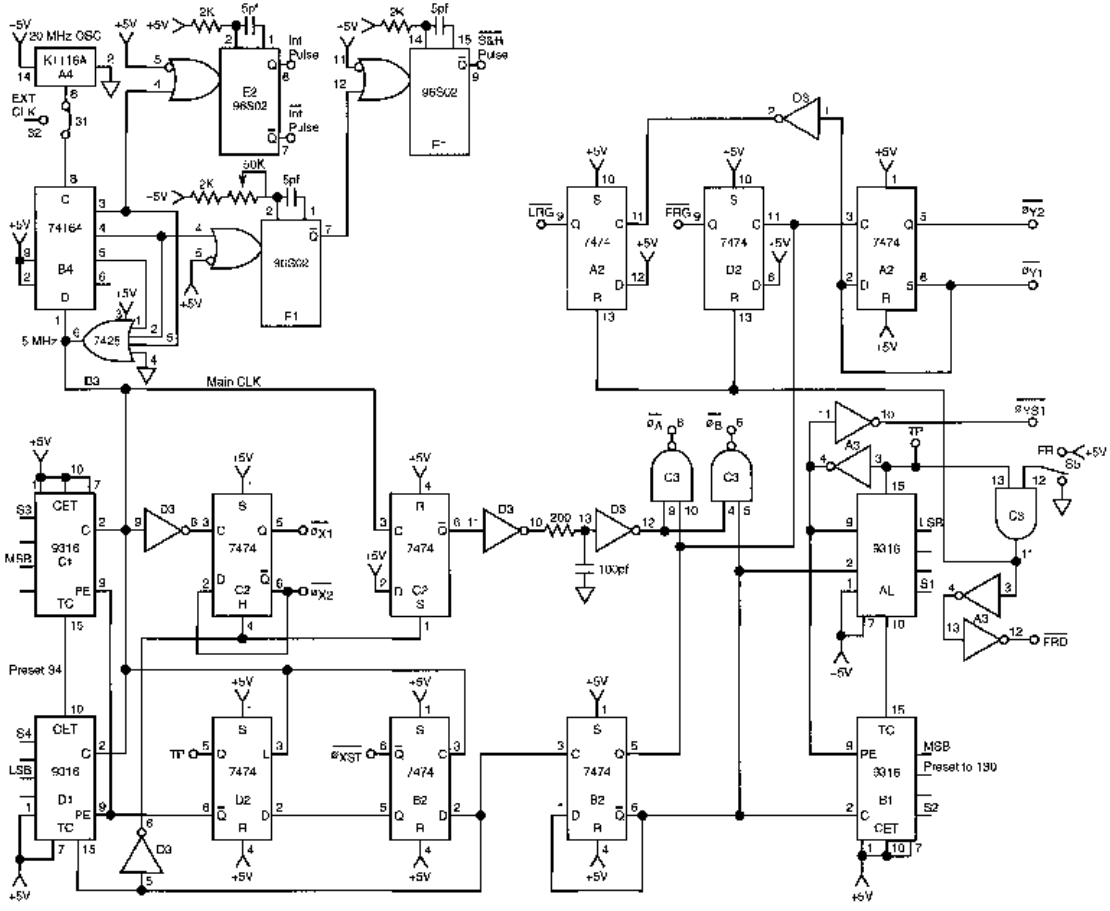


Figure 7. Digital Application Circuit

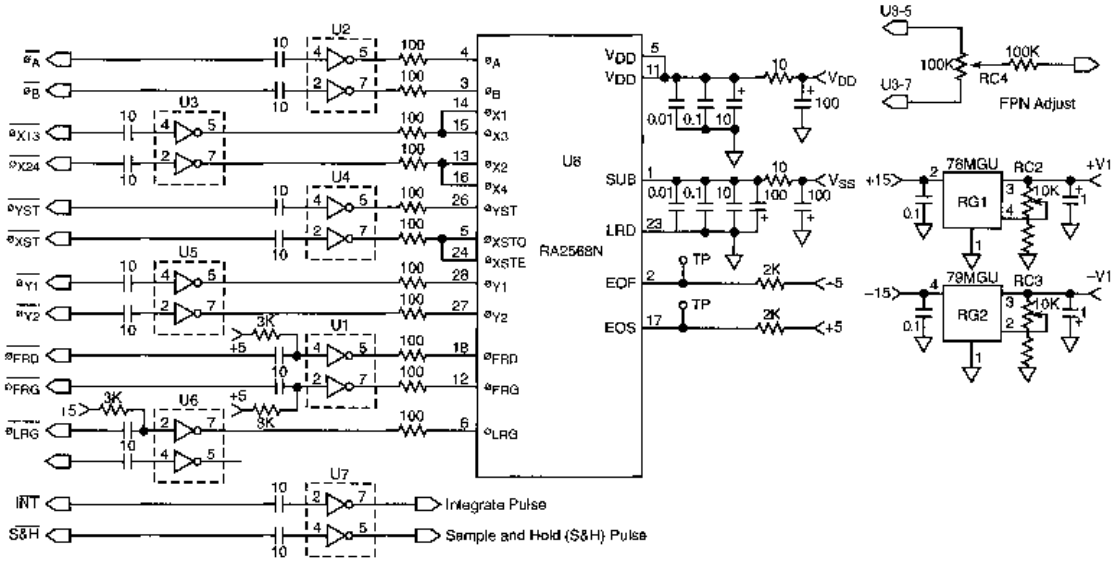


Figure 8. Evaluation Board Circuit

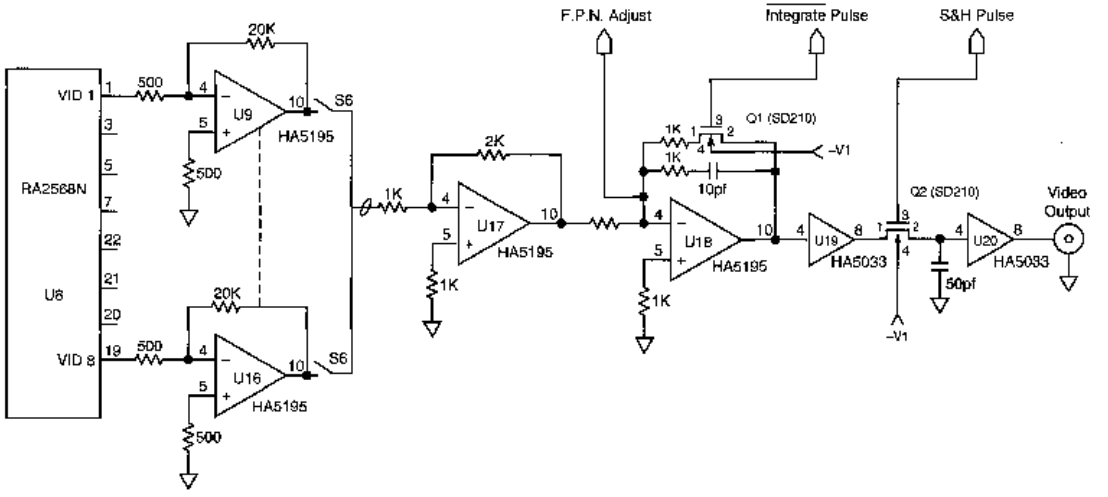


Figure 9. Analog Application Circuit

Table 1. Array Mechanical Specifications

		Units
Number of diodes	65,536	
Diode X, Y center-to-center spacing	40/1.57	µm/mils
Diode sensing area	963	μm^2
Fill factor	60	%
Package size (28-pin DIP)	0.8 x 1.4	$inch^2$

Table 2. Timing Specifications [1,2,3]

Sym	Parameter	Min	Typ	Max	Units
t_{XT}	$ø_X$ to $ø_{XST}$ delay	50			ns
t_{XA}	$ø_{XST}$ to $ø_A$ or $ø_B$ delay	100			ns
t_{AB}	$ø_A$ and $ø_B$ pulse width	0.4		6.4	µs
t_{LRG}	$ø_{LRG}$ pulse width	15			µs
t_{FRG}	$ø_{FRG}$ pulse width	14			µs
t_{FRD}	$ø_{FRD}$ pulse width	10			µs
t_{DLR}	$ø_{FRG}$ to $ø_{LRG}$ delay	1			µs
t_{FS}	$ø_{FRD}$ to $ø_{FRG}$ delay	4			µs
t_{YA}	$ø_{Y2}$ to $ø_A$ delay [4]	20			ns
t_S	Set-up time	50			ns
t_H	Hold time	50			ns

Notes:
1. 5 MHz clock rate operation
2. $t_r \sim t_f \sim 10 - 15$ ns
3. Clock amplitude ±13.5V
4. $t_{YA} = t_{YB}$

Table 3. Electrical Specifications

Pin	Sym	Function	Min	Typ	Max	Units
1	SUB	Substrate	-10	-6	-2	V DC
2	EOF	End of frame pulse [1]		7		V Ampl
3	$ø_B$	Multiplex clock [2]	9	13.5	15	V Ampl
4	$ø_A$	Multiplex clock [2]	9	13.5	15	V Ampl
5	$ø_{XSTO}$	Horizontal odd start	9	13.5	15	V Ampl
6	$ø_{LRG}$	Line reset gate	5	13.5	15	V Ampl
11	V_{DD}	Positive supply	7	8	15	V DC
12	$ø_{FRG}$	Frame reset gate	7	8	15	V Ampl
13	$ø_{X2}$	Horizontal even clock [2]	12	13.5	15	V Ampl
14	$ø_{X1}$	Horizontal odd clock [2]	12	13.5	15	V Ampl
15	$ø_{X3}$	Horizontal odd clock [2]	12	13.5	15	V Ampl
16	$ø_{X4}$	Horizontal even clock [2]	12	13.5	15	V Ampl
17	EOS	End of scan pulse [1]		7		V Ampl
18	$ø_{FRD}$	Frame reset drain	7	13.5	15	V Ampl
23	LRD	Line reset drain		0		V DC
24	$ø_{XSTE}$	Horizontal even start	9	13.5	15	V Ampl
25	V_{DD}	Positive supply	7	8	15	V DC
26	$ø_{YST}$	Vertical start clock [2]	8	13.5	15	V Ampl
27	$ø_{Y2}$	Vertical Y clock [2]	10	13.5	15	V Ampl
28	$ø_{Y1}$	Vertical Y clock [2]	10	13.5	15	V Ampl

Notes:
1. EOS and EOF were pulled up to +5V with a 2KΩ resistor
2. $0.5 \le (V_{CLK})^- - \text{Sub} \le 1$,
   $0 \le V_{DD} - (V_{CLK})^+ \le 1$,
   where $(V_{CLK})^-$ and $(V_{CLK})^+$ are the negative and positive rails of the clock.

Table 4. Terminal Capacitance with 10V Bias

Pin	Sym	Capacitance (pF)
2	EOF	5
3	ϕ_B	22
4	ϕ_A	21
5	ϕ_{XSTO}	9
6	ϕ_{LRG}	48
7	VID 1	5
8	VID 3	5
9	VID 5	5
10	VID 7	5
12	ϕ_{FRG}	27
13	ϕ_{X2}	30
14	ϕ_{X1}	30
15	ϕ_{X3}	30
16	ϕ_{X4}	30
17	EOS	4
18	ϕ_{FRD}	135
19	VID 8	5
20	VID 6	5
21	VID 4	5
22	VID 2	5
23	LRD	49
24	ϕ_{XSTE}	10
26	ϕ_{YST}	4
27	ϕ_{Y2}	28
28	ϕ_{Y1}	29

Table 5. Array Performance Characteristics

Sym	Parameter	Min	Typ	Max	Units
DR	Dynamic range (max signal/RMS noise) [1]		300:1		
E_{NE}	Noise equivalent exposure (p-p) [2]		.001		$\mu J/cm^2$
E_{Sat}	Saturation exposure [1]		0.37	0.45	$\mu J/cm^2$
Q_{Sat}	Saturation charge		0.8		pC
R	Responsivity [1]		5.78	6.68	$V/\mu J/cm^2$
V_{Dark}	Average dark signal [3]		2	4	%
f_S	Video sample rate [4]			40	MHz
PRNU	Photo response nonuniformity [1]		5	10	±%

Notes:

1 A 2870°K tungsten source and an HA-11 visible spectrum filter was used with the bandwidth of 370 nm to 1040 nm measured @ 50% V_{Sat}

2 At 570 nm

3 As a percentage of saturation; Integration time = 40 ms

4 Eight video outputs combined

5 All measurements taken with application circuits in Figures 8 and 9

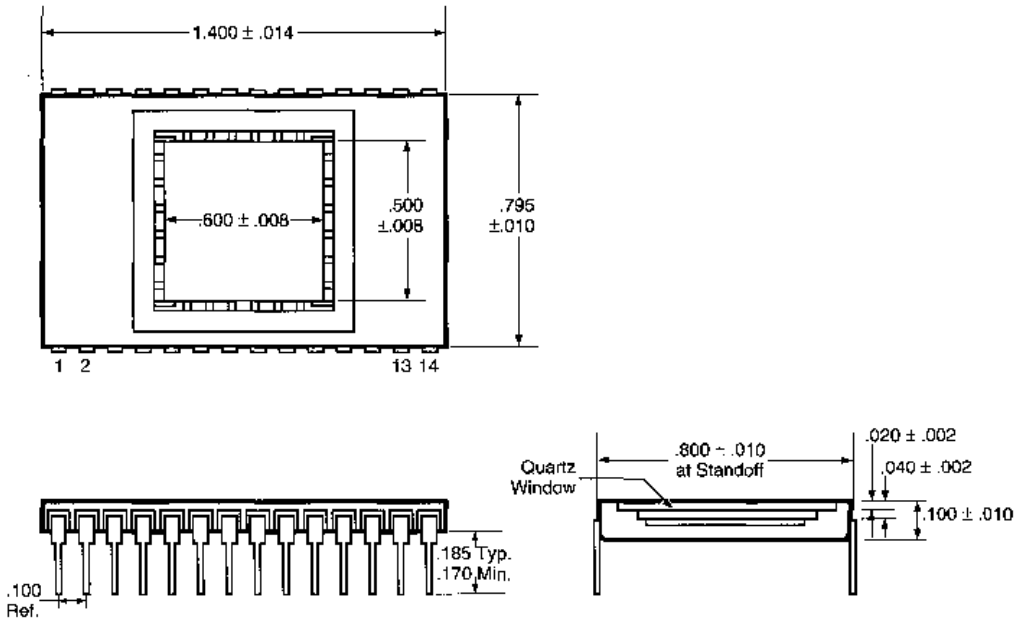


Figure 10. Package Dimensions

Ordering Information

Part Number	Description
RA2568NAQ-011	High frame rate 256 x 256 matrix array, quartz window
RA2568NAF-011	High frame rate 256 x 256 matrix array, fiber optic window
RC0504ANN-011	Evaluation board for RA2568NAQ-011 and RA2568NAF-011 arrays

055-0236
March 1992

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Introduction

The Reticon RA3812P is a two-dimensional self-scanned optical sensor array consisting of 456 silicon photodiodes in a 38 x 12 matrix. This device is a functional equivalent to low resolution vidicon camera tubes, but with the advantages of higher geometric accuracy, high sensitivity, small size, low voltage, low power, and all-solid-state ruggedness and reliability. The RA3812P is designed for applications in the areas of pattern recognition, character recognition, and guidance.

Key Features

- 456 light sensitive elements
- 4-mil element centers in both X and Y directions
- Frame storage–each diode integrates photo-current for the entire frame time
- Self-scanned in both X and Y directions by on-chip shift registers and multiplexers to provide a single serial video output
- Nonburning sensors
- Solid state reliability
- Low power dissipation
- 16-pin ceramic dual-inline package (0.3 inch x 0.8 inch) with scratch-resistant glass window

General Description

The RA3812P is housed in a 16-lead integrated circuit package (0.8 inch x 0.3 inch outline) with a ground and polished window (see Figure 8). The devices are fabricated on a monolithic silicon chip containing the photodiode matrix, as well as access switches and two integrated MOS shift registers for scanning in the X and Y directions. Each shift register is driven by a two-phase clock. The diode-to-diode sample rate is set by the X-register clock frequency, while the line rate is set by the Y-register clock frequency.

A basic circuit for driving the RA3812P is shown in Figure 3. This circuit supplies clock signals for both the X and Y registers and provides first-stage video amplification which has a video output similar to that shown in Figure 4.

Clock and Start Requirements

This array is self-starting, with no external start pulse required. The X-register should be driven by complementary square wave clock phases ϕ_1 and ϕ_2 as shown in Figure 4. These two phases can be generated from an input TTL clock run at the desired data rate which supplies the basic timing. The Y-register is driven by complementary square wave clocks run at the desired line rate. Keep crossovers on clock phases close to 50% to minimize odd/even fixed pattern noise.

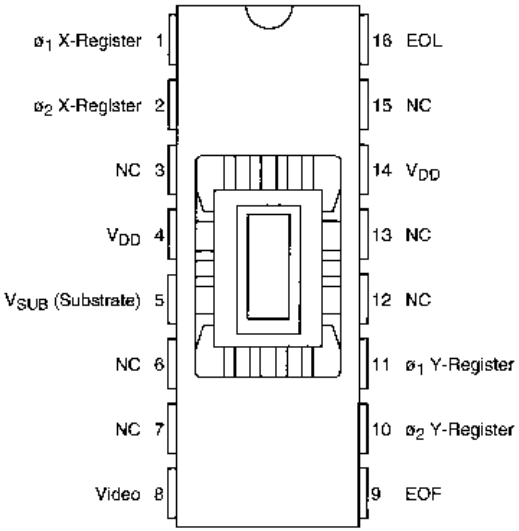


Figure 1. Pinout Configuration

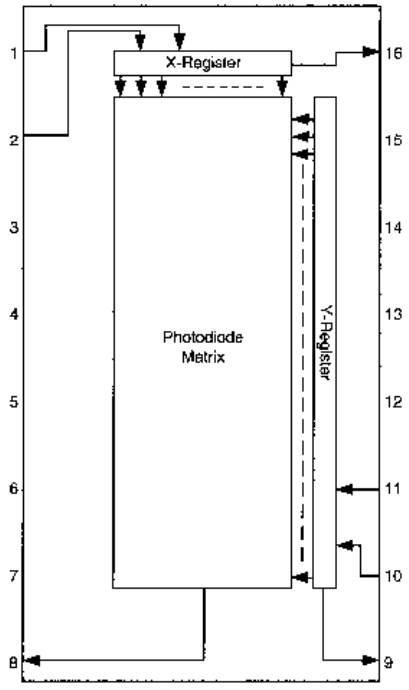


Figure 2. Block Diagram

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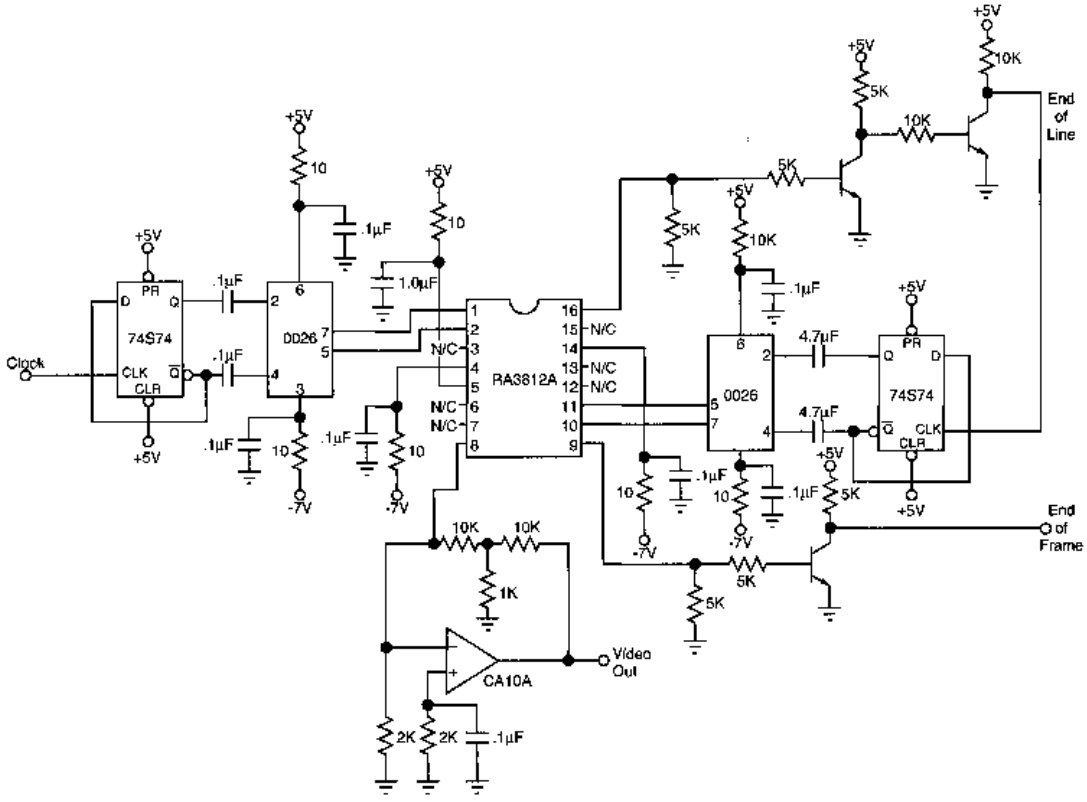


Figure 3. Basic Circuit for Operation of RA3812P Photodiode Array

Signal Extraction

The video output appears on pin 8 and consists of a train of current pulses each containing a charge equal to the photocurrent in the corresponding photodiode integrated over a frame time. To obtain good signal-to-noise or dynamic range, these pulses should be processed by a resettable integrator which may be followed by a sample-and-hold circuit. Switching transients will be superimposed on the current pulses, but the effect of these is essentially eliminated by the integrator circuit which integrates the current flow in each sample period including both the signal and the switching transients. Since the switching transients must integrate to zero, even low-level signals can be recovered.

End-of-Line and End-of-Frame

End-of-line pulses appear one sample period after the last element in each line (see Figure 4). The end-of-line output can be used to time the Y-register clocks so that the next line can be scanned. After the last line is scanned, a new bit is automatically loaded into the Y-register to start a new frame. If more sophisticated scanning is required, the Y-register should be timed by an externally-generated TTL pulse train with an appropriate repetition rate. For example, an interlace pattern where only the odd lines are scanned in one frame and only the even lines in the next frame can be produced by clocking the Y-register at twice the line rate and adding one step at the end of each frame.

An end-of-frame output (see Figure 5) appears on pin 9 during the last and first line of each frame. This output can be used for frame synchronization purposes.

Sensitivity and Spectral Response

The RA3812P operates in the frame storage mode. This means that each diode integrates photocurrent for an entire frame time and empties the integrated charge onto the video line when it is sampled once each frame time. The sensitivity of each diode is, therefore, over 456 times the sensitivity of an individual diode of equal size operated in the photoconductive mode. The output of each diode (below saturation) is proportional to the light intensity times the frame time and can be specified in terms of charge out per unit of exposure. A plot of output versus exposure is shown in Figure 6. Spectral response is typical of high-quality diffused silicon photodiodes, covering the range from the near UV to the near IR with peak response at 750 nm. Typical spectral response is shown in Figure 7.

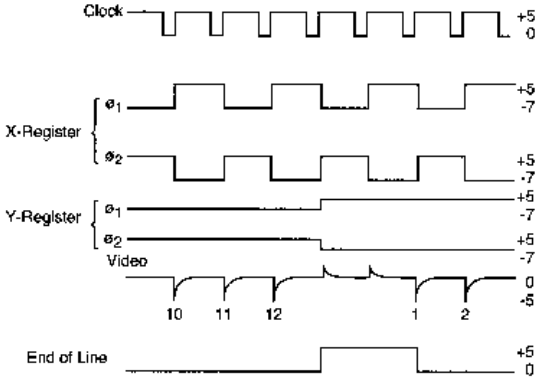


Figure 4. Timing Diagram

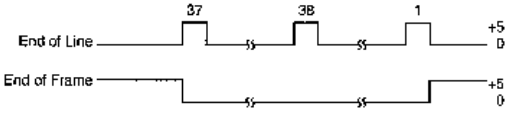


Figure 5. Timing Diagram for End-of-Frame Output

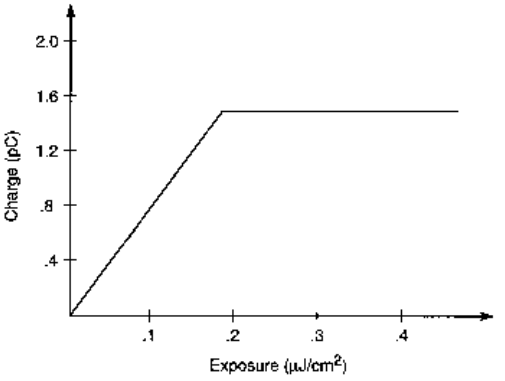


Figure 6. Charge Output per Cell Versus Exposure where Exposure Equals Light Intensity Times Frame Time

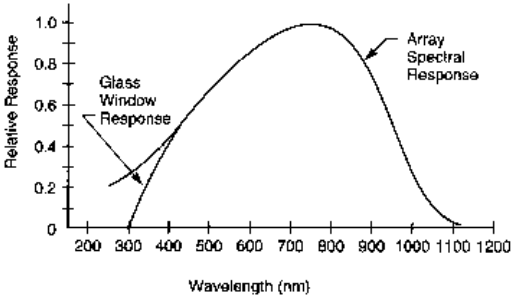


Figure 7. Relative Spectral Response as a Function of Wavelength

Table 1. Electrical Characteristics (25°C) (Voltages with respect to substrate (pin 5); substrate typically held at +5V)

	Min	Typ	Max	Units
Video output line bias		-5	-8	V
Supply voltage V_{DD}	-11	-12	-13	V
Clock pulse amplitude	-11	-12	-13	V
End of line/frame output resistance		5		KΩ
End of line output pulse width [1]		2/f		s
Video line capacitance (at -5V with respect to substrate)		40		pF
Diode sample rate (f)	10^4		4×10^6	Hz
Frame rate [2]	19		7500	fps
Power dissipation (DC)		10		mW

Notes:
1. f = diode sample rate
2. fps = frames per second

Table 2. Electro-Optical Characteristics (25°C)

	Typ	Max	Units
Photodiode sensitivity [1]	9		$pC/\mu J/cm^2$
Uniformity of sensitivity [1,2]	±8	±12	%
Saturation exposure [1]	.18		$\mu J/cm^2$
Saturation charge (with typical input and bias voltages)	1.6		pC

Notes:
1. 2870°K tungsten source
2. Neglects first and last elements of each line

Table 3. Mechanical Characteristics

	Typ	Units
Number of diodes	456	
Number of rows	12	
Number of columns	38	
Spacing (row and column)	4	mils
Diode sensing area	8	$mils^2$
Package size (16-pin DIP)	.31 x .8	inch

Absolute Maximum Rating

	Min	Max	Units
Voltage with respect to substrate	0	-20	V
Storage temperature	-55	+85	°C
Temperature under bias	-55	+85	°C

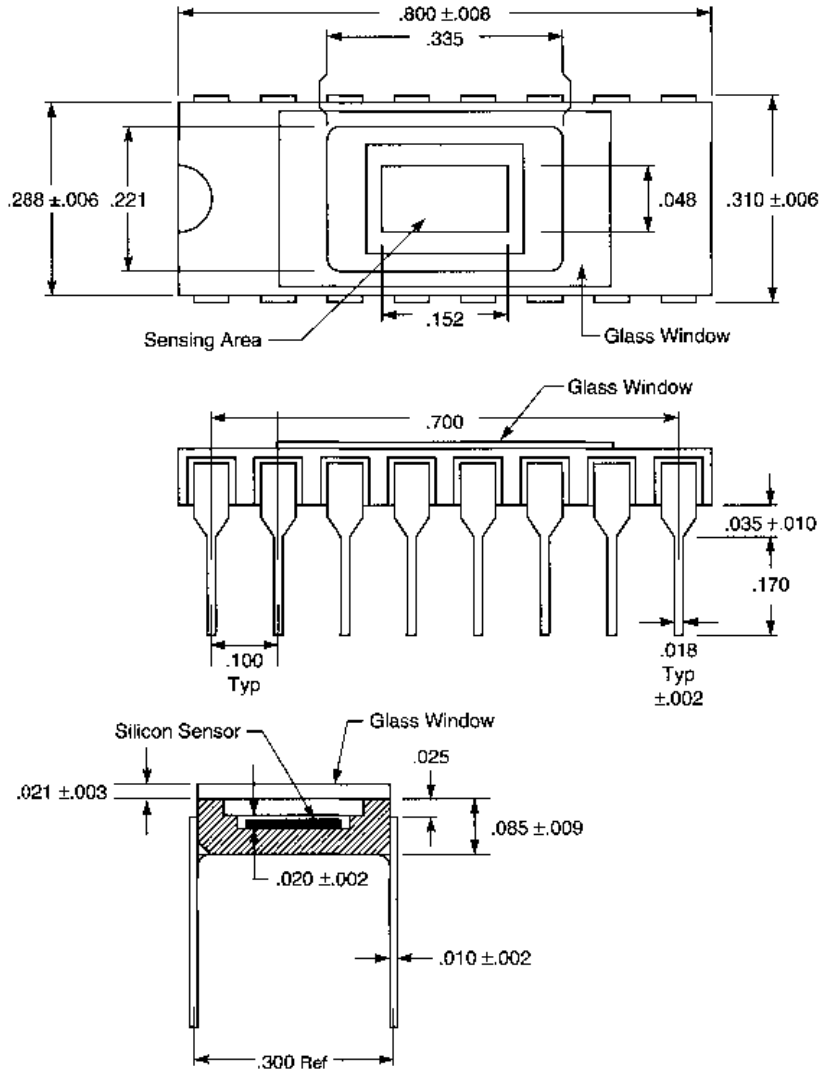


Figure 8. Package Dimensions

Ordering Information

Part Number
RA3812PAG-011

055-0221
January 1992

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RA6464N
Solid State High Speed Image Sensor Array

Description

The Reticon RA6464N is a very-high-speed PMOS 64 x 64 pixel imaging array. It has 32 parallel outputs that allow extremely high read out rates. Frame rates to over 24,000 frames per second make it ideal for high speed motion analysis and other applications formerly restricted to high-speed film cameras. The 'center-out half-plane scanning' sequence makes it well suited for high-speed tracking and guidance applications since the center portion of the array is read out first.

The RA6464N is furnished in a rugged 69-pin ceramic pin grid array (PGA) package. Top and bottom views of the package are shown in Figure 1. The pin assignments are shown in Figure 2. The unique 'center-out' scan sequence is shown in Figure 3. Package dimensions and mechanical information are illustrated in Figure 10.

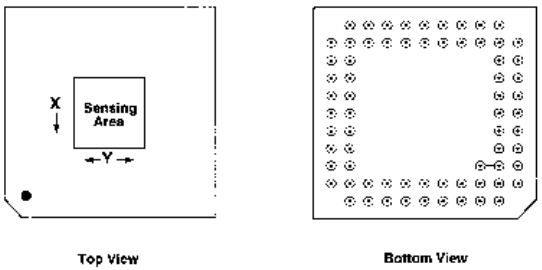


Figure 1. Sensing Area and Pinout Configuration

Key Features

- Center-out half-plane scanning
- Very high speed operation (>24,000 FPS)
- High sensitivity ($E_{SAT} \approx 50$ nJ/cm^2)
- Large active pixel area
- 32 parallel video outputs

Device Operation

An input/output diagram is shown in Figure 4. A simplified diagram for the device is shown in Figure 5. Notice that the photo-sensitive area is divided into two half-planes. These half-planes output their contents simultaneously, each through their dedicated 16 parallel outputs.

The device has a dynamic 'center-out' shift register that is loaded in the middle and shifts in both directions towards the ends. A "1" is loaded into the middle of the register. As the register is clocked, any stage containing a "1" connects an entire row of pixels to their respective video lines. Then, the ϕ_M clocks connect those video lines to the output circuitry.

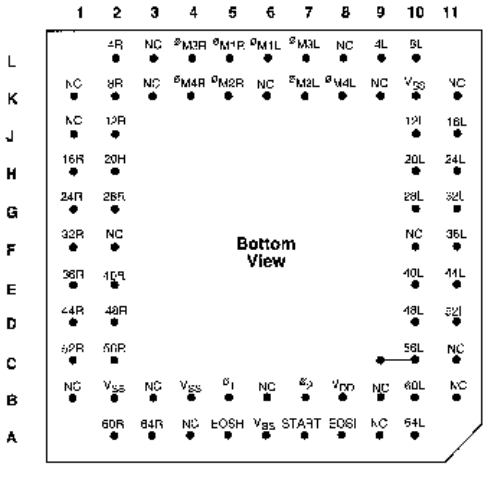


Figure 2. Pin Assignment

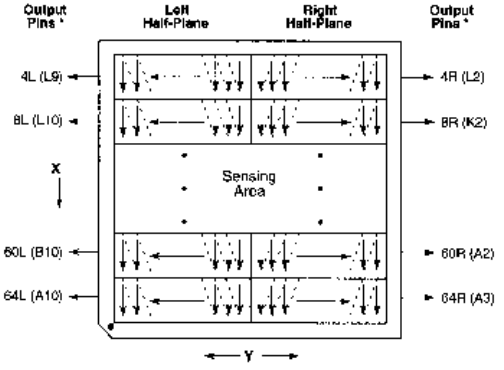
Since there is one output for each set of four columns in each half-plane, it only takes four cycles of the ϕ_M clocks to output the entire row. Each half-plane is doing this in parallel, so two rows are output together.

The readout continues until 64 rows have been output. This takes only 16 cycles of the y-register (vertical) clocks. The integration time (the total light-gathering time) is the time between start pulses.

Notation of Outputs: Output nR (or nL) refers to the output pin that outputs information for columns n, n-1, n-2, and n-3 on the Right (or Left) side of the array. Examples: output 4R outputs information for columns 4, 3, 2, and 1 on the right side of the array; output 36L outputs information for columns 36, 35, 34, and 33 on the left side of the array.

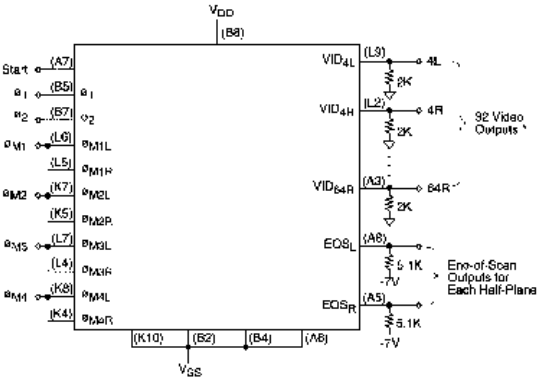
Location (pq) refers to the pin at coordinates p and q as defined by the grid in Figure 2. Examples: (L2) refers to the pin at location L2 in Figure 2 (which is output pin 4R). (B7) refers to the pin at location B7 in Figure 2 (which is clock input ϕ_2). Therefore: 60L (B10) refers to the output for columns 60, 59, 58, and 57 on the left side of the array, located at position B10.

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* See text for explanation of output pin notation.

Figure 3. Sensing Area Scanning Sequence



* See text for explanation of output pin notation.

Figure 4. Input/Output Diagram

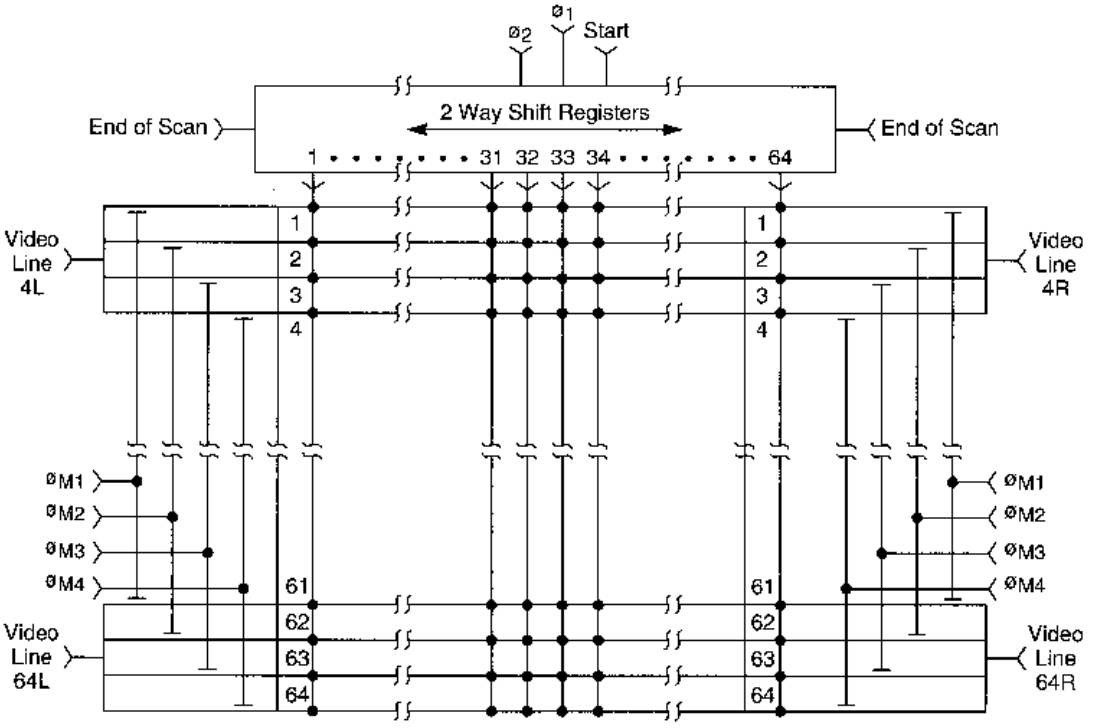


Figure 5. Simplified Diagram

Timing

The y-register clock selects two rows (one in each half-plane) with each clock transition. Then, the x-multiplexer clocks are each pulsed to sequentially connect each of four diodes to the same output. The y-register clocks change state again, and the cycle continues until the entire array has been read out. It is important to note that the y-register shifts on every transition (change of state) of $ø_1$ and $ø_2$, not just every full clock period.

The sequence is started by loading a start pulse into the y-register. The start pulse is a negative-going pulse. The start pulse must fall to its negative value at least 50 ns before the rising edge of $ø_2$ and must stay negative for at least 20 ns after $ø_2$ has reached its positive state. As Figure 6a shows, the start pulse can occur early and last well beyond the rising edge of $ø_2$. The first two rows are accessed when the rising edge of $ø_2$ loads the start pulse. The rise and fall times of the start pulse are not critical.

$ø_1$ and $ø_2$ clocks are usually complementary square waves. The two clocks can both be positive at the same time, but should never be negative at the same time. Simultaneous negative clocks cause unpredictable behavior. Clock transients are minimized if the two clocks are exact complements and have 50% clock crossovers. Rising and falling edges are more critical than those of the start pulse.

The multiplexing clocks directly connect the photodiodes and their video lines to the outside circuitry. The negative-going pulses must not overlap or pixel signals will become mixed. The FET switch (multiplexer clocks) rise and fall times are not critical.

The sequence given in the timing diagram is the typical sequence to output the pixels. However, the multiplexer clocks can be pulsed in any desired order if the application requires a different scanning sequence. The y-register may only be operated as described above.

Opto-Electronic Performance

Figure 7 shows the device spectral response with a quartz window and with a fiber optic window. The specification table values were determined using a 2870°K light source with a Fish-Schurman HA-11 infrared-absorbing filter.

The pixels are located on 100 µm centers in both the x and y axes. Therefore, the area per pixel is 10,000 $µm^2$. The active area (the area that can sense light) is 8768 $µm^2$ which corresponds to a fill factor of about 88%.

Saturation charge is 2 pC, or about 12.5 million electrons. The rms read noise is about 1100 noise electrons.

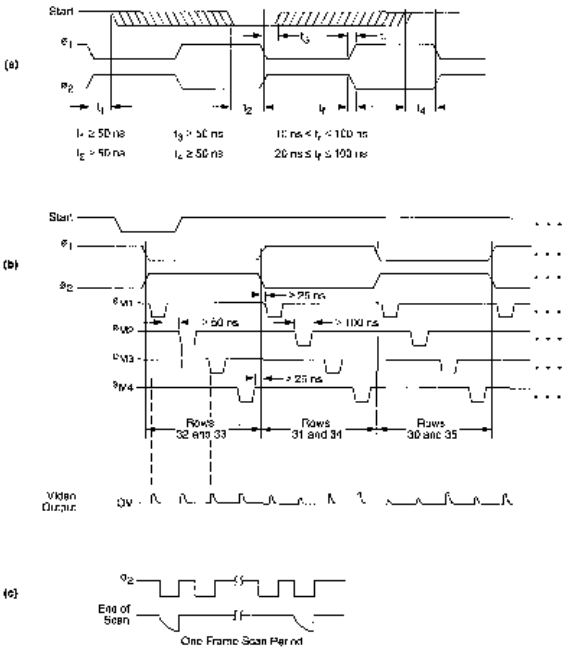


Figure 6. Timing Diagram

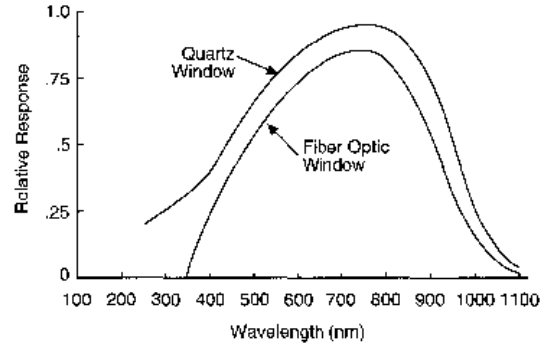


Figure 7. Typical Spectral Response

Signal Extraction

The signal is simply the voltage or current pulse that occurs when each photodiode is connected to the output line (see Figure 6). Only a simple resistor load is needed to read the voltage pulse (see Figure 8a). A current integrator (Figure 8b) can also be used, thus averaging out the effects of clock transients, etc. This integrator's output must be sampled-and-held and then its capacitor must be reset after each pixel is read out.

The RA6464N can also be used as an array of fewer – but bigger – pixels. The user need merely sum up charge from adjacent pixels before resetting the external charge integrator. Therefore, the RA6464N can also be used as a high-speed 32 x 32, 16 x 16, etc. If the application does not require square pixels, the user can configure the readout for 64 x 32, 16 x 32, 64 x 1, and so on.

Example Circuits

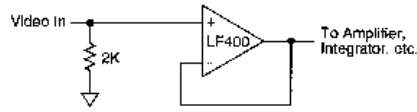
A circuit that provides all the necessary timing signals to operate the RA6464N is shown in Figure 9.

The applied clock is a TTL level square wave of up to 20 MHz. This clock goes into a 9316 IC configured as a divide-by-three counter. It's output is fed into another 9316 which is configured as a divide-by-four counter. This counter outputs to a D flip-flop that toggles and generates the two y-register clock phases. The DS0026 drivers translate the TTL level signals to the proper voltage levels.

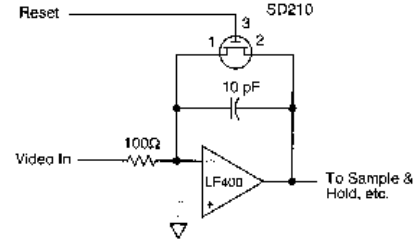
The outputs of the counters also feed the shift and clock inputs of the 74LS164 shift register. The shifted pulse from this register becomes the four multiplexer clock phases.

The last section generates the start pulse. The switches are connected to the 9316 preset inputs. The switches set the number of counts per frame and thus the integration time.

Appropriate output circuits are shown in Figure 8.



(A) Simple Voltage Buffer with Recharge Path



(B) Charge Integrator with Reset Switch

Figure 8. Video Output Circuits

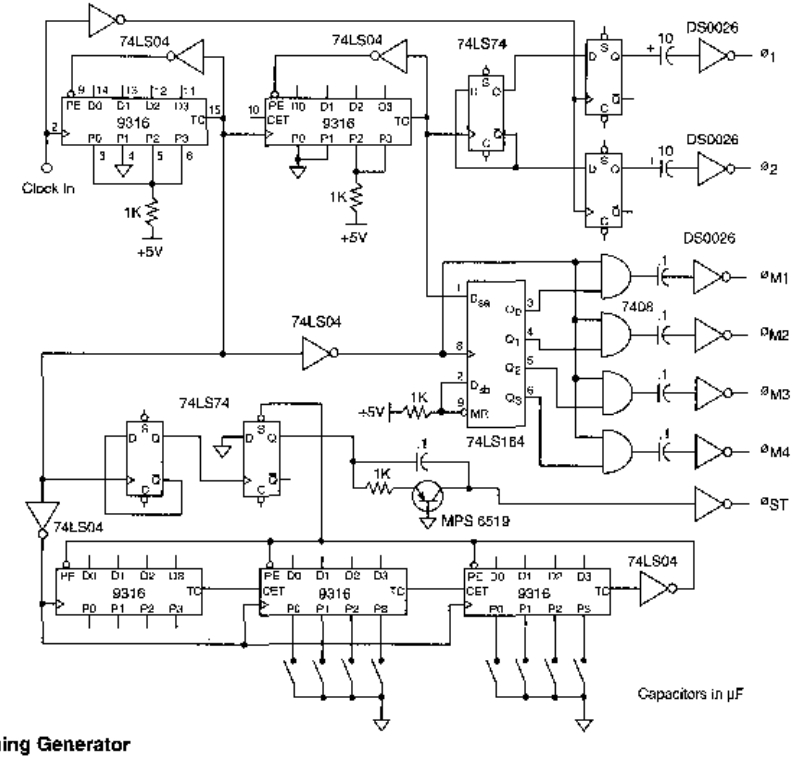


Figure 9. Timing Generator

Table 1. Input Requirements

Parameter	Sym	Comments	Min	Typ	Max	Units
Negative supply	V_{DD}		-9	-7	-5	V
Positive supply	V_{SS}		+3	+5	+7	V
Shift register clock phases [1]	ϕ_1, ϕ_2	High clock level	+4.5	+5	+5	V
		Low clock level	-7	-7	-6	V
		Rise & fall times	10	20	100	ns
		Clock line capacitance		15		pF
		Frequency	4		775	kHz
Multiplex, clock phases [1]	ϕ_{M1}, ϕ_{M2}, ϕ_{M3}, ϕ_{M4}	High clock level	+4.5	+5	+5	V
		Low clock level	-7	-7	-6	V
		Rise & fall times	10	20	100	ns
		Clock line capacitance		10		pF

Note:
[1] All 2-phase and 4-phase clocks should use the same high and low clock levels.

Table 2. Electro-Optical Characteristics

Parameter	Sym	Comments	Min	Typ	Max	Units
Center-to-center spacing		Both axes		100		µm
Active area				8768		μm^2
Fill factor				88		%
Sensitivity				4.0 x 10^{-5}		$C/J/cm^2$
Photo response nonuniformity [4,5]	PRNU	@ 600 nm @ 5% Q_{Sat}		⊥8	⊥12	%
Saturation charge	Q_{Sat}			2.0		pC
Saturation exposure	E_{Sat}	@ 600 nm		50		nJ/cm^2
RMS noise electrons		Readout noise		1100		e -
Noise equivalent exposure [1]	E_{NE}			.50		nJ/cm^2
Average dark current				1	2	pA
Dynamic range [2,4]	DR	$DR = Q_{Sat}/FPN_{P-P}$		70:1		
Power dissipation [3]	P			10		mW
Maximum video output		R_{Load} = 2 KΩ				
		Pixel rate = 50 kHz		280		mV
		Pixel rate = 500 kHz		280		mV
		Pixel rate = 5.2 MHz		160		mV
		Pixel rate = 6.4 MHz		130		mV

Notes:
[1] Noise equivalent exposure is determined by the external interface circuit components and layout. With an amplifier input noise ≤ 1000 electrons per pixel, and with reasonable circuit layout, 8 X 10^{-3} nJ/cm^2 or less is possible.
[2] FPN_{P-P} = fixed pattern noise (peak-to-peak)
[3] The power dissipation increases with clock frequency. For a pixel output frequency of less than 2 MHz, the power dissipation is less than 10 mW.
[4] First and last rows, first and last columns are not included.
[5] At 50% Q_{Sat} with HA-11 filter:
+% NU = $[(V_{Max} - V_{Avg})/V_{Avg}]$ x 100%
-% NU = $[(V_{Avg} - V_{Min})/V_{Avg}]$ x 100%

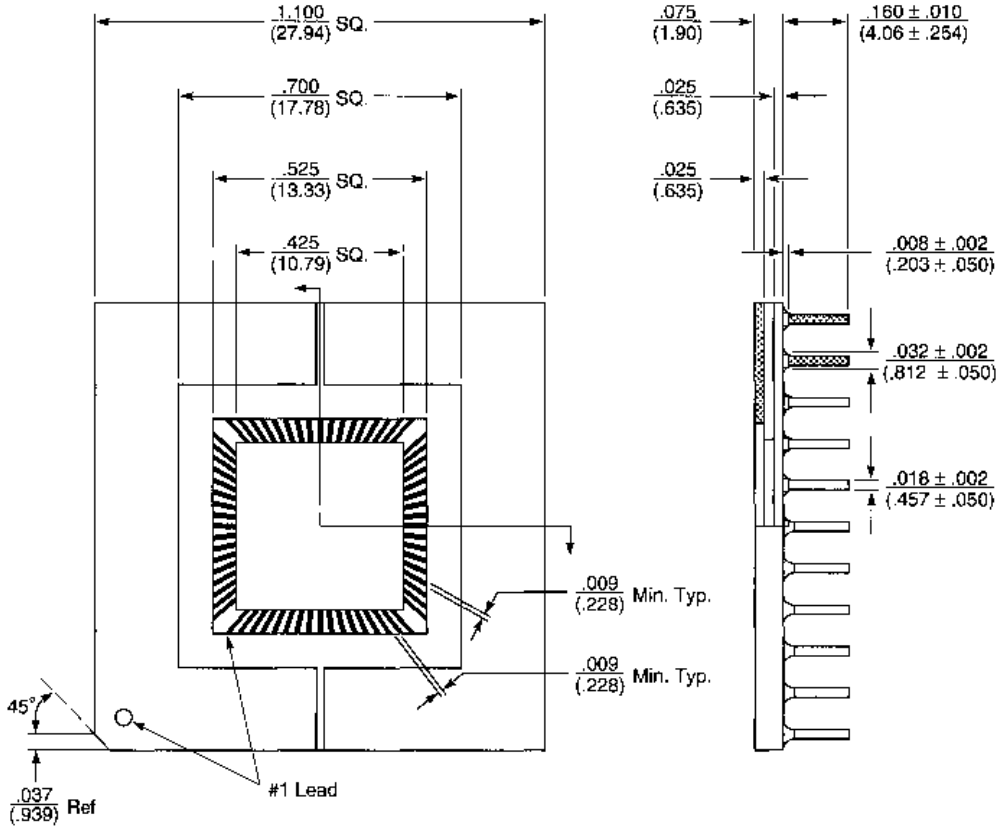


Figure 10. Package Dimensions

Ordering Information

Part No.	Description
RA6464NAQ-011	High-speed 64 x 64 array, with quartz window
RA6464NAF-011	High-speed 64 x 64 array, with fiber optic window

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General Description

The RA0512J is a full frame CCD sensor designed specifically for use in astronomy, spectroscopy and related scientific imaging applications. Its combination of very low noise and low dark current make it ideal for low light level, high dynamic range, and high resolution applications.

The imager is structured in a serial-parallel-serial configuration so charge packets (imaging data) in the vertical (parallel) registers can be shifted either up or down to two identical horizontal (serial) shift registers. One is at the top and another is at the bottom of the array. Three-phase clocks are needed to drive both vertical and horizontal shift registers.

The array is available in a 40-pin ceramic package as shown in Figure 1. Package dimensions are shown in Figure 7. It is available with a quartz window or unwindowed. The device is indifferent to its orientation in a circuit due to the symmetry of the pinout (see Table 1 for complete pinout description).

NOTE: The RA0512J does not contain gate protection circuitry to protect the input and output pins from static damage. Special handling precautions should be used to avoid static damage.

Features

- 262,144 picture elements (pixels) in a 512 x 512 configuration
- 27 µm square pixels
- 3-Phase buried channel process
- On-chip output amplifier for low noise and high speed readout
- High dynamic range: over 98 dB at -110°C (183°K)
- Serial-parallel-serial configuration for selectable bidirectional readout
- Usable spectral response from 450 nm to 1050 nm

MPP Operation

A major source of dark current in devices such as this originates in surface states at the Si-SiO_2 interface. A unique design and process enables the RA0512J to be run in the "Multi-Pinned Phase" or MPP mode of operation. This helps eliminate dark current generation in the interface surface states. By holding the vertical clocks at negative potential during integration and horizontal signal readout, the surface of the sensing area is inverted. As a result, the surface will not be depleted and surface states will not generate dark current. Dark current densities of less than 50 pa/cm^2 have been achieved using the MPP mode of operation, resulting in integration times of more than 30 seconds at room temperature.

Functional Description

Imaging Area

The imaging area is an array of 512 columns (vertical CCD shift registers) which are isolated from each other by 5 µm channel-stop regions. Each column has 512 picture elements. The pixel size is 27 µm x 27 µm. The total imaging area is 13.8 mm x 13.8 mm. Typical spectral response as a function of wavelength is shown in Figure 2.

In the vertical direction, each pixel corresponds to one stage (three electrodes) of the shift register. The three-electrode groups are driven by three-phase clocks ($ø_{1C}$ - $ø_{3C}$) brought in from both edges of the array to improve clock electrode response time.

Charge packets (imaging data) in the vertical registers can be shifted either up or down to the top or bottom horizontal registers by interchanging two of the three phases ($ø_{1C}$ and $ø_{2C}$). See Figure 3 for functional diagram.

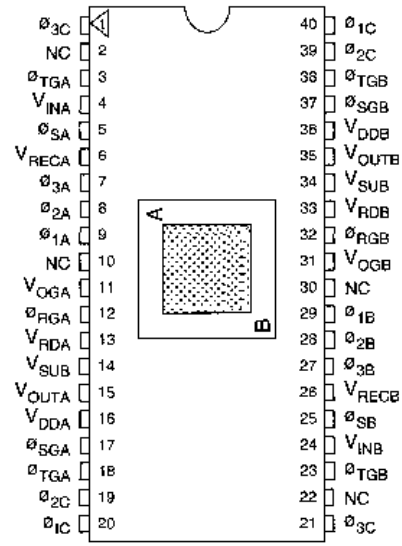


Figure 1. Pinout Configuration

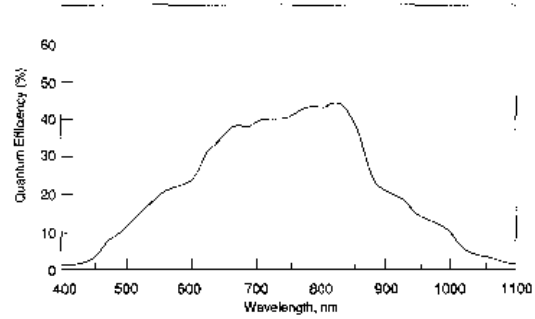


Figure 2. Typical Spectral Response

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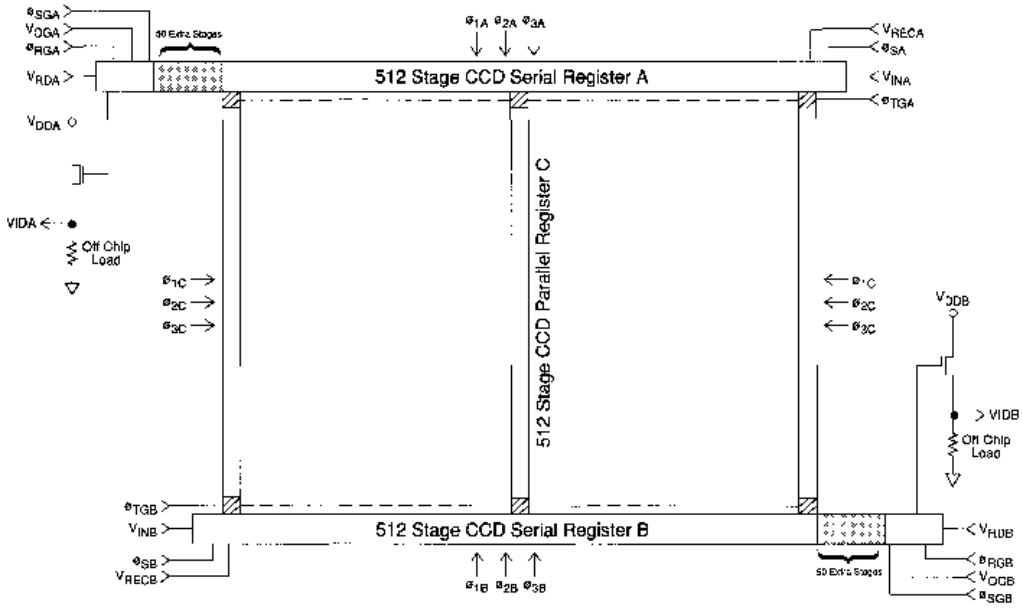


Figure 3. Functional Diagram

A transfer gate ($ø_{TG}$) is provided at the interface of the vertical and horizontal registers for controlling charge flow. Charge flow is from $ø_{3C}$ gate of the vertical shift register into $ø_2$ and $ø_3$ gates of the horizontal shift register. The control function is performed by pulsing the transfer gate either high or low to permit or prevent the charge flow from the vertical register into the horizontal register for readout.

When the potential of the vertical register electrodes is held steady, a potential well is created beneath the storage gates ($ø_{1C}$ and $ø_{2C}$). When an image impinges on the sensing area, an electrical signal of the scene will be collected in the potential well during this integration period.

Following the integration interval, the collected charge (signal) in the array can be read out as a full-frame image by transferring the charge, one or more rows at a time, into the horizontal shift register. From there, charge can be shifted serially to the output amplifier.

A mechanical shutter is needed to shield the array from incident light during the read out process. A strobe illumination could be used to simulate the shuttered mode of operation. Image smearing degrades the performance, particularly at low data rates, unless such shuttering is provided.

Horizontal Registers

There are two identical horizontal shift registers which are driven by three-phase clocks($ø_{1A}$-$ø_{3A}$, $ø_{1B}$-$ø_{3B}$), one at the top and one at the bottom of the imaging area. Each shift register has 512 stages plus an extension of 50 stages. As a result, amplifier power is dissipated more efficiently and dark current generated by localized heating is minimized.

Summing Mode

At the end of each serial register, there is an output summing well which can be clocked to allow multiple-pixel summation of the scene. This summing well is located after the 50th extra stage of the horizontal registers and prior to the DC biased gate (V_{OG}) as shown in Figure 5. The summing gate (SG) can be clocked with one of the serial clock phases or with its own clock generator (see Figure 6 for summing gate timing). For example, two parallel lines of charge are additively transferred into the serial register, then the summing gate is pulsed low after the charge from two serial pixels has been transferred into the summing well. Thus, the resulting signal represents the sum of charges in four (2 x 2) contiguous pixels from the imaging section. It effectively reduces the 512 x 512 device to a 256 x 256 array and increases the pixel size by 4 times. Other variations of this technique can be useful for low-light level situations, i.e., scenes with low contrast, or a low signal-to-noise ratio. There is, of course, a loss in resolution which accompanies the gain in effective pixel size.

Output Amplifier

There is an on-chip amplifier which is located at the end of each extended serial shift register. The amplifier is a single-stage buried-channel transistor (Figure 5) designed to operate in the source-follower configuration with an off-chip load resistor (1KΩ - 20KΩ). It has a bandwidth of approximately 5 MHz with a 10 pF load.

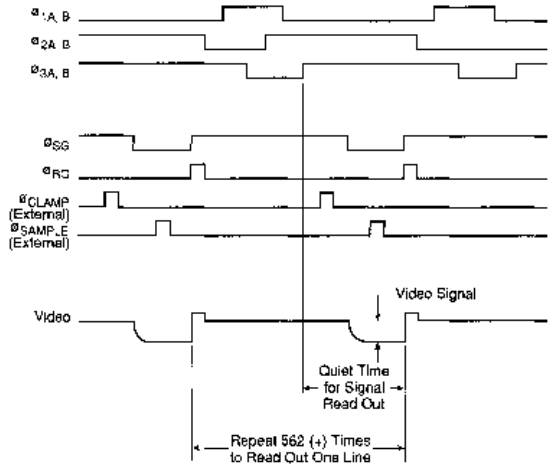


Figure 4A. Horizontal CCD Shift Register Timing Low Noise Operation

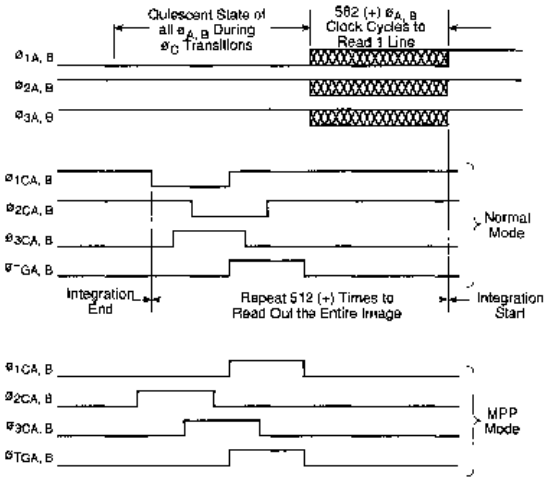


Figure 4B. Vertical CCD Shift Register Timing Diagram

Timing Requirements

The timing recommended to run the RA0512J imager in the low speed and low noise mode of operation is shown in Figures 4A and 4B. Other types of three-phase clocks can also be used to drive both the vertical and horizontal registers. For example, 50% duty cycle, three-phase clocks can be used to drive the horizontal register for high-speed operation. However, the large full well capacity and low noise floor will be sacrificed.

Figure 4A shows the timing of the horizontal three-phase clocks, summing well clock, reset clock, and external clamping and sampling clocks. To achieve high charge transfer efficiency and high full well capacity, serial clocks must overlap by more than 1 µs. In addition, the rise and fall times of the three-phase clocks may be more than 300 ns to prevent possible injection of spurious charge into the CCD channel. After the three-phase clock transitions, the clocks are held steady to provide a quiet period for signal readout. During this quiet period, the output amplifier is clamped and the signal charge in the summing well is transferred into the output sensing node. The output signal is then sampled and the sensing node is reset.

This timing is repeated 562 (or more) times to allow the readout of one complete line of the image. The video signal from one pixel is also shown in Figure 4A.

Figure 4B shows the timing requirements for the vertical register. Overlapping of the vertical clocks are normally longer than 5 µs. Rise and fall times of all clocks may be 300 ns or longer. All clock transitions should occur when the horizontal clocks are held steady.

Timing for MPP and normal mode is shown. The difference between the two modes is that during an integration, all clocks must be held low for MPP mode. The clocks should repeat 562 times (or more) to read out the entire image.

Array Cooling

Both the dark current and noise performance of the array can be improved by cooling. The dark current will be reduced 50% for every 7°C reduction in array temperature. The noise floor of the output amplifier is proportional to $\sqrt{kTC}$ where k is Boltzmann's constant, T is the array temperature in degrees Kelvin and C is the output node capacitance of approximately .17 pF. Cooling can be achieved via a thermo-electric, Joule-Thomson cooler, or liquid nitrogen dewar.

UV Coating

The RA0512JAU CCD is available with a special UV enhancement coating which extends the spectral response range to 120 nm. A thin layer of lumogen is deposited directly on the frontside illuminated arrays and will emit at 550 nm when excited by 120 nm - 450 nm light. The coating is transparent in the visible and near-infrared spectrums. UV coated devices are designed by the -3XX part number.

Backside Illumination - Thinning

The RA0512JAU is also available in a thinned version which greatly improves the quantum efficiency in the visible and near-infrared while also giving excellent performance in the 200 - 400 nm UV range. The imaging area of the device is thinned to 10 µ using a chemical etch procedure. Then a flash-oxide treatment is applied to the thinned area. To activate the flash oxide it is necessary to UV flood the array (expose the array to a UV light source for 5 - 10 minutes or longer, using a mercury lamp (eprom eraser)) to charge the device. Once the array is returned to room temperature, the charge will decrease requiring another charging. Thinned devices have pinouts which are mirror images of the frontside devices and are designated by the 2XX part number.

Specifications

Recommended operating conditions for the RA0512J are shown in Table 2. Typical device specifications are shown in Table 3, and Table 4 gives typical capacitance values.

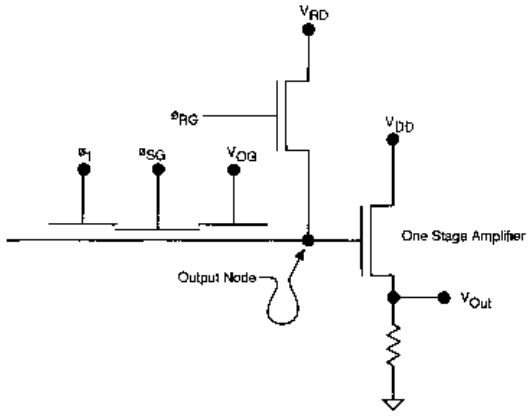


Figure 5. Output Structure

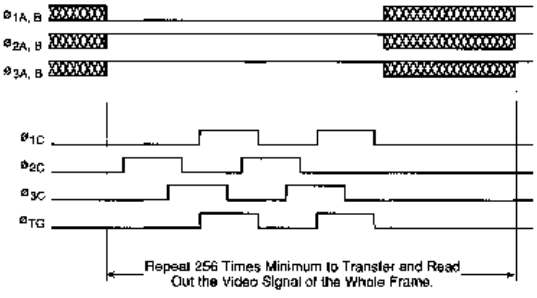


Figure 6A. Timing Comparison Between $\phi_{A, B}$ and ϕ_C

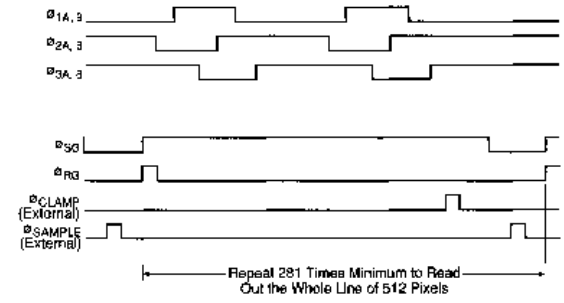


Figure 6B. Timing Comparison between $\phi_{A, B}$ and ϕ_{SG}

Table 1. Pin Descriptions

Pin No.	Sym	Function	Register
1	ϕ_{3C}	Parallel phase 3 clock	C
2	N/C		
3	ϕ_{TGA}	Parallel transfer gate to reg. A	A
4	VINA	Input diode	A
5	ϕ_{SA}	Input sample gate	A
6	VRECA	Input receiving gate	A
7	ϕ_{3A}	Serial phase 3 clock	A
8	ϕ_{2A}	Serial phase 2 clock	A
9	ϕ_{1A}	Serial phase 1 clock	A
10	N/C		
11	V_{OGA}	Output bias gate	A
12	ϕ_{RGA}	Reset gate	A
13	V_{RDA}	Reset drain	A
14	V_{SUB}	Substrate bias	
15	V_{OUTA}	Video amplifier output	A
16	V_{DDA}	Drain supply of amplifier	A
17	SGA	Summing well gate	A
18	ϕ_{TGA}	Parallel transfer gate to reg. A	C
19	ϕ_{2C}	Parallel phase 2 clock	C
20	ϕ_{1C}	Parallel phase 1 clock	C
21	ϕ_{3C}	Parallel phase 3 clock	C
22	N/C		
23	ϕ_{TGB}	Parallel transfer gate to reg. B	B
24	VINB	Input diode	B
25	ϕ_{SB}	Input sample gate	B
26	VRECB	Input receiving gate	B
27	ϕ_{3B}	Serial phase 3 clock	B
28	ϕ_{2B}	Serial phase 2 clock	B
29	ϕ_{1B}	Serial phase 1 clock	B
30	N/C		
31	VOGB	Output bias gate	B
32	ϕ_{RGB}	Reset gate	B
33	V_{RDB}	Reset drain	B
34	V_{SUB}	Substrate bias	
35	V_{OUTB}	Video amplifier output	B
36	V_{DDB}	Drain supply of amplifier	B
37	SGB	Summing well gate	B
38	ϕ_{TGB}	Parallel transfer gate to reg. B	C
39	ϕ_{2C}	Parallel phase 2 clock	C
40	ϕ_{1C}	Parallel phase 1 clock	C

Note: Pins 1, 19, 20 are internally connected to pins 21, 39, 40 respectively. This allows the vertical clocks to be driven from both sides of the sensor to improve clock response time.

Table 2. Recommended Operating Conditions

Definition		Symbol	Parameter						Units
			Normal Mode			MPP Mode			
			Low	Typ	High	Low	Typ	High	
DC supply		V_{DD}	20	21	22	20	21	25	V DC
Output gate bias		V_{OG}	3	6	8	1	2	5	V DC
Reset drain bias		V_{RD}	12	13	14	12	13	14	V DC
Substrate bias		V_{SUB}, V_{SS}	0	-0.5	-5.0	0	-1	-5.0	V DC
Serial clocks	High	$ø_A$, $ø_B$		12			10		V
	Low			0			-2		V
Vertical clocks	High	$ø_{1C}$, $ø_{2C}$, $ø_{3C}$		12			2.0		V
	Low			0			-10		V
Transfer gate clock	High	$ø_{TG}$		12			2		V
	Low			0			-10		V
Reset gate clock	High	$ø_{RG}$		15			12		V
	Low			0		0	0	1	V
Summing gate clock	High	$ø_{SG}$		12			5		V
	Low			0			-5		V

Table 3. Typical Device Specifications

Test Conditions: Temperature - 230°K (-43°C); Pixel Rate - 50 kHz; Tint - 10 sec

Parameter	Sym	Min	Typ	Max	Units
Format			512 x 512 full frame		
Pixel size			27 µm x 27 µm		
Imaging area			13.8 mm x 13.8 mm		
Dynamic range [1]	DR				
Normal mode			83,333:1 (98 dB)		
MPP mode			58,333:1 (95 dB)		
Full well charge	Q_{sat}				
Normal mode			500		K electrons
MPP mode			350		K electrons
Saturation voltage [2]	V_{sat}				
Normal mode			350		mV
MPP mode			220		mV
Dark current [3,6,7]	DL				
Normal mode			1.0		na/cm^2
MPP mode			50		pa/cm^2
Saturation exposure	E_{sat}		5.7		$µJ/cm^2$
Responsivity	R		20		$V/µJ/cm^2$
Photo-response nonuniformity [4]	PRNU		5	10	±%
Dark signal nonuniformity [3]	DSNU		4		mV
Charge transfer efficiency	CTE		.99999		
Output amplifier gain			.69		µV/electron
Read noise [5]			6		electrons

Notes:
1. Full well/read noise
2. R_{Load} = 5.1K
3. Pixels greater than 30% of the local average of 10 pixels on a line are considered defects and are ignored.
4. Pixels greater or less than 10% of the local average of 10 pixels on a line are considered defects and are ignored.
5. Measured at -110°C.
6. Typical dark current for thinned version is 2 times higher than frontside illuminated device.
7. At 23°C.

Table 4. Typical Capacitance Values

Parameter	Sym	Pin No.	Typ Value	Units
Parallel clocks	ϕ_{1C}	20, 40	2100	pF
	ϕ_{2C}	19, 39	1550	pF
	ϕ_{3C}	1, 21	2150	pF
Serial clocks	$\phi_{1A/B}$	9, 29	135	pF
	$\phi_{2A/B}$	8, 28	90	pF
	$\phi_{3A/B}$	7, 27	180	pF
Transfer clocks	$\phi_{TGA/B}$	3, 18, 23, 38	71	pF
Video output	$V_{OutA/B}$	15, 35	10	pF
Reset gate clock	$\phi_{RGA,B}$	12, 32	21	pF
Summing gate clock	$\phi_{SGA,B}$	17, 37	9	pF

Absolute Maximum Ratings

Storage temperature: -150°C to +50°C

Voltages: measured with respect to substrate pins 14 & 34

Pin 1, 3, 7, 8, 9, 17, 18, 19, 20, 21, 23, 27, 28, 29, 37, 38, 39, 40	-15V to +15V
All other pins	0V to 25V

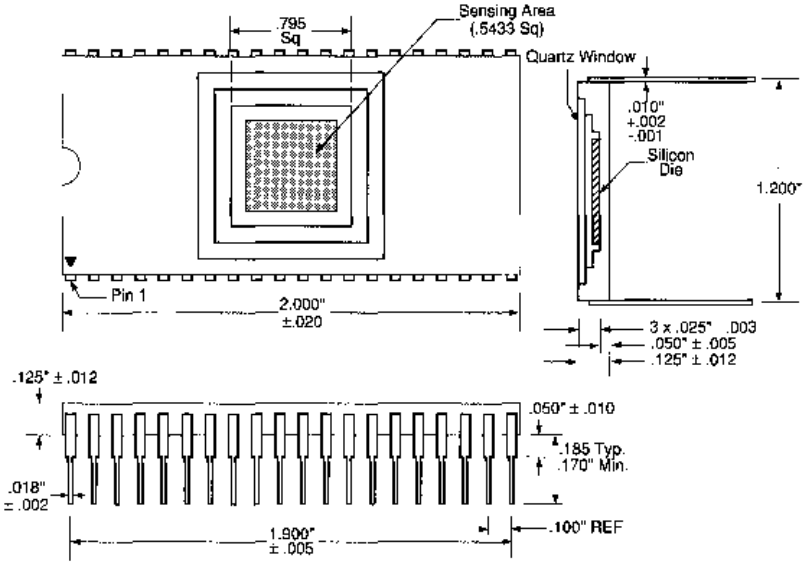


Figure 7. Package Dimensions

Ordering Information

Grade	Maximum Point Defects	Maximum Column Defects	Maximum Cluster Defects	Unsealed Part Number	Quartz Window
0	0	0	0	RA0512JAU-011	RA0512JAQ-011
1	10	0	1	RA0512JAU-020	RA0512JAQ-020
2	100	0	2	RA0512JAU-021	RA0512JAQ-021

Defect Definition

A. Point defects - Hot, low or trap
   1. Hot pixel - a pixel with an output signal 10 times greater than average dark current.
   2. Low pixel - a pixel with an output signal 50% lower than average background near full-well
   3. Charge trap - defect greater than 0.7% of full-well

B. Other
   1. Column defect - Ten or more contiguous point defects in a single column
   2. Cluster defect - Two to nine contiguous point defects

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General Description

The RA1024J is a full frame CCD sensor designed specifically for use in astronomy, spectroscopy and related scientific imaging applications. Its combination of very low noise and low dark current make it ideal for low light level, high dynamic range, and high resolution applications.

The imager is structured in a serial-parallel-serial configuration so charge packets (imaging data) in the vertical (parallel) registers can be shifted either up or down to two identical horizontal (serial) shift registers. One is at the top and another is at the bottom of the array. Three-phase clocks are needed to drive both vertical and horizontal shift registers.

The array is available in a 40-pin ceramic package as shown in Figure 1. Package dimensions are shown in Figure 7. It is available with a quartz window or unwindowed. The device is indifferent to its orientation in a circuit due to the symmetry of the pinout (see Table 1 for complete pinout description).

NOTE: The RA1024J does not contain gate protection circuitry to protect the input and output pins from static damage. Special handling precautions should be used to avoid static damage.

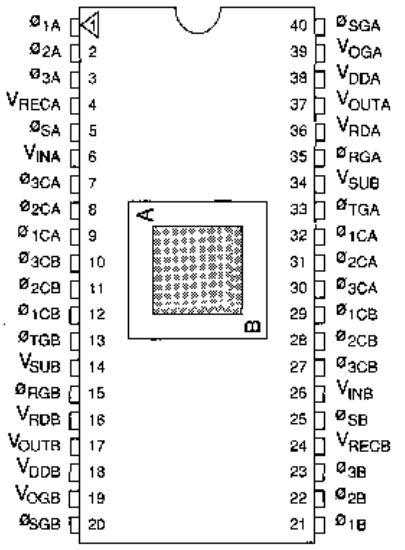


Figure 1. Pinout Configuration

Features

- 1,048,576 picture elements (pixels) in a 1024 x 1024 configuration
- 13.5 µm square pixels
- 3-Phase buried channel process
- On-chip output amplifier for low noise and high speed readout
- High dynamic range: over 97 dB at -110°C (183°K)
- Serial-parallel-serial configuration for selectable bidirectional readout
- Usable spectral response from 450 nm to 1050 nm

MPP Operation

A major source of dark current in devices such as this originates in surface states at the $Si\text{-}SiO_2$ interface. A unique design and process enables the RA1024J to be run in the "Multi-Pinned Phase" or MPP mode of operation. This helps eliminate dark current generation in the interface surface states. By holding the vertical clocks at negative potential during integration and horizontal signal readout, the surface of the sensing area is inverted. As a result, the surface will not be depleted and surface states will not generate dark current. Dark current densities of less than 50 pa/cm^2 have been achieved using the MPP mode of operation, resulting in integration times of more than 30 seconds at room temperature.

Functional Description

Imaging Area

The imaging area is an array of 1024 columns (vertical CCD shift registers) which are isolated from each other by 3.5 µm channel-stop regions. Each column has 1024 picture elements. The pixel size is 13.5 µm x 13.5 µm. The total imaging area is 13.8 mm x 13.8 mm. Typical spectral response as a function of wavelength is shown in Figure 2.

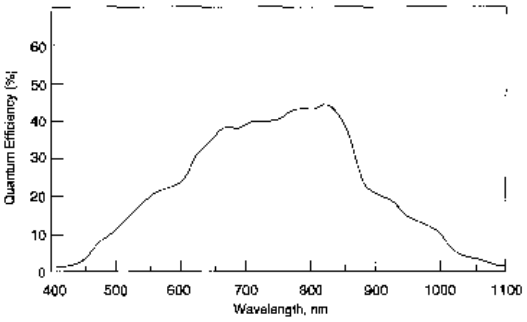


Figure 2. Typical Spectral Response

In the vertical direction, each pixel corresponds to one stage (three electrodes) of the shift register. The three-electrode groups are driven by three-phase clocks ($ø_{1C}$ - $ø_{3C}$) brought in from both edges of the array to improve clock electrode response time.

Charge packets (imaging data) in the vertical registers can be shifted either up or down to the top or bottom horizontal registers by interchanging two of the three phases ($ø_{1C}$ and $ø_{3C}$). See Figure 3 for functional diagram.

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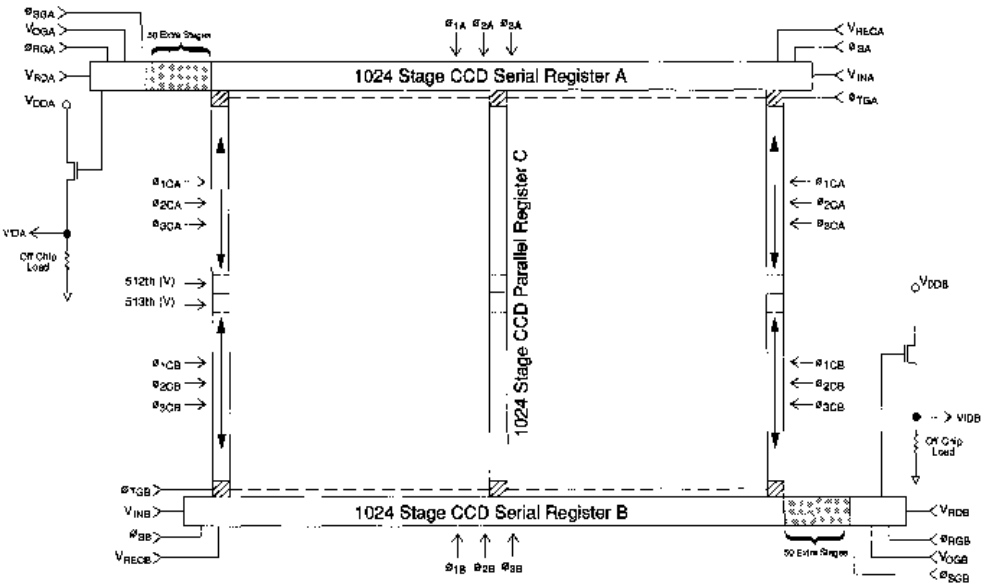


Figure 3. Functional Diagram

A transfer gate ($ø_{TG}$) is provided at the interface of the vertical and horizontal registers for controlling charge flow. Charge flow is from $ø_{3C}$ gate of the vertical shift register into the $ø_2$ and $ø_3$ gates of the horizontal shift register. The control function is performed by pulsing the transfer gate either high or low to permit or prevent the charge flow from the vertical register into the horizontal register for readout.

When the potential of the vertical register electrodes is held steady, a potential well is created beneath the storage gates ($ø_{1C}$ and $ø_{2C}$). When an image impinges on the sensing area, an electrical signal of the scene will be collected in the potential well during this integration period.

Following the integration interval, the collected charge (signal) in the array can be read out as a full-frame image by transferring the charge, one or more rows at a time, into the horizontal shift register. From there, charge can be shifted serially to the output amplifier.

A mechanical shutter is needed to shield the array from incident light during the read out process. A strobe illumination could be used to simulate the shuttered mode of operation. Image smearing degrades the performance, particularly at low data rates, unless such shuttering is provided.

Horizontal Registers

There are two identical horizontal shift registers which are driven by three-phase clocks ($ø_{1A}$ - $ø_{3A}$, $ø_{1B}$ - $ø_{3B}$), one at the top and one at the bottom of the imaging area. Each shift register has 1024 stages plus an extension of 48 stages. As a result, amplifier power is dissipated more efficiently and dark current generated by localized heating is minimized.

Summing Mode

At the end of each serial register, there is an output summing well which can be clocked to allow multiple-pixel summation of the scene. This summing well is located after the 50th extra stage of the horizontal registers and prior to the DC biased gate (V_{OG}) as shown in Figure 5. The summing gate (SG) can be clocked with one of the serial clock phases or with its own clock generator (see Figure 6 for summing gate timing). For example, two parallel lines of charge are additively transferred into the serial register, then the summing gate is pulsed low after the charge from two serial pixels has been transferred into the summing well. Thus, the resulting signal represents the sum of charges in four (2 x 2) contiguous pixels from the imaging section. It effectively reduces the 1024 x 1024 device to a 512 x 512 array and increases the pixel size by 4 times. Other variations of this technique can be useful for low-light level situations, i.e., scenes with low contrast, or a low signal-to-noise ratio. There is, of course, a loss in resolution which accompanies the gain in effective pixel size.

Output Amplifier

There is an on-chip amplifier which is located at the end of each extended serial shift register. The amplifier is a single-stage buried-channel transistor (Figure 5) designed to operate in the source-follower configuration with an off-chip load resistor (1KΩ - 20KΩ). It has a bandwidth of approximately 10 MHz with a 10 pF load.

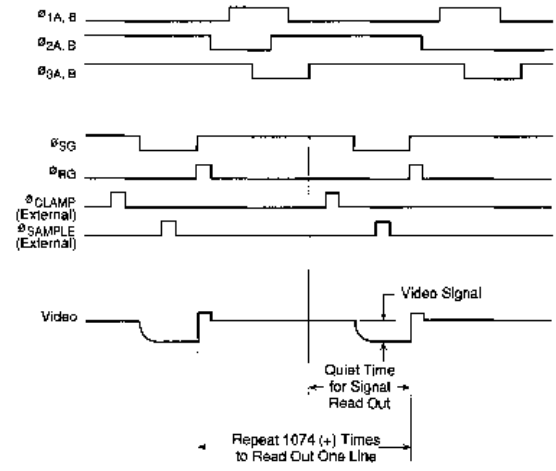


Figure 4A. Horizontal CCD Shift Register Timing Diagram

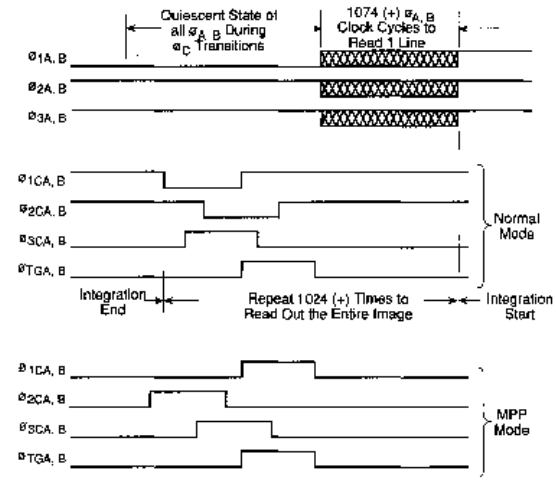


Figure 4B. Vertical CCD Shift Register Timing Diagram

Timing Requirements

The timing recommended to run the RA1024J imager in the low speed and low noise mode of operation is shown in Figures 4A and 4B. Other types of three-phase clocks can also be used to drive both the vertical and horizontal registers. For example, 50% duty cycle, three-phase clocks can be used to drive the horizontal register for high-speed operation. However, the large full well capacity and low noise floor will be sacrificed.

Figure 4A shows the timing of the horizontal three-phase clocks, summing well clock, reset clock, and external clamping and sampling clocks. To achieve high charge transfer efficiency and high full well capacity, serial clocks must overlap by more than 1 µs. In addition, the rise and fall times of the three-phase clocks may be more than 300 ns to prevent possible injection of spurious charge into the CCD channel. After the three-phase clock transitions, the clocks are held steady to provide a quiet period for signal readout. During this quiet period, the output amplifier is clamped and the signal charge in the summing well is transferred into the output sensing node. The output signal is then sampled and the sensing node is reset.

This timing is repeated 1,072 (or more) times to allow the readout of one complete line of the image. The video signal from one pixel is also shown in Figure 4A.

Figure 4B shows the timing requirements for the vertical register. Overlapping of the vertical clocks are normally longer than 5 µs. Rise and fall times of all clocks may be 300 ns or longer. All clock transitions should occur when the horizontal clocks are held steady.

Timing for MPP and normal mode is shown. The difference between the two modes is that during an integration, all clocks must be held low for MPP mode. The clocks should repeat 1,024 times (or more) to read out the entire image.

Array Cooling

Both the dark current and noise performance of the array can be improved by cooling. The dark current will be reduced 50% for every 7°C reduction in array temperature. The noise floor of the output amplifier is proportional to $\sqrt{kTC}$ where k is Boltzmann's constant, T is the array temperature in degrees Kelvin and C is the output node capacitance of approximately .17 pF. Cooling can be achieved via a thermo-electric, Joule-Thomson cooler, or liquid nitrogen dewar.

UV Coating

The RA1024JAU CCD is available with a special UV enhancement coating which extends the spectral response range to 120 nm. A thin layer of lumogen is deposited directly on the frontside illuminated arrays and will emit at 550 nm when excited by 120 nm - 450 nm light. The coating is transparent in the visible and near-infrared spectrums. UV coated devices are designated by the -3XX part number.

Backside Illumination - Thinning

The RA1024JAU is also available in a thinned version which greatly improves the quantum efficiency in the visible and near-infrared while also giving excellent performance in the 200 - 400 nm UV range. The imaging area of the device is thinned to 10 µ using a chemical etch procedure. Then a flash-oxide treatment is applied to the thinned area. To activate the flash-oxide, it is necessary to UV flood the array (expose the array to a UV light source for 5 - 10 minutes or longer, using a mercury lamp (eprom eraser)) to charge the device. Once the array is returned to room temperature the charge will decrease requiring another charging. Thinned devices have pinouts which are mirror images of the frontside devices and are designated by the -2XX part number.

Specifications

Recommended operating conditions for the RA1024J are shown in Table 2. Typical device specifications are shown in Table 3, and Table 4 gives typical capacitance values.

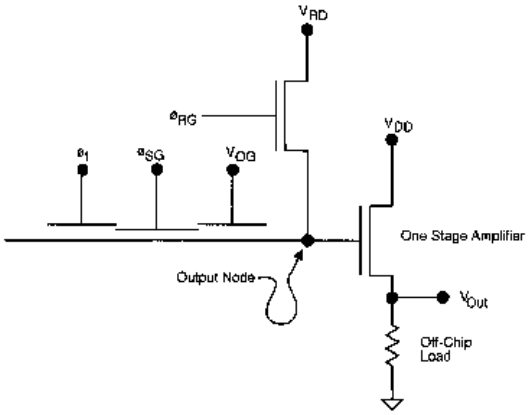


Figure 5. Output Structure

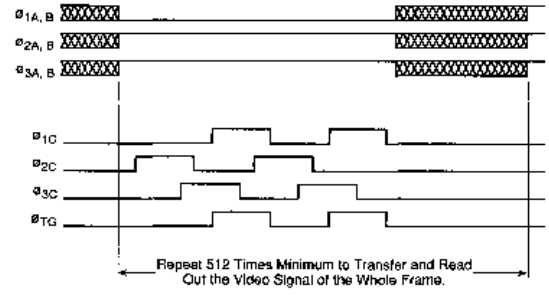


Figure 6A. Timing Comparison Between $\phi_{A, B}$ and ϕ_C in the Summing Mode. Two Vertically Adjacent Pixels are Summed into the Horizontal (Serial) Shift Register before being Read Out. (Vertical Clocks ϕ_C are in the MPP Mode.)

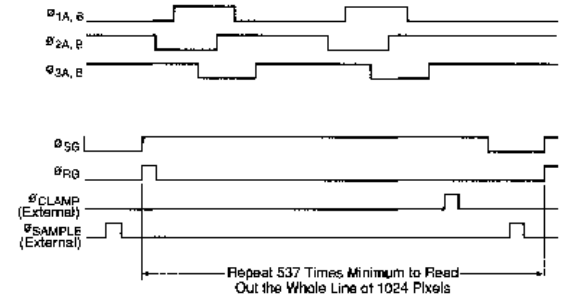


Figure 6B. Timing Comparison between $\phi_{A, B}$ and ϕ_{SG} in the Summing Mode. Two Horizontal Adjacent Pixels were Summed into the Summing Well (controlled by ϕ_{SG}) before being Read Out Serially.

Table 1. Pin Descriptions

Pin No.	Sym	Function	Register
1	ϕ_{1A}	Serial phase 1 clock	A
2	ϕ_{2A}	Serial phase 2 clock	A
3	ϕ_{3A}	Serial phase 3 clock	A
4	V_{RECA}	Input receiving gate	A
5	ϕ_{SA}	Input sample gate	A
6	V_{INA}	Input diode	A
7, 30	ϕ_{3CA}	Parallel phase 3 clock	C Upper
8, 31	ϕ_{2CA}	Parallel phase 2 clock	C Upper
9, 32	ϕ_{1CA}	Parallel phase 1 clock	C Upper
10, 27	ϕ_{3CB}	Parallel phase 3 clock	C Lower
11, 28	ϕ_{2CB}	Parallel phase 2 clock	C Lower
12, 29	ϕ_{1CB}	Parallel phase 1 clock	C Lower
13	ϕ_{TGB}	Transfer gate clock	B
14	V_{SUB}	Substrate	
15	ϕ_{RGB}	Reset gate clock	B
16	V_{RDB}	Reset drain	B
17	V_{OUTB}	Video output	B
18	V_{DDB}	Drain supply of amplifier	B
19	V_{OGB}	Output gate bias	B
20	ϕ_{SGB}	Summing well gate clock	B
21	ϕ_{1B}	Serial phase 1 clock	B
22	ϕ_{2B}	Serial phase 2 clock	B
23	ϕ_{3B}	Serial phase 3 clock	B
24	V_{RECB}	Input receiving gate	B
25	ϕ_{SB}	Input sample gate	B
26	V_{INB}	Input diode	B
33	ϕ_{TGA}	Transfer gate clock	A
34	V_{SUB}	Substrate	
35	ϕ_{RGA}	Reset gate	A
36	V_{RDA}	Reset drain	A
37	V_{OUTA}	Video output	A
38	V_{DDA}	Drain supply of amplifier	A
39	V_{OGA}	Output gate	A
40	ϕ_{SGA}	Summing well gate clock	A

Table 2. Recommended Operating Conditions

Definition		Symbol	Parameter						Units
			Normal Mode			MPP Mode			
			Low	Typ	High	Low	Typ	High	
DC supply		V_{DD}	20	21	22	20	21	25	V DC
Output gate bias		V_{OG}	3	6	8	1	2	5	V DC
Reset drain bias		V_{RD}	12	13	14	12	13	14	V DC
Substrate bias		V_{SUB}, V_{SS}	0	-0.5	-5.0	0	-1	-5.0	V DC
Serial clocks	High	$ø_A$, $ø_B$		12			10		V
	Low			0			-2		V
Vertical clocks	High	$ø_{1C}$, $ø_{2C}$, $ø_{3C}$		12			2.0		V
	Low			0			-10		V
Transfer gate clock	High	$ø_{TG}$		12			2		V
	Low			0			-10		V
Reset gate clock	High	$ø_{RG}$		15			12		V
	Low			0		0	0	1	V
Summing gate clock	High	$ø_{SG}$		12			5		V
	Low			0			-5		V

Table 3. Typical Device Specifications

Test Conditions: Temperature - 230°K (-43°C); Pixel Rate - 50 kHz; Tint - 10 sec

Parameter	Sym	Min	Typ	Max	Units
Format			1024 x 1024 full frame		
Pixel size			13.5 µm x 13.5 µm		
Imaging area			13.8 mm x 13.8 mm		
Dynamic range [1]	DR				
Normal mode			58,333:1 (95 dB)		
MPP mode			40,000:1 (92 dB)		
Full well charge	Q_{sat}				
Normal mode			175		K electrons
MPP mode			120		K electrons
Saturation voltage [2]	V_{sat}				
Normal mode			150		mV
MPP mode			120		mV
Dark current [3,6,7]	DL				
Normal mode			1.0		na/cm^2
MPP mode			50		pa/cm^2
Saturation exposure	E_{sat}				µJ/cm^2
Responsivity	R				V/µJ/cm^2
Photo-response nonuniformity [4]	PRNU		3	5	±%
Dark signal nonuniformity [3]	DSNU		4		mV
Charge transfer efficiency	CTE		.99999		
Output amplifier gain			.69		µV/electron
Read noise [5]			3		electrons

Notes:

1 Full well/read noise

2 R_{Load} = 5.1K

3 Pixels greater than 30% of the local average of 10 pixels on a line are considered defects and are ignored.

4 Pixels greater or less than 10% of the local average of 10 pixels on a line are considered defects and are ignored.

5 Measured at -110°C.

6 Typical dark current for thinned version is 2 times higher then frontside illuminated device.

7 At 23°C.

Table 4. Typical Capacitance Values

Parameter	Sym	Pin No.	Typ Value	Units
Parallel clocks	ϕ_{1C}	20, 40	2100	pF
	ϕ_{2C}	19, 39	1550	pF
	ϕ_{3C}	1, 21	2150	pF
Serial clocks	$\phi_{1A/B}$	9, 29	135	pF
	$\phi_{2A/B}$	8, 28	90	pF
	$\phi_{3A/B}$	7, 27	180	pF
Transfer clocks	$\phi_{TGA/B}$	3, 18, 23, 38	71	pF
Video output	$V_{OutA/B}$	15, 35	10	pF
Reset gate clock	$\phi_{RGA,B}$	12, 32	21	pF
Summing gate clock	$\phi_{SGA,B}$	17, 37	9	pF

Absolute Maximum Ratings

Storage temperature: -150°C to +50°C

Voltages: measured with respect to substrate pins 14 & 34

Pins 1, 2, 3, 7, 8, 9, 10, 11, 12, 13, 20, 21, 22, 23, 27, 28, 29, 30, 31, 32, 33, 40	-15V to +15V
All other pins	0V to 25V

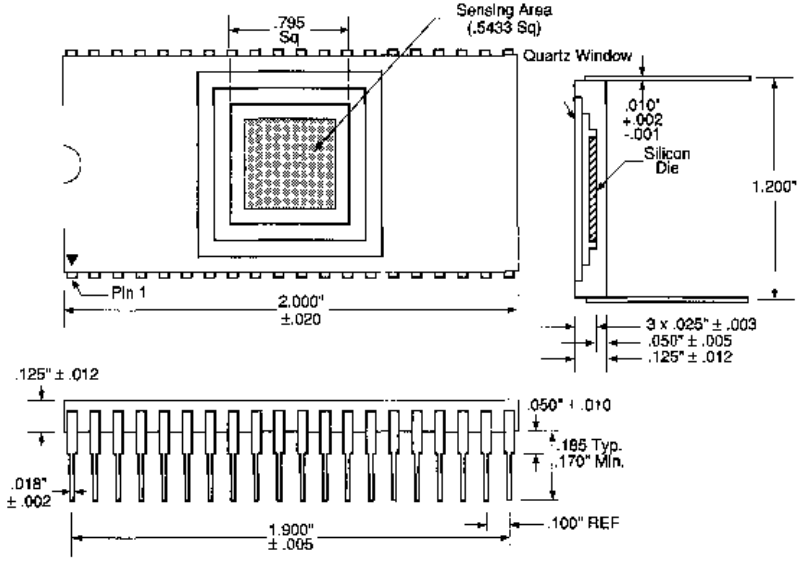


Figure 7. Package Dimensions

Ordering Information

Grade	Maximum Point Defects	Maximum Column Defects	Maximum Cluster Defects	Part Number
1	10	0	1	RA1024JAU-020
2	100	0	2	RA1024JAU-021
3	100	10	5	RA1024JAU-022

Defect Definition

A. Point defects - Hot, low or trap
   1. Hot pixel - a pixel with an output signal 10 times greater than average dark current.
   2. Low pixel - a pixel with an output signal 50% lower than average background near full-well
   3. Charge trap - defect greater than 0.7% of full-well

B. Other
   1. Column defect - Ten or more contiguous point defects in a single column
   2. Cluster defect - Two to nine contiguous point defects

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General Description

The RA1200J is a full frame CCD sensor designed specifically for use in astronomy, spectroscopy and related scientific imaging applications. Its combination of very low noise and low dark current make it ideal for low light level, high dynamic range, and high resolution applications.

The imager is structured in a serial-parallel-serial configuration so charge packets (imaging data) in the vertical (parallel) registers can be shifted either up or down to two identical horizontal (serial) shift registers. One is at the top and another is at the bottom of the array. Three-phase clocks are needed to drive both vertical and horizontal shift registers.

The array is available in a 48-pin ceramic package as shown in Figure 1. Package dimensions are shown in Figure 7. It is available with a quartz window or unwindowed. The device is indifferent to its orientation in a circuit due to the symmetry of the pinout (see Table 1 for complete pinout description).

NOTE: The RA1200J does not contain gate protection circuitry to protect the input and output pins from static damage. Special handling precautions should be used to avoid static damage.

Features

- 480,000 picture elements (pixels) in a 400 x 1200 configuration
- 27 µm square pixels
- 3-Phase buried channel process
- On-chip output amplifier for low noise and high speed readout
- High dynamic range: over 102 dB at -110°C (183°K)
- Serial-parallel-serial configuration for selectable bidirectional readout
- Usable spectral response from 450 nm to 1050 nm

MPP Operation

A major source of dark current in devices such as this originates in surface states at the Si-SiO_2 interface. A unique design and process enables the RA1200J to be run in the "Multi-Pinned Phase" or MPP mode of operation. This helps eliminate dark current generation in the interface surface states. By holding the vertical clocks at negative potential during integration and horizontal signal readout, the surface of the sensing area is inverted. As a result, the surface will not be depleted and surface states will not generate dark current. Dark current densities of less than 50 pa/cm^2 have been achieved using the MPP mode of operation, resulting in integration times of more than 30 seconds at room temperature.

Functional Description

Imaging Area

The imaging area is an array of 1200 columns (vertical CCD shift registers) which are isolated from each other by 5 µm channel-stop regions. Each column has 400 picture elements. The pixel size is 27 µm x 27 µm. The imaging area is divided into two sections of 200 x 1200 pixels. Each section can be operated independently with its own three-phase vertical clock. If both sections share the same clocks, the device operates as a full frame 400 x 1200 imager. Typical spectral response as a function of wavelength is shown in Figure 2.

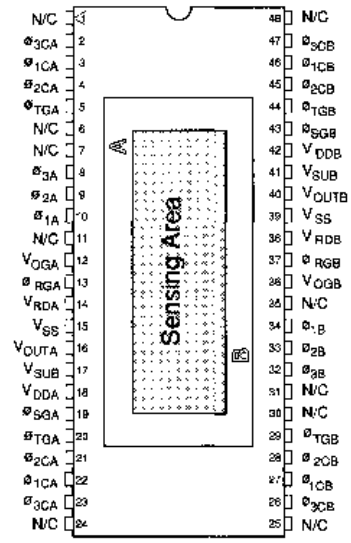


Figure 1. Pinout Configuration

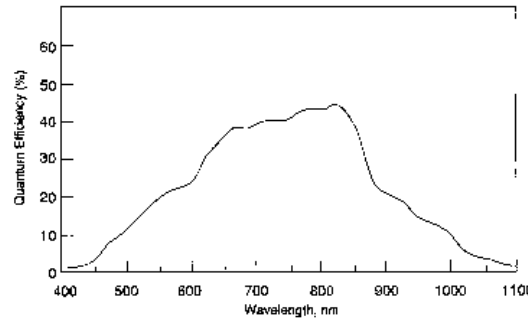


Figure 2. Typical Spectral Response

In the vertical direction, each pixel corresponds to one stage (three electrodes) of the shift register. The three-electrode groups are driven by three-phase clocks ($ø_{1C}$ - $ø_{3C}$) brought in from both edges of the array for improving response time.

Charge packets (imaging data) in the vertical registers can be shifted either up or down to the top or bottom horizontal registers

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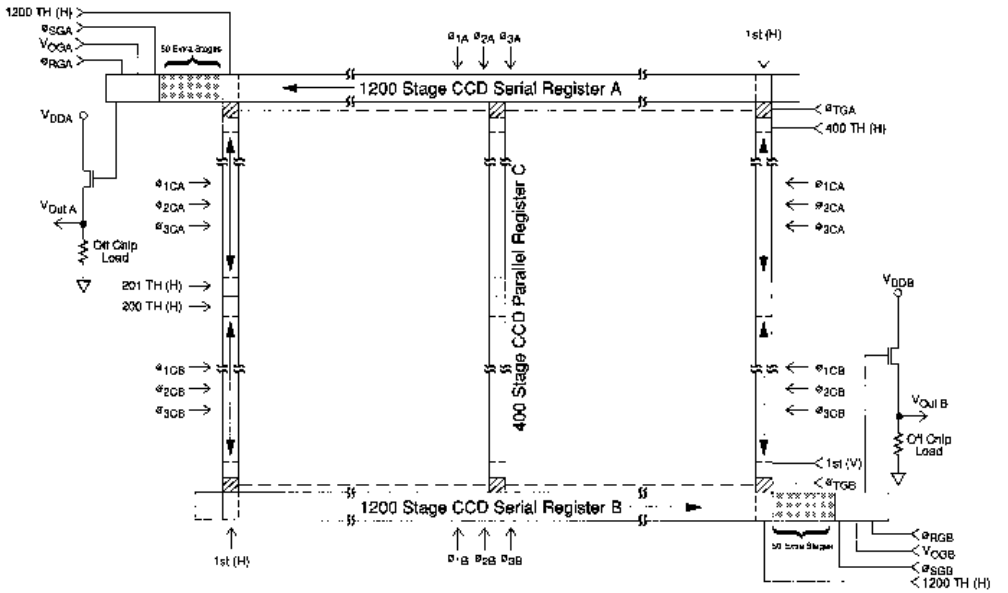


Figure 3. Functional Diagram

by interchanging one of the three phases ($ø_{1C}$ and $ø_{2C}$). See Figure 3 for functional diagram.

A transfer gate ($ø_{TG}$) is provided at the interface of the vertical and horizontal registers for controlling charge flow. Charge flow is from $ø_{3C}$ gate of the vertical shift register into $ø_2$ and $ø_3$ gates of the horizontal shift register. The control function is performed by pulsing the transfer gate either high or low to permit or prevent the charge flow from the vertical register into the horizontal register for readout.

When the potential of the vertical register electrodes is held steady, a potential well is created beneath the storage gates ($ø_{1C}$ and $ø_{2C}$). When an image impinges on the sensing area, an electrical signal of the scene will be collected in the potential well during this integration period.

Following the integration interval, the collected charge (signal) in the array can be read out as a full-frame image by transferring the charge, one or more rows at a time, into the horizontal shift register. From there, charge can be shifted serially to the output amplifier.

A mechanical shutter is needed to shield the array from incident light during the read out process. A strobe illumination could be used to simulate the shuttered mode of operation. Image smearing degrades the performance, particularly at low data rates, unless such shuttering is provided.

Horizontal Registers

There are two identical horizontal shift registers which are driven by three-phase clocks, one at the top and one at the bottom of the imaging area. Each shift register has 1200 stages plus an extension of 50 stages. As a result, amplifier power is dissipated more efficiently and dark current generated by localized heating is minimized.

Summing Mode

At the end of each serial register, there is an output summing well which can be clocked to allow multiple-pixel summation of the scene. This summing well is located after the 50th extra stage of the horizontal registers and prior to the DC biased gate (V_{OG}) as shown in Figure 5. The summing gate (SG) can be clocked with one of the serial clock phases or with its own clock generator (see Figure 6 for summing gate timing). For example, two parallel lines of charge are additively transferred into the serial register, then the summing gate is pulsed low after the charge from two serial pixels has been transferred into the summing well. Thus, the resulting signal represents the sum of charges in four (2 x 2) contiguous pixels from the imaging section. It effectively reduces the 400 x 1200 device to a 200 x 600 array and increases the pixel size by 4 times. Other variations of this technique can be useful for low-light level situations, i.e., scenes with low contrast, or a low signal-to-noise ratio. There is, of course, a loss in resolution which accompanies the gain in effective pixel size.

Output Amplifier

There is an on-chip amplifier which is located at the end of each extended serial shift register. The amplifier is a single-stage buried-channel transistor (Figure 5) designed to operate in the source-follower configuration with an off-chip load resistor (1KΩ - 20KΩ). It has a bandwidth of approximately 10 MHz with a 10 pF load.

Timing Requirements

The timing recommended to run the RA1200J imager in the low speed and low noise mode of operation is shown in Figures 4A and 4B. Other types of three-phase clocks can also be used to drive both the vertical and horizontal registers. For example, 50% duty cycle, three-phase clocks can be used to drive the

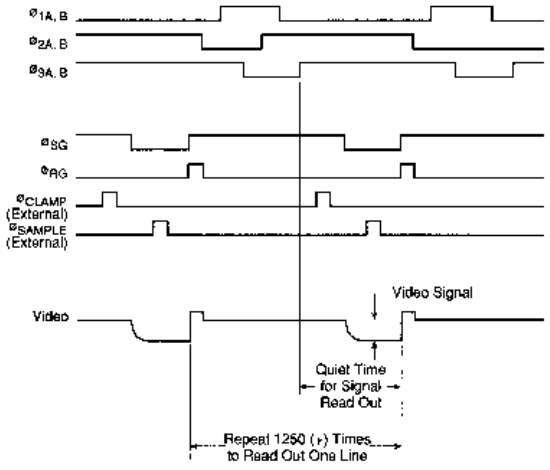


Figure 4A. Horizontal CCD Shift Register Timing Diagram

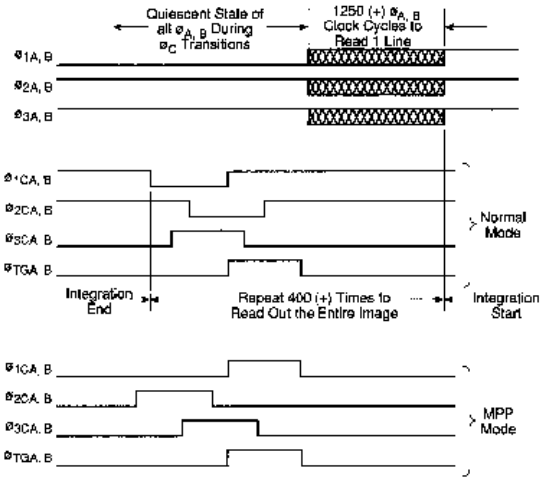


Figure 4B. Vertical CCD Shift Register Timing Diagram

horizontal register for high-speed operation. However, the large full well capacity and low noise floor will be sacrificed.

Figure 4A shows the timing of the horizontal three-phase clocks, summing well clock, reset clock, and external clamping and sampling clocks. To achieve high charge transfer efficiency and high full well capacity, the serial clocks must overlap by more than 1 µs. In addition, the rise and fall times of the three-phase clocks may be more than 300 ns to prevent possible injection of spurious charge into the CCD channel. After the three-phase clock transitions, the clocks are held steady to provide a quiet period for signal readout. During this quiet period, the output amplifier is clamped and the signal charge in the summing well is transferred into the output sensing node. The output signal is then sampled and the sensing node is reset.

This timing is repeated 1,250 (or more) times to allow the readout of one complete line of the image. The video signal from one pixel is also shown in Figure 4A.

Figure 4B shows the timing requirements for the vertical register. Overlapping of the vertical clocks are normally longer than 5 µs. Rise and fall times of all clocks may be 300 ns or longer. All clock transitions should occur when the horizontal clocks are held steady.

Timing for MPP and normal mode is shown. The difference between the two modes is that during an integration, all clocks must be held low for MPP mode. The clocks should repeat 400 times (or more) to read out the entire image.

Array Cooling

Both the dark current and noise performance of the array can be improved by cooling. The dark current will be reduced 50% for every 7°C reduction in array temperature. The noise floor of the output amplifier is proportional to $\sqrt{kTC}$ where k is Boltzmann's constant and T is the array temperature in degrees Kelvin and C is the output node capacitance of approximately .17 pF. Cooling can be achieved via a thermo-electric, Joule-Thomson cooler, or liquid nitrogen dewar.

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Backside Illumination - Thinning

The RA1200JAU is also available in a thinned version which greatly improves the quantum efficiency in the visible and near-infrared while also giving excellent performance in the 200 - 400 nm UV range. The imaging area of the device is thinned to 10 µ using a chemical etch procedure. Then a flash-oxide treatment is applied to the thinned area. To activate the flash-oxide it is necessary to UV flood the array (expose the array to a UV light source for 5 - 10 minutes or longer, using a mercury lamp (eprom eraser)) to charge the device. Once the array is returned to room temperature the charge will decrease requiring another charging. Thinned devices have pinouts which are mirror images of the frontside devices and are designated by the 2XX part number.

Specifications

Recommended operating conditions for the RA1200J are shown in Table 2. Typical device specifications are shown in Table 3, and Table 4 gives typical capacitance values.

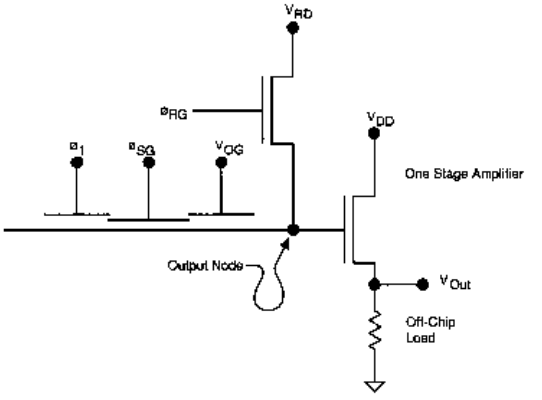


Figure 5. Output Structure

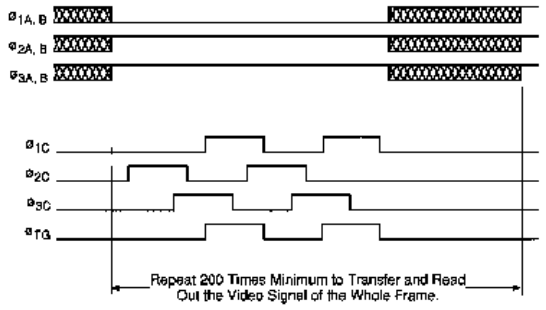


Figure 6A. Vertical Summing Two rows of data are summed into the horizontal (serial) shift register

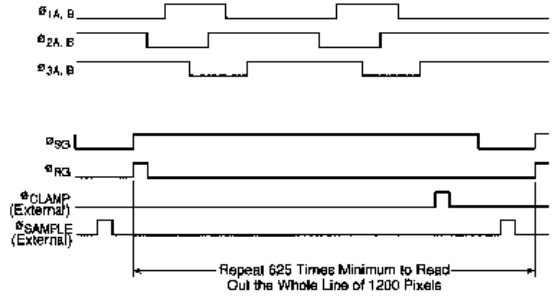


Figure 6B. Horizontal Summing Two rows of data are summed into the horizontal (serial) shift register

Table 1. Pin Descriptions

Pin No.	Sym	Function	Register
1, 24	N/C		C Upper
2, 23	ϕ_{3CA}	Parallel phase 3 clock	C Upper
3, 22	ϕ_{1CA}	Parallel phase 1 clock	C Upper
4, 21	ϕ_{2CA}	Parallel phase 2 clock	C Upper
5, 20	ϕ_{TGA}	Transfer gate clock	
6, 7	N/C		
8	ϕ_{3A}	Serial phase 3 clock	A
9	ϕ_{2A}	Serial phase 2 clock	A
10	ϕ_{1A}	Serial phase 1 clock	A
11	N/C		A
12	V_{OGA}	Output bias gate	A
13	ϕ_{RGA}	Reset gate clock	A
14	V_{RDA}	Reset drain	A
15, 39	V_{SS}	Top side contact of substrate	
16	V_{OUTA}	Video output (top)	A
17, 41	V_{SUB}	Substrate	
18	V_{DDA}	Drain supply of amplifier	A
19	ϕ_{SGA}	Summing well gate clock	A
25, 48	N/C		C Lower
26, 47	ϕ_{3CB}	Parallel phase 3 clock	C Lower
27, 46	ϕ_{1CB}	Parallel phase 1 clock	C Lower
28, 45	ϕ_{2CB}	Parallel phase 2 clock	C Lower
29, 44	ϕ_{TGB}	Transfer gate clock	
30, 31	N/C		
32	ϕ_{3B}	Serial phase 3 clock	B
33	ϕ_{2B}	Serial phase 2 clock	B
34	ϕ_{1B}	Serial phase 1 clock	B
35	N/C		B
36	V_{OGB}	Output bias gate	B
37	ϕ_{RGB}	Reset gate clock	B
38	V_{RDB}	Reset drain	B
40	V_{OUTB}	Video output (bottom)	B
42	V_{DDB}	Drain supply of amplifier	B
43	ϕ_{SGB}	Summing well gate clock	B

Table 2. Recommended Operating Conditions

Definition		Symbol	Parameter						Units
			Normal Mode			MPP Mode			
			Low	Typ	High	Low	Typ	High	
DC supply		V_{DD}	20	21	22	20	21	25	V DC
Output gate bias		V_{OG}	3	6	8	1	2	5	V DC
Reset drain bias		V_{RD}	12	13	14	12	13	14	V DC
Substrate bias		V_{SUB}, V_{SS}	0	-0.5	-5.0	0	-1	-5.0	V DC
Serial clocks	High	$ø_A$, $ø_B$		12			10		V
	Low			0			-2		V
Vertical clocks	High	$ø_{1C}$, $ø_{2C}$, $ø_{3C}$		12			2.0		V
	Low			0			-10		V
Transfer gate clock	High	$ø_{TG}$		12			2		V
	Low			0			-10		V
Reset gate clock	High	$ø_{RG}$		15			12		V
	Low			0		0	0	1	V
Summing gate clock	High	$ø_{SG}$		12			5		V
	Low			0			-5		V

Table 3. Typical Device Specifications

Test Conditions: Temperature - 230°K (-43°C); Pixel Rate - 50 kHz; Tint - 10 sec

Parameter	Sym	Min	Typ	Max	Units
Format			400 x 1200 full frame		
Pixel size			27 µm x 27 µm		
Imaging area			32.4 mm x 10.8 mm		
Dynamic range [1]	DR				
Normal mode			125,000:1 (102 dB)		
MPP mode			116,666:1 (101 dB)		
Full well charge	Q_{sat}				
Normal mode			500		K electrons
MPP mode			350		K electrons
Saturation voltage [2]	V_{sat}				
Normal mode			250		mV
MPP mode			220		mV
Dark current [3,6,7]	DL				
Normal mode			1.0		na/cm^2
MPP mode			50		pa/cm^2
Saturation exposure	E_{sat}		5.7		µJ/cm^2
Responsivity	R		20		V/µJ/cm^2
Photo-response nonuniformity [4]	PRNU		5	5	±%
Dark signal nonuniformity [3]	DSNU		4		mV
Charge transfer efficiency	CTE		.99999		
Output amplifier gain			.69		µV/electron
Read noise [5]			3		electrons

Notes:

1 Full well/read noise

2 R_{Load} = 5.1K

3 Pixels greater than 30% of the local average of 10 pixels on a line are considered defects and are ignored.

4 Pixels greater or less than 10% of the local average of 10 pixels on a line are considered defects and are ignored.

5 Measured at -110°C.

6 Typical dark current for thinned version is 2 times higher then frontside illuminated device.

7 At 23°C.

Table 4. Typical Capacitance Values

Parameter	Sym	Pin No.	Typ Value	Units
Parallel clocks	$ø_{1C}$	20, 40	2100	pF
	$ø_{2C}$	19, 39	1550	pF
	$ø_{3C}$	1, 21	2150	pF
Serial clocks	$ø_{1A/B}$	9, 29	135	pF
	$ø_{2A/B}$	8, 28	90	pF
	$ø_{3A/B}$	7, 27	180	pF
Transfer clocks	$ø_{TGA/B}$	3, 18, 23, 38	71	pF
Video output	$V_{OutA/B}$	15, 35	10	pF
Reset gate clock	$ø_{RGA,B}$	12, 32	21	pF
Summing gate clock	$ø_{SGA,B}$	17, 37	9	pF

Absolute Maximum Ratings

Storage temperature: -150°C to +50°C

Voltages: measured with respect to substrate pins 15, 17, 39 & 41

Pin 2, 3, 4, 5, 8, 9, 10, 19, 20, 21, 22, 23, 26, 27, 28, 29, 32, 33, 34, 43, 44, 45, 46, 47	-15V to +15V
All other pins	0V to +25V

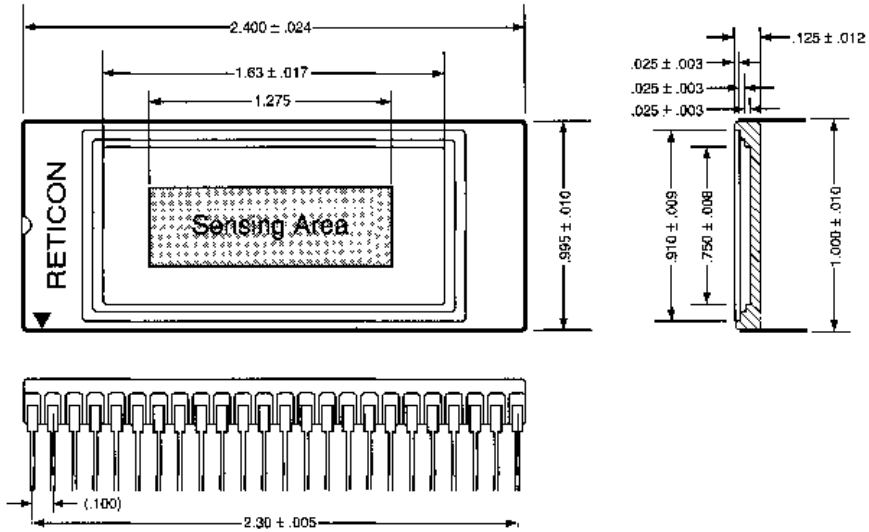


Figure 7. Package Dimensions

Ordering Information

Grade	Maximum Point Defects	Maximum Column Defects	Unsealed Part Number	Quartz Window
1	10	0	RA1200JAU-020	RA1200JAQ-020
2	100	0	RA1200JAU-021	RA1200JAQ-021
3	100	10	RA1200JAU-022	RA1200JAQ-022

Defect Definition

A. Point defects - Hot, low or trap
   1. Hot pixel - a pixel with an output signal 10 times greater than average dark current.
   2. Low pixel - a pixel with an output signal 50% lower than average background near full-well.
   3. Charge trap - defect greater than 0.7% of full-well

B. Other
   1. Column defect - ten or more contiguous point defects in a single column
   2. Cluster defect - two to nine contiguous point defects

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April 1992

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RA2000J
Full Frame CCD Imager

General Description

The RA2000J is a full frame CCD sensor designed specifically for use in astronomy, spectroscopy and related scientific imaging applications. Its combination of very low noise and low dark current make it ideal for low light level, high dynamic range, and high resolution applications.

The imager is structured in a serial-parallel-serial four quadrant configuration so charge packets (imaging data) in the vertical (parallel) registers can be shifted either up or down to four identical horizontal (serial) shift registers. Two are at the top and two are at the bottom of the array. Three-phase clocks are needed to drive both vertical and horizontal shift registers.

The array is available in a 56-pin metal package as shown in Figure 1. Package dimensions are shown in Figure 7. It is available with a quartz window or unwindowed. The device is indifferent to its orientation in a circuit due to the symmetry of the pinout (see Table 1 for complete pinout description).

NOTE: The RA2000J does not contain gate protection circuitry to protect the input and output pins from static damage. Special handling precautions should be used to avoid static damage.

Features

- 4,194,304 picture elements (pixels) in a 2048 x 2048 configuration
- 13.5 µm square pixels
- 3-Phase buried channel process
- On-chip output amplifiers for low noise and high speed readout
- High dynamic range: over 95 dB at -110°C (183°K)
- Serial-parallel-serial configuration for selectable four quadrant readout
- Usable spectral response from 450 nm to 1050 nm

MPP Operation

A major source of dark current in devices such as this originates in surface states at the Si-SiO_2 interface. A unique design and process enables the RA2000J to be run in the "Multi-Pinned Phase" or MPP mode of operation. This helps eliminate dark current generation in the interface surface states. By holding the vertical clocks at negative potential during integration and horizontal signal readout, the surface of the sensing area is inverted. As a result, the surface will not be depleted and surface states will not generate dark current. Dark current densities of less than 50 pA/cm^2 have been achieved using the MPP mode of operation, resulting in integration times of more than 30 seconds at room temperature.

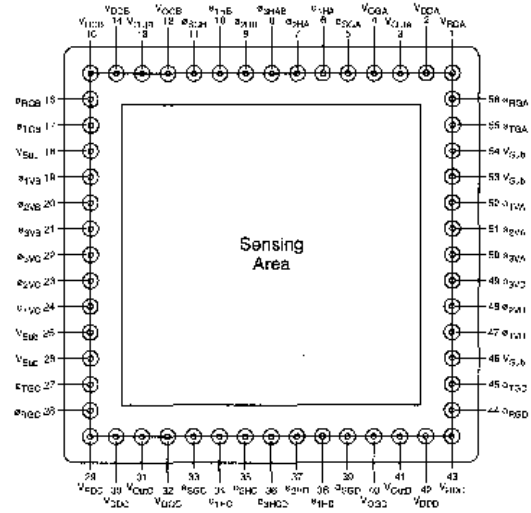


Figure 1. Pinout Configuration

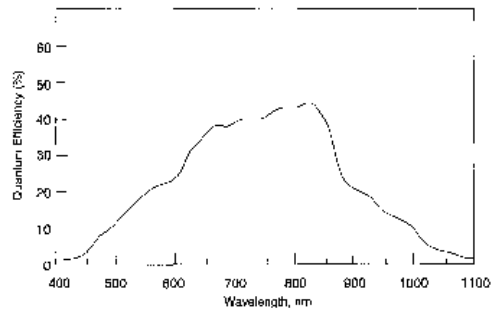


Figure 2. Typical Spectral Response

Functional Description

Imaging Area

The imaging area is an array of 2048 columns (vertical CCD shift registers) which are isolated from each other by 3.5 µm channel-stop regions. Each column has 2048 picture elements. The pixel size is 13.5 µm x 13.5 µm. The total imaging area is 27.6 mm x 27.6 mm. Typical spectral response as a function of wavelength is shown in Figure 2.

In the vertical direction, each pixel corresponds to one stage (three electrodes) of the shift register. The three-electrode groups are driven by three-phase clocks($ø_{1C}$ - $ø_{3C}$) brought in from both edges of the array to improve clock electrode response time.

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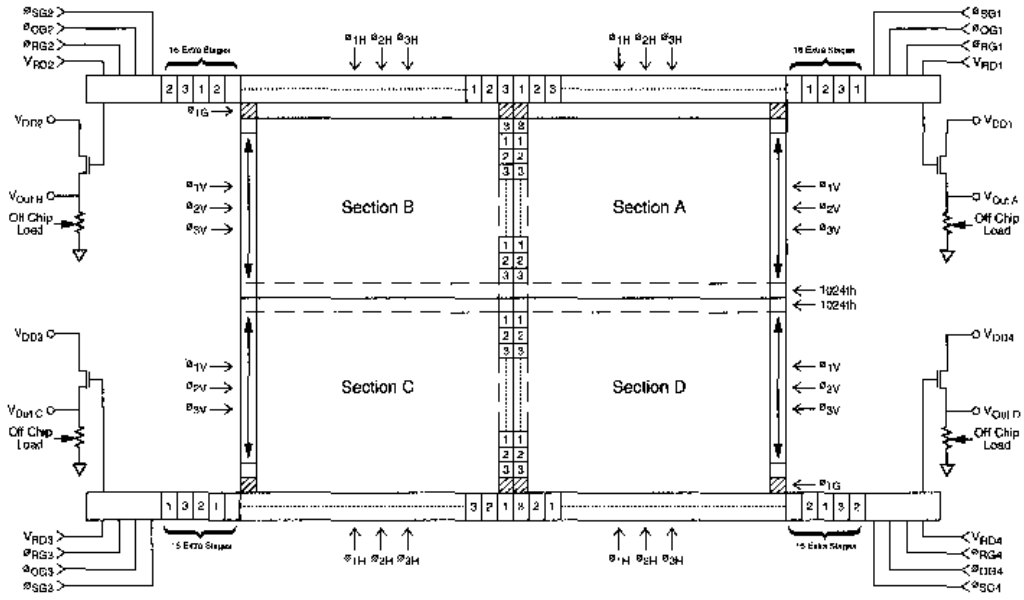


Figure 3. Functional Diagram

Charge packets (imaging data) in the vertical registers can be shifted either up or down to the top or bottom horizontal registers by interchanging two of the three phases ($ø_{1C}$ and $ø_{2C}$). See Figure 3 for functional diagram.

A transfer gate ($ø_{TG}$) is provided at the interface of the vertical and horizontal registers for controlling charge flow. Charge flow is from $ø_{3C}$ gate of the vertical shift register into $ø_2$ and $ø_3$ gates of the horizontal shift register. The control function is performed by pulsing the transfer gate either high or low to permit or prevent the charge flow from the vertical register into the horizontal register for readout.

When the potential of the vertical register electrodes is held steady, a potential well is created beneath the storage gates ($ø_{1C}$ and $ø_{2C}$). When an image impinges on the sensing area, an electrical signal of the scene will be collected in the potential well during this integration period.

Following the integration interval, the collected charge (signal) in the array can be read out as a full-frame image by transferring the charge, one or more rows at a time, into the horizontal shift register. From there, charge can be shifted serially to the output amplifier.

A mechanical shutter is needed to shield the array from incident light during the read out process. A strobe illumination could be used to simulate the shuttered mode of operation. Image smearing degrades the performance, particularly at low data rates, unless such shuttering is provided.

Horizontal Registers

There are four identical horizontal shift registers which are driven by three-phase clocks ($ø_{1A}$ - $ø_{3A}$, $ø_{1B}$ - $ø_{3B}$), two at the top and two at the bottom of the imaging area. Each shift register has 1024 stages plus an extension of 16 stages. As a result, amplifier power is dissipated more efficiently and dark current generated by localized heating is minimized.

Summing Mode

At the end of each serial register, there is an output summing well which can be clocked to allow multiple-pixel summation of the scene. This summing well is located after the 16th extra stage of the horizontal registers and prior to the DC biased gate (V_{OG}) as shown in Figure 5. The summing gate (SG) can be clocked with one of the serial clock phases or with its own clock generator (see Figure 6 for summing gate timing). For example, two parallel lines of charge are additively transferred into the serial register, then the summing gate is pulsed low after the charge from two serial pixels has been transferred into the summing well. Thus, the resulting signal represents the sum of charges in four (2 x 2) contiguous pixels from the imaging section. It effectively reduces the 2048 x 2048 device to a 1024 x 1024 array and increases the pixel size by 4 times. Other variations of this technique can be useful for low-light level situations, i.e., scenes with low contrast, or a low signal-to-noise ratio. There is, of course, a loss in resolution which accompanies the gain in effective pixel size.

Output Amplifier

There is an on-chip amplifier which is located at the end of each extended serial shift register. The amplifier is a single-stage buried-channel transistor (Figure 5) designed to operate in the source-follower configuration with an off-chip load resistor (1KΩ - 20KΩ). It has a bandwidth of approximately 5 MHz with a 10 pF load.

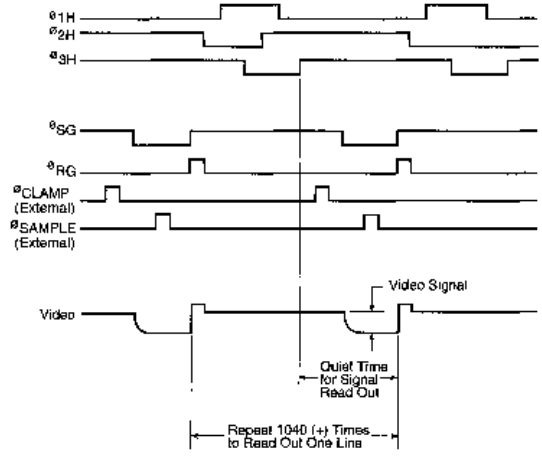


Figure 4A. Horizontal CCD Shift Register Timing (for both Normal and MPP Mode)

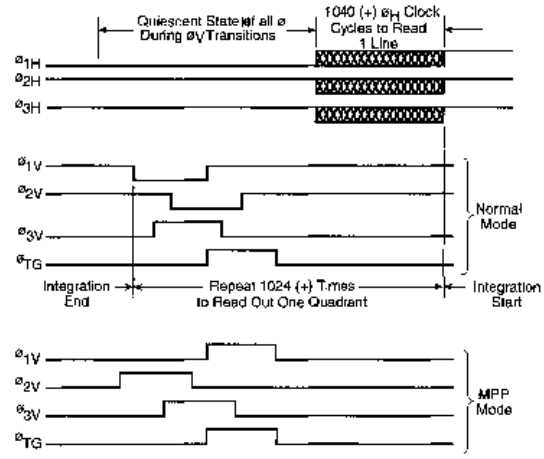


Figure 4B. Vertical CCD Shift Register Timing Diagram ($ø_{1V-3V}$) (and its relationship to horizontal clocks in both Normal and MPP Mode)

Timing Requirements

The timing recommended to run the RA2000J imager in the low speed and low noise mode of operation is shown in Figures 4A and 4B. Other types of three-phase clocks can also be used to drive both the vertical and horizontal registers. For example, 50% duty cycle, three-phase clocks can be used to drive the horizontal register for high-speed operation. However, the large full well capacity and low noise floor will be sacrificed.

Figure 4A shows the timing of the horizontal three-phase clocks, summing well clock, reset clock, and external clamping and sampling clocks. To achieve high charge transfer efficiency and high full well capacity, serial clocks must overlap by more than 1 µs. In addition, the rise and fall times of the three-phase clocks may be more than 300 ns to prevent possible injection of spurious charge into the CCD channel. After the three-phase clock transitions, the clocks are held steady to provide a quiet period for signal readout. During this quiet period, the output amplifier is clamped and the signal charge in the summing well is transferred into the output sensing node. The output signal is then sampled and the sensing node is reset.

This timing is repeated 1,040 (or more) times to allow the readout of each 1024 x 1024 quadrant of the image. The video signal from one pixel is also shown in Figure 4A.

Figure 4B shows the timing requirements for the vertical register. Overlapping of the vertical clocks are normally longer than 5 µs. Rise and fall times of all clocks may be 300 ns or longer. All clock transitions should occur when the horizontal clocks are held steady.

Timing for MPP and normal mode is shown. The difference between the two modes is that during an integration, all clocks must be held low for MPP mode. The clocks should repeat 1,024 times (or more) to read out the entire image.

Array Cooling

Both the dark current and noise performance of the array can be improved by cooling. The dark current will be reduced 50% for every 7°C reduction in array temperature. The noise floor of the output amplifier is proportional to $\sqrt{kTC}$ where k is Boltzmann's constant, T is the array temperature in degrees Kelvin and C is the output node capacitance of approximately .17 pF. Cooling can be achieved via a thermo-electric, Joule-Thomson cooler, or liquid nitrogen dewar.

UV Coating

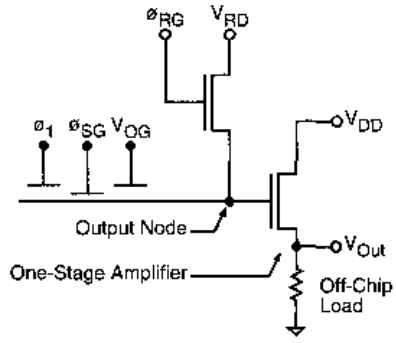
The RA2000JAU CCD is available with a special UV enhancement coating which extends the spectral response range to 120 nm. A thin layer of lumogen is deposited directly on the frontside illuminated arrays and will emit at 550 nm when excited by 120 nm - 450 nm light. The coating is transparent in the visible and near-infrared spectrums. UV coated devices are designated by the -3XX part number.

Backside Illumination - Thinning

The RA2000JAU is also available in a thinned version which greatly improves the quantum efficiency in the visible and near-infrared while also giving excellent performance in the 200 - 400 nm UV range. The imaging area of the device is thinned to 10 µ using a chemical etch procedure. Then a flash-oxide treatment is applied to the thinned area. To activate the flash oxide it is necessary to UV flood the array (expose the array to a UV light source for 5 - 10 minutes or longer, using a mercury lamp (EPROM eraser)) to charge the device. Once the array is returned to room temperature, the charge will decrease requiring another charging. Thinned devices have pinouts which are mirror images of the frontside devices and are designated by the 2XX part number.

Specifications

Recommended operating conditions for the RA2000J are shown in Table 2. Typical device specifications are shown in Table 3, and Table 4 gives typical capacitance values.



Note: Outputs A & C shown. For outputs B & D, exchange $ø_2$ for $ø_1$ shown.

Figure 5. Output Structure

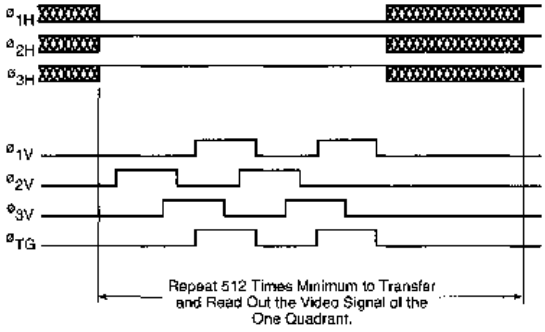


Figure 6A. Timing Comparison Between $ø_H$ qne $ø_v$ In the Summing Mode. Two vertically adjacent pixels are summed into the Horizontal (Serial) Register before being read out (Vertical Clocks $ø_v$ are in the MPP Mode).

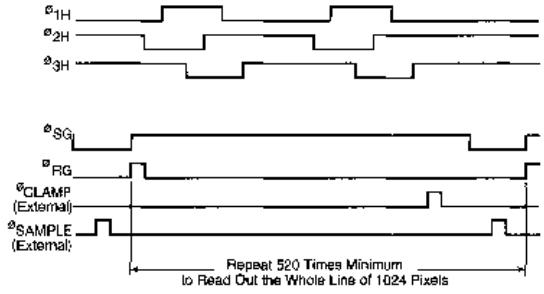


Figure 6B. Timing Comparison Between $ø_H$ and $ø_{SG}$ In the Summing Mode. Two horizontally adjacent pixels were summed into the Summing Well (controlled by $ø_{SG}$) before being read out serially.

Table 1. Pin descriptions for the RA2000J

Pin #	Sym	Function	Register
1	V_{RDA}	Reset drain	A
2	V_{DDA}	Drain supply of amplifier	A
3	V_{OutA}	Video output	A
4	V_{OGA}	Output bias gate	A
5	$ø_{SGA}$	Output summing gate	A
6	$ø_{1HA}$	Serial phase 1	A
7	$ø_{2HA}$	Serial phase 2	A
8	$ø_{3HA/B}$	Serial phase 3	A/B
9	$ø_{2HB}$	Serial phase 2	B
10	$ø_{1HB}$	Serial phase 1	B
11	$ø_{SGB}$	Summing well gate clock	B
12	V_{OGB}	Output bias gate	B
13	V_{OutB}	Video output	B
14	V_{DDB}	Drain supply of amplifier	B
15	V_{RDB}	Reset drain	B
16	$ø_{RGB}$	Reset gate clock	B
17	$ø_{TGB}$	Transfer gate clock	B
18	V_{Sub}	Substrate	
19	$ø_{1VB}$	Parallel phase 1	B
20	$ø_{2VB}$	Parallel phase 2	B
21	$ø_{3VB}$	Parallel phase 3	B
22	$ø_{3VC}$	Parallel phase 3	C
23	$ø_{2VC}$	Parallel phase 2	C
24	$ø_{1VC}$	Parallel phase 1	C
25	V_{Sub}	Substrate	
26	V_{Sub}	Substrate	
27	$ø_{TGC}$	Transfer gate clock	C
28	$ø_{RGC}$	Reset gate clock	C
29	V_{RDC}	Reset drain	C
30	V_{DDC}	Drain supply of amplifer	C
31	V_{OutC}	Video output	C
32	V_{OGC}	Ouput gate bias	C
33	$ø_{SGC}$	Summing well gate clock	C
34	$ø_{1HC}$	Serial phase 1	C
35	$ø_{2HC}$	Serial phase 2	C
36	$ø_{3HC/D}$	Serial phase 3	C/D
37	$ø_{2HD}$	Serial phase 2	D
38	$ø_{1HD}$	Serial phase 1	D
39	$ø_{SGD}$	Summing well gate clock	D
40	V_{OGD}	Output bias gate	D
41	V_{OutD}	Video output	D
42	V_{DDD}	Drain supply of amplifier	D
43	V_{RDD}	Reset drain	D
44	$ø_{RGD}$	Reset gate clock	D
45	$ø_{TGD}$	Transfer gate clock	D
46	V_{Sub}	Substrate	
47	$ø_{1VD}$	Parallel phase 1	D
48	$ø_{2VD}$	Parallel phase 2	D
49	$ø_{3VD}$	Parallel phase 3	D
50	$ø_{3VA}$	Parallel phase 3	A
51	$ø_{2VA}$	Parallel phase 2	A
52	$ø_{1VA}$	Parallel phase 1	A
53	V_{Sub}	Substrate	
54	V_{Sub}	Substrate	
55	$ø_{TGA}$	Transfer gate clock	A
56	$ø_{RGA}$	Reset gate clock	A

Table 2. Recommended Operating Conditions

Definition		Sym	Parameter						Units
			Normal Mode			MPP Mode			
			Low	Typ	High	Low	Typ	High	
DC supply		V_{DD}	16	18	22	16	18	22	V DC
Output gate bias		V_{OG}	5	6	8	1	2	5	V DC
Reset drain bias		V_{RD}		10	14		10	14	V DC
Substrate bias		V_{Sub}	-5	0	0	-5	0		V DC
Serial clocks	High	$ø_H$		12			+6		V
	Low			0			-4		V
Vertical clocks	High	$ø_V$		12			+3.5		V
	Low			0			-10		V
Transfer gate clock	High	$ø_{TG}$		12			2		V
	Low			0			-10		V
Reset gate clock	High	$ø_{RG}$		12			10		V
	Low		0	0		0	0	1	V
Summing gate clock	High	$ø_{SG}$		12			5		V
	Low			0			-5		V

Table 3. Device Specifications

Parameter	Sym	Min	Typ	Max	Units
Format			2048 X 2048 Full frame		
Pixel size			13.5 µm x 13.5 µm		
Imaging area			27.6 mm x 27.6 mm		
Dynamic range [1]	DR				
Normal mode			57500:1 (95 dB)		
MPP mode			40000:1 (92 dB)		
Full well charge	Q_{sat}				
Normal mode			175		K electrons
MPP mode			120		K electrons
Saturation voltage [2]	V_{sat}				
Normal mode			125		mV
MPP mode			80		mV
Dark current [3,6,7]	DL				
Normal mode			1		nA/cm^2
MPP mode			50		pA/cm^2
Saturation exposure	E_{sat}		1.42		$µJ/cm^2$
Responsitivity	R		20		$V/µJ/cm^2$
Photo-response nonuniformity [4]	PRNU		3	5	±%
Dark signal nonuniformity [3]	DSNU				mV
Charge transfer efficiency	CTE		0.99999		
Output amplifier gain			1		µV/electron
Read noise [5]			3		electrons

Notes:
1. Full well/read noise
2. R_{Load} = 5.1K
3. Pixels greater than 30% of the local average of 10 pixels on a line are considered defects and are ignored.
4. Pixels greater or less than 10% of the local average of 10 pixels on a line are considered defects and are ignored.
5. Measured at -110°C.
6. Typical dark current for thinned version is 2 times higher than frontside illuminated device.
7. At 23°C.

Table 4. Typical Capacitance Values

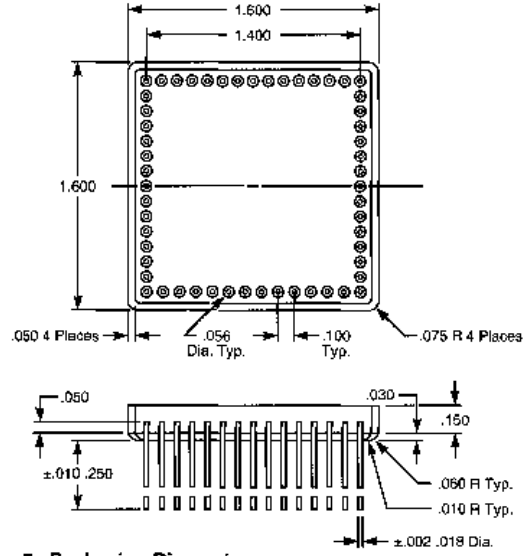
Parameter	Sym	Pin No.	Typ Value	Units
Parallel clocks	$\phi_{1V/A, B, C, D}$	52, 19, 24, 47	4200	pF
	$\phi_{2V/A, B, C, D}$	51, 20, 23, 48	3100	pF
	$\phi_{3V/A, B, C, D}$	50, 21, 22, 49	8600	pF
Serial clocks	$\phi_{1H/A, B, C, D}$	6, 10, 34, 38	135	pF
	$\phi_{2H/A, B, C, D}$	7, 9, 35, 37	90	pF
	$\phi_{3H/A, B, C, D}$	8, 36	180	pF
Transfer clock	$\phi_{TG/A, B, C, D}$	55, 17, 27, 45	71	pF
Video output	$V_{Out/A, B, C, D}$	3, 13, 31, 41	10	pF
Reset gate clock	$\phi_{RG/A, B, C, D}$	56, 16, 28, 44	21	pF
Summing gate clock	$\phi_{SG/A, B, C, D}$	5, 11, 33, 39	9	pF

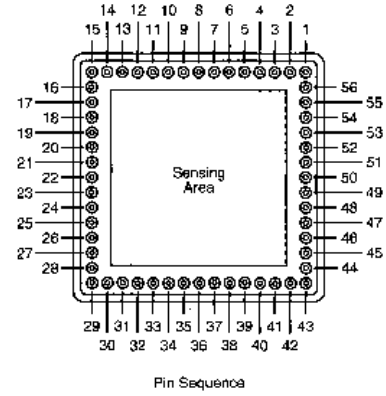
Absolute Maximum Ratings

Storage temperature: -150°C to +50°C

Voltages: Measured with respect to substrate pins 18, 25, 26, 46, 53 & 54

Pins 1, 2, 3, 13, 14, 15, 29, 30, 31, 41, 42, 43	0V to +25V
All other pins	-15V to +15V





Pin Sequence

Figure 7. Packaging Dimensions

Ordering Information

Grade	Maximum Point Defects	Maximum Column Defects	Maximum Cluster Defects	Unsealed Part Number	Quartz Window Part Number
1	150	8	20	RA2000JAU-020	RA2000JAQ-020
2	300	20	40	RA2000JAU-021	RA2000JAQ-021
3	600	40	80	RA2000JAU-022	RA2000JAQ-022

Defect Definition

A. Point defects - Hot, low or trap
   1. Hot pixel - a pixel with an output signal 10 times greater than average dark current.
   2. Low pixel - a pixel with an output signal 50% lower than average background near full-well.
   3. Charge trap - defect greater than 2500 electrons.

B. Other
   1. Column defect - Ten or more contiguous point defects in a single column
   2. Cluster defect - Two to nine contiguous point defects

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April 1992

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Description

EG&G Reticon's RA2048J array is a high-speed CCD imager designed to operate in the Time Delay Integration (TDI) mode. This array was designed for industrial inspection, noncontact measurement, pattern recognition, and any production line inspection tasks needing high-speed in very low light.

Key Features

- 2048 x 64 elements (integrating along the 64 elements)
- 22 µm x 27 µm picture elements
- 27 µm center-to-center spacing in x and y direction
- High dynamic range
- High charge transfer efficiency
- Effective data rates to 128 MHz
- Vertically-summed charges for increased sensitivity
- Bidirectional vertical shifting
- 16 parallel outputs per direction for high effective data rates

Packaging

Devices are packaged in 64-pin dual-inline side-brazed ceramic packages with ground and polished glass windows. The pinout configuration and pinout functions are shown in Figure 1 and Table 1 respectively. Package dimensions are shown in Figure 9.

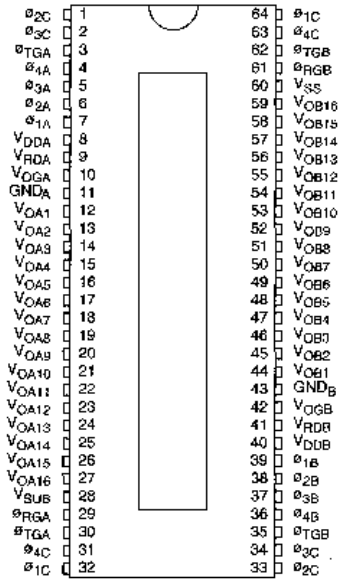


Figure 1. Pinout Configuration

Functional Description

The RA2048J TDI imager is structured in a serial-parallel-serial configuration and is intended to operate in the TDI mode. This device can also be operated as a full frame imager if shuttered.

Time Delay Integration (TDI) Mode

TDI is a known technique for increasing the sensitivity of a line scan imaging array. The RA2048J provides a series of 64 lines (linear arrays) of integration with a horizontal resolution of 2048 elements each. By synchronizing the relative motion of the image scene with the clock frequency in the vertical or transverse (TDI) direction, the charge is summed over the number of available TDI elements (64).

This mode of operation effectively increases the total array exposure time by a factor of 64, compared to a typical line scan sensor, without sacrificing the resolution or the scanning speed. The TDI mode also provides an increase in signal-to-noise ratio via an averaging down of random spatial variation of photoresponse and dark signal. The charge packets (imaging data) in the vertical registers are shifted in parallel to the serial shift register.

The image of the scene impinges on the array from the front. Photo-generated charge representing the scene will be collected in the potential wells during an integration period which corresponds to one line time. One line time equals the reciprocal of the vertical clock frequency. The charge packets are then shifted vertically to the next sequential row. As the scene is allowed to be imaged on subsequent rows, the additional charge created is summed with charge generated in previous rows. This process is repeated over the 64 TDI rows, resulting in a column of 2048 elements that have integrated for 64 line times. Information is then transferred in parallel via a transfer pulse to the horizontal shift register, to be clocked out serially within one line time. Since the subsequent line follows only one row behind, the next line scan is read out with almost no delay.

Full Frame Imaging Mode

The array information can be read out as a full-frame. When the device is operated as a full-frame imager, a mechanical shutter is needed to shield the array from incident light during the readout process. Strobed illumination could be used to simulate a shutter. Shuttering improves the performance, particularly at low data rates, by avoiding smearing.

Schematic Description

Figure 3 shows a schematic layout of the chip. The imaging area is an array of 2048 vertical 64-stage buried-channel CCD shift registers in parallel. The parallel shift registers (TDI columns) are contiguous optically and are isolated from each other by 5 µm boron-implanted channel stop regions. All readout registers are driven by the same four-phase clock. To reduce the RC time constant and response time of the long poly gates, the four phase clocks are brought in from both edges of the array. The charge handling capacity of

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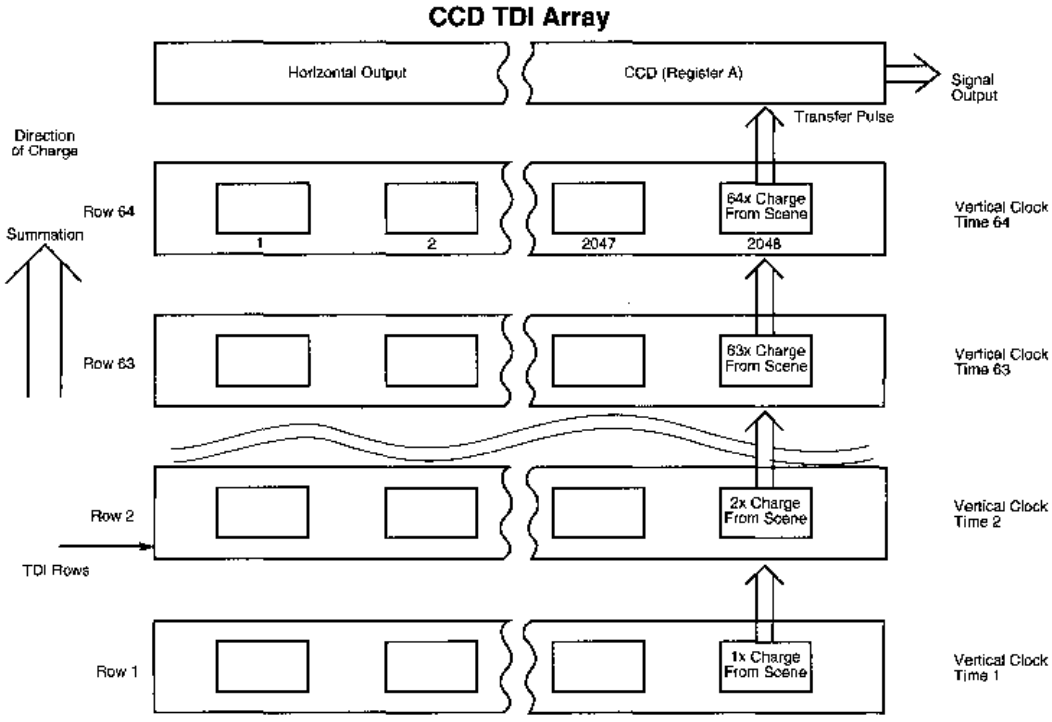


Figure 2. Image on Array Moves Relative to, and Synchronous with, Direction of Charge Transfer

each pixel is approximataley 1 million electrons. Five additional dummy shift registers are added at each end of the array to eliminate the edge effects which may cause response nonuniformity.

Output

The TDI imager is designed for high-speed imaging by using multiple output structures. There are two identical horizontal shift registers (A and B) which are driven by four-phase clocks. Shift register A is at the top and shift register B is at the bottom of the imaging area. Each shift register has its own transfer pulse, $ø_{TA}$ and $ø_{TB}$ respectively, and 16 taps (video outputs), one for every 128 x 64 elements. If the device operates at its maximum frequency of 8 MHz, this parallel output structure provides an increase in the maximum effective serial scanning rate to 128 MHz (8 MHz x 16).

Each video output tap has its own two-stage amplifier, as shown in Figure 4, which has a 3 dB bandwidth of 25 MHz and a gain of 0.75.

Geometry

The image area is an array of 2048 optically continuous columns (vertical CCD shift registers) which are isolated from each other by 5 µm channel-stop regions. Each column has 64 picture elements (pixels). The pixel size is 22 µm x 27 µm micrometers.

Operation

When vertical clocks $ø_{1C}$, $ø_{2C}$, $ø_{3C}$, $ø_{4C}$ are applied to the four phase electrodes of the vertical registers, potential wells are created beneath the high gates so that the charge can be integrated and stored in these wells. The charge can then be shifted, up into the horizontal (serial) shift register A or down into the horizontal shift register B. At the interface of the vertical and horizontal registers, a transfer gate is provided for controlling the charge flow.

The diagram in Figure 5 shows the timing needed to transfer the integrated charges from the vertical shift registers into the horizontal shift register A. The voltage transition from high (5V) to low (-8V) applied to the vertical clock will result in a transfer of charge contained under each corresponding gate to the next high gate. This, in turn, will transfer the charge to the next high gate by the same mechanism. After 64 sets of four transitions from high to low of $ø_{4C}$, $ø_{1C}$, $ø_{2C}$ and $ø_{3C}$, the charge flows through the transfer gate ($ø_{TGA}$) set high, into the high gate of the horizontal shift register ($ø_{1A, B}$) as shown in the figure. The transfer gate B ($ø_{TGB}$) is always at low state (0V) when the A register is used.

The same timing diagram is used to transfer the charge into the horizontal shift register B except that the clocks applied to the vertical shift registers, $ø_{1C}$ and $ø_{3C}$, are interchanged. An identical transfer gate clock ($ø_{TGA, B}$) is applied to the transfer gate B ($ø_{TGB}$). The transfer gate A ($ø_{TGA}$) is main-

tained at low state (0V) for this case. For horizontal clocking of register B, use ϕ_{1B} through ϕ_{4B} instead of ϕ_{1A} through ϕ_{4A}.

The output amplifier is a gated charge integrator. In this output scheme, the output node (node A in Figure 4) is reset to the DC voltage (V_{RD}) applied to the drain of the reset transistor when the reset gate clock (ϕ_{RG}) is pulsed high to turn on the reset transistor.

When $\phi_{RGA,\,B}$ is low, the reset transistor is off and the signal charge can be dumped to the capacitance of node A when $\phi_{1A,\,B}$ goes low. The charge variation of node A is then measured as a voltage at the output of the two-stage amplifier which is operated in the source-follower configuration with an external resistance load. For simplicity, the reset gate ϕ_{RGA} (ϕ_{RGB}) can be tied to ϕ_{1A} (ϕ_{1B}) to achieve the reset function. Figure 6 shows the timing relationship between $\phi_{1A,\,B}$, $\phi_{RGA,\,B}$ and video output (V_{OA}, V_{OB}).

Table 2 shows recommended operating conditions for this device.

Performance

Table 3 summarizes the performance characteristics of the device, while Table 4 lists typical clock input capacitances.

Spectral response of the RA2048J is similar to that of other CCD devices. A typical spectral response curve is shown in Figure 7.

RA2048J Evaluation Circuit

A complete evaluation circuit for the RA2048J is available from Reticon. The RC0505ANN board provides the user with an easy means of evaluating the operation and performance of the RA2048J. The board measures 4.5" x 9.3", requires +5V and ±15V supplies, and can be adjusted for pixel rates of up to 8 MHz per output tap.

Further details can be obtained from the RC0505ANN manual.

One Directional Option

The RA2048J array can be purchased with either two directional or one directional shifting, depending on the user's application. If the one directional option is chosen, the functional side (A or B) is indicated by a dot on the edge of the package, (see Figure 8).

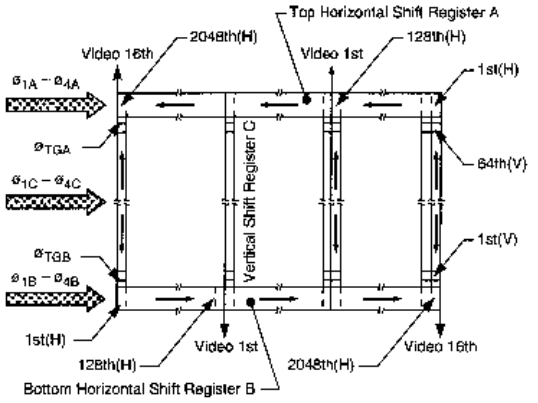


Figure 3. Schematic Layout

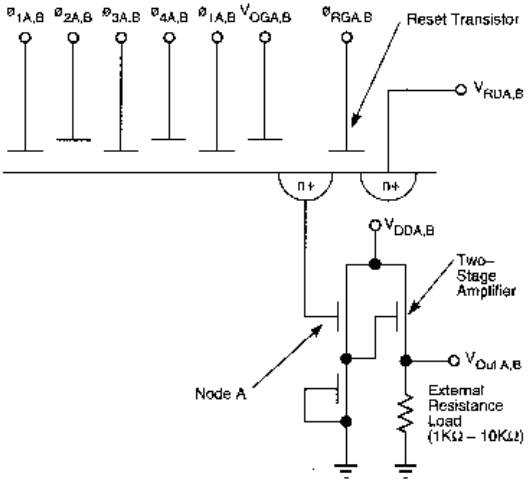
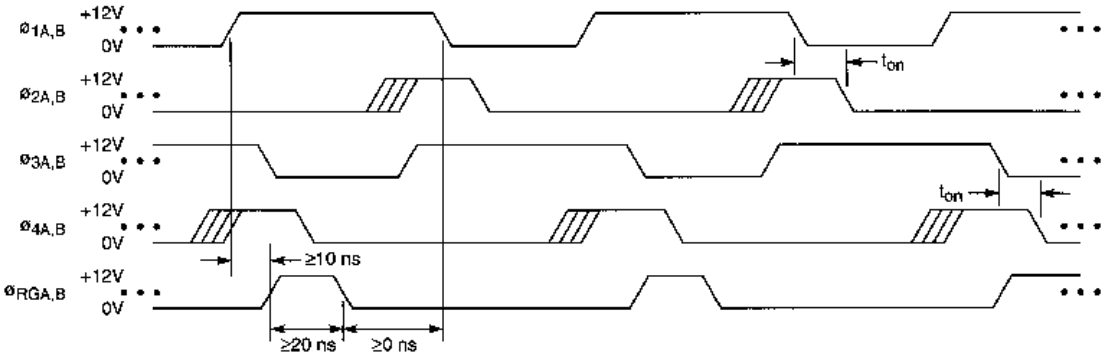
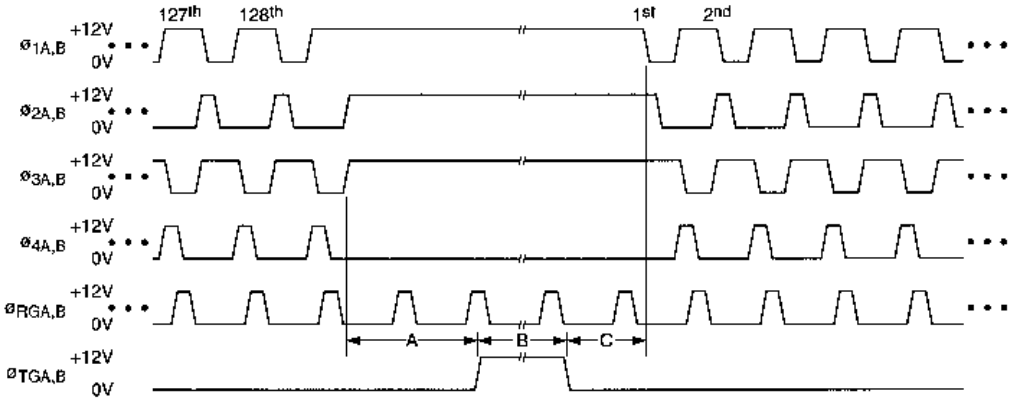


Figure 4. Output Charge Detection Circuitry (2 Stage Amp)



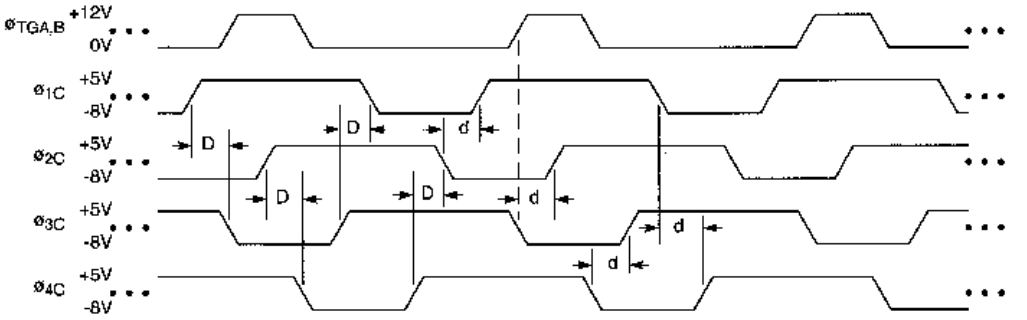
$ø_{1A,B}$ and $ø_{3A,B}$ must be crossing ≥80%; $ø_{2A,B}$ and $ø_{4A,B}$ can be nonoverlapping or may cross from 0% to 50%.

(a) Horizontal Timing



A ≥0.5 µs B ≥3 µs C ≥0.5 µs

(b) Line Timing



D ≥1 µs d ≥1 µs

(c) Vertical Timing (Side A)

Figure 5. Timing Diagrams

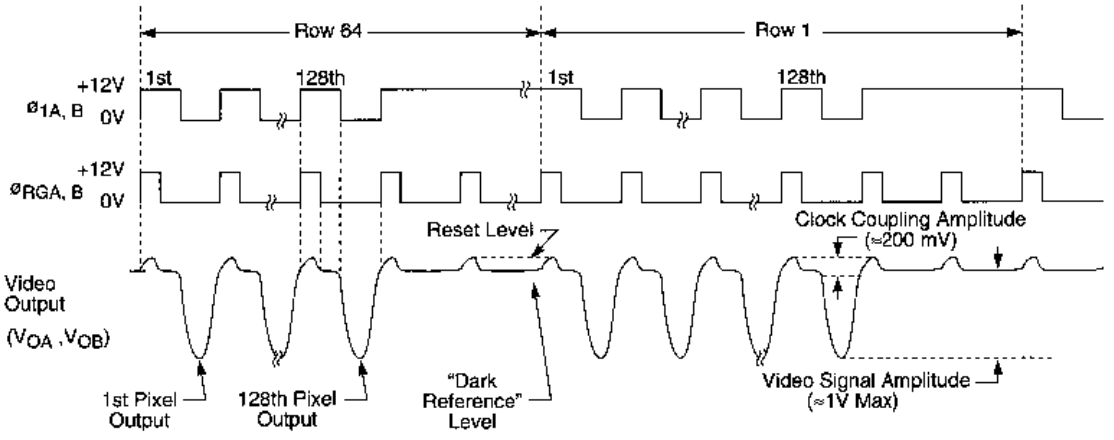


Figure 6. Timing Relationship between $ø_{1A, B}$, $ø_{RGA, B}$ and Video Output (V_{OA}, V_{OB})

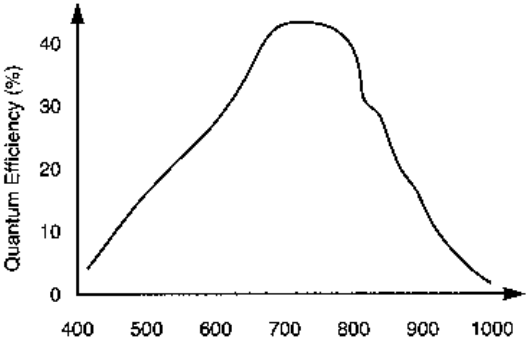


Figure 7. Typical Quantum Efficiency

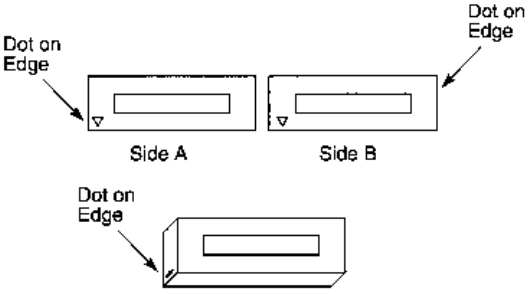


Figure 8. One Directional Option

Table 1. Pinout Functions for the RA2048J

Pin #	Sym	Function	Register
1, 33	ϕ_{2C}	TDI vertical phase 2	C
2, 34	ϕ_{3C}	TDI vertical phase 3	C
3, 30	ϕTGA	Transfer Gate (top)	A
4	ϕ_{4A}	Horizontal phase 4	A
5	ϕ_{3A}	Horizontal phase 3	A
6	ϕ_{2A}	Horizontal phase 2	A
7	ϕ_{1A}	Horizontal phase 1	A
8	V_{DDA}	Drain supply - amplifier	A
9	V_{RDA}	Drain supply - reset transistor	A
10	V_{OGA}	Output bias gate	A
11	Gnd-A	Amplifier ground	A
12-27	V_{OA1}-V_{OA16}	1st-16th video output	A
28	V_{SUB}	Backside contact	
29	ϕ_{RGA}	Reset gate clock	A
31, 63	ϕ_{4C}	TDI vertical phase 4	C
32, 64	ϕ_{1C}	TDI vertical phase 1	C
35, 62	ϕ_{TGB}	Transfer gate (bottom)	B
36	ϕ_{4B}	Horizontal phase 4	B
37	ϕ_{3B}	Horizontal phase 3	B
38	ϕ_{2B}	Horizontal phase 2	B
39	ϕ_{1B}	Horizontal phase 1	B
40	V_{DDB}	Drain supply - amplifier	B
41	V_{RDB}	Drain supply - reset transistor	B
42	V_{OGB}	Output bias gate	B
43	Gnd-B	Amplifier ground	B
44-59	V_{OB1}-V_{OB16}	1st-16th video output	B
60	V_{SS}	Top side common	
61	ϕ_{RGB}	Reset gate clock	B

Table 2. Recommended Operating Conditions

Parameter	Supply		Voltage **		
			Min	Typ	Max
DC supply	V_{DD}		11	12	13
Reset drain bias	V_{RD} *		11	11.5	12
Output gate bias	V_{OG}		3.8	4.7	7
Transfer gate clock	ϕ_{TG}	(Low)		V_{SUB}	
		(High)	11	12	13
Horizontal clocks	$\phi_{A, B}$	(Low)		0	
		(High)	11	12	13
Vertical clock	ϕ_C	(Low)	-7	-7.5	-8.0
	ϕ_C	(High)	4	5	6
Ground voltage	GND			0	
Substrate bias	V_{SS}		-2.5	-3.0	-5.0
	V_{SUB}		-2.5	-3.0	-5.0
Reset gate clock	ϕ_{RG}	(Low)		0	
		(High)	11	12	13

* To maximize charge transfer efficiency, $V_{RD} = \phi_{RG}$ -1V

** For best performance, operate at typical

Table 3. Array Performance Characteristics in the Circuit Shown In Figure 5 (Temperature 25°C, Fish Schurman 1 mm Thick HA-11 IR Filter Used, Device Operated in TDI Imaging Mode)

		Min	Typ	Max	Unit
DR_{rms}	Dynamic range [1]		5500:1		
Esat	Saturation exposure [2]		4.3		nJ/cm^2
R	Responsivity [2]		.230		$V/nJ/cm^2$
PRNU	Photo response nonuniformity [2, 3]		±5	±12	%
	Tap to tap [2, 4]		±7	±17	%
V_{DA}	Dark signal [5]		.07	1.0	%
V_{sat}	Saturation output voltage [2]	0.8	1.0		V
N_{p-p}	Peak-to-peak noise		1		mV
R_{DC}	DC reset level [6]		4.2		V
D_{DC}	DC dark level [6]		3.8		V
P_{DC}	DC power dissipation [6]		600		mW
f_{clock}	Operating frequency			8	MHz
QE	Quantum efficiency [7]		42		%
CTE	Charge transfer efficiency	.99990	0.99995		
	Max line rate per second			53,000	

Notes:

1 Defined as V_{sat}/N_{rms}, where $N_{rms} = Np\text{-}p/5$ @ 1 MHz

2 Measured with a 2870°K tungsten light source with HA-11 filter

3 Measured at about 50% V_{sat}. First elements of every tap are ignored and also the last element of tap 1
+ NU% = $(V_{max} - V_{avg})/V_{avg} * 100$
- NU% = $(V_{avg} - V_{min})/V_{avg} * 100$

4 Defined as +NU% = (Maxavg - Avg)/Avg * 100 and -NU% = (Avg - Minavg)/Avg * 100, where
Avg = (Tap1avg + Tap2avg . . . + Tap16avg)/16

5 Measured at 25°C with 312 µs integration time

6 Measured with no illumination

7 At 700 nm

Table 4. Typical Clock Capacitance *

Clock	Capacitance (pf)
$ø_{1A} = ø_{1B}$	550
$ø_{2A} = ø_{2B}$	400
$ø_{3A} = ø_{3B}$	400
$ø_{4A} = ø_{4B}$	320
$ø_{1C} = ø_{3C}$	460
$ø_{2C} = ø_{4C}$	260
$ø_{RGA} = ø_{RGB}$	110
$ø_{TGA} = ø_{TGB}$	180

* measured at 10V bias

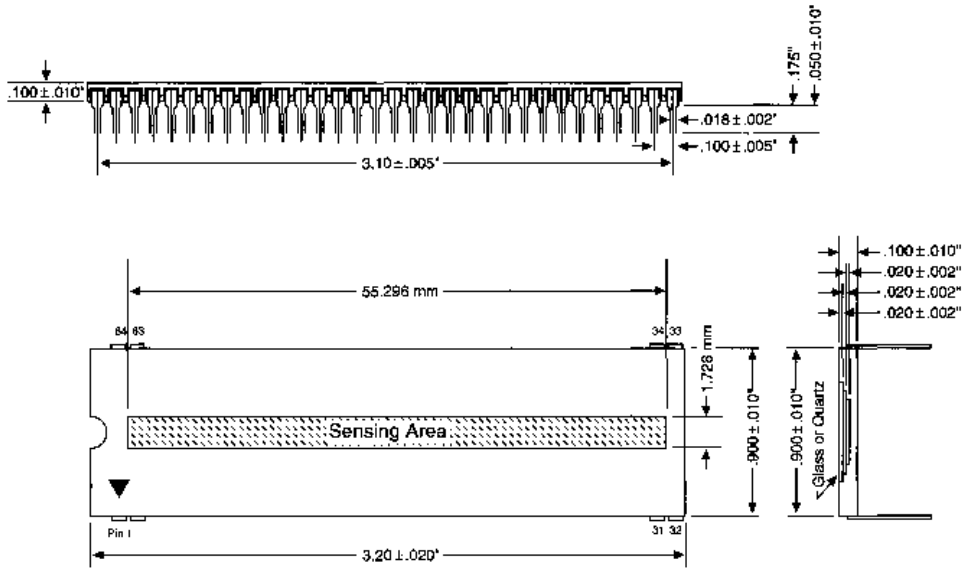


Figure 9. Package Dimensions

Ordering Information

Ordering Number	Device	Evaluation Circuit
RA2048JAG-011 RA2048JAG-020	Bidirectional One directional	RC0505ANN-011

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Circular Arrays

RO0720B

General Description

The RO0720B is a high resolution circular solid state scanner designed specifically for applications such as focusing, tracking, angle discrimination, etc. This monolithic integrated circuit contains a circular array of 720 photodiodes at 0.5° spacing and is available in two aperture versions, .2 and 1.9 mm, designated the RO0720BAG and RO0720BJG, respectively. These arrays are packaged with a ground and polished glass window.

Equivalent Circuit

The package and pin configuration is shown in Figure 1 and a simplified equivalent circuit is shown in Figure 2. The actual array is circular with the No. 1 diode at right center (scan is clockwise), and with the last diode physically adjacent to the first diode (Figure 1). The array may be operated in either a self-start or external start mode. The self-start mode permits uninterrupted circular scan and is accomplished by buffering the End-of-Scan output with external circuitry and connecting it to the start input. The external mode may be used to obtain longer integration time, much as in a linear array.

Each cell consists of a photosensor with an associated junction capacitance and is connected through an MOS transistor switch to a common video output line. The switches are turned on and off in sequence by the shift-register multiplexing circuits, thereby periodically recharging each cell to 5V and storing approximately 5 pC on its capacitance.

The multiplexing circuits are driven by four clock phases which are easily generated from a TTL master clock which sets the cell-to-cell sampling rate. During the cycle scan time, the charge on each junction capacitor is gradually removed by the reverse current flowing in the associated photodiode.

The reverse current is made up of two components: the photocurrent and the dark leakage current (the latter is typically 1 pA per pixel at room temperature). The photocurrent is proportional to the light intensity or irradiance. During a scan time, the charge removed from each cell is the product of the photocurrent and the scan time. This charge must be replaced through the video line when the diode is sampled once each scan. Thus, the output signal obtained from each scan of an N-element array is a train of N charge pulses, each proportional to the light exposure on the corresponding photodiode.

In addition to the signal charge, switching transients are capacitively coupled into the video line by the multiplex switches. The RO0720B has associated with each sensing diode a dummy diode covered with an opaque mask. Transients similar to those introduced into the video line are introduced into the dummy video line and, therefore, can be nearly eliminated and a cleaner signal recovered by reading out the video and dummy lines differentially.

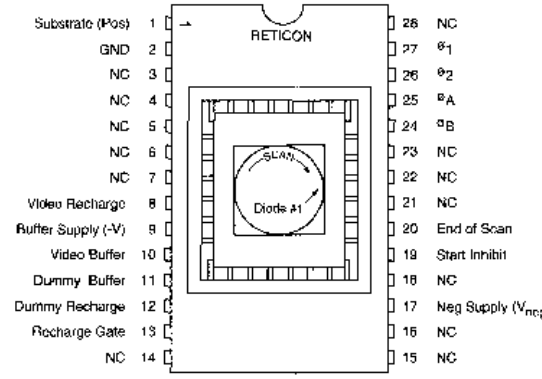


Figure 1. Pinout Configuration

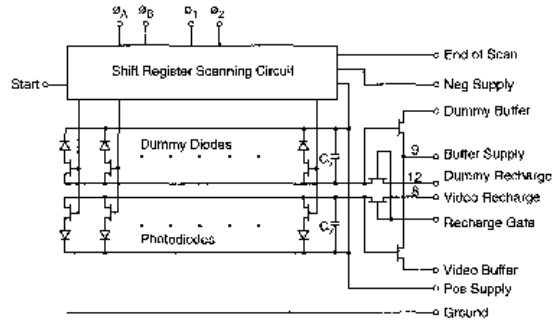


Figure 2. Simplified Equivalent Circuit

Sensor Geometry

In the RO0720B circular scanners the light-sensing area is a long, circular region defined by an aperture in an opaque mask. Bar-shaped photodiodes extend across the aperture and are connected to the multiplex switches buried under the mask. The entire aperture is photosensitive; photocurrent generated by light incident between the photodiodes will usually be collected by the nearest diode. Figure 3 shows simplified aperture geometry along with an idealized response function, which would be obtained by scanning a point source of visible light along the length of the aperture. The dimensions a, b, and c indicated in Figure 3 are as follows for the RO0720BAG: the photodiode width *a* is 20 µm, the center-to-center spacing *b* is approximately 30.1 µm at the inside radius, and the aperture width *c* is 200 µm. Refer to the Array Mechanical Characteristics and Figure 4 for detailed geometry of both the RO0720BAG and the RO0720BJG.

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If the full angular resolution of 0.5° is not required, the array may be operated with simplified clock drive and 1° resolution. In this mode, the A and B clocks are both connected to V_{neg}; performance is otherwise similar except individual diode output charge is doubled and resolution halved. Clock generation is also simplified.

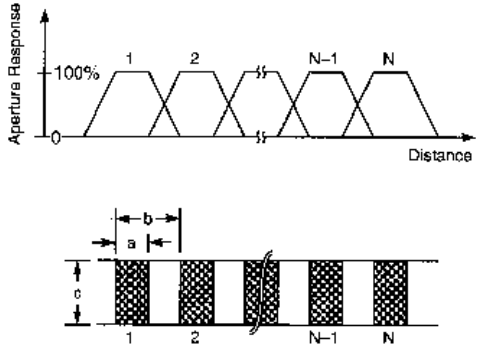


Figure 3. Sensor Geometry and Idealized Aperture Response Function

Sensitivity and Spectral Response

The spectral response of the RO0720B is similar to that of other high-quality silicon photodetectors, covering the range from the near UV to the near IR. Relative spectral response is shown as a function of wavelength in Figure 5. Note that relatively high responsivity is maintained even in the blue end of the spectrum because there is no interfering structure covering the diode. Since many applications involve use of visible light, sensitivity and uniformity of response are specified using a source with the spectral distribution shown in the dotted line of Figure 5. This spectral distribution is produced by filtering a 2870°K tungsten source with a Fish-Schurman HA-11 heat-absorbing 1 mm thick filter.

Since Reticon scanners operate in the charge-storage mode, the charge output of each diode (below saturation) is proportional to exposure, i.e., the irradiance or light intensity multiplied by the integration time or the time interval between successive start pulses. Thus, there is an obvious trade-off between scanning speed and the required light intensity. Plots of charge output versus exposure are shown in Figure 6 for the light source of Figure 5.

Dark Response and Dynamic Range

There are three components to the dark output signal from a Reticon scanner: (1) the integrated dark leakage current, (2) the fixed pattern caused by incomplete cancellation of clock switching transients between the sensing and dummy diodes, and (3) the random (thermal) pixel noise.

The dark leakage current will vary significantly from element to element but is typically 1 pA per diode at room temperature. Assuming this value, leakage current would contribute an output charge of 4 pC with a four second line time. Thus, dark current will contribute about 1% of saturated output signal for t_L = 40 ms, 0.1% for t_L = 4 ms, and so on. The dark current is a very strong function of temperature, approximately doubling every 7°C. Thus, the maximum allowable

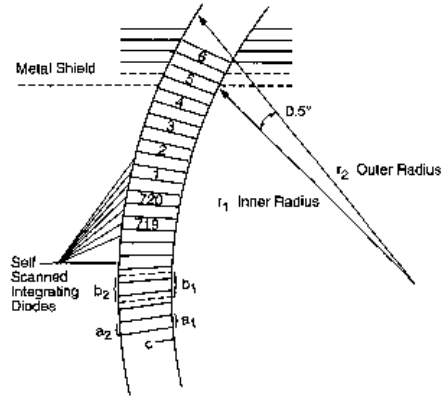


Figure 4. Geometry for the RO0720B Array

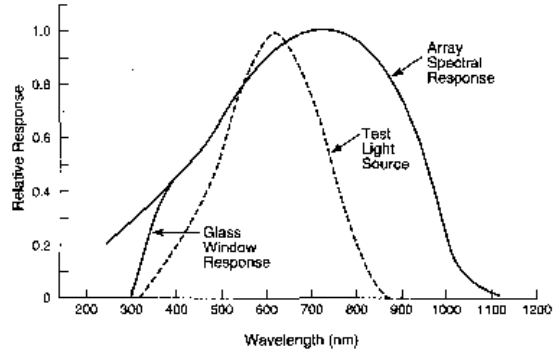


Figure 5. Relative Spectral Response as a Function of Wavelength. Dotted line shows distribution of light source for performance measurements.

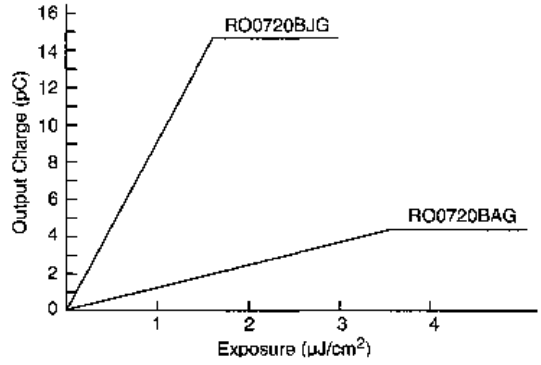


Figure 6. Signal Charge Per Cell as a Function of Exposure for Light Source of Figure 5

scan period becomes correspondingly shorter at high temperatures and longer at low temperatures. An important feature of these devices is the low power dissipation, which means that self-heating is negligible.

The switching transients are very nearly cancelled by the differential output. Residual uncancelled transients will result in a fixed pattern which is typically 1% of the saturated output signal for unprocessed video.

Pixel noise is the random, nonrepetitive fluctuations which are superimposed on the dark level, and is the ultimate limiting noise which cannot be removed by signal processing. Its rms value will generally be amplifier-limited at a value less than about 0.1% of the saturation level, depending on the noise bandwidth and preamplifier used.

If the saturation level is compared to the amplitude of the dark-signal nonuniformity, the dynamic range is typically better than 100:1 for unprocessed video (refer to Array Performance Characteristics and Note 6).

If the saturation level is compared to the rms noise on each individual element, a dynamic range of greater than 1000:1 can be achieved with these devices.

Drive Requirements

Two power supplies to the array are required—nominally +5 and -10 volts. Four clock phases are required to drive the RO0720B and a properly timed start pulse is required to initiate each scan. Figure 7 shows the proper timing of the input clock and start signals. Note that ϕ_1 and ϕ_2 are complementary square waves. The ϕ_A and ϕ_B clocks are complements, but are not square waves. Pixel diodes are sampled on the negative-going transitions of ϕ_2, ϕ_B, ϕ_1, ϕ_B, ϕ_2, ϕ_B, etc. The start-pulse timing is noncritical except that it must be negative at least 50 ns before one positive-going transition of ϕ_1 and holding beyond ϕ_1's rise by a minimum of 50 ns. The number of master clock periods between start pulses is arbitrary except that it must be equal to or greater than 720.

A suitable drive circuit for the RO0720B is shown in Figure 8.

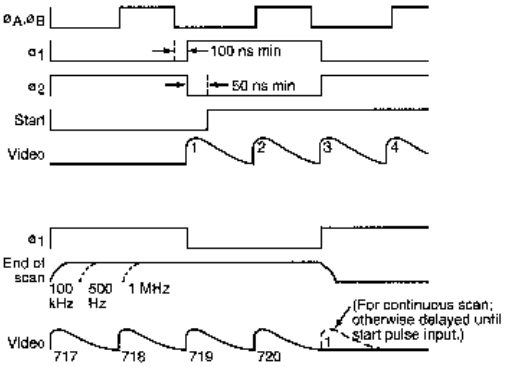


Figure 7. Timing Diagram

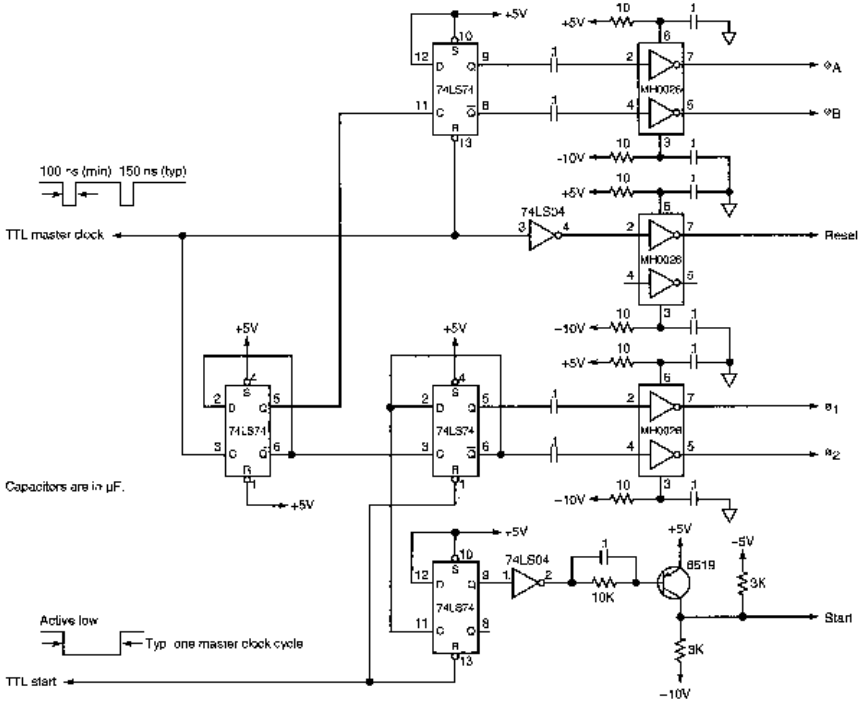


Figure 8. Drive Circuit

Signal Extraction

The video output of the RO0720B is a train of 720 charge pulses flowing onto the video-recharge-line and dummy-recharge-line capacitances during each scan with timing as shown in Figure 7. The pulses on the dummy line contain switching transients only; those on the video line contain switching transients plus the video signal. An output circuit is required which is capable of differentially amplifying these pulses to a usable voltage level. Two types of amplifier circuits are in common use: (1) a simple differential current amplifier, and (2) video-line integrate, with reset. The latter typically will be followed by a sample-and-hold circuit which can provide a greater signal-to-noise ratio.

Current Amplifier. The video signal may be amplified using an op amp connected as a differential amplifier. A suggested circuit is shown in Figure 9. In this mode, the recharge gate is biased ON by connecting it to the negative supply and the signal is obtained through the video and dummy recharge lines. The unused buffer amplifiers are biased OFF by connecting all pins to the positive supply. An example of the video output of the circuit of Figure 9 is shown in the oscilloscope photograph of Figure 11.

Videoline Integrate, with Reset. This alternative signal-processing scheme makes use of the internal buffer amplifiers and recharge switches. Immediately after the multiplex switch is closed to sample a diode, the voltage change on the video line is sensed through the buffer amplifier. The recharge gate is then pulsed negative to reset the video line before the next diode is sampled. This circuit configuration is shown in Figure 10.

End of Scan

An output pulse is provided when the last four diodes are sampled. The end-of-scan (EOS) output is provided primarily for test purposes, but it may be used for positive synchronization of the start sequence, or for self-starting in the continuous-scan mode. The waveforms are comparatively slow, so that external pulse shaping is ordinarily required. (Refer to EOS waveform, Figure 7.)

When not in use, the EOS output should be connected to the positive supply to avoid introduction of unwanted "glitches" into the video. When EOS is used, it is recommended that voltage excursions on the EOS terminal be minimized. Figures 9, 10, and 13 have different buffers; amplifier circuits shown for the EOS output and the circuit selected for a given application are dependent on the user's requirements. The circuit in Figure 13 can be used when the EOS output is connected to the start input to give an uninterrupted circular scan, with the first element interrogated immediately following the last element. Some accessory circuit boards, notably the RO0720B board, are not capable of functioning in this manner (without modification) because of a built-in flyback interruption that occupies a minimum of eight counts.

Evaluation Circuit Board, RC0720B

The RC0720B evaluation circuit board which contains all required drive and amplifier circuitry for operation of the RO0720B is available from Reticon. The circuit provides a high-quality sampled-and-held output as shown in Figure 12 and is highly recommended for first time array evaluation.

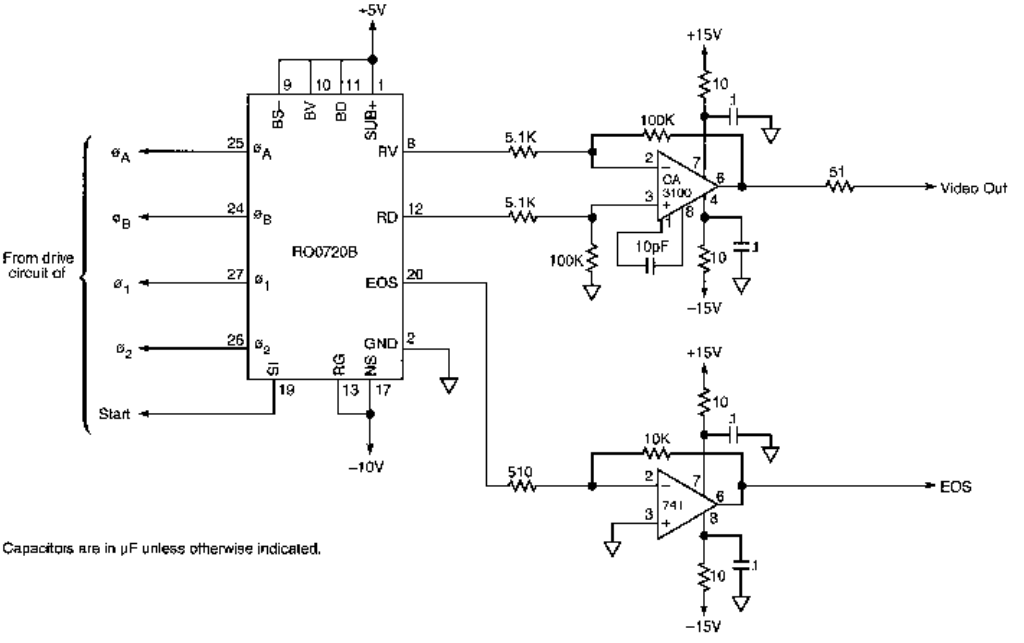


Figure 9. Suggested Current Amplifier Circuit

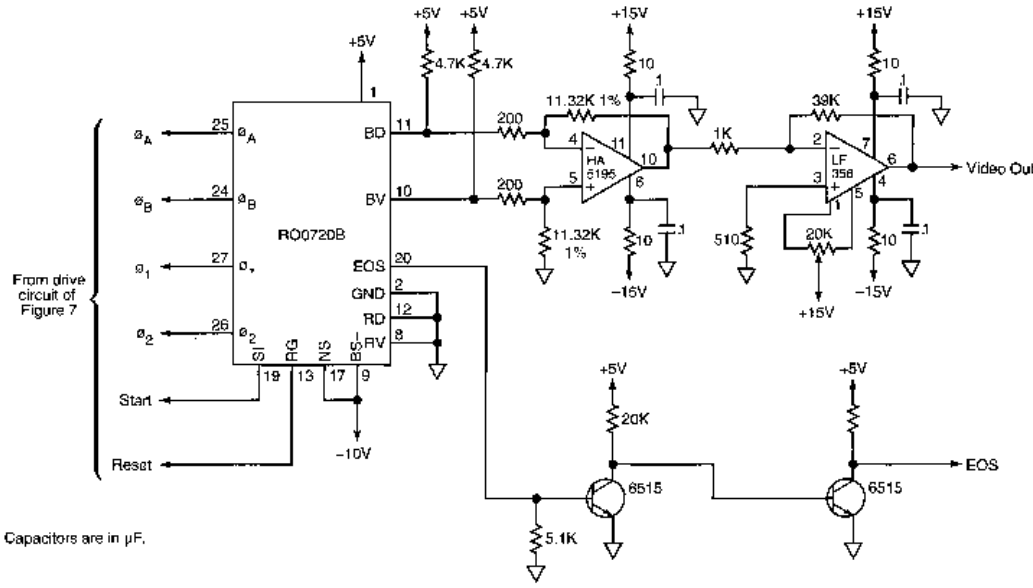


Figure 10. Video Line Integration Differential Amplifier Circuit (Sample-and-Hold Circuit not shown)

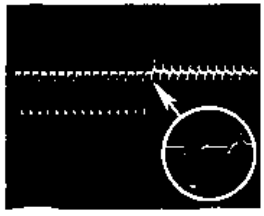


Figure 11. Oscilloscope Photo Showing Output of Figure 9

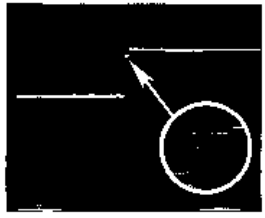


Figure 12. Oscilloscope Photo Showing Video Output of Integrate Sample-and-Hold Amplifier

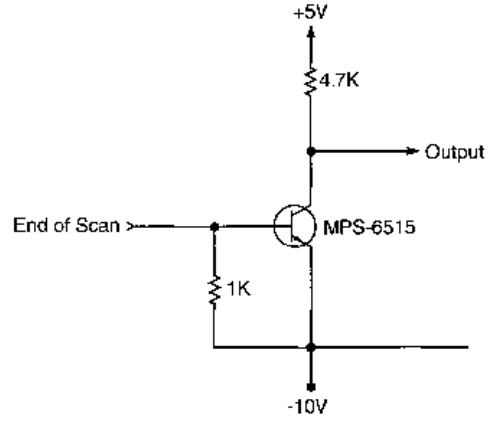


Figure 13. Suggested End-of-Scan Output Circuit

Table 1. Array Mechanical Characteristics
(Refer to Figures 4 and 13)

	RO0720BAG	RO0720BJG	Units
Number of diodes	720	720	
Center-to-center spacing			
at inner radius (b_1)	30.1	15.3	µm
at outer radius (b_2)	31.9	31.9	µm
Aperture inner radius (r_1)	3.45	1.75	mm
Aperture outer radius (r_2)	3.65	3.65	mm
Aperture width (r_2 - r_1) = C	.2	1.9	mm
Diode diffusion width			
Inner radius (a_1)	20	.5	µm
Outer radius (a_2)	20	20	µm

Table 2. Array Performance Characteristics (23°C)

Parameter	Min	Typ	Max	Units
Sensitivity				
BAG [1]		11		pC/µJ/cm^2
BJG [1]		91		pC/µJ/cm^2
Non-uniformity of response (NUS) [1,2]		10	15	±%
Saturation exposure				
BAG		.35		µJ/cm^2
BJG		.16		µJ/cm^2
Saturation charge				
BAG		3.9		pC
BJG		14.6		pC
Dynamic range				
DR_{RMS} [3]		2000		rms
DR_{FPN} [4]	100	200		

Notes:
1 Using light source of Figure 5.
2 Measured with uniform illumination at approximately 50% saturation. Neglects first 2 and last 2 diodes.
3 Defined as saturated output to RMS pixel noise.
4 Defined as saturated output to peak-to-peak dark fixed pattern.

Table 3. Electrical Characteristics (23°C)

Parameter	Min	Typ	Max	Units
Positive supply voltage V_P [1]	4.5	5	5.5	V
Clock voltage high V_{CH}	V_{P-1}	5	V_P	V
Clock voltage low V_{CL}	-10	-10	-6.5	V
Start voltage high V_{SH}	V_{P-1}	5	V_P	V
Start voltage low V_{SL}	-10	-10	-5	V
Sample frequency f_S			1	MHz
Clock input capacitance [2] (Phases 1 and 2)		45		pF
Clock input capacitance [2] (Phases A and B)		37		pF
Video line capacitance C_V [2] (Pins 4 and 9 tied)		45		pF
Dummy line capacitance C_D (Pins 8 and 9 tied)		47		pF
Buffer output capacitance C_B		2		pF
Recharge gate capacitance (Pin 9)		3		pF
End of scan capacitance		2		pF

Notes:
1 No terminal should ever be allowed to go more positive than V_P.
2 Measured at 5V bias.

Absolute Maximum Ratings

	Min	Max	Units
Voltage on any terminal	V_P-20	V_P	V
Storage temperature	-55	+125	°C
Temperature under bias	-55	+85	°C

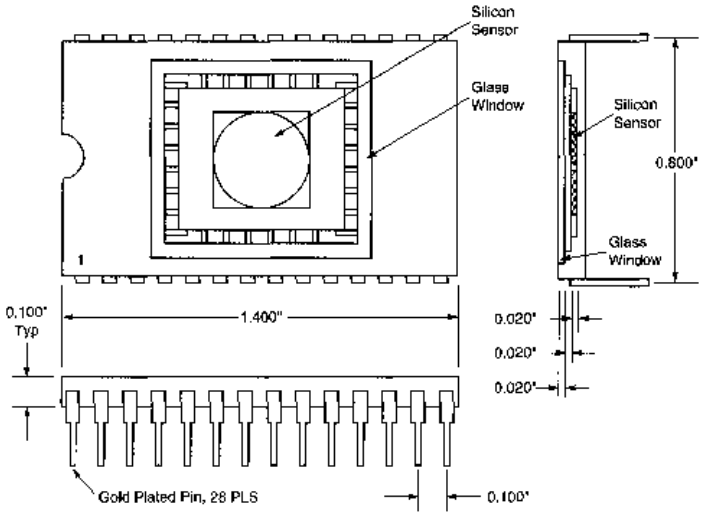


Figure 14. Package Dimensions

Ordering Information *

Part Number	Evaluation Circuit
RO0720BAG-011	RC0720ONB-011
RO0720BJG-011	RC0720ONB-011

* Includes standard arrays. For all options, consult your local sales office.

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IR Arrays

RA0128NIU
SI Series

Introduction

Reticon has successfully combined the advantages of thin film PtSI SBD technology with our standard photodiode arrays to produce a 128 x 128 monolithic area array which is sensitive in the mid-infrared (MIR) spectral region. The platinum silicide Schottky barrier diode (PtSi SBD) is the most practical and cost effective technology for providing high resolution infrared staring focal plane arrays (FPA) for both industrial and military applications.

The 128 x 128 PtSi FPA is backside illuminated and is sensitive in the 1 to 5.5 µm spectral range. Visible and near infrared photons are absorbed in the silicon before they reach the photo-detector area, and long-wavelength IR (LWIR) photons create holes with insufficient energy to jump the metal-semiconductor (Schottky) Barrier. With backside illumination, the array is sensitive to wavelengths from 1 to 5.5 µm without the need for external filters. Applications include noncontact temperature monitoring for industrial and medical uses, missile seekers, surveillance, tracking, process control, and nondestructive testing.

Key Features

- High resolution: 128 x 128 elements
- High fill factor: 59% with a 60 µm x 60 µm pixel size
- Two horizontal readout registers for high speed imaging
- High frame rate: greater than 450 frames/sec
- Spectral response: 1 to 5.5 µm
- Excellent element-to-element uniformity: 0.5% rms
- High video sampling rates: up to 10 MHz pixel rate
- On-chip pre-amplifer and reset structure
- High electron sensitivity: 0.7 µV/e^-
- Wide dynamic range ≥1000:1 rms
- Backside illumination provides inherent (visible and near infrared) filtering
- 28-pin dual-inline ceramic package

Description

The 128 x 128 PtSi FPA has 16,348 pixels arranged in a matrix of 128 rows by 128 columns. Each pixel has a fill factor of 59% and is 60 µm x 60 µm. The chip dimensions are 433 mil x 453 mil of which 302 mil x 302 mil is the sensing area. This device is provided in a standard 28-pin dual-inline ceramic package, (see Figure 7), which accommodates backside illumination of the chip and simplifies cryogenic cooling. Figure 1 shows the pinout configuration and Table 1 shows the pin description of the 128 x 128 PtSi FPA.

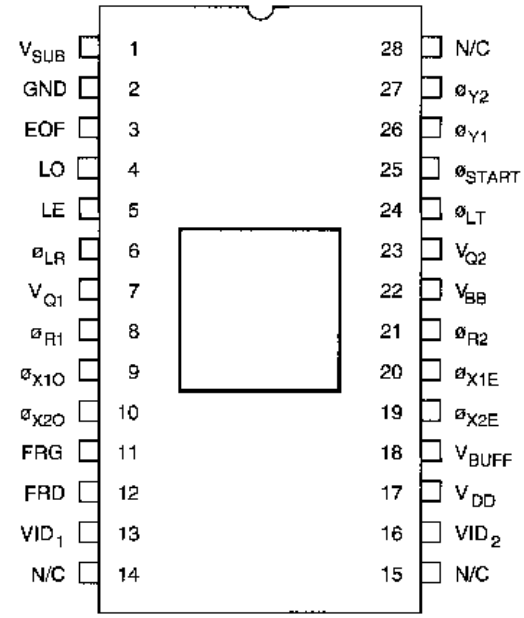


Figure 1. Pinout Configuration

The array can be scanned with pixel readout rates up to 10 MHz to yield frame rates greater than 450 frames/sec. Each line of photodiodes is parallel loaded into two high speed bucket-brigade device (BBD) analog shift registers and then sequentially shifted out. The outputs of the two BBDs can then be easily multiplexed externally to reconstruct the line information. The entire frame of 128 lines may be sequentially accessed, or just the odd or even lines may be read out. If the output of one BBD is used and just the even or odd lines are accessed, a frame will contain every other pixel in 64 lines for a 64 x 64 array. The time between the readout of a pixel, one frame period, is the integration time.

The devices are fabricated using an advanced double poly NMOS process. Each device consists of several functional elements to control the operation of the device, as shown in Figure 2. The functional elements are described in the following paragraphs.

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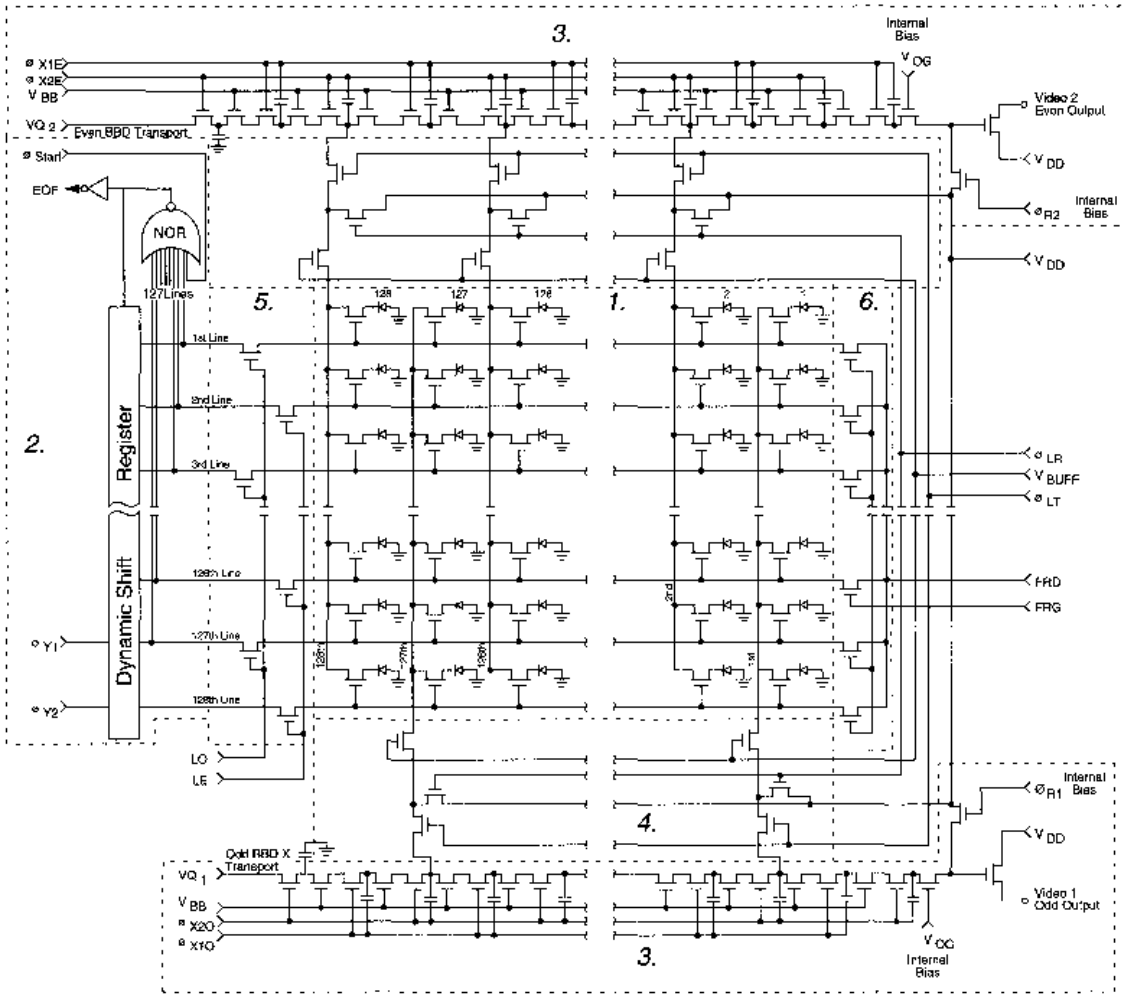


Figure 2. Schematic Diagram RA0128NIU

Photodiode Array

The first element consists of a 128 x 128 Schottky barrier photodiode array, schematically indicated by the columns and rows (lines) of individual photodiodes. Each diode in a column is connected through a multiplex switch to a column video line, which is common to all diodes in that column. The gates of all the multiplex switches in a row (line) are connected together, so that when a row of multiplex switches is turned on, the signal in a row of diodes is transferred simultaneously to the 128 column video lines. When a diode is selected by the multiplex switch, the potential of the diode will be reset to a value of (V_{GM} - V_{TM}), where V_{GM} and V_{TM} represent the clock high voltage and threshold voltage of the multiplex switch, respectively. The signal charge removed from the selected diode will be transferred through the column video line into the BBD for readout. After the multiplex switch is turned off, the diode starts to integrate the photon-generated charge. The total integration time of each diode is the time between two consecutive readouts of the same diode.

Dynamic Shift Register

The second element consists of a two-phase (2ø) dynamic shift register. The shift register turns on each row (line) of multiplex switches in sequence, allowing the photodiode charge to transfer through each column video line into the appropriate BBD. The dynamic shift register is driven by two-phase clocks denoted by $ø_{Y1}$ and $ø_{Y2}$ in Figure 2. Odd lines are accessed while $ø_{Y1}$ clocks are high, even lines while $ø_{Y2}$ is high. The dynamic shift register can be self-starting if fast consecutive frames are desired, or it can be controlled by an external start pulse ($ø_{Start}$). These functions are performed by a "NOR" circuit. Tied to each output of the shift register (except for the 128th position) are inputs to a NOR gate. When there is an output from any of the 127 output positions, the NOR gate keeps the shift register from restarting. Once the bit occupies the last position, the NOR gate's output goes high and the shift register starts again with the rising edge of $ø_{Y1}$. The $ø_{Start}$ is also connected to the NOR gate. It can be used to inhibit the register from starting by pulling $ø_{Start}$ to V_{DD}. The shift register will not start to access lines until both $ø_{Start}$ and the outputs from lines 1 - 127 are low.

The NOR gate output is connected to an external pin, EOF (End of Frame), through an open drain inverter. This output is normally tied to V_{DD} through a 3KΩ resistor. When there is a bit in any row except the last, or if $ø_{Start}$ is active, EOF will remain high. It goes immediately low on the rising edge of $ø_{Y2}$ if $ø_{Start}$ is low, and none of the rows 1 - 127 are active.

Bucket-Brigade Device Analog Shift Register

Two bucket-brigade analog shift registers accept the signal from the column video lines and shift it out sequentially to two output amplifiers. Each BBD is driven by a two-phase clock, denoted by $ø_{X1}$ and $ø_{X2}$ in Figure 2. A "fat zero" input port is provided to improve the transfer efficiency of the register. The outputs from both BBD registers are multiplexed off-chip to obtain one line of combined video information.

As shown in Figure 2, there are several other terminals associated with the two BBD registers. V_{BB} is the tetrode-gate bias that is biased at a DC voltage a few volts below the $ø_{X1}$ and $ø_{X2}$ high level. V_{Q1} and V_{Q2} are the input bias for the "fat zero" input port. These inputs control the bias level in the dark. Normally, these terminals are biased to approximately 10V; however, when the odd and even videos are summed together, either input bias voltage may be used to adjust the corresponding dark-level output to remove the odd-and-even pattern. Figure 4 shows the relationship between the output dark signal level and V_{Q1}, V_{Q2} bias voltage. The shaded area represents the optimum bias range. $ø_{R1}$ and $ø_{R2}$ are the reset clocks for the output amplifiers, which are shown in Figure 2 at the outputs of both bucket brigades. On the even side, the signal appears at the gate of the output amplifiers when $ø_{X1}$ drops to a low potential. While $ø_{X1}$ is high and before the next sample appears, this node is cleared by charging it to the reset voltage, V_{DD}. This

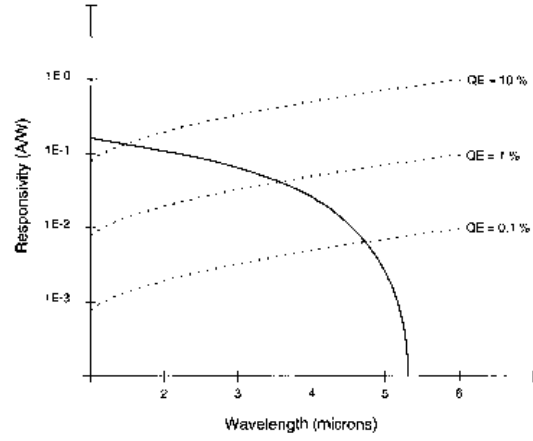


Figure 3. Spectral Response

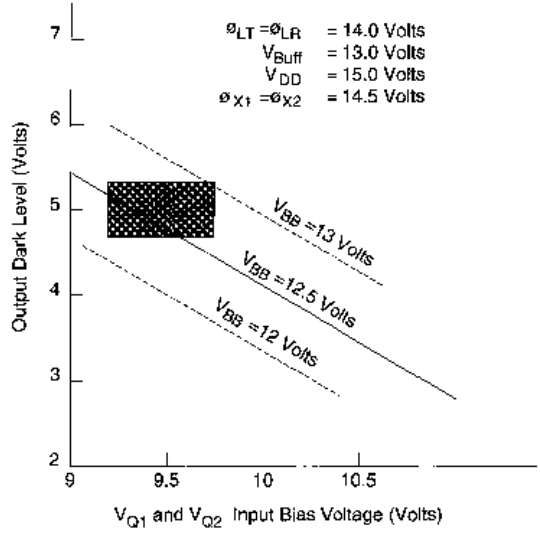


Figure 4. Operation Range of V_{Q1}, V_{Q2} Bias

can be easily done if $ø_{R2}$ is clocked synchronously with $ø_{X1}$. The complementary situation applies to the odd video output, with signal appearing while $ø_{X2}$ is low, and reset while $ø_{X2}$ is high. Normally, the synchronous relationship is obtained by direct connection of $ø_{X1}$ to $ø_{R2}$, and direct connection of $ø_{X2}$ to $ø_{R1}$.

VID_1 and VID_2 are the respective odd and even video output terminals. The video output is that of a source follower. Normally, the output of each source follower is terminated by a 3KΩ resistor to ground. This configuration provides the proper bias current for the source follower.

Line Transfer (ϕ_{LT}), Line Reset (ϕ_{LR}) and Buffer Gate (V_{BUFF})

The fourth functional element consists of a video line reset switch, ϕ_{LR}; a line transfer switch, ϕ_{LT}; and a buffer gate, V_{BUFF}. The line reset switch, ϕ_{LR}, provides a reference bias for all the video lines while all the sensor diodes are integrating signal charges. All the charges collected from stray capacitances along the video lines and all the excess signal charges leaked from the sensor diodes are drained into the sink voltage, V_{DD}, through operation of the ϕ_{LR} gate. In this way, ϕ_{LR} functions as an antiblooming and anticrosstalk gate. Prior to the moment when the dynamic shift register is to select a row of diodes, the ϕ_{LR} gate is turned off and the transfer gate (ϕ_{LT}) is turned on. This prepares the video lines to accept charge from the next row of photodiodes to be transferred into the BBDs.

The bias applied to the ϕ_{LR} switch should be lower than that of ϕ_{LT}. This will prevent possible loss of signal charge through the ϕ_{LR} switch as a result of threshold voltage mismatch between the ϕ_{LR} and ϕ_{LT} transistors. The effect of different gate potentials on ϕ_{LR} and ϕ_{LT} results in adding a fixed amount of charge Qf into the video signal where $Q_f = (\Delta V_G + \Delta V_T)C_V$. These quantities ΔV_G and ΔV_T are the gate potential and threshold voltage differences of the ϕ_{LR} and ϕ_{LT} gates, respectively, and C_V is the capacitance of the video line.

To minimize Q_f, a buffer gate V_{BUFF} is introduced in front of the ϕ_{LR} and ϕ_{LT} switches. This buffer gate is biased at a DC potential below the ϕ_{LR} and ϕ_{LT} "high" potential. The function of this buffer gate is to isolate the video line capacitance C_V from the effect of ΔV_G and ΔV_T. With the introduction of this buffer gate, Q_f becomes $(\Delta V_G + \Delta V_T)C_J$, where C_J is the junction capacitance of the n^+ diffusion between ϕ_{LR} and ϕ_{LT} switches. The capacitance C_J is much smaller than C_V and results in great reduction of Q_f. Normally ϕ_{LR} is clocked synchronously with ϕ_{X2}. However, to avoid crosstalk and permit adjustment for optimum blooming control, a separate driver is used for ϕ_{LR}.

Field Select Switches LO and LE

The fifth functional element consists of the field select switches LO and LE. As evident from Figure 2, the LO input terminal controls the gates that switch all of the odd-numbered outputs from the dynamic shift register; the LE terminal controls the gates that switch the even numbered outputs. These dynamic shift register outputs in turn control the row selection. When the LO line is held at V_{DD}, the odd rows of diodes may be selected by the dynamic shift register, and when the LE line is held at V_{DD}, the even rows of diodes may be selected. The LO and LE gates are turned on by applying a high (V_{DD}) potential and are turned off by applying a low (0V) potential. For sequential scan of all 128 lines, both LE and LO are held at V_{DD}.

Frame Reset Gate (FRG) and Frame Reset Drain (FRD)

The sixth element consists of the frame reset gate FRG and reset drain FRD. These switches provide an access to the multiplex switches of all the diodes in the matrix and allows the entire frame to be reset. When the frame reset control is not being used it is held low. However, when a particular exposure is desired, this control may be used to clear the diodes by taking the FRG terminal to V_{DD}. When using the frame reset, a shutter or pulsed-light input should be used to ensure the same exposure for all the photodiodes.

There are two inputs for controlling the frame reset operation, the frame reset gate, FRG, and frame reset drain, FRD. In addition, LE and LO must be pulsed off during the reset operation. The timing sequence for this operation is shown in Figure 6. The longest of the control pulses are LE and LO. They should be held negative 200 nanoseconds longer than the frame reset gate with pulse width overlap as seen in Figure 6. The FRD can be continuously active, but within and before the trailing edge of FRG. FRD must be pulled to ground to allow the vertical shift register's multiplexing line to discharge. This is done to ensure that the multiplexing switches are off.

Device Operation

Figure 5 shows the timing diagram for the device when operated in the noninterlaced and continuous mode of operation. It requires two sets of complementary clocks, ϕ_{Y1} and ϕ_{Y2}, to drive the dynamic shift register and ϕ_{X1} and ϕ_{X2} to drive the two BBD registers. It also requires a ϕ_{LT} clock to control the charge transfer from the column video lines into the BBDs. The line reset clock, ϕ_{LR}, is for blooming control and has the same timing as ϕ_{X1}. The reset gates ϕ_{R1} and ϕ_{R2} for the

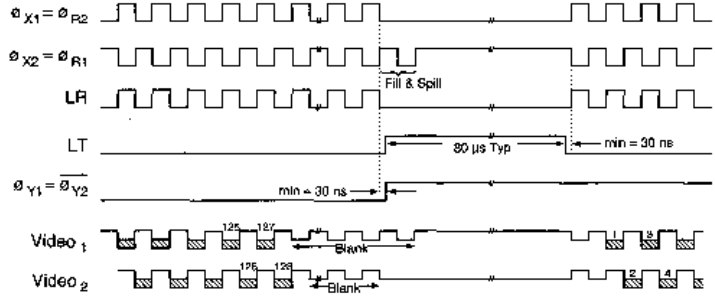


Figure 5. Timing Diagram for RA0128NIU Noninterlaced Continuous Operation

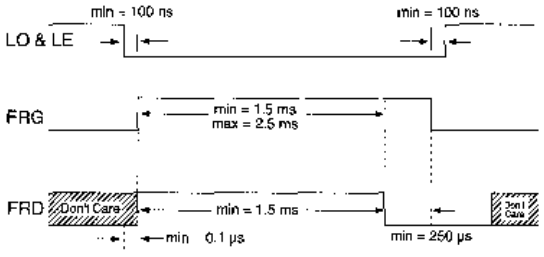


Figure 6. Timing Sequence for Frame Reset

output amplifiers are directly tied to ϕ_{X2} and ϕ_{X1}, respectively. The timing relations and rise and fall times of the various clocks are summarized in Table 3.

Before a new row of diodes is selected by the dynamic shift register, which occurs when ϕ_{Y1} and ϕ_{Y2} changes states, the line reset ϕ_{LR} should be turned off to prevent signal charge from being drained into V_{DD}. A minimum pulse width of ϕ_{LT} is also required to accommodate complete charge transfer from the video line into the BBD register. During the time when the signal is being transferred into the BBD register, the $\phi_{X1,2}$ clocks driving the register must stop with the clocks at high potential on the buckets receiving charge from video line. This will cause a deep potential well for the signal charge to flow into. The buckets receiving charge for both the odd and even transport registers are driven by ϕ_{X2} and the charge transfer takes place simultaneously for both registers during the time ϕ_{X2} is held high. Note that there is an extra clock of ϕ_{X2} with the ϕ_{LT} pulse. The function of this extra clock is to dump the "fat zero" charge of the BBD register into the video lines. This "fill and spill" action significantly improves the transfer efficiency of the signal charge from the video lines into the BBD register.

The ϕ_{LT} clock is then shut off before the BBD register shifts the signal charge to the output amplifiers. During readout, the odd BBD register produces the first pixel. It reads out on the second low-going ϕ_{X2} clock after the transfer period. The second pixel is produced by the even BBD register. Since this even pixel must transfer through an extra half-stage, which is controlled by ϕ_{X1}, it is produced when ϕ_{X1} goes low. This provides an easily multiplexed signal by means of a simple external adder-amplifer.

Specifications

Table 4 shows the operating biases and clock amplitudes in accordance with the timing diagram of Figure 5. With the exception of the supply inputs, such as V_{DD}, the input impedance to input terminals is essentially capacitive. The capacitances are listed in Table 2.

Optical to Electrical Performance

Table 5 lists a summary of optical characteristics, and the spectral response is shown in Figure 3.

Evaluation Detector Head

A complete LN2 cooled detector head useful for evaluating the performance and operating characteristics of the RA0128NIU is available from Reticon. The head consists of a LN2 dewar with 4 hour hold time, complete drive and video circuitry, and a 100 mm F1.8 silicon lens. The output at the RH0128NI detector head is RS170 compatible video which can be displayed on any standard TV monitor. Contact your local sales office for more information on the RH0128NI detector head.

Table 1. Pin Description

Pin Number	Pin Name	Pin Definition
1	V_{Sub}	Substrate voltage
2	GND	Ground
3	EOF	End of frame
4	LO	Odd line control
5	LE	Even line control
6	ϕ_{LR}	Video line reset switch
7	V_{Q1}	Odd analog shift register input bias
8	ϕ_{R1}	Reset gate clock for the odd reset switch
9	ϕ_{X1O}	Phase 1 clock to the Odd BBD register
10	ϕ_{X2O}	Phase 2 clock to the Odd BBD register
11	FRG	Frame reset gate
12	FRD	Frame reset drain
13	VID_1	Odd video output
14	NC	No connection
15	NC	No connection
16	VID_2	Even video output
17	V_{DD}	Power supply voltage
18	V_{BUFF}	Buffer gate switch bias
19	ϕ_{X2E}	Phase 2 clock to even BBD register
20	ϕ_{X1E}	Phase 1 clock to even BBD register
21	ϕ_{R2}	Reset gate clock of the even reset transistor
22	V_{BB}	Tetrode-gate bias
23	V_{Q2}	Input bias for the even analog shift register
24	ϕ_{LT}	Line transfer switch
25	ϕ_{Start}	Start pulse for Digital dynamic shift register
26	ϕ_{Y1}	Phase 1 clock to Digital register
27	ϕ_{Y2}	Phase 2 clock to Digital register
28	NC	No connection

Table 2. Terminal Input Capacitance

Pin Number	Symbol	Capacitance (pF)
1	V_{Sub}	Substrate
2	GND	800
3	EOF	5
4	LO	17
5	LE	17
6	ϕ_{LR}	17
7	V_{Q1}	4
8	ϕ_{R1}	3
9	ϕ_{X1O}	22
10	ϕ_{X2O}	23
11	FRG	12
12	FRD	140
13	VID_1	12
14	NC	No connection
15	NC	No connection
16	VID_2	12
17	V_{DD}	230
18	V_{BUFF}	32
19	ϕ_{X2E}	23
20	ϕ_{X1E}	23
21	ϕ_{R2}	3
22	V_{BB}	31
23	V_{Q2}	4
24	ϕ_{LT}	17
25	ϕ_{Start}	5
26	ϕ_{Y1}	33
27	ϕ_{Y2}	33
28	NC	No connection

Table 3. Clock Rise and Fall Timing

Parameters	Min	Typ	Max	Units
ϕ_{X1}, ϕ_{X2} Rise time	20	60		ns
ϕ_{X1}, ϕ_{X2} Fall time	20	60		ns
ϕ_{Y1}, ϕ_{Y2} Rise time	20	60		ns
ϕ_{Y1}, ϕ_{Y2} Fall time	20	60		ns
Clock crossing ϕ_{X1}, ϕ_{X2}	0 [1]	40	50	% V_{DD}
Clock crossing ϕ_{Y1}, ϕ_{Y2}	20	50	80	% V_{DD}

Note:

[1] Clocks may be nonoverlaping with maximum of 50 nanoseconds dead time between rising and falling edges.

Table 4. Electrical Characteristics (77°K)

Symbol	Parameter		Min	Typ	Max	Units
ϕ_X	Bucket-Brigade register clock	High	V_{DD}-1	V_{DD}-0.5	V_{DD}	V
		Low	-0.5	0.3	0.5	
ϕ_Y	Digital register clock	High	V_{DD}-1	V_{DD}-0.5	V_{DD}	V
		Low	-0.5	0.3	0.5	
ϕ_{LT}	Line transfer	High	V_{DD}-1	V_{DD}-0.5	V_{DD}	V
		Low	-0.5	0.2	0.5	
ϕ_{LR}	Line reset	High	V_{DD}-1	V_{DD}-0.5	V_{DD}	V
		Low	-0.5	0.3	0.5	
ϕ_R	Video reset	High	V_{DD}	V_{DD}+1	V_{DD}+1.5	V
		Low	-0.5	0.3	0.5	
ϕ_{Start}	Digital register start pulse	High	V_{DD}-1	V_{DD}-0.5	V_{DD}	V
		Low	-0.5	0.3	0.5	
ϕ_{FRG}	Frame reset gate (frame reset mode only)	High	V_{DD}-1	V_{DD}-0.5	V_{DD}	V
		Low	-0.5	0.3	0.5	
ϕ_{FRD}	Frame reset drain (frame reset mode only)	High	V_{DD}-3.5	V_{DD}-3	V_{DD}-2.5	V
		Low	-0.5	0.3	0.5	
EOF	End of frame	High			V_{DD}	V
	(sync current)	Low			1.5	mA
V_{DD}	Power supply voltage		12	15	18	V
V_Q	BBD input bias		9	10	11	V
V_{BUFF}	Isolation gate bias		V_{DD}-2	V_{DD}-1.5	V_{DD}	V
V_{BB}	Transport bias		V_{DD}-3	V_{DD}-2.5	V_{DD}-1	V
V_{Sub}	Substrate voltage		-1	0		V
LO & LE	Line control		V_{DD}-1	V_{DD}-0.5	V_{DD}	V

Table 5. Electro-optical Characteristics (77°K and 2.5 MHz Pixel Rate)

Parameter	Typical	Units
Architecture	Photodiode	
Array size	128 x 128	pixels
Pixel size	60 x 60	μm^2
Fill factor	59	%
Chip size	433 x 453	mil^2
Cutoff wavelength (λ_c) Optical:	5.0 ~ 5.5	µm
Saturation charge (Q_{Sat})	2000K	electrons
Electron sensitivity	0.7	µV/e
Horizontal clock frequency	5	MHz
Maximum data rate	10	MHz/pixel
Frame rate	>450	frames/sec
Horizontal CTE	>.99996	
Readout noise at 80°K background	2000	electrons rms
Readout noise at 300°K background	2200	electrons rms
Dynamic range	>1000:1	peak signal to rms noise
MRT (without uniformity correction)	1	°C
Uniformity (element to element)	≤0.5%	rms
(overall)	≤±5%	
Offspec pixels	≤20	pixels

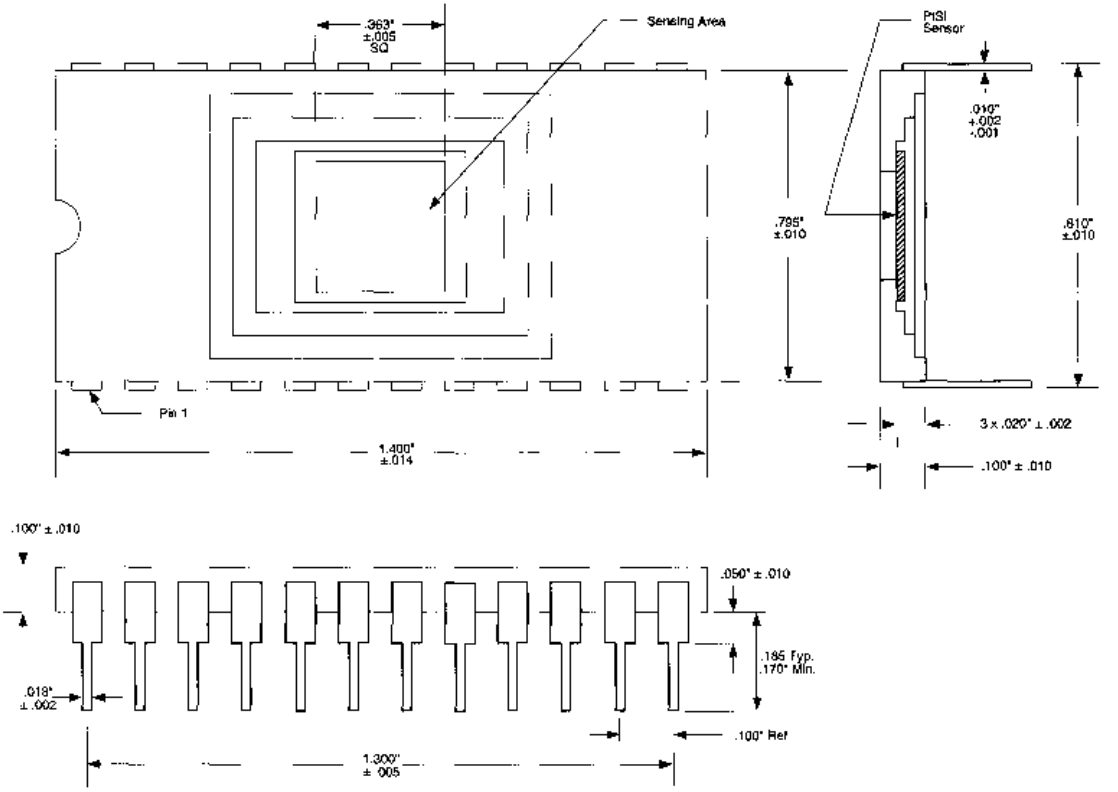


Figure 7. Package Dimensions

Ordering Information

Part Number	Detector Head
RA0128NIU-011	RH0128NIL-011

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General Description

Reticon has successfully combined the advantages of thin-film platinum silicide Schottky-barrier diode (PtSi SBD) technology with self-scanned readout methods to produce a self-scanned PtSi infrared linear array for scientific applications. This device is available in a standard 34-pin dual-inline ceramic package (which accommodates backside-illumination of the chip and simplifies the cryogenic cooling requirement) as shown in Figure 1. Table 1 shows the pin definition of the PtSi "SI" series arrays.

Since the substrate material is silicon, backside-illumination of the chip has the inherent advantage of blocking the visible and very near infrared photons (i.e., by absorption) from reaching the photo-detector area. In addition, long wavelength infrared photons lack sufficient energy to excite carriers to jump the metal-semiconductor (i.e., Schottky) barrier thus limiting the photoresponse from the shortwave infrared (SWIR) to the midwave infrared (MWIR) spectral region. The result is an array which is sensitive to wavelengths from 1.1 to 5 µm without the need for external filters.

The array comes in two sizes, 1024 and 512 elements. Each element of the array is 25 µm wide and 2500 µm long giving each a slit-like 100:1 aspect ratio suitable for coupling to monochromators or spectrographs. Applications for this array include: IR spectroscopy, remote sensing, push-broom imaging, and industrial temperature monitoring.

Key Features

- PtSi Schottky-barrier diode
- 1024 and 512 element IR linear array
- 25 µm pixel-to-pixel spacing
- 2.5 mm pixel length
- 60% fill factor
- 1.1 to 5 µm infrared spectral response
- Self-scanned structure
- Excellent element-to-element nonuniformity: <1% rms

Sensor Characteristics

The photosensing area of this device is composed of an array of thin-film PtSi SBDs. The pixel-to-pixel spacing is 25 µm. The pixel length is 2.5 mm. Each PtSi SBD is surrounded by an n^+ guard ring for suppressing leakage current. A channel stop is used to separate two adjacent pixels. Figure 2 shows the sensor geometry. The photo sensitive area of each pixel is 15 µm x 2500 µm. The length of the sensor elements is 2.5 mm giving each element a slit-like geometry with 100:1 aspect ratio suitable for coupling to monochromators or spectrographs. Figure 3 shows the typical spectral response and quantum efficiency.

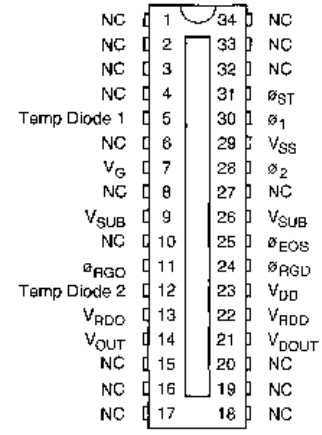


Figure 1. Pinout Configuration

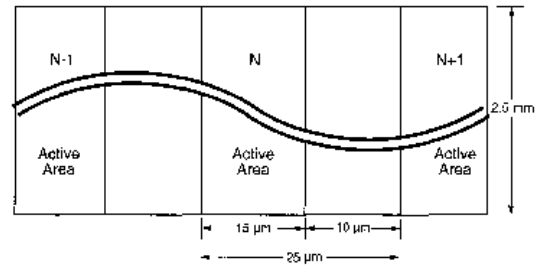


Figure 2. Sensor Geometry

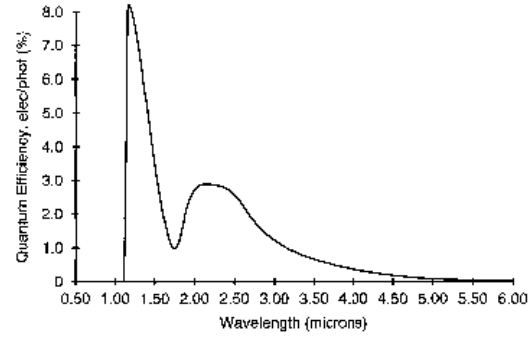


Figure 3. Absolute Quantum Efficiency versus Wavelength. Typical Reticon PtSi SBD shown. Optical cavity peaked for 3.5 µm wavelength.

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Operation

In order to understand the operation of the PtSi SBD array, it is helpful to know some of the similarities and differences that exist between a p-n junction diode and an SBD detector. The SBD operates in the storage mode just like the p-n junction diode. Its capacitance per unit area is about the same as the p-n junction diode and they both have a similar voltage compliance. Therefore, the saturation charge is comparable for similar diode areas. The SBD also has reverse bias characteristics similar to the p-n junction, however, its dark leakage current is several orders of magnitude larger than that of a p-n junction of the same area at the same temperature. As a result it is necessary to cool the SBD array in order to reduce the dark leakage current to a negligible value. In order to realize reasonable integration times, the array must be operated near liquid nitrogen temperatures (i.e., 77°K).

Both the SBD and the p-n junction diode are photon detectors. However, they differ significantly in sensitivity. In the visible and very near infrared region, photons are absorbed in the bulk silicon and a p-n junction will collect charge generated up to a distance of a diffusion length. As a result, a p-n junction detector has a collection volume much larger than the actual depletion region of the junction. In contrast to this, photons in the infrared spectral region are not absorbed in the bulk silicon but only in the thin silicide film. therefore, the collection volume of a SBD is much smaller than that of a p-n junction detector. This is one reason for the much lower sensitivity of the SBD as compared to the p-n junction detector of equal surface area.

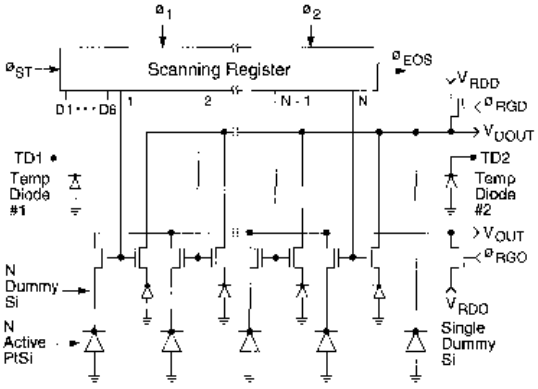


Figure 4. Equivalent Circuit

Scanning Circuit

The simplified equivalent circuit of an SI Series PtSi array is shown in Figure 4. Each cell consists of an active SBD photodiode and a dummy photodiode, both with an associated storage capacitance. These diodes are connected through MOS multiplex switches to active and dummy video lines. The shift register is driven by complimentary square wave clocks with periodic start pulses being introduced to initiate each scan. Cell-to-cell sampling rate is determined by the clock frequency. Integration time is the interval between start pulses. The output signal obtained from each scan of an N element array is a train of N charge pulses each proportional to the light intensity on the corresponding photodiode. In addition to the signal charge, switching transients are capacitively coupled into the active video line by the multiplex switches. These same transients are introduced into the dummy video line and, therefore, can be eliminated and a clean signal recovered by reading out the video and dummy lines differentially.

Clock and Voltage Requirements

Scanning is achieved by means of a digital shift register. The shift register is driven by complimentary square wave clocks, $ø_1$ and $ø_2$. The clock amplitude should be equal to V_{DD} - V_{SS}. With V_{DD} – 5V and V_{SS} = 0V, the clock inputs will be HCMOS compatible. Since each photodiode is read out on the positive transition of $ø_2$, the frequency of the clock signal should be set equal to the desired video data rate.

The start pulse of similar amplitude to the clocks is required to load the shift register and initiate each readout period. A timing diagram for the start and clock signals is shown in Figure 5. Note: $ø_1$ and $ø_2$ clocks need to be continuously applied to the device. The time between start pulses determines the integration period. Note: Six dummy diodes are provided for dark reference at the front of both the RL0512SIU and RL1024SIU.

End of Scan

An output pulse useful primarily for test purposes is provided after the last photodiode is sampled by the shift register scanning circuit. The timing of the EOS output is shown in Figure 5. The voltage levels on the EOS output will be determined by the V_{DD} and V_{SS} voltage levels supplied to the photodiode array. When V_{DD} is at +5V and V_{SS} is operated at 0V, the EOS output will be compatible with HCMOS family of logic devices.

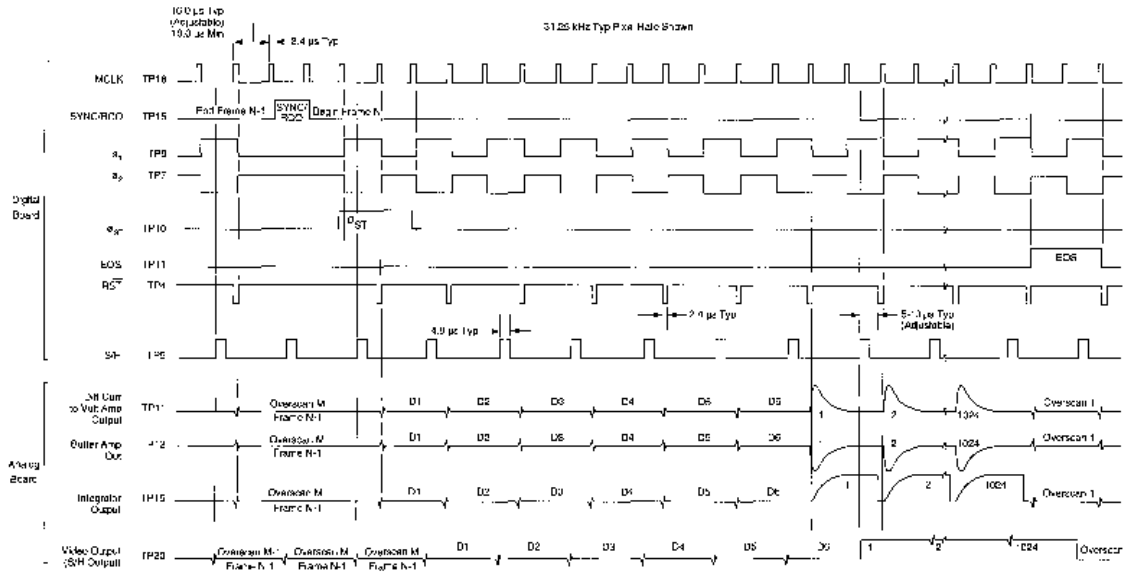


Figure 5. Timing Diagram

Amplifier Requirements

A recommended output circuit for use with SI devices is a simple current amplifier. A current amplifier holds the video line at a virtual ground and senses the current pulses flowing into the video line to recharge the diodes through their respective multiplex switches as they are sampled in sequence. These current pulses are converted to a train of voltage pulses corresponding to the light intensity on the various diodes. In this mode of operation, the current amplifier must provide a positive bias voltage to the video line since the PtSi photodiode is reverse biased in actual operation. Figure 6 shows a simple recharge amplifier suitable for use with SI series devices.

Dark Current

During normal operation, at liquid nitrogen (i.e., 77°K) temperatures, the array will saturate in ≈10 seconds due to dark current leakage. Under actual operating conditions, however, the maximum integration time is usually determined by the background photon flux hitting the detector and not the dark current leakage. For unfiltered 300°K blackbody radiation, the array saturates in ≈0.1 seconds with standard FOV apertures in Reticon's standard evaluation detector head.

Evaluation Detector Head

A complete, pour filled LN_2 cooled detector head useful for evaluating the performance and operating characteristics of the SI Series arrays is available from Reticon. The RH0512SIU or RH1024SIU consists of a 512 or 1024 element PtSi linear array, an LN_2 dewar with >8 hour hold time and complete drive and video processing circuitry. Contact EG&G Reticon for more information.

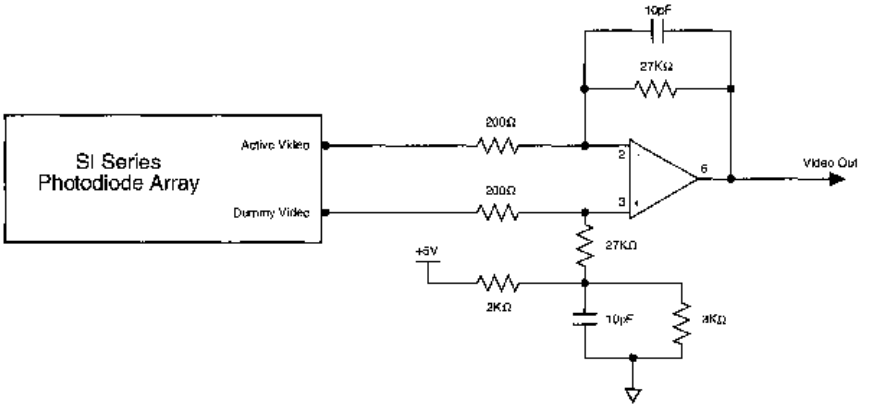


Figure 6. Simplified Recharge Mode Video Amplifier

Table 1. Pin Definition of the Wide Aperture, Linear PtSi IR SI Series Array

Pin Number	Pin Name	Pin Definition
1	NC	
2	NC	
3	NC	
4	NC	
5	TD1	Temperature diode #1
6	NC	
7	V_G	Guard ring voltage
8	NC	
9	V_{Sub}	Bottomside substrate contact
10	NC	
11	$ø_{RGO}$	Active video reset gate
12	TD2	Temperature diode #2
13	V_{RDO}	Active video reset drain
14	V_{Out}	Active video output
15	NC	
16	NC	
17	NC	
18	NC	
19	NC	
20	NC	
21	V_{DOut}	Dummy video output
22	V_{RDD}	Dummy video reset drain
23	V_{DD}	Scanning register (N-Well)
24	$ø_{RGD}$	Dummy video reset gate
25	$ø_{EOS}$	End of scan pulse output
26	V_{Sub}	Bottomside substrate contact
27	NC	
28	$ø_2$	Shift register clock; phase 2
29	V_{SS}	Topside substrate contact
30	$ø_1$	Shift register clock; phase 1
31	$ø_{ST}$	Start pulse input
32	NC	
33	NC	
34	NC	

Table 2. Electrical Characteristics (25°C)
(All voltages measured with respect to Pin 29, V_{SS})

Signal	Sym		Typ	Units
Scanning register (N-Well)	V_{DD}		5	V
Guard ring	V_G		5	V
Substrate	V_{SS}, V_{SUB}		0	V
Start pulse $ø_{st}$	V_{HS}	High	5	V
	V_{LS}	Low	0	V
Clock $ø_1$, $ø_2$	V_{H1}, V_{H2}	High	5	V
	V_{L1}, V_{L2}	Low	0	V
Reset gate $ø_{RGO}$, $ø_{RGD}$	V_{HRGO}, V_{HRGD}	High	5	V
	V_{LRGO}, V_{LRGD}	Low	0	V
Video bias	V_{Out}, V_{DOut}		2.5	V
Reset drain	V_{RDO}, V_{RDD}		2.5	V
Clock rate $ø_1$, $ø_2$ [1]	f_1, f_2		1	MHz (max)
Capacitance $ø_1$, $ø_2$ at 5V bias [1]	C_1, C_2			
RL0512SIU			31	pF
RL1024SIU			35	pF
Capacitance, each video line at 2.5V bias [1]	C_{Out}, C_{DOut}			
RL0512SIU			10	pF
RL1024SIU			18	pF

Note:
1 Calculated, not measured.

Table 3. Electro-Optical Characteristics (80°K)

Parameters	Typ	Units
Center-to-center spacing	25	µm
Pixel width (active area)	15	µm
Pixel length (active area)	2.5	mm
Fill factor	60	%
Number of pixels	1024 and 512	elements
Quantum efficiency @ 1.15 µm	8	%
Cutoff wavelength (λ_C)	5.0	µm
Maximum readout rate [1]	1	MHz
Saturation charge	7	pC
Saturation voltage [2]	7	V
Dark signal (80°K dark slide) [2]	0.15	V
Light on signal (300°K blackbody) [2]	3.5	V
Light off signal [2,3]	2.5	V
Thermodynamic noise (300°K blackbody) [2]	1.0	mV_{rms}
Dynamic range [2,4]	3500:1	rms
Pixel-to-pixel nonuniformity (300°K blackbody) [2]	<1%	rms

Notes:
1 Calculated, not measured
2 Measured using RH1024SIU Evaluation Dewar with no cold filters and a 41 ms integration time
3 Measured with the dewar window covered by a black anodized aluminum blank at ambient temperature
4 Dyn R = (V_{Sat} - Light on signal/thermodynamic noise)

Table 4. Absolute Maximum Ratings

	Min	Max	Units
Voltage applied to any terminal with respect to V_{SS}	0	+15	V

	A	B
RL0512SIU	0.567 ± .006	0.504 inch
RL1024SIU	1.071 ± .011	1.008 inch

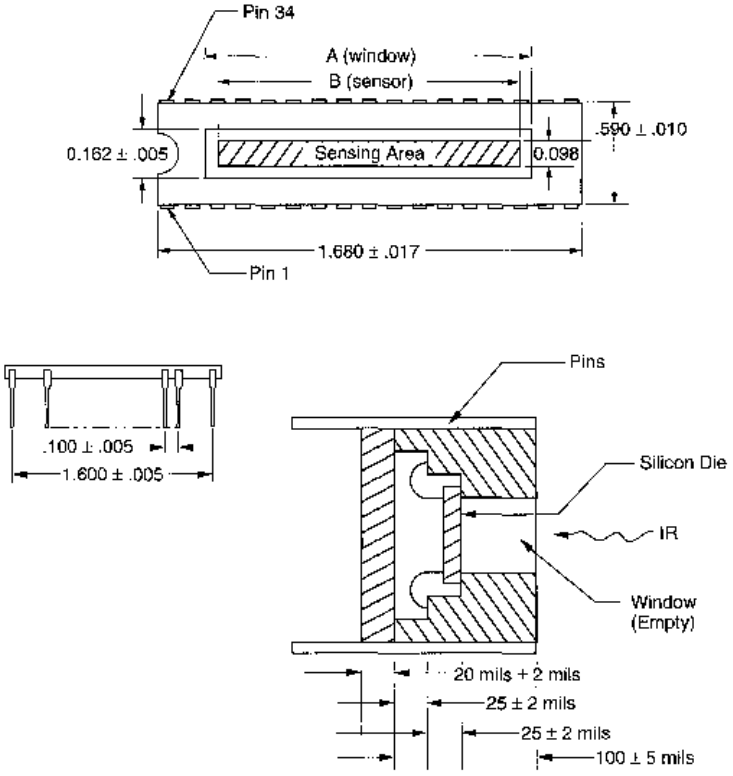


Figure 7. Package Dimensions (all dimensions are typical and in inches unless otherwise specified)

Ordering Information

Array Part Number	Evaluation Detector Head (includes detector)
RL0512SIU-011 RL1024SIU-011	RH0512SIU-011 RH1024SIU-011

055-0298
March 1992

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Custom Arrays

EG&G Reticon prides itself in having the broadest selection of image sensors of any manufacturer, enabling users to select an off-the-shelf device for use in a new product design. However, some new product requirements cannot be satisfied with available devices. In order to provide the optimal new product specifications, a special image sensor may be required.

EG&G Reticon offers a full custom capability to satisfy numerous special needs:

- **Charge-Coupled Devices (CCD)** -- Our advanced CCD technology offers high data rates, low noise, and small pixel geometries. Also, we can combine CCD technology with backside thinning of dice for greater sensitivity and UV response.

  EG&G Reticon offers custom CCD analog signal processing capability as well. We make CCD transversal filters, convolvers, binary-analog and analog-analog correlators, beam formers, multiplexers, adaptive equalizers, and many other innovative custom CCD products. The many high-frequency applications for these devices include DFT spectrum analysis, spread spectrum processing, voice processing, sonar processing, and modems.

- **Page and Character Scan Image Sensors** -- EG&G Reticon is a leading supplier of image sensors for scanning applications. Whether you need a matrix configuration for OCR or a long-line linear array for scanning documents, we can provide a custom configuration to satisfy your specific requirements.

- **Spectroscopy Image Sensor** -- We introduced the use of wide-aperture image sensors for spectroscopic applications. Wide-aperture devices provide the highest possible dynamic range for special applications. Also we make sensors with fiber optic faceplates for coupling to image intensifiers, achieving still higher performance.

- **Special Image Sensors** -- We handle the many special requirements needed for state-of-the-art imaging systems. We can provide devices with high-resolution pixel geometries, ultra-low noise performance, and super-high pixel scanning rates using special parallel processing. Also, we design custom multiplexers for IR sensing devices.

To sustain operation in special environments such as space, cryogenic, and military testing, unique packaging configurations can also be provided.

Custom image sensors are available with many different window configurations. Glass and quartz are used on standard devices, and sapphire, fiber optic, or other materials are also available.

Please consult our sales offices to discuss your custom requirements.

Multiplexers

M Series
RA0128M

The EG&G Reticon M Series parallel-in-serial-out multiplexer is a general purpose digital scanner for hybrid imager applications, especially applicable for infrared arrays made with compound semiconductor materials (InSb, etc.). These devices are available in die form and dual-inline packages for evaluation and/or nonhybrid applications (see Figure 1). A simplified block diagram of the multiplexer is shown in Figure 2.

The M Series is available in four lengths (32, 64, 128, or 256 multiplexing switches) on 4-mil center-to-center spacing. Each switch has an input connection bonding pad on-chip, with a 70 µm x 200 µm area for wire bonds or flip-chip bonds (see Figures 3 and 4).

Mirror-image configuration is provided for interdigitated image applications (see Typical Application). The M Series is fabricated in standard Reticon PMOS silicon gate technology. Very small photodiodes are connected to the multiplex switches for use in testing.

Key Features

- 32, 64, 128 or 256 elements (RL0032M, RL0064M, RL0128M, and RL0256M respectively)
- 100 µm spacing
- On-chip bonding pad suitable for wire bonds or flip-chip bonds
- Photodiode with each bonding pad for optical testing
- Standard and mirror images available for interdigitated linear array
- Low power requirements
- Diode reset feature
- Dummy video output for fixed pattern cancellation
- Low output video line capacitance

Operation

As shown in Figure 2, the shift register is clocked with a two-phase complementary clock (see clock specifications). A start pulse is required to initiate the scan (see start pulse specification). Upon entry of the start pulse, the dummy and the active video signals are sequentially interrogated through the multiplexer switches as the loaded bit is clocked down the shift register. An End-Of-Scan (EOS) signal occurs at the termination of each scan.

The off-chip sensors are bonded to the pads. There are two sets of switches, one an active and the other a dummy switch. The sources of the active switches are connected to the bonding pads, while the dummy switches are not connected to any pads. When the switches are simultaneously scanned by the shift register, both the signal charge and the dummy signal are read out through the active and dummy video lines, respectively. The dummy video line output signal is then subtracted from the active video line output signal in external circuitry, minimizing the fixed pattern noise generated by the multiplexing switches.

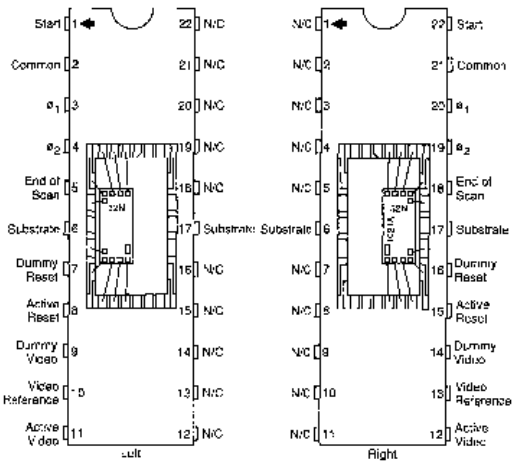


Figure 1. Pinout Configurations

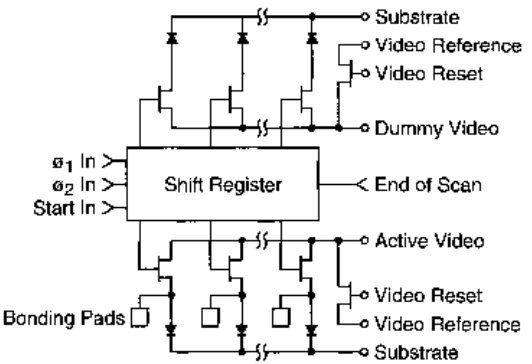


Figure 2. Simplified Block Diagram of the Multiplexer

Multiplex switch resistance as a function of clock voltage is provided in Table 1. The test setup used to obtain these resistance measurements is shown in Figure 9. I/O capacitance is given in Table 2.

Reset switches are provided on each video for use in signal processing (see Typical Application). The switch resistance values are given in Table 3. A reset switch resistance measurement set-up is shown in Figure 10.

General I/O timing relationships are shown in Figure 5. The detailed clock specifications and timing are covered under Clock, Start and EOS Specifications.

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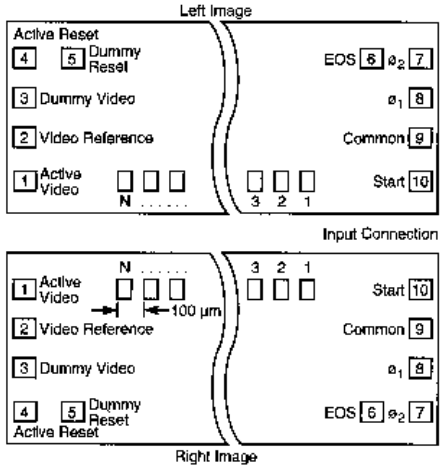


Figure 3. Left and Right Side Flip Chip Set (Shift Register Scanning from Right to Left)

The photodiode sites, indicated in Figure 2, are used for testing. They are each in parallel with a sensor bonding pad; together with the pad, each represents a capacitance of 0.3 pF.

Electrical Specifications

1. Shift Register Clocks ($ø_1$ and $ø_2$)

These clocks operate the shift register. For optimum multiplexer operation the clocks should cross at the midpoint. Figure 6 shows the typical midpoint crossing of 50%. The range of operation should be between 25% to 75%.

The clock rise (t_r) and fall (t_f) times should be between 5 ns and 100 ns. The clock amplitude operates within the range -9V to -16V and is typically at -15V with respect to the substrate. The clock frequency f($ø_1$) ranges from several kHz to 7 MHz.

2. Start Pulse ($ø_{ST}$)

The start pulse ($ø_{ST}$) loads the shift register with a voltage pulse to initiate the scanning process. It loads the register on each $ø_2$ low-to-high (negative-to-positive) transition as long as the start pulse is held low. Therefore, to ensure that only one bit is loaded, the start pulse should be low during only one $ø_2$ rising edge. Figure 5 illustrates the timing relationship with respect to $ø_2$. The rise (t_r) and fall (t_f) times should be between 5 ns and 100 ns. The clock amplitude of $ø_{ST}$ should be between -10V and -7V. The setup time (t_{set}) should be at least 30 ns, the hold time (t_{hold}) at least 30 ns, and t_{off} at least 50 ns.

Note: The shift register will load multiple bits if the start pulse is low for more than one $ø_2$ rising edge.

3. End of Scan (EOS)

The EOS pulse is generated at the output of the shift register to mark the termination of the scan. The last position is accessed with the $ø_1$ clock going negative. On the next $ø_2$ falling edge, the output pulse is applied to the gate of the EOS transistor. The drain of this transistor is brought out on the EOS pad, and the source is tied to the common. Therefore, tying a resistor >5KΩ from EOS to -5V (referenced to substrate) provides a load on which a positive-going pulse is observed upon the scan termination. See Figure 5 for EOS timing relationship referenced to $ø_2$. The internal delays (delay for Turn On [t_{dn}] and Turn Off [t_{df}] are typically in range of 50 ns < t_{dn} < 100 ns and 10 ns < t_{df} < 100 ns. The internal switch resistance with -15V clocks is typically 8KΩ. EOS amplitude is determined by the value of the resistor tied from EOS to the minus supply. Typical resistance value of 10KΩ provides a positive-going 4V pulse.

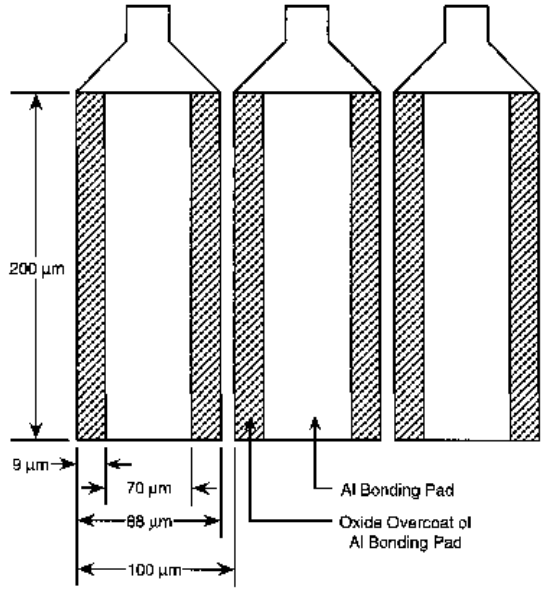


Figure 4. Switch Connection Bonding Pads

Typical Application

Figure 7 shows the interdigitated application of the mirrored devices where both left and right side devices are used with an array of sensor diodes. All three chips are bonded in a hybrid substrate, the pads bonded as shown. The clock inputs and video outputs are then bonded either to other dice on the substrate or to pin connections on a package to accommodate inputs and outputs for the clocks and the video. In this particular application photodiodes are accessed by using two devices, one for accessing the even numbered diodes and the other for the odd numbered diodes in the array. When the multiplexers are scanned, integrated-image charges will appear in sequence at the output, each one proportional to the light exposure at a given site.

Reset switches are provided for use in signal processing. They can be used to integrate signal charges on a capacitor (i.e., the video line capacitor or an external capacitor) then used to reset the capacitor after each multiplex site has been read out (see Figure 5 and Figure 8).

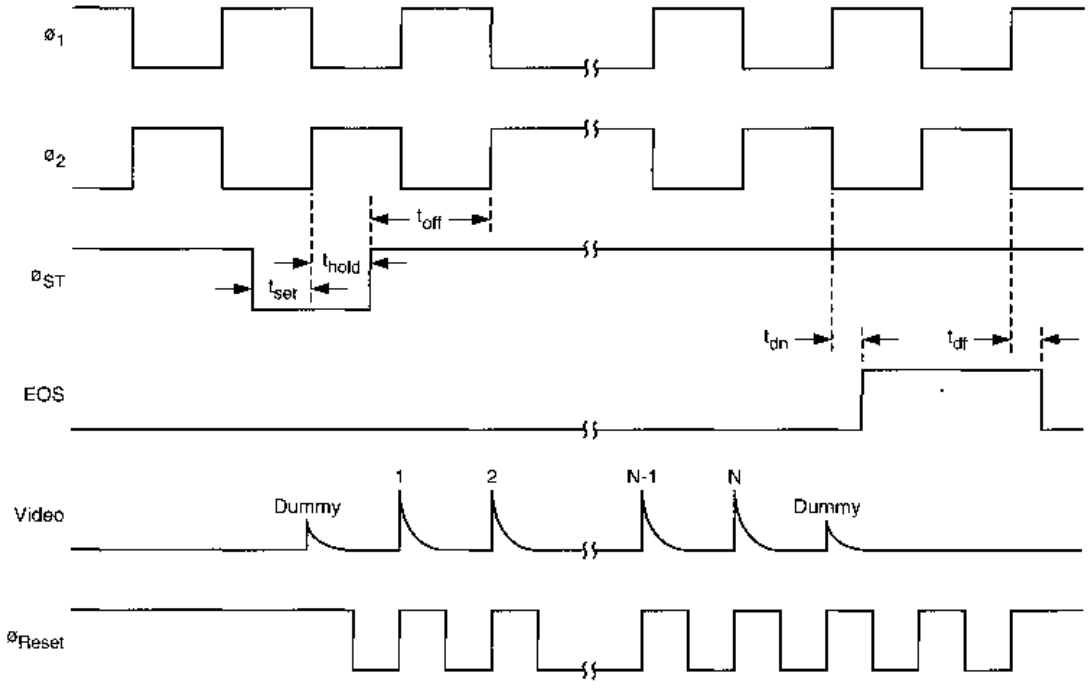


Figure 5. General Linear M Series Timing Diagram

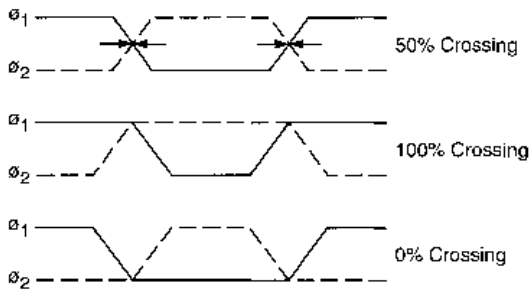
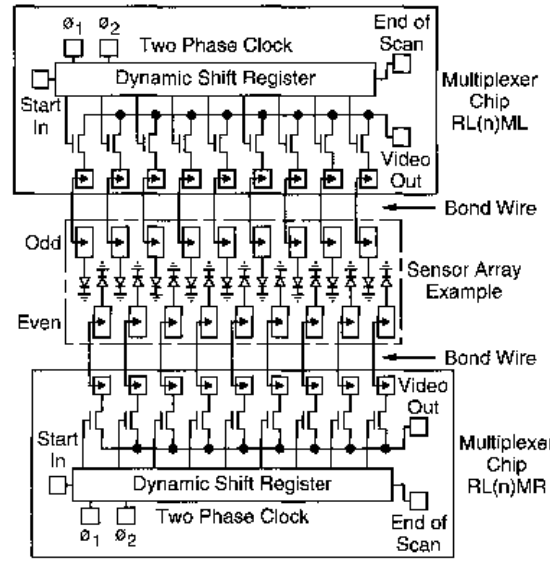
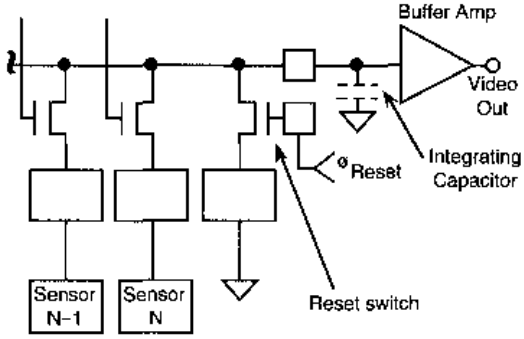


Figure 6. Definition of Clock Crossing



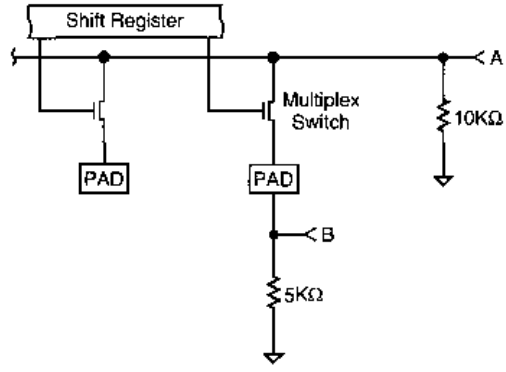
n = # of Shift Register Elements
L = Left
R = Right

Figure 7. Interdigitated Photodiode Array



Note:
The reset switch can be continuously active, while the shift register remains inactive, thus discharging any extraneous charges accumulating on the video line.

Figure 8. Reset Switch



The resistances were measured using points A and B in the circuit as shown.

Figure 9. Multiplex Switch Resistance Test Set Up

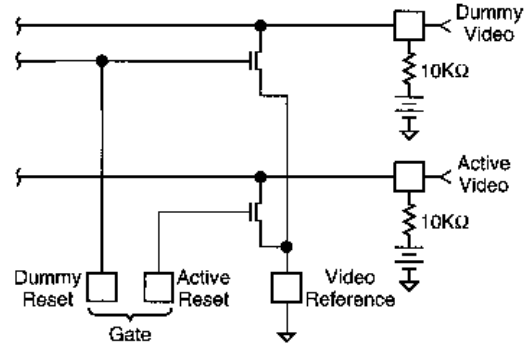


Figure 10. Reset Switch Resistance Measurement Set Up

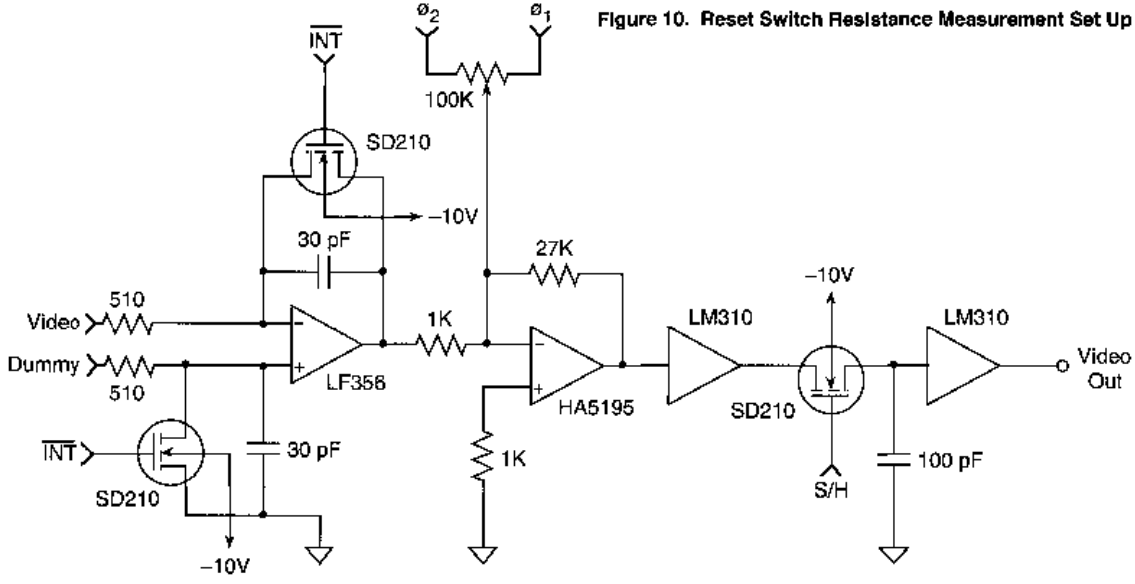


Figure 11. Test Circuit

Table 1. Multiplex Switch On-Resistance versus Clock Amplitude

Small sample variations are less than ±5% of the typical resistance.

Clock Amplitude	Typical Resistance
-15V	8.3 KΩ
-14V	10.5 KΩ
-13V	15.0 KΩ
-12V	26.7 KΩ
-11V	68.0 KΩ
-10V	235.0 KΩ

Table 2. I/O Capacitances [1, 2, 3]

	Device Type			
	256 Taps	128 Taps	64 Taps	32 Taps
ϕ_{X1}	81	41	22	13
ϕ_{X2}	81	41	22	13
ϕ_{Start}	4	3	4	3
EOS	20	11	7	5
Active video	15	8	5	4
Dummy video	15	8	5	4
Active reset	4.5	3.8	1.2	3
Dummy reset	4.5	3.8	1.2	3
Video reference	5	3.5	1.2	3.5

Notes:

1 Capacitance in picofarad (pF).
2 Measured with bias of -5V (with respect to substrate).
3 The readings are typical values.

Table 3. Reset Switch On-Resistance versus Reset Gate Voltage

Reset Gate Voltage	Resistance of Reset Gate
-15V	3.3 KΩ
-14V	3.5 KΩ
-13V	3.7 KΩ
-12V	4.1 KΩ
-11V	4.7 KΩ
-10V	5.2 KΩ

Table 4. Electro-Optical Characteristics (25°C)

	Min	Typ	Max	Units
Center-to-center spacing landing pads		100		µm
Pad aperture width		175		µm
Pad capacitance		0.3		pF
Dark fixed pattern nonuniformity [1, 2, 5]			±3	$\%V_{SAT}$
Between adjacent elements [1, 2, 5]			2	$\%V_{SAT}$
Photo response nonuniformity [1, 3, 5]		±7	±10	%
Dark signal leakage [1, 4, 5]			4	$\%V_{SAT}$
End of scan resistance		5	10	KΩ
Saturation [1, 3, 5]	1.3	1.6	1.8	V

Notes:

1 All measurements taken with typical clock and power supply voltages, using test circuit in Figure 11.
2 Scan time = 1.3 ms
3 Using 2870°K light source with HA-11 filter
4 Measured at 40 ms scan time
5 This specification applies to the small photodiodes on the die used to test the multiplex switches.

Table 5. Electrical Characteristics (25°C)

	Min	Typ	Max	Units
Clock amplitude [1]	-9	-15	-16	V
Start amplitude [1]	-7		-10	V
Reset clock amplitude [1]	-7	-15	-16	V
Common voltage	+4.5	+5	+5.5	V
Substrate voltage	+4.5	+5	+5.5	V
Video reference [2]	-2	0	+1.0	V
Clock frequency			7	MHz

Notes:

1 Measured with respect to substrate. Substrate is normally run at +5V for compatibility with TTL clock circuits.

2 With +5V substrate and -15V clock with respect to substrate.

	A
RL0032M	1.080±.011
RL0064M	1.080±.011
RL0128M	1.080±.011
RL0256M	1.600±.016

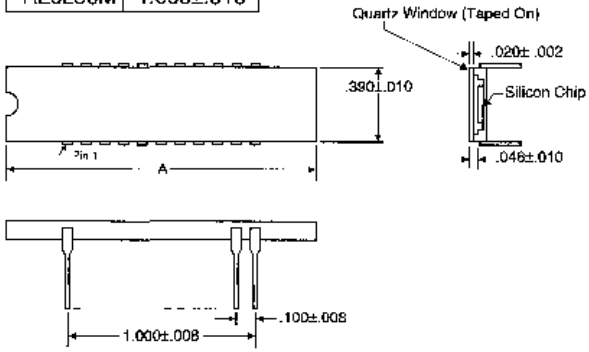


Figure 12. Package Dimensions

Ordering Information*

Mux Type	Package Order Number	Die Order Number
RL0032ML	RL0032MAU-011	RL0032MAD-001
RL0032MR	RL0032MAU-020	RL0032MAD-002
RL0064ML	RL0064MAU-011	RL0064MAD-001
RL0064MR	RL0064MAU-020	RL0064MAD-002
RL0128ML	RL0128MAU-011	RL0128MAD-001
RL0128MR	RL0128MAU-020	RL0128MAD-002
RL0256ML	RL0256MAU-011	RL0256MAD-001
RL0256MR	RL0256MAU-020	RL0256MAD-002

L denotes left element mux
R denotes right element mux
*Includes standard devices. For all options, consult your local sales office.

055-0209
January 1992

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General Description

The RA0128M is a 128 x 128 area multiplexing array. This device is derived from a slight modification of the EG&G Reticon standard area image sensor (RA0128N). Each sensing diode is made accessible directly from the surface of the device through an aluminum metal landing pad. The dimension of the metal landing pads are 50 µm x 50 µm. Using this landing pad, other types of sensing materials can be coupled to the sensing diode of the device, and thus it can function as a multiplexer to read out the video signals detected by the foreign sensing materials. Figure 1 shows the I/O pad layout of the RA0128M. Figure 2 shows the cross section view of one multiplexer cell.

The operation and specifications for the 128 x 128 device can be found in the RA0100A/RA0128N datasheet. Essentially it is a two-dimensional self-scanned optical sensor with optimized characteristics. 16,384 discrete photo diodes are geometrically arranged into a 128x128 matrix. The center-to-center spacing of the photodiodes are 60 µm in both the horizontal and vertical directions. A two-phase dynamic shift register is used to scan the vertical lines in sequence. When a vertical line is addressed by the dynamic shift register, the signal charges stored in the sensing diodes in that line will be transferred in parallel into two vertical bucket brigade (BBD) analog shift registers. The odd-numbered diodes are transferred into one BBD register, and the even-numbered diodes into another BBD register. The signal charges are then clocked out to two output nodes, where the charges are converted into video voltages. The RA0128M is packaged in a 24-pin dual-in-line package with a ground polished window covering the mask-defined active area. However, the RA0128M is usually delivered in die form since it requires additional processing steps for coupling the detector sensing material onto the device.

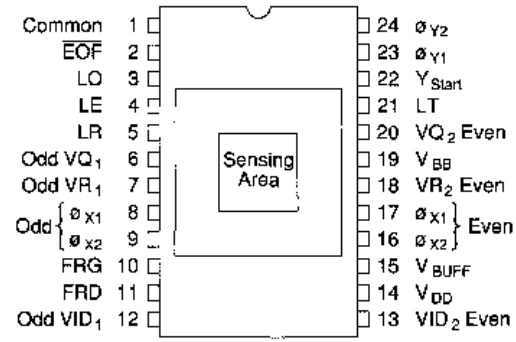


Figure 1. Pinout Configuration for Packaged Devices

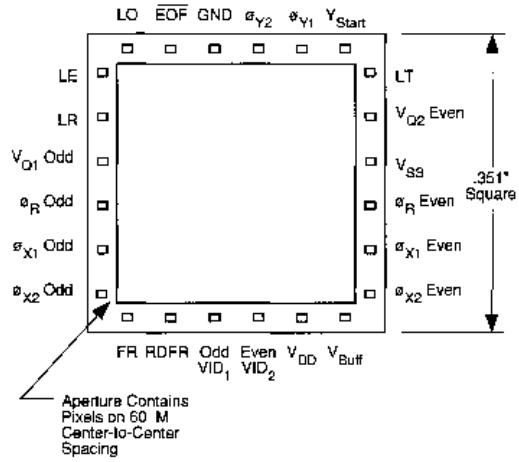


Figure 2. Pad Layout for Unpackaged Die

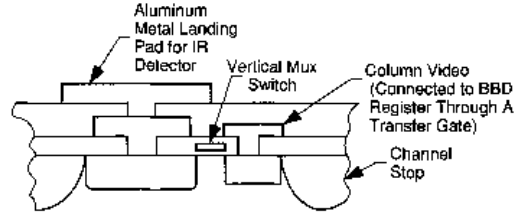


Figure 3. Cross Section of One Multiplexer Cell

345 POTRERO AVENUE SUNNYVALE, CALIFORNIA 94086-4197 (408) 738-4266 FAX: (408) 738-6979

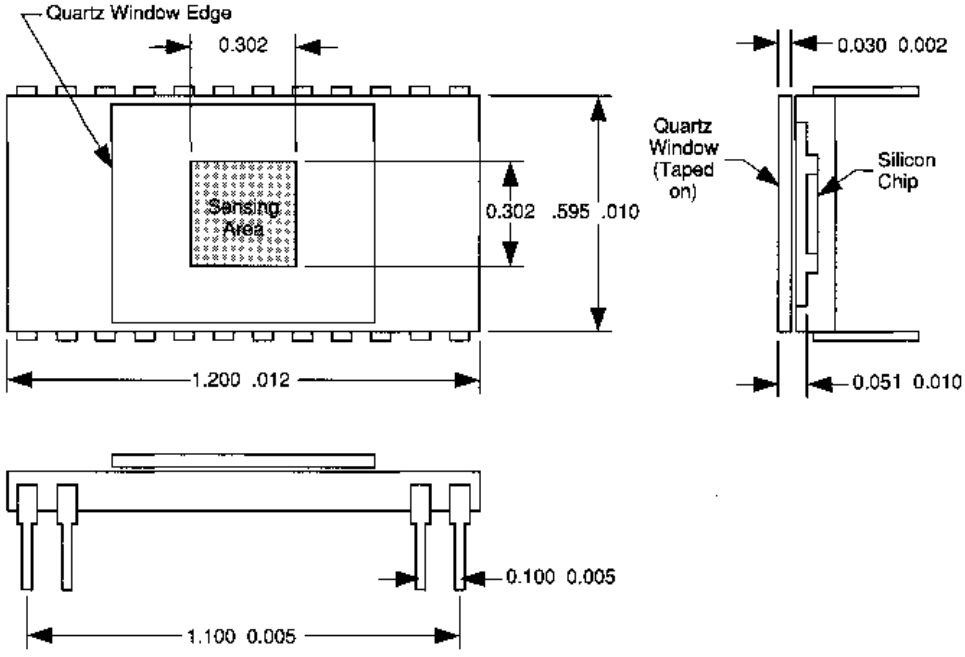


Figure 4. Package Dimensions (in Inches) for the RA0128MAU-111

Ordering Information

Multiplexer	Package	Die
RA0128M	RA0128MAU-111	RA0128MAD-002

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Evaluation Board Performance Characteristics

Typical Evaluation Board Performance Characteristics

Array Part Number	Evaluation Board Part Number	Type of Video and Polarity	Supply Voltage (See Note 1)	Current (Typical)	V_{sat} (Typical)	Sampling Frequency Minimum (See Note 2)	Sampling Frequency Maximum (See Note 2)	Dark Pattern (P-P) Typical (See Note 3)	Typical Clock/Switching Noise (P-P)	Typical Single Pixel Random Noise (P-P) (See Note 4)	Typical Dynamic Range (See Note 5)	Interface Connection	Mechanical Size (inches)	Number of Outputs
RL0064AAG	RC0200LNN/ RC0201LNN	recharge (neg)	+5V -15V +15V	@300 mA @ 75 mA @ 40 mA	3.6V	50 kHz	300 kHz	100 mV	Included in dark pattern		36/1	Solder terminals/ 14-pin DIP socket	4.5 x 6.5/ 2.25 x 3.5	1
RA0100AAQ RA0100AAF	RC0502ANA	S/H	+5V +15V -15V	@400 mA @150 mA @ 40 mA	2.0V	500 kHz	5 MHz	20 mV	800 mV	5 mV	700/1	Dual 22-pin PCB edge connector	4.5 x 6.5	1
RA1441AAB	RC0501ANN	Buffered	-15V	@ 50 mA	2.0V	50 kHz	400 kHz	100 mV	200 mV	N/A	20/1	Dual 22-pin PCB edge connector	4.5 x 4.5	14
RA0256BAQ	RC0503ANC	S/H	+5V +15V -15V	@100 mA @200 mA @150 mA	3.5V	1.9 MHz	8 MHz	20 mV	350 mV	15 mV	230/1	Dual 22-pin PCB edge connector	4.5 x 6.5	1
RL1284DAQ	RC0716LNB-020	Pulsed (neg)	+5V +15V -15V	@500 mA @800 mA @ 50 mA	1.5V	1.0 MHz	10 MHz	<5 mV	200 mV	<1 mV	1500/1	Dual 22-pin PCB edge connector (.156"SP)	4.5 x 9	8
RL1288DAQ	RC0716LNB-011	Pulsed (neg)	+5V +15V -15V	@500 mA @800 mA @ 50 mA	1.5V	1.0 MHz	10 MHz	<5 mV	200 mV	<1 mV	1500/1	Dual 22-pin PCB edge connector (.156"SP)	4.5 x 9	16
RL0128GAG	RC0301LNN	recharge (pos)	+5V -15V -10V	@200 mA @ 50 mA @ 50 mA	3.0V	75 kHz	1 MHz	300 mV	300 mV	10 mV	300/1	8 Male wire wrap pins on .1C-C	3 x 3	1
RL0128GAG	RC0100LNB/ RC0104LNN	S/H (neg)	-15V +5V	@300 mA @700 mA	2.4V	300 kHz	1 MHz	30 mV	75 mV	8 mV	300/1	Dual 22-pin PCB edge connector (.156"SP)/16 pin socket	4.5 x 6/ 3 x 3	1
SB/TB Series	RC1030LNN	S/H	+15V +5V -15V	@ 75 mA @ 70 mA @ 50 mA	10V		50 kHz			2.5 mV (SB) 1.25 mV (TB)	4000:1 (SB) 8000:1 (TB)	Dual 22-pin PCB edge connector (.156"SP)	3 x 4	1

Typical Evaluation Board Performance Characteristics

Array Part Number	Evaluation Board Part Number	Type of Video and Polarity	Supply Voltage (See Note 1)	Current (Typical)	V_{sat} (Typical)	Sampling Frequency Minimum (See Note 2)	Sampling Frequency Maximum (See Note 2)	Dark Pattern (P-P) Typical (See Note 3)	Typical Clock/Switching Noise (P-P)	Typical Single Pixel Random Noise (P-P) (See Note 4)	Typical Dynamic Range (See Note 5)	Interface Connection	Mechanical Size (inches)	Number of Outputs
SR Series	RC1010LNN RC1011LNN	S/H (neg)	+15V +5V -15V	@ 75 mA @200 mA @ 75 mA	5.5V		100 kHz			3.0 mV	2000:1	Dual 22-pin PCB edge connector (.156"SP)	4.5 x 8 4.5 x 3	1
RA204BJ	RC0505ANN	Pulse (neg)	+15V +5V -15V	@450 mA @800 mA @150 mA	.9V	250 kHz	8 MHz			0.16 mV	5600:1	Dual 22-pin PCB edge connector (.156"SP)	4.5 x 9.3	16
RL0256GAG	RC0100LNB/ RC0104LNN	S/H (neg)	-15V +5V	@300 mA @700 mA	1.6V	300 kHz	1 MHz	20 mV	75 mV	8 mV	200/1	Dual 22-pin PCB edge connector (.156"SP)/16 pin socket	4.5 x 6/ 3 x 3	1
RL0256GAG	RC0301LNN	recharge (pos)	+5V +15V -10V	@200 mA @ 50 mA @ 50 mA	3.0V	75 kHz	1 MHz	300 mV	300 mV	10 mV	300/1	8 Male wire wrap pins on .1C-C	3 x 3	1
RL0512GAG	RC0100LNB/ RC0105LNN	S/H (neg)	-15V +5V	@300 mA @700 mA	2.4V	300 kHz	1 MHz	30 mV	75 mV	8 mV	250/1	Dual 22-pin PCB edge connector (.156"SP)/16 Pin Socket	4.5 x 6/ 3 x 3	1
RL0512GAG	RC0302LNN	recharge (pos)	+5V +15V -10V	@200 mA @ 50 mA @ 50 mA	3.0V	75 kHz	1 MHz	300 mV	300 mV	10 mV	300/1	8 Male wire wrap pins on 1C-C	3 x 3	1
RL1024GAG	RC0303LNN	recharge (pos)	+5V +15V -10V	@200 mA @ 50 mA @ 50 mA	3.0V	75 kHz	1 MHz	300 mV	300 mV	10 mV	300/1	8 Male wire wrap pins on .1" C-C	3 x 3	1
RL1024GAG	RC0100LNB/ RC0106LNN	S/H (neg)	-15V +5V	@300 mA @700 mA	2.0V	300 kHz	1 MHz	26 mV	75 mV	8 mV	250/1	Dual 22-pin PCB edge connector (.156"SP)/16 pin socket	4.5 x 6 3 x 3	1
RL1024HAG/ RL1024HDQ	RC0100LNB/ RC0107LNN	S/H (neg)	-15V +5V	@300 mA @700 mA	2.5V	300 kHz	1.5 MHz	30 mV	50 mV	10 mV	250/1	Dual 22-pin PCB edge connector (.156"SP)/16 pin socket	4.5 x 6/ 3 x 3.625	1

Typical Evaluation Board Performance Characteristics

Array Part Number	Evaluation Board Part Number	Type of Video and Polarity	Supply Voltage (See Note 1)	Current (Typical)	V_{sat} (Typical)	Sampling Frequency Minimum (See Note 2)	Sampling Frequency Maximum (See Note 2)	Dark Pattern (P-P) Typical (See Note 3)	Typical Clock/Switching Noise (P-P)	Typical Single Pixel Random Noise (P-P) (See Note 4)	Typical Dynamic Range (See Note 5)	Interface Connection	Mechanical Size (inches)	Number of Outputs
RL1024HAG/ RL1024HDQ	RC1024LNN	recharge	+5V +15V -15V	@200 mA @ 40 mA @100 mA	5.0V	300 kHz	1 MHz	25 mV	70 mV	25 mV	200/1	Dual 22-pin PCB edge connector (.156"SP)	4 x 4.75	1
RL1728HAG	RC0100LNB/ RC0108LNN	S/H (neg)	-15V +5V	@300 mA @700 mA	3.0V	300 kHz	1.5 MHz	15 mV	30 mV	10 mV	300/1	Dual 22-pin PCB edge connector (.156"SP)/16 pin socket	4.5 x 6/ 3 x 3.6	1
RL2048HAG/ RL2048HDQ	RC0100LNB/ RC0108LNN	S/H (neg)	-15V +5V	@300 mA @700 mA	3.0V	300 kHz	1.5 MHz	15 mV	30 mV	10 mV	300/1	Dual 22-pin PCB edge connector (.156"SP)/16 pin socket	4.5 x 6/ 3 x 3.6	1
RL0128KAQ	RC0100LNB/ RC0104LNN	S/H (neg)	-15V +5V	@300 mA @700 mA	2.4V	300 kHz	1 MHz	30 mV	75 mV	8 mV	300/1	Dual 22-pin PCB edge connector (.156"SP)/16 pin socket	4.5 x 6/ 3 x 3	1
RL0128KAQ	RC0301LNN	recharge (pos)	+5V +15V -10V	@200 mA @ 50 mA @ 50 mA	3.0V	75 kHz	1 MHz	300 mV	300 mV	10 mV	300/1	8 Male wire wrap pins on .1C-C	3 x 3	1
RL0256KAQ	RC0100LNB/ RC0104LNN	S/H (neg)	-15V +5V	@300 mA @700 mA	1.6V	300 kHz	1 MHz	20 mV	75 mV	8 mV	200/1	Dual 22-pin PCB edge connector (.156"SP)/16 pin socket	4.5 x 6/ 3 x 3	1
RL0256KAQ	RC0301LNN	recharge (pos)	+5V +15V -10V	@200 mA @ 50 mA @ 50 mA	3.0V	75 kHz	1 MHz	300 mV	300 mV	10 mV	300/1	8 Male wire wrap pins on .1C-C	3 x 3	1
RL0512KAQ	RC0100LNB/ RC0105LNN	S/H (neg)	-15V +5V	@300 mA @700 mA	2.4V	300 kHz	1 MHz	30 mV	75 mV	8 mV	300/1	Dual 22-pin PCB edge connector (.156"SP)/16 pin socket	4.5 x 6/ 3 x 3	1
RL0512KAQ	RC0302LNN	recharge (pos)	+5V +15V -10V	@200 mA @ 50 mA @ 50 mA	3.0V	75 kHz	1 MHz	300 mV	300 mV	10 mV	300/1	8 Male wire wrap pins on .1C-C socket	3 x 3	1

Typical Evaluation Board Performance Characteristics

Array Part Number	Evaluation Board Part Number	Type of Video and Polarity	Supply Voltage (See Note 1)	Current (Typical)	V_{sat} (Typical)	Sampling Frequency Minimum (See Note 2)	Sampling Frequency Maximum (See Note 2)	Dark Pattern (P-P) Typical (See Note 3)	Typical Clock/Switching Noise (P-P)	Typical Single Pixel Random Noise (P-P) (See Note 4)	Typical Dynamic Range (See Note 5)	Interface Connection	Mechanical Size (inches)	Number of Outputs
RL1024KAQ	RC0100LNB RC0106LNN	S/H (neg)	-15V +5V	@300 mA @700 mA	2.0V	300 kHz	1 MHz	26 mV	75 mV	8 mV	250/1	Dual 22-pin PCB edge connector (.156"SP)/16-pin socket	4.5 x 6/ 3 x 3	1
RL1024KAQ	RC0303LNN	recharge (pos)	+5V +15V -10V	@200 mA @ 50 mA @ 50 mA	3.0V	75 kHz	1 MHz	300 mV	300 mV	10 mV	300/1	8 Male wire wrap pins on .1 C-C	3 x 3	1
RL0128LAB	RC0400LNN/ RC0402LNN	recharge (neg)	+5V -15V +15V	@300 mA @ 75 mA @ 40 mA	5.0V	50 kHz	300 kHz	100 mV	Included in dark pattern		50/1	Solder terminals/ 14-pin DIP socket	4.5 x 6.5/ 2.25 x 3.5	1
RO0064NAG	RC0064ONN	recharge (neg)	+5V +15V -15V	@ 60 mA @ 50 mA @ 50 mA	6.0V	50 kHz	700 kHz	20 mV	20 mV	5 mV	1200/1	Test Points	4.5 x 6.5	1
RA0128NAQ	RC0502ANA	S/H	+5V +15V -15V	@400 mA @150 mA @ 40 mA	2.0V	500 kHz	5 MHz	20 mV	800 mV	5 mV	700/1	Dual 22-pin PCB edge connector	4.5 x 6.5	1
RL4096NAG RL4096NFQ	RC4096LNA	S/H (neg)	+5V +15V -15V	@750 mA @150 mA @300 mA	2.5V	400 kHz	2 MHz	35 mV	Included in dark pattern		70/1	Dual 22-pin PCB edge connector	4.5 x 10	1
D Series Linear	RC0730LNB	S/H (pos)	+5V +12V -12V	@600 mA @350 mA @200 mA	2.5V	100 kHz	10 MHz	8 mV	150 mV	1 mV	2500/1	Dual 22-pin PCB edge connector (.156"SP)	4.5 x 10	1
S&T Series*	RC1000LNN/ RC1001LNN	S/H (pos)	+5V +15V -15V	@500 mA @175 mA @175 mA	6.0V	20 kHz	250 kHz	*10 mV	200 mV	1.5 mV	4000/1	Dual 22-pin PCB edge connector (.156"SP)/16 pin socket	4.5 x 8.0	1

* At 250 kHz clock frequency

Notes:

1. Voltage limits are nominal ± .1V
2. Minimum and maximum sampling frequencies are the typical values attainable with the standard oscillator components supplied with the evaluation circuit. If other frequencies are desired, component values must be changed and performance characteristics may be altered.
3. Excludes dark leakage signal
4. RMS single pixel noise would be 1/4 to 1/6 the random P-P value
5. Dynamic range is defined as V_{sat}/single pixel random noise and excludes dark leakage, dark pattern noise, and clock switching noise.

Operation and Alignment Procedures

RC0100
RC0730
RC1000/1001
RC1030

General Description

The Reticon RC0100 series circuit provides all clock, start, video amplifier, and blanking requirements for Reticon C, E, G, H, K and some RA series photodiode arrays.

Each circuit consists of two printed circuit boards – an RC0100LNB-011 "Motherboard", approximately 4.5 x 6 inches in dimension, which contains the clock and start generators, blanking circuit, sample-and-hold circuit, and buffer amplifiers, and the array board which contains a socket for the array, clock driver circuits, and a pre-amplifier.

Different array boards are needed for the various types of arrays:

RL0256CXX-XXX	–	RC0101LNN-011
RL0512CXX-XXX	–	RC0102LNN-011
RL1024CXX-XXX	–	RC0103LNN-011
RL0128GXX-XXX	–	RC0104LNN-011
RL0256GXX-XXX	–	RC0104LNN-011
RL0512GXX-XXX	–	RC0105LNN-011
RL1024GXX-XXX	–	RC0106LNN-011
RL0128KXX-XXX	–	RC0104LNN-011
RL0256KXX-XXX	–	RC0104LNN-011
RL0512KXX-XXX	–	RC0105LNN-011
RL1024KXX-XXX	–	RC0106LNN-011
RL0128EXX-XXX	–	RC0101LNN-011
RL0256EXX-XXX	–	RC0102LNN-011
RL0512EXX-XXX	–	RC0103LNN-011
RL1024HXX-XXX	–	RC0107LNN-011
RL1728HXX-XXX	–	RC0108LNN-011
RL2048HXX-XXX	–	RC0108LNN-011
RA5050AXX-XXX	–	RC0110ANA-011
RA3232AXX-XXX	–	RC0110ANA-020

The array boards are connected to the RC0100 Mother-board via connector J1/P1, or an optional 16-pin, 30 inch maximum, flat ribbon cable can be used. J1 is the 16-pin connector located approximately in the center of the RC0100 board. P1 is the male mating connector located on the array board. P2 is the edge connector of the RC0100 board.

Internal/External Clock Operation

The RC0100 Motherboard contains an internal clock generator which supplies the master timing signal. Provisions are also made for an external clock input.

For internal clock operation, jumper INT CLOCK. The frequency range of the internal clock is controlled by the selection of capacitors C1-A and C1-B. Refer to Table A of the RC0100LNB-011 schematic drawing for values for desired frequency range. R2, a 50K pot will allow for variance of the frequency within the selected frequency range. Boards are shipped from the factory with the clock frequency set at approximately 200 kHz internal operation.

For external clock operation, jumper EXT CLOCK, and apply an external clock into P2-Z. The external clock pulse should be an active TTL high clock with a minimum pulse width of 20 ns, and a maximum pulse width of 200 µs.

Internal/External Start Operation

The RC0100 Motherboard contains an internal start pulse generator. Provisions for an external start pulse are also available.

For internal start operation, jumper INT START, and set the desired interval between the start pulses, using the three four-position rocker switches S1, S2, and S3. Each switch has a weight of 2n and a maximum count of 4096 is available. For optimum operation, the scan time should not exceed 40 ms, because dark current increases with longer integration time. The minimum count between start pulses is eight, plus the number of elements in the array. Boards are shipped from the factory set in this configuration.

NOTE: If a scan time of >5 ms is used, change C28 on the RC0100 board to a .1 µF capacitor.

Because of an inherent count of one in the start pulse generator, the setting on the rocker switches will be one less than the actual count, i.e., if a count of 520 is desired, set the rocker switches to 519.

The blanking period (time between last element of previous scan and first element of next scan) is defined as the count of the start pulse generator minus the number of elements in the array.

For external start operation, jumper EXT START, and inject an external start signal into P2-A. The external start should be an active high TTL pulse with a minimum pulse width of the clock pulse width plus 50 ns, and a maximum pulse width of less than one clock period.

If an external start is used, it should be synchronized with the negative-going edge of the clock to ensure that the start pulse envelopes one and only one positive transition of the clock pulse.

Power Requirements

Connect +5 ± 0.1V @ 700 mA and -15 ± 0.1V @ 300 mA to P2 - E and P2 - Y, respectively. Connect ground to any pin from P2 - 1 to P2 - 22.

CAUTION

While performing the alignment procedure as outlined in the following pages, it will be necessary to monitor the output of the CA10A at TP3 (J1 Pin 1). If, at any time, this pin is shorted to any other pin or to ground, damage will result to the CA10A. Use caution when hooking probes to TP3.

Section 1

Alignment Procedure

RC0100 Motherboard with RC0101, 0102, or 0103 and Four Phase C Array

1. **Jumper Connections.** Split pads are provided to program the RC0100 board for the desired configuration. Refer to Table B of the RC0100LNB-011 schematic for correct configuration. See Figure 1 for location of split pads. Place the 2 phase/4 phase jumper (W3) in the 4 phase position.

2. Monitor TP1 and adjust R2 (if internal clock is used) for the desired frequency. The maximum frequency is 2 MHz. Adjust R11 for a 300ns, negative going pulse width.

3. Monitor P2-B and set the desired start pulse interval (if internal start is used). Synchronize the scope at P2 - B during alignment.

4. Monitor TP2 and adjust R64 for a 100ns pulse width.

5. Monitor TP3. Darken the array and adjust R4 (pot on component side of the array board) until the video signal is centered around –5V DC. Saturate the array, readjust if necessary, so no signal or switch spike is more negative than –8V DC. Do not over saturate.

6. Monitor J2-N (video output). The video output will be a sample-and-hold boxcar type signal.

7. Darken the array and adjust R36 until the average video is centered around the blanking period. (During blanking time, the video line is clamped to zero.)

8. R50, R51, and R52 control the odd/even pattern balance. With the array in complete darkness, adjust R51 for equal amplitude of the odd video elements.

9. With the array still in the dark, adjust R52 for equal amplitude of the even video elements.

10. With the array still in the dark, adjust R50 for equal amplitude of the odd and even elements. There is some interaction between R51, R52, and R50. Repeat Steps 8, 9, and 10 until the desired degree of balance is obtained.

11. With the array still in darkness, adjust R32 until the first two video elements are as close in amplitude as possible to the other elements.

12. Monitor P2-N. Adjust R11 until optimum performance is observed at the video output. Optimum adjustment of R11 results in a balance of maximum video output, minimum switching spikes, and fixed pattern tracking from dark to 90% of saturation. If clock frequency is below 500 kHz, R11 should be fully clockwise. This adjustment will interact with all the previous adjustments. Go back to Step 7 and touch up as necessary.

Section 2

Alignment Procedure

RC0100 Motherboard with RC0101, 0102, or 0103 with E Array

1. **Jumper Connections.** Refer to Table B of the RC0100LNB-011 schematic correct configuration. See Figure 1 for location of split pads. Place the 2 phase/4 phase jumper (W3) in the 2 phase position.

2. Monitor TP1. Adjust R2 for desired frequency (if internal clock is used). Maximum frequency in 2 MHz. Adjust R11 for a 300 ns, negative going pulse width.

3. Monitor P2 - B. Set desired start pulse interval using rocker switches S1, S2, and S3 (if internal start is used).

4. Monitor TP2 and adjust R64 for a 100 ns pulse width.

5. Monitor TP3. With the array in complete darkness, adjust R4 (pot on component side of the array board) until the video is centered around –5V DC. Saturate the array, readjust if necessary, so no signal or switching spike is more negative than –8V DC. Do not over saturate.

6. Monitor P2-N. Video output signal will be a sample-and-hold boxcar signal.

7. Darken the array and adjust R36 until the video elements are centered around the blanking level. (The blanking period is clamped to zero.)

8. With the array still in the dark, adjust either R51 or R52 until every other element is the same amplitude. (One of these pots will have no effect on the video signal.)

9. With the array still in the dark, adjust R50 to bring the odd and even elements together.

10. With the array still in the dark, adjust R32 (pot on the Motherboard) until the first two elements are as close to the same amplitude as the other elements as possible.

11. Adjust R11 until optimum performance is observed. Optimum adjustment of R11 results in a balance of maximum video output, minimum switching spikes, and fixed pattern tracking from dark to 90% of saturation. If clock frequency is below 500 kHz, R11 should be fully clockwise.

12. Due to interaction between all the previous adjustments, return to Step 7 and realign until the desired response is achieved.

Section 3

Alignment Procedure

RC0100 Motherboard with RC0104, 0105, or 0106 and G Series Array

1. **Jumper Connections.** Split pads are provided to program the RC0100 board for the desired configuration. Refer to Table B of RC0100LNB-011 schematic for correct configuration. See Figure 1 for location of split pads.

2. Monitor TP1. Adjust R2 for the desired frequency, 1 MHz maximum. Adjust R11 for a 700 ns, negative going pulse width.

3. Monitor P2-B. Set the desired start pulse interval, using rocker switches S1, S2, and S3.

4. Monitor TP2 and adjust R64 for a 100 ns pulse width.

5. Darken the array, monitor TP3 and adjust R2 (pot on the component side of the array board) to where the video signal is approximately centered at –2V to -3V DC. Saturate the array, readjust R2 if necessary, so no signal or switching spike is more negative than –8V DC. Do not over saturate.

NOTE: Potentiometer R51, R52, R50, and R32 have no effect when the RC0100 is used in conjunction with a G Series array board.

6. Monitor P2-N. The video output will be a sample-and-hold boxcar signal.

7. Darken the array and adjust R36 until the video signal is centered around the blanking level. (Blanking is clamped at zero.)

8. Adjust R11 until optimum performance is observed on the video. Optimum adjustment of R11 results in a balance of maximum video output, minimum switching spikes, and fixed pattern tracking from dark to 90% of saturation.

9. With the array in dark, readjust R36 if necessary, to bring the video level with the blanking.

Section 4

Alignment Procedure

RC0100 Motherboard with RC0104, 0105, or 0106 and K Series Array

1. **Jumper Connections.** Split pads are provided to program the RC0100 board for desired configuration. Refer to Table B, column G, of the RC0100LNB-011 schematic for correct configuration. See Figure 1 for location of split pads.

2. Monitor TP1. Adjust R2 for the desired frequency, 1 MHz maximum. Adjust R11 for a 700 ns, negative going pulse width.

3. Monitor P2-B. Set the desired start pulse interval, using rocker switches S1, S2, and S3.

4. Monitor TP2 and adjust R64 for a 100 ns pulse width.

5. Darken the array, monitor TP3 and adjust R2 (pot on the component side of the array board) to where the video signal is approximately centered at –2 to -3V DC. Saturate the array, readjust R2 if necessary, so no signal or switching spike is more negative than –8V DC. Do not over saturate.

NOTE: Potentiometer R51, R52, R50, and R32 have no effect when the RC0100 is used in conjunction with a K Series array board.

6. Monitor P2-N. The video output will be a sample-and-hold boxcar signal.

7. Darken the array and adjust R36 until the video signal is centered around the blanking level. (Blanking is clamped at zero.)

8. Adjust R11 until optimum performance is observed on the video. Optimum adjustment of R11 results in a balance of maximum video output, minimum switching spikes, and fixed pattern tracking from dark to 90% of saturation.

9. With the array in dark, readjust R36 if necessary, to bring the video level with the blanking.

Section 5

Alignment Procedure

RC0100 Motherboard with RC0107 or 0108 and H Series Array

1. **Jumper Connections.** Split pads are provided to program the RC0100 board for the desired config-uration. Refer to Table B of the RC0100LNB-011 schematic for correct configuration. See Figure 1 for location of split pads.

2. Monitor TP1 and adjust R2 (if internal clock is used) for the desired frequency. The maximum frequency is 1.5 MHz. Adjust R11 for a 200 ns, negative going pulse width.

3. Monitor P2-B and set the desired pulse interval (if Internal start is used). Synchronize the oscilloscope at P2-B during alignment.

4. Monitor TP2 and adjust R64 for a 100 ns pulse width.

5. Monitor TP3. With the array in dark, adjust R24 (1K pot on the array board) to zero the baseline of the video. Saturate the array and readjust R24 if necessary, so no signal or switching spikes go more negative than –8V DC. Do not over saturate.

NOTE: R51, R52, R50, and R32 on the RC0100 board will have no effect when an H Series array board is used.

6. With the array still in the dark, adjust R7 (200Ω pot on the array board) for best odd/even pattern.

7. Monitor the video output at P2-N. With the array in the dark, adjust R36 on the Motherboard until the video is centered with the blanking level.

8. Adjust R25 (100K pot on the array board) until the first three video elements are as close in amplitude as possible to the other elements.

9. Adjust R11 until optimum performance is derived on the video. Optimum adjustment of R11 results in a balance of maximum video output, minimum switching spikes, and a fixed pattern tracking from dark to 90% of saturation. This adjustment will interact with the previous adjustments. Go back to Step 5 and touch up as necessary.

Section 6

Alignment Procedure

RC0100 Motherboard with RC0110ANA-020 with RA3232A Array or RC0110ANA-011 with RA5050A Array

1. **Jumper Connections.** Split pads are provided to program the RC0100 board for the desired configuration. Refer to Table B of the RC0100LNB-011 schematic for proper configuration.

2. Monitor TP1. Adjust R2 for desired frequency. Maximum frequency is 1 MHz. Adjust R11 for a 600 ns, negative going pulse width.

3. Monitor P2-B. Set desired start pulse interval using rocker switches S1, S2, and S3 (if internal start is used). Start pulse interval must be at least 41 clock periods for an RA3232A or 59 clock periods for an RA5050A, giving a minimum line "flyback" of 9 clock periods.

4. Monitor TP2 and adjust R64 for a 100 ns pulse width, sync scope at EOF terminal on the array board.

5. Monitor TP3. With the array in complete darkness, adjust R13 (potentiometer on component side of array board) until the video is centered around –5V DC. Saturate the array, readjust if necessary, so no signal or switch spike is more negative than –8V DC. Do not over saturate.

6. Monitor P2-N. Darken the array and adjust R36 until the video elements are centered around the blanking level. (The blanking period is clamped to zero.)

7. Adjust R11 until optimum performance is derived on the video. Optimum adjustment of R11 results in a balance of maximum video output, minimum switching spikes, and fixed pattern tracking from dark to 90% of saturation.

8. The first element of each line is always low in amplitude. The second element's amplitude can be corrected by shorting out CR1, CR2 and/or CR3. This will vary with arrays and may require none, one, two or all of these shorted out for best results.

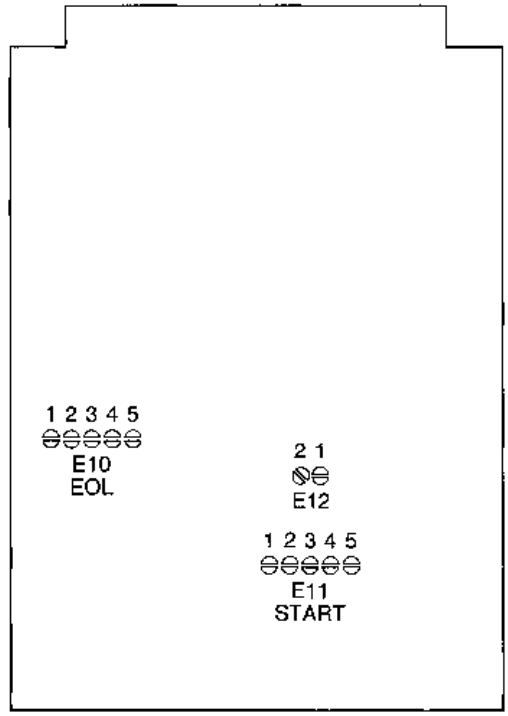
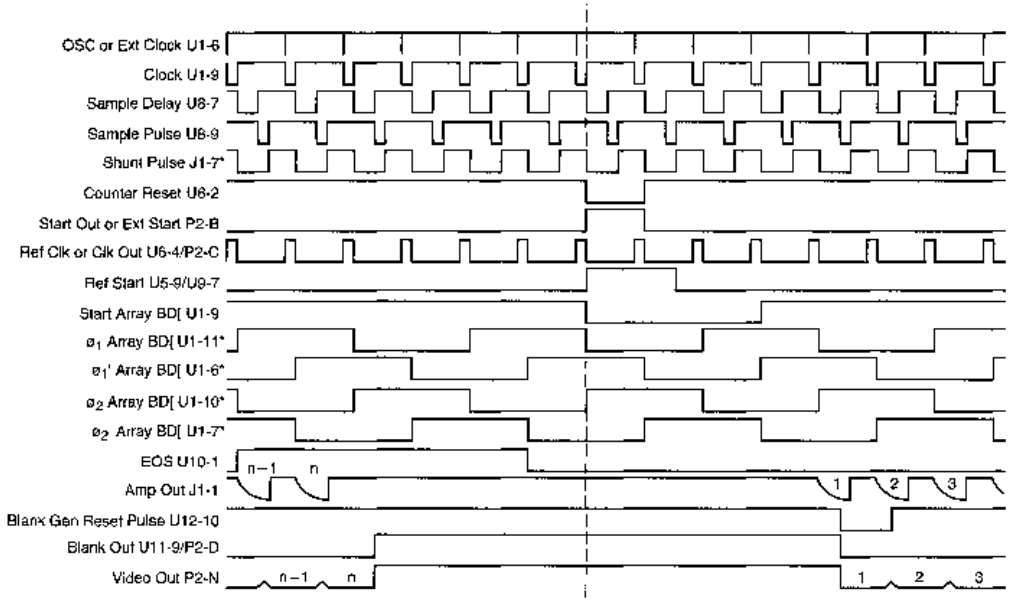
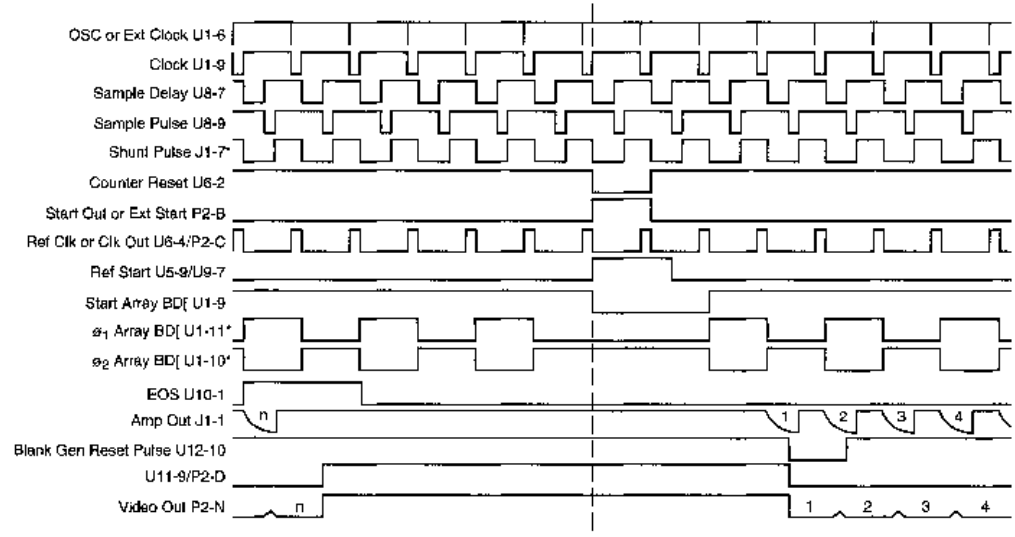


Figure 1. Split Pad Location



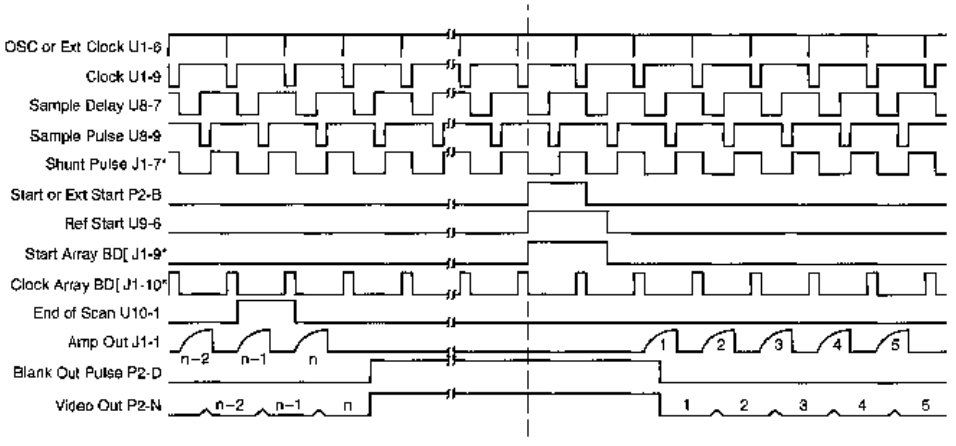
* Denotes MOS level signals, all other except video are TTL

Figure 2. Timing Diagram, RC0100 Series Circuit BDS, 4 Phase Operation, C Series Array



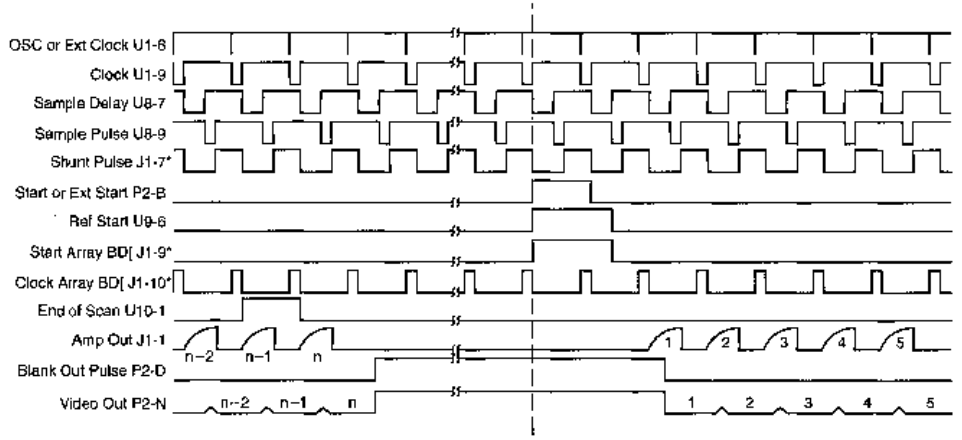
* Denotes MOS level signals, all other except video are TTL

Figure 3. Timing Diagram, RC0100 Series Circuit BDS, 2 Phase Operation, E Series Array



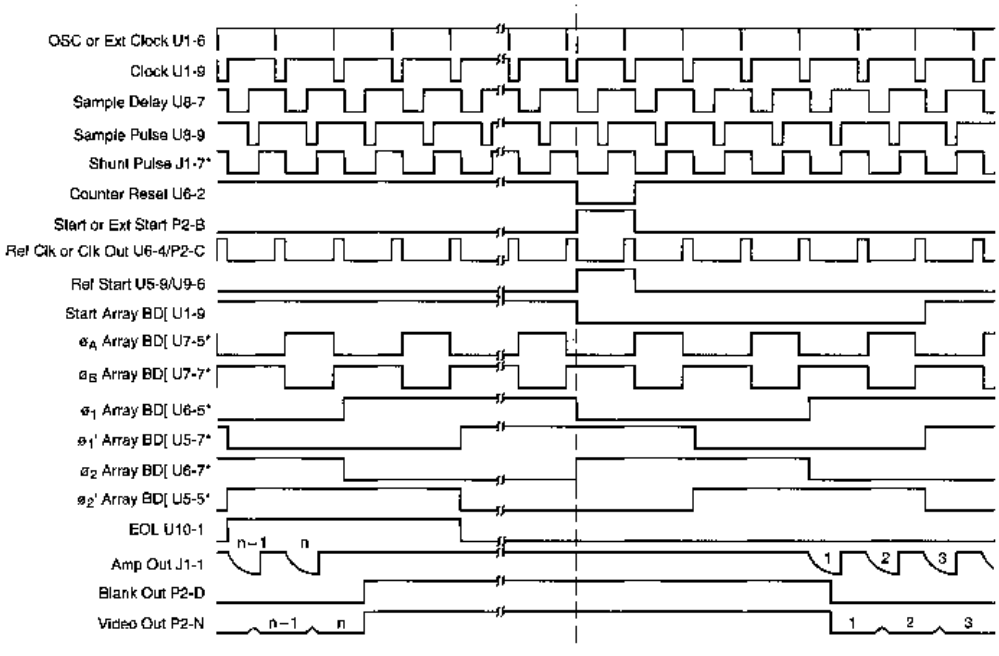
* Denotes MOS level signals, all other except video are TTL

Figure 4. Timing Diagram, RC0100 Series Circuit BDS, G Series Array



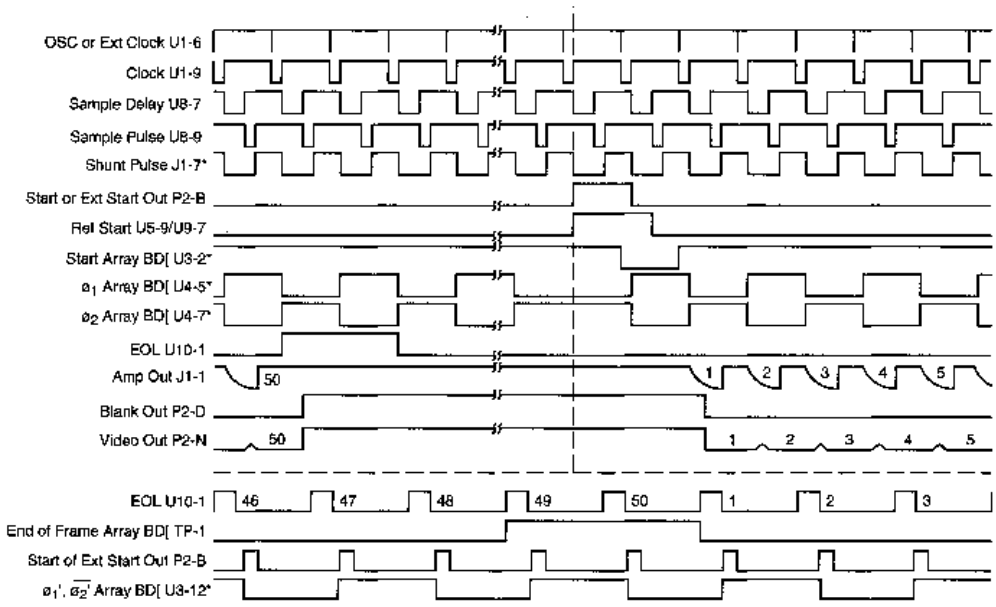
* Denotes MOS level signals, all other except video are TTL

Figure 5. Timing Diagram, RC0100 Series Circuit BDS, K Series Array



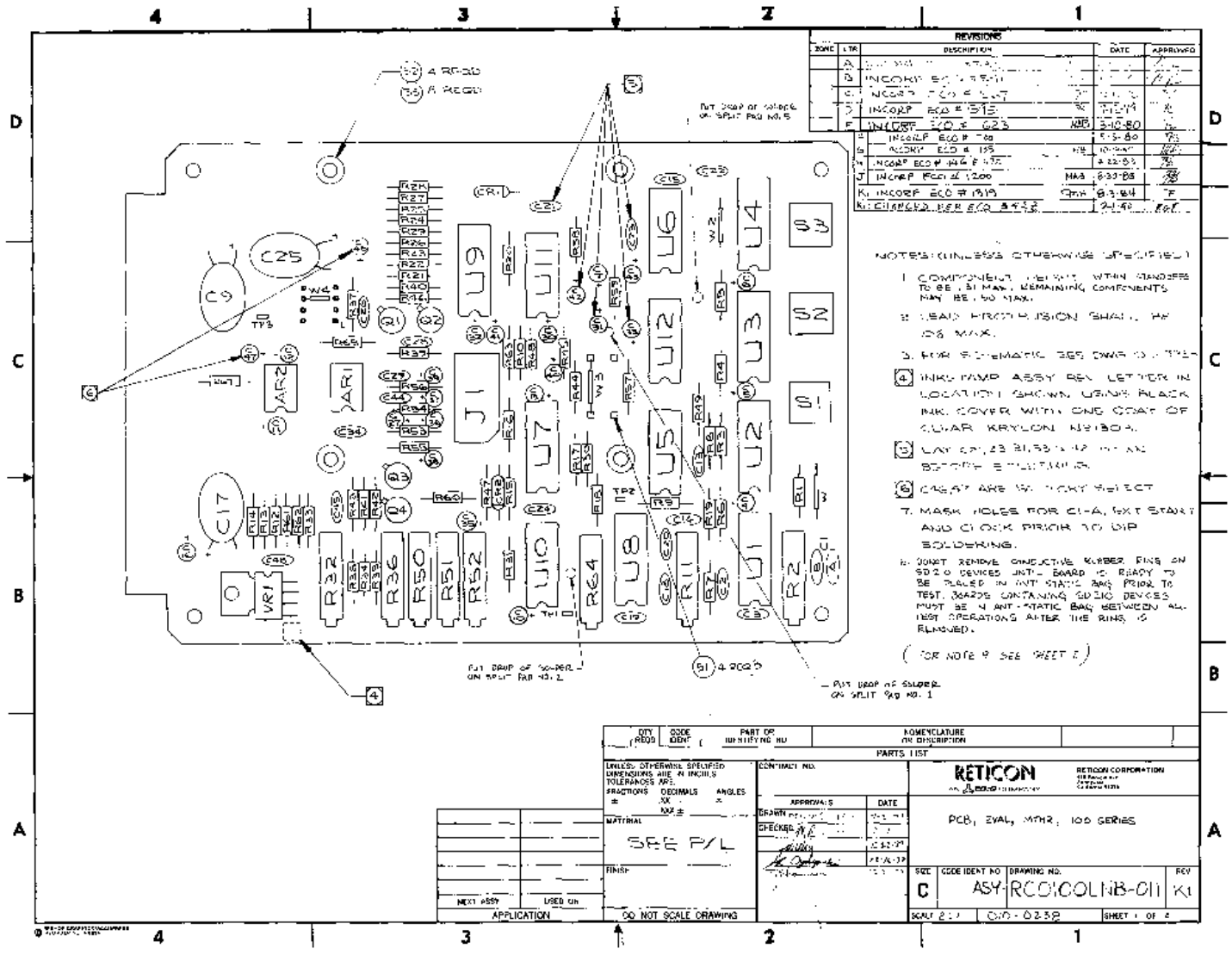
* Denotes MOS level signals, all other except video are TTL

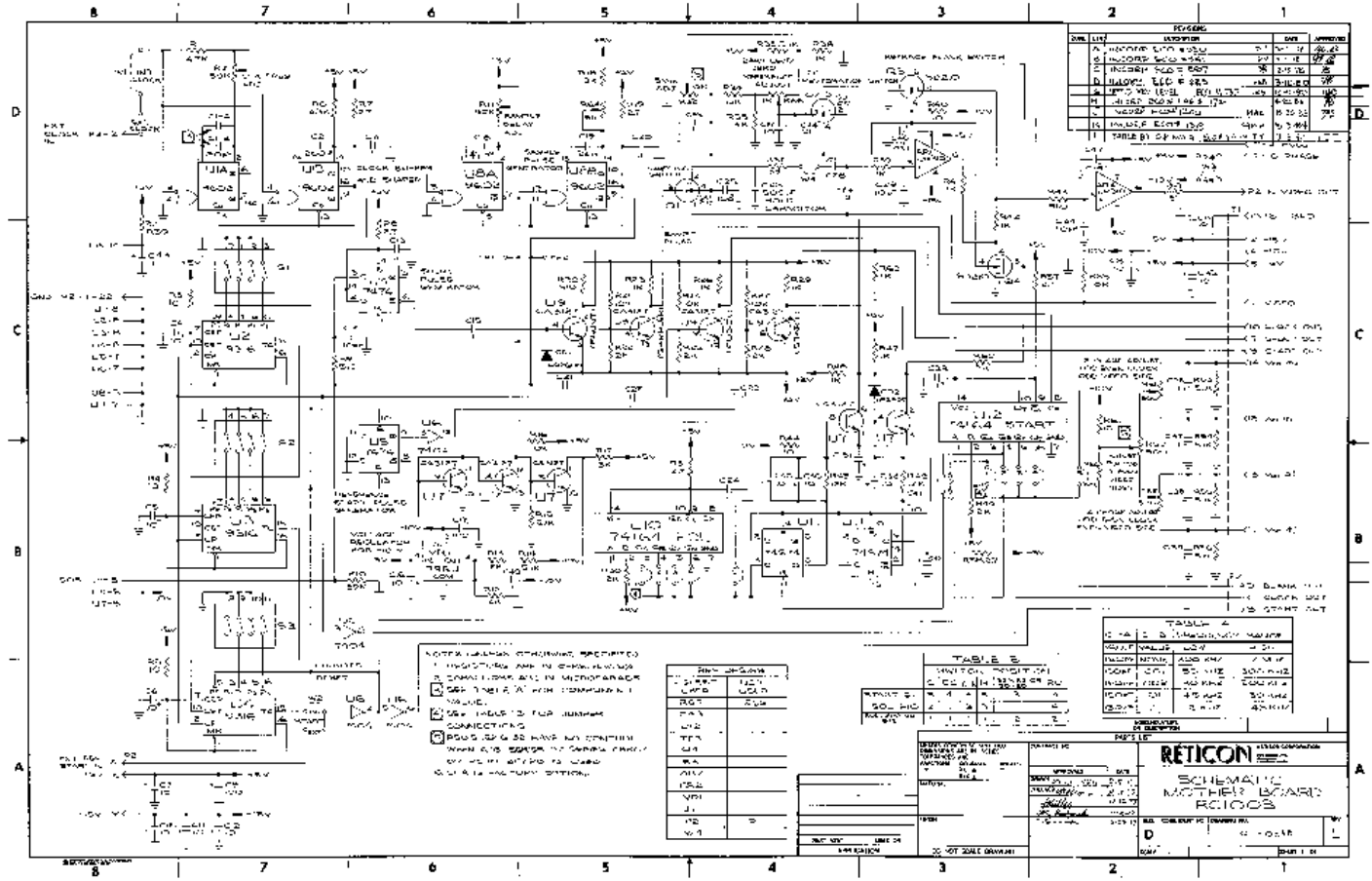
Figure 6. Timing Diagram, RC0100 Series Circuit BDS, H Series Array



* Denotes MOS level signals, all other except video are TTL

Figure 7. Timing Diagram, RC0100 Series Circuit BDS, RA5050A Array


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
INCORP ECO # 515
INCORP ECO # 623
INCORP ECO # 788
INCORP ECO # 1200
INCORP ECO # 1319
CHANGED PER ECO 3443
NOTES: (UNLESS OTHERWISE SPECIFIED)
1. COMPONENT HEIGHT WITHIN STANDOFFS TO BE .31 MAX., REMAINING COMPONENTS MAY BE .50 MAX.
2. LEAD PROTRUSION SHALL BE .05 MAX.
3. FOR SCHEMATIC SEE DWG NO. 02358
4. INK LAMP ASSY REV LETTER IN LOCATION SHOWN USING BLACK INK, COVER WITH ONE COAT OF CLEAR KRYLON #1302A.
5. CUT C21, 23, 31, 33 LEAD AS SHOWN BEFORE INSTALLATION.
6. CAPACITORS W. POINT SELECT
7. MASK HOLES FOR C1-A, EXT START AND CLOCK PRIOR TO DIP SOLDERING.
8. DON'T REMOVE CONDUCTIVE RUBBER RING ON 8020 DEVICES UNTIL BOARD IS READY TO BE PLACED IN ANTI-STATIC BAG PRIOR TO TEST. BOARDS CONTAINING 8020 DEVICES MUST BE IN ANTI-STATIC BAG BETWEEN ALL TEST OPERATIONS AFTER THE RING IS REMOVED.
(FOR NOTE 9 SEE SHEET 2)
4 RC-30
8 RC01
PUT DROP OF SOLDER ON SPLIT PAD NO. 5
PUT DROP OF SOLDER ON SPLIT PAD NO. 2
4 PCB'S
PUT DROP OF SOLDER ON SPLIT PAD NO. 1
PARTS LIST
QTY REQD | CODE IDENT | PART OR IDENTIFYING NO | NOMENCLATURE OR DESCRIPTION
RETICON
RETICON CORPORATION
PCB, EVAL, MTHR; 100 SERIES
SIZE C | CODE IDENT NO | DRAWING NO. ASY-RC01COLNB-01 | REV K1
SCALE 2:1 | C/O - 02358 | SHEET 1 OF 2
MATERIAL SEE P/L
FINISH
DO NOT SCALE DRAWING
APPROVALS | DATE
DRAWN
CHECKED
NEXT ASSY | USED ON
APPLICATION


RETICON
SCHEMATIC
MOTHER BOARD
RC100S
RC0100

055-0285
March 1992

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General Description

The RC0730 is an evaluation circuit board for Reticon's D Series Linear Charge Coupled photodiode arrays and is intended for those who want to gain rapid familiarity with the device's operational characteristics. The board contains the necessary clock generation circuits and analog signal processing circuits for operating the device; however, it has not been optimized for any specific application.

Power Requirements

The board is designed to operate from a triple output linear source supplying +15, +12, and −12V DC. Power is applied to the board through edge connector pins or test points: +5V on H or TP8, +12V on E or TP9 and −12V on A or TP11. Ground connections to the board are on edge connector pins 1 through 22. See "Specifications" section for current and voltage requirements for each of the power inputs.

Specifications

Mechanical:

Dimensions:	4.5" x 10"

Electrical:

Power Inputs:	+12	(± 0.1) V DC @ 275 mA
	−12	(± 0.1) V DC @ 150 mA
	+5	(± 0.1) V DC @ 450 mA
Clock frequency (TP4):		20 MHz maximum 100 kHz minimum

Video outputs (Video load resistor = 3 KΩ):

Discrete video outputs (TP14 and TP16):

Reset level:	6.5V DC
Dark level:	5.8V DC
Saturated output:	−1V ± 20% below dark level

Combined video output (TP18):

Data rate:	10 MHz maximum
DC level:	Adjustable +1 to −1V DC
Saturated output:	+ 2.4V ± 20%
P-P pixel noise:	3 mV (typical)

External clock input:	TTL Compatible
External start input:	TTL Compatible
Clock outputs:	TTL Compatible
Sync output:	TTL Compatible

Operational Description

There are two basic circuits interfacing the image device. The block diagram, Figure1, shows the two circuits separated by a dotted line. The analog signal processing circuit is located on the right side of the dotted line and the digital circuit is located on the left. Refer to schematic diagram 011-0656 and timing diagram 020-0369 for specific circuit and timing information.

Digital Section

The master oscillator U5 provides the master clock (MCLK) signal used to generate all the board timing. Frequency of the MCLK can be adjusted with R1 and C8. The MCLK signal is divided by two with U6 for two phase 50% duty cycle output signals from pins 5 and 6. The crossover points of these signals are controlled with U10 and U11 and then level translated with U12 and U14 to provide the image array main clocks $\varnothing_1$ and $\varnothing_2$. The transfer clock $\varnothing_T$ is derived from the output of the D flip-flop U7 pin 6. The transfer clock (U7 pin 6) is clocked low with the output of the integration counter U3 pin 15. The output of the integration counter also enables the transfer counter U4 to start counting while disabling itself. At the completion of the transfer count sequence, the output of the transfer counter will reset the transfer clock high and enable the integration counters, thus completing the sequence. The transfer pulse is buffered and level translated to provide the image array $\varnothing_T$ clock. The video sampling and multiplex timing is derived from the same source which provides the image array main clocks (U6 pin 5 and 6), gated by NOR circuit U9 and level translated by U20.

Analog Section

The array, driven by the clocks derived in the digital circuit, produces video outputs with amplitudes proportional to exposure (light intensity multiplied by integration time). These signals appear as voltage levels on the video output load resistors R54 and 55 for the combined video or R51 and 52 for the discrete video outputs.

The RC0730 board can be configured to process the video signals in two ways. Selecting jumper settings W6 and W10 will configure the board to output the "odd" and "even" video signals as two discrete outputs. High speed emitter follower transistors Q5 and Q6 provide the buffering necessary for 20 MHz operation. The odd video output is on test point 14 and the even video output is on test point 16.

The odd and even video outputs can be combined into a single output signal by selecting jumper settings W7 and W11. The odd video output is then routed to the high speed video op-amp U17 that provides gain control with R4. The even video output is routed to a second high speed video op-amp U18 with fixed gain. Gain of the odd video channel can then be adjusted using R4 to match the signal level of the even video channel and therefore eliminating gain imbalances in the system. The amplified video signal from U17 and U18 is AC coupled by C74 and

C76 and then DC restored once per line by FET transistors in U19. The DC restoration level is adjustable for the odd and even video channels with R5 and R6, respectively. The odd and even video channels are combined by alternately sampling, holding and multiplexing the two signals with the FET switches in U21. While the odd video channel is being sampled onto hold capacitor C86, even video is multiplexed to the high impedance output buffer U22 from hold capacitor C91. During the next cycle of the clock, even video is sampled while odd video is multiplexed to the output stage. The combined, sampled and held video signal is buffered with emitter follower transistor Q8 and can be monitored on test point 18.

Input Signals

In the usual mode of operation the RC0730 evaluation board generates all the necessary signals to operate the image array; however, the board does have provisions for accepting external master clock and/or start signals. These external inputs can be used to synchronize the image array output to the user's system.

Clock Input (pin W/TP2)

The RC0730 can be externally clocked by selecting jumper setting W5 and applying a TTL clock signal on this input. The combined video data rate (at TP18) will be equal to the frequency of this clock. The timing of this signal is non-critical with the exception of a minimum low time of 25 ns. Frequency of this signal should be limited to 20 MHz maximum.

Start Input (pin P/TP5)

By selecting jumper setting W2 and inputting a TTL signal on this input, the array transfer clock and thus the start of a readout and new integration period will be externally controlled. A low to high transition will enable the transfer counter, U4, to count. A minimum high time of 50 ns is required to meet the $\varnothing_1$ to $\varnothing_T$ array clocking requirements. The high to low transition of the start input signal will set the array $\varnothing_T$ clock active and thus start a new integration period when $\varnothing_T$ ends. The terminal count from U4 will then set $\varnothing_T$ low to end the transfer sequence and start the video read-out. Care must be taken to ensure that the array clock timing requirements are met when the external start input is used.

Line Reset Input (TP12)

The external Line Reset function can be implemented by connecting jumper W9. This connects the image array Line Reset input to TP12. A reset signal (active high) can be applied to this terminal to simultaneously reset the photodiodes at any time during scan. Operation and timing of this input is shown in the timing diagram, Figure 2. The positive and negative voltage swings of this signal will need to be adjusted to compensate for image array performance variations.

When operating the image array in the "normal" (non-line reset) mode, integration time is measured from falling edge to falling edge of $\varnothing_T$. When employing line reset, integration time is measured from the falling edge of $\varnothing_{LR}$ to the falling edge of $\varnothing_T$. Image array output is directly related to integration time. Therefore if integration time is "halved" by invoking $\varnothing_{LR}$ while light intensity remains constant, video output will be halved. This is important to bear in mind when adjusting the peak positive excursion of the $\varnothing_{LR}$ input (VLRH). Typically VLRH would be from +2.5V to +4.5V (+3.5V, nominal) above ground potential. For proper array anti-blooming characteristics the $\varnothing_{LR}$ negative swing (VLRL) typically ranges from +1.5V to +2V from ground potential.

As can be seen, the $\varnothing_{LR}$ input is relatively critical in terms of timing and amplitudes. This array input is also sensitive to "glitches" on the rising and falling edges of $\varnothing_{LR}$. It is recommended that user circuitry develop a $\varnothing_{LR}$ signal that is synchronous with Start or Sync, that VLRL and VLRH be adjustable and that $\varnothing_{LR}$ be free of glitches and "ringing."

Output Signals

Sync (pin K/TP7)

This is a TTL output for the purpose of synchronizing an oscilloscope or user circuitry to the array line scan time. The timing and polarity of this output is shown in timing diagram 020-0369.

Clock Output (pin T/TP4)

This is a TTL output for the purpose of monitoring the master clock frequency of the board. It may be used for re-sampling purposes such as A/D conversions. The combined video data rate (TP18) is equal to the frequency of this clock while the discrete video output rate (TP14, TP16) is one-half this rate.

Scan Buffer Output (pin Z/TP1)

The Scan Buffer output is a signal produced from the image array which provides pulses that are synchronized to the timing of the first and the last pixel of the image array. The timing of this signal is shown in timing diagram 020-0369. The scan buffer output signal can be used to synchronize external circuitry with the time in which the array is outputting active video information.

Discrete Video Outputs (TP14 and TP16)

The separate odd and even buffered video outputs can be monitored on these test points. The odd video is on TP14 and the even is on TP16.

Combined Video Outputs (TP18)

The combined processed video signal can be monitored at this test point.

Alignment

RC0730 evaluation boards, as shipped from the factory, have been thoroughly aligned with either the user's array or with a typical test array. Upon applying power to the board, the following procedure should be followed to optimize circuit performance. Proper alignment of the RC0730 can be accomplished only when the board is driven with power as specified in this document. Photographs in this document were taken at a clock frequency of 5 MHz.

Procedure

Connect the power supplies to the RC0730 evaluation board in accordance with the pin-out listed in the section "Power Requirements." Install the D Series image sensor in the U13 socket, making sure of correct orientation. Apply power to the board.

Master Clock

The RC0730 master clock may be derived from the on-board clock oscillator or from an external source. If the on-board clock generator is desired, select jumper setting W4. From Table A select the capacitor for the frequency range desired and install it in the Berg pin sockets for C8. (The RC0730 is factory shipped with a 47 pF capacitor installed.) With an oscilloscope, monitor the clock output on pin T or TP4 and adjust potentiometer R1 for the desired data rate.

If an external master clock is desired, select jumper setting W5 and input the external clock on edge connector pin W or TP2.

Table A

Capacitor (C8) Value (pF)	Clock Frequency Range TP4 (MHz)
10	10 – 20
47	3 – 10
100	1 – 4
250	.6 – 2
500	.2 – 1

Start/Sync

The RC0730 start pulse repetition rate which controls integration (line scan) time may be derived from the on-board counters or from an external source. If the on-board counters are desired select jumper setting W3. The integration time is controlled by the presetting of a 4-bit Transfer Counter and a 12-bit Integration Counter. The transfer counter, programmed by SW4, should be preset to provide a minimum of .2 µs transfer time. The transfer counter must be set to a value of 2 or greater; with an oscilloscope, monitor ϕ_T signal on pin 22 of U13. Adjust the Transfer Counter value using SW4 for the desired transfer time (high level) or a minimum of .2 µs. The integration counter, which is controlled by SW1, SW2, and SW3, can then be preset to the desired integration time. The minimum count for the integration counter is the array length plus 15 counts. Adjust the binary weighted switches SW1, SW2, SW3 for the desired integration time (low level).

When using master clock frequencies of 1 MHz or less, it is suggested that the transfer counter be programmed to a count of 2. At frequencies greater than 1 MHz, a transfer count of 15 is recommended.

If external start operation is desired, select jumper setting W2 and input the externally generated start signal at TP5 or on edge connector pin P in accordance with the timing shown in 020-0369.

NOTE: Use the sync output to synchronize the oscilloscope for the remainder of this procedure.

Combined Video Output (TP18)

To combine the two video outputs from the image array into one output signal, select the jumper settings W7 and W11. With an oscilloscope, monitor the video output of TP18. Completely darken the array (U13) by placing a suitable (non-abrasive) opaque covering over the window. With the vertical sensitivity of the oscilloscope set to .1V/div. and the vertical input coupling to GND, adjust the ground reference of the scope trace so that it is on the graticule centerline. Set the channel coupling to DC. Adjust potentiometer R5 and R6 until video dark level is at ground and the odd/even pattern is minimized. See Photos 1 and 2. There will be some interaction between R5 and R6 during this adjustment and therefore it will require several adjustments of each potentiometer. To fully optimize this adjustment it will require increasing the verticle sensitivity of the oscilloscope.

Remove the opaque material covering the array. With a suitable light source (preferably a steady state DC powered source), illuminate the array to approximately 50% of saturation. Adjust the gain potentiometer R4 until the odd/even pattern is removed in the illuminated video signal. See Photos 3 and 4. Since this adjustment may affect the previous dark level adjustment, repeat the Dark and Light adjustments until the odd/even patterns are removed throughout the light/dark range.

NOTE: This output is limited to 10 MHz video data rate. For optimum performance capacitive loading of this output should be <20 pF.

Anti-Blooming Control

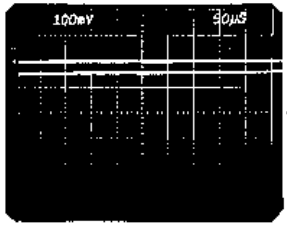
Select jumper setting W8. Adjust potentiometer R2 for a voltage of 0V on pin 10 of U13. Illuminate the image array to an exposure level beyond saturation. The output video signal will appear as shown in Photo 5. The video line will bloom during the retrace time as shown. The degree of blooming will depend on exposure level. Adjust potentiometer R2 until the video line blooming is minimized as shown in Photo 6. The saturated video output signal will be approximately 2 - 2.3V for the correct adjustment of R2.

Discrete Video Outputs (TP14 and TP16)

Select jumper settings W6 and W10. With an oscilloscope monitor the video output signals on test points TP14 and TP16. Illuminate the array to approximately 50% of saturation. The signals should appear as shown in Photo 7.

Scan Buffer Output

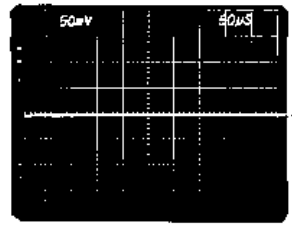
With an oscilloscope, monitor the scan buffer output signal (TP1 or pin Z) and the video output signals (TP14 and TP16). Adjust potentiometer R3 until there is a single pulse coincident with the first and the last video pixel. Refer to Photo 7 for an example of the proper adjustment of this signal. The photos below are expanded views of the first and last pixels of the image array showing the timing of the Scan Buffer output pulses.



DC Level Mis-adjusted

0 Volts DC

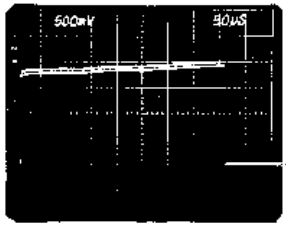
Photo 1



DC Level Adjusted Correctly

0 Volts DC

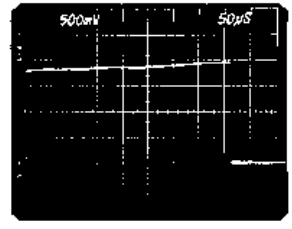
Photo 2



Gain Adjusted Incorrectly

Dark Level (0 Volts DC)

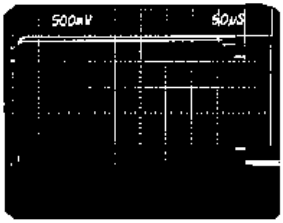
Photo 3



Gain Adjusted Correctly

Dark Level (0 Volts DC)

Photo 4

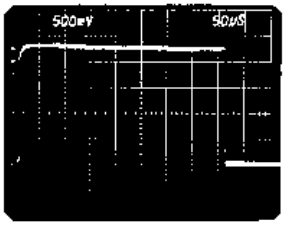


Saturated Output without Blooming Control (V_{LR} = 0 Volts)

Dark Level (0 Volts DC)

Note Blooming of Dark Level

Photo 5



Saturated Output with Blooming Control (V_{LR} = 1.73 Volts)

Dark Level (0 Volts DC)

Photo 6

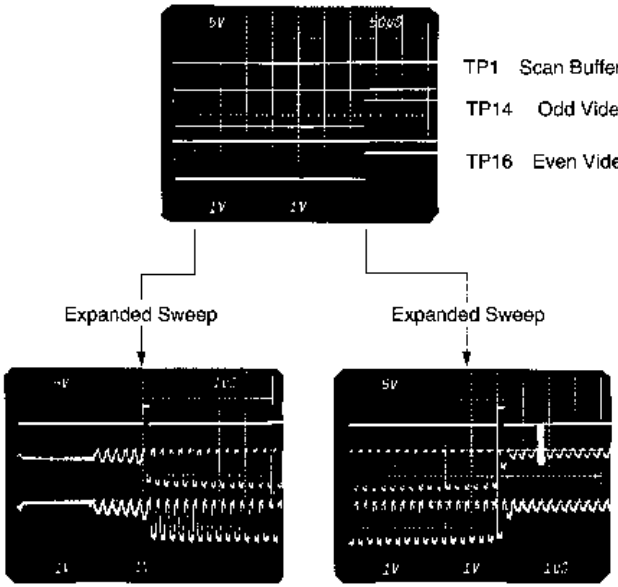


Photo 7

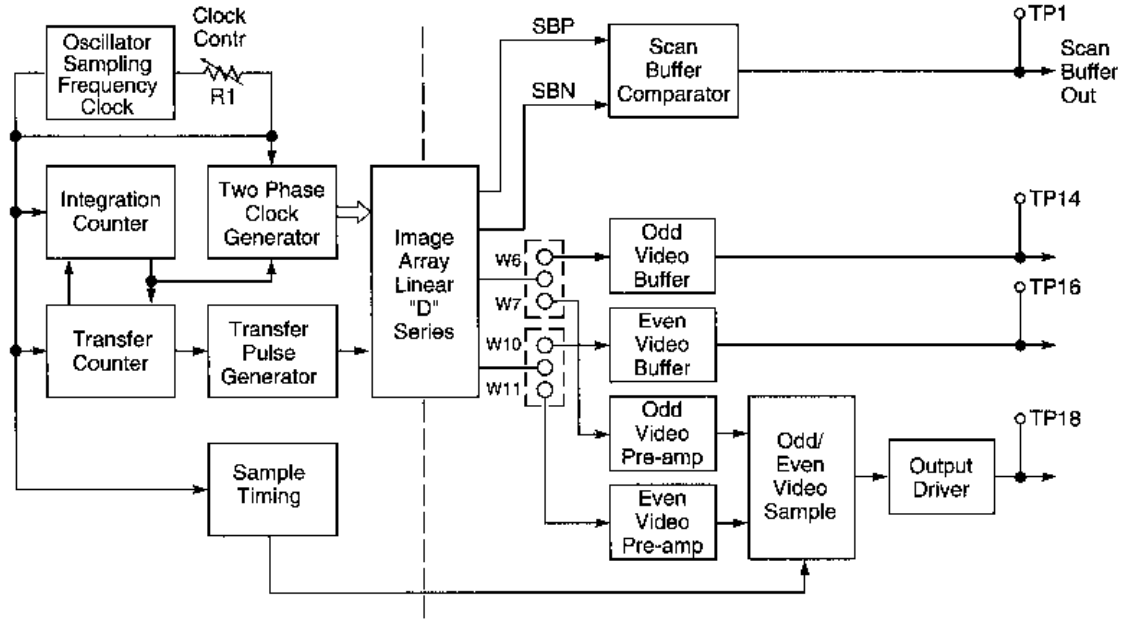
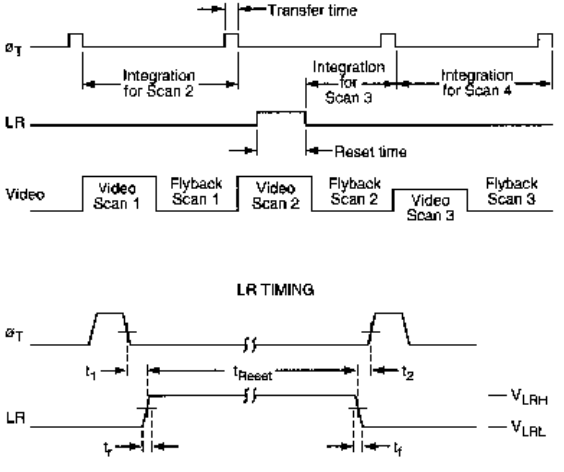
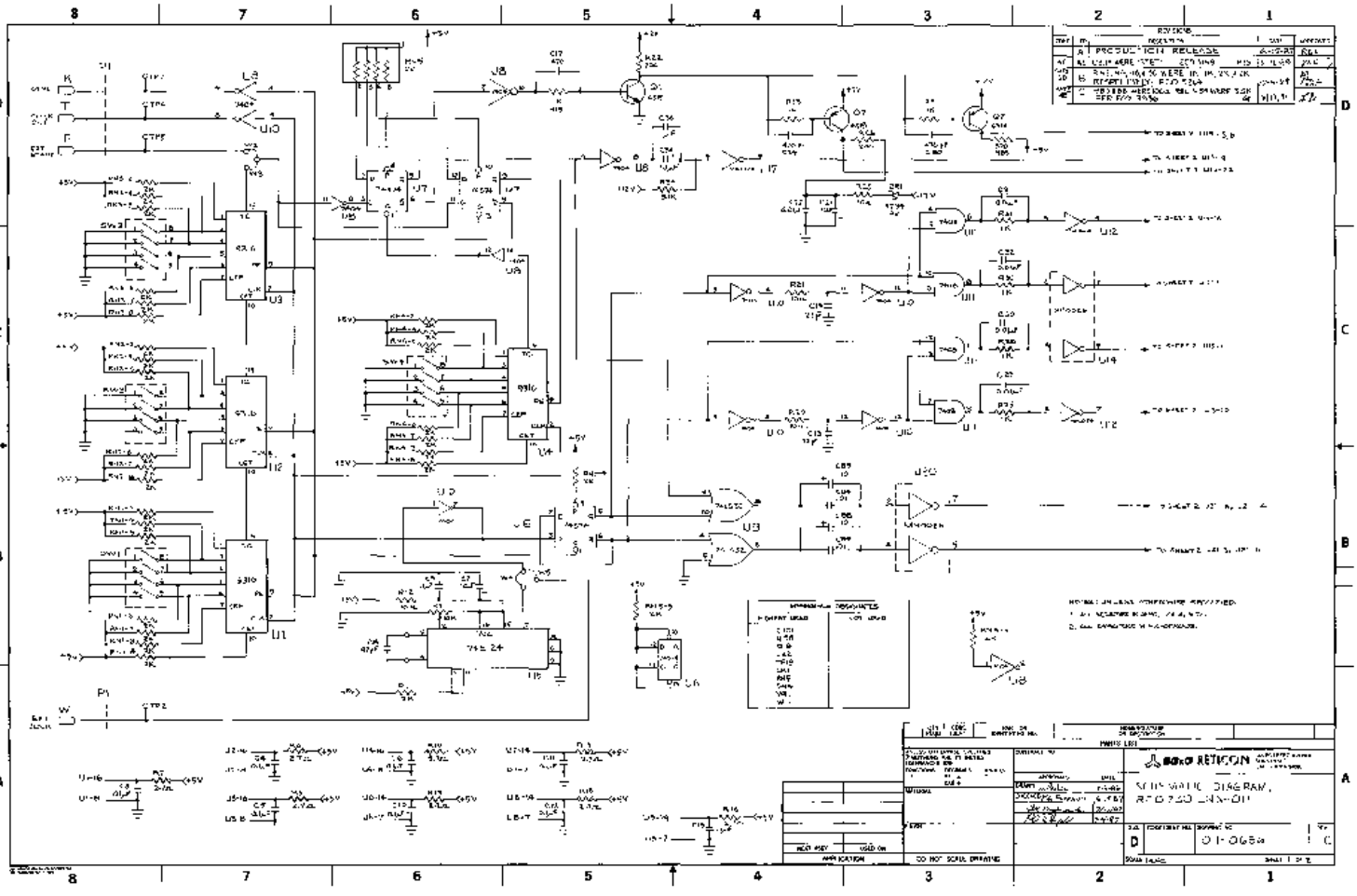


Figure 1. Block Diagram

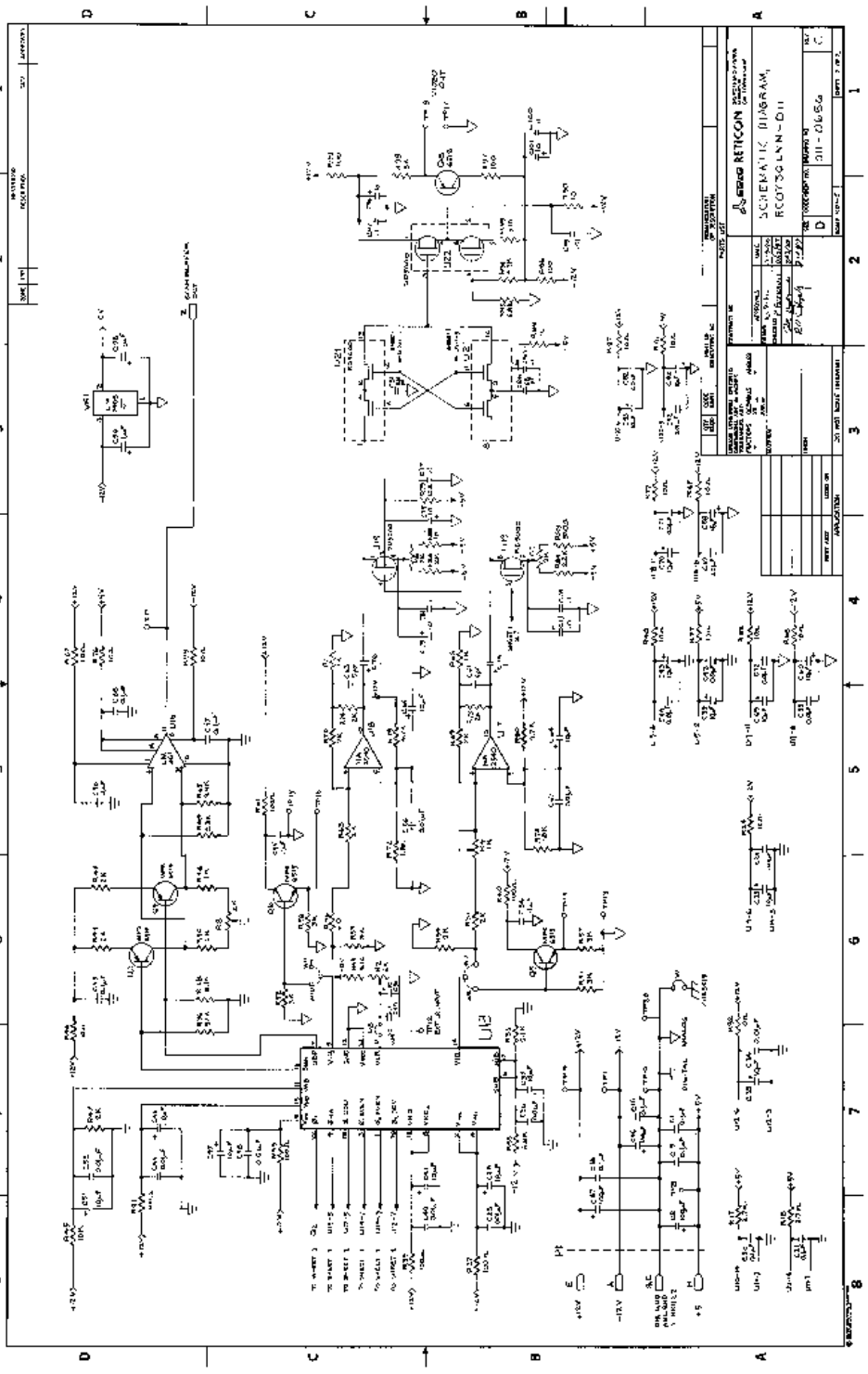


	Min	Max	Units
t_r	10	50	ns
t_f	10	50	ns
t_{RESET}	8	-	µs
t_1	200	-	ns
t_2	200	-	ns
V_{LRH}	+2.5	+4.5	V
V_{LRL}	0	+2.0	V

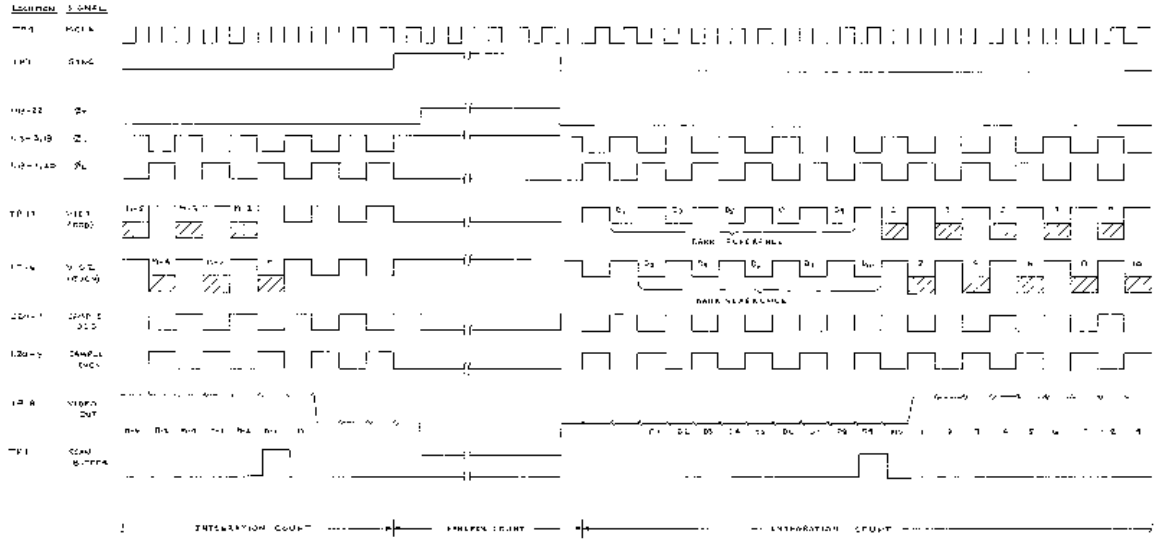
Figure 2. Timing Diagram, RC07030 Line Reset



RC0730



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVAL
	A	PRODUCTION RELEASE	6-17-87	RSF
D2	B	TIMING OF EOM BUFFER PER ECO #4447	3-5-92	KJT



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± .XXX ±	CONTRACT NO	RETICON CORPORATION		
MATERIAL	APPROVALS / DRAWN L. Ramsey / DATE 6-17-87 / CHECKED / DATE	TIMING DIAGRAM, RC0730		
FINISH		SIZE B	CODE IDENT NO.	DRAWING NO. 020-0369 REV B
NEXT ASSY USED ON		SCALE		SHEET 1 OF 1
APPLICATION	DO NOT SCALE DRAWING			

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RC0730

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General Description

The RC1000 Mother and RC1001 Satellite evaluation boards form a set designed to provide all of the necessary signals and video processing circuitry to operate the Reticon S and T Series Linear Photodiode Arrays. This evaluation board set provides the user an easy means to evaluate the operation of these linear photodiode arrays. External Start and Clock control inputs are provided at the edge connector of the mother board to allow synchronization of the board operation with a user system.

The evaluation board set has been designed to provide good noise performance at a reasonable cost. The Sampled and Held video output signal will have a typical dynamic range of 4000:1 (saturated output/p-p pixel noise). With care in shielding of the satellite board from external electro-magnetic radiation, even higher levels of performance can be seen. In order to achieve this level of performance the video data rate is limited to a value lower than the capability of the photodiode array itself.

The satellite board may be remotely located from the mother board by extending the analog and digital cables. Some degradation in noise performance may be seen with increasing cable lengths. Shielding of the video signal lines from RF signals is suggested when using extended cables.

Provision for cooling of the photodiode array using a thermoelectric cooler is possible by means of the access hole located directly beneath the array.

Specifications

Mechanical		
Dimensions:	Mother Board	4.5 x 8.0 inches
	Satellite Board	4.5 x 2.0 inches
Connectors:	Mother Board Edge	22/44 pin dual
	Satellite Digital	16-pin ribbon
	Satellite Analog	6 pin
Electrical		
Power Inputs:	+15 analog	+15V DC (± 0.1) @ 75 mA
	+15 digital	+15V DC (± 0.1) @ 100 mA
	+ 5 digital	+ 5V DC (± 0.1) @ 500 mA
	−15 analog	−15V DC (± 0.1) @ 75 mA
	−15 digital	−15V DC (± 0.1) @ 100 mA
Frequency Range:	250 kHz maximum	
Video Output:	Saturation	+6V ± 20%
	Peak to Peak Pixel Noise	1.5 mV typ.
	DC Dark Level Range	+300 mV to −600 mV
Clock Output:	Pulse Width:	2.5 µsecond negative
	Amplitude:	TTL Compatible
Ext. Clock Input:	Pulse Width:	50 nanosecond minimum
	Amplitude:	TTL Compatible
Ext. Start Input:	Pulse Width:	See Timing Diagram
	Amplitude:	TTL Compatible
Sync Output:	Pulse Width:	See Timing Diagram
	Amplitude:	TTL Compatible

NOTE: Peak-to-peak pixel noise is dependent upon a number of parameters. Careful attention should be given to the following parameters for optimum noise performance.

1. Power supply noise and ripple levels should be <1mV p-p.
2. Utilize low impedance power supply connections.
3. Minimize the lengths of the analog and digital cables.
4. Shield the board from electro-magnetic radiation sources.

Power Requirements

The board set is designed to be operated from a triple output source supplying +5V, +15V and –15V to the circuit's separate analog and digital sections. For lower noise operation, power can be supplied to the analog and digital sections of the mother board from separate sources with a common low impedance ground connection at the PC board edge connector. (See specifications section for current and voltage requirements for each power supply input.) The edge connector pin assignments are shown below.

Signal	Symbol	Edge Pin	Test Point
+15 analog	+15VA	C	7
+15 digital	+15VD	H	5
+5 digital	+5V	K	4
–15 analog	–15VA	A	8
–15 digital	–15VD	E	6
Ground		1-22	10

Operational Description

There are two basic circuits interfacing the photodiode array. Figure 1 is a simplified block diagram that shows the two sections separated by a dotted line. The digital section is on the left and the analog section is on the right. The circuitry contained on the satellite board is shown within the center box. Refer to the schematic diagrams of the RC1000LNN–011, –020 and RC1001LNN–011 for the detailed circuit of the block diagram and the timing diagram for functional timing information.

Digital Section

The one-shot oscillator and pulse width control (U11) provide the master clock (MCLK) signal used to generate all the board timing. Frequency of the MCLK can be adjusted with R35. The integration counters (U8, U9 and U10) are clocked at the MCLK frequency and provide an output pulse on pin 15 of U10 that is active high for 1 out of N MCLK cycles. N is determined by the binary weighted count of the setting of switches SW1, SW2, and SW3. This output signal (MSTART) along with MCLK are inputs to the clock and start generator (PAL U7). U7 outputs a "start pulse" and four properly timed clock phases which are then level translated and sent to the photodiode array.

Analog Section

The analog portion of the circuit begins on the satellite board with the active and dummy video outputs of the photodiode array. These outputs are each amplified by transistor amplifiers Q1, Q2 and Q3 for the active video and Q4, Q5, and Q6 for the dummy video. The amplified video signal lines are then routed to the differential integrator (U1) on the mother board. The integrator is reset once each pixel by the signal generated by U7 and level translated by U5. The output of the integrator is AC coupled and then DC restored by Q3 to an adjustable DC level set by R1. The video signal is DC restored synchronously with the integrator reset. The DC restored video signal is buffered with a unity gain amplifier (U2) and then sampled and held by Q5 and C24. The S&T jumper (E4 – E6) controls the sampling process. For S Series arrays, a sample pulse occurs every MCLK cycle. T Series device video is sampled once for every two MCLK cycles. Q4 serves to reduce any glitches introduced by the sampling process. The sample timing and pulse width is developed by one shot U12. The sample and held video signal is buffered with unity gain amplifier U3 and sent to the output BNC connector J1.

Input Signals

In the usual mode of operation, the RC1000 mother board generates all the necessary signals to operate the photodiode array. The board has provisions for accepting an external master clock and/or start signals. These external inputs can be used to synchronize the array output to the user's system.

Ext. Clock Input (pin X/TP1)

The RC1000 mother board can be externally clocked by selecting jumper settings E2-E3 and applying a TTL clock signal on this input. Timing of this signal is non-critical since the pulse width will be determined by the one shot U11. The frequency of this signal will determine the video output pixel rate and should not exceed 250 kHz.

Ext. Start Input (pin M/TP3)

The read out operation of the photodiode array can be externally controlled by selecting jumper settings E8-E9 and inputting an active high TTL signal on this input. The external MSTART must have a minimum positive pulse width of 200 nanoseconds. The falling edge of EXT MSTART must occur no sooner than 20 nanoseconds after the falling edge of MCLK at TP-9. The minimum number of master clock cycles between start pulses must be the array length plus 4 counts for S Series arrays and twice the array length plus 4 counts for T Series arrays. The number of clock cycles between start pulses must be divisible by 4.

Output Signals

Clock Output (pin U/TP9)

This output is provided to synchronize user circuitry to the RC1000 BNC video pixel data. It may be used for re-sampling purposes such as A/D conversions. J1 video pixel data is stable at the rising edge of MCLK at TP-9. The MCLK output is at TTL levels.

Sync Output (pin P/TP2)

This is a TTL output signal for the purpose of synchronizing an oscilloscope or user circuitry to the photodiode array line scan time. The timing and polarity of this output is shown in Figure 2.

End of Scan (EOS) Outputs (Satellite Board Test Points)

The photodiode array produces an output pulse from each (odd and even) shift register at the time when the last pixel is being read out. These signals can be monitored at the test points provided on the satellite board. Timing and polarity is shown in Figure 2. Capacitive loading of these output signals will affect the fall time.

Video Output (J1)

The final sampled and held video output signal can be monitored at this output. The timing of this signal is shown in Figure 2.

Alignment

The RC1000 and RC1001 boards as shipped from the factory have been thoroughly aligned with either the user's array or with a typical test array. Upon applying power to the board, the following alignment procedure should be followed to achieve optimum circuit performance. Proper alignment of the board set can be accomplished only when the board is driven with power as specified in this document.

The photographs used in this alignment procedure were taken using an RC1000LNN–011 mother board and an RL1024SAQ–011 array. The MCLK frequency was set at 100 kHz. The MSTART repetition rate was set at 1024 +128 for ease in recognizing "flyback" time. Ground potential for all photos is the oscilloscope graticule centerline.

Procedure

Connect the power supplies to the mother board in accordance with the pin out as listed in the "Power Requirements" section. Install a Photodiode Array in the socket of the satellite board. Apply power to the board.

If the array in use is an S Series, the S&T jumper, on the RC1000, should be set from E4 to E5. For T Series arrays, set this jumper from E5 to E6.

MClk

The RC1000 mother board Master Clock may be derived from the on-board oscillator or from an external source. If the on-board clock generator is desired, select jumper setting E1-E2. With an oscilloscope, monitor the clock oscillator output on pin 6 of U11. Adjust potentiometer R35 for the desired video output data rate. If external master clock operation is desired, select jumper setting E2-E3 and input a clock signal on pin X of the board edge connector.

MStart

The RC1000 mother board integration time (start pulse) may be derived from the on-board integration counters or from an external source. If internal operation is desired, select jumper setting E7-E8. The integration time will then be controlled with the binary weighted switch settings of SW1, SW2 and SW3. With an oscilloscope, monitor the sync output on pin P of the board edge connector and set the integration time for the desired rate. S Series devices require a minimum start repetition rate of n + 4, where n equals the number of array photodiodes. The minimum number of counts for the setting of the switches for T Series arrays is (n x 2) + 4.

If external integration time control is desired, select jumper setting E8-E9 and input the start signal on pin M of the edge connector in accordance with the conditions described in the "Input Signals" section.

Use the Sync output to synchronize the oscilloscope for the remainder of this procedure.

Dark Fixed Pattern

With an oscilloscope, monitor the video output on the BNC connector J1. Completely darken the array. Set the vertical sensitivity of the oscilloscope to .5V/division.

With R1, R23, R24 and R25 set to the center of their ranges, dark output video might appear similar to that in photo 1. Adjust the "even pixel offset adjust" potentiometer, R23, until the even pixels appear as in photo 2. Adjust the "odd pixel offset adjust" potentiometer, R25, until the odd pixels appear similar to photo 3. Increase the verticle sensitivity to 200 mV per division. Alternately adjust R23 and R25 until the odd and even pixel offset is minimized as shown in photo 4. Increase the verticle sensitivity to 100 mV per division. Adjust the "odd/even pixel balance adjust" potentiometer, R24, until the dark fixed pattern is minimized as in photo 5.

Dark Video DC Level

Increase the verticle sensitivity to 50 mV per division. Adjust potentiometer R1 until the DC level of the video output trace is at ground level as shown in photo 6.

Illuminate the array with a suitable DC light source. The "saturated" video output should appear similar to that of photo 7.

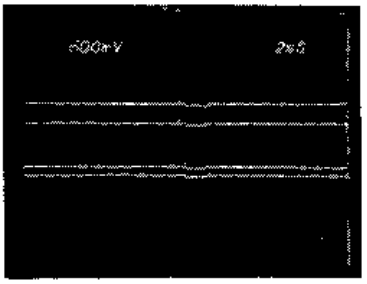


Photo 1

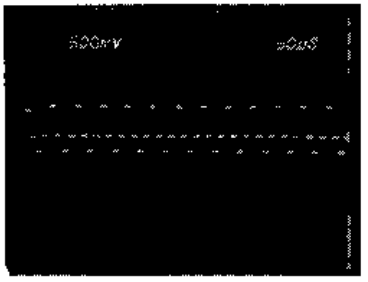


Photo 2

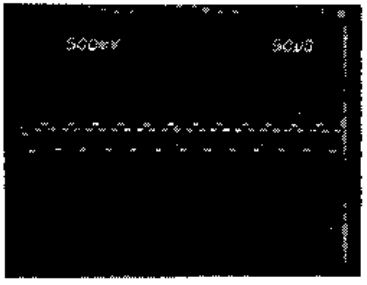


Photo 3

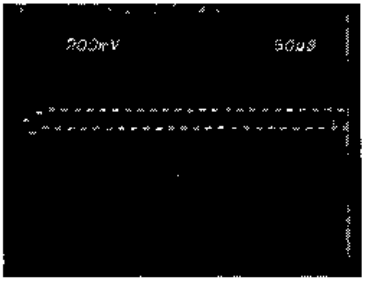


Photo 4

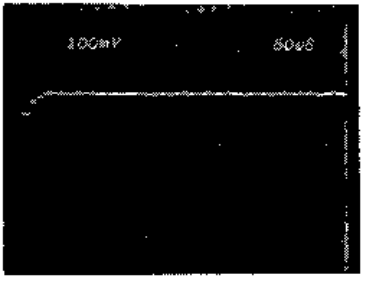


Photo 5

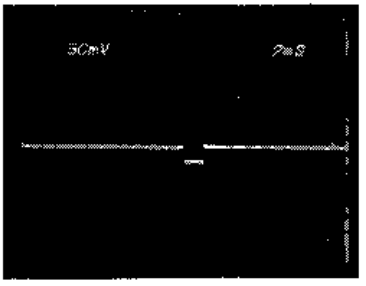


Photo 6

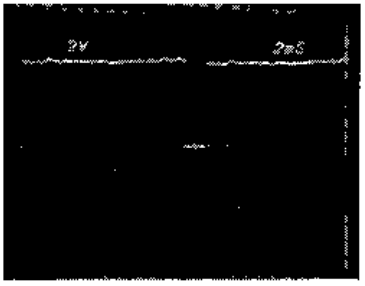


Photo 7

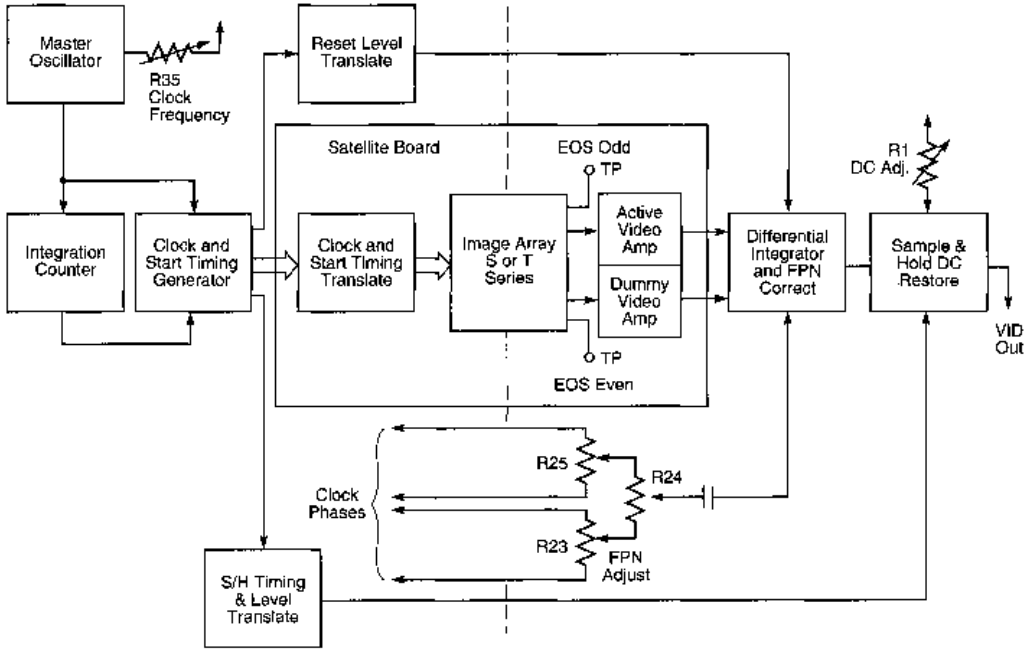
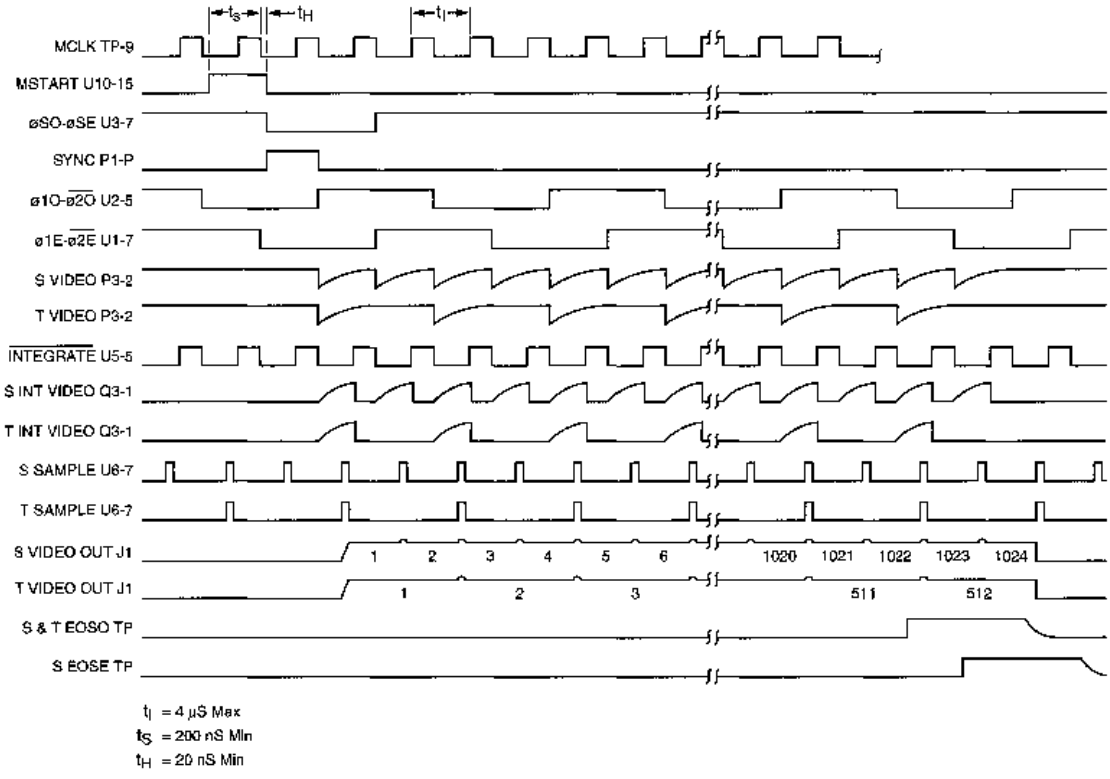
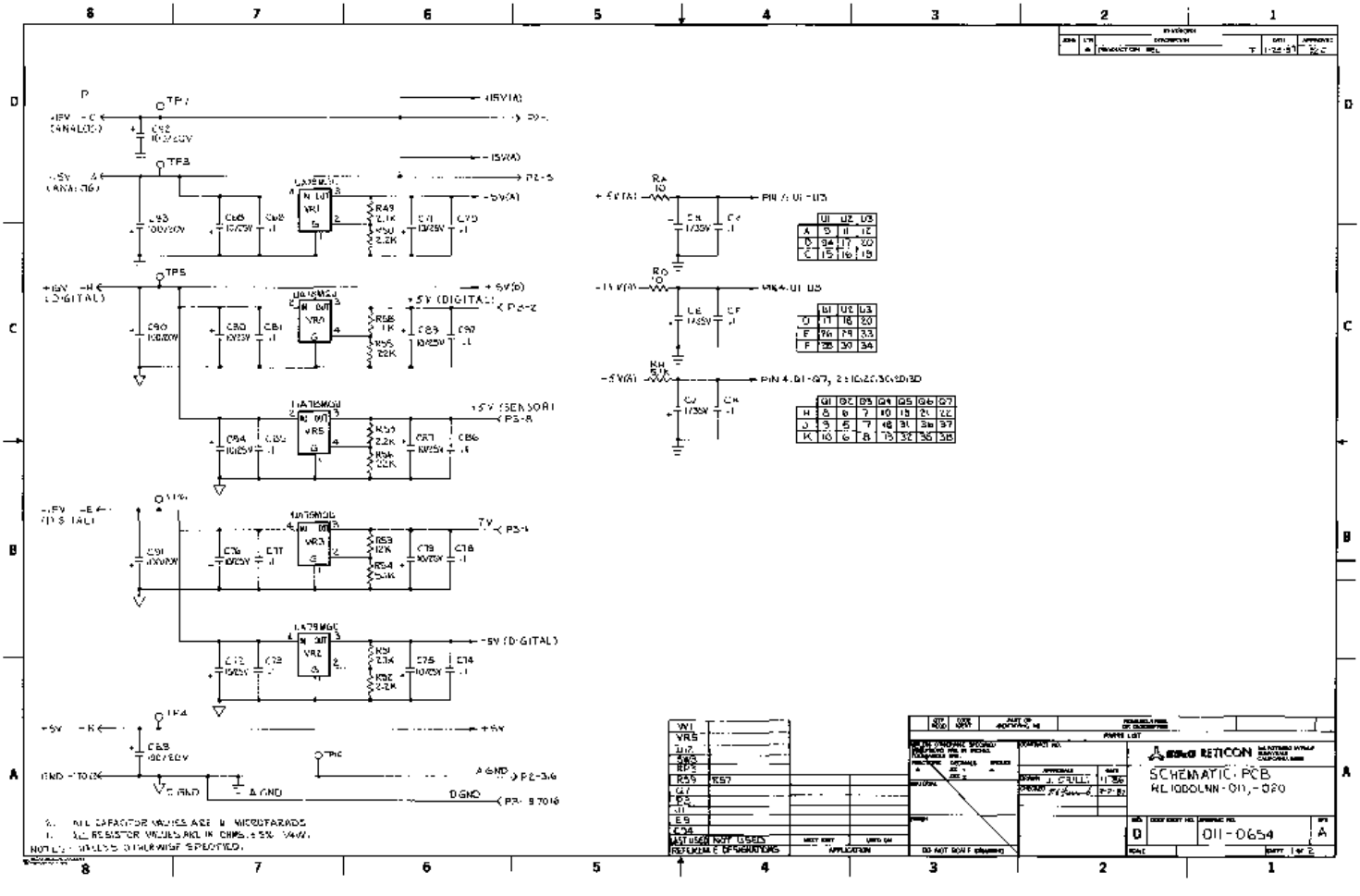


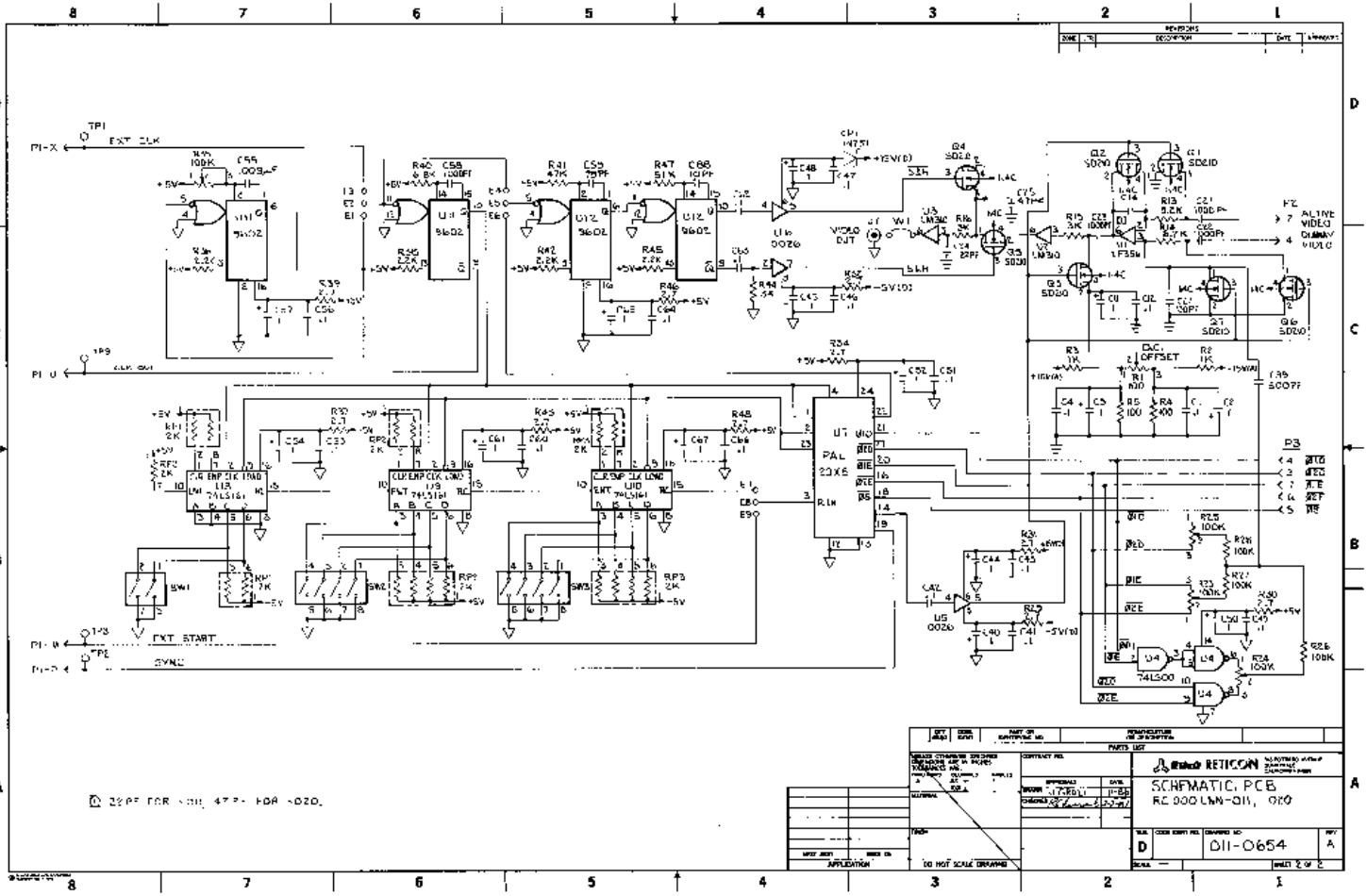
Figure 1. Block Diagram

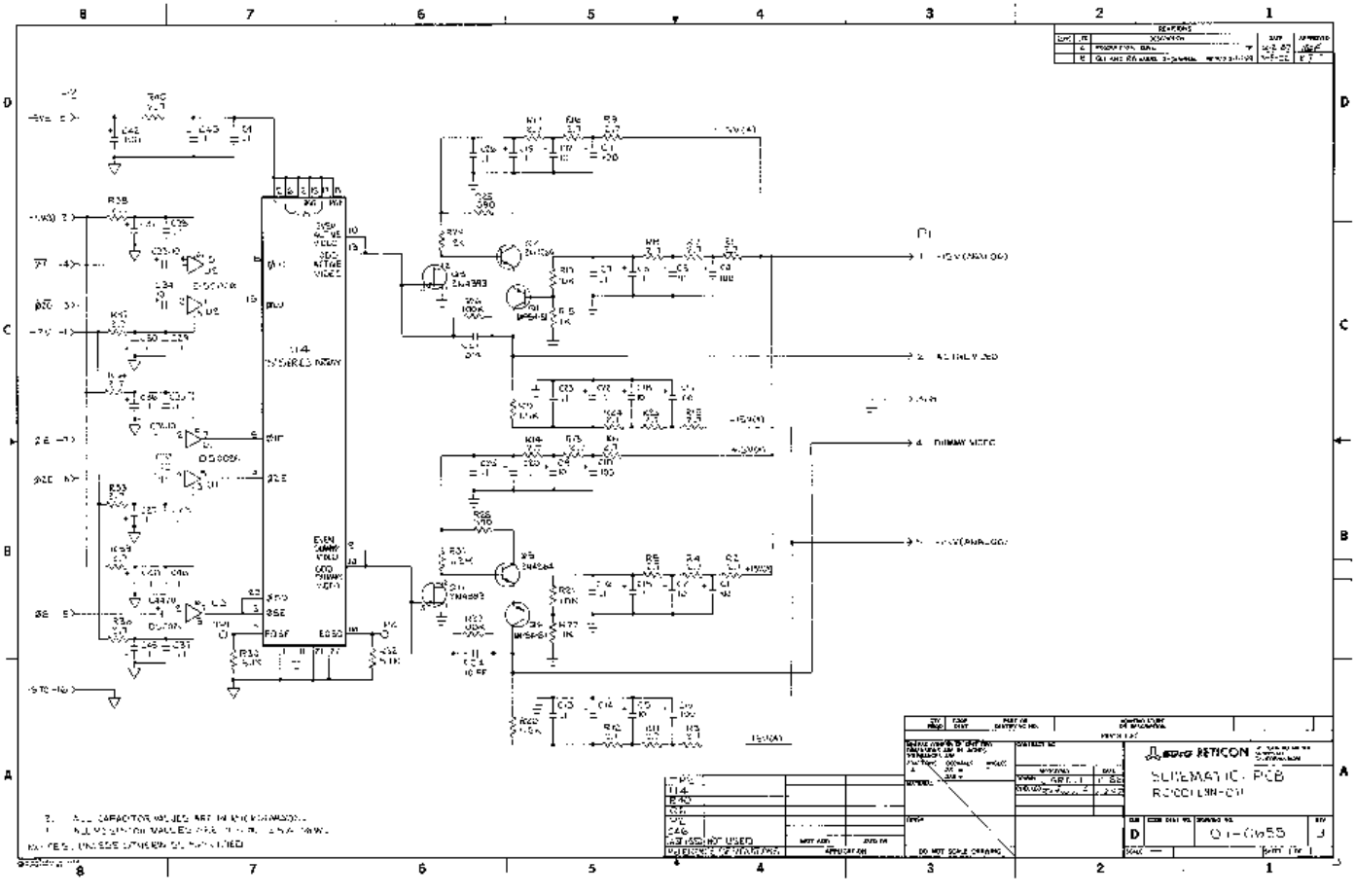


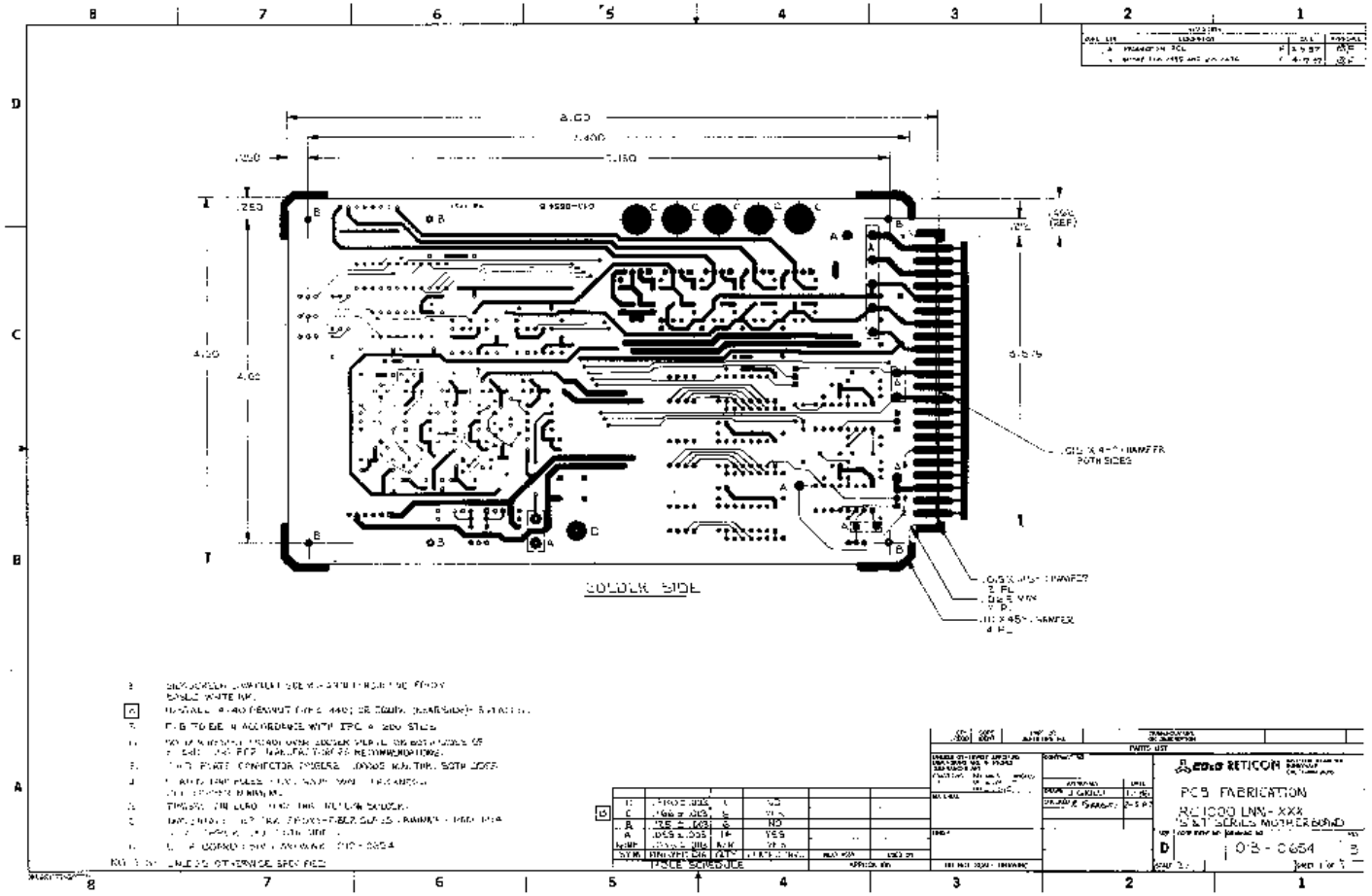
t_I = 4 µS Max
t_S = 200 nS Min
t_H = 20 nS Min

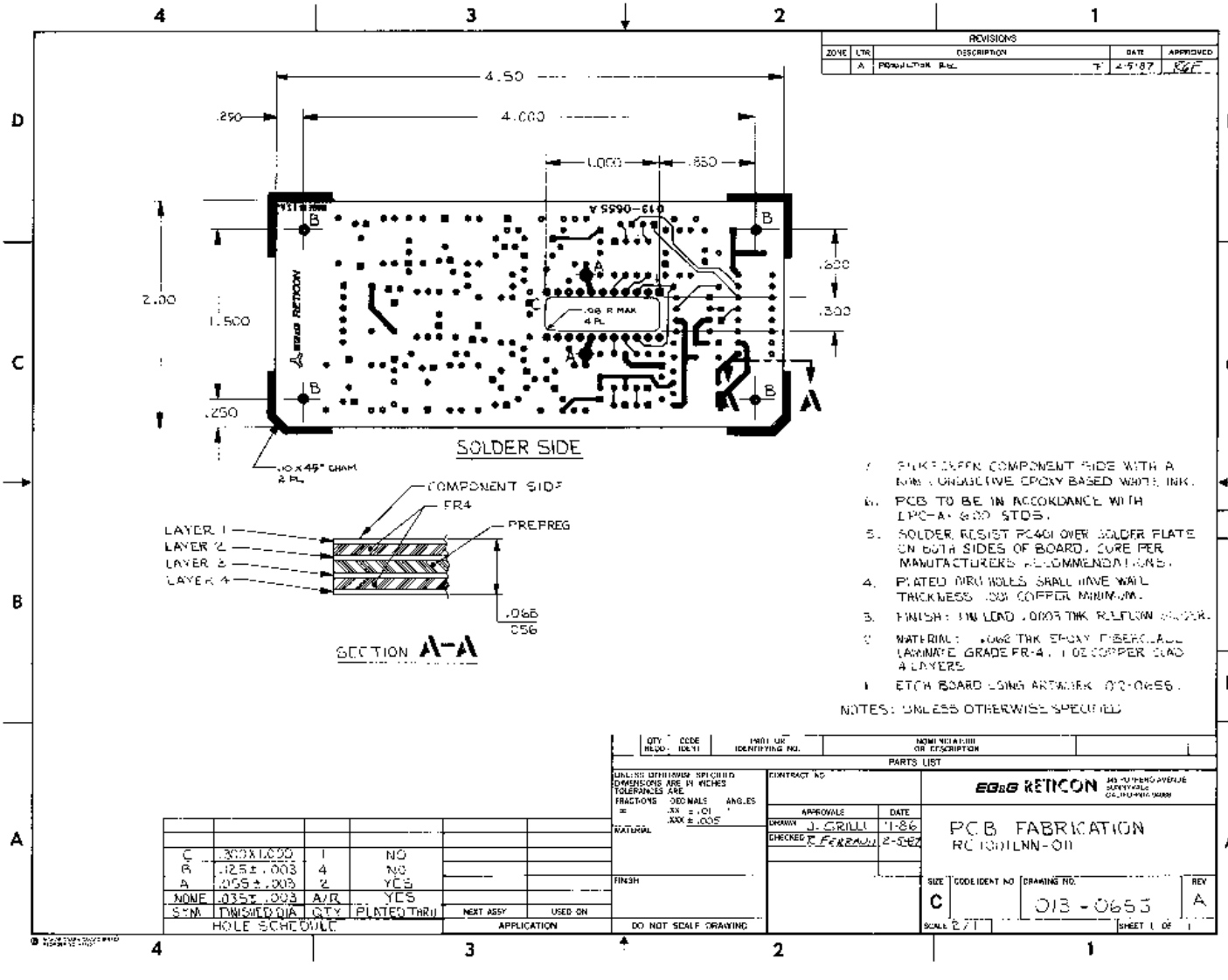
Figure 2. Timing Diagram


SCHEMATIC PCB
RC1000LNN-011,-020
011-0654
RETICON


SCHEMATIC, PCB
RC1000 LWN-011, 020
011-0654
D
A
RETICON
PARTS LIST
DO NOT SCALE DRAWING
EXT CLK
EXT START
SYNC
PAL 20X6
74LS00
VIDEO OUT
ACTIVE VIDEO CHANNEL VIDEO
D.C. OFFSET


SCHEMATIC - PCB
RC001.SCH-01
01-0055


8.00
7.400
7.150
.250
.250
4.150
4.00
.500 (REF.)
SOLDER SIDE
PCB FABRICATION
RC1000 LNN-XXX
G & T SERIES MOTHERBOARD
013-0654
PRICE SCHEDULE



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General Description

The RC1030LNN is a general purpose evaluation circuit designed to provide all of the necessary timing signals and video processing circuitry to operate the Reticon SB and TB Series Linear Photodiode Arrays. The evaluation board provides the user an easy means to evaluate the operation of these linear photodiode arrays. External Start and Clock control inputs are provided at the edge connector of the board to allow synchronization of the board operation with a user system.

The evaluation board has been designed to provide good noise performance at a reasonable cost. The Sample-and-Held video output signal will have a typical dynamic range of 4000:1 for the SB device and 8000:1 for the TB. Dynamic range is defined as the saturated output divided by the peak-to-peak pixel noise. In terms of RMS noise, the dynamic range would be approximately 5 times greater or 20000:1 for the SB and 40000:1 for the TB. In order to observe this type of performance, power supplied to the board must be in accordance with that described in this manual. Careful shielding of the board from external electro-magnetic sources is also required due to the high gain amplifiers on the board. In order to achieve this level of performance, the video data rate is limited to a value lower than the capability of the photodiode array itself.

Provision for cooling of the photodiode array using a thermoelectric cooler is possible by means of the access hole located directly beneath the array.

Power Requirements

The board is designed to be operated from a triple output source supplying +5V, +15V, and -15V to the circuit's separate analog and digital sections. On-board voltage regulators provide an analog +5V supply and an analog -5V supply from the +15 and -15V inputs. The analog and digital ground planes have been completely separated on the board and are each brought separately to the PCB edge connector. These two ground planes can be tied together at the board edge connector and then grounded at the power supply using a good low impedance conductor. Alternately, each ground plane could have a separate low impedance cable with a common connection at the power supply itself.

The PC board edge connector pin assignments for each power supply input and ground connections are shown below. See "Specifications" section for current and voltage requirements for each power supply input.

Signal	Sym	Edge Pin	Test Point
+15 Volts	+15V DC	9	TP 1
+5 Volts	+5V DC	22	TP 3
-15 Volts	-15V DC	7	TP 2
Analog Ground	AGND	11, 34-44	TP 11
Digital Ground	DGND	13, 23-33	TP 4

Specifications

Mechanical		
Dimensions:		3.0 in x 4.0 in
Connectors:	Edge connector	22/44-pin dual .100" CTC
	Video output	Coaxial BNC
Electrical		
Power Inputs:	+15V	+15V DC (±.1V DC) @ 75 mA
	+5V	+5V DC (±.1V DC) @ 70 mA
	-15V	-15V DC (±.1V DC) @ 50 mA
Video Data Rate:		50 kHz maximum
Video Output:	Saturation	+10V (±20%)
	Peak-to-peak pixel noise	
	-011	2.5 mV (typ)
	-020	1.25 mV (typ)
	DC Dark Level adj. range	+2V to -2V
Clock Output:	Pulse width	2 µs positive
	Amplitude	HCMOS compatible
Ext. Clock Input:	Pulse width	50 ns minimum
	Amplitude	HCMOS compatible
Ext. Start Input:	Pulse width	See Timing Diagram
	Amplitude	HCMOS compatible
Sync Output:	Pulse width	See Timing Diagram
	Amplitude	HCMOS compatible

Note: Peak-to-peak pixel noise is dependent upon a number of parameters. Careful attention should be given to the following parameters for optimum noise performance.

1. Power supply noise and ripple levels should be <1 mV_{p-p}.
2. Utilize low impedance power supply connections.
3. Minimize the lengths of the analog and digital cables.
4. Shield the board from electro-magnetic radiation sources.

345 POTRERO AVENUE SUNNYVALE, CALIFORNIA 94086-4197 (408) 738-4266 FAX: (408) 738-6979

Operational Description

There are two basic circuits interfacing the photodiode array. Figure 1 is a simplified block diagram that shows the two sections separated by a dotted line. The digital section is on the left and the analog section is on the right. Refer to the schematic diagrams of the RC1030LNN for the detailed circuit of the block diagram. Refer to the timing diagram of Figure 2 for functional timing information.

Digital Section

The one-shot oscillator and pulse width control, U2, provide the master clock (MCLK) signal used to generate all the board timing. Frequency of the MCLK can be adjusted with R1. The MCLK signal clocks the 16 bit pre-settable counter, U4, used to control integration time of the photodiode array. Refer to the schematic of the EPLD U4 for the detailed circuit of this device. The output of U4, pin 6, is an active high pulse for 1 cycle of N MCLK cycles. N is determined by the binary weighted count of the setting of the DIP switches SW1, SW2, SW3, and SW4. This output signal, SYNC, is routed to the timing generator, EPLD U5, and is also used to reload the 16 bit counter for the next count cycle.

The timing generator, U5, requires 4 inputs and produces 5 outputs for the photodiode array and video processing section. Refer to the schematic diagram of U5 for the detailed circuit of this EPLD. The MCLK and SYNC signals are used to derive the 3 photodiode array signals, ϕ_1, ϕ_2, and START. ϕ_1 and ϕ_2 are complimentary 2-phase clock signals used to clock the photodiode array shift register. The photodiodes will be accessed at the frequency of these signals which is 1/2 the frequency of the MCLK signal. The start signal is a pulse shaped version of the SYNC signal and controls the loading of the photodiode array shift register and thus the start of a new readout period. A delayed and pulse shaped MCLK signal from U3, DCLK, is used to derive the SAMPLE signal for the sample and hold circuit. The $\overline{\text{MCLK}}$ signal input is used to develop the RESET output signal for the resetting of the integrator in the video processing section.

Analog Section

The analog portion of the circuit begins the with the active and dummy video outputs of the photodiode array. These outputs are differentially amplified by operational amplifier, U8. A video line bias of +2.5V is provided by U7 and zener diode CR1. The output signal from U8 is a train of voltage pulses corresponding to the charge detected on each photodiode as they are readout in sequence. The pulses will ride on a +2.5V DC level. A second stage differential amplifier U9 is used to cancel the DC offset of the video signal. The amplified charge pulses from the photodiode array are then integrated by U10 on capacitor C29. The integrator is reset by Q2 once each period prior to the next charge pulse. The output of the integrator is AC coupled and then DC restored by Q4 to an adjustable DC level set by R37. The video signal is DC restored synchronously with the integrator reset. The DC restored video signal is then sampled and held by U11 and C36. The sample-and-held video signal is routed to the output BNC connector J1 and to the PCB edge connector P1 - 2.

Input Signals

In the usual mode of operation, the RC1030LNN evaluation board generates all the necessary signals to operate the photodiode array. The board has provisions for accepting an external master clock and/or start signals. These external inputs can be used to synchronize the array output to the user's system.

External Clock Input, pin P1 - 15/TP7

The RC1030 can be externally clocked by selecting jumper settings E1 - E2 and applying an HCMOS level clock signal on this input. Timing of this signal is noncritical since the pulse width will be determined by the one shot U2-B. The frequency of this signal will be twice that of the video output pixel rate and should not exceed 100 kHz.

Ext. Start Input, pin P1 - 20/TP6

The readout operation of the photodiode array can be externally controlled by selecting jumper settings E5 - E6 and inputting an active-high HCMOS signal on this input. The external START must have a minimum positive pulse width of 200 ns. The falling edge of EXT START must occur no sooner than 20 ns after the falling edge of $\overline{\text{MCLK}}$ at TP8. The minimum number of master clock cycles, MCLK's, between start pulses will be twice the array length plus 4 counts.

External Line Reset, TP9

By selecting jumper setting E7 - E8 simultaneous resetting of the photodiodes can be controlled by this input. Pulling this input low will reset all the photodiodes in the array. The integration time is then different for each photodiode in the array. The integration for a given diode n is the time between the rising edge of LR to the next readout time for diode n. This mode of operation is suitable for synchronizing the array with flashed or pulsed light sources.

Output Signals

Clock Output, pin P1 - 17/TP8

This output is provided to synchronize user circuitry to the RC1030 BNC video pixel data. The frequency of this signal will be twice that of the video data rate.

Sync Output, pin P1 - 19/TP5

This is an HCMOS output signal for the purpose of synchronizing an oscilloscope or user circuitry to the photodiode array line scan time. The timing and polarity of this output is shown in Figure 2.

End-of-Scan (EOS) Output, TP10

The photodiode array produces an output pulse from the shift register at the end of the active array scan time. The timing of this signal is shown in Figure 2. This is an HCMOS compatible output signal.

Video Output, J1

The final sampled-and-held video output signal can be monitored at this output. The timing of this signal is shown in Figure 2.

Alignment Procedures

The RC1030 evaluation boards, as shipped from the factory, have been thoroughly aligned with either the user's array or with a typical test array. Upon applying power to the board, the following alignment procedure should be followed to achieve optimum circuit performance. Proper alignment of the board set can be accomplished only when the board is driven with power as specified in this document.

The photographs used in this alignment procedure were taken using an RC1030LNN-011 board and an RL1024SBQ-011 array. The MCLK frequency was set at 80 kHz. The MSTART repetition rate was set at 2048 + 128 counts for ease in recognizing "flyback" time (time between active scans).

Procedure

Connect the power supplies to the board in accordance with the pinout as listed in the "Power Requirements" section. Install a photodiode array in the socket for U1. Be certain to observe proper pin orientation when installing the photodiode array. Apply power to the board.

MCLK

The RC1030 board Master Clock may be derived from the on-board clock oscillator or from an external source. If the on board clock generator is desired, select jumper setting E2 - E3. With an oscilloscope, monitor the clock oscillator output on test point 8, TP 8. Adjust potentiometer R1 for the desired clock rate. If external master clock operation is desired, select jumper setting E1 - E2 and input a clock signal on pin P1 - 15 of the board edge connector or TP 7.

MSTART

The RC1030 board integration time (start pulse) may be derived from the on-board integration counters or from an external source. If internal operation is desired, select jumper setting E4 - E5. The integration time will then be controlled with the binary weighted switch settings of SW1, SW2, SW3, and SW4. With an oscilloscope, monitor the sync output on pin P1 - 19 of the board edge connector and set the integration time for the desired rate. The minimum count for a given array size is given by the equation (2 x n) + 4, where n equals the number of array photodiodes. For example, the minimum count setting for an RL1024SB device would be (2 x 1024) + 4 or 2052 counts. The DIP switch settings would be as follows:

— SW4 —	— SW3 —	—SW2 —	— SW1 —
off off off off	on off off off	off off off off	off on off off
(msb)			(lsb)
	2048	+	4 = 2052

If external integration time control is desired, select jumper setting E5 - E6 and input the start signal on pin 20 of the edge connector in accordance with the conditions described in the "Input Signals" section.

Use the Sync output to synchronize the oscilloscope for the remainder of this procedure.

Integrator Bias Adjustment

With an oscilloscope, monitor the output signal from pin 6 of U10. Darken the photodiode array using an opaque material to cover the window over the array. Set the oscilloscope vertical sensitivity to .2V/div. and the horizontal time base for 50 µs/div. Adjust the potentiometer R20 until the slope on each pixel is minimized. See photos 1, 2 and 3 for examples of this adjustment.

Dark Video DC Level

Set the horizontal time base to 5 mS/div. Monitor the video output signal at J1 or edge connector pin, P1 - 2. Adjust potentiometer R37 until the DC level of the video "flyback" time is at ground level as shown in photo 4.

Antiblooming Control Adjustment

If external LR control is not desired, select jumper setting E8 - E9. Set the oscilloscope vertical sensitivity to 5V/div. Adjust potentiometer R42 fully clockwise. Remove the opaque covering from the array and increase the illumination on the array with a suitable DC light source to a level such that the output from the photodiodes stops increasing and the "flyback" time starts to go positive from the ground level. The "saturated" video output should appear similar to that of photo 6. Adjust the antiblooming control, R42, counterclockwise until the "flyback" time is brought back to the ground level. Adjusting R42 too far will result in reducing the saturated output voltage as shown in photo 7. With the correct setting of R42, the video should appear similar to that shown in photo 8.

Video Output

The final 4 photos indicate the typical array performance when exposed to various light levels. Actual performance seen from other photodiode arrays may vary somewhat from the photos due to normal process variations in nonuniformity of sensitivity, dark leakage current, saturation charge, etc. Photo 9 is exposed to "saturation", photo 11 is zero exposure. Photo 12 is the typical p-p noise level on a single pixel. Photo 12 was taken by storing maximum and minimum excursions of a given pixel for 128 scans using a digital oscilloscope.

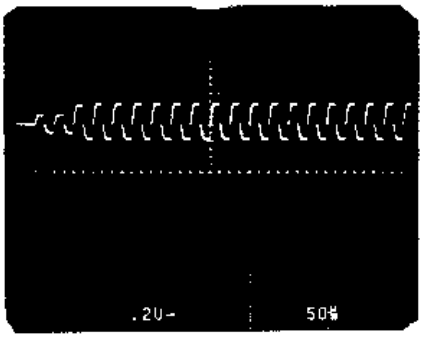


Photo 1. Integrator Bias Set Correctly

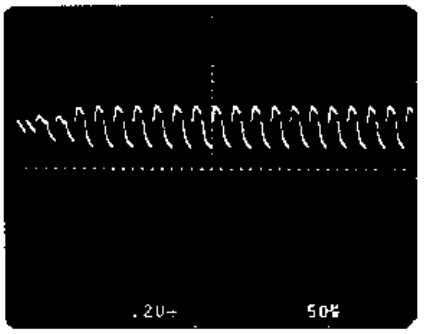


Photo 2. Integrator Bias Set Incorrectly

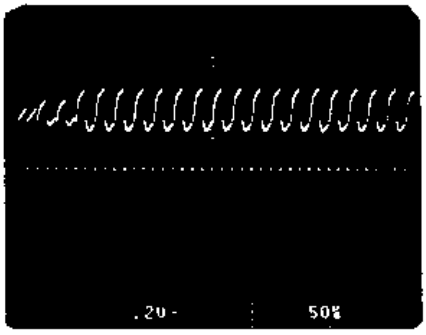


Photo 3. Integrator Bias Set Incorrectly

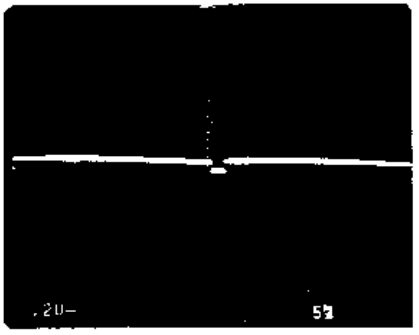


Photo 4. Dark Level Set Correctly

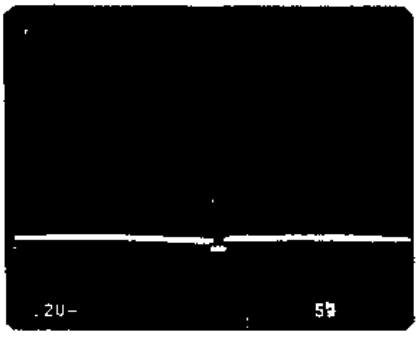


Photo 5. Dark Level Set Incorrectly

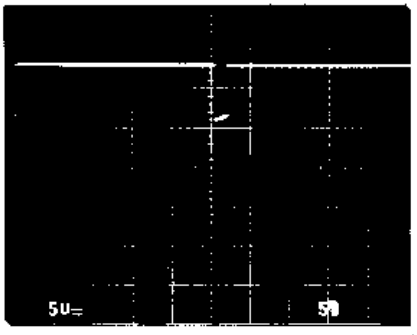


Photo 6. No Blooming Control

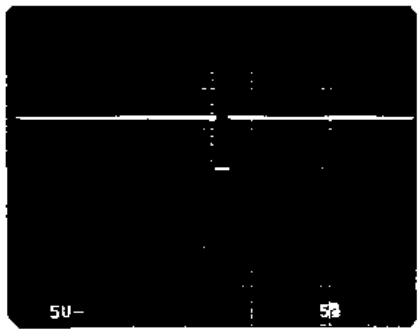


Photo 7. Blooming Control Set Too Low

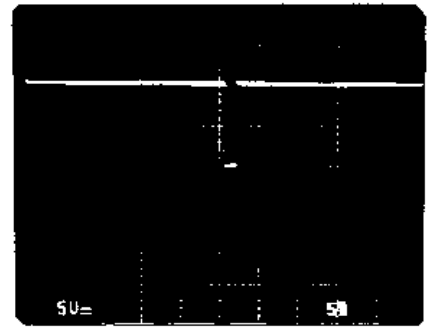


Photo 8. Blooming Control Set Correctly

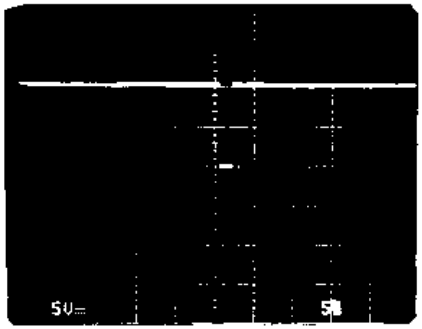


Photo 9. Video Output @ Saturation Exposure

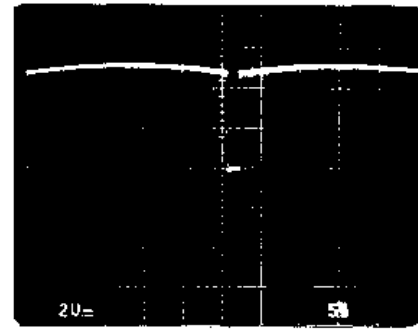


Photo 10. Video Output @ 50% Saturation Exposure

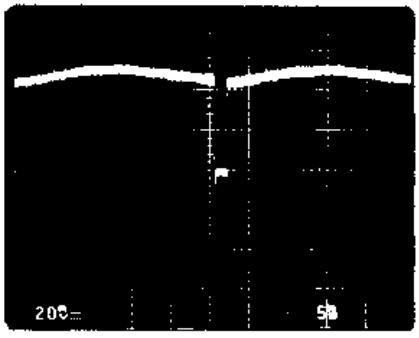


Photo 11. Video Output @ Zero Exposure

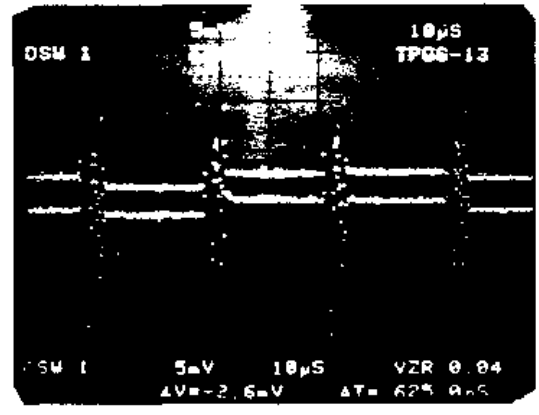


Photo 12. Video Output P-P Pixel Noise

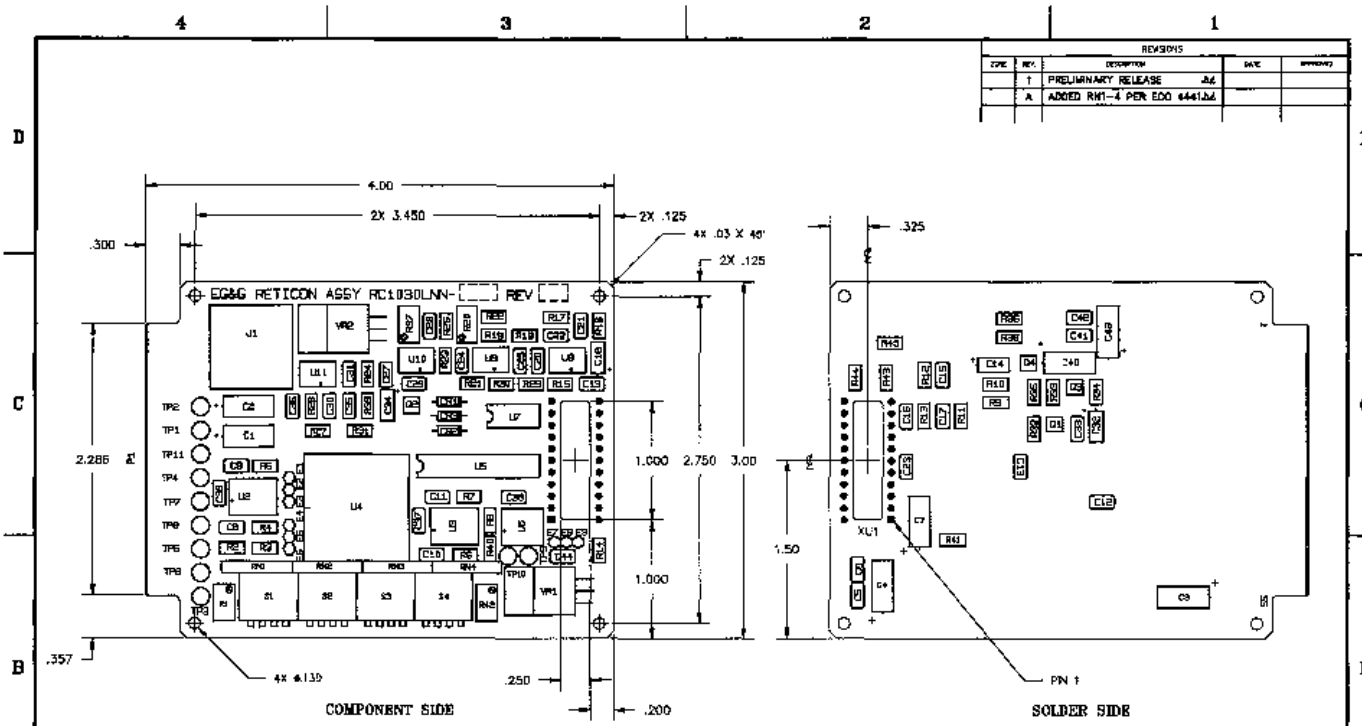
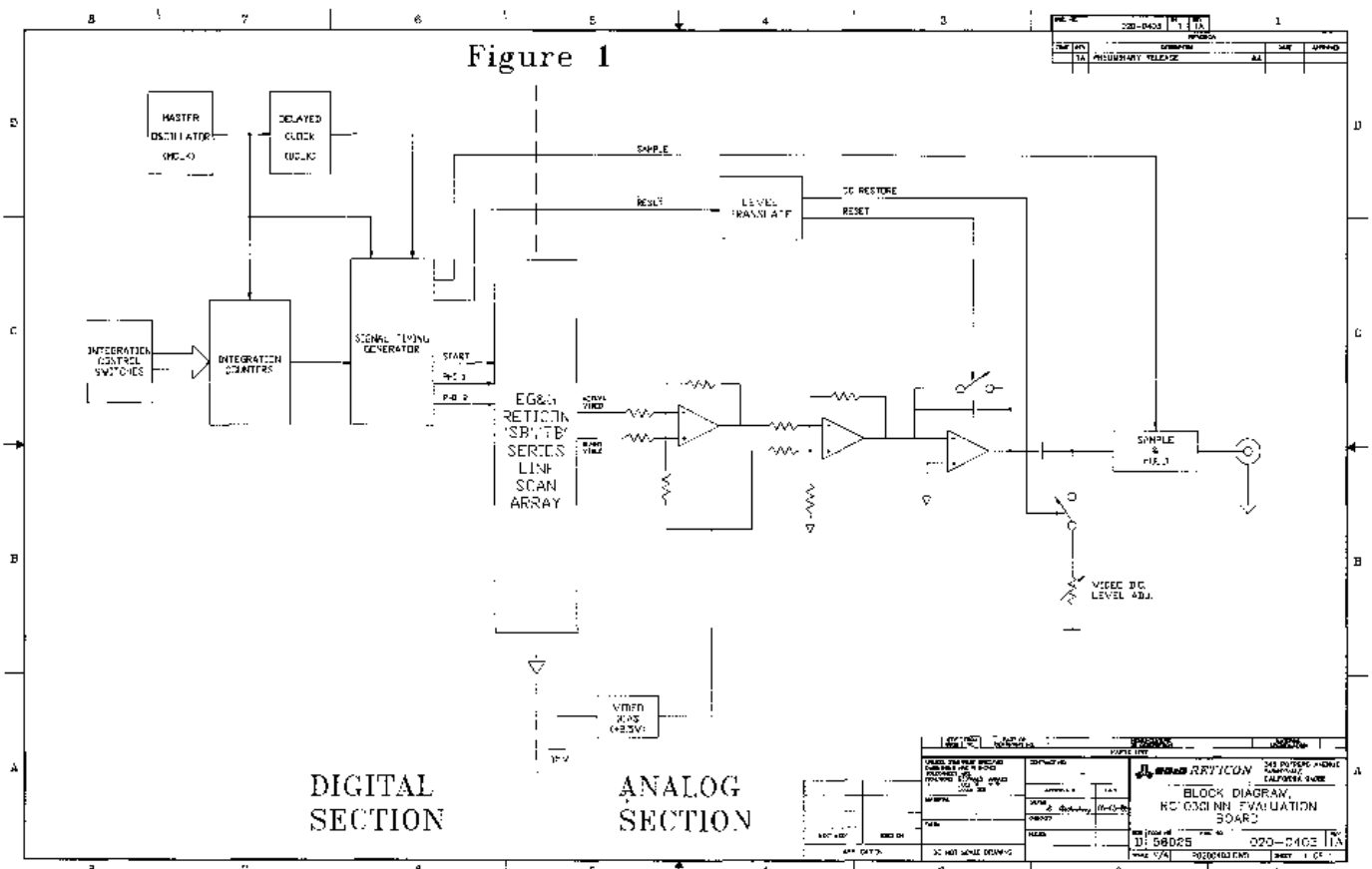
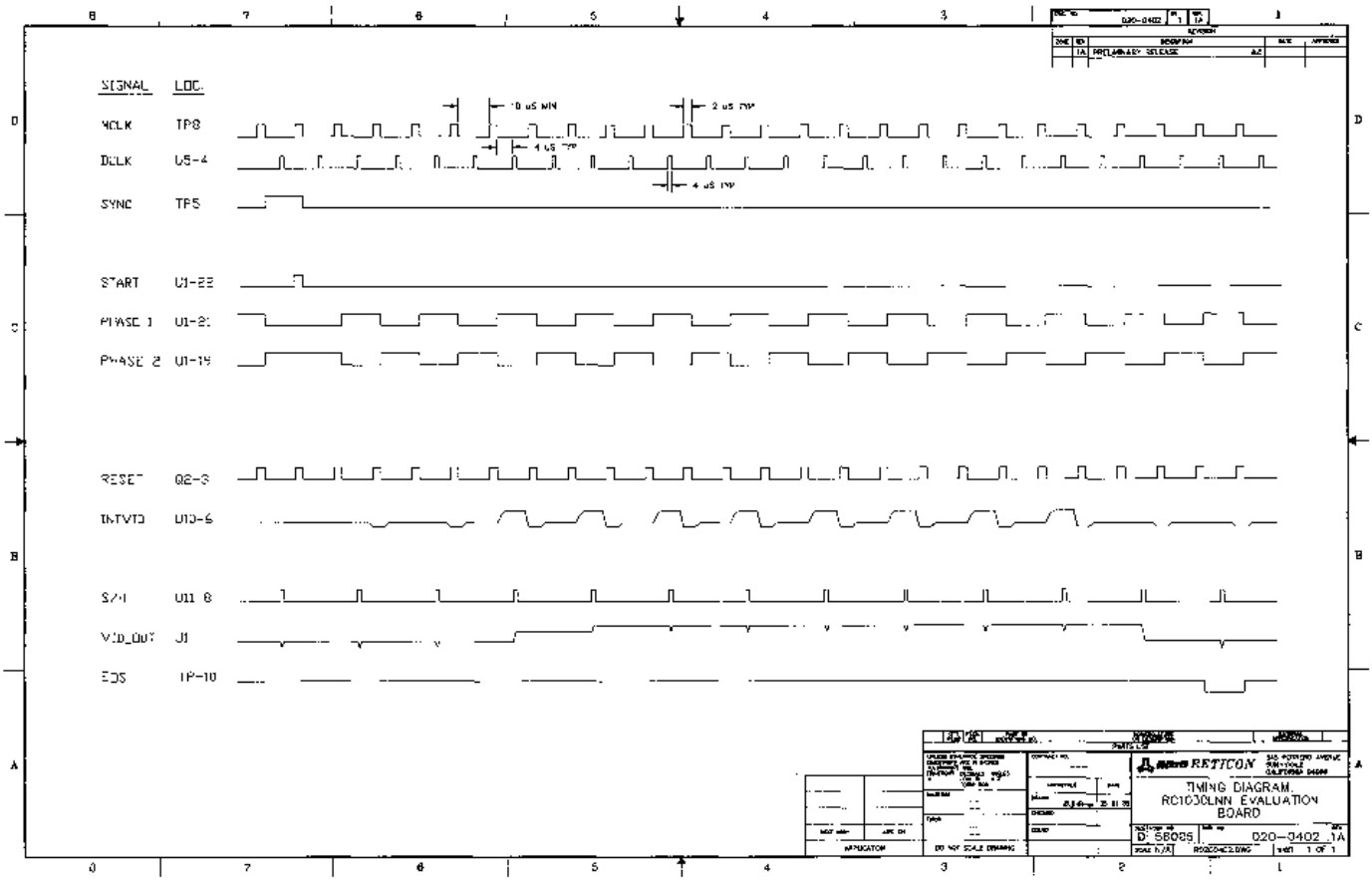
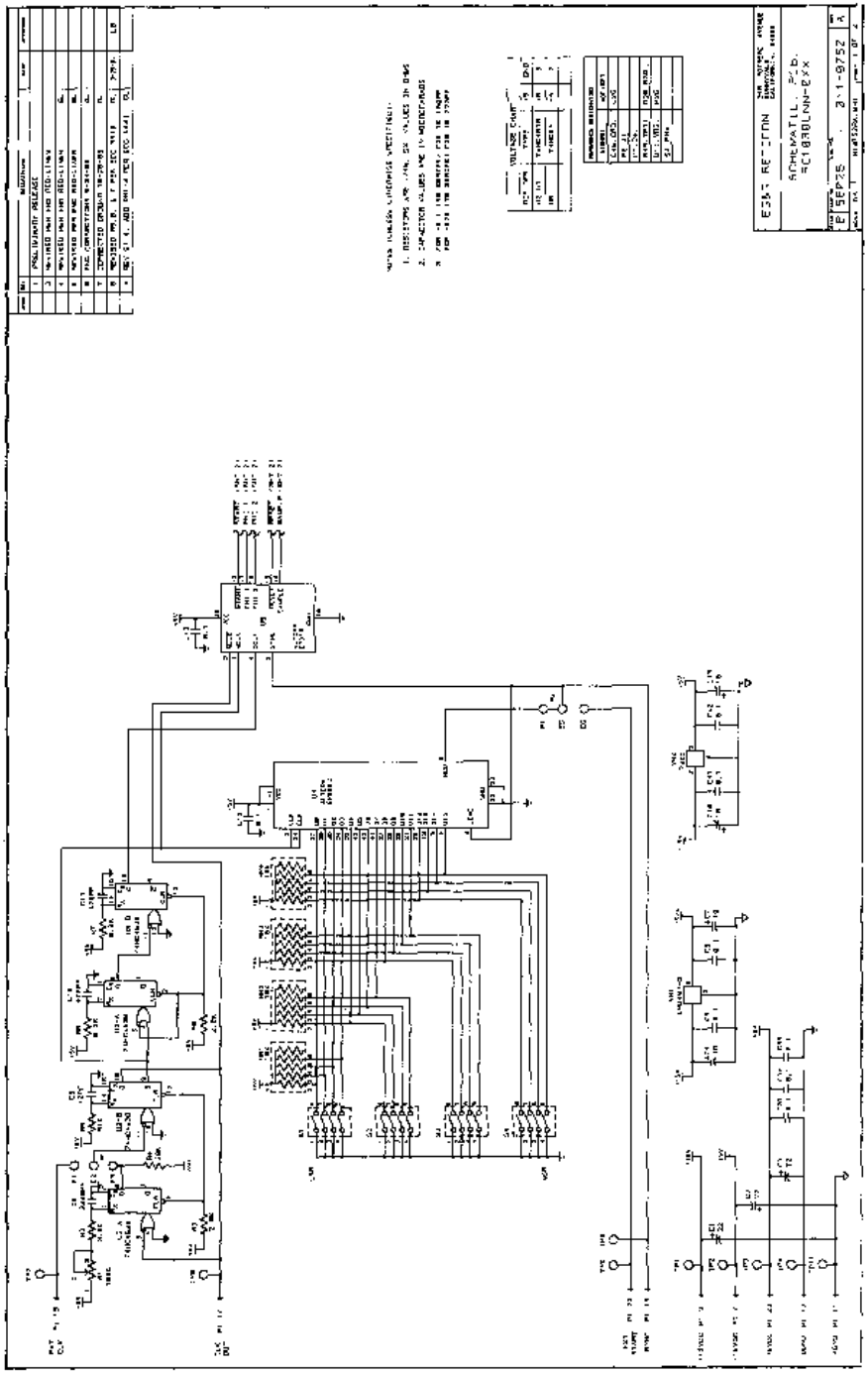
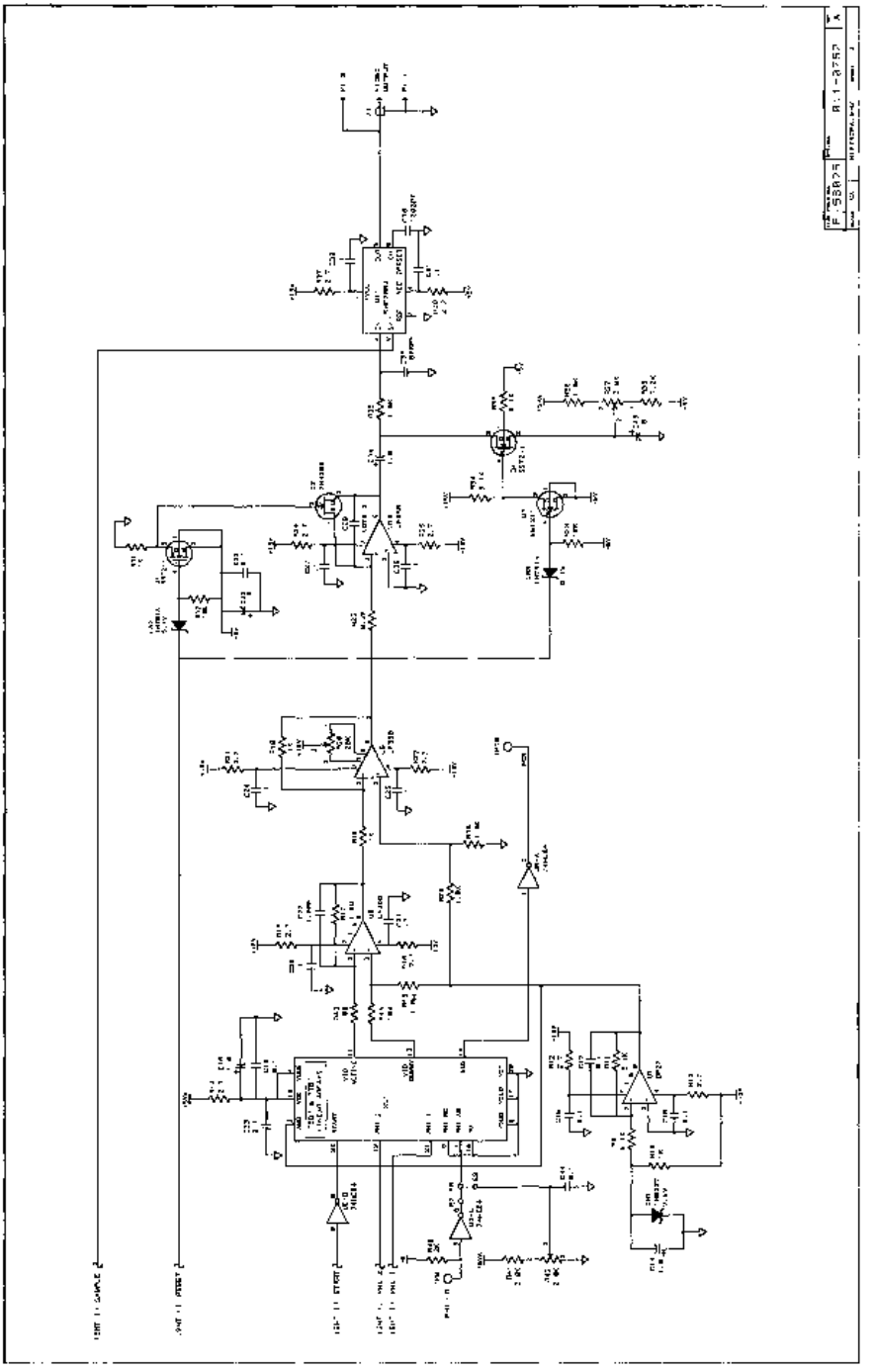

REVISIONS
ZONE REV. DESCRIPTION DATE APPROVED
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A ADDED RN1-4 PER ECO 6441JM
4.00
2X 3.450
2X .125
4X .03 X 45°
2X .125
.300
EG&G RETICON ASSY RC1030LNN-[ ] REV [ ]
2.286
1.000
2.750
3.00
1.000
.357
4X ø.139
.250
.200
.325
1.50
XU1
PIN 1
COMPONENT SIDE
SOLDER SIDE
NOTES (UNLESS OTHERWISE SPECIFIED):
1. SEE SEPERATE PARTS LIST PL-010-0752
2. COMPONENT VALUES SHOWN FOR REFERENCE ONLY:
a. RESISTORS IN OHMS
b. CAPACITORS IN MICROFARADS
3. COMPONENT HEIGHT SHALL BE .65 MAX ON COMPONENT SIDE ; .20 MAX ON SOLDER SIDE
4. LEAD PROTRUSION SHALL BE .06 MAX
5. SQUARE PADS DENOTE PIN 1 OF IC'S, EMMITER OF TRANSISTORS, POSITIVE END OF POLARIZED CAPACITORS AND PIN 1 OF CONNECTORS
PARTS LIST
RETICON
PCB ASSEMBLY-
RC1030LNN-0XX
C 56025 RC1030LNN-0XX A
SCALE NONE M010752.DWG SHEET 1 OF 1

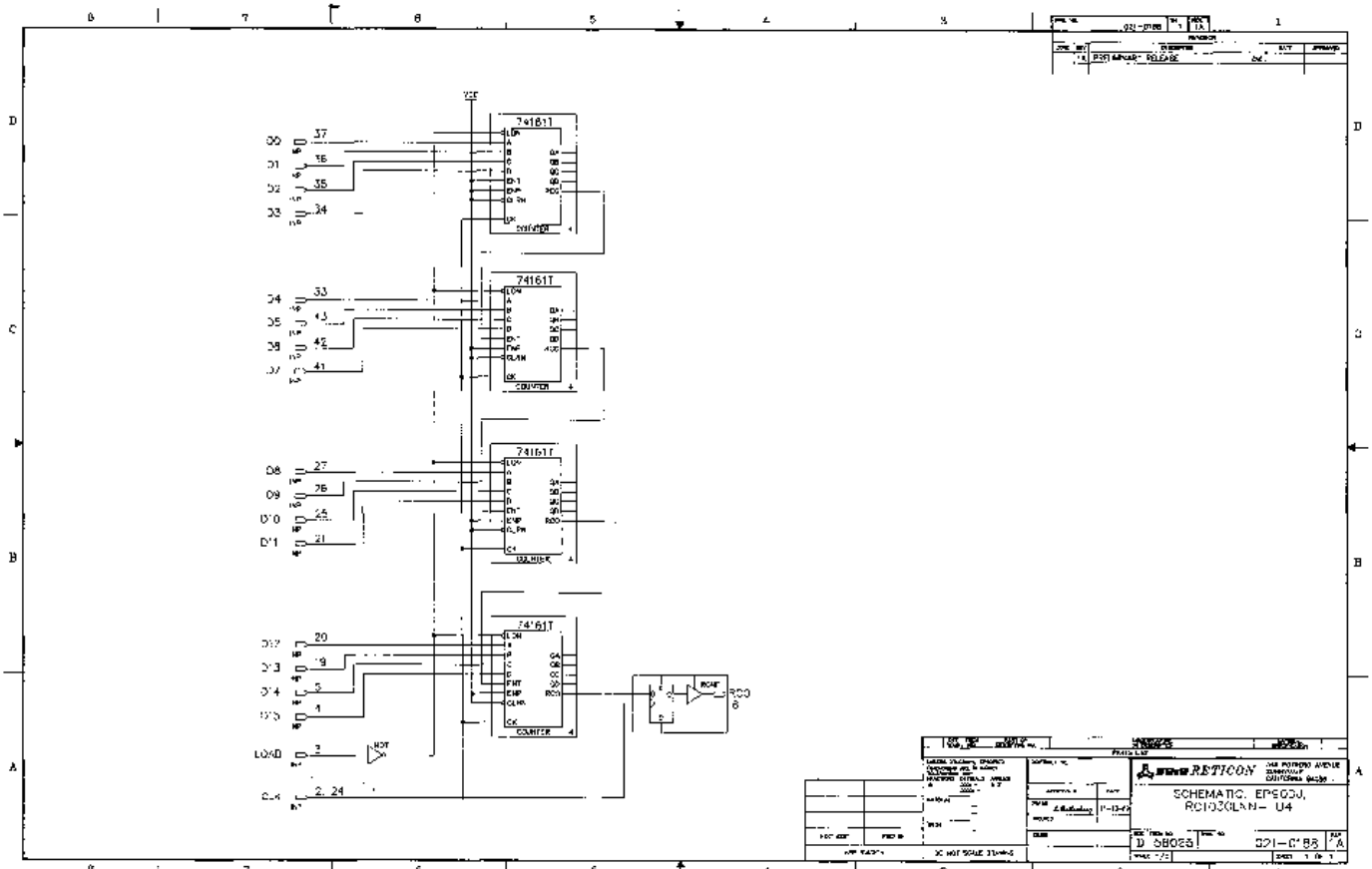
Figure 1

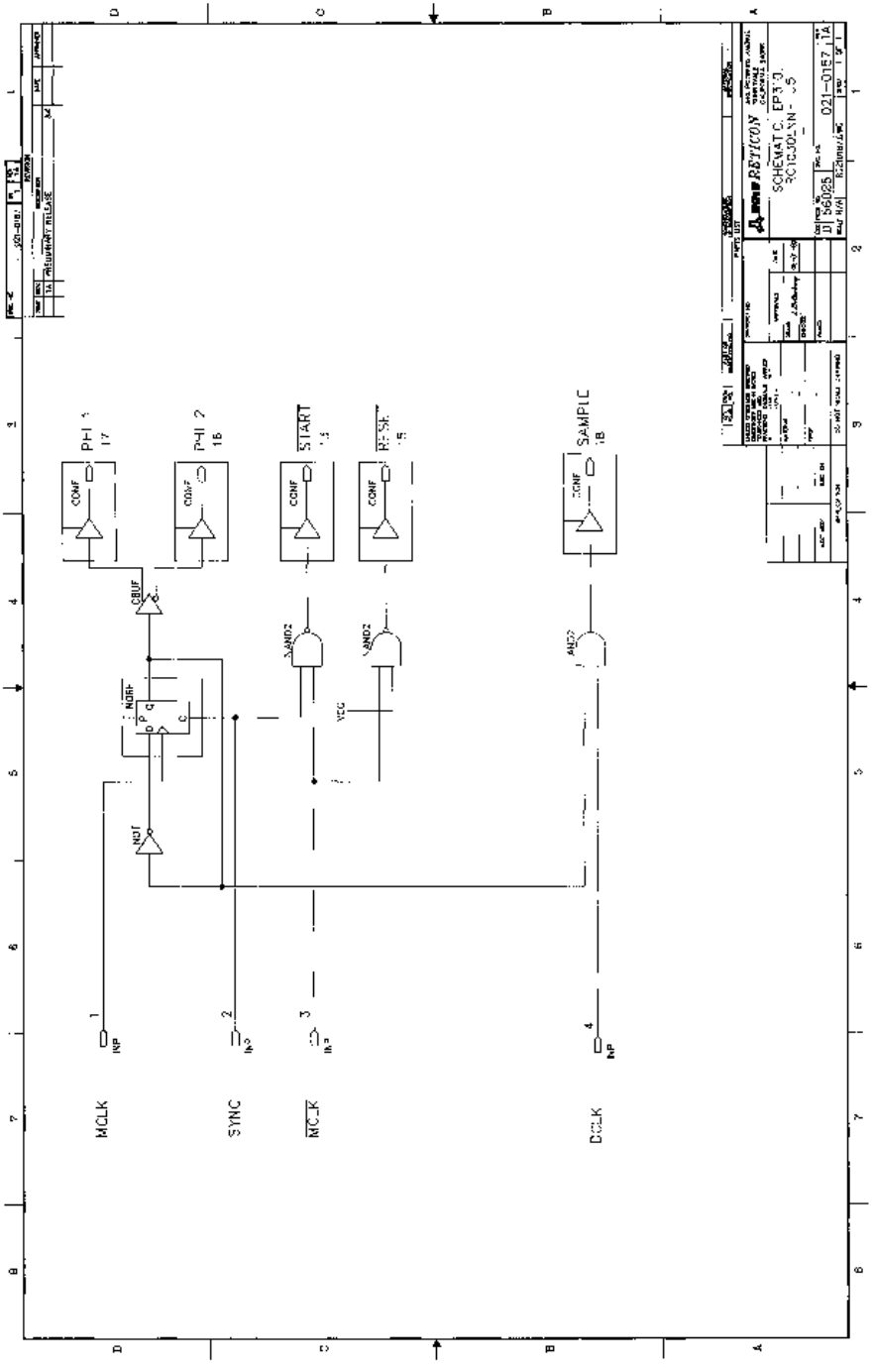

MASTER OSCILLATOR
DELAYED CLOCK
SAMPLE
RESET
LEVEL TRANSLATE
DC RESTORE
RESET
INTEGRATION CONTROL SWITCHES
INTEGRATION COUNTERS
SIGNAL TIMING GENERATOR
START
EG&G RETICON SERIES LINE SCAN ARRAY
SAMPLE & HOLD
VIDEO DC LEVEL ADJ.
DIGITAL SECTION
ANALOG SECTION
RETICON
BLOCK DIAGRAM, RC1030LNN EVALUATION BOARD
ID 58025
020-0403 1A


SIGNAL
LOC.
MCLK
TP8
DCLK
U5-4
SYNC
TP5
START
U1-23
PHASE 1
U1-21
PHASE 2
U1-19
RESET
U2-8
INTVTO
U10-6
S/H
U11 8
VID_OUT
J1
EOS
TP-10
2 uS TYP
4 uS TYP
RETTON
TIMING DIAGRAM,
RC1030LNN EVALUATION
BOARD
D 58085
020-0402_1A






74161T
74161T
74161T
74161T
RETICON
SCHEMATIC, EPSON,
RC1030LNN – U4
D 58028
021-0188
A



055-0273
March 1992

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Application Information

Illumination Sources

EG&G Reticon image sensors detect electromagnetic radiation from 200 to 1100 nanometers. The short wavelength response will be limited to about 350 nanometers when using either a glass window or fiber optic faceplate.

Sources of illumination with energy in the detection wavelength range are all suitable for image sensors. A few of the possible sources are:

Incandescent lamps
Fluorescent lamps
Sunlight
Light emitting diode (LED)
Laser
Phosphor output

The primary requirement is to have a sufficient amount of intensity to operate the image sensor at the desired integration time.

Please refer to Applications Note 121 for more information on light sources and spectral response.

Cleaning Windows

The windows of an image sensor must be kept clean to ensure transmittance of incident radiation through the window. Lack of window cleanliness will contribute to nonuniformity of sensitivity and may prevent proper operation in some applications. The windows are easily cleaned by using a soft lint-free cloth or paper soaked in a residue-free organic solution, such as alcohol.

Note: Windows should never be wiped with a dry cloth or paper. Never clean a window with array energized.

Fiber Optic Faceplates

Some image sensors are available with fiber optic faceplates instead of quartz or glass windows. This enables the user to efficiently couple the image sensor to other electro-optical devices such as an image intensifier. The S Series wide aperture linear image sensor and the RA0100A/0128N area image sensors are available as standard products with a fiber optic faceplate. The optical fiber used on these devices has a 6 micron core size with a numerical aperture of 1. Most EG&G Reticon image sensors can accommodate a fiber optic faceplate. Please consult the factory for more details.

Cooling Image Sensors

The signal-to-noise ratio performance of any image sensor can be improved by reducing its temperature. For each 7° Celsius drop in temperature, the dark leakage current is cut in half. Some applications call for a very wide dynamic range and/or long integration times which can only be achieved by cooling the device.

Typically, cooled devices are housed in a nitrogen purged atmosphere to prevent condensation. Cooling can be achieved in several ways. The method most often used is a thermoelectric cooler. Using the Peltier effect, and multiple stage coolers, it is possible to cool an image sensor by over 50°C. There are several manufacturers of these coolers which have configurations suitable for Reticon image sensors.

Another cooling method is the Joule-Thomson cooler which cools by adiabatic expansion of a gas that is initially below its saturation temperature. The expanded gas, thus cooled, is passed back over the incoming gas, resulting in regenerative cooling. There are also several manufacturers of this type of cooler available for image sensors.

A third method is to mount the image sensor on a "cold finger" which is attached to a dewar of liquid coolant.

Image Intensifiers

Some applications require higher sensitivity than can be achieved by standard image sensors. EG&G Reticon offers several wide aperture devices for increased sensitivity. The coupling of image intensifiers, available from several magnifications, can improve the sensitivity of photodiode arrays.

An image intensifier consists of a photo cathode for converting light into electrons. These electrons are multiplied through a microchannel plate and then strike an output phosphor coated on the inside of a fiber optic faceplate. These image intensifiers can provide gains of 1,000 to 10,000, enabling lower light level operation. The output by the image intensifier couples directly to the fiber optic faceplate of the image sensor and can be attached with an appropriate optical cement.

Special Selection

At times, the specifications on the EG&G Reticon image sensors are not adequate for some applications. Special requirements for characteristics such as lower dark leakage or improved nonuniformity of sensitivity may be accommodated by requesting specially selected devices.

Please consult one of our sales offices with your special requirements. We will gladly consider your request and determine if we can satisfy your need. There will be a selection charge and additional delivery time.

Application Notes

101 - "Application of Reticon Photodiode Arrays as Electronic and X-Ray Detectors"

121 - "Spectral Response of Reticon Linear Photodiode Arrays"

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Application of Reticon Photodiode Arrays as Electron and X-Ray Detectors

General Description

Reticon self-scanning photodiode arrays were designed primarily for detection of visible and near infrared light; however, these devices make excellent detectors of more energetic radiation as well. They are particularly useful for detecting soft x-rays in the 1 to 10Å wavelength (1.2 to 12 KeV photon energy) range and electrons in the 10 to 100 KeV range. These ranges can be extended by relatively minor changes in the device structure.

Although, in principle any Reticon photodiode array can be used to detect electrons or x-rays, the most suitable standard devices are the "C" and "B" series with the wide aperture option.[1] [2] The "C" series devices have a 17 mil wide sensing area with 128, 256, 384 or 512 individual sensors on 2 mil centers or 256, 512, 768 or 1024 sensors on 1 mil centers. The "B" series devices have a 24 mil wide sensing area and either 512 or 1024 elements on 1 mil centers.

The user should provide an external shield to protect the areas of the silicon chip outside the sensing aperture. These areas contain mutiplex switches and shift register scanning circuits which can be damaged by exposure to ionizing radiation. The actual sensing area should then be defined by an aperture in the shield which is aligned inside the 17 or 24 mil aperture on the silicon chip. The proper alignment is illustrated in Figure 1.

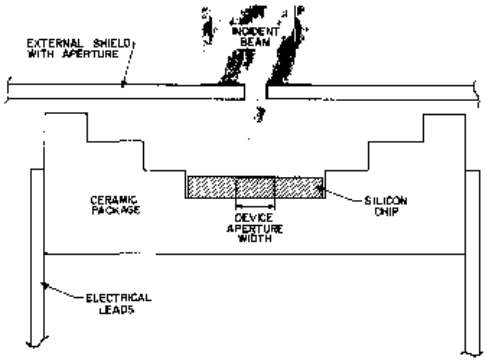


Figure 1. Cross Section of Packaged Reticon Array Showing Required Alignment of External Shield to Device Aperture

Reticon arrays are normally assembled in a ceramic dual-inline package and sealed with a quartz window 20 mils thick. For x-ray or electron sensing applications this window must of course be omitted. In addition, the sensing area of a standard array is covered by a protective silicon dioxide layer nominally 3 µm thick. This layer is completely transparent to light but will partially absorb an incident electron or x-ray beam. For this reason, it is sometimes desirable to reduce the thickness of the oxide layer. With a relatively minor process change devices can be produced which have the silicon dioxide layer thickness reduced to 1 µm. With more substantial process changes, the oxide layer can be eliminated completely in the area over the diodes. An oxide layer should remain between the diodes for reliability reasons.

Electron Detection

An incident high energy electron dissipates its energy over some path length by the creation of secondary electron-hole pairs. In silicon, one electron-hole pair is created for each 3.66 eV of energy dissipated. All of the secondary holes generated in the silicon within a diffusion length of the surface (approximately 50 µm) will be collected and stored on the nearest photodiode. This charge will be read-out as signal charge when the array is scanned. Holes generated within the oxide or deeper than one diffusion length within the silicon will not be collected and will not contribute to the signal charge.

Low energy electrons will lose all or most of their energy in the oxide layer covering the silicon surface and may therefore not be detected. The calculated range of electrons in SiO_2 is shown in Figure 2 as a function of energy.[3] It can be seen from the figure that electrons with energy less than about 25 KeV will be stopped in a 3 µm thick oxide layer and electrons

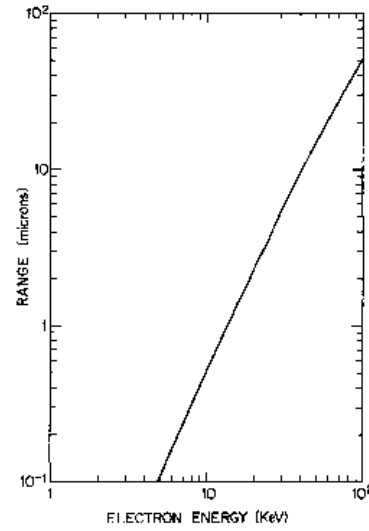


Figure 2. Range-Energy Relationship for Electrons in SiO_2 (see Reference 3)

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with energy less than about 12 KeV will be stopped in a 1 μm oxide layer. Energies in excess of these minimum values but less than about 100 KeV will be deposited in the silicon within one diffusion length of the surface and will generate a signal of one electronic charge per 3.66 eV of energy. Electrons with energy greater than 100 KeV will penetrate deeper than a diffusion length and only a fraction of the generated secondaries will be collected.

An experimental curve of charge gain as a function of incident electron energy is shown in Figure 3 for a device with a 1 μm oxide layer.[4] The offset of about 11 KeV agrees reasonably well with the theoretical range energy curve of Figure 2. Note that a single incident 30 KeV electron will produce a detectable signal of 5000 electronic charges. Studies on standard Reticon devices with a 3 μm oxide layer show similar results except that the offset voltage is increased to approximately 25 KeV as expected from Figure 2.[5]

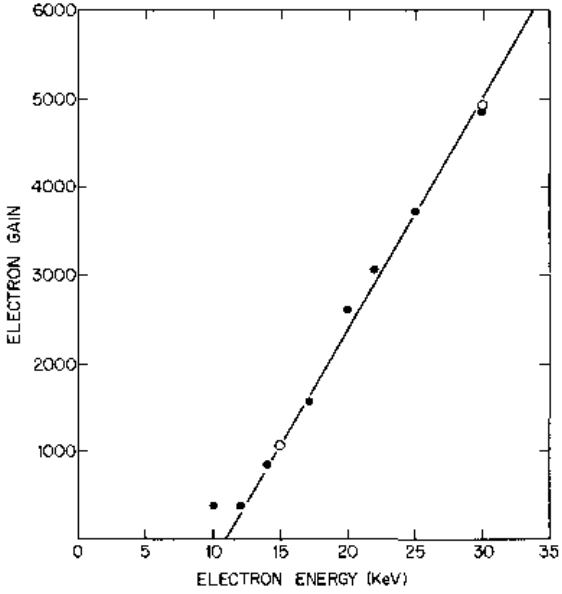


Figure 3. Charge Gain Versus Electron Energy for RL1024B with 1 μm Oxide Layer (see Reference 4)

One application in which Reticon arrays are used as electron detectors is in the self-scanned digicon tubes manufactured by Electronic Vision Corporation, 11661 Sorrento Valley Road, San Diego, California 92121.

These devices consist of a semitransparent photocathode, a magnetically focused electron imaging section and a Reticon photodiode array target. An optical image on the photocathode generates photoelectrons which are accelerated through approximately 20 KeV and focused onto the Reticon array where one incident photoelectron generates several thousand secondary electron-hole pairs to produce a corresponding charge gain. The read-out noise is sufficiently low that single electron events can be detected.[4,5] A discussion of the self-scanned digicon for applications in low light level astronomical spectroscopy is presented in Reference 4.

In addition to low light level imaging tubes such as the digicon, Reticon arrays may be used in electron spectroscopy and a variety of other electron detecting applications.

X-Ray Detection

When an x-ray beam is incident on a material such as silicon, it is attenuated exponentially, i.e., its intensity decreases with distance according to the relation $I = I_o \exp(-x/\alpha)$ where I_o is the incident intensity and I is the intensity at any distance x from the surface. The parameter α (the absorption coefficient) is the probability per unit path length of an x-ray photon being absorbed. On the average a photon will travel a distance of $1/\alpha$ before being absorbed.

When a photon is absorbed its energy is transferred to an electron which then gives up the energy by generating secondary electron-hole pairs. From here on the problem is the same as for direct detection of electrons. One secondary is produced for each 3.66 eV of absorbed energy and all the secondary holes produced in the silicon within a diffusion length of the surface will be collected and contribute to the signal charge.

The absorption coefficient of silicon is shown as a function of wavelength (or photon energy) in Figure 4. The absorption coefficient of SiO_2 is slightly different but has a similar wavelength dependence. Note that short wavelength (high energy) x-rays have a very low absorption coefficient and a

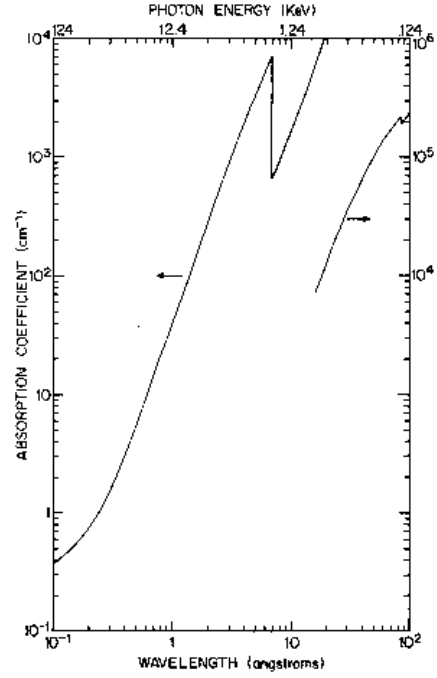


Figure 4. X-ray Absorption Coefficient of Silicon as a Function of Wavelength and Photon Energy

beam would penetrate all the way through a silicon device with very little energy being absorbed. Long wavelength (low energy) x-rays, on the other hand, have a very large absorption coefficient and most of the beam energy will be absorbed in the oxide without reaching the silicon. Calculated response curves considering both effects are shown in Figure 5. The calculations were carried out for three oxide thicknesses: 0, 1 and 3 μm. A diffusion length of 50 μm was assumed in each case. The notch in the response curves is due to an absorption edge associated with silicon atoms in the SiO_2 layer.

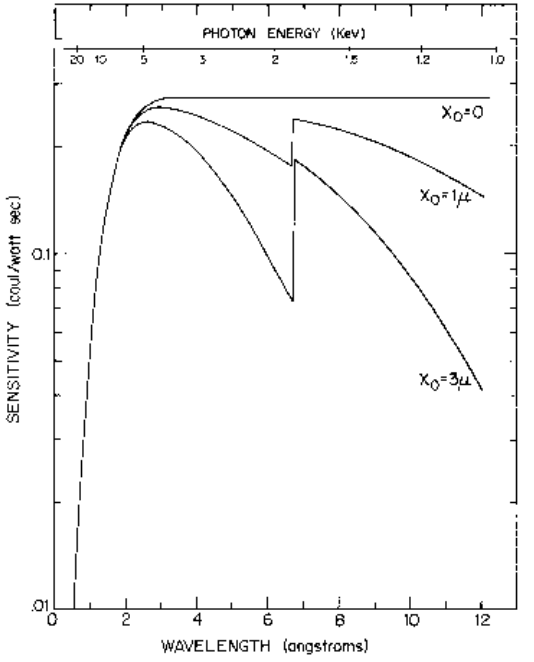


Figure 5. Theoretical X-ray Response of Reticon Photodiode Arrays for 0, 1 and 3 μm Oxide Thickness and 50 μm Diffusion Length

It can be seen from Figure 5 that the peak sensitivity is at about 5 Å wavelength and that standard devices make quite good detectors over a range from about 1 to 12 angstroms. At long wavelengths the sensitivity can be significantly improved by reducing or eliminating the oxide layer. For wavelengths longer than 15 or 20 angstroms, the sensitivity is expected to decrease even for zero oxide thickness. This is because most of the energy is absorbed so close to the silicon surface that some of the secondary electron-hole pairs will be lost by surface recombination.

For wavelengths between very soft x-rays (about 20 Å) and the ultraviolet (about 2500 Å) no experimental work has been reported and calculations are difficult. It is possible, however, that Reticon devices could be useful over a portion of this range.

For wavelengths shorter than 1 Å the sensitivity falls off rapidly, but the devices may still be useful for high intensity beams. In this range the sensitivity in coul/watt sec is approximately given by 1.4×10^{-3} times α in cm^{-1}.

The method of calculating the signal charge which will be read-out of each cell when the array is scanned is illustrated by the following example:

Consider a standard "C /17" series array masked externally to expose a 10 mil wide sensing area. Each cell then has a sensing area of 1 mil x 10 mil = 10 mil^2 = 6.5×10^{-5} cm^2. Suppose an x-ray beam with an intensity of 10 μwatt/cm^2 and a wavelength of 4 Å is to be detected and the array is scanned at 100 lines/sec. The energy incident on each cell per line is then:

$$10^{-5} \frac{\text{watts}}{cm^2} \times 6.5 \times 10^{-5}\ cm^2 \times .01\ \text{sec} = 6.5 \times 10^{-12}\ \text{watt sec}$$

From Figure 5 the sensitivity at 4 Å is 0.2 coul/watt sec. Therefore, the signal charge is:

$$0.2 \frac{\text{coul}}{\text{watt sec}} \times 6.5 \times 10^{-12}\ \text{watt sec} = 1.3\ \text{pC}.$$

Since the saturation charge of a "C/17" device (see data sheet) is 3.2 pC, the above exposure results in a signal equal to 40% of saturation.

Radiation Damage

While many Reticon devices are being used in electron and x-ray applications with no serious problems, the user should be aware that continued exposure to high energy radiation can cause radiation damage effects.[6, 7] These effects are cumulative and permanent.

The most serious effect, which can fortunately be eliminated by shielding, is a shift in the threshold voltage of the MOS transistors used in the multiplex switches and scanning circuits of the array. If these are not shielded, the scanning circuit will cease to function after a radiation dose of about 10^5 rads. The absorbed dose varies with the oxide thickness and the electron or x-ray energy. For 20 KeV electrons incident on a silicon surface covered by 1 μm of oxide it is about 3×10^{-7} rads per incident electron/cm^2. Working through the numbers, this means that the device would fail after an exposure sufficient to cause saturation about 2000 times.

With proper shielding the failure mechanism described above can be completely eliminated. However, there is a second radiation effect which relates to the sensor elements themselves and therefore cannot be eliminated by shielding. This effect is an increase in the dark leakage current which has a typical initial value of about 1 pA per cell and increases by about a factor of 10 after a dose of 10^7 rads. The effect is not catastrophic and saturates after the above dose. A dark current of 10 pA is not objectionable for most applications. If it is a problem it can be reduced by cooling the device. Dark current changes by about a factor of 2 every 7° C.

Ordering and Handling Information

Reticon photodiode arrays for use as radiation detectors must be specially ordered WITHOUT SEALED WINDOW. Devices so ordered will be shipped with a window taped in place to provide mechanical protection during shipping and handling. The devices can be functionally tested as light detectors while this temporary window is in place. After removal of the window, care should be taken to avoid touching the silicon surface or the delicate 1 mil diameter wire bonds. Unsealed devices should be stored and handled in a clean, dry environment.

Any standard Reticon array with a 3 µm oxide layer may be ordered unsealed at the regular price. Any "C/17" or "B/24" series devices may also be ordered with a 1 µm oxide layer. However, a 10% premium is charged for special processing and handling. Tooling is now available to fabricate "B /24" devices with zero oxide thickness over the diodes and 1 µm oxide between diodes. These are also available at a 10% premium over standard prices.

For applications not covered by standard "B/24" or "C/17" series devices, Reticon has a complete custom design capability. Custom devices can be built in a wide variety of geometric configurations.

Disclaimer

While the information contained in this article is believed to be accurate, Reticon sensor arrays are designed and tested only as optical detectors and no specific performance guarantees can be made for devices used to detect x-rays or electrons.

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Spectral Response of Reticon Linear Photodiode Arrays

1.0 Preface

The purpose of this application note is to provide users of Reticon linear arrays with more detailed information on spectral response and quantum efficiency than is contained in the data sheets.

Included in this information are calibrated spectral response data taken on samples of the Reticon RL1024S device with fiber optic window, with a quartz window and with no window. Also included are data for glass windows calculated using published optical absorption data for the glass material. Because of design similarities, these data apply to **all** Reticon photodiode arrays (as well as the S series and T series listed in Table 1).

The S series and all wide aperture arrays in these families are normally shipped with a quartz window. Narrow aperture versions are shipped with a glass window unless otherwise specified.

2.0 Sensitivity

Sensitivity is the photocurrent (amps) flowing in a diode per unit of light intensity or irradiance (W/cm^2). Since A x sec = C and W x sec = J, sensitivity can be equivalently expressed in terms of signal charge (C) stored on a diode per unit of exposure (J/cm^2), where exposure is defined as the integral of irradiance over the integration time. Thus, the units of sensitivity are $A/W/cm^2 = C/J/cm^2$.

Because silicon photodiodes are not equally sensitive to all wavelengths, it is necessary to specify the wavelength distribution of the light source in order for a sensitivity specification to be meaningful.

3.0 Sensitivity with Monochromatic Sources

Tables 3, 4, 5 and 6 give sensitivity data as a function of wavelength. The data in the column headed REL SENS are the sensitivities at each wavelength relative to the peak at 750 nm and are applicable to all device types considered in this report.

The data in the column headed ABS SENS should be multiplied by the pixel area (cm^2) for each sensor type to yield the sensitivity in $A/W/cm^2$ at each wavelength. Thus neglecting any effects of the window used to seal the package, the sensitivity of the various types in the table below simply scale with their pixel area. The pixel areas for each family of sensors are given in Table 1. Refer to Figure1 for typical sensor geometry.

4.0 Window Effects

The data in Table 3 were taken on a windowless device and show the basic silicon sensitivity. The data in Table 4 are for a quartz windowed device and are identical to Table 3 except for a 5% reflection loss across the entire spectral range. Table 5 shows data for a glass window used in many Reticon devices. It is similar to the quartz window data except for a loss of response in the ultraviolet which is unimportant for most applications. Table 6 gives data for a fiber optic faceplate available on S series devices. The relative response data from Tables 3 to 6 are plotted in Figures 2 to 5.

Unless specially ordered otherwise, the windows used on the various device types are as shown in Table 1.

Table 1. Pixel Area and Window Material for Various Reticon Linear Diode Array Families

Sensor Type	Diode Spacing b (μm)	Aperture Width c (μm)	Pixel Area b x c (cm^2)	Window
A	50.8	50.8	2.58×10^{-5}	glass
C	25.4	25.4	6.45×10^{-6}	glass
C/17	25.4	431.8	1.10×10^{-4}	quartz
G	25.0	26.0	6.5×10^{-6}	glass
H	15.0	16.0	2.4×10^{-6}	glass
H/20	15.0	300.0	4.5×10^{-5}	quartz
L	63.5	76.2	4.84×10^{-5}	glass
S	25.0	2500.0	6.25×10^{-4}	quartz
SF	25.0	2500.0	6.25×10^{-4}	fiber optic

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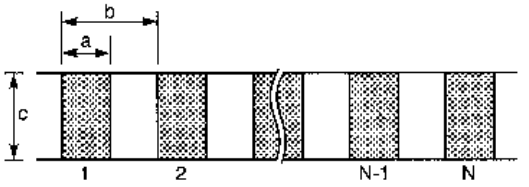


Figure 1. Typical Sensor Geometry of Reticon Line Scanner. Center-to-center spacing of diodes is *b*. Aperture width is *c*.

5.0 Sensitivity with Broadband Light Source

In most applications the light source is not monochromatic, but is rather a lamp or lamp/filter combination with output distributed over a range of wavelengths. Because of various considerations (including convenience in testing, differences in intended application, and historical reasons) various Reticon devices as well as those of other manufacturers have sensitivity specified with different light sources. This makes a direct comparison between the device types difficult on the basis of data sheet numbers. The intent of this section is to present the information necessary to facilitate such comparisons. The various light sources include the following:

2870°K tungsten lamp. This lamp puts out a very broad spectral distribution with most of its energy in the infrared at wavelengths beyond the range where silicon is sensitive. Therefore, since most of the energy is wasted, sensitivity to this source will appear relatively low.

2870°K tungsten lamp band limited between 370 and 1040 nm. The same lamp is used, but the energy at wavelengths longer than 1040 nm (to which silicon is not sensitive) is ignored in measuring the irradiance or exposure. Therefore, since the same signal charge is obtained at a lower measured exposure the specified sensitivity number is higher. It will actually be an average of the sensitivity over the 370 to 1040 nm wavelength range weighted by the intensity distribution of the lamp over this range.

2870°K tungsten lamp with HA-11 filter. The output of a tungsten lamp falls off rather sharply at short wavelengths while the Fish-Schurman HA-11 filter absorbs long wavelengths. The combination gives a roughly symmetrical spectral distribution centered at 600 nm and having an approximately 200 nm width at half height. The response to this source will be very close to that measured for a monochromatic source at 600 nm.

The relative response of a Reticon linear array to these and other common sources is shown in Table 2.

Table 2. Relative Response of a Reticon Linear Array

Source	Relative Responsivity
750 nm monochromatic	1.00
2870°K tungsten, band-limited 370-1040 nm	.90
He-Ne laser	.90
2870°K tungsten, with HA-11 filter	.78
White fluorescent lamp	.72
2870°K tungsten, broadband	.30

6.0 Quantum Efficiency

Quantum efficiency (QE) is the efficiency of converting input photons of light into electrons of charge and is expressed as a percent. Quantum efficiency is related to sensitivity, but the two are not proportional because the energy carried by a photon depends on wavelength according to the relation $E_p = hc/\lambda$ where E_p is the photon energy, h is Planck's constant, c is the velocity of light and λ is the wavelength. If E_p is expressed in eV and λ in nm, the above relation becomes $E_p = 1240/\lambda$.

If either the quantum efficiency or the responsivity is known, the other can be calculated from the relation $QE = E_pS/A$ where E_p is the photon energy in eV, S is the sensitivity in $C/J/cm^2$ and A is the pixel area in cm^2.

In Tables 3 through 6, quantum efficiency is given as a function of wavelength in the column headed QE. These data are applicable to all devices with the indicated window independent of pixel area.

7.0 Examples

At times it is desirable to compare sensitivity performance of a number of Reticon diode sensor families. Since sensitivity is dependent upon light source characteristics, and these characteristics are not always identical, it is helpful to calculate sensitivity of the various families for a particular given light source. Example 1 is a sample of one such comparison. Example 2 extends the comparison one step further by calculating saturation exposure when the sensitivity is known. These calculations are particularly useful for determining light power requirements and integration time when using lasers as a light source.

Example 1

Calculate and compare the sensitivity for the G array and the narrow aperture C array using a 600 nm monochromatic light source. The data sheet sensitivities are considerably different because the C is specified with broadband light and the G is specified using a broadband light filtered with a 1 mm HA-11 filter. However, with monochromatic light both should be similar because both have approximately the same pixel area.

A. G Array

1. From Table 5 (Glass Window), the ABS SENS at 600 nm = .3789.
2. From Table 1, the pixel area is 6.5×10^{-6} cm^2.
3. Using (ABS SENS) x pixel area (cm^2) = sensitivity: $(.3789) \times (6.5 \times 10^{-6}\ cm^2) = 2.46 \times 10^{-6}$ A/W/cm^2 = 2.46 pA/μW/cm^2.

Note: This sensitivity is close to that given in the G data sheet since 600 nm is near the peak of the HA-11 filter.

B. C Array (Narrow Aperture)

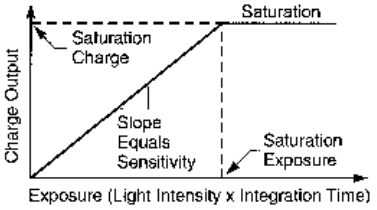
1. From Table 5 (Glass Window), the ABS SENS at 600 nm = .3789.
2. From Table 1, the pixel area is 6.45×10^{-6} cm^2.
3. Using (ABS SENS) x pixel area (cm^2) = sensitivity: $(.3789) \times (6.45 \times 10^{-6}\ cm^2) = 2.44 \times 10^{-6}$ A/W/cm^2 = 2.44 pA/μW/cm^2.

C. Comparison

From the calculations of Step A and Step B, one determines the sensitivities of the G array and the C array with the narrow aperture are approximately equal, i.e., 2.46 pA/μW/cm^2 = 2.44 pA/μW/cm^2.

Example 2

Referring to the calculations in Example 1, if the sensitivity is known, then the saturation exposure (E_{Sat}) can be calculated. The saturation exposure is that exposure level that produces a saturated output charge. The relationship of saturation charge (Q_{Sat}), saturation exposure (E_{Sat}) and sensitivity (S) is graphically shown below:



Output charge versus exposure characteristic.

A. G Array
1. Sensitivity (S) = Q_{Sat}/E_{Sat} , therefore $E_{Sat} = Q_{Sat}/S$.
2. From Example 1, S = 2.46 pA/μW/cm^2.
3. From Section 2, A/W/cm^2 = C/J/cm^2, therefore 2.46 pA/μW/cm^2 = 2.46 pC/μJ/cm^2.
4. Q_{Sat} is a data sheet parameter and for a G array it is specified as 3.2 pC.
5. It then follows that $E_{Sat} = Q_{Sat}/S$ = 3.2 pC/(2.46 pC/μJ/cm^2)=1.3 μJ/cm^2.

B. For the case of the narrow aperture C array
1. Q_{Sat} is specified on the C array data sheet as 4 pC.
2. From Example 1, S = 2.44 pA/μW/cm^2 = 2.44 pC/μJ/cm^2.
3. It then follows that since $E_{Sat} = Q_{Sat}/S$ then E_{Sat} = 4 pC/(2.44 pC/μJ/cm^2) = 1.64 μJ/cm^2.

Table 3. Typical Photodiode Spectral Response
Quartz Window Removed

Peak absolute sensitivity is .4737 A/W at 750 nm.

Wavelength (nm)	ABS SENS	REL SENS	QE
250	.0974	.2057	.4832
300	.1320	.2786	.5456
350	.1550	.3271	.5490
400	.2103	.4438	.6518
450	.2664	.5623	.7340
500	.3192	.6738	.7916
550	.3425	.7230	.7722
600	.3978	.8397	.8221
650	.4447	.9388	.8484
700	.4542	.9588	.8046
750	.4737	1.0000	.7832
800	.4643	.9800	.7196
850	.4207	.8881	.6137
900	.3686	.7781	.5079
950	.2529	.5338	.3300
1000	.1313	.2771	.1628
1050	.0333	.0702	.0393
1100	.0143	.0303	.0162

Optical measurements referenced to standard OP444B.

Table 4. Typical Photodiode Spectral Response
Quartz Window

Peak absolute sensitivity is .4512 A/W at 750 nm.

Wavelength (nm)	ABS SENS	REL SENS	QE
250	.0943	.2090	.4677
300	.1242	.2754	.5135
350	.1500	.3325	.5315
400	.1992	.4415	.6175
450	.2525	.5596	.6957
500	.3028	.6712	.7510
550	.3362	.7452	.7581
600	.3789	.8397	.7830
650	.4192	.9292	.7998
700	.4313	.9560	.7640
750	.4512	1.0000	.7459
800	.4403	.9759	.6825
850	.4055	.8988	.5915
900	.3539	.7843	.4876
950	.2412	.5346	.3148
1000	.1259	.2791	.1562
1050	.0318	.0705	.0375
1100	.0137	.0304	.0155

Optical measurements referenced to standard OP444B.

Table 5. Typical Photodiode Spectral Response
Glass Window

Peak absolute sensitivity is .4512 A/W at 750 nm.

Wavelength (nm)	ABS SENS	REL SENS	QE
250	.0000	.0000	.0000
300	.0000	.0000	.0000
350	.1140	.2527	.4036
400	.1932	.4282	.5989
450	.2500	.5540	.6900
500	.3028	.6712	.7510
550	.3362	.7452	.7581
600	.3789	.8397	.7830
650	.4192	.9292	.7998
700	.4313	.9560	.7640
750	.4512	1.0000	.7459
800	.4403	.9759	.6825
850	.4055	.8988	.5915
900	.3539	.7843	.4876
950	.2412	.5346	.3148
1000	.1259	.2791	.1562
1050	.0318	.0705	.0375
1100	.0137	.0304	.0155

Optical measurements referenced to standard OP444B.

Table 6. Typical Photodiode Spectral Response
Fiber Optic Window

Peak absolute sensitivity is .4165 A/W at 750 nm.

Wavelength (nm)	ABS SENS	REL SENS	QE
250	.0016	.0038	.0078
300	.0000	.0000	.0000
350	.0025	.0059	.0088
400	.1162	.2790	.3602
450	.2012	.4830	.5543
500	.2619	.6288	.6495
550	.3133	.7522	.7063
600	.3473	.8339	.7177
650	.3752	.9010	.7158
700	.4001	.9606	.7087
750	.4165	1.0000	.6886
800	.3954	.9493	.6128
850	.3295	.7911	.4806
900	.2625	.6302	.3616
950	.1697	.4074	.2215
1000	.0768	.1845	.0953
1050	.0207	.0497	.0244
1100	.0102	.0246	.0115

Optical measurements referenced to standard OP444B.

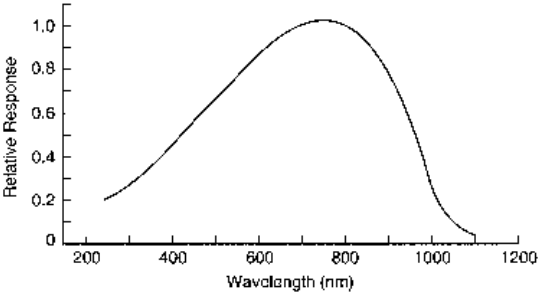


Figure 2. Typical Relative Spectral Response, Window Removed

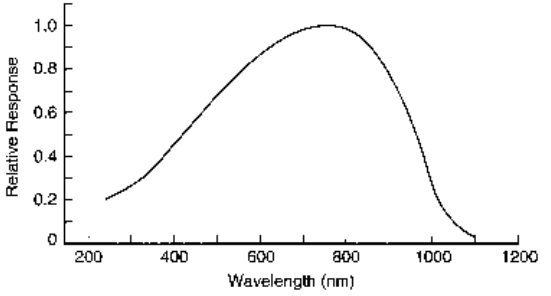


Figure 3. Typical Relative Spectral Response, Quartz Window

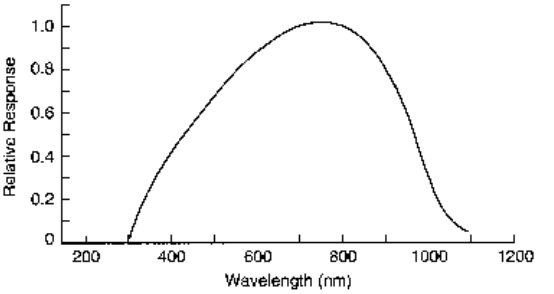


Figure 4. Typical Relative Spectral Response, Glass Window

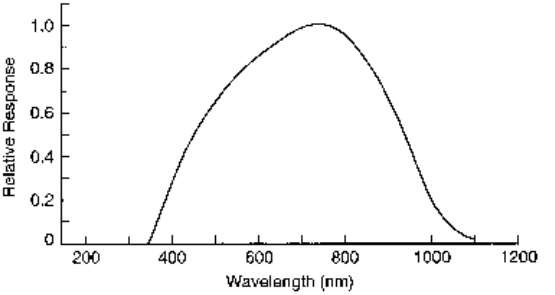


Figure 5. Typical Relative Spectral Response, Fiber Optic Window

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March 1992

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Evolution of the Solid-State Image Sensor

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In any project, research must be done to find the state-of-the-art in design and fabrication. The field of solid-state image sensors is no exception, otherwise time and resources would be wasted repeating tests and observations documented years ago. In today's engineering environment, this waste cannot exist. To obtain this necessary preliminary design background, extensive research was made into the beginnings of the image sensor. This paper covers the three main disciplines: CCD, CID, and photodiodes, including early works, the refinements, and the present technology.

Journal of Imaging Science 29: 1–7 (1985)

Introduction

The present day solid-state image sensor comes in three different technologies: self-scanned diode array; charge injection (CID) array; and charge-coupled (CCD) array. All of these sensors work on the principle of charge storage (or photon-flux integration) to improve their sensitivity.

The major difference between these sensors is found in the readout techniques utilized: the diode array uses a digital scanner to multiplex each signal charge into a common video line; the CID array injects charge into a sense node; and the CCD sensor shifts the signal charge in series to an output-sensing node. Each technique has its merits as well as drawbacks, which lends each technique to certain specific applications and makes it difficult to say that one is superior to the others overall. The trend for future development in solid-state image sensors is to combine the merits of these different techniques into one device.

Each of the three image sensors have come a long way from the first primitive forms to their present structures. The developmental history of each of the three technologies is the subject of this paper.

Charge Storage Operation of the Photodiode

One of the most significant developments leading to the realization of a practical solid-state image sensor was the utilization of the p-n junction photodiode in an integrating or storage mode.[1] Charge-storage operation is based on the principle that, if a p-n junction is reverse-biased and then open-circuited, the charge stored on the depletion-layer capacitance decays at a rate proportional to the incident illumination level.

In the dark, only generation-recombination current (dark current) is available to discharge the depletion-layer capacitance; and, since both depletion-layer capacitance and generation-recombination current are directly proportional to area, the time constant is independent of area. In the dark, time constants of several minutes may be attained in large-area, properly processed silicon-planar-junctions; however, for most standard MOS processes, and for small-geometry photodiodes, a time constant of several seconds is more typical. Figure 1 shows a typical unilluminated decay characteristic for a high-quality p-n junction. Figure 2 shows decay characteristics of the same diode for several illumination levels. The photon-generated current is directly proportional to the illumination level and therefore the amount of charge removed in a given interval of time is directly proportional to the integral of illumination taken over that interval. Thus, by monitoring the charge required periodically to re-establish the initial-voltage condition, one may obtain a signal proportional to the incident illumination. The advantages of this mode of operation are:

1. Improved responsivity resulting from integration of the incident illumination;
2. Electronic control of responsivity by varying the integration time, hence a wide dynamic range.

Two functional elements are necessary to realize charge-storage operation:

1. A charge-storage element. This can be a p-n junction diode, as used in self-scanned photodiode arrays, or an MOS-induced junction, as used in CID and CCD arrays;
2. A charge-reset and sensing circuit.

Figure 3 shows a practical structure which possesses the above characteristics with a p-n photodiode for the photon detection and charge storage. The charge-reset and sensing are done by a MOS FET switch and a voltage source, together with a load resistor, RL. When the MOS switch is turned on, the p-n junction will be reset to a fixed potential, V_0. The charge removed will generate a voltage drop across the load resistor, RL, which represents the total illumination during

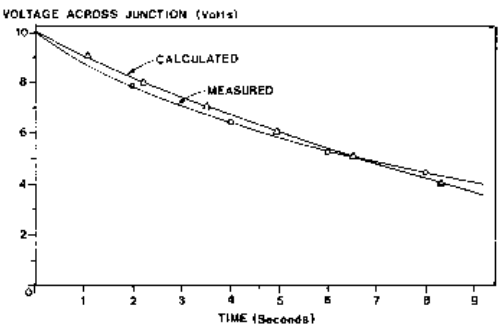


Figure 1. Voltage decay of a silicon planar p-n junction in the dark.

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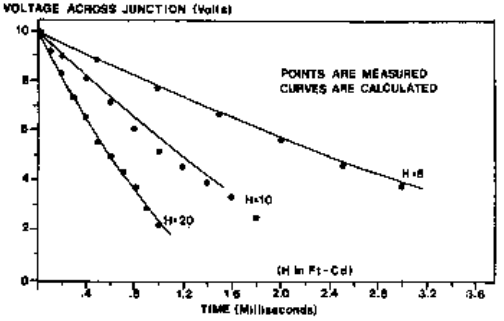


Figure 2. Voltage decay of an illuminated silicon planar p-n junction.

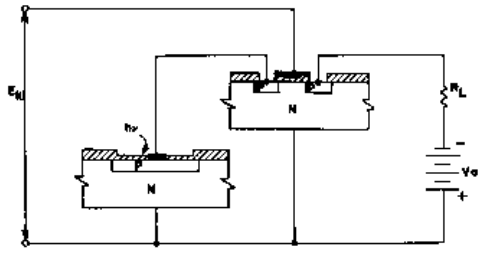


Figure 3. Practical structure using an MOS switch for charging the photodiode.

the integration period. This structure forms the heart of the self-scanned diode array. The CID and CCD use different charge-reset and sensing schemes, which will be discussed later.

Self-Scanned Diode Array Structure—Advantages and Drawbacks

The first practical implementation of storage-mode operation in a monolithic integrated structure was shown in 1965.[2] This device used MOS field effect transistors to access photodiodes (Fig. 3), and was the predecessor to today's self-scanned photodiode arrays. The first array consisted of 200 photodiodes on 2.5 mil centers. Each photodiode was associated with a MOS-FET. The gates of the MOS-FETs were individually brought off-chip where they were connected to an externally fabricated scan generator. This was done before the advent of gate protection, and thus required the utmost care in handling.

The photodiode image sensor was almost immediately displaced by the phototransistor operating in the storage mode.[3] The phototransistor was thought to have many advantages over the photodiode MOS-FET combination, partly

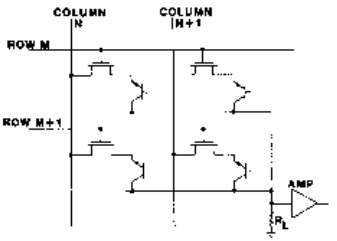


Figure 4. Circuit diagram of an x/y-addressable phototransistor array.

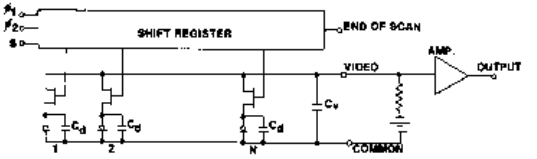


Figure 5. Equivalent circuit for a self-scanned diode array.

because transistor technology was much farther advanced at that time than MOS technology. Some of the advantages supporting the phototransistor approach were:

1. Lower operating voltages;
2. Signal enhancement due to the transistor gain;
3. Ease of fabrication.

The major disadvantages, and factors which eventually returned the photodiode to favor, were the random variations in transistor gain and the low-level threshold due to the emitter offset. However, during the several years of development effort trying to improve phototransistor uniformity, both linear and area arrays were developed using phototransistors.

Figure 4 shows an integration of phototransistor array and insulated-gate FET into an x-y addressable matrix. The scanning of the x and y required an external scan generator. The interface between the external scanner and the array degraded performance, increased cost, and reduced reliability.

During the period when the phototransistor was in vogue, MOS technology was being developed, and in particular, silicon gate technology was developed. The marriage between MOS integrated circuit technology and the photodiode array has resulted in today's self-scanning photodiode image sensors.

Figure 5 shows an equivalent circuit of a self-scanned photodiode array. The basic device consists of a silicon chip containing a row of photodiodes and a parallel shift register. Connected to each stage of the shift register is the gate of an MOS switch which couples the adjacent photodiode to a common video line. The shift register is driven by complementary square wave clock voltages and each scan is initiated by a start pulse. The start pulse loads a bit which is clocked through the register, successively closing and opening the switches, thus connecting each photodiode in turn to the video line. As each photodiode is accessed, it is charged to the video line potential and left open-circuited until the next scan. During this period it will be discharged by an amount equal to the instantaneous photocurrent integrated over the line scan time. Each time a diode is sampled, this integrated charge must be replaced through the video line. The resulting video signal is a train of charge pulses, each having a magnitude proportional to the light intensity on the corresponding

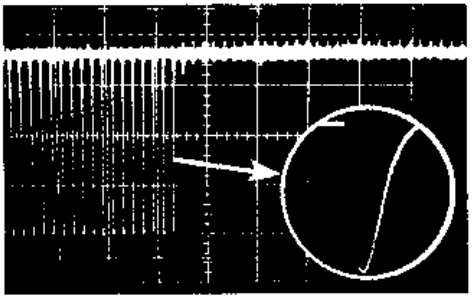


Figure 6. Output waveform using the circuit of Fig. 5.

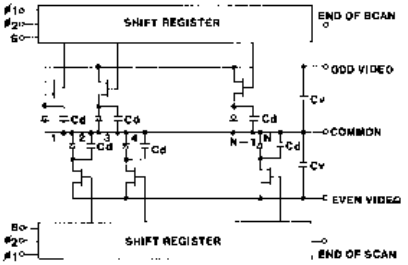


Figure 7. Equivalent circuit for an interdigitated diode array.

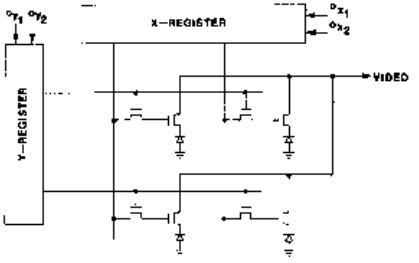


Figure 9. Schematic of a two-dimensional area array, each diode requiring two multiplex switches.

photodiode. Figure 6 shows an oscilloscope photo of such a charge output.

The center-to-center distance of a self-scanned photodiode array is usually limited by that of the scan register. To increase the density of a diode array, an interdigitated structure was introduced. Figure 7 is an equivalent circuit of such an interdigitated sensor. It consists of two simple self-scanned arrays with the sensors interdigitated from either side to form a continuous row. By properly phasing the clock drives to the two shift registers, all of the diodes can be sampled in proper sequence. The two video lines can then be connected together to provide a continuous train of output charge pulses. Figure 8 shows the historical development of the linear solid-state image sensor.

To achieve a two-dimensional diode array, each diode requires two multiplex switches, as shown in Fig. 9. This requirement makes the center-to-center distance of the array quite large (100 μm). As a result, the highest-density array that has ever been made using this structure is about 50 by 50 pixels. To obtain a higher-density array, a line integration

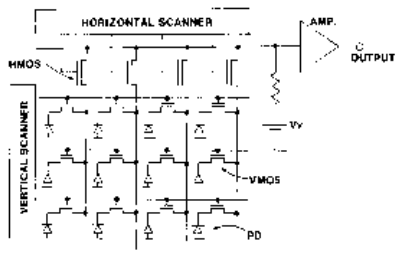


Figure 10. Two-dimensional area array using line integration, each diode requiring only one multiple switch.

structure was developed as shown in Fig. 10. The vertical scanner selects one row at a time, transfers the diode charges into the vertical video lines, and then reads out in sequence by a horizontal scanner. Using this structure, area arrays with

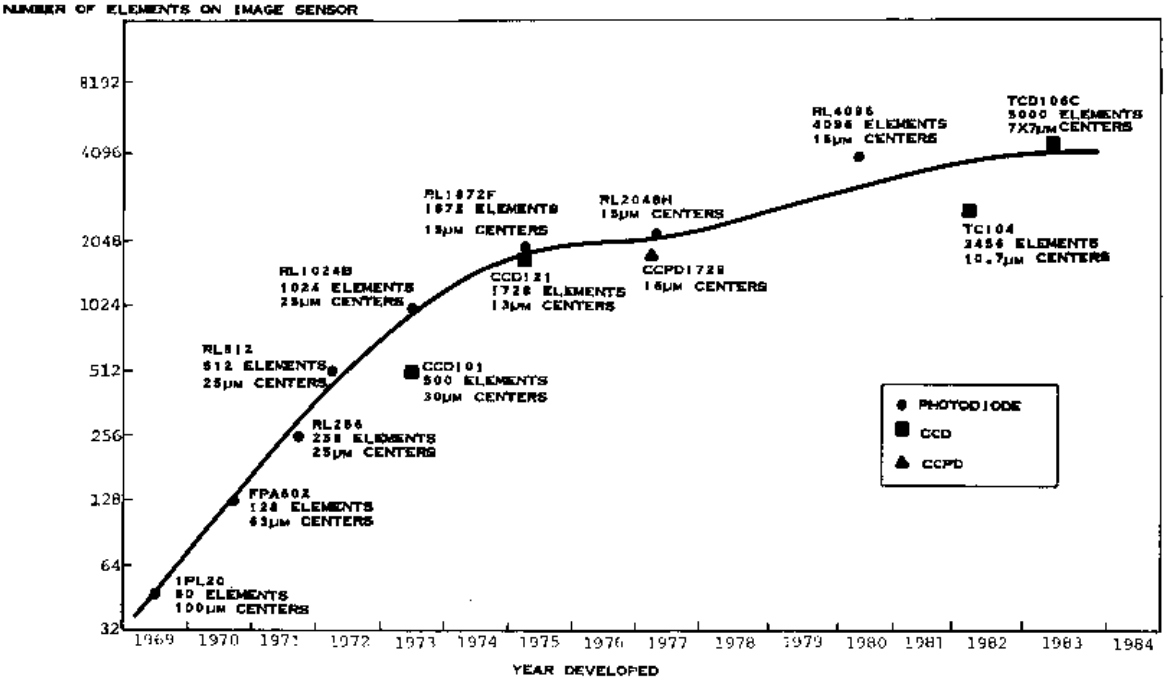


Figure 8. Historical development of the linear solid-state image sensor.

the resolution of commercial TV cameras have been developed.[4] The advantages of the self-scanned diode are:

(*a*) High quantum efficiency—the full and smooth silicon spectral responses can be utilized;
(*b*) Ease of manufacturing—compatible with modern MOS technology;
(*c*) Low dark current;
(*d*) Flexibility of design—the photodiode can be in any shape, any size. Custom arrays with very wide apertures, circular apertures, as well as random access structures can be easily implemented;
(*e*) No smearing, no shading problem resulting from charge transfer loss as in CCD arrays;
(*f*) Isolated diode—less of a blooming problem;
(*g*) Entire active area is sensitive to light.

The drawbacks of the diode array are fixed-pattern noise and high video-line capacitance, which make low-light-level imaging difficult.

CID Array Structure—Advantages and Drawbacks

The development of charge-injection image sensors started in the early 70's at General Electric.[5,6] CID sensors employ intracell transfer and injection to sense photo-generated charge at each sensing site. Sites are addressed by an *x-y* coincident-voltage technique similar to that used in digital memory. In early structures, readout was performed by injecting the charge from individual sites into the substrate and detecting the resultant displacement current. Figure 11*a* depicts a basic CID structure. The charge collected during the integration is maintained in the potential well formed by the two MOS storage capacitors, as shown in Fig. 11*b*. Readout of a selected site is accomplished by removing the voltage on both capacitors, allowing the charge to be injected into the substrate, as shown in Fig. 11*c*. When the voltage is removed from only one of the electrodes, as occurs along a selected row and column during readout, charge is transferred to the remaining potential well and is not injected into the substrate.

The raw video signal consists of the substrate charge injected from each sensing site in sequence. The signal appears in combination with the parasitic capacitive coupling of the

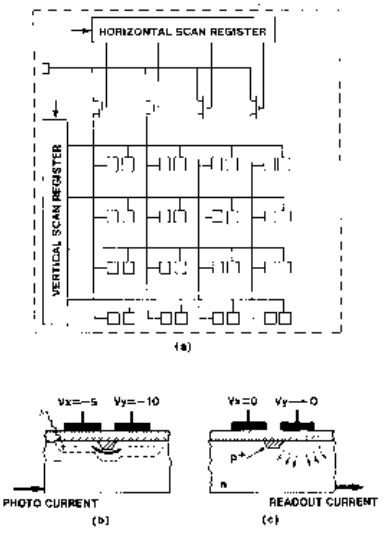


Figure 11. Change injection device. (*a*) Basic readout organization. (*b*) One cell integration and charge transfer. (*c*) During charge injection.

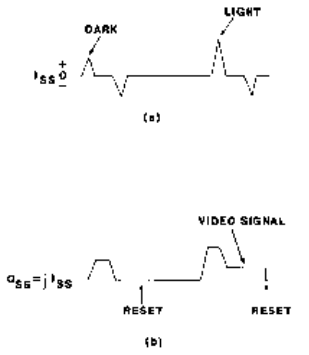


Figure 12. CID video signal. (*a*) Substrate current results from charge injection. (*b*) Current integration to cancel out parasitic coupling.

drive voltage to the substrate. The drive voltage interference can be canceled out through the use of an integrating readout technique. The pulse train of Fig. 12*a* shows the substrate current signal that results from interrogation of a dark and an illuminated element. The level of illumination will cause a change in the height of the leading pulse edge. If this current signal is integrated, the light-generated information is recovered. The integral of this current waveform, as seen in Fig. 12*b*, results in self-cancellation of the parasitic drive-line interference. This type of readout scheme is referred to as "sequential injection."[6]

Readout can also be implemented by measuring charge transfer between two storage capacitors that are used at each sensing site in an array. In an X-Y addressable array, the transfer can be performed on all sensing sites along a row in parallel. Each row can also be cleared of signal charge by performing the injection operation in parallel at all sites in the addressed row. This readout technique has been termed "parallel injection."[7]

A diagram of a 4 × 4 array using parallel injection is illustrated in Fig. 13 with the relative surface potentials and signal charge included. At the beginning of a line scan, all rows have voltage applied and the column lines are reset to a reference voltage, *Vs*, by means of switches S1 through S4, and then allowed to float. Voltage is removed from the row selected for readout (×3 in Fig. 13) causing the signal charge at all sites of that row to transfer to the column electrodes. The voltage on each floating column line then changes by an amount equal to the signal charge divided by the column capacitance. The horizontal scanning register is then operated to scan all col-

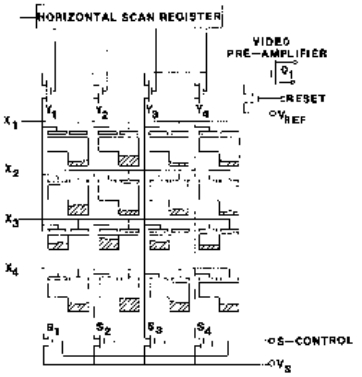


Figure 13. Schematic diagram of a 4 × 4 CID array designed for parallel-injection readout. Silicon surface potentials and signal charge locations are included.

umn voltages and deliver the video signal to the on-chip preamplifier, $Q1$. The input voltage to $Q1$ is reset to a reference level prior to each step of the horizontal scan register.

At the end of each line scan all charges in the selected row can be injected simultaneously by driving all column voltages to zero through switches S1 to S4. Alternately, the injection operation can be omitted and voltage reapplied to the row after readout, causing the signal charge to transfer back under the row electrodes. This action retains the signal charge and constitutes a nondestructive readout (NDRO) operation.

The CID imaging technique requires that the collected photon-generated charge be ultimately disposed of by injection into the substrate. Upon injection, this charge must either recombine or be collected to avoid interference with subsequent readouts. For the high lifetime material usually required for image sensors, recombination is not a suitable method of charge disposition, since recollection of this charge can give rise to objectionable image lag and crosstalk. For this reason, most CID imagers are fabricated on epitaxial material. The epitaxial junction, which underlies the imaging array, acts as a buried collector for the injected charge. If the thickness of the epitaxial layer is comparable to the spacing between sensing sites, most of the injected charge will be collected by the reverse-biased epitaxial junction and injection crosstalk is minimized.

CID cameras with resolution close to standard TV cameras are commercially available. They are commonly used in security and surveillance systems as well as for industrial applications. CID imagers have the following advantages:

(*a*) Low blooming due to expitaxial structure;
(*b*) Flexibility of operation—can be operated in nondestructive readout mode;
(*c*) Flexibility of design can be implemented in random access structure;
(*d*) No smearing, no shading due to charge transfer inefficiency;
(*e*) Entire active area is sensitive to light;
(*f*) Low dark current.

The drawbacks of CID sensors are:

(*a*) Poor spectral resonse due to absorption of long wavelength photons by polysilicon gates;
(*b*) Fixed pattern noise and high video line capacitance make low-light-level imaging difficult;
(*c*) Requires an epitaxial substrate, which is not compatible with standard MOS process;
(*d*) Loss of sensitivity due to absorption of photons by epitaxial layer.

CCD Array Structure—Advantages and Drawbacks

Unlike the bucket-brigade (BBD) devices in which the signal charges are transferred by charging and discharging of capacitors,[8] the CCD devices transfer the signal charge by manipulation of MOS potential wells. The development of CCD began in 1969 at Bell Labs.[9] In the simplest implementation, CCD's consist of closely spaced capacitors on an isolated surface of a semiconductor, as shown in Fig. 14. Figure

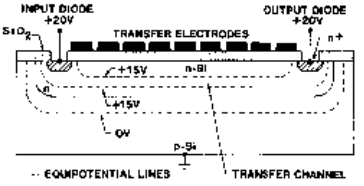


Figure 15. Longitudinal cross section through a bulk channel CCD showing the channel layer in contact with the reverse biased input-output diodes and equipotential lines which indicate the actual position of the transfer channel.

14*a* shows the potential well during integration and storage when only one electrode is turned on. During charge transfer, with two adjacent electrodes simultaneously turned on to the same potential, the charge packet will distribute uniformly underneath the two electrodes. When the first electrode is turned off, the charge will be pushed completely to the second one (Fig. 14*b*). To continue this charge transfer, the following electrode is pulsed to a high potential, and so on. This simple-but-powerful concept proved to be so stimulating that, almost overnight, a host of electrode structure variations and dozens of potential applications were conceived.

The device described here transfers and stores the signal charge in the potential wells at the silicon-silicon dioxide interface and is referred to as a surface-channel CCD. The interaction of the signal-charge packets with interface states imposes certain lower limits on transfer inefficiency and transfer noise. To prevent this interaction, the effective transfer channel can be located away from the $Si\text{-}SiO_2$ interface, deeper into the bulk of the device, with the use of an epitaxial or ion-implemented silicon layer of opposite polarity to that of the substrate. As shown in Fig. 15, this layer is in electrical contact with the output diode, which drains out all mobile carriers when suitably reverse-biased. The potential minimum under each transfer electrode will then be formed inside this layer, but generally away from the $Si\text{-}SiO_2$ interface. The clock pulses applied to the transfer electrodes modulate the channel potential to produce moving potential wells, just as in the case of a surface channel CCD. This device is referred to as "bulk channel" or "buried channel CCD."[10]

Through the development history of the CCD, numerous electrode structures have been proposed. Some popular structures used by designers are:

(*a*) Two-phase, double-layer poly-silicon gate with ion-implanted barrier;
(*b*) Four-phase, double-layer silicon gate structure;
(*c*) Three-phase, triple-layer silicon gate structure.

Recently a new virtual phase structure has been developed at Texas Instruments.[11] This structure, utilizing surface potential pinning effects, requires only a one-layer poly-silicon gate. The other electrode is an accumulation layer formed by ion-implantation on the silicon surface. As a result, it provides low dark current and smooth spectral response for image-sensing applications.

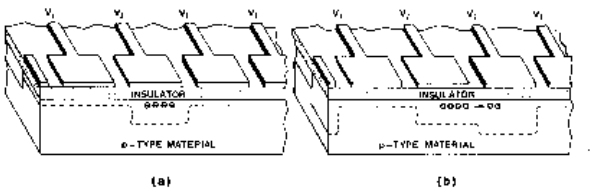


Figure 14. Basic cell of a 3-phase CCD formed by three MOS capacitors shown (*a*) during integration and storage and (*b*) during charge transfer.

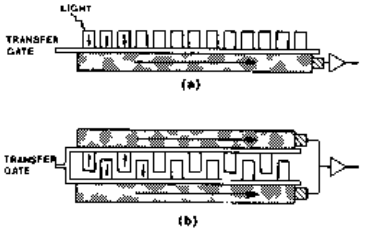


Figure 16. Readout organizations of CCD linear image sensors. (*a*) CCD with separate integration sites, (*b*) bilinear arrangement.

The application of CCD to image sensing is straightforward. Figure 16 shows a block diagram of a linear array. In Fig. 16*a*, the linear sensor consists of a row of isolated photosensors, a transfer gate, and a light-shielded CCD readout shift register. The photosensors, normally depleted MOS capacitors, integrate the photons. After one integration period, the transfer gate is opened, and all the charges integrated at the photosensors transfer in parallel into the CCD readout register, which has one complete transfer cell opposite to each photosensor. After the gate is closed, the photosensors immediately start integrating the next line, while the previous line is read out along the transfer register. At the end of the register, there is an output amplifier, normally a gated charge integrator, which converts the charge into signal voltage. The maximum number of resolution elements obtainable from such a device is given by the maximum feasible overall device length divided by the cell dimension. A practical limit on the number of elements is given when the transfer inefficiency product of the readout register exceeds about 0.5, at which point the modulation transfer function for spatial frequencies at the Nyquist limit incident at the end of the device farthest from the output is reduced to 37%. In both cases, when the resolution is limited either by the cell dimension, or by insufficient transfer efficiency, a bilinear approach, according to Fig. 16*b*, can yield an additional factor of two in resolution. Two structures corresponding to Fig. 16*a* are integrated into a single device by interdigitating the two sets of photosensors. The pulse trains from the two registers are combined at the output with an alternate merge that conserves the proper phase relation.

For area imaging using CCD, two readout organizations are being used; a frame-transfer structure, and an interline-transfer structure, as shown in Fig. 17. In the frame-transfer structure (Fig. 17*a*), a separate shielded storage area is needed. After integration, the charges collected in the sensing area are shifted rapidly into the storge area. While the sensing area is integrating the next field, the signal charges in the storage area are read out line by line. In an interline structure (Fig. 17*b*), a separted, shielded vertical CCD register is needed along each column of sensing cells. After the end of integration, the charges in the sensing cells are transferred into the vertical shift register in parallel. While the photosensors are integrating the next field, the vertical shift register transfers the charge into the horizontal readout register one line at a time.

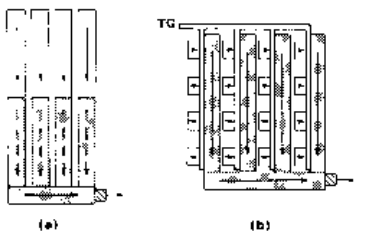


Figure 17. Readout organizations of image sensors: (*a*) frame-transfer organization, and (*b*) interline-transfer device.

The major advantages of CCD image sensors are:

(*a*) Low noise, high sensitivity—suitable for low-light-level imaging;
(*b*) A CCD structure suitable for high resolution sensor integration;
(*c*) Low dark current, smooth spectral response for virtual phase structure;

However, the CCD imagers also possess the following drawbacks:

(*a*) More complicated fabrication process;
(*b*) More serious blooming and smearing problems as compared with other types of sensors;
(*c*) Poor quantum efficiency and spectral response for multi-layer gate structures;
(*d*) High dark current for buried-channel structures;
(*e*) Limited operating voltage range for virtual phase structures;
(*f*) Less flexibility of design compared with other types of sensors;
(*g*) Low saturation charge.

Present Status for Solid-State Image Sensor Developments

Although tremendous progress has been made in the development of solid-state image sensors, efforts to develop a better, denser, and cheaper array have never stopped. The two major driving forces behind the development of the next-generation sensors are the VCR consumer market and robotic industrial applications. For the VCR market, the major concerns are the sensor cost, sensitivity, spectral response, blooming control, and dynamic range. To achieve the required parameters, efforts have been made to combine the advantages of the photodiode, with its better spectral response, and the CCD register, with its low-noise readout.[12,13] Considerable progress has also been made on blooming control. A vertical blooming control scheme[4] and electron-hole recombination scheme through surface traps[14] have been successfully implemented.

In industrial applications, the major considerations are higher density, especially for copier and printing applications, and faster speed. To obtain a higher density, a linear array with serpentine shift registers has been implemented.[15] A bilinear array structure with four output registers has enabled the integration of a 5732-element sensor in ½"-long silicon.[16] For high speed operation, in addition to pushing for higher clock rates, multiple output structures are also quite popular.[17,18]

Conclusions

This brief discussion of the various structures of solid-state image sensors is intended to provide some basic technical information and historical background for the reader. It is hoped this introduction will stimulate interest for further research in the field of solid-state image sensors.

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Self-scanned photodiode array: a multichannel spectrometric detector

Yair Talmi and R. W. Simpson

The performance characteristics of a 1024-element self-scanned photodiode array, related to its use as a multichannel spectrometric detector are described. The parameters discussed include, spectral and temporal response, blooming, geometric accuracy, noise sources, dynamic range, signal integration and spectral as well as spatial resolution.

I. Introduction

In the last decade, there has been considerable interest in the utilization of image devices, both linear and area, as multichannel (parallel) spectrometric detectors. The advantages of such detectors are derived from their capability to monitor simultaneously and digitally acquire entire spectra. The speed and ease of data acquisition and interpretation achieved by these electronic photographic plates have turned them into an attractive candidate for the evolutionary cycle of spectrometric detector development, i.e., photographic plates (parallel) to electronic photomultiplier tubes (PMTs) (single) to optoelectronic image devices (parallel).

Until recently, unfortunately, optoelectronic image devices (OIDs) were designed by manufacturers with very little knowledge of, interest in, or sympathy for the needs of research spectroscopists ("an economically uninteresting, eccentric, and rare group of scientists"). Consequently, the spectrometric performance of these devices has been always unsatisfactory in some respect: an insufficient number of individual sensors (pixels); poor UV and IR response; laggy signal readout; pixel-to-pixel signal cross talk (blooming); too narrow dynamic range; wrong geometry; poor geometric stability and registration; stray light in the detector's enclosure; etc.

Recently, after years of unsuccessful persuasion campaigns, conducted by a handful of "poor" spectroscopists and finally won by fewer yet, "rich" ones, EG&G-Reticon has introduced a new self-scanned linear photodiode array (SPD) that has been specifically designed as a parallel spectrometric detector. A self-scanned linear photodiode array is a large scale integrated circuit fabricated on a single monolithic silicon crystal. It contains a row of photodiode sensors, typically on 25-μm centers, along with a scanning circuitry for sequential readout (Fig. 1).

In a self-scanned photodiode array the photodiode geometry is defined by diffused p-type bars in a n-type silicon substrate. The center-to-center distance between the diodes defines the resolution in the scan direction. The height of the diode sensing area is determined by an aperture in a metal mask, which runs perpendicular to the p-type bars. Light incident on the sensing area generates a charge, which is collected and stored on the p-type bars during the integration period. The accumulated charges are then sequentially switched into the video output for readout. The n-type as well as the p-type silicon surface is photosensitive. Light incident on one of the p-regions will generate charge, which is stored on that diode. Charge generated by light incident on the n-type surface between two p-regions will divide between the adjacent diodes to produce the idealized response function shown at the bottom of Fig. 2.

In conventional devices designed for facsimile scanning applications, the aperture dimension is the same as the center-to-center spacing, resulting in a square resolution element. In spectroscopy, where often the

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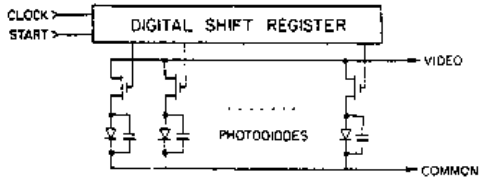


Fig. 1. Simplified schematic diagram of typical self-scanned photodiode array.

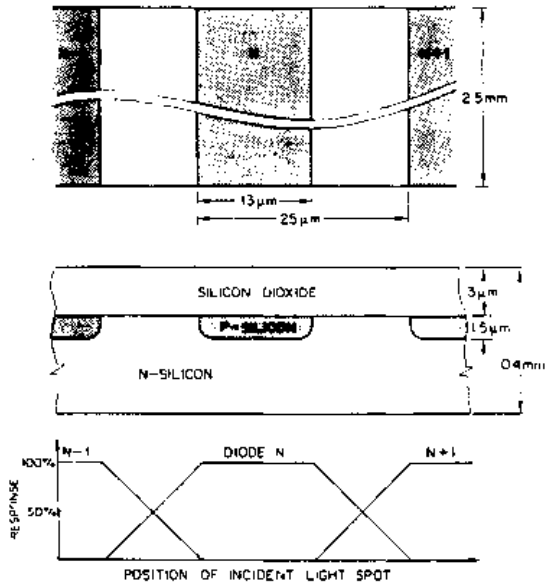


Fig. 2. Sensor (diode) geometry and idealized aperture function.

measured record is one-dimensional, it is desirable to increase the aperture to collect more light.

This paper intends to present an account of the spectrometric performance of a new SPD, the EG&G-Reticon *S*-series device, with individual diodes whose apertures have been increased to 2.5 mm (Fig. 2), so that an aspect ratio of 100:1 has been achieved, corresponding to the typical aspect ratio of a conventional polychromator slit. This evaluation is generally applicable, but specific results were obtained with the EG&G-PARC Optical Multichannel Analyzer (OMA) detection system, model 1218 (detector controller) and model 1412 (detector head).

This paper will be succeeded by a sequel to be published in *Analytical Chemistry* that will discuss more specifically the feasibility of this detection system to a few areas of spectroscopy including molecular absorption and emission (fluorescence), laser microprobe, and induction-coupled-plasma atomic emission.

II. Spectral and Energy Response

A. UV–NIR Region

Experimental setup: deuterium, tungsten, and xenon (short-arc) lamps were used as primary sources. Monochromatic light necessary for quantum efficiency measurements was obtained through the use of narrow bandpass spectral filters (two matched filters in tandem arrangement for each point). Neutral-density filters (ND) were used for light attenuation. An EG&G calibrated photodiode served as the radiometric detector. Similar measurements were performed by the EG&G Electro-Optics Division, Salem, Massachusetts, and Optronics, Inc., although the equipment used was different (spectrometer-based radiometers), and the SPD was electrically shorted, i.e., transformed to a giant single photodiode. This was necessary because neither company had an OMA system available to them.

Figure 3 shows the spectral response curves obtained by the three laboratories. Only the Optronics data are shown, however, <250 nm, because the spectral filters available to us (in this region) were too broad (≃30 nm HBW). The experimental agreement between the three curves is well within what is expected for such measurements. The UV response of the SPD is very high and does not show any declining tendency even at 190 nm. Although not yet verified, it is expected that the SPD will be responsive in the entire VUV region. In the soft x-ray region, however, <500 eV, it has been shown to be rather insensitive.[1]

We vacuum deposited directly on the surface of the diodes a very thin (~0.2-μm) layer of various organic phosphors (UV to blue light converters) that extended the response of the SPD to the VUV and x-ray regions (≃15–20% quantum efficiency at 150 nm). In the x-ray region, however, rare-earth phosphors (nonvolatile) should be more appropriate.[1] At the higher x-ray region, i.e., >2 keV, it seems advantageous to deposit the phosphors on an optical fiber coupler attached to the diode array.[2] This approach allows easy removal of the phosphors if necessary and provides much better protection of the array from the high energy photons.

B. Direct X-Ray and Electron Detection

Because their energy is higher, x rays produce more charge pairs per incident photon in silicon devices than visible or UV light. It has been shown that both diode arrays[3] and CCDs[4] respond directly to soft x rays in the 1–10-keV region. Considering the low preamplifier noise of these devices and their high x-ray quantum efficiency, a sensitivity approaching photon-counting levels should be easily achievable. No damage to the array was observed when the array was used as an x-ray spectrometer detector.[5]

Self-scanned diode arrays are also excellent electron detectors. (Approximately one charge is produced for every 3.6 eV of electron energy once the silicon–oxide overcoat is penetrated.) Diode arrays were used as targets in electron bombarded (EBT) intensified imagers, e.g., Digicons,[6] and also as transmission electron

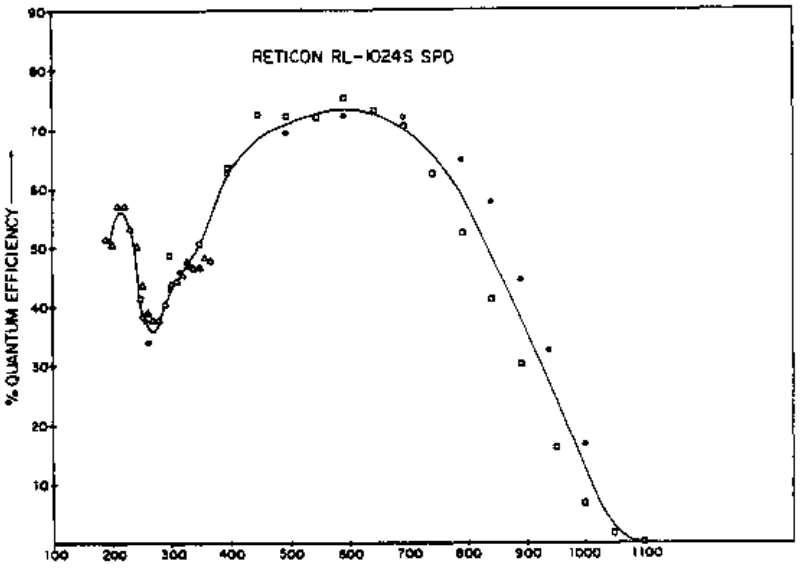


Fig. 3. UV-NIR spectral response characteristics of EG&G-Reticon RL-1024S photodiode array: ○, measured by authors at ~20°C; □, measured by EG&G Electro-Optics Division at 25°C; △, measured by Optronics at 25°C.

microscope (energy absorption spectrometry) detectors.[7]

At electron energies <20 keV (Digicons) low-level target damage has been noticed, manifested as an increase in the dark charge level by as much as a factor of 10 over the initial level.[6] An effect of that magnitude is tolerable in many applications. Furthermore, this damage can be annealed by exposure of the array to 4.5-keV energy electrons[8] (possibly correlated to the energy required to penetrate the trapping silicon–silicon oxide interface). At higher energies,[7] however, the increase in dark charge level did not show a tendency to reach a saturation level but rather increased at a rate roughly proportional to the square root of the exposure (equivalent) charge. It has not as yet been established whether damage of that magnitude can be annealed. Nevertheless, since the response of the diode array to high-energy electron radiation is very high, single electron detection is easily accomplished[8] so that in many applications the incident flux can be greatly reduced to minimize target damage. Figure 4 shows the electron transmission spectrum of carbon obtained in real time.[7] Finally, diode arrays can also be used as spatial (as well as spectral) multichannel detectors for both electron radiation and x rays.[9]

III. Readout Lag

Readout lag is a phenomenon associated with electron readout beam image devices (vacuum devices), whereby a complete readout of the latent signal stored on target cannot be achieved with a single scan.

The SPD however (similar to other nonvacuum solid state imagers) is practically lag-free: each diode is fully recharged in <1 μsec.

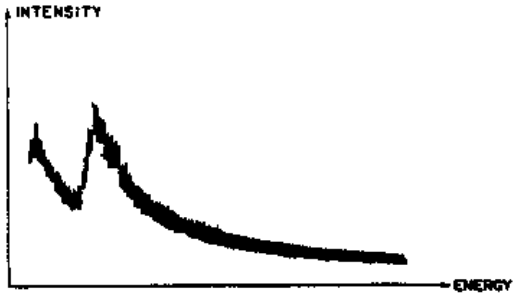


Fig. 4. Electron transmission spectrum of carbon directly detected by photodiode array.

It has been reported[10] that a residual charge (lag) of ~1% was observed after saturation of the SPD. This phenomenon, however, has been attributed to the 1-msec time constant of the preamplifier feedback circuit and was not observed with the EG&G-PARC voltage mode preamplifier.

The lag of the SPD was measured in the following manner: The emission spectrum of a single xenon flash produced by a stroboscope was detected (stored) by the SPD. This flash, whose decay time is substantially shorter than the SPD scan time (16 msec), also provided the external trigger pulse necessary to initiate five sequential readout scans. Any residual charge (lag) not read in the first scan would have shown in the following four scans. Figure 5 shows the first five consecutive scans (in a display-compressed mode) as well as the

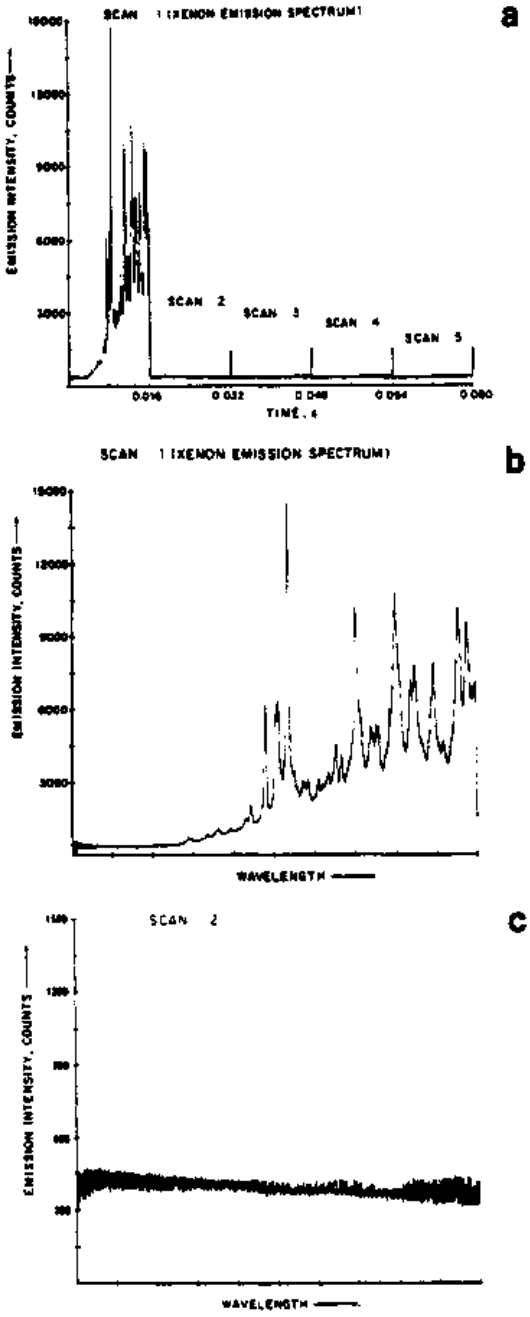


Fig. 5. (a) Five consecutive photodiode array scans (readouts) following detection of single xenon flash; (b) emission spectrum of xenon flash, first scan after detection; (c) second detector scan, no traces of xenon emission spectrum are noticeable.

Table I. Effect of Diode Saturation on Adjacent Diodes

Integration period (sec)	Signal level (counts)	Channel (diode) no.
0.080	20.4	150
0.800	204	150
8.000	2020	150
0.080	122	195
0.800	1232	195
8.000	12210	195
0.080	220	200
0.800	2205	200
8.000	ADC saturated (≃22000)	200
0.016	2282	230
0.096	13667	230
0.800	Saturated (≃diode saturation level)	230
8.000	Saturated (≃ten times diode saturation level)	230

expanded (all 1024 pixels) first and second scans. No apparent trace of the xenon spectrum is noticeable in the second scan. Even when the light level was raised to ~5 times the ADC level (for the most intense xenon spectral feature), the lag was <0.1%.

IV. Blooming

As will be shown, stray light in the detector assembly can drastically reduce the intraspectral dynamic range of an image detector. Similarly, blooming, signal cross talk between adjacent pixels (due to charge spillover), may also reduce the dynamic range, although the apparent effect is more specific in nature, similar to that caused by near-field veiling glare. Blooming will degrade the accuracy of the transferred spectra since high intensity spectra features can partially (or fully) mask any neighboring weak spectral features, i.e., spectral interference.

To study the extent of blooming in SPDs, two experiments were performed:

(1) The line emission spectrum of a Ne discharge lamp (600–800-nm region) and the UV transmission spectra of various spectral filters were on-target recorded at various integration times. As the integration time was raised, the magnitude of the signals was proportionally raised, first above the ADC level ($\simeq 2 \times 10^7$ electrons) and then above the diode saturation level ($\simeq 2 \times 10^8$ electrons). Low-intensity spectral features were measured and the interference from nearby saturated features studied. By measuring the intensity profile of isolated spectral lines at the same integration times, it was possible to determine the intensity measured by the line-wing diodes (apparent blooming) and therefore to differentiate it from real blooming.

A spectral filter, 40% peak transmission at 240 nm and a HBW of 5 nm, was selected to simulate a transmission spectrum. This spectrum was recorded on-target at different integration times, and the reciprocity of the signal was measured at a few diodes (Table I). The reciprocity has been clearly maintained despite the saturation of nearby diodes, thus indicating that the

blooming is minimal. Indeed, the architecture of the SPD suggests that charge spillover is a gradual and contained process, one diode at a time, and its effect is therefore highly localized (particularly considering the magnitude of the diode junction capacitance). Similarly, the discharge lamp experiment has shown that even at a line intensity ratio of 500:1 (the highest ratio observed for two adjacent lines), no apparent blooming was observed for two lines separated by as little as 12 pixels.

(2) A He–Ne laser beam was split with a prism, and each beam was separately attenuated (ND filters) and focused into the target of the SPD. By varying the degree of attenuation and the spatial separation between the beams, the combined effects of blooming and veiling glare were measured.

At a 1000:1 signal intensity ratio, even where the more intense beam produced a charge signal 20 times above the ADC saturation level and with a spatial separation (peak to peak) of 15 diodes, the cross talk measured was <1%.

V. Geometric Accuracy

Spectrometry in general and spectrophotometry in particular require a high degree of wavelength accuracy, i.e., the accuracy at which a predetermined narrow region of the spectrum can be addressed. Furthermore, adequate wavelength accuracy is absolutely essential for various computer data processing manipulations, e.g., differentiation, smoothing, and spectral stripping,[1] where relatively minute addressing errors can cause serious measurement errors.

Unlike scanning spectrometers, whose wavelength accuracy is mechanically limited, an SPD-based spectrometer is limited mainly by vibration and thermal expansion of the optical components, assuming stability of the light source. Thus, the wavelength accuracy of an SPD spectrometer is directly related to the geometric (spatial) accuracy of the grating, a spectral-to-spatial transformer. The geometric accuracy of the SPD itself is excellent, reflecting the accurate manufacturing techniques of integrated circuits and the millidegree (Celsius) precision thermostating achieved.

To evaluate the overall geometric accuracy performance of a SPD spectrometer, the following experiments were performed.

(1) The SPD was accurately placed at the exit focal plane of an EG&G-PARC model 1208 (an Ebert-Fastie mount) 0.3-m polychromator. A 240-nm blazed 2400-g/mm grating has produced a spectral bandpass of ~0.035 nm/diode.

To reduce the effect of polychromator vignetting, only the central 12.5 mm of the focal plane (500 central diodes) was used. The UV-transmission spectrum of a holmium–oxide filter was detected in real time. The filter, securely held in front of the entrance slit, was removed and reinstalled a few times, and the wavelength position (diode address) of the 280- and 288-nm bands was determined (Table II). As long as the grating position remained constant (unaltered spectral window), the absolute position of the bands also remained constant. (These measurements were taken during a 1-h period.) Furthermore, even after the spectral window was changed (grating rotation), the relative position of the two bands remained constant to within a single diode (0.035 nm). The error of one diode, which sets the limit on the geometric accuracy of the SPD, originates from the architecture of the OMA system (see Sec. IX). Other systems utilizing centroid finding techniques should provide a geometric accuracy that is a small fraction of a diode width. Alternatively, Hg emission lines were used as internal spectral standards from which the apexes of the two bands could be determined, again with an accuracy of 0.035 nm.

Table II. Geometric Accuracy (Wavelength vs Diode Number) of the SPD Measured with Ho–Oxide Spectral Filter

Grating position	No. of measurements[a]	Peak ratio (band 280/band 288)	Pixel separation between peaks
1	10	1.3175 ± 0.0017	59 ± 0.0
2	10	1.3178 ± 0.0015	60 ± 0.0
3	10	1.3176 ± 0.0018	59 ± 0.0
4	10	1.3173 ± 0.0017	60 ± 0.0

[a] Holmium–oxide filter was removed and reset each measurement.

(2) The geometric accuracy was also determined with a JACO model 75-150 a 1-m Czerny-Turner mount polychromator with a 590-g/mm grating blazed at 250 nm, 0.0206-nm/diode spectral bandpass. The SPD was used to monitor the emission spectra of various samples excited by an induction coupled plasma source.

Using only two internal standard reference lines, located at diodes 6 and 20, it was possible to determine the identity of all other lines across the entire array (1024 diodes) with a wavelength accuracy of 0.0206 nm.

Thus, unless a highly spatially unstable source is used, a polychromator with a linear dispersion could be generally expected to provide a minimum overall wavelength accuracy of 0.025 mm (diode width) × reciprocal linear dispersion (nm/mm).

VI. Noise Sources

There are many definitions for dynamic range when applied to optical multichannel spectroscopy, as will be discussed. Nevertheless, regardless of its definition, dynamic range is set by the ratio of the maximum signal level that the detection system can accommodate (without being overloaded) and its overall noise.

Thus, a discussion of dynamic range should be preceded by a discussion concerning both the noise sources in the system and other limiting factors.

A. Fixed Pattern

Each diode array has a characteristic fixed pattern (spectrum) that is caused by stray capacitive coupling of the transients arising from the clock driving signals to the video lines by external stray capacitances and by diode-to-diode dark charge variations. The level of this fixed pattern is typically 1% of full scale range, and it is easily digitally (computer) subtracted (Fig. 6). How-

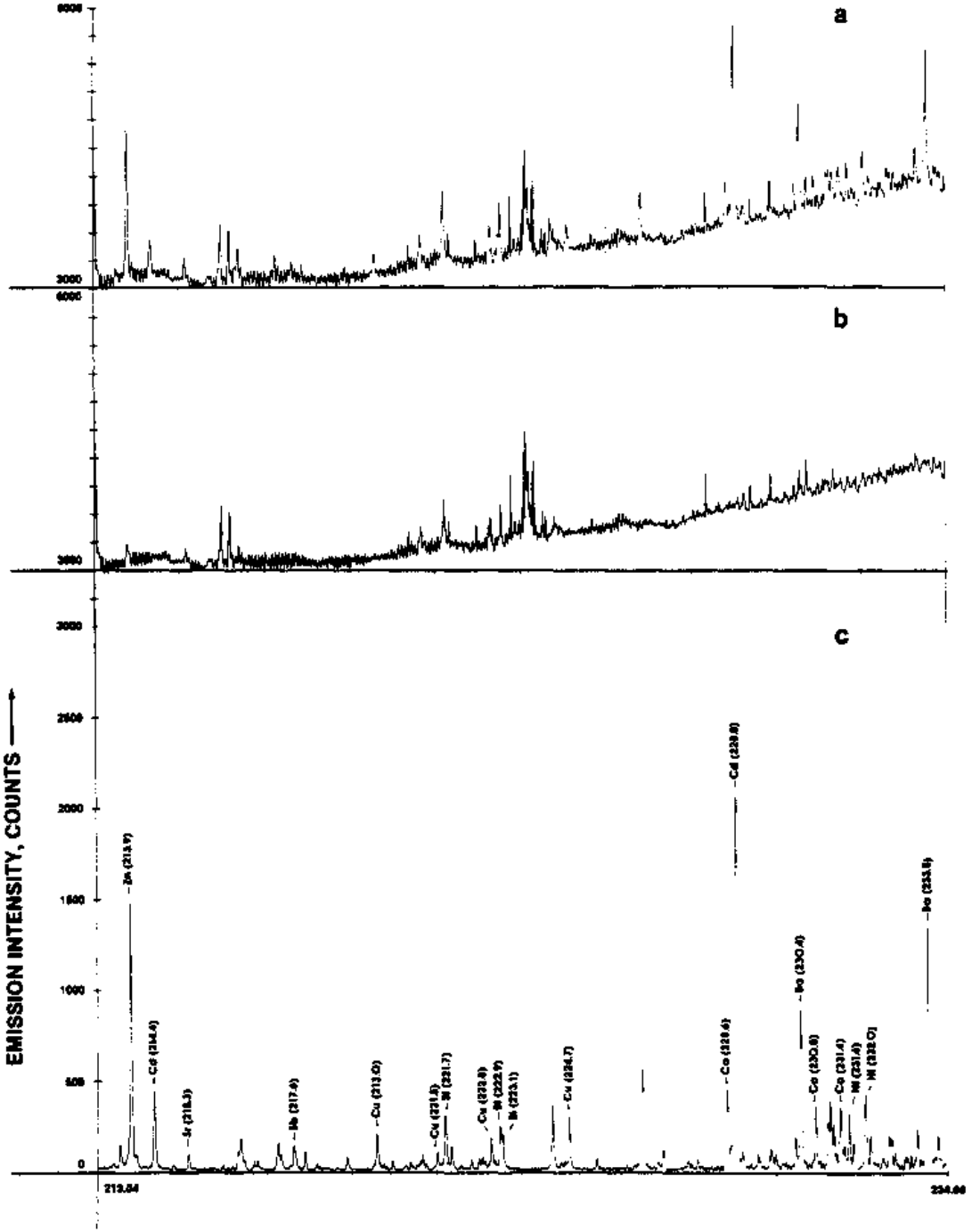


Fig. 6. Analysis of synthetic aqueous solution containing various elements at 40-μg/liter concentration range using induction coupled plasma excitation source: (a) spectrum of solution time 8 sec; (b) spectrum of distilled H_2O (background), integration time, 8 sec; (c) difference spectrum (a)–(b).

ever, although it is subtractable, any temporal variations in the fixed pattern increase the overall noise of the system.

The fixed pattern is temperature dependent and appears to have a 1/f (flicker noise) characteristic. Although the exact origin of the flicker noise has not been determined, it is suspected that it relates to flicker noise in the (MOS-FET) multiplex switches. The flicker noise limits the extent to which the SNR can be improved by in-memory digital averaging to approximately a factor of 10 in the present system.

B. Dark Current and Dark Current Shot Noise

All silicon image detectors are subject to thermally generated dark current and its associated statistical fluctuations (noise). The adverse effects of dark current on the overall performance of the diode array can take a few forms: (1) Dark current buildup can rapidly reduce the maximum signal limit by reducing the net signal-reading range of the ADC and, in long exposures, by competitively (with the photon generated signal) discharging the reverse-biased diodes. (2) Dark noise can become large enough to compromise the overall noise performance of the diode array. (3) Dark current fluctuations, caused by corresponding detector temperature fluctuations, can also contribute to the system's noise. All these effects, however, can be significantly reduced by cooling the array, since the dark current is halved for each 6.7°C reduction in temperature.

The dark current shot noise N_d in electrons is given by

$$N_d = \left(\frac{I_d t_i}{q_e}\right)^{1/2},$$

where I_d is the dark current, t_i the integration (exposure) time between consecutive readouts, and q_e is the electronic charge. At 25°C, the typical N_d value for an N-series diode array, after 1 sec of integration, is ~5600 electrons rms, but at −20°C it is only 545 electrons rms. Figure 7 shows t_i values at which the dark current becomes significant at various temperatures and illumination levels.

Clearly, as the light flux increases the dark current becomes less significant, and the integration time at which the sum of dark and light shot noise equals that of the preamplifier approaches the asymptote: $t_i = (N_r)/F$, where N_r is the readout noise, and F is the effective light flux in charges/sec, i.e., the light flux in photons/sec multiplied by the quantum efficiency.

Since the dark current is temperature dependent, fluctuations in the temperature of the detector cause proportional fluctuations in dark current. If the technique of digitized subtraction of a (stored) dark spectrum is used to remove the effects of dark current and fixed pattern, these temperature dependent fluctuations show up as low frequency noise. The higher the temperature of the sensor, the higher the effect of temperature fluctuations on dark current. Ideally, the fluctuations in dark current should be kept below the

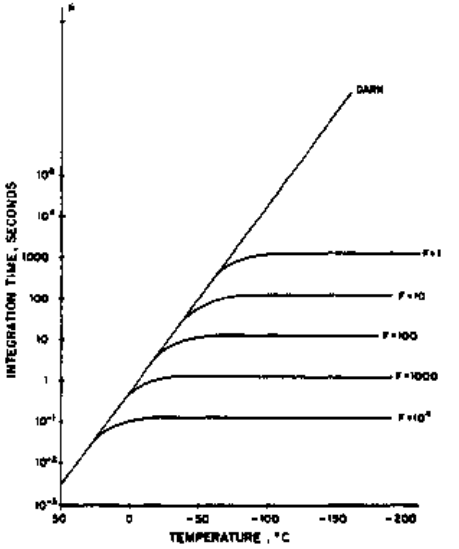


Fig. 7. Signal integration time at various temperatures and illumination levels (in charges) at which the combined dark current shot noise and signal shot noise are equal to preamplifier noise.

readout noise level of the sensor. To achieve that, the temperature fluctuations δT must not exceed

$$\delta T = \frac{6.7°\mathrm{C}N_r}{t_i I_d \ln 2} = 6.7N_r/(t_i I_{d0}(\ln 2) \exp(T/6.7 \ln 2),$$

where 6.7°C is the temperature increment that doubles the dark current level, I_d, N_r is the readout noise (at t_i = 16 msec), T is the sensor temperature (in °C), and I_{d0} is the dark current at 0°C. For an integration period of 15 sec, at T = −20°C, the dark current is 47 fA and if N_r = 1500 electrons = 2.4×10^{-16} coulomb, the necessary temperature stability is $\delta T = 3.3 \times 10^{-3}$ °C, clearly requiring high stability thermostating. Alternatively, the criterion for thermostat performance may be chosen as that degree of control that limits the uncertainty in dark current to a value no greater than that of the dark current shot noise. Now

$$\delta T = \frac{6.7}{\ln 2}\left(\frac{q_e}{I_d \cdot t_i}\right)^{1/2},$$

and for the conditions stated, $\delta T = 4.6 \times 10^{-3}$ °C. To achieve such a degree of thermostating, it is necessary to employ a closed loop thermostat with the highest possible loop gain that is consistent with stability considerations. The most convenient and controllable approach for moderate cooling, i.e., −25°C, is to use thermoelectric (Peltier effect) coolers. In using these coolers, it is essential that no noise be impressed on the cooler drive, since it can be transferred to the preamplifier by stray capacitance.

To avoid water condensation on the cooled detector's surface, the detector head assembly is kept at a moderate vacuum (~20–400 Torr). Typically, reevacuation is necessary every 2–4 weeks.

C. Thermodynamic Noise

Thermodynamic noise of SPD arrays is the result of the uncertainty in resetting the individual diodes during the readout process. This noise has been described[12] by $N_{th} = (1/q_e)[KT(2C_p + 2C_{cr})]^{1/2}$, where K is the Boltzmann constant, T the absolute temperature, C_p the diode capacitance, and C_{cr} the clock line-to-video line stray capacitance. At 25°C, N_{th} is ~1000 electrons rms for the 1024-element (S-series) diode array.

D. Preamplifier Noise

The preamplifier noise is given by $N_a = (1/q_e)[(i_n t_p)^2 + (e_n C)^2]^{1/2}$, where i_n is the preamplifier noise current referred to the input, e_n the preamplifier noise voltage referred to the input, t_p is the diode readout time, and C is the total capacitance at the amplifier input node, including that of the video line, amplifier input, and stray capacitances. With the proper choice of the input device and the circuit design, N_a can be reduced below the thermodynamic noise. The total readout noise N_r is given by $N_r = (N_a^2 + N_{th}^2)^{1/2}$.

VII. Dynamic Range

OIDs are designed, manufactured, and tested by electronic and optical engineers primarily for TV and other imaging applications. The jargon and definitions used to characterize the performance of these devices are, therefore, not aimed at or meant to be coherent to physical scientists. We, therefore, chose to begin this discussion by redefining dynamic range in terms that are both characteristic of parallel detectors and more meaningful to spectroscopists.

A. Simultaneous-Intraspectral Dynamic Range

This term is essentially the spectroscopic equivalent of the more familiar *intrascenic dynamic* range term used in imaging applications. It is defined as the ratio of the most intense and least intense spectral features that can be *simultaneously* detected within a *single* readout regardless of the length of integration time t_i between consecutive readouts. The apparent simplicity of this definition, however, can be very misleading, as our experience suggests. First, dynamic range does not automatically mean linear transfer characteristics (signal input to signal output relationship). In fact, often (particularly in imaging applications) a nonlinear transfer characteristic is preferred. Second, intrascenic dynamic range should not be confused with *single*-diode optoelectronic dynamic range, defined here as the ratio of the most and least intense spectral feature that can be detected by a single pixel or resolution element. This parameter, therefore, refers to the dynamic range of each *individual* diode and not to that of the *parallel* multichannel device as a whole. The main reason for the difference between the two terms is the *veiling glare* phenomenon, stray light in the detector enclosure due to internal reflections. Veiling glare is particularly severe with image-intensified detectors, primarily because of light transmitted through the semitransparent photocathode that is internally reflected by the glass and metallic internal components. A point-in-case is the image dissector, an imaging device with an optoelectronic dynamic range characteristic of PMTs, 10^6:1. The intrascenic dynamic range of this device, however, can be <1000:1 because of veiling glare. The intrascenic dynamic range of the SPD can also be limited by its dark current. Even with a 14-bit ADC, thermally generated (dark) charge buildup can seriously reduce the useful signal-reading range of the detection system. Figure 8 shows the integration time values t_i at which 20 and 100% of the ADC range and 100% of the

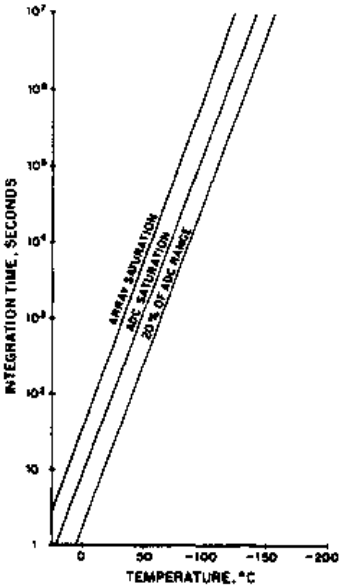


Fig. 8. Integration time values (at different temperatures) at which 20 and 100% of the ADC range and 100% of the diode charge storage (8.8×10^7) are wasted on dark current.

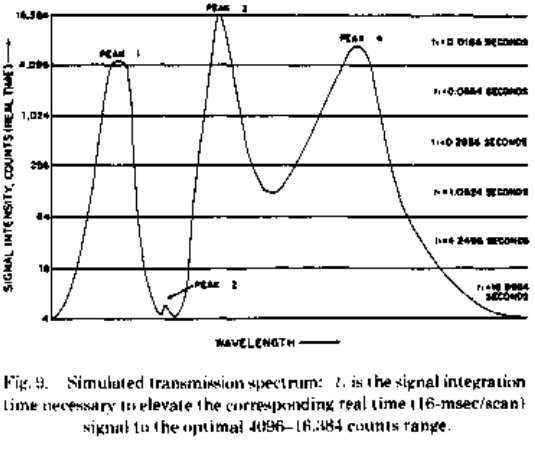
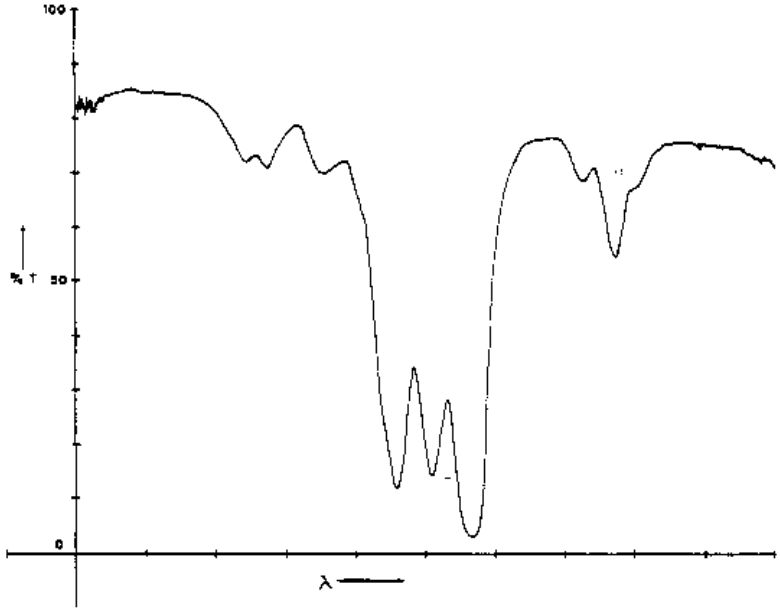
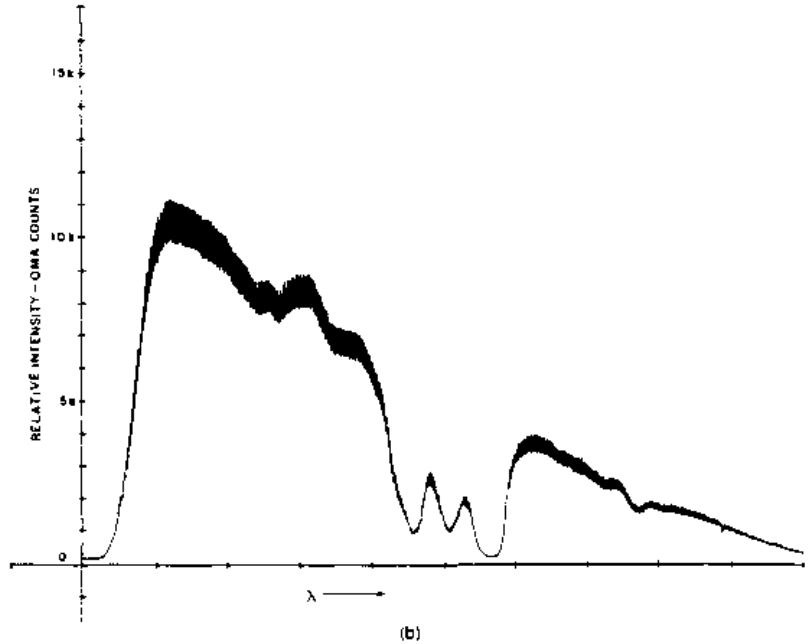


Fig. 9. Simulated transmission spectrum: t_i is the signal integration time necessary to elevate the corresponding real time (16-msec/scan) signal to the optimal 4096–16,384 counts range.



(a)

See caption on page 1410.



(b)

diode charge storage are utilized for parasitic dark charge readout at different temperatures. Furthermore, because of the relatively large diode-to-diode dark current variations, it is impossible to use simple electronic (signal-bias) clipping procedures to increase the useful range of the ADC. Nevertheless, integration periods of a few hours have been successfully accomplished at very low temperatures,[11] even though at the expense of reducing the detector's red response.

B. Accumulative (Memory) Dynamic Range

The useful dynamic range of the SPD can be enhanced by ensemble averaging, i.e., accumulation (superimposition) of consecutive digitized spectra (readouts) in the computer memory rather than on-target (integration). The OMA-2 has a memory dynamic range of 2.1×10^9 (2^{31}) counts. However, as previously stated, the experienced averaging advantage for long accumulation times has been somewhat lower than the theoretical value [square root of the number of consecutive (stored) readouts] because of $1/f$ type noise dominance.

C. Variable Integration Time (VIT)

This mode of operation is unique to energy detectors capable of signal integration. Different signal integration times are used for different regions of the spectrum, inversely proportional to their corresponding signal levels, to make maximum use of the available range of the ADC. The principles of operation of the VIT technique are demonstrated in Fig. 9. In this case, six exposures of the (simulated) spectrum are obtained at six integration time periods t_i (progressively increased by a factor of 4) and stored in memory. This procedure enables the elevation of each of the six (real-time) signal-level intervals to the same 4096–16,384-count measurement level, thus greatly improving the spectrometric accuracy and precision. However, a certain degree of signal deterioration can be expected due to dark charge buildup, localized (and limited) blooming, near- and far-field veiling glare, and spectrometer stray light. The transmission spectrum of a Ho-oxide filter (Fig. 10) demonstrates the low level interferences, due to blooming, characteristic of the SPD. This technique has proven more flexible and less susceptible to instrumental errors compared with other common constant energy (signal) techniques, e.g., slit width servo and automatic variable preamplifier gain.

To measure the dynamic range, the linearity and reciprocity (signal intensity × integration time) of the SPD, the following experiments were performed:

1. Calibration with Neutral Density (ND) Filters.

(a) The linearity (transfer characteristics with a γ value of 1) of the single-diode optoelectronic dynamic range was tested with precalibrated ND filters, whose precise values (to within <1%) were obtained independently with linear photon counters (PMT). Collimated beams from highly stabilized light sources passing through various spectral filters were used to measure the linearity at different wavelengths.

(b) The intrascenic dynamic range was measured with a neutral density wedge filter (Kodak, photographic step tablet 2) whose discrete optical density

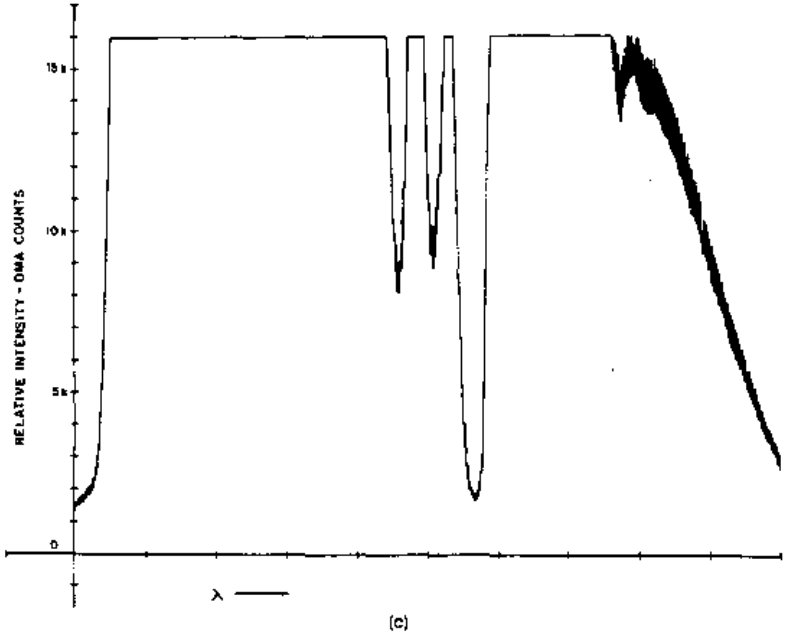


Fig. 10. Transmission spectrum of Ho-oxide filter. JACO (Mark X) polychromator was used with 600-g/mm (blazed at 300-nm) grating, 6 nm/diode (25 μm): (a) transmission spectrum, 183-msec signal integration; (b) transmitted spectrum, 183-msec signal integration; (c) same as (b) but 1.68 sec. Parts (a) and (b) are on page 1409.

(absorbance) steps vary from ~0.05 to 3.0. The incident and transmitted (I^0 and I_i) images of the wedge filter (backilluminated with an elongated fluorescent lamp) were focused with an 85-mm ($f/1.8$) lens onto the target of the SPD. These images along with the dark-pattern image D_i were used to produce the absorbance image.

$$A_i = \log\left(\frac{I_i^0 - D_i}{I_i - D_i}\right),$$

where i is the variable diode index (from 0 to 1023).

2. *Calibration with Pulsed LEDs.*

This experiment served two purposes: to verify Talbot's (law) behavior of SPD detectors and to determine their reciprocity. Talbot law in its modern version states that light fluctuating periodically is exactly equivalent to steady radiation of the same average value $R[F(t)] = R[\bar{F}]$, where $\bar{F} = \int |F(t)dt|/T$, $F(t)$ is the periodically fluctuating light, and R is the evoked response. LEDs (either with green or red spectral response) were used as the variable frequency chopped (pulsed) light sources. The pulse width was kept constant (always <3% duty factor), while varying the pulse frequency within the 0.1-Hz to 100-kHz range. Alternatively, both pulse width and pulse frequency were altered. In either case, control of pulse width, pulse frequency, and detector integration time determine the total photon energy incident on the SPD. The spectral output of the LED (a red shift was observed at high frequencies when the pulse width exceeded 3% of duty factor) was carefully monitored and maintained constant to within ±1 diode (0.14 nm). Pulse width and pulse frequency were measured with an accuracy better

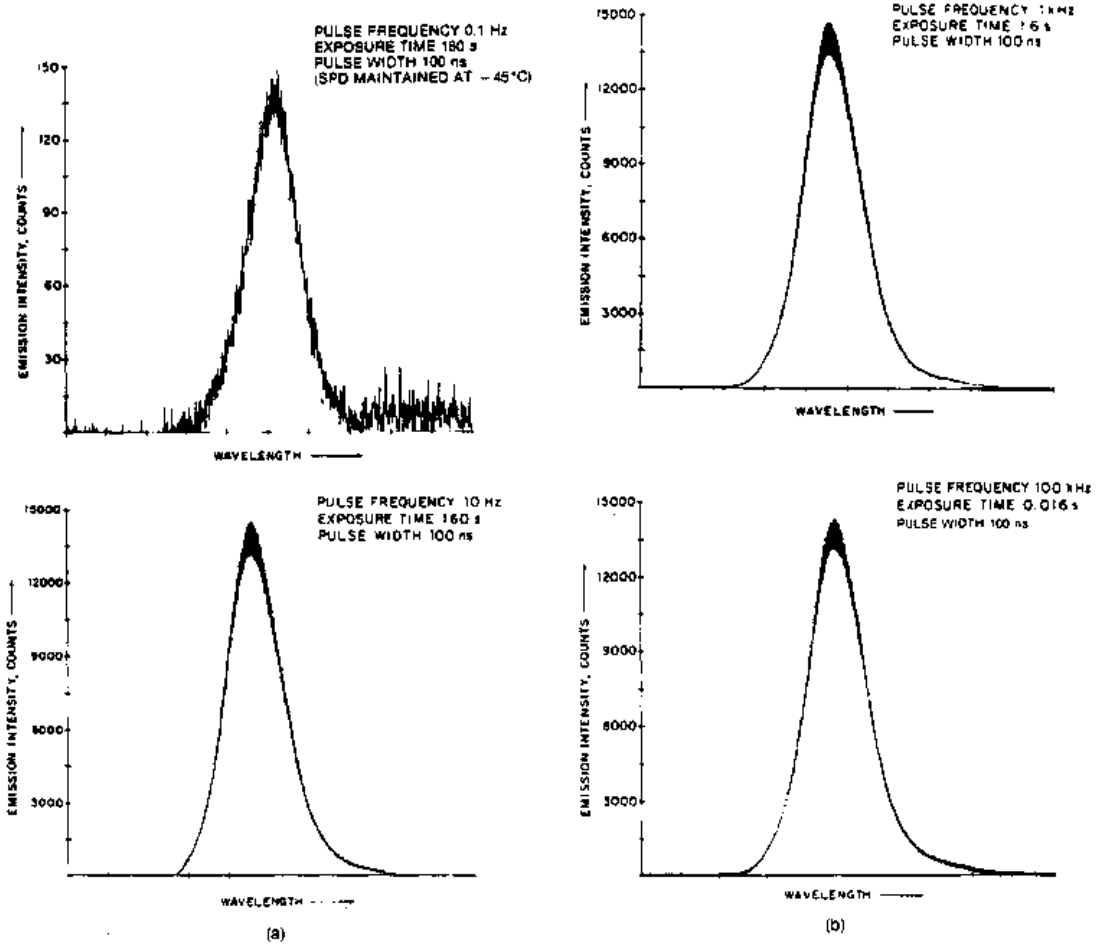


Fig. 11. Verification of reciprocity of photodiode array detector: signal intensity × signal integration = constant. Red-emitting LED was pulsed at frequencies varying from 0.1 Hz to 100 kHz.

than 1 and 3%, respectively. Verification of the reciprocity of the LED itself (0.1 Hz to 100 kHz) was achieved independently using EG&G-PARC photon counters.

VIII. Results and Discussion

The measured diode electrooptical dynamic range of the SPD was in good agreement with the 14-bit ADC limit of the detection system. This behavior was anticipated from the nonlaggy nature of the SPD and the relatively high saturation level of its individual diodes ($\simeq 10^5$ counts). The linearity within the 10^4:1 measured range was <1%. The reciprocity of the SPD (by pulsed LEDs) over a range of 10^6:1 was found to be linear to within <3% (the overall estimated accuracy of the measurement apparatus) (Fig. 11). Based on work done elsewhere,[10] it should be possible to stretch significantly the reciprocity range by further cooling the SPD.

More difficult to assess and less conclusive results (at the present time) were obtained for the intrascenic dynamic range. With the experimental setup utilized, stray light, primarily from the high transmittance steps of the wedge filter, was observed. Good linearity, step position vs step optical density, was obtained when a signal 0.1% the magnitude of the first transmission step was subtracted from all subsequent steps (2–21) (Fig. 12). This apparent far-field veiling glare (stray light) could have been caused by internal light reflections between the diode's silicon surface and the window of the SPD. However, most probably,[13] it is the result of glare in the focusing lens. Veiling glare in the detector itself should be reduced by

(1) removing the SPD's protective window, especially since the evacuated detector head has its own quartz window; and

(2) using the SPD with an optical-fiber (coupler) faceplate window, eliminating window-to-target light reflections.

Recent experiments[13] have shown the veiling glare level to be lower than the stray light level of various short focal-length (0.2–0.5-m) polychromators typically used in conjunction with OMA detectors.

IX. Resolution and Spectral Information Transfer

The architectural structure of the RL-1024S detector was discussed previously. The device comprises 1024 discrete photodiodes with a 25-μm center-to-center separation, each 2.5 mm high. The 100:1 aspect ratio of the diodes is an excellent design compromise aimed at matching the profile of a typical spectrometer slit. Based on those data, the spectral resolution of the diode

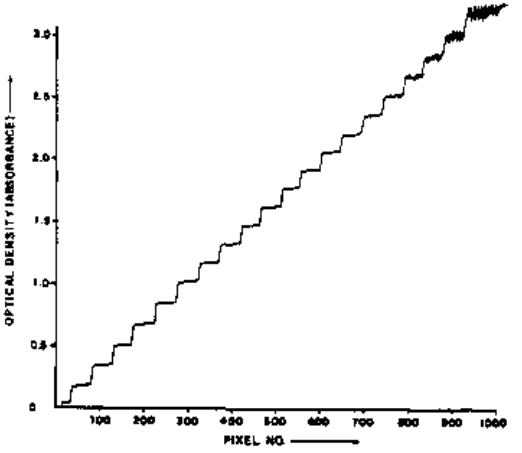


Fig. 12. Linear ($\gamma = 1$) behavior of the intrascenic dynamic range of the SPD. All 21 steps of a Kodak (density) wedge filter are clearly recognized. Raw data were computer compensated for the 0.1% observed stray light (mostly from the camera lens).

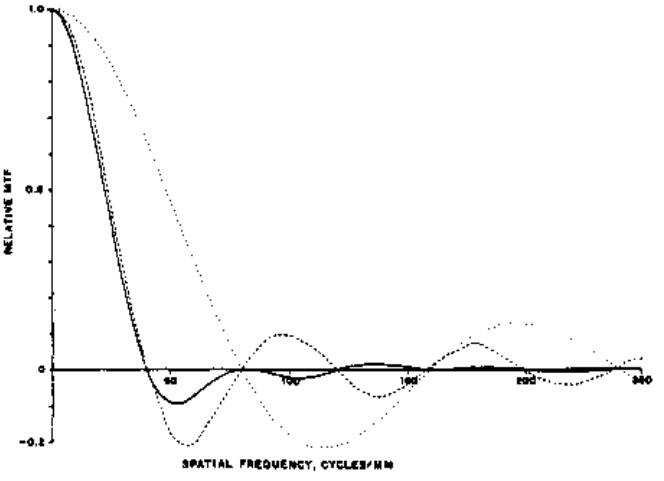


Fig. 13. MTF of the S-series (solid curve), array with a 25-μm pitch and rectangular 25-μm wide pixel (dashed curve), and array with 12.5-μm wide pixels at 25-μm pitch (dotted curve).

array is often erroneously defined as its diode spectral bandwidth, 0.025 mm × reciprocal dispersion (nm/mm) of the spectrometer. Actually, the spatial response profile of the photodiode array along the array axis is trapezoidal rather than rectangular[14] (Fig. 2). Therefore, although the diodes are discrete, their spectral (or imaging) information transfer shows a partial overlap. This overlap leads to a substantial reduction in aliasing with only a slight reduction in resolution. Figure 13 compares the modulation transfer function (MTF) of the RL-1024S diode array with a 25-μm diode width and pitch to that of two other theoretical arrays (CCDs) with a rectangular response pixel profile, one with a 25-μm pixel width and pitch and the other with a 12.5-μm width and a 25-μm pitch (similar to Fairchild's 488 × 380 area array CCD). Clearly, the last two arrays, particularly the second, have higher MTF values beyond the Nyquist criterion limit and are therefore subject to severe response aliasing.

Aliasing can cause severe interpretation errors when spectra with periodic line structures, e.g., molecular vibronic spectra, are measured, as shown in Fig. 14, for the SPD and the second theoretical (CCD) array. The aliasing detector can falsely increase the apparent periodic wavelength-separation (intervals) between the lines well above the real value (resulting in a lower apparent spatial resolution). Even more serious are the potential errors associated with arrays with dead spaces (second theoretical array) between the pixels. A narrow spectral line could fall on a dead space instead of on the pixel and therefore be severely attenuated, or worse, undetected (Fig. 15).

Finally, although the physical overlap of adjacent diodes causes a certain degree of information cross talk, the spectral resolution of the SPD is practically limited by the spectral dispersion system utilized (Fig. 16).

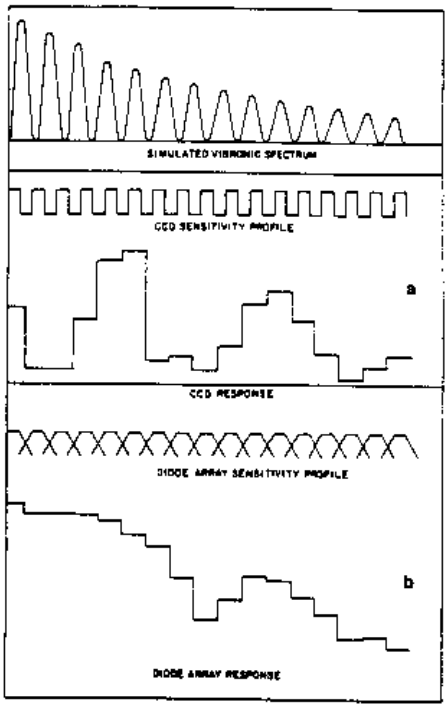


Fig. 15. Distortion of spectral line using CCD array with identical pixel width and pitch and SPD: (a) peak maximum out-of-phase with the sensitivity profile of the detector; (b) peak maximum is in-phase.

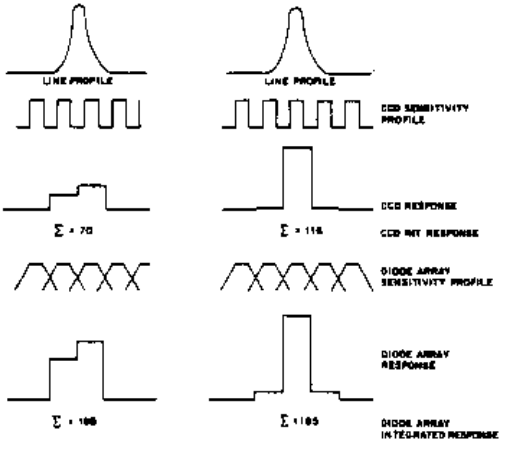


Fig. 14. Distortion of simulated vibronic spectrum caused by detector aliasing using (a) CCD array with identical pixel pitch and (b) SPD (more accurately preserving the spectral record).

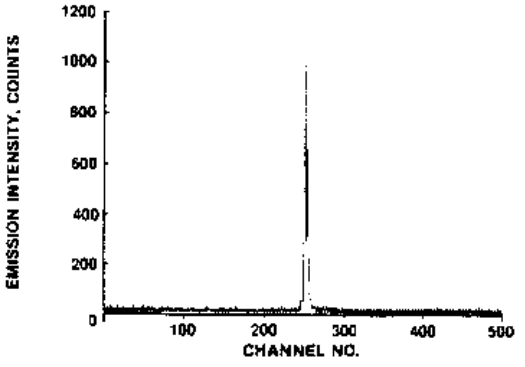


Fig. 16. Spectral profile of the beryllium doublet. (JACO model 75-150 a 1-m spectrograph with 590-g/mm (250-nm blazed) grating produced spectral bandwidth of ~0.0206 nm/diode (25 μm). Induction coupled plasma was used as the excitation source (1 μg/liter beryllium solution was used).

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A need and method for nonuniformity correction in solid state image sensor

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Abstract

When the solid state image devices were introduced into the optical industry, they revolutionized the techniques for image detection, but not without the user tolerating its nonuniformity. This nonuniformity anomaly is usually ignored in many optical imaging applications; accordingly, its existence and effects are known only by a few among the device implementors. In some applications, this anomaly may seriously impair a system design; consequently, the unwary should be informed of its existence. The nonuniformity can be induced electrically and/or optically into a video signal's transmission path, and in turn it produces an arbitrary gray scale on an image space, derived from a uniformly exposed target. This paper defines the nonuniformity in relation to the solid state imaging devices, demonstrates the need to compensate it in low-contrast image application, and discusses an inexpensive network to perform the compensation and the results of its implementation.

Introduction

The solid state imaging devices [1,2], otherwise known as mosaic devices[3], have substantially broadened and enhanced many applications in the field of optics, but not without the user tolerating its nonuniformity.

The importance of the nonuniformity and its correction lies in enhancing the signal-to-noise ratio especially in low-contrast signal detection. In most applications, this nonuniformity is neglected, but in some, it can obscure the image signal and render the sensor's detectability useless. The sketch in figure 1 exemplifies the process of the

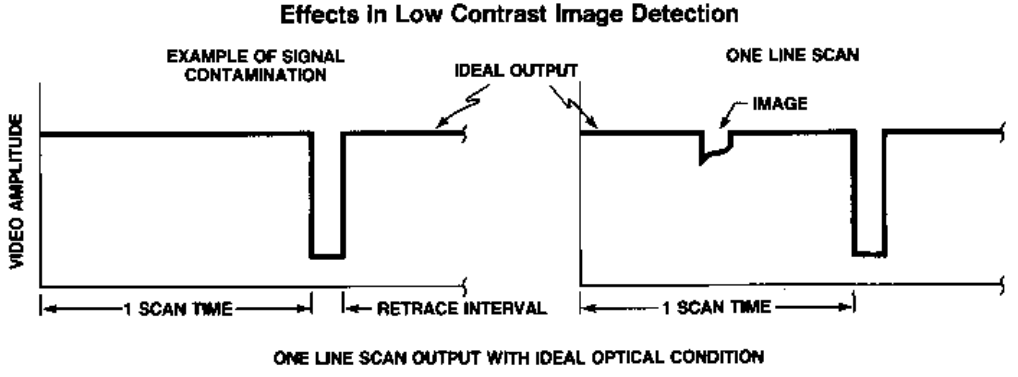


Figure 1a

signal-to-noise degradation with a single scan of the video signal as it could be seen on the scope trace. Figure 1a shows the image signal while figure 1b shows the same signal obscured in the nonuniformity noise. Furthermore, its correction should generally be desired, because the state of the art makes it difficult to design a device with ideal uniformity, i.e., the nonuniformity inherently exists in all present day solid state imaging devices on the market.

This paper defines nonuniformity in relationship to the image devices, discusses its effects on the optical signals and presents a method for its compensation. In addition, the discussion includes a related nonuniformity effect which is found in most optical paths. The nonuniformity is characteristically similar to those existing in the devices, and in most applications, they coexist.

Of the two major organizations of image devices, the line scan and matrix array, the discussion will be based on the line scan array. The distinction between them is that the line scan array has all the photo sensing cells aligned in a single row, whereas the 2 dimensional matrix arrays are arranged in rows and columns. However, they are similar enough that the line scan discussion will suffice for both.

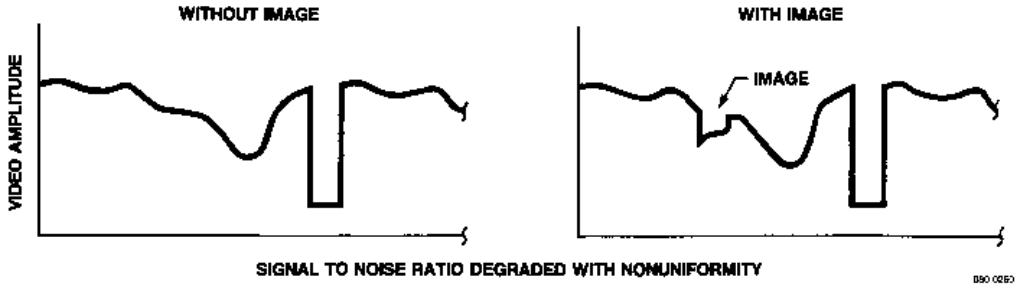


Figure 1b

Definition and Characteristic of Nonuniformity

Nonuniformity is the variation in the video pixels from an array whose photo cells are illuminated with equal exposure. It is expressed in plus or minus percent deviations from the average level, where the average is the sum of the maximum and minimum pixels divided by two.

Nonuniformity causes the slope of each cell's conversion transfer function to differ among one another. Accordingly, when each photo cell is illuminated with equal exposure, the output pixels will vary in proportion to the transfer slope, in other words, its gain.

Hypothetical Array with Three Photo Site

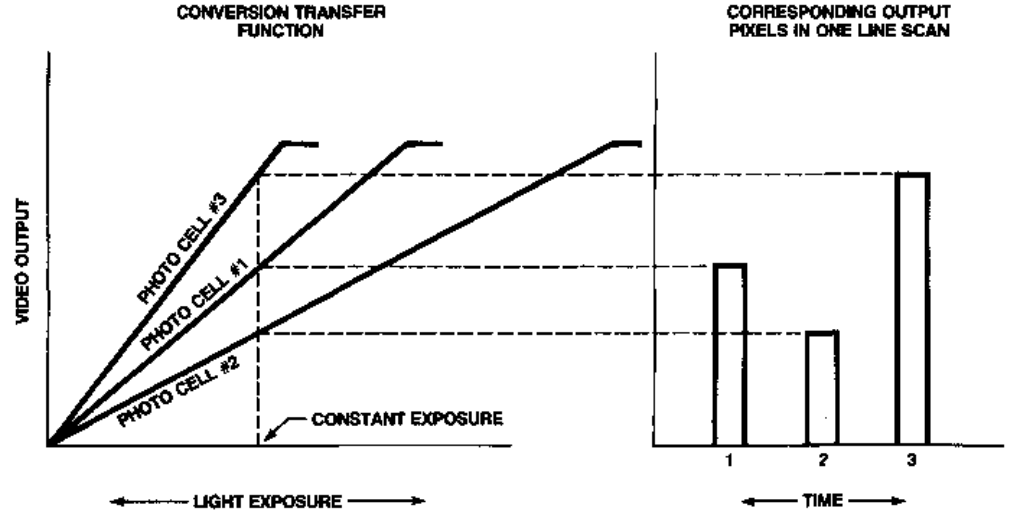


Figure 2

Figure 2 illustrates this gain difference with a 3-photo-cell hypothetical line array. Consistent with the slope changes, the nonuniformity of the array can be compensated by changing each cell's gain with an output circuit and making the gain of each cell equal.

The intercept point of the transfer function was ignored because nonuniformity is discussed in light of the low-contrast signal-to-noise ratio enhancement, whereas, the intercept point is related to low-light signal processing. The intercept point is a measure of the offset levels of each pixel with no illumination. These variations, known as fix-pattern noise", FPN, are usually less than 1% and in some devices less than 0.1% of the maximum output at saturation exposure. Hence, if these variations are compared to nonuniformity of ±10% at 50% saturation exposure, such as in case of low contrast signal with high background exposure, FPN can be ignored.

A Compensation Technique

There are many slope correction techniques employed in the industry. They employ a variety of circuits, i.e., digital, analog or the combination of the two, but most are based on an old established algorithm, that is used in automatic gain control and voltage regulator circuits. In its simplest form, the correction takes place within a closed loop feedback network with a multiplier as its variable gain element. This loop will hold a constant output as the input voltage is varied. Figure 3 shows the feedback network.

Simplified AGC Loop all Filters for Base Band Signal Process is Ignored

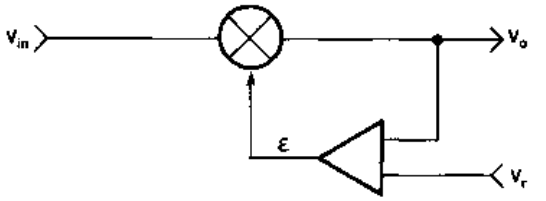


Figure 3

Briefly described as the input, V_{in}, is varied, the loop maintains the output very close to the reference, V_r, because an error, ε, develops as the absolute difference between V_o and V_r and changes the multiplier coefficient to reduce this difference. This correction algorithm is used in the compensation network presented in this paper.

The correction requires a two step operation, one is the write mode and the other the read mode. The write mode stores the multiplying coefficients by the following process. The array is first exposed under uniform illumination, then each pixel is processed through the loop and forced to a constant level. As the loop corrects each pixel, its corresponding multiplying correction factor, MCF, proportional to ε, is stored in memory. These stored factors are then used to correct the multiplier gain in the read mode.

The read mode is the normal imaging process where the array produces the pixels proportional to the image exposed on the array. As each pixel is passed through the multiplier, each corresponding MCF stored in memory is read out and multiplied with the pixel. The pixel multiplication with the MCF corrects the cell's transfer gain to produce nonuniformity corrected pixels. Figure 4 is a block diagram that illustrates both of the above described processes. Figure 4a is the system reading in the MCF, while the system is illuminated under a constant exposure. Figure 4b is the system in its normal imaging operation with its nonuniformity corrected.

This process of controlling each cell's gain to equal all others, not only corrects the nonuniformity caused by the imaging devices, but it can correct those optical gain variations induced by the optical path. The optical correction follows from the slope correction if the intensity variation is caused by a constant attenuation factor in the transmission path. An example is the shading caused by limited aperture width, dust particles on lens, etc. Since the undesired shadings, to the first order, effect the transfer gain of each spatial point on the object line or plane to the image line or plane, the shading correction can also be simultaneously corrected with the imaging device. The correction to include shading is performed with the same two step operation.

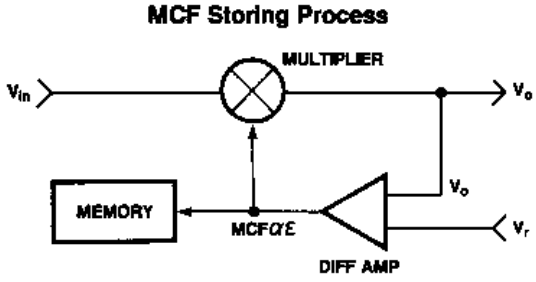


Figure 4a

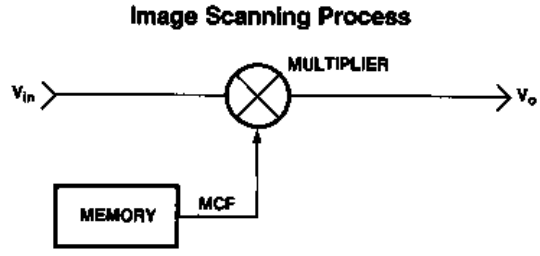


Figure 4b

The only difference is that a uniformly reflecting target is placed in the object plane of the optical system when the system is in the write mode.

Implementation Design Method

In the discussion of the compensation design method, the following definition will be used to describe the compensation performance.

The Uniformity Correction Factor, UCF, is defined as the ratio of nonuniformity before correction over the residue nonuniformity left after correction, i.e., when a device with nonuniformity equal to ±10% is corrected to ±1%, it will have UCF = 10.

The Correcting Range, CR, is defined as the maximum range over which the system will correct the nonuniformity, i.e., in a system where nonuniformity is ±15%, a CR ≅ 30% will sufficiently cover the range to compensate the nonuniformity whereas CR<30% will not.

The limits of CR and UCF are predicted by parameters of the closed loop transfer function of figure 3, and constrained by the dynamic range of circuit, which is usually determined by its components.

The two parameters of concern are the closed loop gain, G, and the error, ε, because 1) G determines the limits of CR, and 2) the error, ε, determines the limits of UCF, because the final maximum residual value of ε after compensation, over the reference voltage is the corrected value of the nonuniformity.

The closed loop gain of the block diagram in figure 3 is

$$G = \frac{V_r K}{V_{in} K - 1}$$

where V_r is the reference voltage
V_{in} is the output voltage
K is the open loop gain

This simple relationship shows, if $KV_{in} > 1$, then G approaches

$$G = \frac{V_r}{V_{in}},$$

hence, the output approaches $V_o = V_r$. Furthermore, they show that the maximum limits imposed on CR are boundless, i.e., maximum value of V_{in} is boundless, and its minimum value is determined by $V_{in}K > 1$.

The error, ε, approaches

$$\varepsilon = \frac{V_r}{V_{in} K} \quad \text{if } V_{in} K \gg 1,$$

thus, by making $\frac{V_r}{V_{in}} \ll K$, ε can be made arbitrarily small. Again, the limits on ε, hence UCF, that are imposed by these relationships are boundless. Accordingly, limits on both CR and UCF are set by the type of circuit and its parameter and components.

Circuit Implementation

To minimize the real estate of a full digital implementation and to retain a relatively high video sampling rate, a system incorporating both analog and digital circuits was implemented. The video signal was kept in its discrete time analog samples, while the MCF, proportional to the error, was converted to digital signals and stored in memory.

Figure 5 shows a block diagram of this implementation. The similarities to the circuit

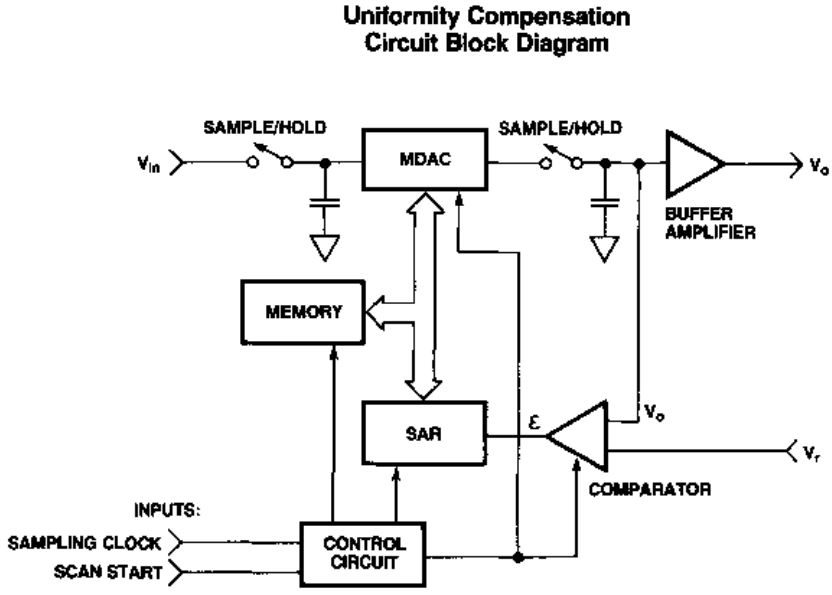


Figure 5

in figure 4 and its operation are readily apparent. In place of the multiplier is a multiplying digital to analog converter, MDAC. The chief advantage of this configuration is the signal pixels remaining in analog format, hence, analog to digital and digital to analog conversions are not required. Since MCF is conveniently converted and stored in digital format, the error and its control circuits were digitally implemented. The MDAC is simply a multiplier for the analog signal which is multiplied with a digital multiplying coefficient. The error for each pixel is converted to a digital MCF by the combined operation of the comparator and the successive approximation register, SAR. The output signal is compared to a reference voltage at the input of the comparator. Then the comparator produces a single bit, its polarity depends on the output signal level relative to the reference voltage. Each bit is successively processed by the SAR which produces the digital MCF proportional to ε. The MCF in turn changes the gain of the MDAC until the output voltage approaches the reference voltage within the limit of error, ε. This limit value determines the value of MCF which is stored in memory.

In the implementation, the gain factor was set to 512, because an 8 bit MDAC was set with a maximum gain of 2.0. Then the lowest gain will be $\frac{2}{256} = 7.81\times10^{-3}$, but as it is readily evident from table 1, below, this low gain is unusable.

V_{in}	Gain	Error
3 volt	0.334	6.5×10^{-4}
2 volt	0.5	9.78×10^{-4}
1 volt	1.0	1.96×10^{-3}
0.5 volt	2.01	3.92×10^{-3}
0.3 volt	3.36	6.55×10^{-3}

Table 1

The table was calculated using the previously discussed relationships with K = 512 and V_r = 1. The maximum gain is 2.0 and the maximum input signal V_{in} is 3 volts. As a result, the maximum correcting voltage range is 0.5 to 3.0 volts or CR = ±0.71. Then the minimum residual nonuniformity is $\pm \frac{\text{maximum } \varepsilon}{V_r}$ = ±0.0039 or ±0.39%.

As described in conjunction with figure 4, after the MCF has been stored and the compensation circuit is switched into its normal image scanning mode, the memory sequentially produces the MCF to change the gain of the MDAC for each MCF's corresponding pixel. During this read mode, the rest of the circuit remains inactive. An advantage with the memory used in this configuration lies in a large volume application, where an image device along with its optical system is compensated together. The MCF could be preprogrammed into a read-only memory and provided with the system, thus eliminating the need for the SAR, comparator, control circuits, etc. and reducing not only complexity but cost as well.

Experimental Measurements

A nonuniformity compensation circuit was constructed in accordance with the block diagram of figure 5. It was constructed to compensate EG&G Reticon's RL1728H scanning diode array[5]. The array operated in a circuit identical to the RC1728 L/N peripheral board[6]. A uniform light source was placed over the array. To exaggerate the nonuniformity, a piece of transparent tape was placed between the light source and the array. The array was set to sample at 1 MHz while the exposure integration time was set to approximately 2 milliseconds. The MCF was sampled into the memory by advancing one pixel for each scan, starting with the first until all 1728 pixels' MCF were stored. Figure 6 is a scope

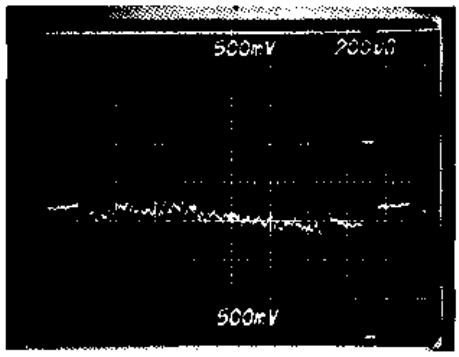


Figure 6. A compensated vs. uncompensated video output of a signal line scan.

photograph of two outputs. Each is a full line scan of the 1728 diodes. The top trace is the output after the uniformity compensation and the bottom trace is the uncompensated output. Each line scan is approximately 8.5 divisions and is seen terminated with the end of line, EOL. The vertical sensitivity of the top trace is uncalibrated and is adjusted to display equal amplitude so that the two traces can be easily compared. Clearly, this photograph shows, at least qualitatively, the improvements in the compensated over the uncompensated video outputs.

To demonstrate the importance and the need for uniformity compensation in low-contrast detection, a piece of wire was placed in the optical path. The output of this image is shown in figure 7. The image signal-to-noise enhancement is in excess of 20 db. The bottom trace shows the target buried in noise whereas the top trace clearly shows the target.

To demonstrate nonuniformity correction in the optical path, a narrow aperture lens was mounted before the array and focused on a uniformly reflecting object plane. The limited aperture causes gradual reduction in the exposure as the array ends are approached, and produces a bending video scan line. This bending scan line is shown in the top trace of figure 8, while the bottom trace shows the compensated output which is free of the nonuniformity caused by the lens. Again, a target was placed in the object plane to demonstrate the enhancement of the signal-to-noise ratio. Figure 9 is a photograph of the same traces as shown in figure 8, except that the sensitivity of the scope was increased to emphasize the improvements in nonuniformity correction and to show its values in low-contrast detection. In this particular case, if a simple level detector was employed, the target could not be detected unless the signal is corrected.

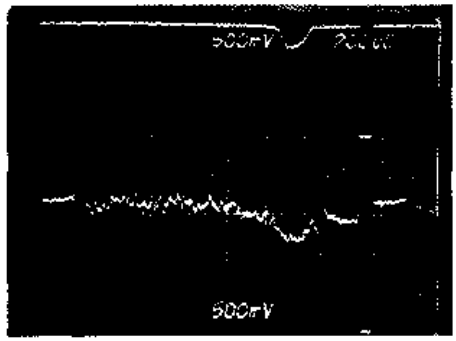


Figure 7. Video output comparison with a target in the optical path.

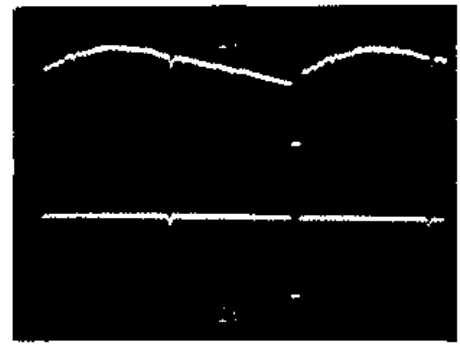


Figure 8. Nonuniformity caused by limited aperture.

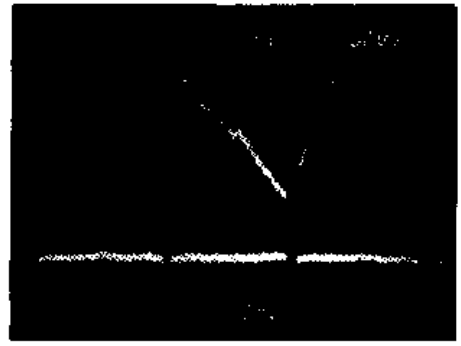


Figure 9. Higher sensitivity trace of figure 8.

Performance measurements showed that the nonuniformity of the corrected output was approximately ±1%; hence, the exaggerated nonuniformity of ±30% in the figure 7 has a UCF equal to 30. Measurements of CR showed slightly greater than ±30%.

Discrepancy Discussion

The theoretical limit for the corrected nonuniformity is ±0.39%. The discrepancy between the measured value of ±1% and the ±0.39% is caused by two factors with cumulative effects, 1) the FPN and 2) the tangential-thermal noise produced by the circuit components. Together, they produce noise variations of approximately 10 mv. With the reference equal to 1 volt, the noise limited corrected nonuniformity will be ±1%.

The discrepancy between the theoretical CR = 71% to the measured value, which is slightly greater than 60%, is caused by the limited V_{in}. The output of the array board is the input voltage to the compensation board; however, instead of anticipated 3 volts maximum, the board produced an output slightly greater than 2 volts.

Conclusion

In light of the low-contrast signals, this paper has 1) discussed the nonuniformities' effects on degrading the signal-to-noise ratio, 2) demonstrated the degradation and the need for restoring the signal-to-noise, and 3) suggested a method for its correction.

Using the suggested correction circuit, measurements were conducted with a 1728 element imaging device. These measurements have shown the effectiveness of the uniformity compensation network in restoring the degraded signal-to-noise ratio with an example of an image

signal buried in nonuniformity noise.

Furthermore, a limited-aperture optical system was measured. This measurement showed the nonuniformity, caused by the limited aperture, reduced the detectability of the image signal in a manner analogous to the image device. As a consequence, the same compensation network removed this nonuniformity and restored the image's detectability.

In low-contrast detection, nonuniformity correctors are not only needed for image array, but for some optically induced non-uniformities as well, especially in applications where a large number of gray levels must be detected.

Acknowledgments

The author wishes to express his gratitude to Bob Maddoux for constructing and testing the Compensation Board, and EG&G Reticon Corp. for their permission and for the use of their resources to write this paper.

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Glossary

Active Area

Active area is the effective light-energy collection area in the neighborhood of any given photodiode or photosite. The captured photons are converted to charge and stored in the photosite storage area until they are accessed. This area is a function of device geometry wavelength.

Blooming

Blooming occurs when the incident light and/or integration time causes an excessive charge build up; this results in spill over into either the video lines or the adjacent elements.

CCPD (Charge Coupled Photodiode Device)

A CCPD is a solid state integrated device, which is made in two parts: an array of photodiodes and a Charge Coupled Device, CCD. The CCD is a well-known analog discrete time delay line which stores and passes charges in a form similar to a long "bucket brigade"; hence, it acts to transport the charge representing image signals. The charge packets generated by each diode are simultaneously transferred into the CCD register, then they are sequentially clocked out.

Dark Signal

Dark signal is the output signal in the absence of light; it is comprised of the following:

(1) Integrated dark leakage current
(2) Fixed pattern noise
(3) The thermodynamic noise

Data Rate

The data rate is the frequency at which pixels are being clocked out of the camera or array.

Dynamic Range

There are two common methods of determining dynamic range:

RMS single pixel: This is where the output from each pixel is individually considered and its dynamic range is the output at saturation divided by the RMS noise on that pixel. A fair approximation of the RMS noise on a single pixel can be determined by measuring the P-P random jitter and dividing by 4 to 6. This type of dynamic range applies to applications requiring high quality imaging such as aerial reconnaissance, graphic arts, spectroscopy, etc., and where the ability of a computer exists to massage out the effects of both nonuniform sensitivity and fixed pattern noise. The RC1024S evaluation circuit is specified in this manner, 10000:1.

P-P across the array: This is sometimes referred to as machine-readable dynamic range that could be obtained with a simple comparator. This can be defined in two ways depending on the particular video processing circuit used: (1) for a simple current amplifier (Reticon recharge circuits), the average saturation value divided by the peak value of the switching transients; (2) for a sample-and-held or resettable integrator waveform, the dynamic range is the average saturation value divided by the P-P dark fixed pattern including any nonuniformity of fixed pattern by excluding diode leakage.

Fixed Pattern Noise (FPN)

FPN is a pixel output pattern in the dark that is the same from scan to scan under fixed conditions. The output may be a periodic 1, 2 or 1, 2, 3, 4 pattern, a random high or low single pixel or group of pixels along the scan output, a low frequency cyclic variation, a positive or negative ramping along the scan or any combination of the aforementioned patterns.

The 1, 2 or 1, 2, 3, 4 pattern is due to the fact that alternate diodes are sampled on different clock phases. This type of FPN is dependent on clock rise and fall times and on circuit layout. The major source of the FPN is the capacitance between the access switches and the video line. As the nth access switch is turning off, the (n+1)st access switch is turning on; thus as one drives a charge into the video line, the other is removing a charge. If both the coupling capacitances between the switches and the video line and the voltage excursions of the switches are the same, then the net charge remaining on the video line is zero. However, if one is looking at current, then any lack of absolute coincidence of the two switch edges in time or shape will result in a switching transient in the output video.

The other mentioned type of FPN can be caused by process variations, contamination, and other such miscellaneous factors.

Frame Rate

Frame rate is the total number of frames from frame start to frame start within a given period of time. The frame rate is equal to the reciprocal of the frame integration time, provided the frame has not been reset between starts.

Frame Reset

Frame reset implies that the entire frame of elements has been reset to a zero charge. The release of the frame reset signal indicates the start of integration of the entire frame simultaneously.

Frame Storage

Frame storage is analogous to the storage mode employed in a RAM device (Random Access Memory). The whole frame video information is stored in a capacitive memory cell as charge which is proportional to the photon energy impinging in the neighborhood of the photodiode. The differences between the RAM and Image Device are: (1) the image device stores the photo integrated charge in analog while the RAM stores charge in digital or ones and zeros; and (2) the RAMs are randomly accessed while frame-type image sensors to date have all been accessed mostly sequentially.

Gray Scale

Gray scale is a measure of the intensity levels of the impinging light source. In most cases, the term is defined relative to the number of resolvable bits of A/D resolution.

Integrated Dark Leakage Current

The dark leakage current is the output signal in the dark which may vary from element to element but is typically 1% of the saturated output at 25°C and 40 ms integration time. It is caused by thermally generated electrons and can be decreased by a factor of two for each 7°C of cooling.

Integration Time

Integration time is the time interval between diode accesses for a given diode. Hence, in a sequentially scanned diode array, the integration time is the interval between the scan initiation or the start pulses.

Line Reset

Line reset is the condition in which all of the elements are reset to a zero integration and held at zero integration until the reset line is released. When the line reset line is released, integration will start.

Line Transfer

The term is operationally defined for the CCPD. The photo converted charges in a line of photodiode arrays are simultaneously transferred into their respective storage locations of a CCD register, which then sequentially transports the charges out of the array.

Nonburning Sensors

The term nonburning sensors implies the immunity that the solid state image devices have against damage caused by high light exposure. In contrast, a vidicon's phosphors are easily damaged under high light exposure. A photodiode solid state sensor will withstand several orders of magnitude of incident radiation over its saturation exposure.

Nonuniformity of Sensitivity

Sensitivity nonuniformity is defined as the differences of photodiode sensitivity along the array when illuminated with a uniform specified light source. It is measured at approximately 50% of saturation and is specified as a ± percentage obtained by dividing the differences of the most and least sensitive elements by the average value of diodes along the array. Check the specific data sheet for light source requirements and diodes ignored. For some older arrays, the measurement conditions are the same except that the formula is:

$$\frac{\text{Highest diode - Lowest}}{\text{Highest diode + Lowest}}$$

Both give comparable results.

Sample-and-Hold

This term is used in signal processing systems. Operationally and ideally, the sampling switch samples a signal voltage or current and stores its value or magnitude at the instant when the switch closes and opens.

Saturation

Saturation occurs when increasing the exposure (watt-sec) of the array does not increase usable output.

Saturation Charge

Saturation charge is the charge output of a given photodiode at saturation. This is usually specified for a given bias, typically 5V.

Saturation Exposure

The exposure (light intensity x integration time) level that produces a saturation output charge is the saturation exposure. The light wavelength distribution must be specified for a meaningful value.

Scan Rate

Scan rate is the total number of scans from scan start to scan start within a given period of time. Example: 500 scans per second. The scan rate can also be considered as the reciprocal of the integration time.

Sensitivity

The photo current (amps) flowing in a diode per unit of light intensity or irradiance (watt/cm^2). The units of sensitivity are amps/watt/cm^2 or coul/joule/cm^2. The wavelength distribution of the light source must be specified in order for a sensitivity specification to be meaningful (reference Application Note 121).

Spectral Response

Spectral response is the normalized output of an image diode response as a function of wavelength or frequency of the light exposure. Usually, the response is normalized to the output at the most responsive wavelength.

Stored Charged Mode (SCM)

In simplified operational definition, the photodiode is viewed as a simple storage capacitor and a current generator. The photodiode produces current in proportion to the incident photo energy in the neighborhood of the diode. The current is collected or stored on the capacitor. Then the charge is read from the photodiode after a given integration time. (The capacitor is really the photodiodes junction capacitance.)

Thermodynamic Noise

Thermodynamic noise is the random, nonrepetitive fluctuations which are superimposed on the dark level. This is the ultimate limiting noise which cannot be removed by signal processing.

Transfer Function

Transfer function is the term used to describe the optical conversion from light exposure to the video signal output for a given photo element, i.e., the ratio of output signal relative to the light exposure. The output is usually described as charge, but it can be described in volts or amps.

Dice Policy

1.	**Testing**	- 100% are tested for electrical functionality
2.	**Visual**	- 100% visual inspection
3.	**Metallization**	- Aluminum with nominal thickness of 10,000 angstroms
4.	**Backing**	- Gold, nominally 2,000 angstroms thick
5.	**Passivation**	- Phosphorus silicate glass
6.	**Mechanical Information**	- Die thickness - 20 ±1 mil (525 ±25 µm) - Bond Pad Size - 5 x 5 mils typical
7.	**Packaging**	- Antistatic waffle pack
8.	**Storage**	- A dry nitrogen atmosphere is recommended, particularly for compression gold ball bonding applications. Thermosonic aluminum wire bonding is recommended.
9.	**Handling**	- All standard procedures for handling and assembling MOS dice should be observed.
10.	**Ordering Information**	- Minimum order and/or release quantity is 500 pieces.
11.	**Warranty**	- THE FOLLOWING ARE IN LIEU OF ALL WARRANTIES, EXPRESS, IMPLIED OR STATUTORY, INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTY OF MERCHANT ABILITY OR FITNESS FOR A PARTICULAR PURPOSE AND OF ANY OTHER WARRANTY OBLIGATION ON THE PART OF SELLER. SELLER SPECIFICALLY MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE WITH RESPECT TO THE DICE. SELLER, except as otherwise hereinafter provided, warrrants the DICE delivered hereunder against faulty workmanship or the use of defective materials and that such DICE will conform to this specification. SELLER warrants that at the time of shipment, SELLER has title to the DICE free and clear of any and all liens and encumbrances. These warranties are the only warranties, except as otherwise provided in this document, made by SELLER and can be amended only by a written instrument signed by an officer of SELLER. SELLER shall not be liable for any consequential or incidental damages under its warranty, as SELLER'S sole liability is to either replace or refund the purchase price of any defective DICE, at SELLER'S option, which are returned to SELLER within ten (10) days from date of shipment of the DICE in question. SELLER'S above warranties shall apply to each DIE for ten (10) days from the date of its shipment and shall not apply to any DICE which (1) have been repaired or altered, except by SELLER, or (2) have been subjected to misuse, negligence, or accident by a party other than SELLER, or (3) have been subject to die attach or wire bond procedures or otherwise damaged or altered during manufacturing or assembly operations. This warranty replaces and has precedence over any other warranty representation made by SELLER or any Quote, Acknowledgement or Invoice document.

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