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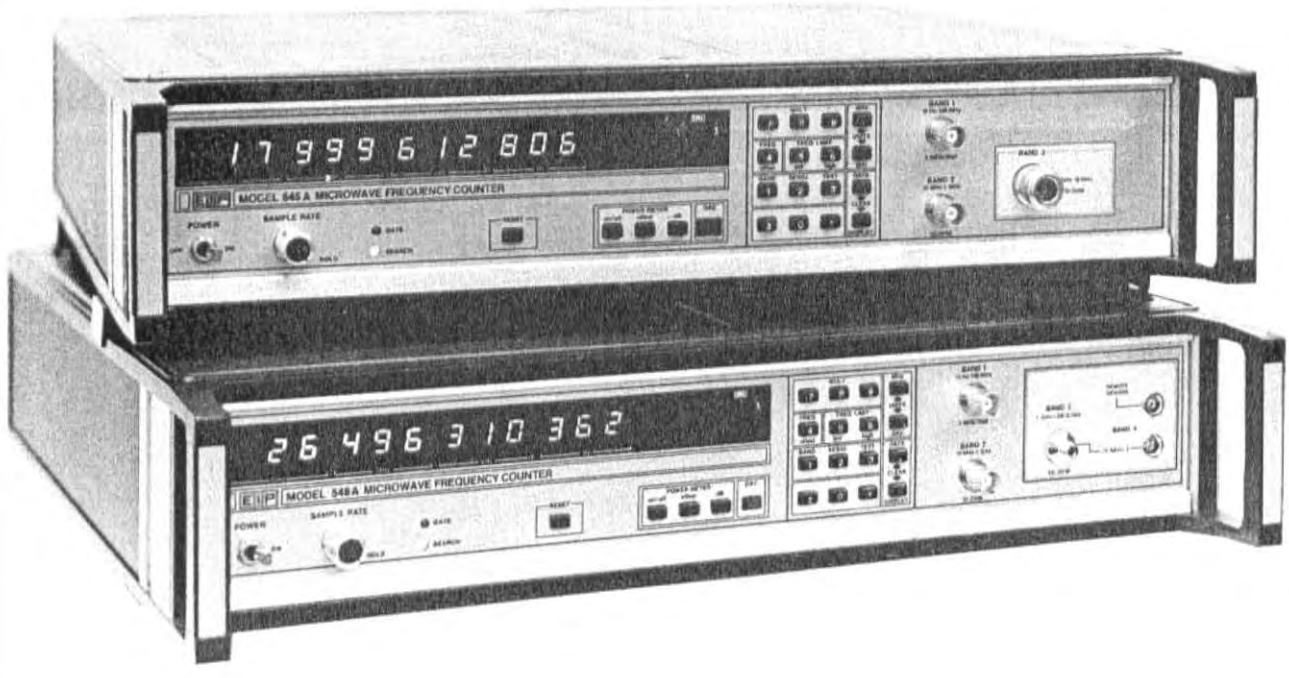
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Models 545A & 548A
Microwave Frequency Counters

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TEL: (408) 433-5900
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Certification

EIP Microwave certifies that this instrument was thoroughly inspected and tested, and found to be in conformance with the specifications noted herein at time of shipment from factory.

Warranty

EIP Microwave warrants this counter to be free from defects in material and workmanship for one year from the date of delivery. Damage due to accident, abuse, or improper signal level, is not covered by the warranty. Removal, defacement, or alteration, of any serial or inspection label, marking, or seal, may void the warranty. EIP Microwave will repair or replace at its option, any components of this counter which prove to be defective during the warranty period, provided the entire counter is returned PREPAID to EIP or an authorized service facility. In-warranty counters will be returned freight prepaid; out-of-warranty units will be returned freight COLLECT. No other warranty other than the above warranty is expressed or implied.

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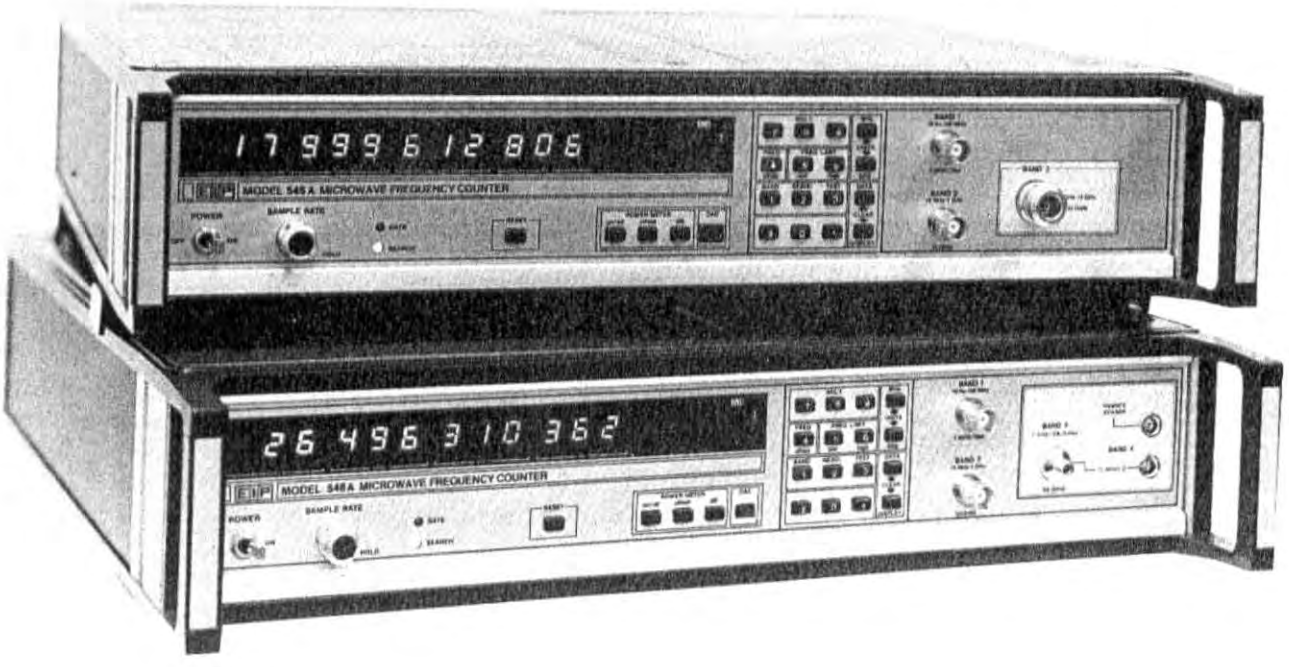
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Section 1
General Information



DESCRIPTION

The 54XA series counters are microprocessor-based heterodyne instruments. The 545A and 548A span the frequency range from 10 Hz to 18 GHz and 10 Hz to 26.5 GHz, respectively. The model 548A, when equipped with frequency extension capability (Option 06), is used in conjunction with a remote sensor (See Model 590) to measure up to 110 GHz.

Using keyboard control, the 54XA series counters provide frequency offsets and frequency selectivity. Options include Power Measurement, full Systems capability via GPIB or BCD/Remote Programming and D/A Converter output.

Full frequency range is covered in three bands. Band 1 is a high impedance input (1 M ohm/20 pF), and spans a 10 Hz to 100 MHz range, with a sensitivity of 25 mV RMS. Band 2 has an input impedance of 50 ohms, a 10 MHz to 1 GHz range, with a sensitivity of −20 dBm. Band 3 has an input impedance of 50 ohms nominal over a range of 1 GHz to 18 (or 26.5) GHz, and a sensitivity to −30 dBm. For frequencies above 26.5 GHz a remote sensor, with an appropriate waveguide input, is called Band 4.

Measurements are presented on a 12 digit LED display that is sectionalized to read GHz, MHz, kHz, and Hz. When the optional power measurement function is activated, the digits on the far right display power in dBm with .1 dB resolution, and frequency resolution is limited to 100 kHz.

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SPECIFICATIONS

BAND 1	
RANGE	10 Hz to 100 MHz
SENSITIVITY	25 mV rms
IMPEDANCE	1 MΩ/20 pF
CONNECTOR	BNC (female)
MAX. INPUT LEVEL	120 V rms *
DAMAGE LEVEL	150 V rms *
	* (Above 1 KHz max. input will decrease at 6 dB/octave down to 3.0 V rms.)

BAND 2	
RANGE	10 MHz to 1 GHz
SENSITIVITY	-20 dBm
DYNAMIC RANGE	30 dB
IMPEDANCE	50Ω Nominal
CONNECTOR	BNC (female)
MAX. INPUT LEVEL	+10 dBm
DAMAGE LEVEL	+27 dBm
ACQUISITION TIME	< 50 msec

BAND 3		
RANGE	1 GHz to 18 GHz (26.5 GHz for model 548A)	
SENSITIVITY	-30 dBm: 1.0 GHz to 12.4 GHz -25 dBm: 12.4 GHz to 18 GHz	-20 dBm: 18 GHz to 22 GHz -15 dBm: 22 GHz to 26.5 GHz
DYNAMIC RANGE	1 GHz to 12.4 GHz, 37 dB 12.4 GHz to 18 GHz, 32 dB	18 GHz to 22 GHz, 27 dB 22 GHz to 26.5 GHz, 22 dB
IMPEDANCE	50Ω Nominal	
CONNECTOR	Model 545A - Precision type N, (female) Model 548A - APC - 3.5 (female)	
MAX. INPUT LEVEL	+7 dBm	
DAMAGE LEVEL	5 Watts (+37 dBm)	
ACQUISITION TIME	~ 250 msec Independent of frequency	
AUTO AMPLITUDE DISCRIMINATION	(Automatic amplitude discrimination of two frequencies) 10 dB	
FM MODULATION	20 MHz P-P up to 10 MHz rate	
VSWR	< 2.5:1 typical	
FREQUENCY LIMIT	Keyboard control of desired limits (standard). Counter will measure largest signal within programmed limits. Signal outside operating band must be separated by at least 100 MHz from either limit. For signals more than 10 dB above desired signal, separation is typically 200 MHz	

TIME BASE	
FREQUENCY	10 MHz TCXO
AGING RATE	$< \lvert 1 \times 10^{-7} \rvert$ per month $\lvert 1 \times 10^{-6} \rvert$ per year
SHORT TERM	$< \lvert 1 \times 10^{-9} \rvert$ rms for one second averaging time.
TEMPERATURE	$< \lvert 1 \times 10^{-6} \rvert$ 0° to + 50°C
LINE VARIATION	$< \lvert 1 \times 10^{-7} \rvert \pm 10\%$ change.
WARM UP TIME	NONE
OUTPUT FREQUENCY	10 MHz, square-wave, 1 V p-p minimum into 50 ohms.
EXT. TIME BASE	Requires 10 MHz, 1 V p-p minimim into 300 ohms.

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SPECIFICATIONS, continued

GENERAL	
RESOLUTION	Front panel keyboard input select 1 Hz to 1 GHz
MEASUREMENT TIME	1 msec for 1 KHz resolution 1 sec for 1 Hz resolution
DISPLAY	12 digit LED sectionalized
ACCURACY	± 1 count ± time base error
TEST	Front panel selected diagnostics
SAMPLE RATE	Controls time between measurements variable from 100 msec typ. to 10 sec. Switchable Hold position holds display indefinitely.
RESET	Resets display to zero and initiates new reading
OFFSETS	Keyboard control of frequency offsets (standard) and power offsets (standard with power measurement Option 02). Displayed frequency (power) is offset by entering value to 1 Hz resolution (0.1 dB power).
OPERATION TEMP.	0°C to 50°C
POWER	100/120/220/240/VAC ± 10% (selectable) 50 to 60 Hz, 60 VA typical
WEIGHT, NET	~ 26 lbs. (11.8 kg)
WEIGHT, SHIPPING	~ 32 lbs. (14.5 kg)
DIMENSIONS (HWD)	3.5" x 16.75" x 14.0" (89 mm X 425 mm X 356 mm)
ACCESSORIES FURNISHED	Power Cord and Manual

BAND 4
Used with 578/06 Counter and 590 Frequency Extension Kit

OPTION	91	92	93	94	95	96
SELECT BAND	41	42	43	44	42 or 43	41 or 42
Waveguide Band	Ka	U	E	W	V	Q
Range	26.5–40 GHz	40–60 GHz	60–90 GHz	90–110 GHz	50–75 GHz	33–50 GHz
Sensitivity (typ)	–25dBm (–20 dBm min)	–25 dBm	–25 dBm	–25 dBm	–25 dBm	–25 dBm
Waveguide Size	WR–28	WR–19	WR–12	WR–10	WR–15	WR–22
Waveguide Flange	UG–599/U	UG–383/U	UG–387/U	UG–387/U	UG–385/U	UG–383/U
Max. Input (typ)	+5 dBm	+5 dBm	+5 dBm	+5 dBm	+5 dBm	+5 dBm
Damage Level	+10 dBm	+10 dBm	+10 dBm	+10 dBm	+10 dBm	+10 dBm
Aquisition Time (typ)	<2.5 sec	<2.5 sec	<2.5 sec	<2.5 sec	<2.5 sec	<2.5 sec

EXAMPLE: If desired measurement is 60 – 90 GHz, the required equipment is:

Model 578 with Option 06 – Extended Frequency and
Model 590 – Extended Frequency Cable Kit with Option 93 – Remote Sensor

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SPECIFICATIONS, continued

OPTIONS — **See Section 10 for detailed information.**

01 D TO A CONVERTER
DAC will convert any three consecutively displayed digits into an analog voltage output on rear panel.

02 POWER METER
1 to 18/26.5 GHz will measure sine wave amplitude to 0.1 dBm resolution from sensitivity to -10 dBm; from -10 dBm to overload and display 0.2 dBm resolution simultaneously with frequency.
Power offset to 0.1 dB resolution, selectable from front panel.
Option will not degrade the basic performance of the counter.

TIME BASE OSCILLATOR OPTIONS:

	03	04	05
AGING RATE/24 HOURS (After 72 hour warm-up)	$< \lvert 5 \times 10^{-9} \rvert$	$< \lvert 1 \times 10^{-9} \rvert$	$< \lvert 5 \times 10^{-10} \rvert$
SHORT TERM STABILITY (1 second average)	$< 1 \times 10^{-10}$ rms	$< 1 \times 10^{-10}$ rms	$< 1 \times 10^{-10}$ rms
0° to +50°C TEMPERATURE STABILITY	$< \lvert 6 \times 10^{-8} \rvert$	$< \lvert 3 \times 10^{-8} \rvert$	$< \lvert 3 \times 10^{-8} \rvert$
± 10% LINE VOLTAGE CHANGE	$< \lvert 5 \times 10^{-10} \rvert$	$< \lvert 2 \times 10^{-10} \rvert$	$< \lvert 2 \times 10^{-10} \rvert$

06 EXTENDED FREQUENCY CAPABILITY —548A
Use in conjunction with models 590 Frequency Extension kit

07 REMOTE PROGRAMMING/BCD OUTPUT

08 GPIB — Provides programming and output capability per IEEE 488-1978.

09 REAR INPUT

10 CHASSIS SLIDES

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Section 2
Installation

SAFETY

The Model 545A/548A Microwave Counter is a Safety Class I instrument. This instrument has been designed and tested according to international safety requirements. This manual contains information, cautions, and warnings that must be followed by the service person to ensure safe operation and to retain the instrument in safe condition.

SAFETY SYMBOLS

WARNING The WARNING sign denotes a hazard. It calls attention to a procedure or practice which, if not correctly performed or adhered to, could result in personal injury.

CAUTION The CAUTION sign denotes a hazard. It calls attention to an operating procedure or practice which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

OVERALL SAFETY CONSIDERATIONS

WARNING

Before this instrument is switched on, the protective earth terminals of this instrument must be connected to the protective conduction of the (mains) power cord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. The protective action must not be negated by the use of an extension cord (power cable) without a protective earth (grounding) conductor.

WARNING

Only fuses with the required rated current, voltage, and specified type should be used. Do not use repaired fuses or short-circuited fuse holders. To do so could cause a shock or fire hazard.

WARNING

Whenever it is likely that the protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.

WARNING

All protective earth terminals. extension cords, autotransformers, and devices connected to this instrument should be connected to a socket outlet provided with a protective earth contact. Any interruption of the protection will cause a potential shock hazard that could result in personal injury.

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INSTALLATION

No special installation instructions are required. The counter is a self-contained bench or rack mounted unit and only requires connection to a standard 100/120/220/240V 50-60 Hz power line for operation.

CAUTION

Check current rating of counter fuse and setting of rear panel VAC selector switch before applying power to counter.

COUNTER IDENTIFICATION

This counter is identified by two sets of numbers, the model number 545A or 548A and a serial number that is located on a label affixed to the rear panel. Both numbers must be mentioned in any correspondence regarding this counter.

SHIPPING

Should it be necessary to ship the counter, wrap it in heavy plastic or kraft paper and repack in original container if available. If the original container cannot be used, use a heavy (275-pound test) double-walled carton with approximately four inches of packing material between the counter and the inner carton. Seal the carton with strong filament tape or strapping. Mark the carton to indicate that it contains a fragile electronic instrument.

STORAGE

The instrument should be stored in an environment that is protected from sand, dust, and other contaminants at an altitude of less than 12,000 m (40,000 ft) and should not be exposed to temperatures beyond the range of -40° C to 75° C, humidity above 95 ±5% (75 ±5% above 30°C, 45 ±5% above 30°C), dripping water, or vibration shock of greater than 2 g.

PERFORMANCE CHECKOUT PROCEDURE

The following procedure can be performed without special tools or equipment.

1. Turn counter power switch off. Check fuse rating and setting of AC POWER switch on rear panel.
2. Connect power cord to 100/120 or 220/240 V, 50-660 Hz single-phase power source. The ground terminal on the power cord plug should be grounded.
3. Turn POWER switch on. Dashes will be displayed for about one second, followed by all 0's. This indicates that automatic self-check has been completed.
4. Press [TEST] [0] [1]. Display should read 200 000 000 ±1.
5. Press [TEST] [0] [2]. Display should read all 8's and all annunciators should be lit.
6. Press [TEST] [0] [3]. Each display segment should light in turn.
7. Press [TEST] [0] [4]. Each digit should light in turn.
8. This completes the performance checkout procedure.

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Section 3
Operation

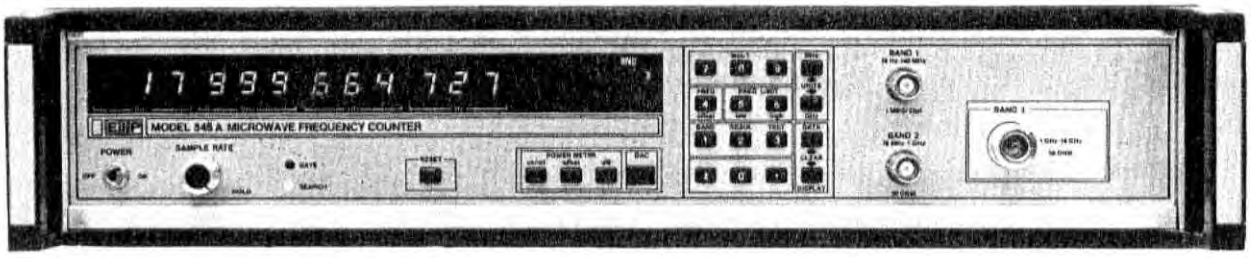


Figure 3-1. Front Panel, Model 545A

FRONT PANEL CONTROLS AND INDICATORS

DISPLAY

- The 12 digit LED display provides a direct numerical readout of a measurement or of an input frequency. The frequency readout is displayed in a fixed position format that is sectionalized in GHz, MHz, kHz and Hz. Power information is displayed in dBm to 0.1 dB resolution, on the three right-most digits. When both power and frequency are displayed, frequency resolution is limited to 100 kHz.

- POWER switch turns counter on.

- SAMPLE RATE/HOLD varies time between measurements from 0.1 to 10 seconds (nominal). (Gate time is added to sample time, thus the minimum reading for 1 Hz resolution is 1.1 seconds.) The last reading is retained indefinitely in HOLD.

- GATE lights when the signal gate is open and a measurement is being made.

- SEARCH lights when the counter is not locked to an input signal.

- RESET manually over-rides all controls, resets the counter and converter, and initiates a new reading.

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OPERATING STATUS

The operating status of the counter is indicated by a series of LEDs. When the counter is displaying input data, instead of a measurement, the appropriate LED status indicator will flash.

- REMOTE lights to indicate that front panel controls are disabled, and that the counter is being controlled by the GPIB option (08), or by the BCD/Remote Programming option (07).
- EXT REF lights to indicate the counter is set to an external time base reference.

CAUTION

When EXT REF lights it does NOT indicate that correct signal level has been applied.

- dBm lights to indicate that the Power Meter option (02) is active.
- FRQ LMT, LOW/HIGH lights when frequency limits for Band 3 operation have been selected.
- OFFSET, PWR/FRQ lights when power and/or frequency offsets are stored in the counter memory.
- Band 1, 2, 3, 41, 42, 43, 44 light to indicate which operating range has been selected. When any Band 4 annunciator is lit it indicates that the Extended Frequency Capability option (06) has been selected (Available on 548A only).
- DAC lights to indicate that the Digital-to-Analog Converter option 01 is active.
- MLT lights to indicate the multiplier function is active.

POWER METER/DAC OPTION KEYBOARD

Four keys control the operation of these options.

- ON/OFF push button activates/deactivates power meter .
- OFFSET push button activates the power offset function.
- dB pushbutton acts as a terminator for the input of power offsets.
- DAC pushbutton, followed by two digits (00-12), activates the DAC option. The number keyed in will select the most significant digit (00 = OFF, 01 = 1 Hz, 12 = 10 GHz).

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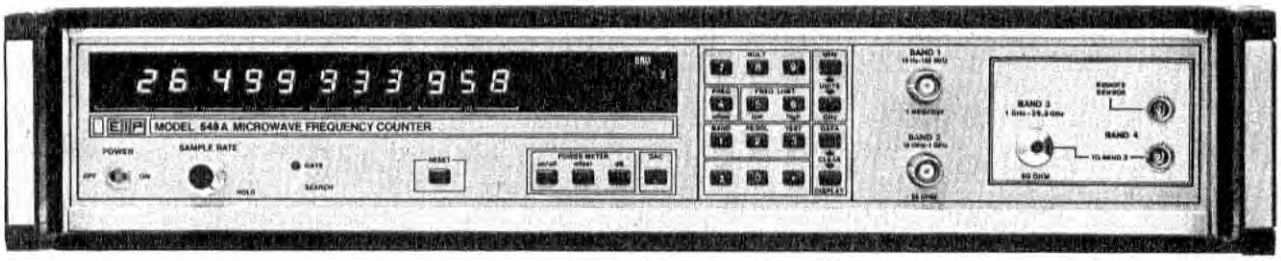


Figure 3-2. Front Panel, 548A

SIGNAL INPUT

- Band 1 input connector (BNC female) has a nominal input impedance of 1 Meg ohms, shunted by 20 pF. It is used for measurements in the range of 10 Hz to 100 MHz.
- Band 2 input connector (BNC female) has a nominal input impedance of 50 ohms. It is used for measurements in the range of 10 MHz to 1 GHz.
- Band 3 input connector on the model 545A is a precision type N female. It is used for counter operation in the range of 1 GHz to 18 GHz. Model 548A has an APC-3.5 female connector that is used for operation in the range of 1 GHz to 26.5 GHz.
- Band 4 is used in conjunction with the Extended Frequency capability option (06), the Model 590 Frequency Extension Cable kit and a remote sensor. Remote sensors are options to the Model 590 and cover waveguide bands from 26.5 to 110 GHz.

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Figure 3-3. Rear Panel

REAR PANEL CONTROLS AND CONNECTORS

- Spaces labeled BAND 1, BAND 2, BAND 3, BAND 4, and TO REMOTE SENSOR are used for those connectors in instruments equipped with Option 09, Rear Panel Input.
- TIME BASE ADJUST control is used with options 03, 04, or 05 only. Screwdriver adjustment allows precise setting of the internal ovenized crystal oscillator.
- TIME BASE INT/EXT switch selects either the internal time base or an external 10 MHz reference.
- TIME BASE connector (BNC female) allows monitoring of internal 10 MHz time base, or input of an external 10 MHz reference.
- DAC OUT connector provides a voltage analog to any specified three digits of frequency displayed, in instruments equipped with Option 01, D to A Converter.
- GPIB connector is used with the IEEE 488 - 1978 General Purpose Interface Bus.
- FUSE provides overload protection. Use a 1 amp slow-blow MDL type fuse for 100/120 V operation. Use a .50 amp slow-blow FST type fuse for 220/240 V operation.
- VAC SWITCH sets the operating voltage of the counter to match power line. There are 4 settings: 100, 120, 220, and 240 VAC. Counter will operate at voltages within ±10% of selected line voltage, at frequencies of 50 to 60 Hz.

CAUTION

Switch setting and fuse rating must match power line voltage.

- AC POWER connector accepts the power cord supplied with the counter.

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Figure 3-4. Keyboard

KEYBOARD

The keyboard consists of 16 pushbuttons that control major functions of the counter. Twelve keys are used for numerical data entry, the digits 0 through 9, the decimal point and the minus sign. Two keys (MHz and GHz) act as terminators for the input of frequency offset or frequency limits. The CLEAR DATA and CLEAR DISPLAY keys are used to clear stored or displayed data. Seven of the numerical keys are also used to select the band, resolution, test function, frequency offset, frequency limits, and multiplier function.

UNITS (MHz/GHz)

PRESS: MHz — Completes Entry Sequence

PRESS: GHz — Completes Entry Sequence

CLEAR (DATA/DISPLAY)

PRESS: DATA CLEAR — Return "STORED" data of selected function to Power On state. Clears Limits (Low/High), Offsets, DAC, and multiplier operations.

PRESS: CLEAR DISPLAY — Clears display. Does not affect stored data. Restores counter to measurement mode.

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BAND SELECTION

To select one of three standard operating bands on the model 545A or 548A .

PRESS: BAND [ ] [1] or BAND [ ] [2] or BAND [ ] [3]

Notice annunciator flash and selected band number will light when chosen. This feature allows multiple inputs to be connected and selected in turn.

The "BAND" KEY followed by a numeric key enables the following band selection.

PRESS: BAND [ ] [1] 10 Hz - 100 MHz Input

PRESS: BAND [ ] [2] 10 MHz - 1 GHz Input

PRESS: BAND [ ] [3] 1 GHz - 18 GHz (Model 545A) 26.5 GHz (Model 548A)

On the model 548A equipped with option 06, a 590 cable kit and appropriate optional remote sensor, Band 4 is selected by:

PRESS: BAND [ ] [4] [X]

For example, with the 91 Sensor you will press: BAND [ ] [4] [1]

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RESOLUTION / GATE TIME SELECTION

The "RESOL" key followed by a numeric key enables following resolutions.

PRESS:	RESOL	0	1 Hz RESOLUTION
PRESS:	RESOL	1	10 Hz RESOLUTION
PRESS:	RESOL	2	100 Hz RESOLUTION
PRESS:	RESOL	3	1 KHz RESOLUTION
PRESS:	RESOL	4	10 KHz RESOLUTION
PRESS:	RESOL	5	100 KHz RESOLUTION
PRESS:	RESOL	6	1 MHz RESOLUTION
PRESS:	RESOL	7	10 MHz RESOLUTION
PRESS:	RESOL	8	100 MHz RESOLUTION
PRESS:	RESOL	9	1 GHz RESOLUTION

As the resolution is decreased from 1 Hz to 1 kHz, the gate time LED should cycle faster:

- 1 Hz resolution equals a gate time of 1 sec.
- 10 Hz = 100 msec Gate time
- 100 Hz = 10 msec Gate time
- 1 KHz to 1 GHz = 1 msec Gate time

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DISPLAY AND DATA ENTRY SEQUENCE

The keyboard display and data entry sequences are segmented into four main groups. All keyboard operations must be started by choosing the function first.

DATA ENTRY - enter offsets or limits

Sequence : 1. FUNCTION , SIGN (plus sign not required) , NUMBER , DECIMAL , NUMBER , UNITS (decimal and second number is optional)

2. FUNCTION , NUMBER

Examples: 1. FREQ OFFSET [±] [1] [•] [2] [GHz]

2. BAND [2]

DISPLAY DATA - display previously entered data

Sequence : FUNCTION , CLEAR DISPLAY

Example : FREQ OFFSET CLEAR DISPLAY

CLEAR DATA - clear entered data

Sequence : 1. FUNCTION , CLEAR DATA

2. FUNCTION , [0] , UNITS

3. FUNCTION , UNITS

Examples: 1. FREQ OFFSET DATA CLEAR

2. FREQ OFFSET [0] GHz

3. FREQ OFFSET GHz

CLEAR ENTRY - clear display before completing data entry

Sequence : FUNCTION , STRING , CLEAR DISPLAY

Example : FREQ OFFSET [1] [•] [2] CLEAR DISPLAY

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MULTIPLY FUNCTION:

In the multiply function the measured frequency is multiplied by an integer up to 99. The result is displayed to 1 KHz resolution. If the results of the multiplications are too big for the front panel to display, the front panel will show F's.

EXAMPLES: PRESS [MULT] AND KEY IN TWO DIGIT NUMBER

EXAMPLE [MULT] [0] [2] FOR MULTIPLIER = 2

NOTE: When "MULT" key is pressed the annunciator "MLT" will flash until the sequence is completed. The two digit multiplier (m) will be displayed as the numbers are entered.

To clear the multiplier function the following operation is performed.

PRESS [MULT] [CLEAR DATA] or PRESS [MULT] [0] [1]

This sequence clears the multiplier function and multiplier (m).

mX ± b

By using the frequency offsets and multiply functions the counter can automatically perform mX ± b calculations.

The equation for the function performed is:

Displayed Reading = mX ± b where m = Multiplier (up to 99) entered from keyboard.

X = Input frequency.

± b = Frequency offset entered from the keyboard.

TO DO mX ± b CALCULATION FOR m = 2, b = -70 MHz

PRESS [MULT] [0] [2] AND [FREQ OFFSET] [±] [7] [0] [MHz]

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FREQUENCY LIMITS

Frequency limits can be entered to 10 MHz resolution .

PRESS: FREQ LIMIT [low] Notice flashing annunciator.

PRESS: [#] Number keys corresponding to desired frequency low limit to 10 MHz resolution.

PRESS: [MHz] or [GHz] To terminate input sequence. Notice FRQ LMT LOW annunciators solidly lit.

PRESS: FREQ LIMIT [high] Notice flashing annunciator

PRESS: [#] Key numbers corresponding to desired freq. Hi limit.

PRESS: [MHz] or [GHz] To terminate input sequence. Notice FRQ LMT Hi annunciator. solidly lit.

To recall stored limits.

PRESS: FREQ LIMIT [low] and CLEAR [DISPLAY] then FREQ LIMIT [high] and CLEAR [DISPLAY]

To clear data memory and remove frequency limits.

PRESS: FREQ LIMIT [low] and DATA [CLEAR] then FREQ LIMIT [high] and DATA [CLEAR] Vary Source. Notice selected limit(s) are erased. Also notice "FRQ LMT LOW HI" annunciators are out.

NOTE: High and low limits should be separated by at least 100 MHz.

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TEST SELECTION

The following tests will verify proper operation of most functional areas of the counter. At the initial turn on the counter performs a RAM and PROM check. During this check dashes are displayed until the check has been completed.

RAM and PROM

The processor writes a sequential bit pattern to each RAM location, then independently reads that pattern. Thus each bit in each location is checked. If the RAM check fails the display will show all "E's". This indicates that the RAM or the RAM decoding is faulty.

The PROM check verifies the PROM bit pattern. If the PROM check fails an error message will be displayed. This indicates that the PROM's or the PROM decoding is faulty. See Section 6.

If both RAM and PROM check are good the counter will begin normal operation about one second after turn on. The counter will now display all 0's.

200 MHz SELF TEST

PRESS: TEST [ ] [0] [1]

Notice display is 200 MHz. This verifies operation of the time base reference and it's associated circuits, the signal selection, the count chain, and the local oscillator.

LED TEST

PRESS: TEST [ ] [0] [2]

Notice all LED segments and yellow annunciators are lit. This verifies operation of all visual indicators

LED SEGMENT TEST

PRESS: TEST [ ] [0] [3]

Notice each segment of each display digit is lit in turn. The sample rate pot will change the rate, and may be adjusted. This checks the segment drivers.

DISPLAY DIGIT TEST

PRESS: TEST [ ] [0] [4]

Notice all segments of each digit are lit in turn to verify that each digit operates independently.
The sample rate pot will change the rate, and may be adjusted.

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KEYBOARD TEST

PRESS: TEST [ ] [0] [5]

Notice display is 05. Press any key and display will indicate a two digit number showing the position of that key within the matrix thus checking keyboard operations. See Figure 6-5 for coordinates.

TO EXIT TESTS

PRESS: CLEAR DISPLAY [ ] to exit a test and return to normal operation.

To exit tests 1 through 4, 6 and 7 you can press any function key. This will exit the test and enter the function selected.

Tests 6 through 10 are used for calibration and troubleshooting. See Pages 6-6 and 6-7.

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SET-UP FOR BASIC FREQUENCY MEASUREMENT

Choose the input band by pressing BAND [ ] and a number key corresponding to the band. Choose resolution by pressing RESOL [ ] and a number key corresponding to required resolution. The signal coupled to the selected input Band Connector will be automatically displayed to the resolution chosen.

NOTE: When pressing the RESOL key the display will go blank for approximately 1/4 second.

FREQUENCY OFFSETS

Frequency OFFSETS can be added or subtracted from the measured value. These OFFSETS can be entered via the front panel keyboard to 1 Hz resolution:

PRESS: FREQ [ ] OFFSET — Notice the flashing annunciator.

PRESS: Number keys corresponding to desired frequency OFFSETS. If OFFSET is to be subtracted press [±] and notice polarity sign indicator at far left of display.

PRESS: MHz [ ] or [ ] GHz to integrate programmed OFFSET into actual frequency measurement. Notice solidly lit annunciator indicating instrument memory is loaded.

PRESS: FREQ [ ] OFFSET — Recalls OFFSET to display, FRQ and OFFSET annunciators flashing.

PRESS: CLEAR [ ] DISPLAY — Notice frequency displayed includes OFFSET; annunciators are lit continuously.

PRESS: FREQ [ ] OFFSET — Recalls OFFSET to display; FRQ and OFFSET annunciators flashing.

PRESS: CLEAR [ ] DATA — Clears data memory and clears offset.
FRQ and OFFSET annunciators are out.
Display is actual frequency without offset.

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DISPLAY ERROR MESSAGES

When an error occurs the error number will be displayed. The probable cause of each error is listed below.

OPERATOR ERRORS

The following error messages indicate an operator error.

01 Illegal Key Sequence.

02 A resolution number was not entered.

03 A band number was not entered; or the number entered was too large.

04 No power reading in current band.

05 Frequency limit high > 18.5 GHz, 27 GHz (548A).

06 (Freq Limit HI) – (Freq Limit Lo) < Min. (100 MHz) difference.

07 Frequency Limit Low < .95 GHz (545A/548A).

08

09 Illegal test mode key sequence.

10 Illegal DAC key sequence.

11 Illegal Multiplier key sequence.

12

13 Option not installed.

COUNTER ERRORS

The following error messages indicate a malfunction within the counter.

31	Check sum error	Section 1 PROM	D0000 - DFFF	A105, U13
32	Check sum error	Section 2 PROM	E000 - EFFF	A105, U17
33	Check sum error	Section 3 PROM	E000 - FFFF	A105, U15

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Section 4
Theory of Operation

GENERAL

The 545A and 548A counters automatically measure and display the frequency of an input signal within the range of 10 Hz to 18 GHz for the 545A, and 10 Hz to 26.5 GHz for the 548A. In both models the frequency is divided into three bands.

BAND 1 operates from 10 Hz to 100 MHz. An impedance converter provides an input impedance of 1 M ohm, shunted by 20 pF.

BAND 2 operates from 10 MHz to 1 GHz, using a heterodyne down converter which converts the input signal into an output signal with a range of 10 MHz to 190 MHz.

BAND 3 operates in the microwave range of 1 to 18 GHz (or 26.5 GHz) and uses a YIG tuned heterodyne converter to translate the input frequency downward to an intermediate frequency (IF) of 125 MHz.

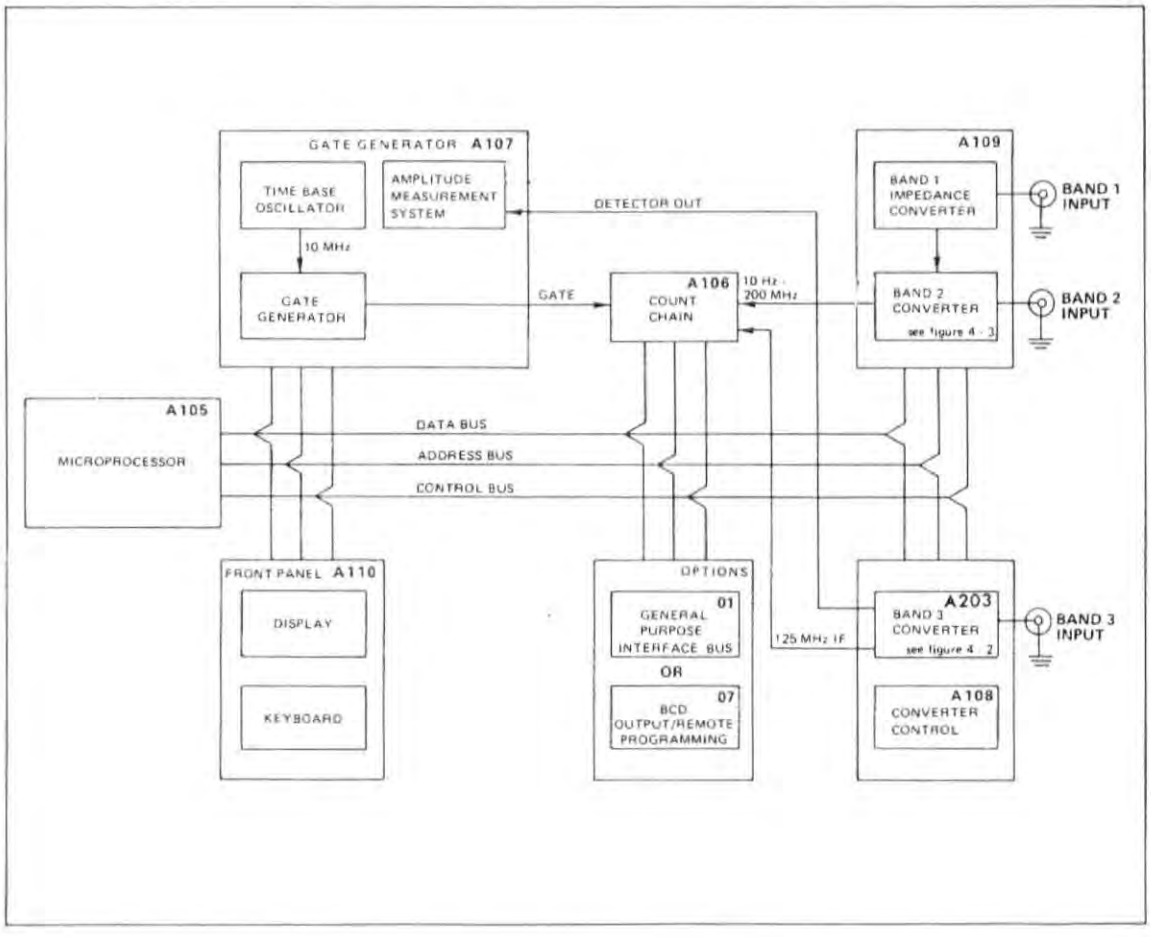


Figure 4-1. Counter Block Diagram, Simplified

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BASIC COUNTER

Overall operation is controlled by the Microprocessor Assembly A105. This assembly contains an eight bit microprocessor, its control logic, and the system memory. It communicates with all other assemblies in the instrument by means of a triple bus system: the data, address, and control bus. On each assembly there is a Peripheral Interface Adaptor (PIA) which provides the interface between the bus system and the instrument hardware.

Frequency measurements are performed by comparing an unknown signal to a reference frequency, namely the time base. A 10 MHz crystal oscillator is used as the internal reference and is a part of the Gate Generator Assembly A107. For increased accuracy and stability, ovenized oscillator options are available, or the user may select an external 10 MHz reference.

A frequency measurement is made by generating a time interval (Gate Time) consisting of a number of cycles of the reference. This Gate Time is then used as an interval during which the input signal is counted by the Count Chain Assembly A106.

Initially, the microprocessor selects one of several available inputs to the Count Chain Assembly and the appropriate Gate Time based on user input information; band selection, resolution, etc. The microprocessor then initiates the measurement cycle by resetting the Count Chain to zero and allowing a gate to be generated. During the gate interval, the Count Chain accumulates the number of cycles of the input signal. At the end of the gate time, the microprocessor reads the stored information in the Count Chain and performs any required calculations necessary to convert the measurement into a direct reading of the unknown frequency. The front panel display is then updated with the new measurement results. Figure 4-1 shows a simplified block diagram of the counter.

BAND 2 CONVERTER

An input signal is applied to the mixer along with an appropriate local oscillator (L.O.) to generate an IF frequency in the range of 10 MHz to 190 MHz. This signal is filtered and amplified to a level suitable for direct measurement by the Count Chain.

The L.O. frequency is generated by the Voltage Controlled Oscillator (VCO) of the Band 3 Converter. This frequency is phase locked to the counter's time base and controlled by the microprocessor. A VCO multiplier serves to either pass along the signal directly or double it. It can also turn off the signal and pass only a DC bias to the mixer.

Two detectors provide outputs proportional to the amplitudes of both the applied RF signal and the resulting IF signal. These outputs are compared in the Signal Comparator, which provides a digital output when the IF amplitude exceeds the RF amplitude.

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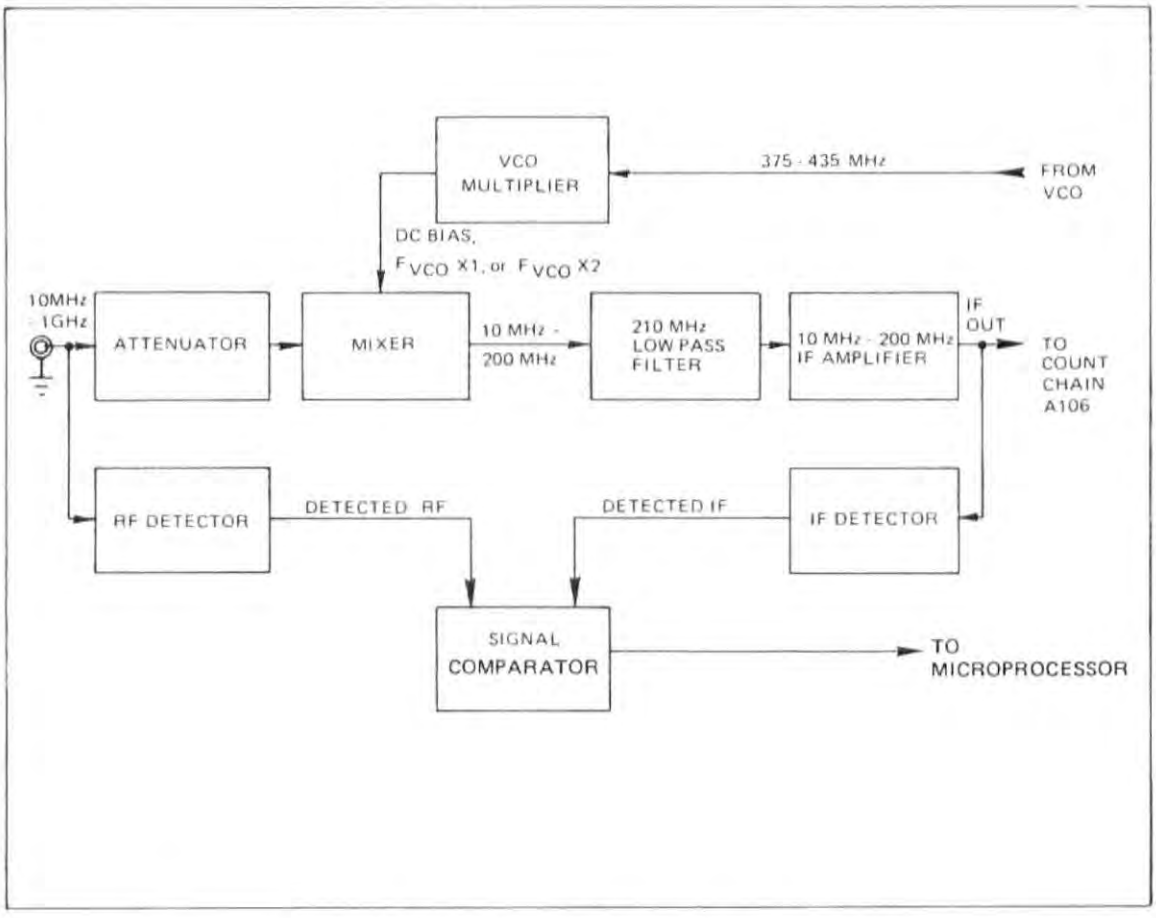


Figure 4-2 Band 2 Converter Block Diagram, Simplified

The output frequency of the system is the difference between the input signal and the L.O. applied to the mixer. Since the L.O. frequency is a harmonic (N) of the VCO frequency, the unknown input frequency can be expressed as $F_{IN}=N\,F_{VCO} \pm F_{IF}$. There are three primary functions of the software operating the converter:

- To select the appropriate harmonic number N.
- To select an appropriate VCO frequency.
- To determine whether the IF frequency is added to, or subtracted from the L.O. frequency.

These functions are accomplished by selecting N and F_{VCO} and looking for an IF signal of the appropriate amplitude and frequency. Overall system gain is such that whenever the correct L.O. frequency is applied, the IF power will exceed the RF power. This is the primary information used in determining the correct VCO frequency and harmonic number. Once an IF is obtained, the harmonic number is verified and the +/- sign in the equation is determined by shifting the VCO frequency and observing the magnitude and direction of the resulting IF shift. Converter operation is diagrammed in figure 4-3.

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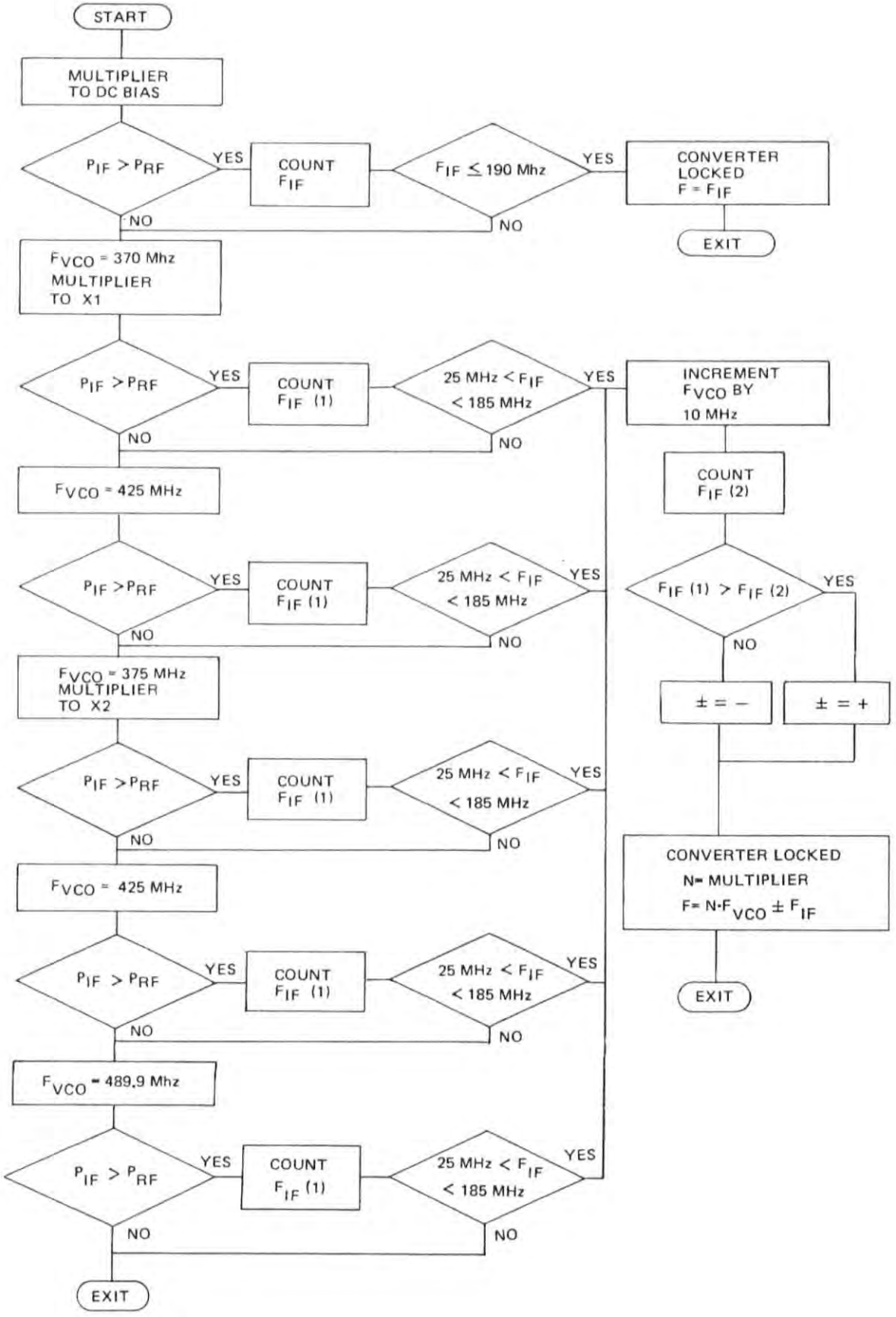


Figure 4-3. Band 2 Converter Operation

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The L.O. frequencies being used, except the range of direct counting (< 190 MHz), have been selected so only IF frequencies from 25 MHz to 185 MHz are required. Since the counter can count signals less than 10 MHz, the restricted operating range provides margin for frequency modulation on the input signal, and for incrementing the VCO frequency.

Figure 4-4 shows the operating ranges for the various harmonics and VCO frequencies used.

Input Frequency Range F_{IN}(MHz)	VCO Frequency F_{VCO}(MHz)	Harmonic Number N	IF Frequency Range F_{IF}(MHz)
10 - 190	—	0	10 - 190
185 - 345	370	1	185 - 25
345 - 400	425	1	80 - 25
400 - 560	375	1	25 - 185
560 - 610	425	1	135 - 185
610 - 725	375	2	140 - 25
725 - 825	425	2	125 - 25
825 - 935	375	2	75 - 185
935 - 1035	425	2	85 - 185
1035 - 1164.8	489.9	2	55.2 - 185

Figure 4-4. Band 2 Operating Ranges

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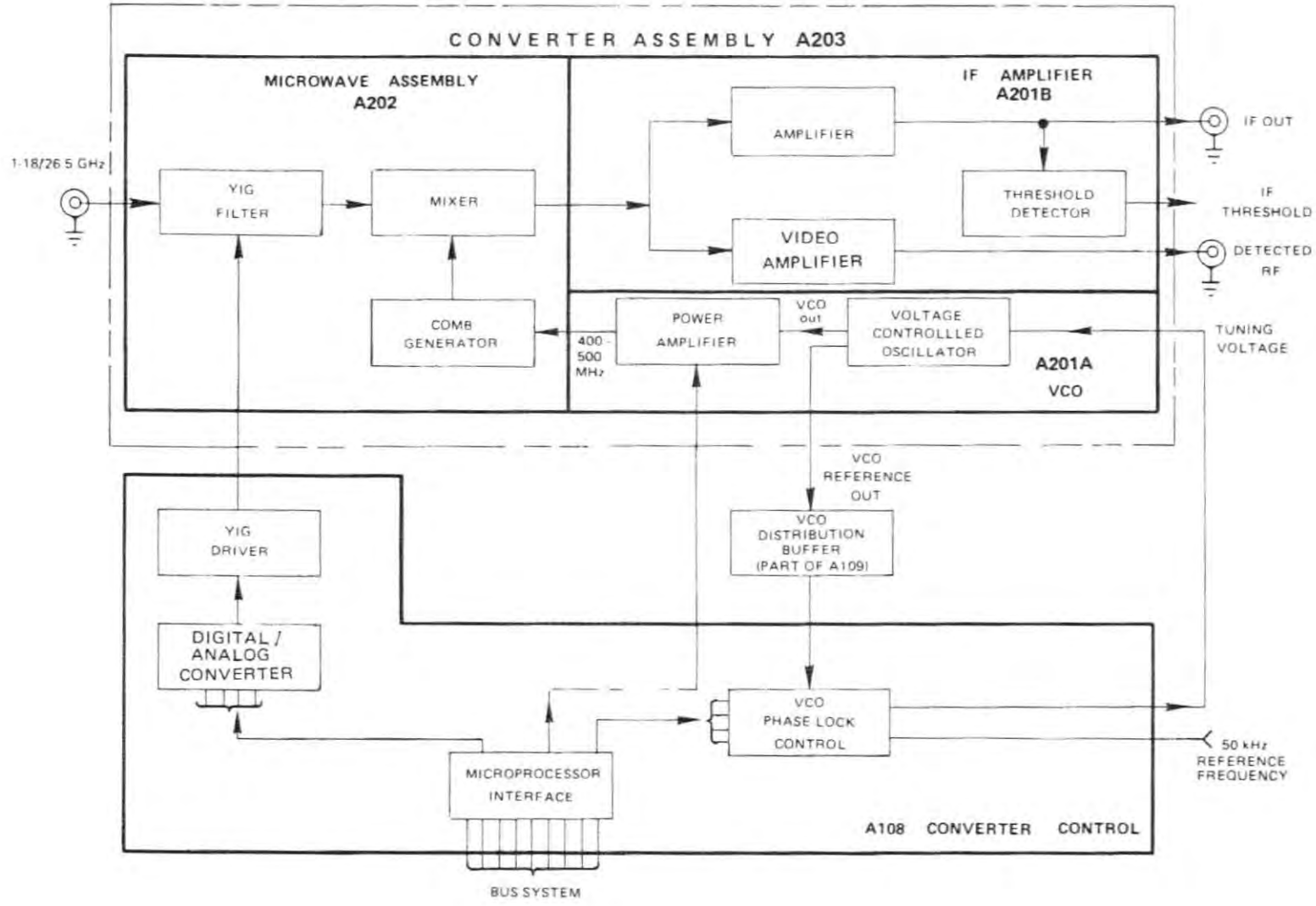


Figure 4-5 Band 3 Converter, Simplified.

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BAND 3 CONVERTER

Measurement of a signal in Band 3 is accomplished by down converting from the microwave range to approximately 125 MHz. This is accomplished by mixing the input signal with a known reference frequency which is found by selecting a VCO harmonic in the range of 400 to 500 MHz. The VCO frequency can be selected in 50 kHz increments by using a microprocessor controlled phase lock system, while retaining the accuracy and stability of the counter's time base reference.

A simplified diagram of the Band 3 converter is shown in figure 4-5. There are two major assemblies. The Converter Control assembly (A108) and the Converter Assembly (A203).

CONVERTER CONTROL A108

The Converter Control assembly contains the interface between the microprocessor bus system and the Converter (A203). A digital-to-analog converter and a precision current (YIG) driver provide a 2 MHz frequency resolution for setting the YIG filter of A202.

A108 also contains the programmable VCO phase lock control system. This system lets the microprocessor interface select any VCO frequency between 400 and 500 MHz, in increments of 50 kHz.

CONVERTER A203

The Converter assembly consists of three subassemblies.

- A201A, Voltage Controlled Oscillator (VCO) Assembly
- A201B, IF Amplifier Assembly
- A202, Microwave Assembly (yig)

The A202 Microwave Assembly contains the YIG filter, mixer and comb generator.

The input signal (1 GHz - 18 GHz/26.5 GHz) passes through a YIG filter on A202. The filter is an electronically tunable bandpass filter, with an operating frequency proportional to its tuning current. This filter determines the approximate frequency of the input signal, and filters out any undesired signals, making it possible to count a signal at one frequency even if a larger signal is present at another frequency.

When tuning the YIG filter to the input signal, the mixer is used as an RF detector, and its output is amplified in the video amplifier on the IF assembly .

The output of the Video amplifier is maximum when the YIG filter is tuned to the input signal. In the case of multiple input signals, the video amplifier output determines which signal is largest.

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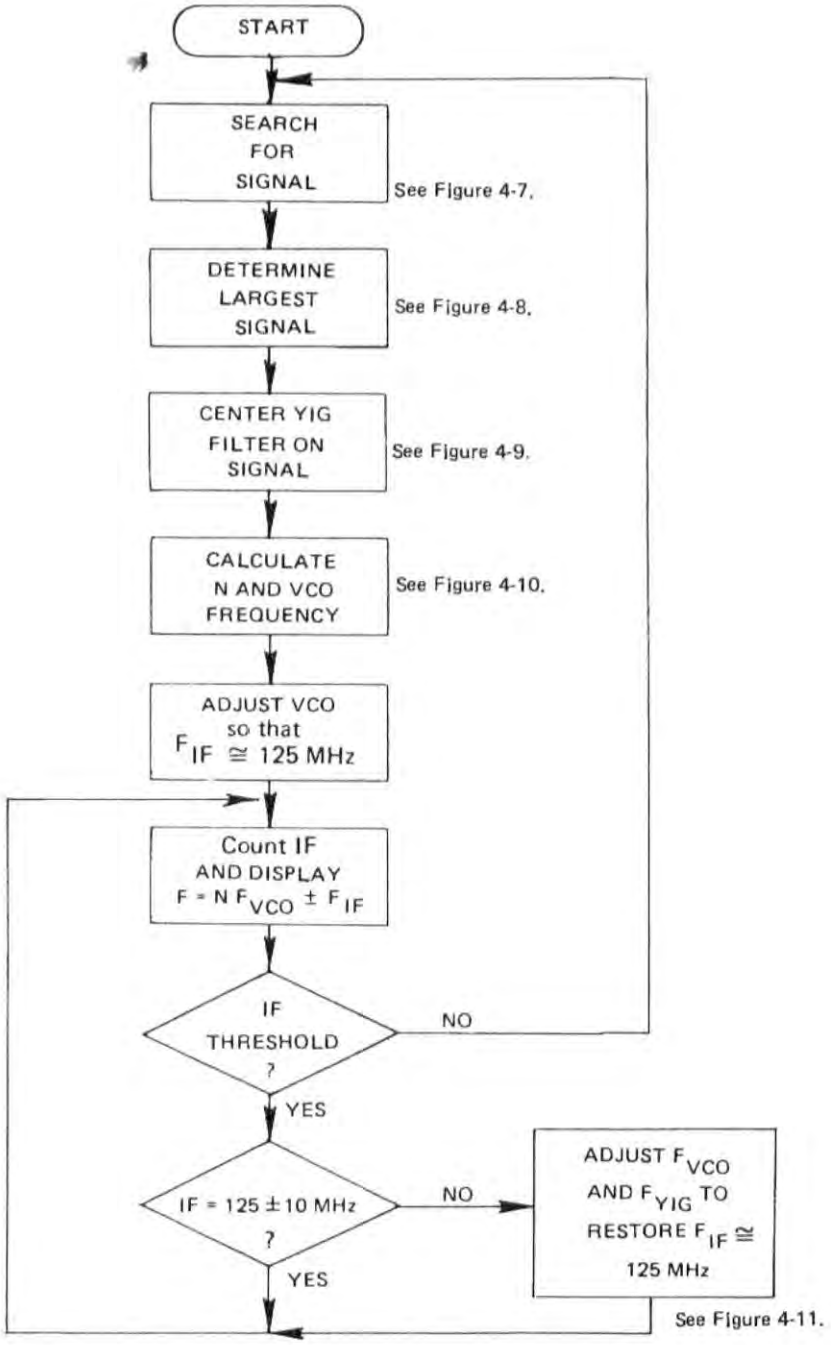


Figure 4-6. Band 3 Operation, Simplified.

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On units equipped with the Power Measurement Option (02), accurate frequency correction factors are stored in the counter's memory. This allows absolute power calibration of the video amplifier output.

Once the YIG filter is tuned to the input signal, the appropriate harmonic number (N) and VCO frequency (F_{VCO}) are selected to produce an IF frequency (F_{IF}) at approximately 125 MHz. An approximation of the input signal is found by using:

$$F_{IN} = N F_{VCO} \pm F_{IF}$$

The IF frequency produced in the mixer is amplified by the high gain IF amplifier and sent to the count chain (A106). The IF threshold detector (A201B) insures sufficient IF amplitude for count accuracy.

OPERATION

First the YIG filter is stepped, (in 64 MHz steps), from its low to high limits. During this search the RF detected output is fed, through a microprocessor controlled step attenuator to a threshold detector. After each step the threshold detector is checked. If triggered, the search mode is halted until the amplitude of the signal is determined. This is done by stepping the filter back and forth through the signal and stepping the attenuator until the signal is attenuated below the threshold. The counter then returns to the search mode to look for any larger signals. After searching the entire frequency range, it returns to the largest signal and begins to center the YIG filter precisely on the input frequency. See Figure 4-6 for a simplified diagram of Band 3 operation. For more detailed descriptions of Band 3 operation see Figures 4-7 through Figure 4-11.

The centering process consists of slowly stepping the YIG filter down (in 2 MHz increments) until a level of 3-6 dB below the peak is reached. This frequency is stored and the process is repeated from the other side by stepping the filter up in 2 MHz steps. The average of the two frequencies obtained is the center of the passband. This is the frequency which is used to determine the N and F_{VCO}.

After centering, N is determined from $N = \frac{F_{YIG} \cdot 125}{500}$ and then rounded up to the next highest integer. From this, F_{VCO} is calculated using $F_{VCO} = \frac{F_{YIG} \cdot 125.}{N}$. Should this yield $F_{VCO} < 400$ MHz, then F_{VCO} is recalculated using $F_{VCO} = \frac{F_{YIG} + 125.}{N}$

Since F_{YIG} is only approximately equal to F_{IN}, the IF frequency will not be exactly 125 MHz. Therefore, the next step in operation is a VCO frequency adjustment to shift F_{IF} into the middle of the IF passband.

VCO frequency correction is achieved by counting F_{IF} and changing F_{VCO} by $\pm \frac{F_{IF} \cdot 125.}{N}$. If the error is large enough to be outside the IF passband (IF threshold is not triggered) then a series of steps (shifting the IF in ± 20 MHz increments) are taken until the signal falls within the passband.

Once the VCO corrections have been made, the converter has acquired the signal and the counter is ready to count and display the input frequency.

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After each measurement, the frequency of the IF is examined. If the input frequency has shifted more than 10 MHz, new frequencies for the YIG and VCO are calculated to restore the IF to 125 MHz. This method provides rapid tracking of a signal being tuned.

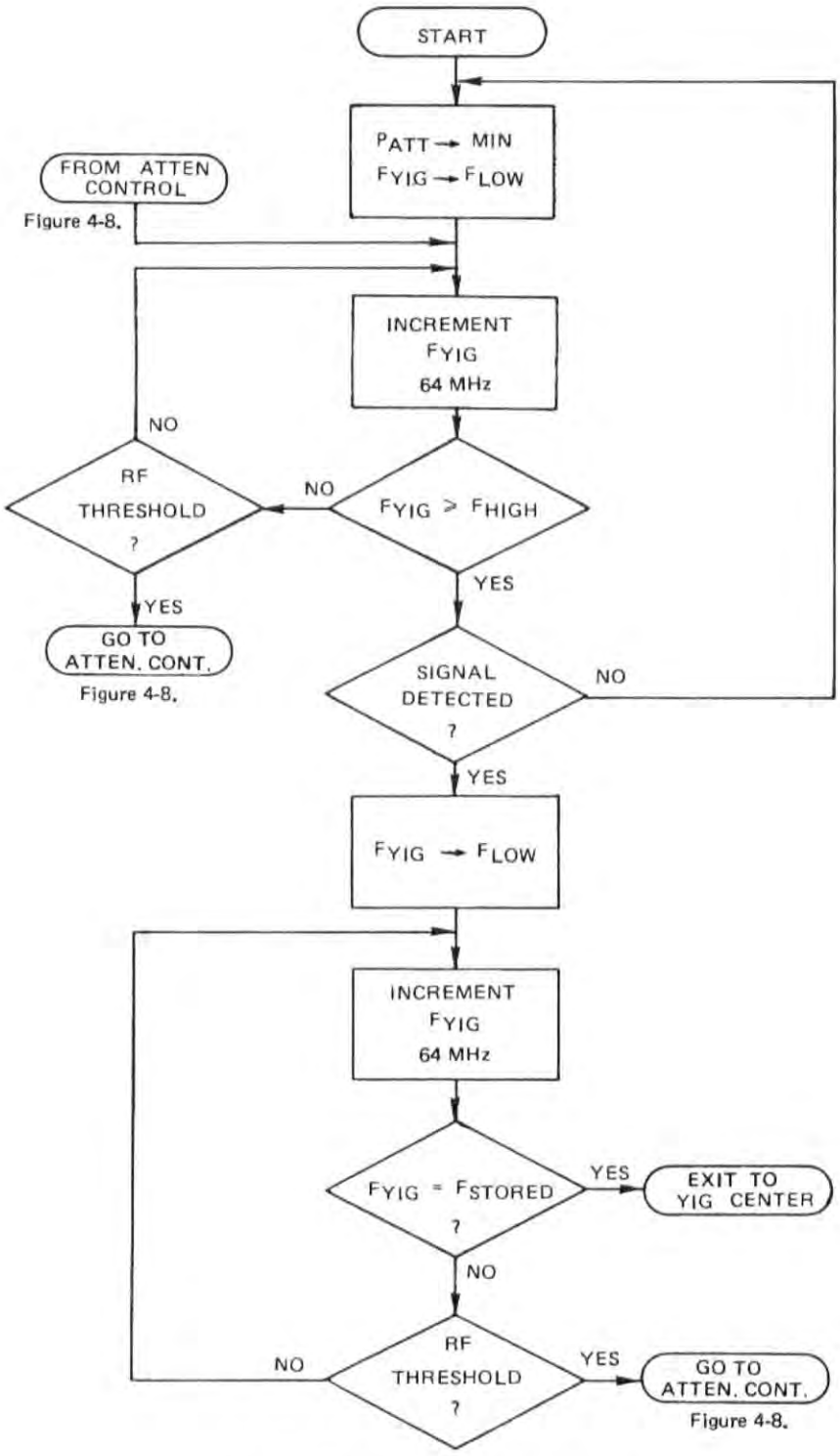


Figure 4-7. Band 3 Search For Signal

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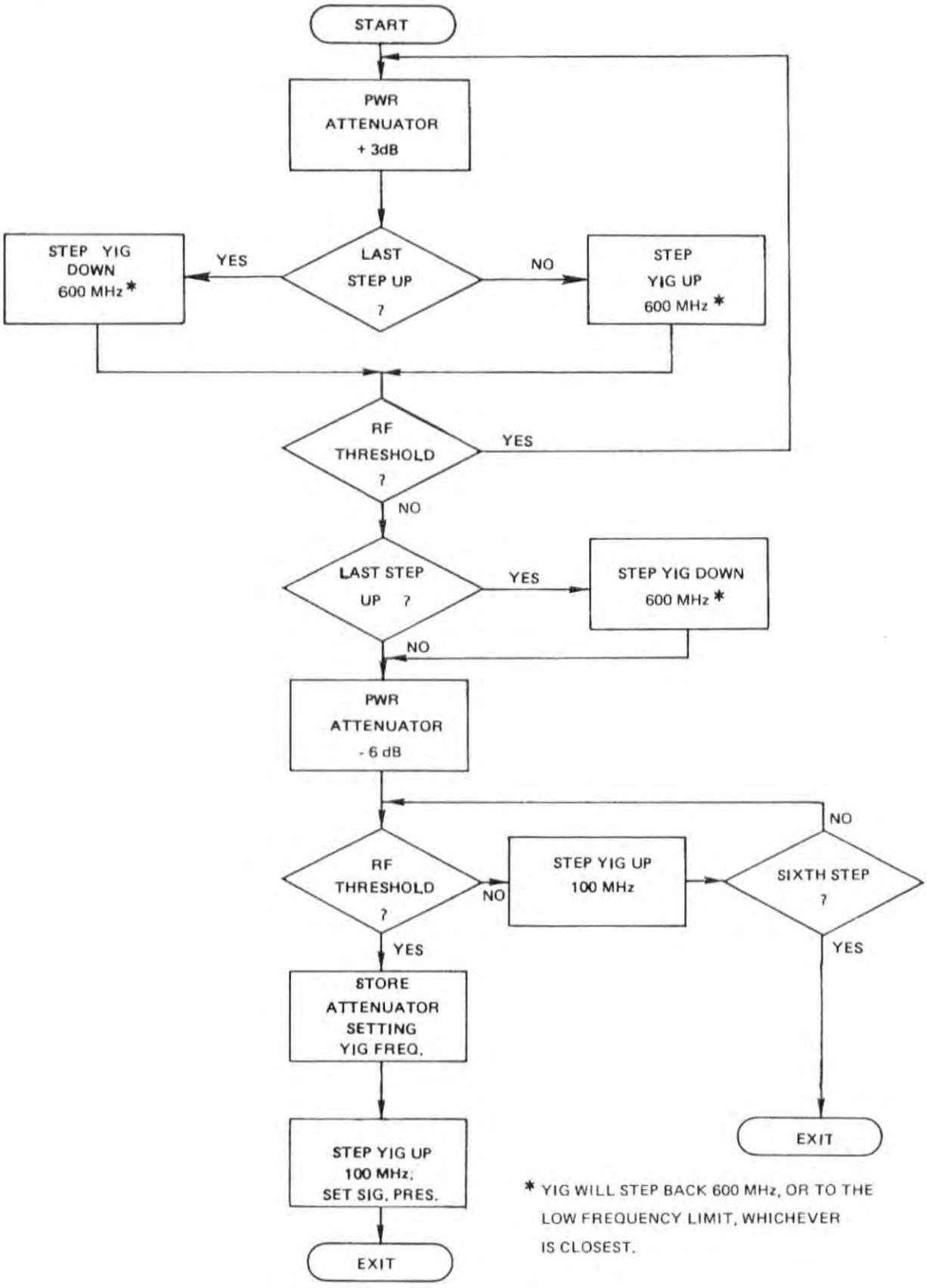


Figure 4-8. Determine Largest Signal

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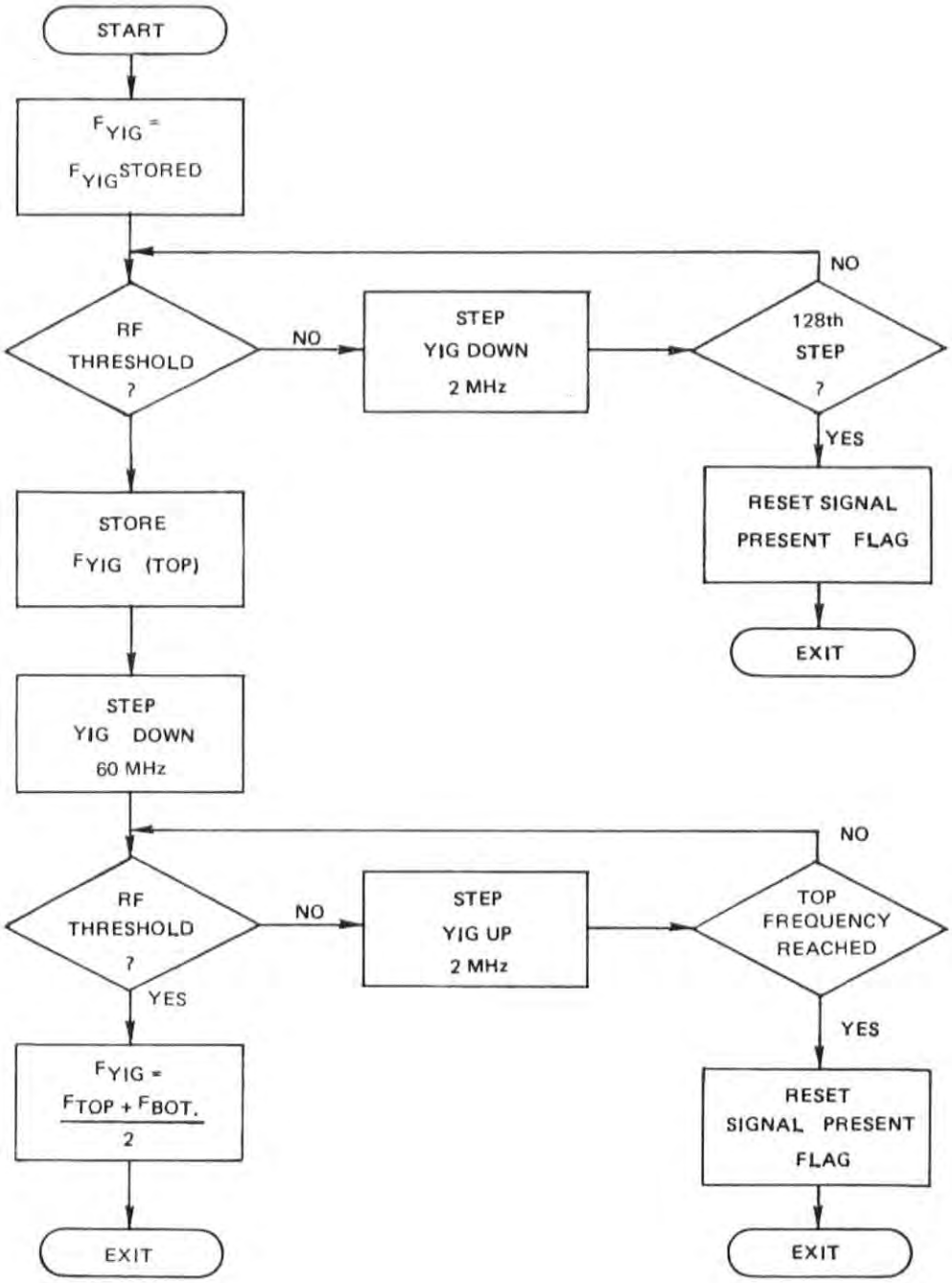


Figure 4-9. YIG Centering

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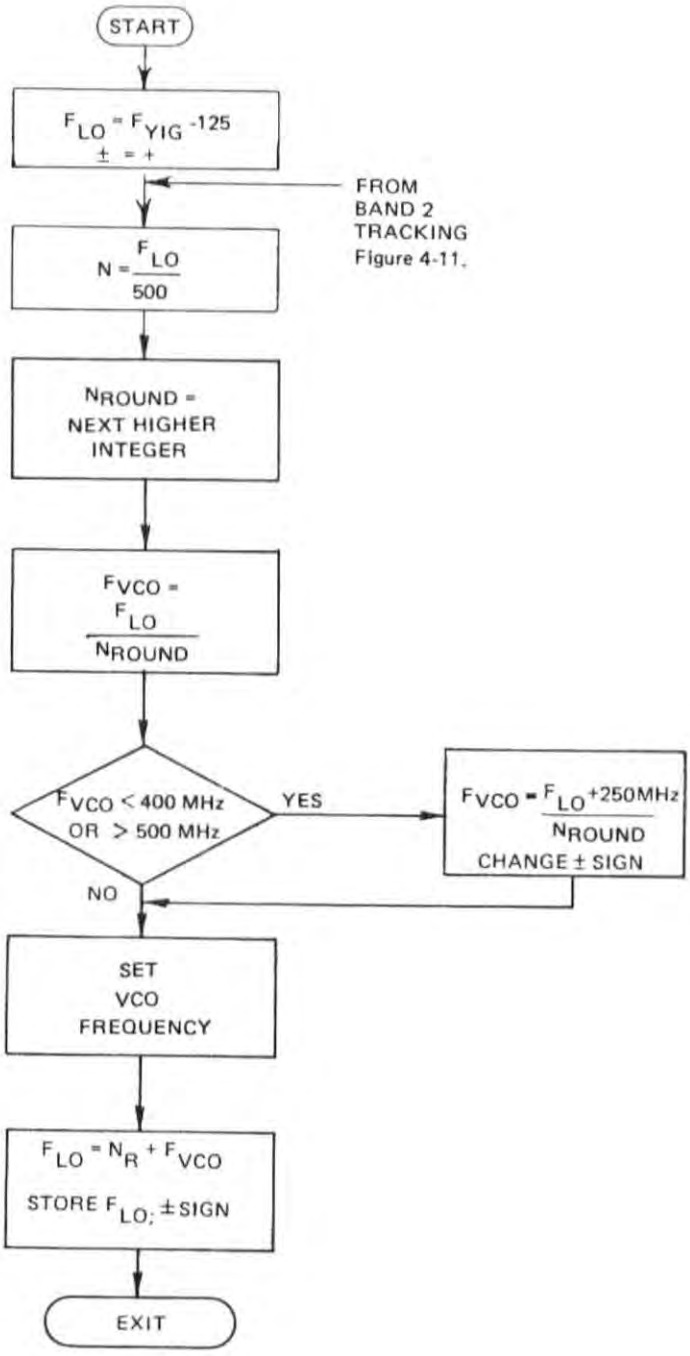


Figure 4-10. Calculate N and VCO Frequency

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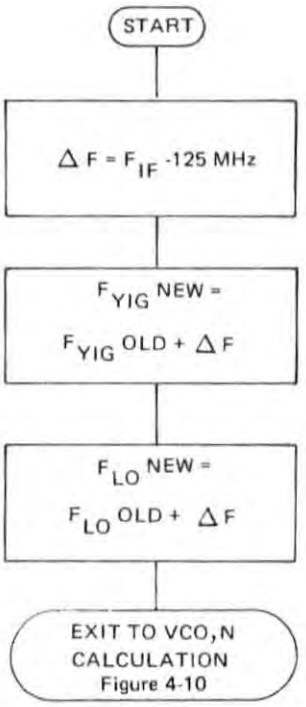


Figure 4-10

Figure 4-11. Band 3 Signal Tracking

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Section 5
Maintenance and Service

This section contains information about your counter and instructions for performing maintenance and service.

MAINTENANCE

FUSE REPLACEMENT

The Model 545A/548A Microwave Counter uses one fuse; it is located on the rear panel next to the voltage select switch.

- o For 100/120 Vac operation use a 1.0-A slow-blow MDL-type fuse.
- o For 220/240 Vac operation use a 0.50-A slow-blow FST-type fuse.

The voltage select switch should be set to the proper line voltage.

WARNING

Be sure the counter is disconnected from the power line.

1. With a flat-edged screw driver, rotate the voltage select switch until the arrow points to the desired line voltage.
2. Change to a fuse with the value specified for the line voltage selected.

WARNING

Only fuses with the required rated current, voltage, and specified type should be used. Do not use repaired fuses or short-circuited fuse holders. To do so could cause a shock or fire hazard.

CAUTION

Always be sure that the voltage select switch is set to correspond to the ac power input voltage, or the counter may be damaged.

AIR CIRCULATION

Air circulates through the vents in the rear panel of the counter. These vents must not be obstructed or the temperature inside the counter may increase enough to reduce counter stability and shorten component life.

PERIODIC MAINTENANCE

No periodic maintenance is required. To maintain accuracy, it is recommended that the counter be recalibrated every six months.

If the following assemblies are repaired or replaced, the counter may require recalibration for proper operation.

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Section 5
Maintenance and Service

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MAINTENANCE

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The Model 545A/548A Microwave Counter uses one fuse; it is located on the rear panel next to the voltage select switch.

- For 100/120 Vac operation use a 1.0-A slow-blow MDL-type fuse.
- For 220/240 Vac operation use a 0.50-A slow-blow FST-type fuse.

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WARNING

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1. With a flat-edged screw driver, rotate the voltage select switch until the arrow points to the desired line voltage.
2. Change to a fuse with the value specified for the line voltage selected.

WARNING

Only fuses with the required rated current, voltage, and specified type should be used. Do not use repaired fuses or short-circuited fuse holders. To do so could cause a shock or fire hazard.

CAUTION

Always be sure that the voltage select switch is set to correspond to the ac power input voltage, or the counter may be damaged.

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Air circulates through the vents in the rear panel of the counter. These vents must not be obstructed or the temperature inside the counter may increase enough to reduce counter stability and shorten component life.

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No periodic maintenance is required. To maintain accuracy, it is recommended that the counter be recalibrated every six months.

If the following assemblies are repaired or replaced, the counter may require recalibration for proper operation.

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- o Power Supply (A101)
- o Gate Generator (A107)
- o Converter Control (A108)
- o Microwave Converter (A102)

Care should be taken when removing any assemblies to prevent damage to components or cables.

CAUTION

Do not attempt repair or disassembly of the Microwave converter (A203) or Time Base Oscillator (A204)assemblies. Opening the sealed covers of these assemblies voids the warranty on the counter. Contact EIP or your sales representative.

SERVICE

DISASSEMBLY, REPAIR, REPLACEMENT, AND REASSEMBLY

GENERAL INSTRUCTIONS

To perform repairs on the 545A/548A printed circuit boards listed in the procedures below, you will need to open the counter by removing the top and/or bottom covers. The top cover may be removed by loosening the six screws that secure it to the counter frame. The bottom cover is held in place to the bottom of the frame by four screws.

Refer to Figure 5-1, Counter Assembly Locations, on page 5-9, for the names and locations of parts and assemblies described in this procedure. Numbers referred to in brackets [ ] in these procedures are keyed to the numbers in Figure 5-1. Cables are referred to by their reference designators (W-) so that they can be located in Figure 5-1. Cables are further identified by their EIP part numbers (2040XXX-01) because these part nmbers are printed on the cables themselves. The format in which socket J1 on the A101 baord is referred to as A101J1 is used throughout this procedure.

WARNING

Before proceeding with any further disassembly, be sure the counter is disconnected from the ac power source. Voltages as high as 230 Vac may exist in the counter. Serious injury or DEATH may result from contact with these potentials.

A101 POWER SUPPLY

Disassembly

1. To remove the A101 board, both top and bottom covers must be removed. Take off the top cover by removing the six screws that secure it to the counter frame [1]. Turn tecounter over and take off the bottom cover by loosening the four screws that hold the bottom cover to the frame.

2. With the counter still up side down, unscrew the four screws that hold the A101 board to the Main Interconnect board (A110).

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3. Return the counter to the upright position. Disconnect from J1 on the A101 board the connector attached to the W6 cable from the transformer (T1).

4. Lift the board extractors [2] away from the center of the board to unlock the board from the card guides [3] and remove the board from the counter.

Reassembly

1. To reassemble, thread the board into the card guides [3], and press it down about an inch.

2. Attach the connector for the W6 cable to A101J1.

2. Press the board down the rest of the way until it is seated.

3. Flip the board extractors [2] down to lock the board into position.

4. Screw in the four screws that attach the A101 board to the Main Interconnect (A100) board from the bottom.

A102 (OPTION 08, GPIB)

If your instrument is equipped with Option 08, GPIB programming capability, the GPIB board will be present in the A102 slot.

Disassembly

1. Lift the board extractors [2] away from the center of the A102 board to unlock it from the card guide [3].

2. Slide the board up and remove from the counter.

Reassembly

1. To reassemble, thread the board into the card guides [3], and press it down until it is seated.

2. Flip the board extractors [2] down to lock the board into position.

A105 MICROPROCESSOR

Disassembly

1. Lift the board extractors [2] away from the center of the A105 board to unlock it from the card guide.

2. Slide the board up and remove from the counter.

Reassembly

1. To reassemble, thread the board into the card guides [3], and press it down until it is seated.

2. Flip the board extractors [2] down to lock the board into position.

A106 COUNT CHAIN

Disassembly

1. Lift the board extractors [2] away from the center of the board to unlock it from the card guide.

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2. Slide the board up about an inch until the cables can be disconnected.
3. Disconnect from A106J1 the connector for the W15 cable (2040210-01) from A109J5.
4. Disconnect from A106J2 the connector for the W14 cable (2040172-01) from A201J1.
5. Lift the board up and out of the instrument.

Reassembly

1. To reassemble, thread the board into the card guides [3], and lower it about an inch.
2. Reconnect cable 2040210-01 to A106J1.
3. Reconnect cable 2040172-01 to A106J2.
4. Press the board the rest of the way down until it is seated.
5. Flip the board extractors [2] down to lock the board into position.

A107 GATE GENERATOR

Disassembly

1. Lift the board extractors [2] away from the center of the board to unlock it from the card guide.
2. Slide the board up until the cables can be disconnected.
3. Disconnect from A107J1 the connector for the W8 cable (2040173-01) from A201J4.
4. Disconnect from A107J3 the connector for the cable (2040227-01) from A108J3.
5. If your instrument is equipped with Option 03/04/05, Time Base Oscillator, disconnect from A107J2 the connector for the W30 cable (2040179-01) from A114,the optional time base oscillator and J6 (not shown) on the Main Interconnect (A100) board) .
6. Lift the board up and out of the instrument.

Reassembly

1. To reassemble, thread the board into the card guides [3], and lower it about an inch.
2. Reconnect cable 2040173-01 to A107J1.
3. Reconnect cable 2040227-01 to A107J3.
4. Reconnect cable 2040179-01 (if present) to A107J2.
5. Press the board the rest of the way down until it is seated.
6. Flip the board extractors [2] down to lock the board into position.

A108 CONVERTER CONTROL (BAND 3)

Disassembly

1. Lift the board extractors [2] away from the center of the board to unlock it from the card guide.
2. Slide the board up about an inch until the cables can be disconnected.

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3. Disconnect from A108J1 the connector for the W6 cable (2040208-01) from A109J3.
4. Disconnect from A108J2 the connector for the W9 cable (2040174-01) from A201J3.
5. Disconnect from A108J3 the connector for the cable (2040227-01) from A107J3.
6. Lift the board up and out of the instrument.

Reassembly

1. To reassemble, thread the board into the card guides [3], and lower it about an inch.
2. Reconnect cable 2040208-01 to A108J1.
3. Reconnect cable 2040174-01 to A108J2.
4. Reconnect cable 2040227-01 to A108J3.
5. Press the board the rest of the way down until it is seated.
6. Flip the board extractors [2] down to lock the board into position.

A109 BAND 2 CONVERTER

Disassembly

1. Lift the board extractors [2] away from the center of the board to unlock it from the card guide [3].
2. Lift off clip [10] that is attached to card cage edge from A109 board.
2. Slide the board up about an inch until the cables can be disconnected.
3. Disconnect from A109J1 the connector for the W17 cable (2040175-01) from A201J2.
4. Disconnect from A109J3 the connector for the W16 cable (2040208-01) from A108J1.
5. Disconnect from A109J4 the connector for the W11 cable (2040166-01) from J112 (Band 2 input on the front panel).
6. Disconnect from A109J5 the connector for the W15 cable (2040210-01) from A106J1.
7. Disconnect from A109J6 the connector for the W10 cable (2040165-01) from J111 (Band 1 input on the front panel).
8. If the instrument is a 548A equipped with option 06, Extended Frequency (Band 4), disconnect from A109J2 the connector for the W27 cable (2040213-01) from P1 on the Option 06 (Band 4 Converter) assembly.
9. Lift the board up and out of the instrument.

Reassembly

1. To reassemble, thread the board into the card guides [3], and lower it about an inch.
2. Reconnect cable 2040175-01 to A109J1.
3. Reconnect cable 2040208-01 to A109J3.
4. Reconnect cable 2040166-01 to A109J4.

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5. Reconnect cable 2040210-01 to A109J5.

6. Reconnect cable 2040165-01 to A109J6.

7. If present, reconnect cable 2040213-01 to A109J2.

8. Press the board the rest of the way down until it is seated.

9. Flip the board extractors [2] down to lock the board into position.

A111 FRONT PANEL LOGIC

Disassembly

1. With top cover off, remove two screws [8] holding front black bracket (5210235-01) [4] to front edge of counter frame.

2. Remove two more screws [9] that hold front panel assembly (consisting of front panel overlay [5], Front Panel Display and Keyboard A110 board, and Front Panel Logic A111 board) to front edge of frame.

3. With the bottom cover off, remove four screws (in positions corresponding to the top screws) that hold front panel assembly to bottom of front edge of counter frame.

4. Loosen eight screws [6] (two on top of right corner post, two on top of left corner post, two on bottom of right corner post and two on bottom of left corner post) that hold front panel board to side panels.

5. Pull side panels [7] apart slightly and pull boards forward and free of side panels so that cable connectors can be disengaged.

6. Disconnect from A11J5 the W19 cable (2040168-01) from transistor U14 on support bracket [8].

7. Disconnect from A111J4 the W20 cable (2040168-00) from R101 (Sample/Hold control) on front panel.

8. Disconnect W1 cable (2010189-01) from power switch assembly (S101) on front panel.

9. Disconnect *at A109/Band 2 Converter board end* W10 cable (2040165-01) for Band 1 from J6A109 and W11 cable (2040166-01) for Band 2 from J4A109. *These cables must stay with the A111 board.*

10. Disconnect from A111P2 the W7 cable (2040169-01) from J1 on A100 (Main Interconnect board).

11. If instrument is a 548A equipped with Option 06, extended frequency, disconnect *at A204 Band 4 Converter end* the W28 cable (2040231-01) from J1A204 and the W29 cable (2040232-01) from J2A204. *These cables must stay with the A111 board.*

A110 FRONT PANEL DISPLAY AND KEYBOARD

To gain access to the A110 (Front panel Display and Keyboard) board, it is necessary to separate the Front Panel Logic (A111) board from the Front Panel Display (A110) board.

1. Unscrew the eight screws (four on the upper edge and four on the lower edge) that hold the A110 and A111 boards and the front panel overlay together and lift the boards from the front panel.

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2. Then unscrew a ninth screw (about halfway down on the left side of the boards) that holds the A110 and A111 boards together.

3. Gently separate the two boards.

Reassembly of A110 to A111

1. To reassemble Front Panel Logic (A111) board to Front Panel Display and Keyboard (A110) board and front panel overlay, replace A111 on A110 as it was when removed from the counter.

2. Secure with screw at center of left edge of both boards.

3. Secure both boards to front panel overlay with eight screws (four on upper edge and four on lower edge).

Reassembly of A110, A111, and Front Panel Overlay to Counter

1. To reassemble front panel assembly to counter, position the front panel assembly just outside of its normal position in the counter so that the cables can be reattached.

2. Reconnect W20 cable 20401342-01 to A111J4.

3. Reattach W19 cable 2040168-01 to A111J5.

4. Reconnect W1 cable 2040167-01 to S101.

5. Reconnect W10 cable 2040165-01 to A109J6.

6. Reconnect W11 cable 2040166-01 to A111J1.

7. Reconnect W7 cable 2040169-01 to A100J1.

8. If the instrument is a 548A with Option 06, reconnect W28 cable (2040231-01) and W29 cable (2040232-01) from Band 4 Converter to A111J1 and A111J2 respectively.

9. Spread the side panels [7] slightly to allow the front panel assembly to be inserted in its proper position.

10. Tighten the two screws [6] on the top of the left corner post, the two screws [6] on the top of the right corner post and the two screws each on the bottom right and left corner posts that hold the front panel boards to the side panels.

11. Secure front panel assembly (consisting of front panel overlay, front panel display and keyboard board and front panel logic board) to top of front edge of frame with two screws [9].

12. Secure black bracket [4] (5210235-01) to front panel assembly with two screws [8].

13. Secure front panel assembly to bottom of front edge of counter frame with four screws in positions corresponding to screws in top of frame.

FACTORY SERVICE

If the counter is being returned to EIP for service or repair, be sure to include to include the following information with the shipment. Pack the counter for shipping per instructions in Section 2.

1. Name and address of owner.

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2. Model and complete serial number of counter.

3. Complete description of the problem (Under what conditions did the problem occur? What was the signal level? What equipment was attached or connected to the counter? Did that equipment experience failure symptoms?).

4. Name and telephone number of someone familiar with the problem who may be contacted by EIP for further information, if necessary.

5. Shipping address to which the counter is to be returned. Include any special shipping instructions.

FIELD SERVICE

EIP has an assembly exchange program. All plug-in assemblies, modules, and the front panel assembly may be exchanged.

After you have identifed a faulty assembly, call EIP with the assembly number and shipping information. A replacement can be shipped within 24 hours. After you have received the replacement assembly, return the faulty assembly to EIP for credit.

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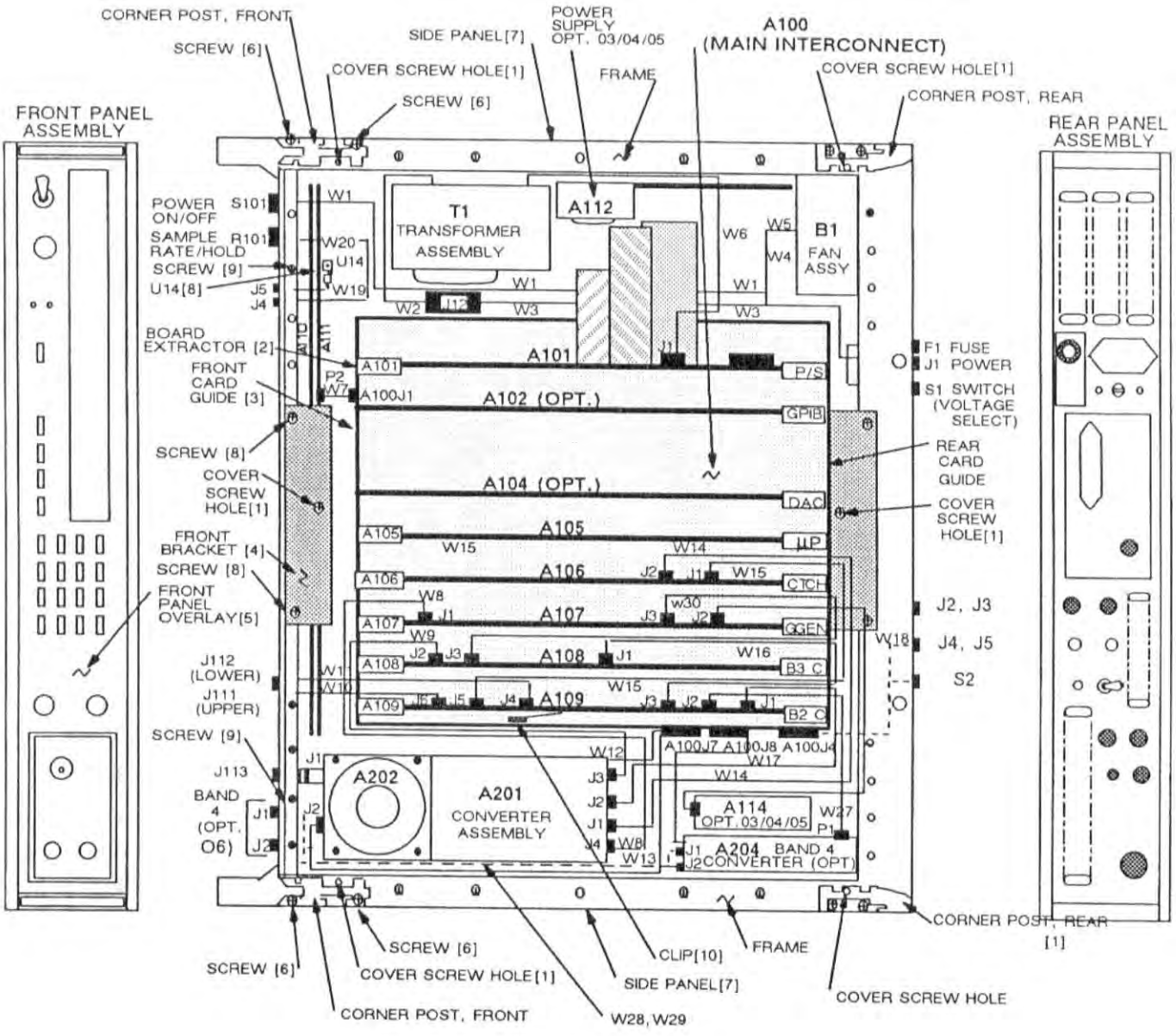


Figure 5-1. Counter Assembly Locations

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Section 6
Troubleshooting

This section defines troubleshooting aids that are incorporated in the 5545A/548A counter. They are:

- Signature analysis
- Self diagnostics
- Keyboard controlled circuit tests

The procedures and tables are provided for troubleshooting to a functional circuit level.

SIGNATURE ANALYSIS

Signature analysis is a technique used to troubleshoot complex logic circuitry. It uses data compression to reduce any data pattern to a 4 character alpha-numeric word.

The start and stop inputs define the measurement window. Each time a transition within the measurement window occurs on the clock input, the probe is sampled, and the logic level is shifted into the analyzer. This information is used to generate a signature unique to that data string. That signature can then be compared to a reference signature, taken from a known good product, to determine if the data string is correct. The counter implements signature analysis in either a free running or program controlled manner.

FREE RUNNING

This mode of signature analysis is essential for troubleshooting problems that could prevent the program from running. A CLRB instruction can be forced by breaking the data bus at A105 E1 and placing it in socket A105 E2, effectively "free running" the microprocessor. "Free running" means forcing a simple instruction (such as NOP or CLRB) on the data bus, which the microprocessor sees at every address location. This causes the microprocessor to continually cycle through its entire address range, accessing everything on the address bus as it does. By strategically placing the start and stop connections the entire bus system can be probed for bad signatures.

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	START	STOP	CLOCK
CONNECTIONS	A105 TP4	A105 TP4	A105 TP3
BUTTONS	IN	IN	IN

LINE	SIGNATURE	LINE	SIGNATURE
A0 (P1 Pin 54)	UUUU		
A1 (P1 Pin 54)	FFFF		
A2 (P1 Pin 53)	8484		
A3 (P1 Pin 51)	P763		
A4 (P1 Pin 50)	1U5P		
A5 (P1 Pin 49)	0356		
A6 (P1 Pin 48)	U759		
A7 (P1 Pin 47)	6F9A		
A8 (P1 Pin 46)	7791		
A9 (P1 Pin 45)	6321		
A10 (P1 Pin 44)	37C5		
A11 (P1 Pin 43)	6U28		
A12 (P1 Pin 42)	4FCA		
A13 (P1 Pin 41)	4868		
A14 (P1 Pin 40)	9UP1		
A15 (P1 Pin 39)	00001		
U3 Pin 7	76AC		
U5 Pin 8	0000		
TP6	854F		
TP7	PACH		
TP8	755F		
TP9	755H		
U8 Pin 19	U3P7		
U9 Pin 18	0003		
U10 Pin 18	0003		
U17 Pin 1	9F14		
U17 Pin 2	9F17		

+ 5V 0003, phase 2 0003 *

* Due to the synchronous qualities of the signature analyzer, phase 2 will read the same as + 5V but the logic probe will be flashing. Likewise, anything gated with phase 2 may have the same signature as the ungated signal.

Figure 6-1. Microprocessor Free Running Signatures

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PROGRAM CONTROLLED

If the counter is working sufficiently to access the test functions, program controlled signature analysis can be used. In program controlled signature analysis the start and stop (and therefore the signature) are controlled by software. This allows the signature analyzer to be used, in many cases, to troubleshoot the hardware outside the bus system.

SELF DIAGNOSTICS

At turn-on, the counter performs several internal diagnostic checks, checking the RAM, PROM, and the associated decoding circuitry. The display shows dashes during these checks. If the counter passes the tests it then enters the normal operating mode. If it fails RAM check, the display will show all Es. If the counter fails any of the PROM checks, an error message will be displayed. Please refer to Figure 6-2.

The counter generates PROM error signatures only during the power up diagnostics check. It is necessary to turn the power off, and then on again, while the signature analyzer is connected, to get a signature.

	START	STOP	CLOCK	PROBE
CONNECTION BUTTONS	A106 TP5 OUT ↑	A106 TP5 IN ↓	A105 TP8 IN ↓	A105 TP6 (+5V)

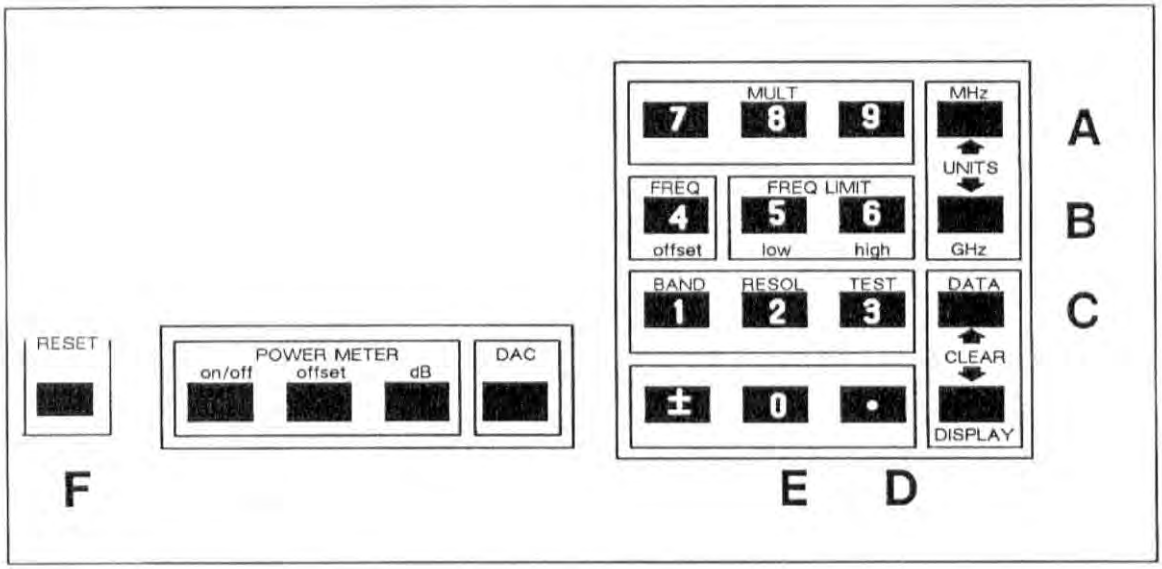
PROBLEM	ERROR	SIGNATURE
Ram Bad	All E's	
A105 U11 (Basic Program) Bad	31	
A105 U12 (Basic Program) Bad	32	
A105 U13 (Basic Program) Bad	33	

Figure 6-2. Self Diagnostic Error Indications

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KEYBOARD CONTROLLED CIRCUIT TESTS

There are 11 keyboard controlled circuit tests (01 thru 11). All tests are accessed by pressing TEST and then the two digit test number. Tests which do not require keyboard inputs to function (tests 01, 02, 03, 04, 06, 07, 11) can be exited by pressing any key. The counter will exit the test and enter the functions selected. Tests which use the keyboard in their operation (tests 05, 08, 09, 10) can be exited by pressing any key not used by the test. All tests can be exited by pressing CLEAR DISPLAY. The counter will return to normal operation. Some tests require hexidecimal coded keyboard inputs (tests 08, 09, 10). For those tests the keyboard is defined in figure 6-3.



KEY	HEX EQUIV.	KEY	HEX EQUIV.
0	0	9	9
1	1	MHz	A
2	2	GHz	B
3	3	CLR DATA	C
4	4		
5	5	•	D
6	6	+/–	E
7	7	RESET	F
8	8	CLR DISPLAY	EXITS TEST

Figure 6-3. Keyboard Configuration For Tests Requiring Hexadecimal Inputs.

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	START	STOP	CLOCK	PROBE
CONNECTION	OUT ↑	IN ↓	IN ↓	
BUTTONS	A106 TP5	A106 TP5	A105 TP8	A105 TP6 (+5V)

BUTTON	COORDINATES	SIGNATURE
Reset	47	U68C
Power Meter ON/OFF	46	U7HA
Power Meter Offset	36	20P6
dB	16	U2F9
DAC	26	811P
7	41	A19C
8	42	66PU
9	43	CCH7
MHz	44	U5PU
4	31	PUPH
5	32	UC70
6	33	HF3A
GHz	34	OPA2
1	21	APH1
2	22	C45H
3	23	1766
CLR DATA	24	H9C8
+/–	11	375U
0	12	H7PC
•	13	UAHH
CLR DISPLAY	EXIT TEST	C75U

Figure 6-4. Keyboard Test Coordinates and Signatures.

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TESTS

01 200 MHz Self Test This test sets the VCO to 400 MHz, divides it by two, and counts the 200 MHz output from the divider. It checks the count chain, VCO and VCO phase lock circuitry, and the gate generator.

02 8's Test This will light all LED's, annunicators, and decimal points. It checks that everything on the display is lit, the intensity of the display, and the alignment of the LED's and annunciators.

03 Display Segment Test This lights one segment of each digit, and one annunciator at a time, cycling through all segments. The cycle rate can be adjusted with the sample rate pot. It verifies that each segment of the display, segment drivers and display multiplexer operate properly and independently.

04 Display Digit Test This lights one entire digit, and its decimal point, at a time. It cycles through all digits and annunciators. The cycle rate is determined by the sample rate pot. It checks each digit and digit driver independently, and verifies operation of the display multiplexer.

05 Keyboard Test This will display the coordinates of each key as it is pressed. It also generates a unique signature for each key, so the keyboard can be checked without the display. Test 05 may be entered by keyboard or by momentarily tying A108 TP1 to A105 TP6. This makes it possible to enter the keyboard test for troubleshooting even if the keyboard is not operating well enough to enter the test in a normal manner. Test 05 checks the keyboard, keyboard interrupt, and keyboard decode circuitry. The coordinates and signatures for each key are shown in figure 6-4.

06 Converter Ramp Test Test 06 continuously ramps the Band 3 Converter DAC from 0 to 27 GHz, in 2 MHz (LSB) steps. It also generates a signature for each of the inputs to the DAC. (See figure 6-5). It can be used to test the yig DAC, yig drivers, yig, and Band 3 RF level circuits.

	START	STOP	CLOCK
CONNECTIONS	A106 TP5	A106 TP5	A105 TP8
BUTTONS	OUT ↑	IN ↓	IN ↓

NODE	SIGNATURE	NODE	SIGNATURE
A108 U4 Pin 2	9U78	A108 U4 Pin 9	7763
A108 U4 Pin 3	9946	A108 U4 Pin 10	HP8A
A108 U4 Pin 4	8F62	A108 U4 Pin 11	P45A
A108 U4 Pin 5	89U9	A108 U4 Pin 12	80A8
A108 U4 Pin 6	833F	A108 U4 Pin 13	77U6
A108 U4 Pin 7	U9CC	A108 U4 Pin 14	7245
A108 U4 Pin 8	FCA6	A108 U4 Pin 15	28U9
+5V	49P4		

Figure 6-5. Converter Ramp Test Signatures

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07 **VCO Test** This test cycles the VCO frequency from 400 to 500 MHz, in increments of 50 kHz. The cycle rate can be adjusted by the sample rate pot. 07 tests the VCO and the phase lock circuitry.

08 **Power Meter Offset Test** This makes it possible to set the power meter zero DAC to any setting. The setting is entered as a four digit hexidecimal number (figure 6-5). The first two digits are used to program the course offset DAC, and the last two digits program the fine offset DAC. Test 08 enables the power meter zero DAC to be tested, and can provide a DC level signal to aid in testing the power meter circuit.

09 **Power Meter Gain Test** This makes it possible to set the power meter sensing circuit to any number. The number is entered as a five digit hexidecimal number (figure 6-5) in the following format.

1st digit	A107 U10 bits 4-7
2nd digit	A107 U10 bits 0-3
3rd digit	A107 U12 bits 4-7 (Power Meter Option only)
4th digit	A107 U12 bits 0-3 (Power Meter Option only)
5th digit bit 0	Sets Amp marked "15 dB Gain" to high gain
5th digit bit 1	Sets Amp marked "30 dB Gain" to high gain

Digit 5 is a 2 bit number, so any number entered for digit 5 will be justified to a number from 0-3. Test 09 checks the RF level and power meter circuits.

10 **Information Read/Alter Routine** Test 10 can read any microprocessor address and, if that address is RAM or I/O, change its contents. The desired address is entered as a 4 digit hexidecimal number (see figure 6-5). When the 4th digit is entered the counter will display the contents of the desired address. The contents are then changed by entering a two digit hexidecimal number.

NOTE

Test 10 can change any temporary storage in the counter, including locations that are essential to the operation of the counter. Changing the wrong location will not damage the counter permanently, but it can cause improper operation. To return the counter to proper operation turn the counter off then back on.

11 Test 11 for the DAC option 01 is described in Section 10.

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SIGNIFICANT ADDRESSES, I/O PORTS

If an I/O bit is configured as an output, the number read by test 10 will be the same number that is programmed. If an I/O bit is configured as an input, the number read by test 10 will be the input signal level on the I/O line. Therefore, if an I/O port is programmed, and then read, the number displayed may not correspond to the number programmed because some bits of the I/O port may be configured as inputs.

DESCRIPTION	ADDRESS OF PA PORTS	ADDRESS OF PB PORTS
PIA on Count Chain (A106)	2C00	2C02
PIA on Gate Generator (A107)	1900	1902
Frequency Control PIA on Converter Control (A108)	1840	1842
Programmable Counter PIA on Converter Control (A108)	1820	1822
PIA on Band 2 Converter (A109)	1880	1882
PIA on Front Panel Logic (A111)	1808	180A
PIA on BCD/Remote (A102)	9A00	9A02
PIA on DAC Board (A103)	A820	A822

DESCRIPTION	ADDRESS
GPIB Address Switch	1C04

Figure 6-6. I/O Addresses.

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Two important I/O port locations are the yig frequency control (address 1840, 1842) and the VCO frequency control (address 1820, 1822).

To convert from the desired yig frequency to the PIA program number:

1. Round the desired frequency to a multiple of 2 MHz (The yig DAC resolution is 2 MHz).
2. Divide the desired frequency in MHz by 2 (F/2).
3. Convert F/2 from decimal to hexidecimal.
4. The two most significant digits are programmed to address 1842, and the two least significant digits are programmed to address 1840.

To convert from the desired VCO frequency to the PIA program number:

EXAMPLE (420. 75 MHz)

1. Round the desired frequency to a multiple of 50 kHz
   (The resolution of the VCO frequency is 50 kHz).
2. Multiply the desired frequency (in MHz) by 5. . . . . 420. 75 X 5 = 2103.75
3. If the result contains no fractional part, go to step 8.
4. Multiply only the fractional part by 16 . . . . . .75 X 16 = 12
5. Add the result to the most significant digit from step 2. . . . . MSD of 2103.75 = 2 - 2 + 12 = 14
6. Convert the result to hexidecimal. . . . . $14_{10} = E_{16}$
7. Replace the MSD from step 2 with the result from step 6
   and drop the fractional part. . . . . 2103.75 → E103
8. The two most significant digits are programmed to address 1822, and the two least significant digits are programmed to address 1820.

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SIGNIFICANT ADDRESSES, RAM

All storage in RAM are in the following formats.

REGISTER FORMAT, FREQUENCY STORAGE		
ADDRESS	SIGN (00 = + , FF = –)	
ADDRESS + 1	100 GHz	10 GHz
ADDRESS + 2	1 GHz	100 MHz
ADDRESS + 3	10 MHz	1 MHz
ADDRESS + 4	100 KHz	10 KHz
ADDRESS + 5	1 KHz	100 Hz
ADDRESS + 6	10 Hz	1 Hz

REGISTER FORMAT, POWER STORAGE		
ADDRESS	SIGN (00 = +, FF = –)	
ADDRESS + 1	NOT	USED
ADDRESS + 2	NOT	USED
ADDRESS + 3	NOT	USED
ADDRESS + 4	NOT	USED
ADDRESS + 5	100 dB	10 dB
ADDRESS + 6	1 dB	. 1 dB

REGISTER	ADDRESS
L.O. frequency	01A8
I.F. frequency	023F
Frequency output to display	01B8
Frequency limit low	025B
Frequency limit high	0254
Frequency offset	0246

Figure 6-7. Frequency Storage Registers

REGISTER	ADDRESS
Power output to display	01BF
Power offset	024D

Figure 6-8. Power Storage Registers

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TROUBLESHOOTING TREES

Troubleshooting trees are intended only as a guide, and do not describe every possible failure situation. Turn power off before removing or installing any P.C. boards or connectors. If the following assemblies are repaired or replaced, recalibration of the counter will be necessary.

- A101 Power Supply
- A107 Gate Generator
- A108 Converter Control
- A203 Converter Assembly

CAUTION

Do not attempt to repair or disassemble
the A203 hybrid assembly.

TEST EQUIPMENT REQUIRED

MANUFACTURER	MODEL	DESCRIPTION	CRITICAL PARAMETERS
Tektronix	475	Oscilloscope	100 MHz min. Bandwidth
Fluke	8050A	D.V.M.	4½ digit resolution
H.P.	182C, 8559A	Spectrum Analyzer	125 MHz
H.P.	5004A	Signature Analyzer	
H.P.	651B	Signal Generator	10 Hz - 10 MHz
Wavetek	2002	Sweeper	10 MHz - 2 GHz
EIP	928	Microwave Source	1 GHz - 18.6 GHz
H.P.	8690A, 8696A	Microwave Sweeper	18 GHz - 26. 5 GHz

Figure 6-9. Troubleshooting Test Equipment (Or Equivalent).

To use the troubleshooting trees:

1. Refer to the main troubleshooting tree.

2. Step through the main troubleshooting tree, performing all necessary checks, until the failure mode is noted.

3. Refer to the appropriate troubleshooting tree for that failure mode.

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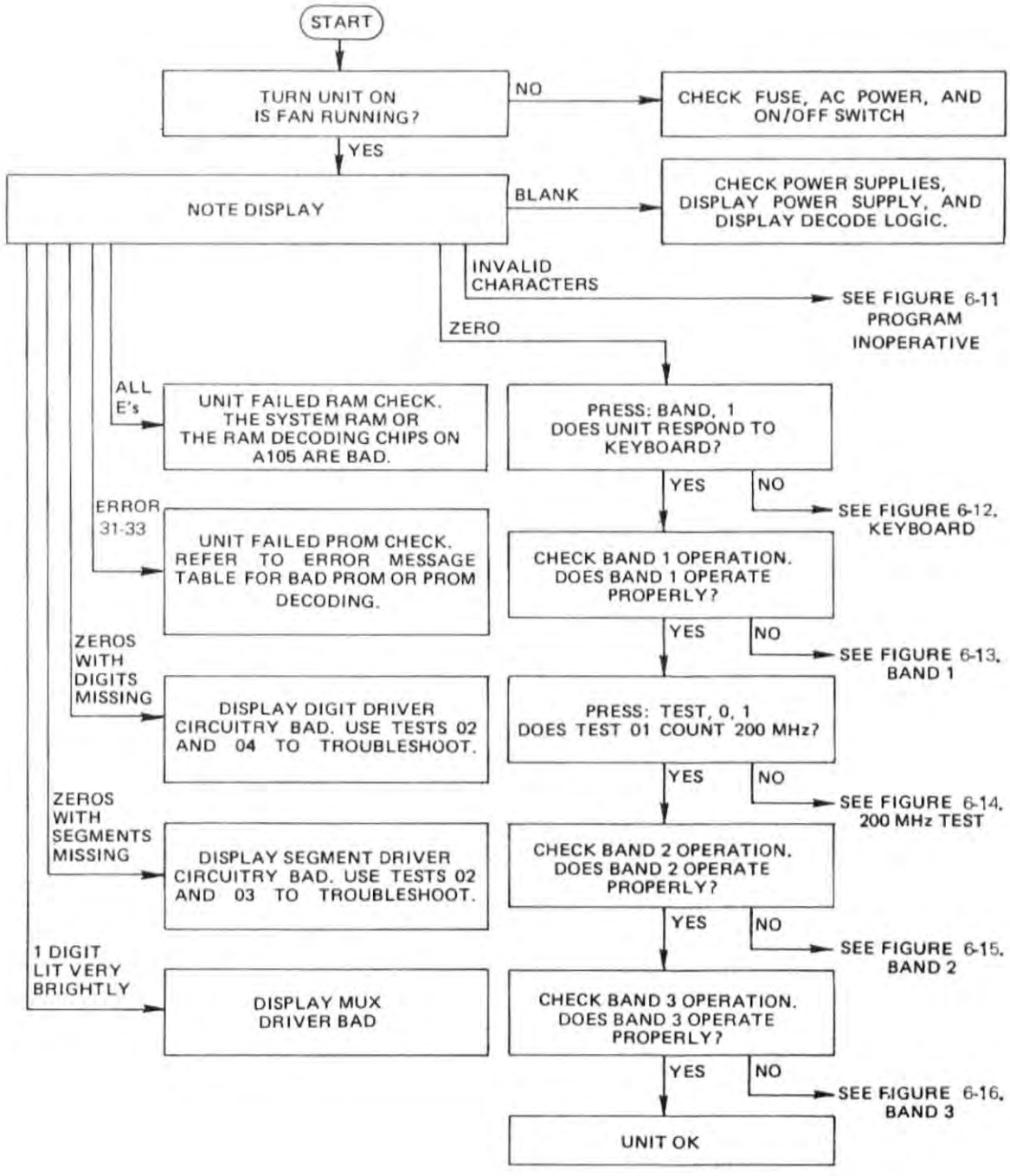


Figure 6-10. Main Troubleshooting Tree

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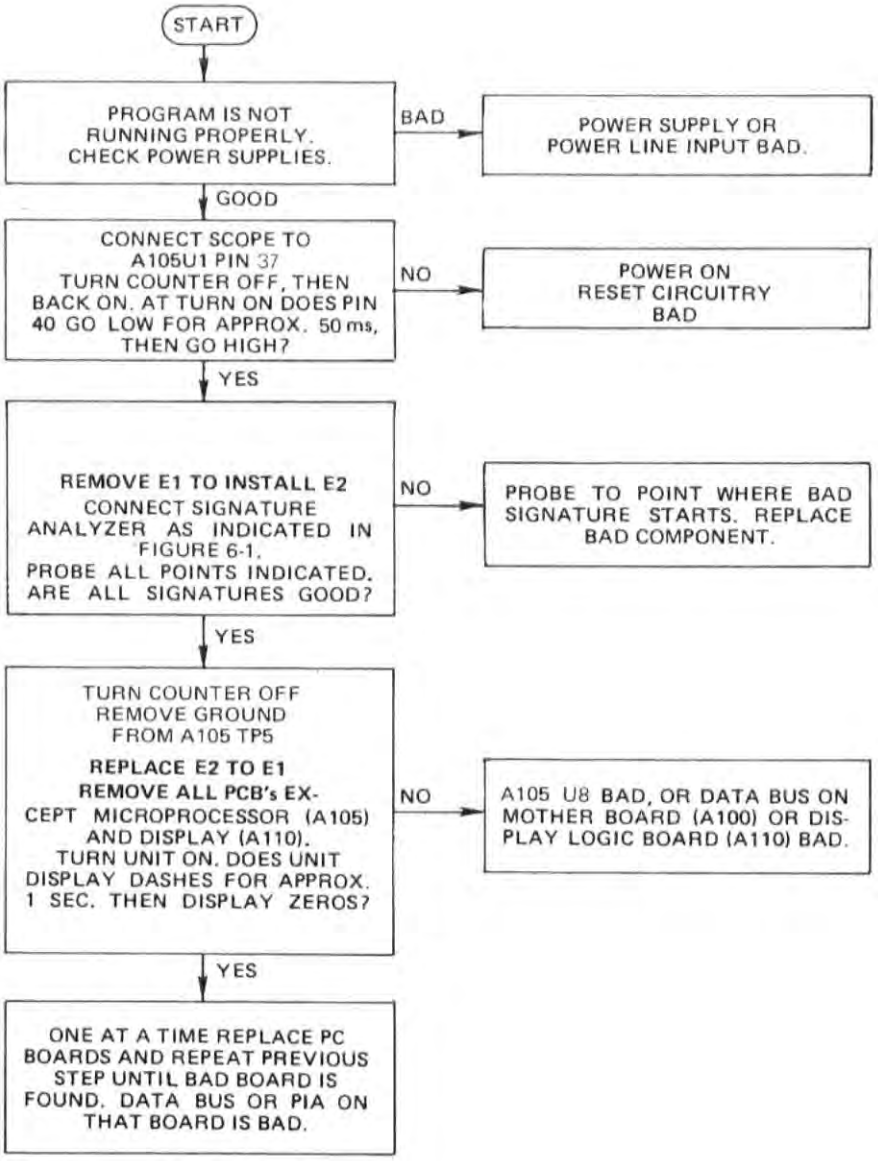


Figure 6-11. Program Inoperative

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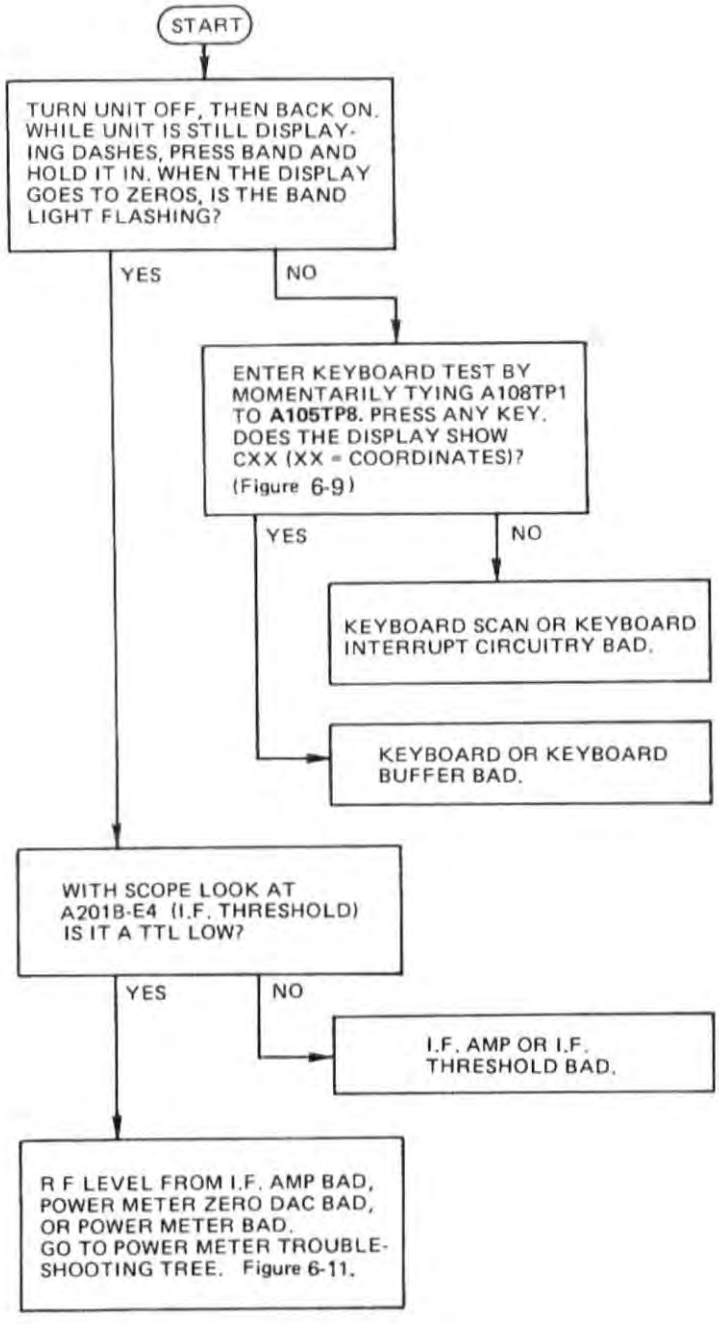


Figure 6-12. Keyboard

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Figure 6-13. Band 1

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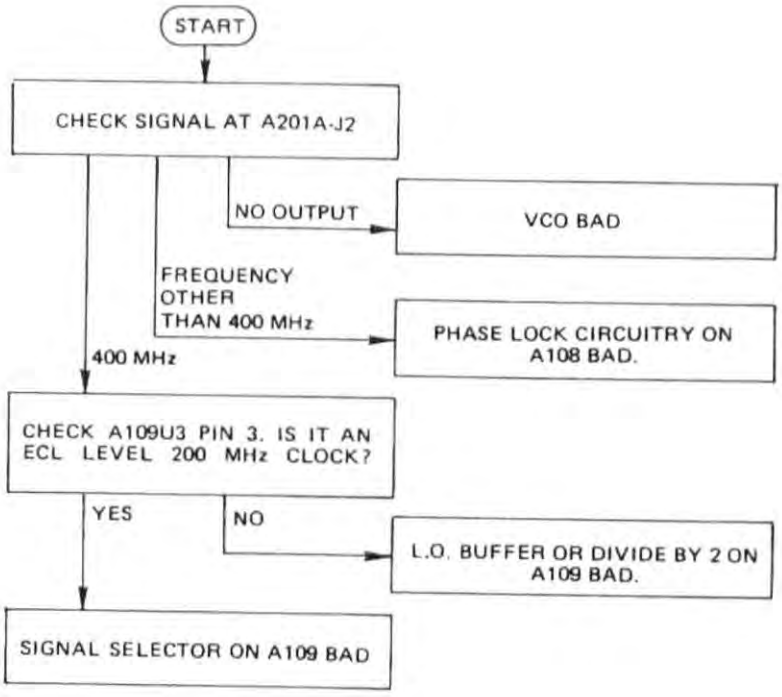


Figure 6-14. 200 MHz Test

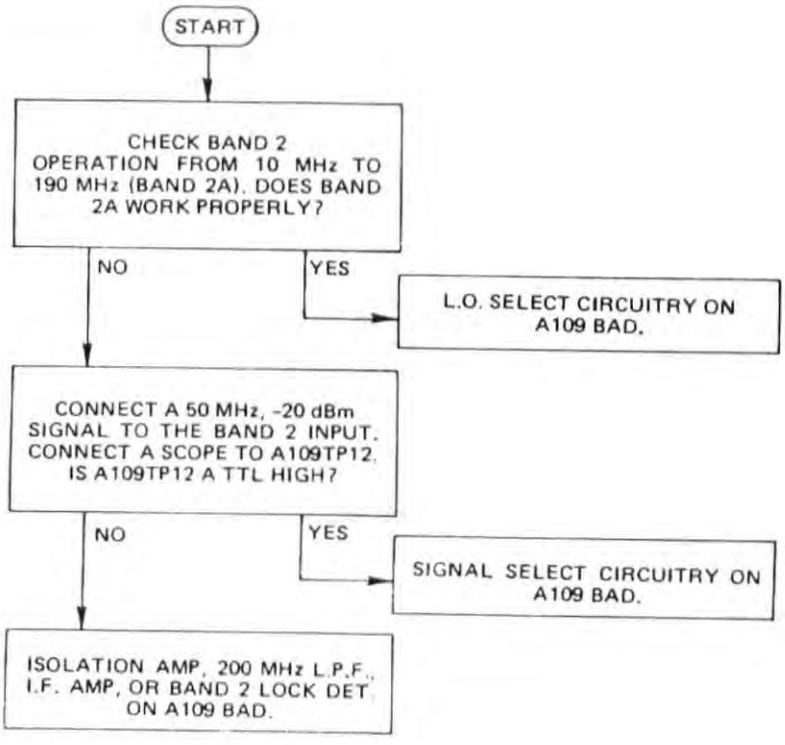


Figure 6-15. Band 2

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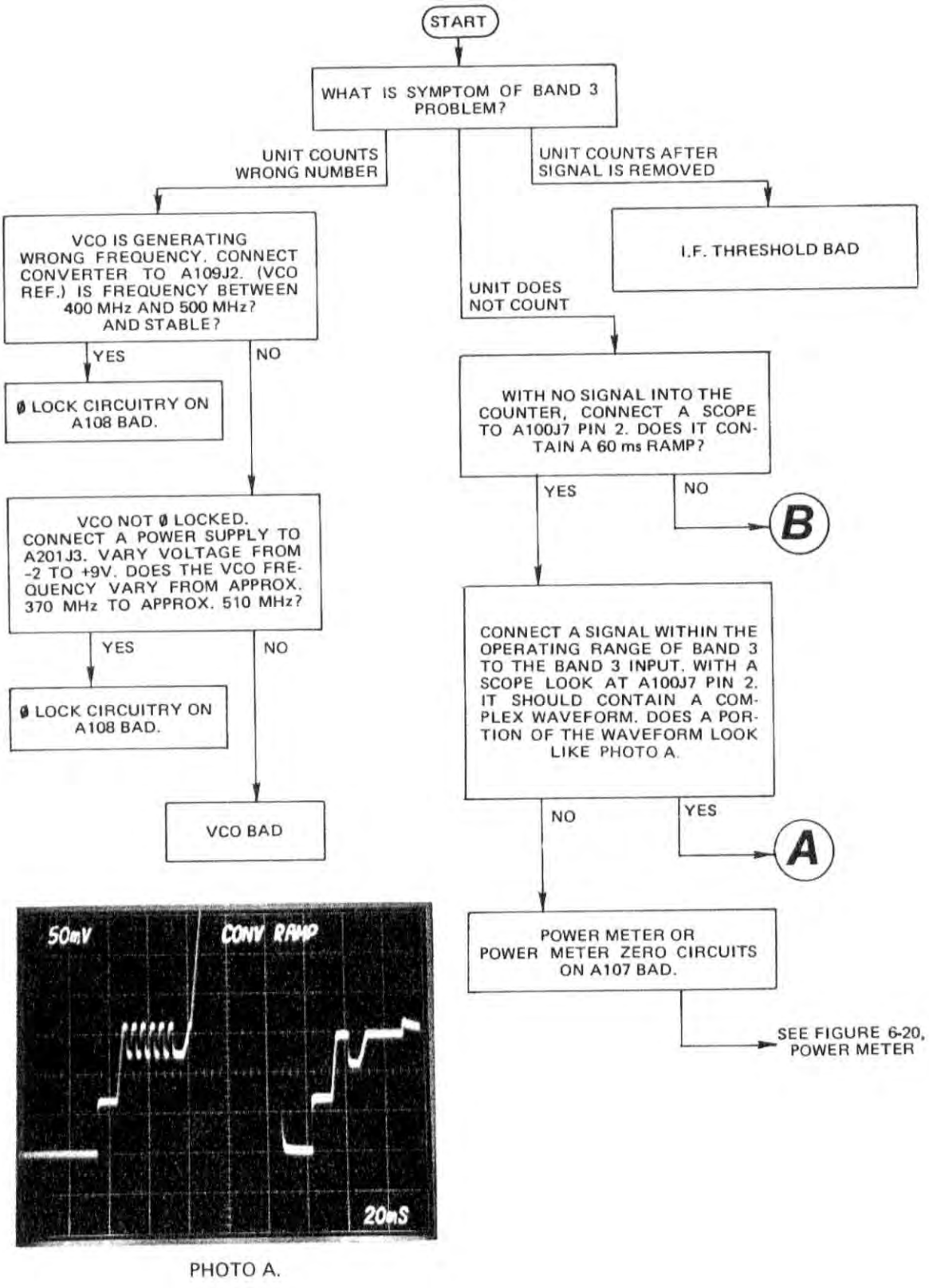


PHOTO A.

Figure 6-17. Band 3

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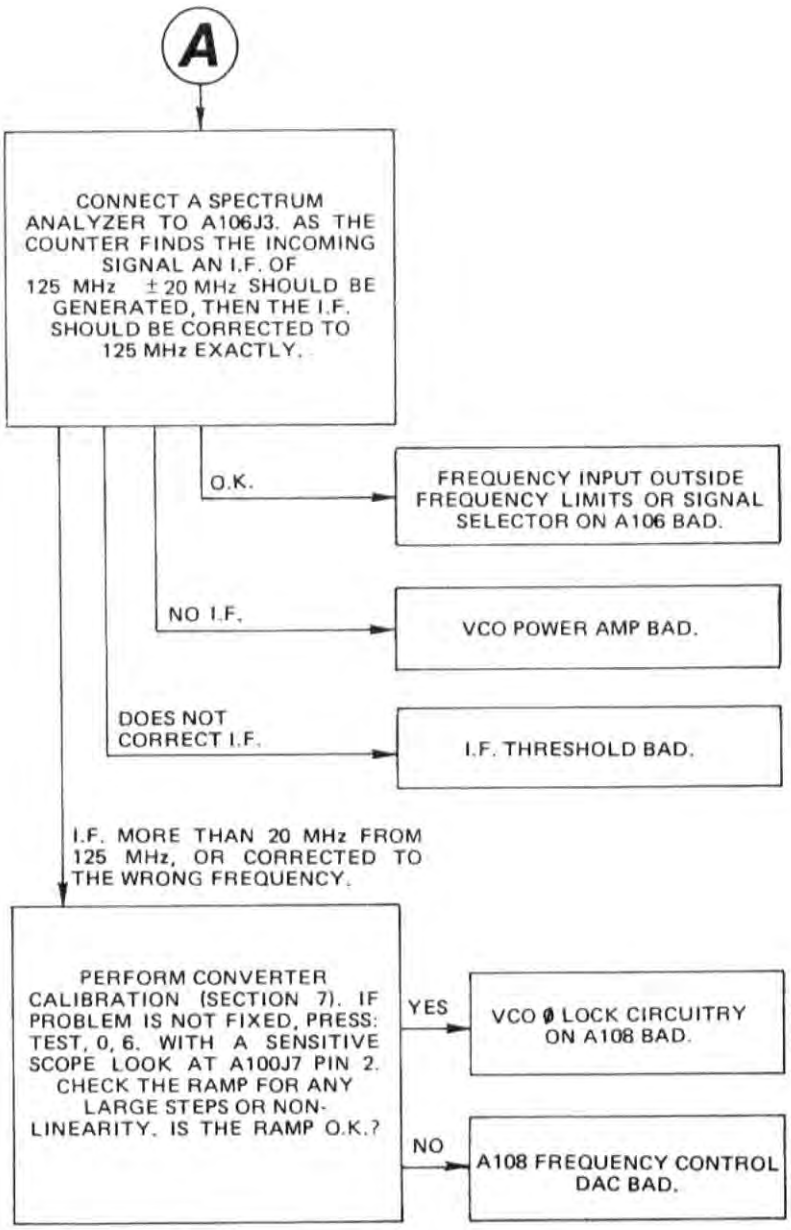


Figure 6-16. Band 3, continued

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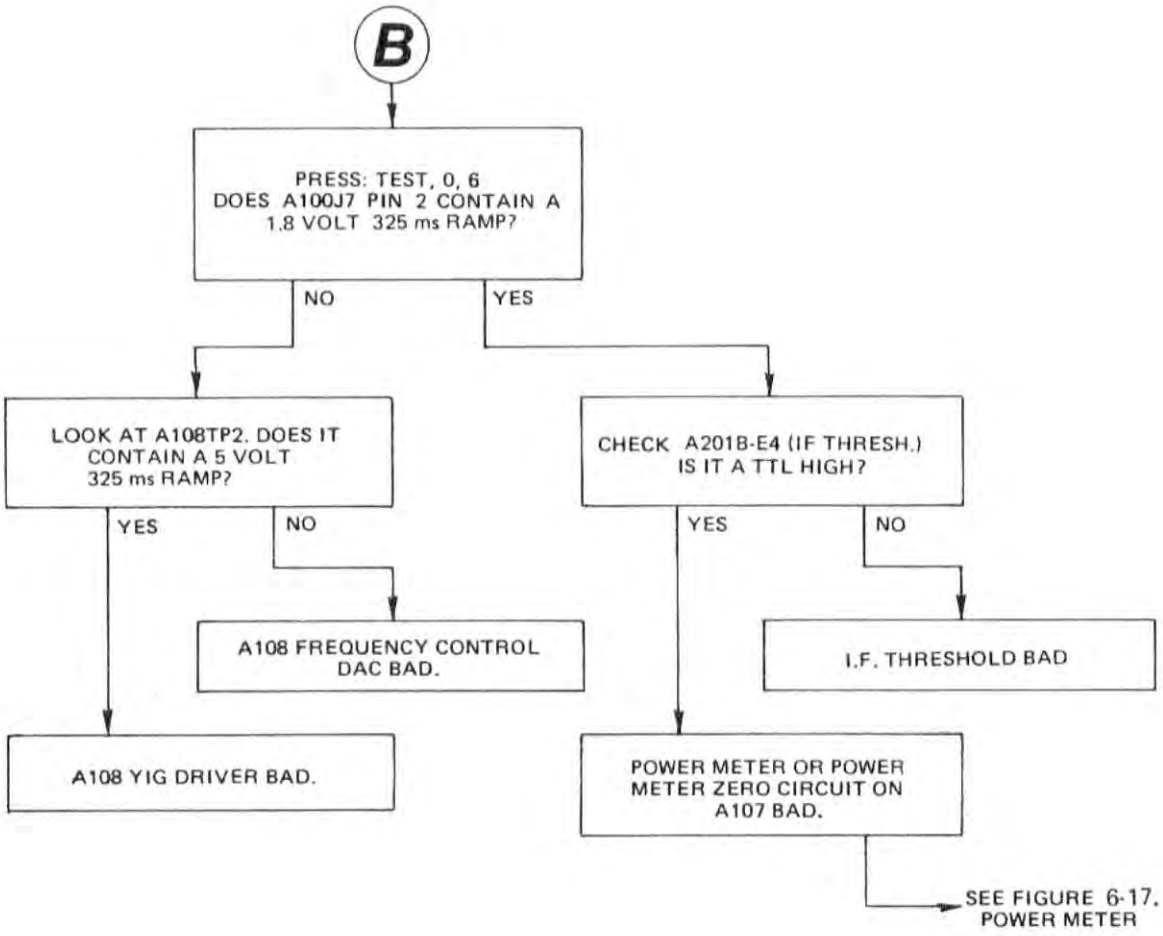


Figure 6-16. Band 3, continued

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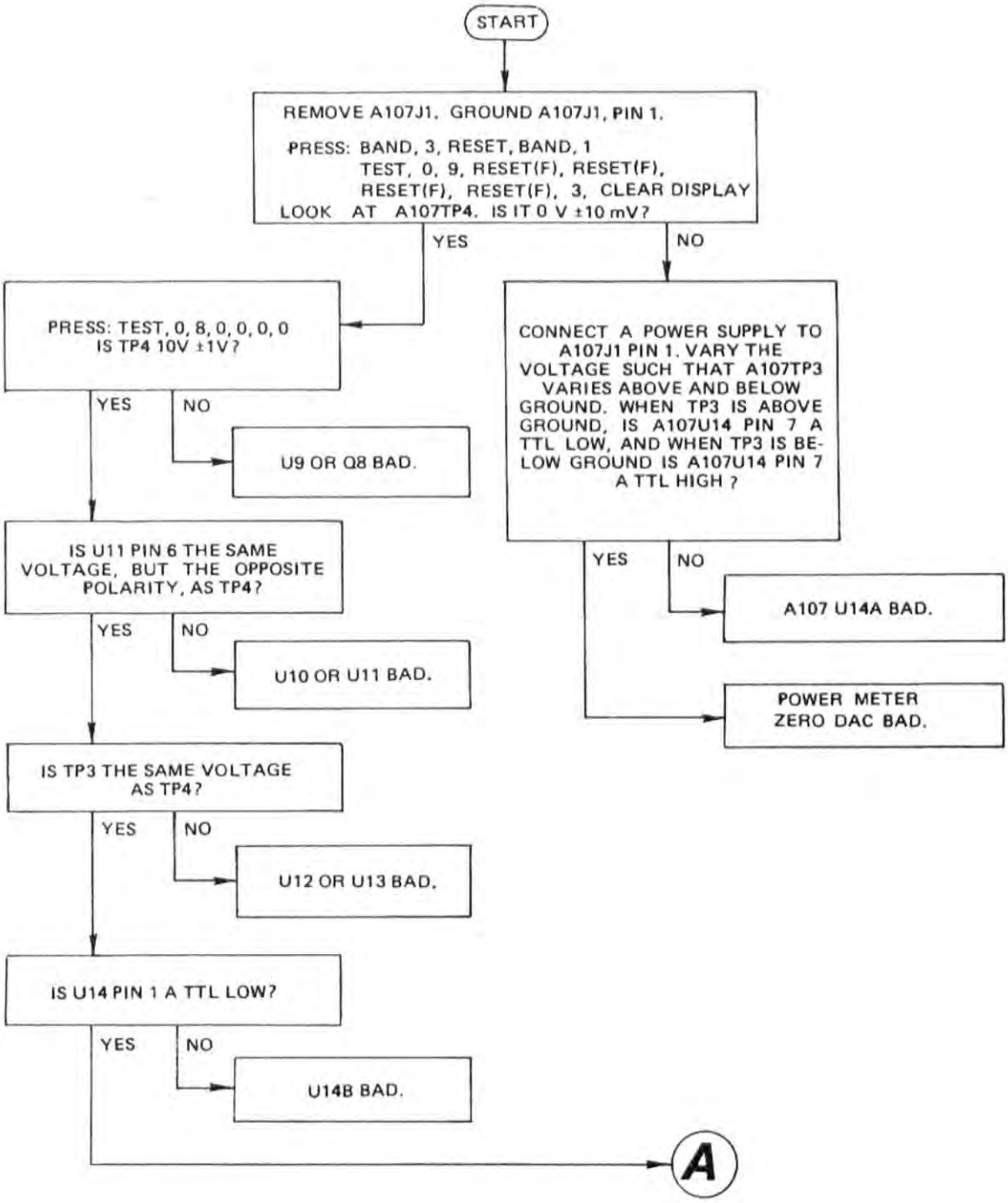


Figure 6-17. Power Meter and Power Meter Zero DAC

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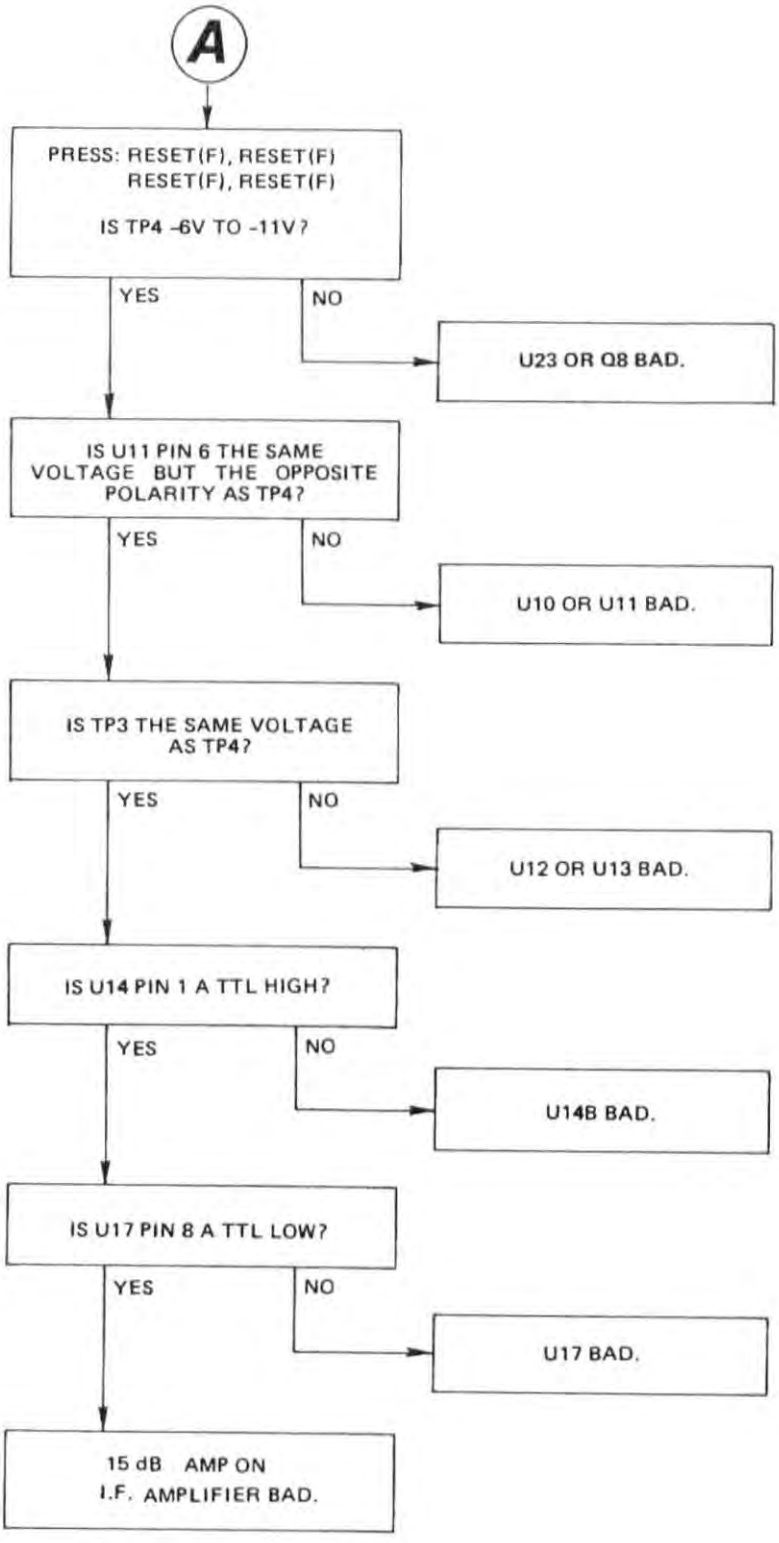


Figure 6-17. Power Meter and Power Meter Zero DAC, continued

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Section 7
Adjustments and Calibrations

GENERAL

To correctly adjust the 545A or 548A counter use the following procedures. Adjustments should only be made if the counter does not operate as specified, or following the replacement of components. If the adjustments do not result in the performance specified then refer to the troubleshooting section of this manual. The test equipment required is:

MANUFACTURER	MODEL	DESCRIPTION	CRITICAL PARAMETERS
Tektronix	475	Oscilloscope	General Purpose
Fluke	8050A	D.V.M.	4½ digit resolution
H.P.	182C, 8559A	Spectrum Analyzer	125 MHz
Wavetek	2002	Sweeper	10 MHz - 2 GHz
EIP	928	Microwave Source	1 GHz -18.6 GHz
H.P.	8690A, 8696A	Microwave Sweeper	18 GHz - 26.5 GHz
EIP	2000017	Service Kit	See Appendix A (A-3)

POWER SUPPLY ADJUSTMENTS

Prior to making any adjustments to the power supply the counter should warm up at least 20 minutes.

Voltages are measured on the back of the Power Supply board (A101).

1. Connect the Digital Volt Meter (DVM) between ground and +12V on A101, pin 1 and 8.
2. Adjust A101 R5 until the voltage measures +12.000 VDC ± .010 VDC.
3. Connect the DVM between ground and -12 V on XA101, pin 1 and 18.
4. Adjust A101 R17 until the voltage measures -12.000 VDC ± .010 VDC.

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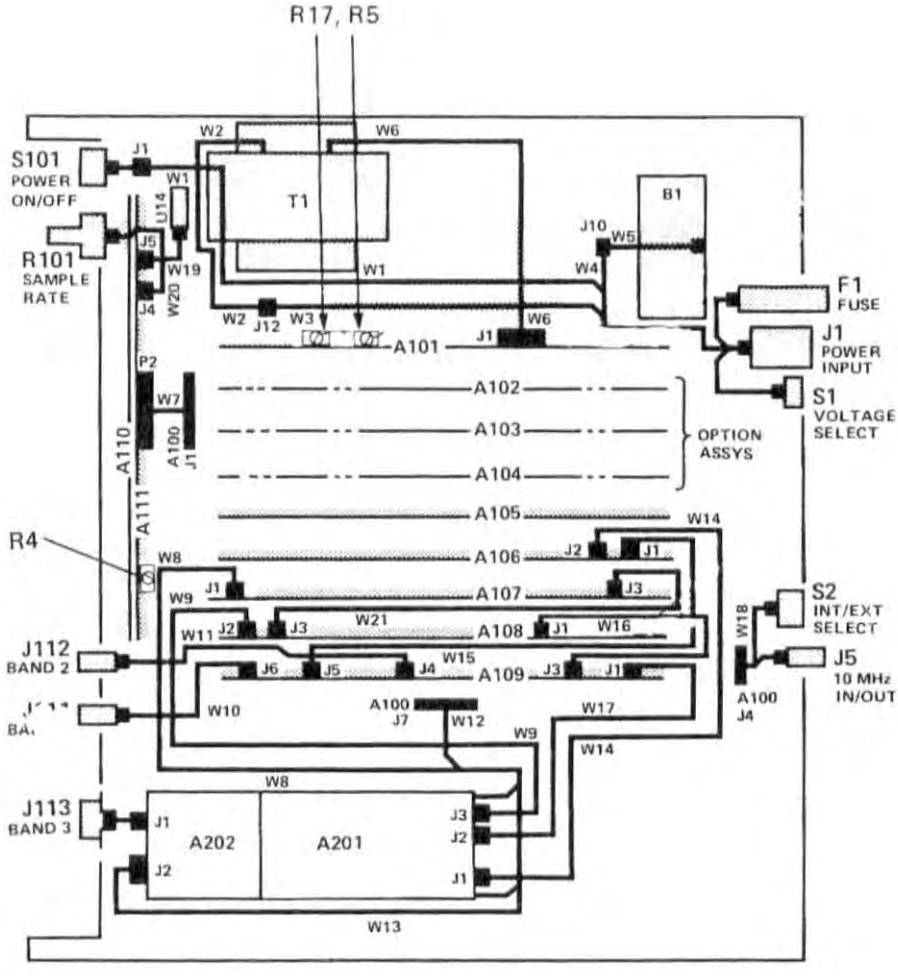


Figure 7-1. Adjustment Locations.

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YIG DAC CALIBRATION PROCESS

THEORY

The purpose of this process is to compensate the nonlinearity of the YIG and DAC error. The process allows a software route start in the EEPROM. The instrument generates a YIG DAC correction table, which resides in EEPROM. After the YIG searches for and centers on a signal, the software corrects the DAC reading (not the DAC itself) according to the correction table. This process yields the true YIG frequency. Then the program tunes the VCO according to the true YIG frequency instead of the ERROR DAC reading.

Each entry of the correction table contains two values:

(1) the YIG frequency and
(2) the DAC reading

Each value consists of 2 bytes. The YIG frequency is represented in hex in 2 MHz increments. For example, if the YIG frequency is 1 GHz then:

1 GHz = 1000 MHz = 2 * 500 MHz = 2 * 01F4 (hex)

and "01F4" is what is written to the table.

The table looks like this:

entry 1	YIG freq 1	DAC reading 1*
entry 2	YIG freq 2	DAC reading 2
. . .	. . .	. . .
. . .	. . .	. . .
entry N	YIG freq n	DAC reading n*

where N must be **at least 2 and can be as much as 248.** *The values in entry 1 and N are extrapolated.

YIG DAC CORRECTION TABLE

Given a DAC reading D, the software first searches through the second row of the table. If D is equal to an exact DAC reading in entry n, where 1 <= m <= 248, then the software generates the corresponding YIG frequency reading. If D falls between 2 consecutive DAC readings in entry p and q, where 1 < = p < q < = 248, then the software uses a linear interpolation algorithm to find the corresponding YIG frequency Y as shown in the following equation:

If:

$$\frac{\text{DAC q} - \text{DAC p}}{\text{YIG q} - \text{YIG p}} = \frac{\text{D} - \text{DAC p}}{\text{Y} - \text{YIG p}}$$

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then Y is:

$$Y = (D - DAC\ p) * \frac{YIG\ q - YIG\ p}{DAC\ q - DAC\ p} + YIG\ p$$

NOTE

When Y is being calculated, the multiplication is performed before the division to avoid precision error.

If for some reason the instrument cannot find a suitable DAC reading entry, ERROR #40 is generated to indicate error in the correction table.

CORRECTION TABLE SETUP

Setting up the correction table is actually the YIG DAC calibration process. The user enters "Test 90" to activate the process. At first the table contains two entries:

	YIG frequency	DAC number
default 1	0	0 hex
default 2	3FFF hex	3FFF hex

The user applies a synthesized signal Y1 GHz to the counter, then enters Y1 GHz through the counter's front panel or via GPIB. After the user enters the number, a routine converts that number to hexadecimal, stores it to the table as the YIG frequency of entry #2, and shifts the original entry #2 to entry #3. Then the counter sweeps the YIG to look for the signal and center the YIG on it. If the searching and centering are successful, the DAC number D1 is read and stored as DAC # of entry #2 of the table. Now the table looks like this:

default 1	0	0
entry 1	Y1	D1
default 2	3FFF	3FFF

The user can repeat the above sequence up to 246 times with the following restrictions:

(1) the sequence must be repeated at least two times.

(2) the frequency entered must be greater than the previous frequency.

If either of the two requirements above are not fulfilled or the counter cannot center the YIG on the signal, the whole process is aborted and the correction table is not altered.

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After N repetitions, the correction table will be as follows:

default 1.	0	0
entry 1.	Y1	D1
entry 2.	Y2	D2
. . .	. . .	. . .
entry N-1.	Y N-1	D N-1
entry N.	YN	DN
default 2.	3FFF	3FFF

where 2 <= N <= 246.

Since default values are used for the first and the last entry, they must be corrected before the user exits the calibration process. The software accomplishes this task by using Y1, Y2, D1, D2 to extrapolate default 1 and Y N-1, YN, D N-1, DN to extrapolate default 2.

The equation is :

$$Y = \frac{D * (Y2 - Y1) + Y1 * D2 - Y2 * D1}{D2 - D1}$$

The final correction table looks like this:

extrapolated entry 0.	Y0	D0
entry 1.	Y1	D1
entry 2.	Y2	D2
. . .	. . .	. . .
entry N-1	Y N-1	D N-1
entry N	YN	DN
extrapolated entry N+1	Y N+1	Y N+1

where 2 <= N <= 246.

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FORMAT AND ADDRESS OF THE CORRECTION TABLE

The correction table resides in EEPROM.

Address: 0C00 hex

Format:

yyyy dddd yyyy dddd .... yyyy dddd FFFF FFFF EEEE

where
- "yyyy" means 2 bytes of YIG frequency
- "dddd" means 2 bytes of DAC reading
- "FFFF FFFF" represents 4 bytes of end of table mark and
- "EEEE" means for software usage.

NOTE

Before performing this procedure, A108 S-1 must be open. (A108 U4, Pin 17 will be high). After calibration, S1 must be on (A108 U4, Pin 17) low to protect calibration.

CALIBRATION PROCEDURE

Manual Calibration

1. Press "BAND 3" on the front panel.
2. Press "TEST 90" on front panel. the counter will then display "F01".
3. Apply a synthesized 1-GHz signal at 0 dBm to Band 3 of the counter.
4. Enter "1" and press "GHz" on the front panel.
5. Counter should display "F02".
6. Apply a synthesized 1.3-GHz signal at 0 dBm to Band 3 of the counter.
7. Enter "1", ".", "3" and press "GHz" on the front panel.
8. Counter should display "F03".
9. Apply a synthesized 10-GHz signal at 0 dBm to Band 3 of the counter.
10. Enter "1", "0" and press "GHz" on the front panel.
11. Counter should display "F04".
12. Apply a synthesized 18-GHz signal at 0 dBm to Band 3 of the counter.
13. Enter "1", "8" and press "GHz" on the front panel.
14. Counter should display "F05".
15. **Go to step 28 if the model of the counter is 535/545/575.**
16. Apply a synthesized 22-GHz signal at 0 dBm to Band 3 of the counter.
17. Enter "2", "2" and press "GHz" on the front panel.

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21. Counter should display "F07".

22. Apply a synthesized signal 25.5 GHz at 0 dBm to Band 3 of the counter.

23. Enter "2", "5", ".", "5" and press "GHz" on the front panel.

24. Counter should display "F08".

25. Apply a synthesized signal 26.5 GHz at 0 dBm to Band 3 of the counter.

26. Enter "2", "6", ".", "5" and press "GHz" on the front panel.

27. Counter should display "F09".

28. Press **"CLEAR DATA"** to abort the process, or press **"CLEAR DISPLAY"** to exit the process.

NOTE:

If the counter can not find or center on the signal, it will display an ERROR #42 message.

NOTE:

The above frequencies are required to calibrate the counter. Other frequencies are at user's choice.

Calibration using GPIB controller.

1. Output "B3TA90" to the counter.

2. Command the signal source to generate 1 GHz at 0 dBm.

3. Output "1G" to the counter.

4. Command the signal source to generate 1.3 GHz at 0 dBm.

5. Output "1.3G" to the counter.

6. Command the signal source to generate 10 GHz at 0 dBm.

7. Output "10G" to the counter.

8. Command the signal source to generate 18 GHz at 0 dBm.

9. Output "18G" to the counter.

10. **Go to step 19 if the model of the counter is 535/545/575.**

11. Command the signal source to generate 22 GHz at 0 dBm.

12. Output "22G" to the counter.

13. Command the signal source to generate 24 GHz at 0 dBm.

14. Output "24G" to the counter.

15. Command the signal source to generate 25.5 GHz at 0 dBm.

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16. Output "25.5G" to the counter.

17. Command the signal source to generate 26.5 GHz at 0 dBm.

18. Output "26.5G" to the counter.

19. Output "C" to exit the calibration process or "D" to abort the process.

NOTE:

When the counter has acquired the signal and is ready to accept the next frequency, the GPIB status byte bit 0 will be set to 1. This can be recognized through service request.

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TIME BASE CALIBRATION

NOTE

For Option 03, 04, 05, refer to Option Section of the manual.

It is important to note that the precision of the time base calibration directly affects overall counter accuracy. Reasons for recalibration, and the procedures to be used, should be thoroughly understood before attempting any readjustment.

The fractional error in the frequency indicated by the counter is equal to the negative of the fractional frequency error of the Time Base Oscillator with respect to its true value. That is:

$$\frac{\triangle f_s}{f_s} = \frac{\triangle f_t}{f_t}$$

where f_s is the true frequency of the measured signal, and f_t is the true frequency of the Time Base Oscillator. Thus, the inaccuracy associated with a frequency measurement is directly related to the quality of the Time Base Oscillator, and a measure of the precision with which it was originally adjusted.

TEMPERATURE COMPENSATED CRYSTAL OSCILLATOR (TCXO)

The standard time base oscillator used in the counter is a TCXO (A113). The range of the actual measured frequencies of this oscillator will differ by no more than 2 parts in 10^6 if the temperature is slowly varied from 0 to +50 degrees C.

With a stable input frequency, the measurement indicated by the counter will fluctuate in proportion to the TCXO drift. To center this fluctuation on the true value of the measured signal, each TCXO has imprinted on its side the frequency setting required at +25 degrees C.

At approximate room temperature (+25 degrees C), the slope of the frequency vs. temperature curve is normally no worse than $\pm 1 \times 10^{-7}$ parts per degree C. When the counter is used in an ordinary laboratory environment, the TCXO may be set as close to 10,000,000 Hz as desired. In this environment, a peak-to-peak temperature variation of 5° C will result in a measured signal error of no more than $\pm 2.5 \times 10^{-7}$ parts. This signal error is due to the temperature characteristics of the time base oscillator.

The natural aging characteristics of the crystal in the time base oscillator can also cause inaccurate signal measurements. Aging refers to the long term, irreversible change in frequency (generally in the positive direction) that all quartz oscillators experience. The magnitude of this frequency fluctuation in the TCXO is less than 3×10^{-7} parts per month as specified. This may improve to at least 1×10^{-6} parts per year when in continuous operation.

Error due to aging adds directly to error due to temperature. The number of times the counter requires recalibration depends on the environment in which the counter operates, and upon the level of accuracy required.

For example, if the counter is subjected to the full operating temperature range one month after proper initial adjustments, the inaccuracy could vary from $+1.3 \times 10^{-6}$ parts to -0.7×10^{-6} parts.

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TCXO CALIBRATION PROCEDURES

METHOD 1 (with accurate frequency counter)

1. Remove top cover of counter. Connect counter to line voltage. Check that ambient temperature is ~20° C.

2. Measure the frequency of the TCXO (at the rear panel 10 MHz connector) with a second counter of known calibration accuracy.

3. Refer to calibration label on TCXO showing offset from 10 MHz required for accurate function over 0 - 50° C range.

4. Adjust the TCXO by turning the calibration screw on the TCXO case until the measured frequency equals that shown on the TCXO calibration label.

METHOD 2 (with accurate frequency source)

1. Apply a 10 000 000 Hz signal from a frequency standard (or other oscillator of suitable accuracy and stability) to the Band 1 input of the counter.

2. Press RESOL [ ] [0] (1 Hz resolution)

3. Adjust the TCXO until the reading on the counter is offset from 10 000 000 Hz by the negative of the frequency shown on the TCXO. For example, if the TCXO calibration label shows a frequency of 10 000 003 Hz, adjust the TCXO until the counter displays 9 999 997 Hz.

DISPLAY INTENSITY

On the front panel logic assembly (A111), R4 may be adjusted to provide the most comfortable display intensity.

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Section 8
Performance Tests

GENERAL

These tests are for the basic counter. Peformance tests for options are in section 10. These tests will enable the user to verify that the counter is operating within specifications.

VARIABLE LINE VOLTAGE

During the performance tests the counter should be connected to the power source, through a variable voltage device, so that line voltage may be varied ±10% from nominal. This will assure proper operating of the counter under various supply conditions.

REQUIRED TEST EQUIPMENT
(or equivalent)

MANUFACTURER	MODEL	DESCRIPTION	CRITICAL PARAMETERS
H.P.	651B	Signal Generator	10 Hz - 10 MHz
Wavetek	2002	Sweeper	10 MHz - 2 GHz
EIP	928	Microwave Source	1 GHz - 18.6 GHz
H.P.	8690A, 8696A	Microwave Sweeper	18 GHz - 26.5 GHz

BAND 1
(10 Hz - 100 MHz)

1. Set the counter to band 1.
2. Connect the signal source output, through a 50 ohm shunt feedthrough resistor, to the band 1 input on the counter.
3. Set the signal level to 25 mv RMS (-19 dBm into 50 ohms).
4. Vary the signal from 10 Hz to 100 MHz (changing signal source as required).

The counter should display the correct input frequency.

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BAND 2
(10 MHz - 1 GHz)

1. Set the counter to band 2.
2. Connect the signal source output to the band 2 input of the counter.
3. Set the signal level to -20 dBm (22 mv RMS).
4. Vary the signal input from 10 MHz to 1 GHz.

The counter should display the correct input frequency.

BAND 3
(548A: 1 GHz - 26.5 GHz)
(545A: 1 GHz - 18 GHz)

1. Set the counter to band 3.
2. Connect the signal source output to the band 3 input of the counter.
3. Vary the signal frequency from 1 GHz to 18/26.5 GHz (changing the signal source as required) at the following levels.

1 GHz – 1.2 GHz	-25 dBm (12 mv RMS)
1.2 GHz – 12.4 GHz	-30 dBm (7 mv RMS)
12.4 GHz – 18 GHz	-25 dBm (12 mv RMS)
18 GHz – 22 GHz	-20 dBm (22 mv RMS)
22 GHz –26.5 GHz	-15 dBm (38 mv RMS)

The counter should display the correct input frequency.

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Section 9
Functional Description and Illustrated Parts Breakdown

This section contains a functional description, a parts list, an illustration, and a schematic diagram for each printed circuit board used in this counter.

Parts are listed alphabetically by component type and then in numeric order within component type. Components that have a different reference designator (REF DES) but the same EIP part number are described for the first such component listed. Subsequent descriptions of that component will refer to the first entry. The total number of like components used on the same assembly will be listed with the first entry in the column identified as UNITS PER ASSEMBLY.

The last two columns of the parts list give the name and the Federal Supply Code for Manufacturers (FSCM) numberof the manufacturer. A list of manufacturers' names, addresses, and FSCM numbers is given in Appendix B. The FSCM number is used in the parts list as a guide to the manufacturer or supplier of a part.

Pages 9-3 through 9-5 contain the top assembly of the counter and other basic information. After page 9-5, the page numbers have a three-digit first number followed by a dashed number. The three-digit number reflects the number of the assembly being described on those pages. The dashed number is the page sequence for the description on that assembly. For example, pages 105-1 through 105-5 all relate to the A105 printed circuit board. This page numbering system facilitates simple, modular page replacement when an assembly revision makes a manual update necessary.

REFERENCE DESIGNATORS

A	Assembly	J	Jack or Connector	S	Switch
B	Battery or Fan	K	Relay	T	Transformer
C	Capacitor	L	Inductor	TP	Test Point
CR	Diode	P	Plug or PCB Contacts	U	Integrated Circuit
DS	Indicator (Display)	Q	Transistor	X	Socket or Holder
F	Fuse	R	Resistor	Q1-3	Q1 through Q3
				Q1/2	Q1 and Q2 (matched pair)

ABBREVIATIONS

CBN	CARBON	NOM	Nominal
CER	Ceramic	PC	Printed Circuit
CMT	Cermet	PCB	Printed Circuit Board
CNTR	Counter	pF	picofarad
CONV	Converter	PREC	Precision
COMP	composition	PROM	Programmable Read Only Memory
CONN	Connector	RAM	Random Access Memory
ELEC	Electrolytic	RSTR	Resistor
FDTH	Feedthrough	RT AN	Right Angle
FLM	Film	S.A.T.	Value or type selected at factory test. Part may not be used.
FML	Female		
GP	General Purpose	SW	Switch
IC	Integrated Circuit	TANT	Tantalum
K	Kilo (x 1,000)	TRIM	Trimmer
LED	Light Emitting Diode	uF	Microfarad
M	Meg(a) (x 1,000,000)	uH	Microhenry
MET OX	Metal Oxide	VAR	Variable
MF	Metal Film	WPRF	Waterproof
mH	Millihenry	WW	Wirewound
ML	Male	XSTR	transistor
MTCH PR	Matched Pair		

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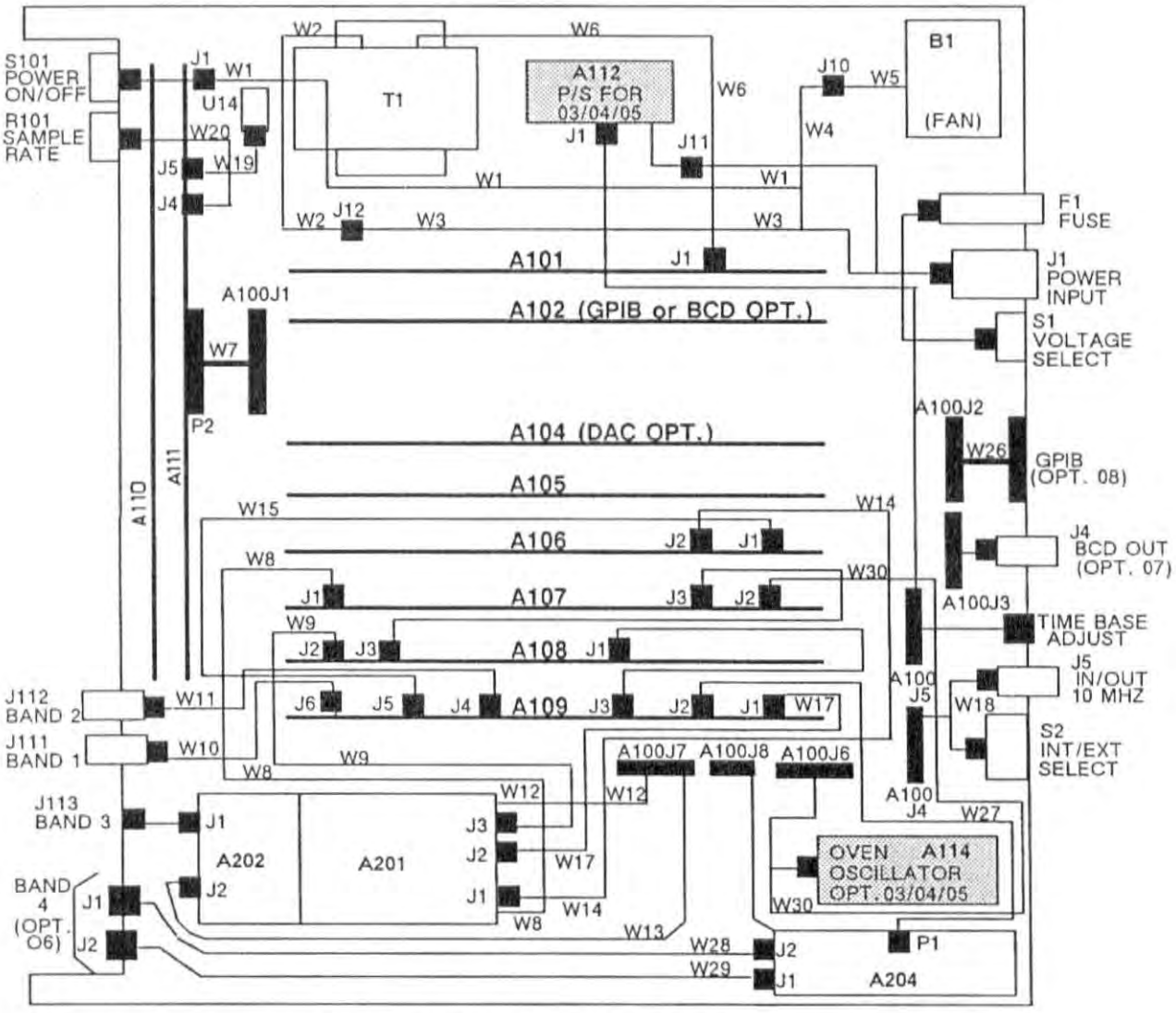


Figure 9-1. Assembly Locations and Cable Connections in Counter

CABLE CONNECTION GUIDE

FROM	CABLE	TO	FROM	CABLE	TO
A1S101J1	W1	A1S1, F1,J1	A108J1	W16	A109J3
A1J12	W2	A1T1	A109J1	W17	A201J2
A1S1	W3	A1J12	A1J5,S2	W18	A100J4
A1J10	W4	A1S1	A1U14	W19	A111J5
A1B1	W5	A1J10	A1R101	W20	A111J4
A101J1	W6	A1T1	A107J3	W21	A108J3
A111P2	W7	A100J1			
A107J1	W8	A201			
A108J2	W9	A201J3			
A1J111	W10	A109J6			
A1J112	W11	A109J4	A100J2	W26	A1,GPIB (OPT. 08)
A201	W12	A100J7	A204P1	W27	A109J2 (BAND 4, OPT 06)
A202J2	W13	A100J7	A204J2	W28	A1J1 (BAND 4, OPT 06)
A106J2	W14	A201J1	A204J1	W29	A1J2 (BAND 4, OPT 06)
A106J1	W15	A109J5	A107J2	W30	A100J6 (OPT. 03/04/05)

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545A/548A MICROWAVE COUNTER

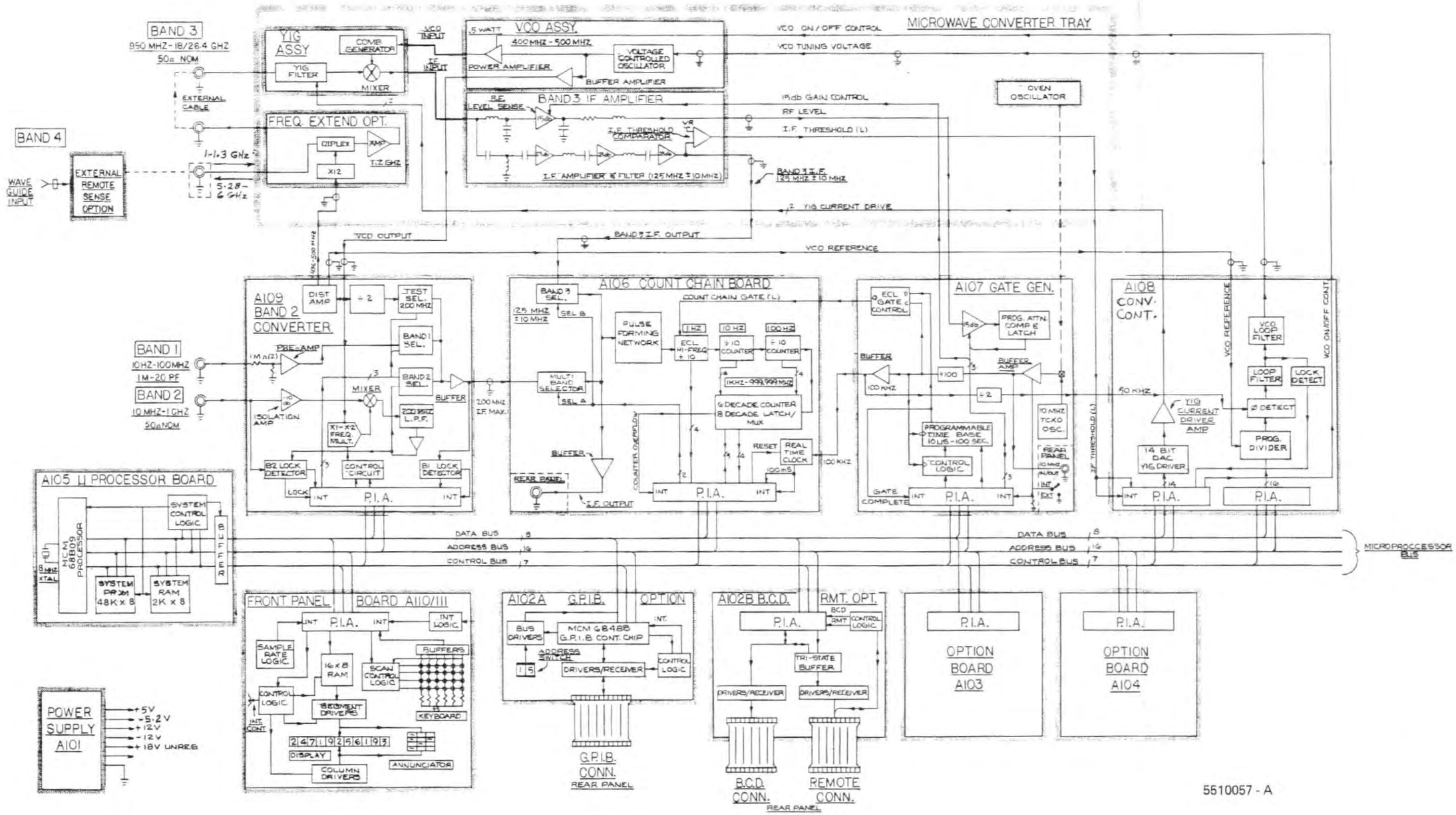
REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
	COUNTER, MODEL 545A	2010224-06		EIP	34257
	MODEL 548A	2010225-06		EIP	34257
-1	FRONT PANEL ASSY	2010218-09,10	1	EIP	
	Knob	5210223	1	5000160	31013
	Button set, 12 + 9	5210220	1	5230005-02	
	Panel	5210378	1		
	Sample Rate Control Assy	2010134-01	1		
	Alignment Pin	5210190	2		
	Retainer Key	5210191	1		
	Switch, toggle, PWR	2010187-01	1		
-2	REAR PANEL ASSY	2010219-01	1	EIP	
	Panel	5210192	1		
	Conn, Filter	2650005	1	3EF1	05245
	Switch, toggle, SPDT, 120V, 5A	4510001	1	7101H	09353
	Fuse holder	5000172	1	031.1653/1666/1663	
	Fuse, 1A, SB, 250V	5000085	1	MDL -1A	71400
	Fuse, .50A, SB, 250 V	5000169	1	FST034-3114	71400
	Conn, BNC	2610024	1	KC -79 -35	91836
	Voltage Select Switch Assy, A151	2010159-01	1		
-3	FAN ASSY	2010136-01	1		
	Fan	5000151	1	760/126LF/182/1115	
	Conn, Plug, 3 pin	2620110	1	03 - 06 - 2032	0000A
	Contact, Male	2620038	2	02 - 06 - 2103	0000A
	Spacer	5210016	2		
-4	FRAME KIT	2010151-01	1		
	Panel, Side, Enclosure	5210210	2		
	Trim, Front Post	5220004	2		
	Trim, Handle	5220025	2		
	Frame	5210248	2		
	Corner Post, Front	5250001	2		
	Corner Post, Rear	5250002	2		
	Handle, Enclosures	5250011	2		
-5	TRANSFORMER, ASSY, A1T1	2010359-01	1		
	Transformer, Power	4900005	1		
	Conn, Plug, 9 pin	2620112	1	03 - 06 - 2092	0000A
	Conn, Housing, 6 pin	2620129	Ref	640427 - 6	AMP
	Contact, Male	2620038	7	02 - 06 - 2103	0000A
	Contact, Female	2620036		02 - 06 - 1103	0000A
-6	FRONT CARD GUIDE ASSY	5210199	1		
-7	REAR CARD GUIDE ASSY	5210200	1		
-8	TOP COVER ASSY	2010212-01	1		
-9	BOTTOM COVER	5210209	1		
-10	TILT BAIL	5000055	1		
-11	Foot, Plastic Enclosure	5220003	4		
-12	Line Cord Set - Domestic	5440002	1		
	Line Cord Set - Export	5440017	1		

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545A/548A Microwave Counter (continued)

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
	PCB ASSEMBLIES			**See Page No.**	
A100	Counter Interconnect	2020180-01	1	100-1	
A101	Power Supply	2020131-01	1	101-1	
A105	Microprocessor	2020215-02	1	105-1	
A106	Count Chain	2020136-03	1	106-1	
A107	Gate Generator	2020197-09	1	107-1	
A108	Converter Control (Band 3)	2020200-04	1	108-1	
A109	Band 2 Converter	2020139-05	1	109-1	
A110	Keyboard Display and Logic	2020140-02	1	110-1	
A111	Front Panel Logic	2020191-02	1	111-1	
A203	Microwave Converter (Band 3)	2020241-06	1	203-1	
A201A	Voltage Control Oscillator (not shown)	2020199-00			
A201B	IF Amplifier) (not shown)	2020143-01			
A202	Microwave (YIG) Assembly (not shown)				
	CABLES				
W17	Front Panel, Flat Ribbon	2040169-01	1		
W19,20	Front Panel, Harness	2040168-01	1		
W1,3,5	RearPanel, Harness	2040167-01	1		
W10	(A1J111-A109J6) Band 1, Coax	2040165-01	1		
W11	(A112-A109J4) Band 2, Coax	2040166-01	1		
W16	(A108J1-A109J3) Coax	2040208-01	1		
W15	(A106J2-A109J5	2040210-01	1		
W12,13	VCO/IF, Harness	2040170-01	1		
W14	(A201BJ1-A106J2) Coax	2040172-01	1		
W8	(A201J4-A107J1) Coax	2040173-01	1		
W9	(A201AJ3-A108J2) Coax	2040174-01	1		
W17	(A201AJ3-A109J1) Coax	2040175-01	1		
	PROMS			REVISION LEVEL OF PROMS MUST BE SPECIFIED WHEN ORDERING PROM SET (SEE LABEL ON PROM)	
A105	BASIC PROM SET	2060025-01			
U11	Section 1	6400010-01	1		
U12	Section 2	6500010-01	1		
U13	Section 3	6500010-02	1		
A105	GPIB OPTION	2060010-02			
U19		6400010-03	1		
A107	POWER METER OPTION	2060010-03			
U20		6400010-05	1		
A105	DAC OPTION	2060010-04			
U13	(contained in basic PROM set)				
A105	BCD/REMOTE OUTPUT OPTION	2060010-05			
U19		6400010-04	1		
A105	BAND 4 OPTION	2060010-06			
U20		6400010-02	1		

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5510057 - A

Figure 9-2. 545A/548A Block Diagram

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A100
COUNTER INTERCONNECT
(202180)

FUNCTIONAL
DESCRIPTION
NOT REQUIRED

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A100 COUNTER INTERCONNECT ASSY

2020180 - G

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A100	Counter Interconnect Assy	2020180	1	EIP	34257
J1	Header, Str, 26 pin	2620078	1	3429 - 2302	76381
J2	Header, Str, 50 pin	2620081	2	3433 - 2302	76381
J3	J2				
J4	Friction Lock, 4 pin	2620061	1	09 - 65 - 1049	0000A
J5	Friction Lock, 6 pin	2620090	1	09 - 65 - 1069	"
J6	Header, Str, 7 pin	2620186	1	09-64-1071	"
J7	Header, Str, 10 pin	2620187	1	09-64-1101	"
J8	Friction Lock, 4 pin	2620068	1	640456-4	AMP
XA101	Conn, 11 position	2620183	1	5193-442-1	AMP
XA102	Conn, 50 position	2620185	1	5193-442-3	"
XA103 thru XA109	Conn, 30 position	2620184	7	5193-442-2	"
	Key Plug	50001030	10	530286 - 2	"

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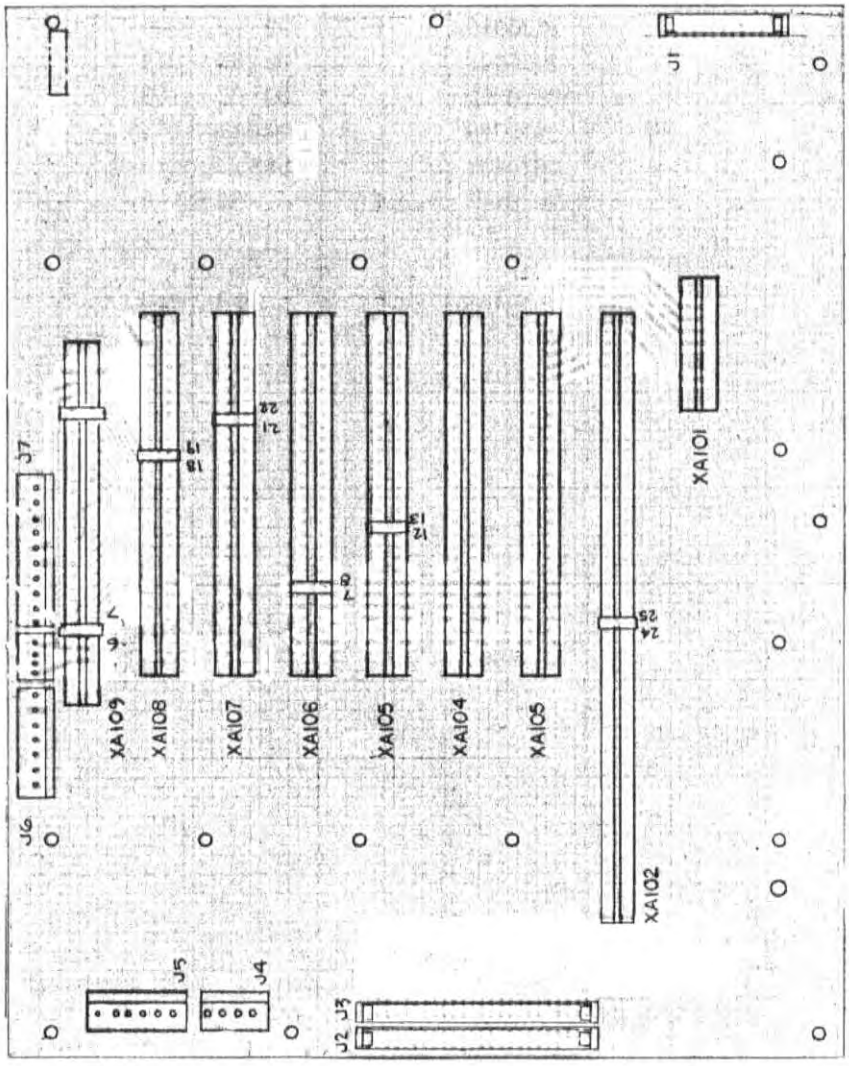
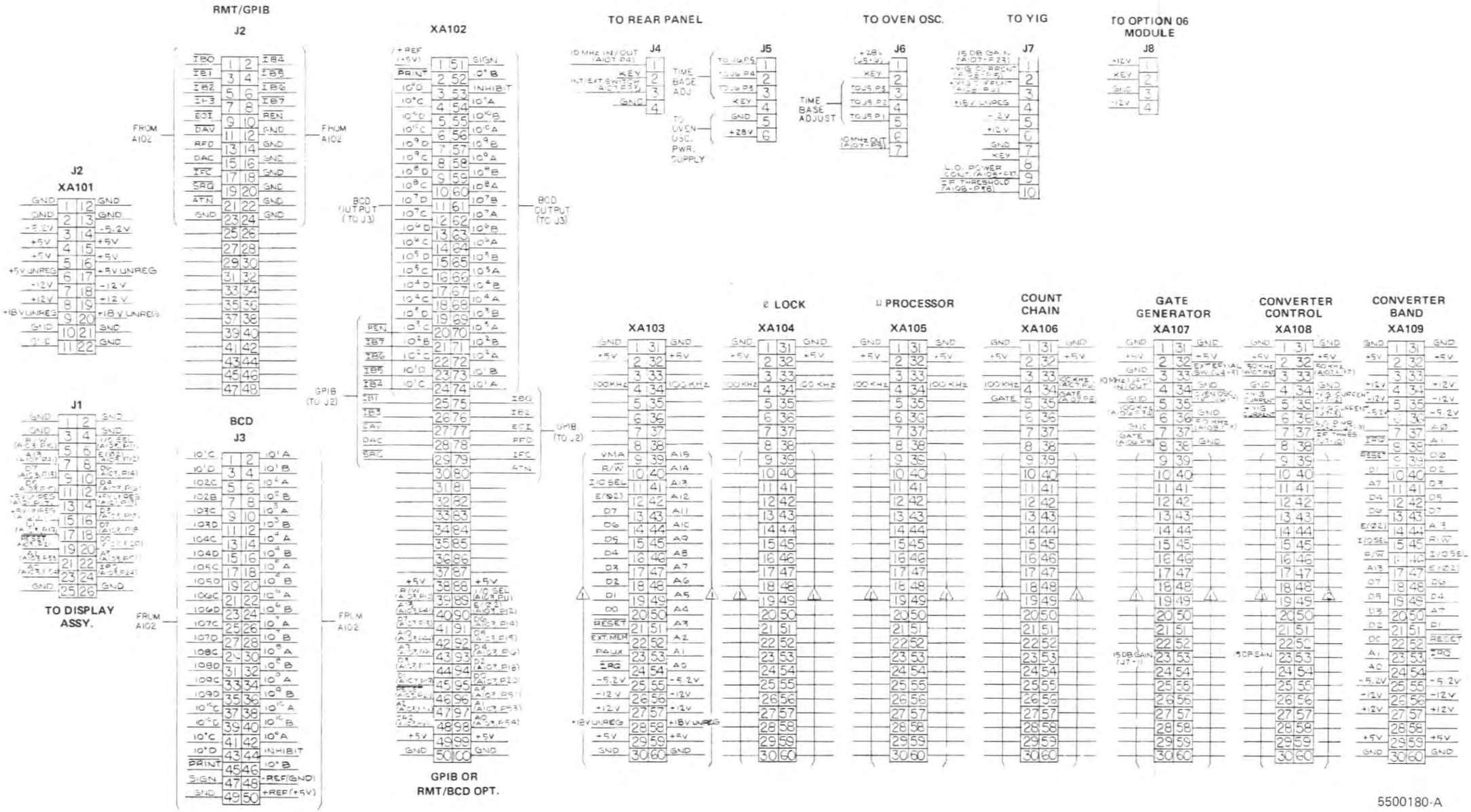


Figure 100-1. Counter Interconnect Component Locator

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⚠ XA103 THRU XA109 HAVE COMMON CONNECTIONS (PIN LINES SHOWN IN BRACKETS).

Figure 100-2. Counter Interconnect Schematic

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A101
POWER SUPPLY
(2020131)

The power Supply furnishes all basic operating voltages required by the counter. The supply consists of two basic sub-assemblies.

- PC Board (A101), containing the rectifiers, filter capacitors, and regulator circuitry.
- Chassis mounted components consisting of the power transformer (T1), primary wiring, F1 fuse; (100/120V), the 220/240V power programming switch; and the on/off power switch (S101) mounted on the front panel.

The basic voltages required by the counter are unregulated +18V, regulated +5V, −5.2V, +12V and −12V.

The input AC voltage is full wave rectified and filtered to produce DC voltages of ± 9V and ± 18V.

The unregulated +18V is used directly as one supply voltage. The +18V is regulated to a +12V by the action of LM305, a series pass transistor (MJE3055), and foldback current limiting circuitry. The −18V is regulated to a −12V by LM304, a series pass transistor, and foldback current limiting circuitry.

The +9V is regulated to +5V by a three terminal regulator containing thermal and current shutdown circuitry. The −9V current is also regulated to −5.2V by a three terminal regulator that contains thermal and current shutdown circuitry.

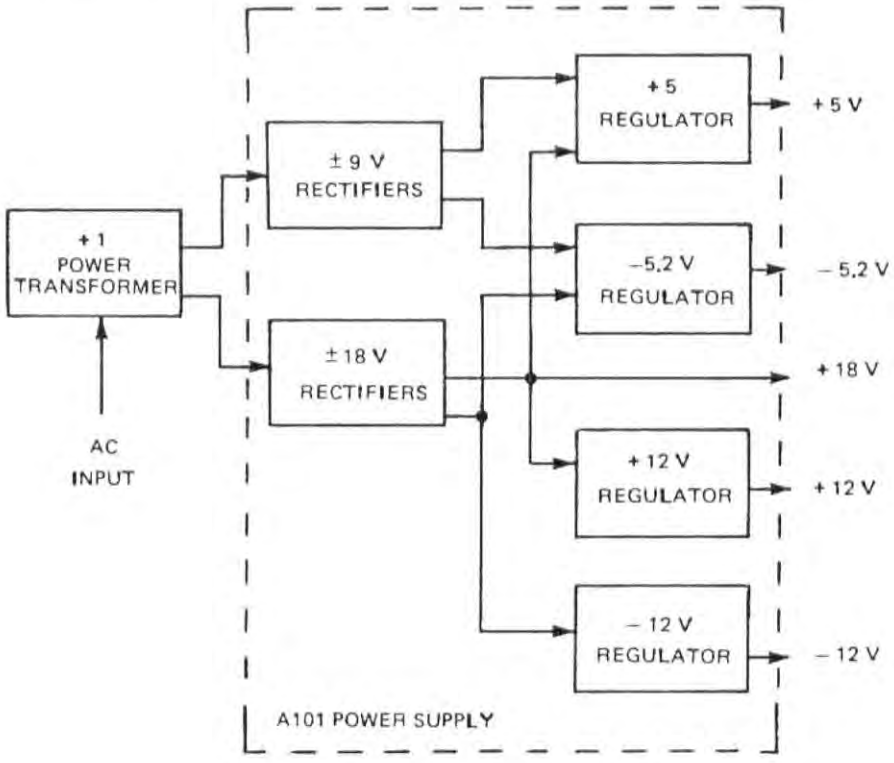


Figure 101-1. Power Supply Functional Diagram

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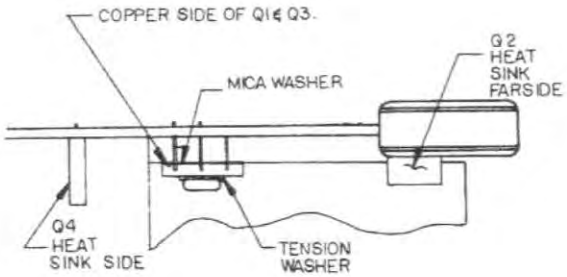
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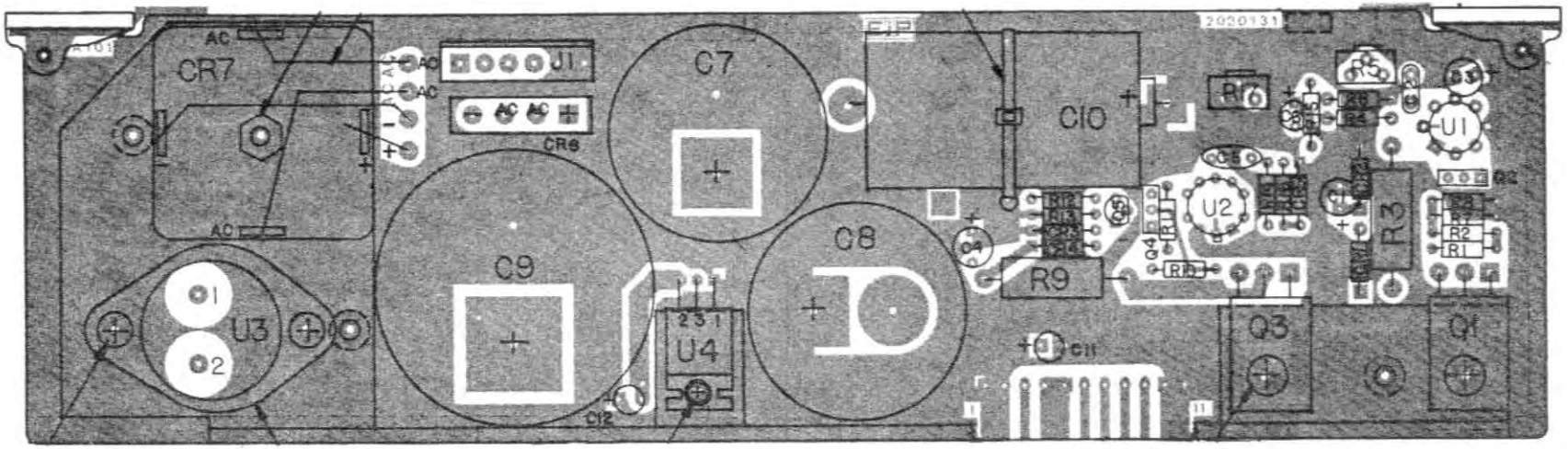
A101 POWER SUPPLY ASSY

2020131-L

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A101	Power Supply Assy	2020131	1	EIP	34257
C1	Tant, 10μF, 20%, 25V	2300029	3	TAG 20 - 10/25(M)	14433
C2	Mica, 47 pF, 5%, 500V	2260004	1	DM10 - 470J	72136
C3	C1				
C4	Tant, 33μF, 20%, 20V	2300023	1	TAG 20 - 33/20 - 20	14433
C5	Cer, .001μF, 20%, 20V	2150001	1	5GA - D10	56289
C6	Tant, 1.0μF, 20% 35V	2300008	2	TAG 20 -1.0/35 - 50	14433
C7	Elec, 14,000μF, 25V	2200017	1	3110HB143U025	80031
C8	Elec, 9,500μF, 15V	2200016	1	3110HA952U025	80031
C9	Elec, 32,000μF, 15V	2200019	1	3110RB323U015	80031
C10	Elec, 4,900μF, 15V	2200020-00	1	3050JJ4920U15JM	80031
C11	C6				
C12	C1				
CR1 thru CR4	Rectifier	2704001	4	IN4001	07263
CR5	Zener, 12V	2720963	1	IN963A	04713
CR6	Rectifier Brdg	2710029	1	MDA970 - 1	04713
CR7	Rectifier, Brdg	2710028	1	MDA990 - 1	04713
J1	Conn, 6 pin (FRCTN Lock)	2620157	1	640445-6	0000A
Q1	NPN Power	4710001	2	MJE3055	04713
Q2	PNP Power	4710002	2	MJE370	04713
Q3	Q1				
Q4	Q2				
Q5	PNP, General Purpose	4704126	1	2N4126	04713
R1	Comp, 68 ohms, 5%, 1/4 W	4010680	2	RC07GF680J	81349
R2	Met Ox, 36 ohms, 2%, 1/4 W	4130360	1	C4/2%/36	24546
R3	Wire Wound, 0.66 ohms, 3%, 4W	4110012	2	RS - 2	91637
R4	Prec, 14.7K ohms, 1%, 1/8 W	4061472	1	RN55D1472F	81349
R5	Var. Cer., 500 ohm	4250014	1	72XR500	73138
R6	Prec, 2.26K ohms, 1%, 1/8 W	4062261	1	RN55D2261F	81349
R7	Met Ox, 820 ohms, 2%, 1/4 W	4130821	2	C4/2%/820	24546
R8	R7				
R9	R3				
R10	R1				
R11	Comp, 100 ohms, 5%, 1/4 W	4010101	1	RC07GF101J	81349
R12	Met Ox, 910 ohms, 2%, 1/4 W	4130911	1	C4/2%/910	24546
R13	Met Ox, 12K ohms, 2%, 1/4 W	4130123	1	C4/2%/12K	24546
R14	Prec, 2.43K ohms, 1%, 1/8 W	4062431	1	RN55D2431F	81349
R15	Prec, 4.7K ohms, 2%, 1/4 W	4130472	1	C4/2%/4.7	24546
R16	Met Ox, 1K ohms, 2%, 1/4 W	4130102	1	C4/2%/1K	24546
R17	Var, Cer, 2K ohms	4250016	1	72XR2K	73138
U1	Voltage Regulator	3040305	1	LM305	0000X
U2	Voltage Regulator	3040304	1	LM304	0000X
U3	+5VDC Regulator	3057805-01	1	UA78H05A	07263
U4	-5.2 V Regulator	3057905	1	MC7905.2 CT	04713

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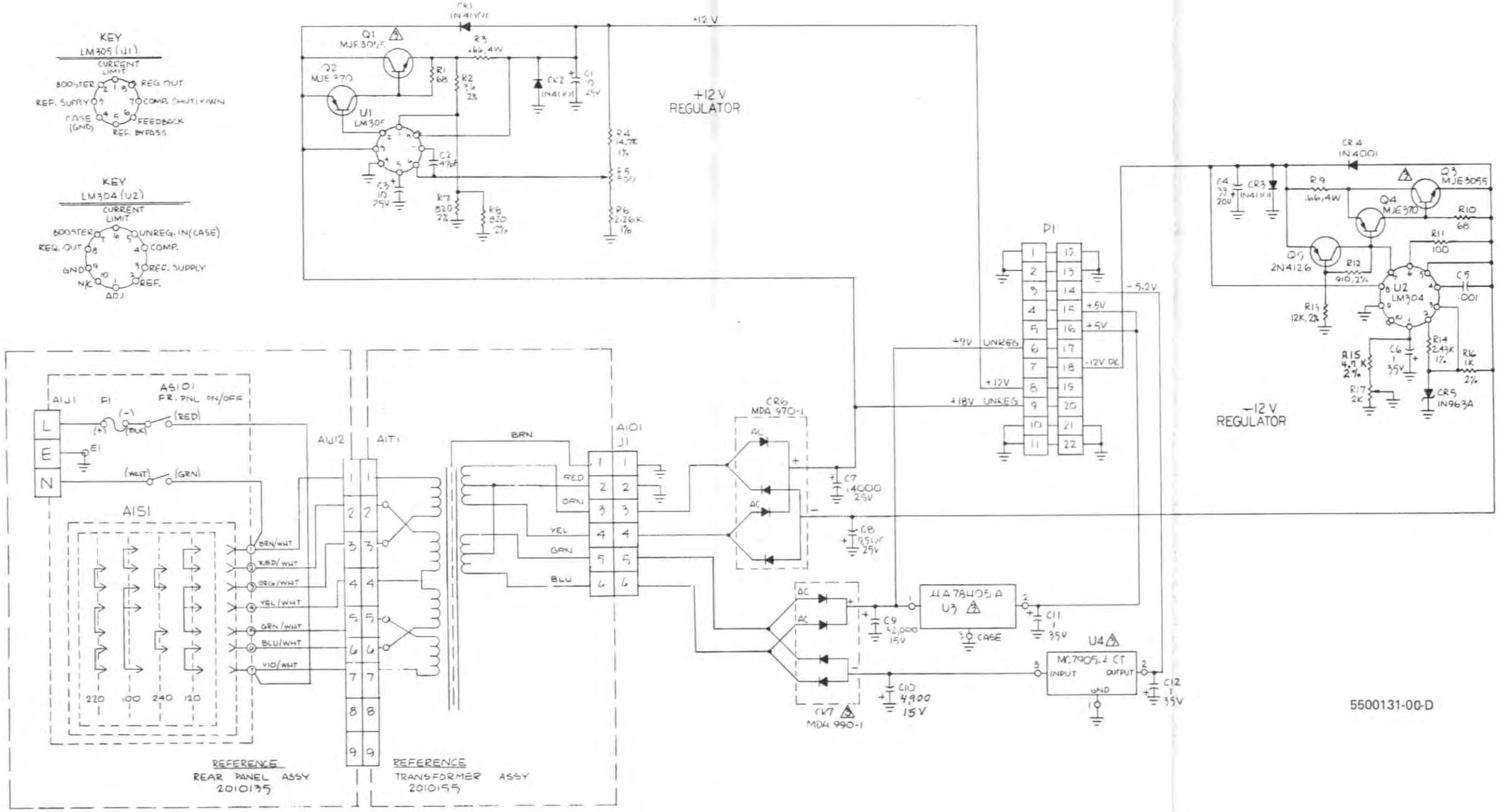




2020131-01- L

Figure 101-2. Power Supply Component Locator

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5500131-00-D

Figure 101-3. Power Supply Schematic

⚠2 CR7, Q1, Q3, U3, U4 ARE MOUNTED ON HEATSINKS.

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A105
MICROPROCESSOR
(2020215)

The Microprocessor board contains the microprocessor, the control logic, and the firmware for controlling the operation of the counter. The board can be divided into five functional blocks.

1. Microprocessor
2. Power-up Reset Circuit
3. Address Decoder
4. RAM and Program Memory
5. Control Logic Buffers.

MICROPROCESSOR

The counter uses a Motorola 68B09 microprocessor. The clock generation circuitry for the digital system is contained within the 6809. The only external components required for clock generation are two 24-pF capacitor and an AT-cut 8-MHz crystal.

The NMI, FIRQ, and DMA functions of the 6809 are not used. Their corresponding control lines are always disabled. The processor state indicators (BS, BA) are also not used by the counter. The HALT and the MRDY controls are connected to the Interconnect board through the edge connector.

POWER–UP RESET CIRCUIT

The Power-up Reset circuit provides a 100-ms reset signal to the entire digital system after the counter is turned on. The reset signal remains true as long as the +5-volt power supply stays below +4 volts.

When the counter is turned on, the voltage across C5 is 0 volts. The output of the comparator U1 is at logic low. The capacitor C5 slowly charges up through R2. The output of the comparator remains low as long as the voltage across C5 is lower than the voltage on pin 3 of the comparator. When the voltage across C5 becomes higher than that on pin 3, the output of the comparator becomes true, removing the reset signal. R3 is provided for hysteresis purposes. When power is removed, C5 will discharge quickly through CR1.

ADDRESS DECODER

The address decoding is performed by a 4-to-16 line decoder. The 64K-byte address space is divided into sixteen 4K-byte blocks, one of which is always enabled.

The enable signals for the memory blocks become true no later than 51 ns after Q. They stay true until a maximum of 40 ns after E has becom false. The 4-to-16-line decoder has open collector outputs. This enables the addressed memory block to be enlarged by wire-ORing two or more outputs together.

The memory map for the counter is as follows:

Volatile RAM Memory	0000 - 07FF
Non-Volatile RAM Memory	0800 - 0FFF
I/O	1000 - 2FFF
Signature Analysis	3000 - 3FFF
Program Memory	4000 - FFEF
Reserved (6809)	FFF0 - FFF1
	FFF2 - FFF3
	FFF4 - FFF5
	FFF6 - FFF7
IRQ	FFF8 - FFF9
	FFFA - FFFB
	FFFC - FFFD
RESET	FFFE - FFFF

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RAM AND PROGRAM MEMORY

RAM

A 2K-byte-wide volatile RAM is provided for the normal operation of the counter. To prevent data from being erroneously written into the RAM, the chip enable signal is active only when the E clock and the RAM memory block enable signal from the address decoder are both active and when the A11 address line is at logic 1.

PROM

A block of 48K bytes of memory are assigned for system program. The Microprocessor board contains three 28-pin sockets for PROMs. Each of the sockets is wired to accept a 16K-byte PROM.

CONTROL LOGIC AND BUFFERS

The digital system of the counter contains three buses: the data bus, the address bus, and the control bus.

DATA BUS

The data bus originates from the microprocessor. For signature analysis, the data bus can be disconnected from the rest of the system at the microprocessor by removing jumper header E1. The data bus on the microprocessor board is buffered from the rest of the digital system. The data bus buffer is enabled only when the address space assigned to I/O is addressed. The direction of the data bus buffer is determined by the state of the R/W control line.

ADDRESS BUS

The address bus also originates from the microprocessor. The address bus buffer is always enabled.

CONTROL BUS

The control bus contains eight control lines. Five of the control lines originate from the Microprocessor board. The other three control lines originate from the rest of the digital system.

R/W, E, and Q originate from the microprocessor. Reset is supplied by the power-up reset circuit. The I/O SEL control line is true when A15 and A14 are at logic 0 and either A13 or A12 or both are at logic 1 levels. The IRQ control line is the wired-OR of all the interrupt request lines. MRDY is the wired-OR of the memory ready control lines. The MRDY and HALT control lines are provided for future expansion.

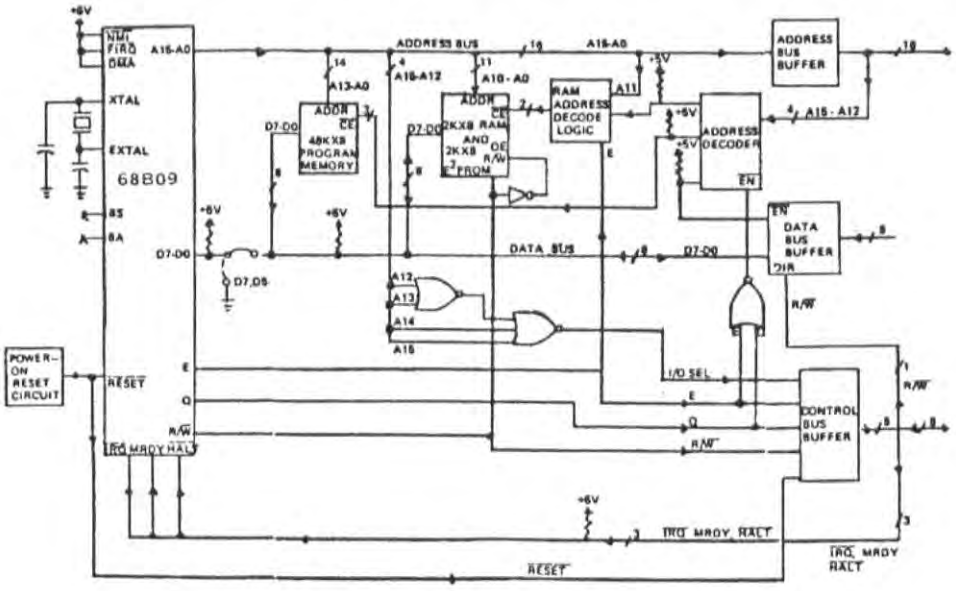


Figure 105-1. Functional Block Diagram, Microprocessor

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A105 MICROPROCESSOR

2020215-02 A

REF DES	DESCRIPTION	EIP NO.	PER ASSY	TYP MFG NO.	TYP FSCM NO.
C1	Mica, 24pF, 5%, 500V	2260018-00	2	CD10ED240J03	14655
C2	C1				
C3	Disc, 0.01µF, 20%, 100V	2150003-00	14	TG - S10	56289
C4	C3				
C5	Tant, 3.9µF, 10%, 15V	2300027-00	1	196D395X9015HA1	56289
C6	C3				
C7	C3				
C8	C3				
C9	Tant, 33µF, 10V	2300015-00	2	TAPA33M10	14433
C10	C3				
C11	C3				
C12	C3				
C13	C3				
C14	C3				
C15	C3				
C16	C3				
C17	C3				
C18	C3				
C19	C9				
CR1	H/C	2710016-00	1	5082-2835	28480
CR2	ZNR, 3.9V	2705228-01	1	IN5228	04713
R1	Met Ox, IM, 5%, 1/4W	4010105-00	1	RC07GF105J	81349
R2	Met Ox, 22K, 5%, 1/4W	4010223-00	1	RC07GF223J	81349
R3	Met Ox, 300K, 5%, 1/4W	4010304-00	1	RC07GF304J	81349
R4	Not used				
R5	Met Ox, 240, 5%, 1/4W	4010241-00	1	RC07GF241J	81349
R6	Met Ox, 4.7K, 5%, 1/4W	4010472-00	4	RC07GF472J	81349
R7	R6				
R8	R6				
R9	R6				
RN1	Res Ntwrk, 9 x 10k, 2%, 2W	4170003-00	3	782-1-R10K	80740
RN2	RN1				
RN3	RN1				
RN4	Res Ntwrk, 9x4.7k, 2%, 1.25W	4170014-00	1	4310R-101-472	32997
TP1 Thru TP10	Pin, T.P. Swage	2620032-00	10	460-2970-02-03	71279
U1	Int: Volt Comparator	3050311-00	1	MLM311P1	27014
U2	Microprocessor	3050025-00	1	MC68B09	04713
U3	Dvr Hex Bus/Buffer	3084365-00	1	SN74LS365N	01295
U4	Not used				
U5	3 Inp NOR Gate	3087427-00	1	DM74LS27	27014
U6	Dvr Line/Oct Buff Invg	3084244-00	2	SN74LS244N	01295
U7	Not used				
U8	Xcvr Octal Bus	3084245-00	1	SN74LS245N	01295

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A105 MICROPROCESSOR

2020215-02 A

REF DES	DESCRIPTION	EIP NO.	PER ASSY	TYP MFG NO.	TYP FSCM NO.
U9	2K x 8 CMOS RAM	3056116-00	1	HM6116LP-4	62786
U10	2K x 8E PROM	6420000-00	1	X2816A	60395
U11	PROM Set: 16K x 8	2060006-00	1		27128
U12	U11				
U13	U11				
U14	3 INP NAND Gate	3087410-00	1	DM74LS10	27014
U15	U6				
U16	4-16 Decoder	3074159-00	1	SN74159N	01295
U17	Hex Inverter	3087404-00	1	DM74LS04	27014
E1	Prog, Header, 16 Pin DIP	5000205-00	1	16-675-191T	51167
Y1	Xtal, 8.00 MHz	2030100-00	1	MP-1	ATRON

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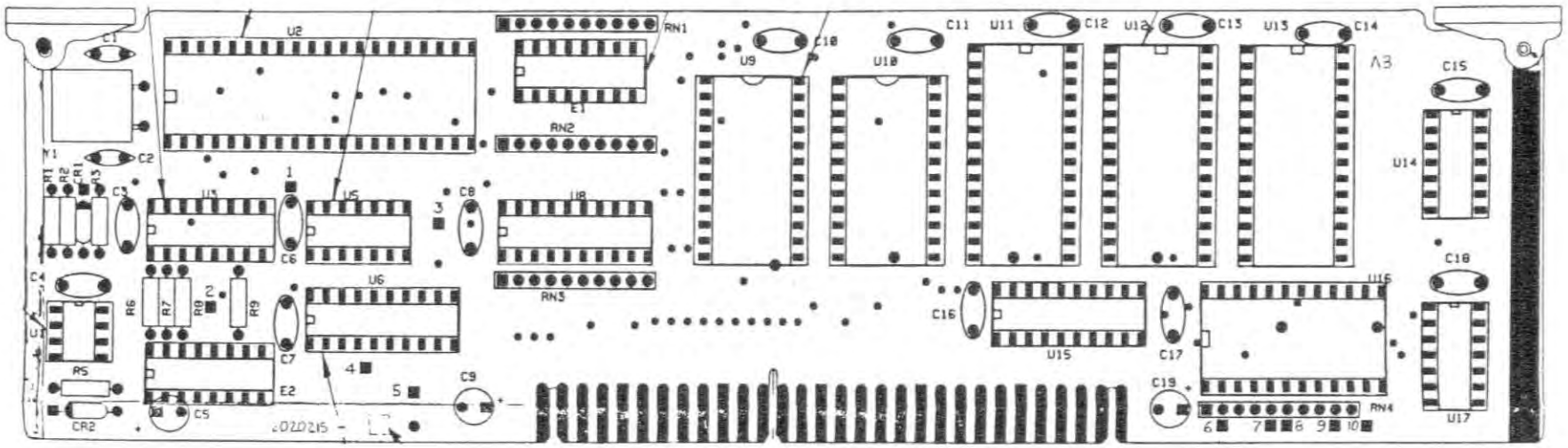
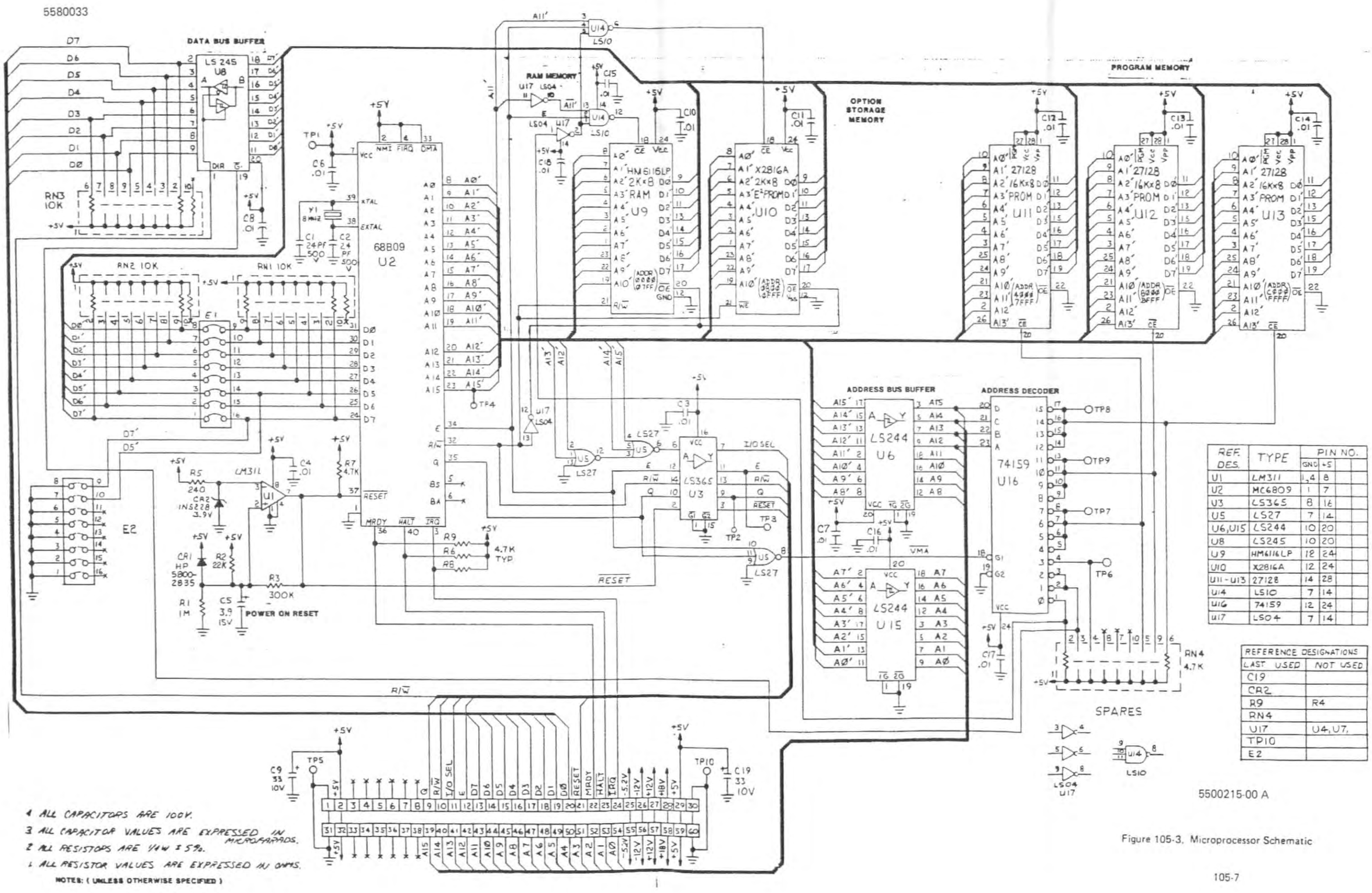


Figure 85-2. Component Locator, Microprocessor

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5580033



REF. DES.	TYPE	PIN NO. GND	+5		
U1	LM311	1,4	8		
U2	MC6809	1	7		
U3	LS365	8	16		
U5	LS27	7	14		
U6,U15	LS244	10	20		
U8	LS245	10	20		
U9	HM6116LP	12	24		
U10	X2816A	12	24		
U11-U13	27128	14	28		
U14	LS10	7	14		
U16	74159	12	24		
U17	LS04	7	14		

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C19	
CR2	
R9	R4
RN4	
U17	U4, U7,
TP10	
E2	

5500215-00 A

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL RESISTOR VALUES ARE EXPRESSED IN OHMS.
2. ALL RESISTORS ARE 1/4W ± 5%.
3. ALL CAPACITOR VALUES ARE EXPRESSED IN MICROFARADS.
4. ALL CAPACITORS ARE 100V.

Figure 105-3. Microprocessor Schematic

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A106
COUNT CHAIN
(2020136)

The Count Chain Assembly receives IF signals from the Band 3 IF Amplifier (A201B) and the Band 2 Converter (A109). It also receives a gate signal and a 100 kHz reference signal from the Gate Generator (A107). The count chain assembly selects the appropriate IF signal, gates it, and counts it to produce a BCD output that represents the input frequency. It also produces one or two IF output signals to be used for options at J3 and J4.

The A106 board receives two IF input signals on J1 and J2. The appropriate input is selected by enabling one of two differential amplifiers (U1A or U1B). Enabling of the appropriate amplifier is achieved by turning on a transistor switch (Q11 or Q12). The appropriate transistor is turned on by the output of an open collector inverter (U7C or U7A) driven by a TTL signal from the PIA (U10).

The output of the input selector differentially drives a squaring circuit. The squaring circuit consists of a differentially driven current mirror (Q1) driving a tunnel diode (CR5). The voltage across the tunnel diode changes abruptly between two states (approximately 0.2V and 0.5V). The signal across the diode drives the pulse forming circuit. This circuit begins with a high speed differential amplifier (Q2 and Q3). The output of this amplifier drives Q4 which is a current switch. The square wave current, from Q4's collector, drives an inductor (L1). The voltage across the inductor is a series of pulses; a positive pulse when Q4 turns on and a negative pulse when Q4 turns off. Diode CR5 tends to remove the negative pulses and increases the damping to improve the amplitude of the positive pulses. The positive pulses from the generator drive a pulse inverter (Q6). The pulse inverter is a high-speed zero bias amplifier that is biased at cut off by diode CR6.

The output of the pulse inverter (Q6) drives the input to the first decade counter (U2). The bias for the U2 input is established by a tracking bias supply (U3, Q7). The voltage at TP2 is equal to the voltage on U2 pin 1, plus a fixed DC offset selected by R45. The BCD outputs from U2 are slew-rate limited, and can only be seen after the counting ends and comes to rest. The carry output on pin 9 is an ECL level U2 signal, and is always visible.

The ECL output of U2 drives an ECL to TTL converter (Q8, Q9 and Q10). This converter is a differential amplifier with a cascode output buffer (Q8). The response of Q8 is improved by inductive peaking provided by L2. The output of Q8 drives a decade counter (U4) which in turn drives a third decade counter (U5). The BCD outputs of U4 and U5 are connected to a 6 decade counter (U6) which derives its clock information directly from the BCD outputs of U5. When counting is finished, 8 decades of BCD data are read by the microprocessor (through the PIA U10) from U6 by a time multiplex process. The multiplexer (set to the first digit by the end of the previous reset clock) loads the multiplex latches with the $\overline{\text{Latch Load}}$ clock, and steps to the remaining 7 digits with 7 pulses on the $\overline{\text{Scan Clock}}$ line. The first decade of BCD data from U2 is read directly from the PIA.

A single reset line is used to reset all count stages to zero before the next count cycle begins.

A real-time clock (U8, U9) is also on the count chain assembly. This circuit takes the 100kHz reference signal, that is coming from the Counter Interconnect Assembly (A100), and divides it by 10,000 to give a 10Hz (100ms) clock. The output from this clock is fed to the PIA to allow the microprocessor to gather time information at a 10Hz rate for timing functions within the program.

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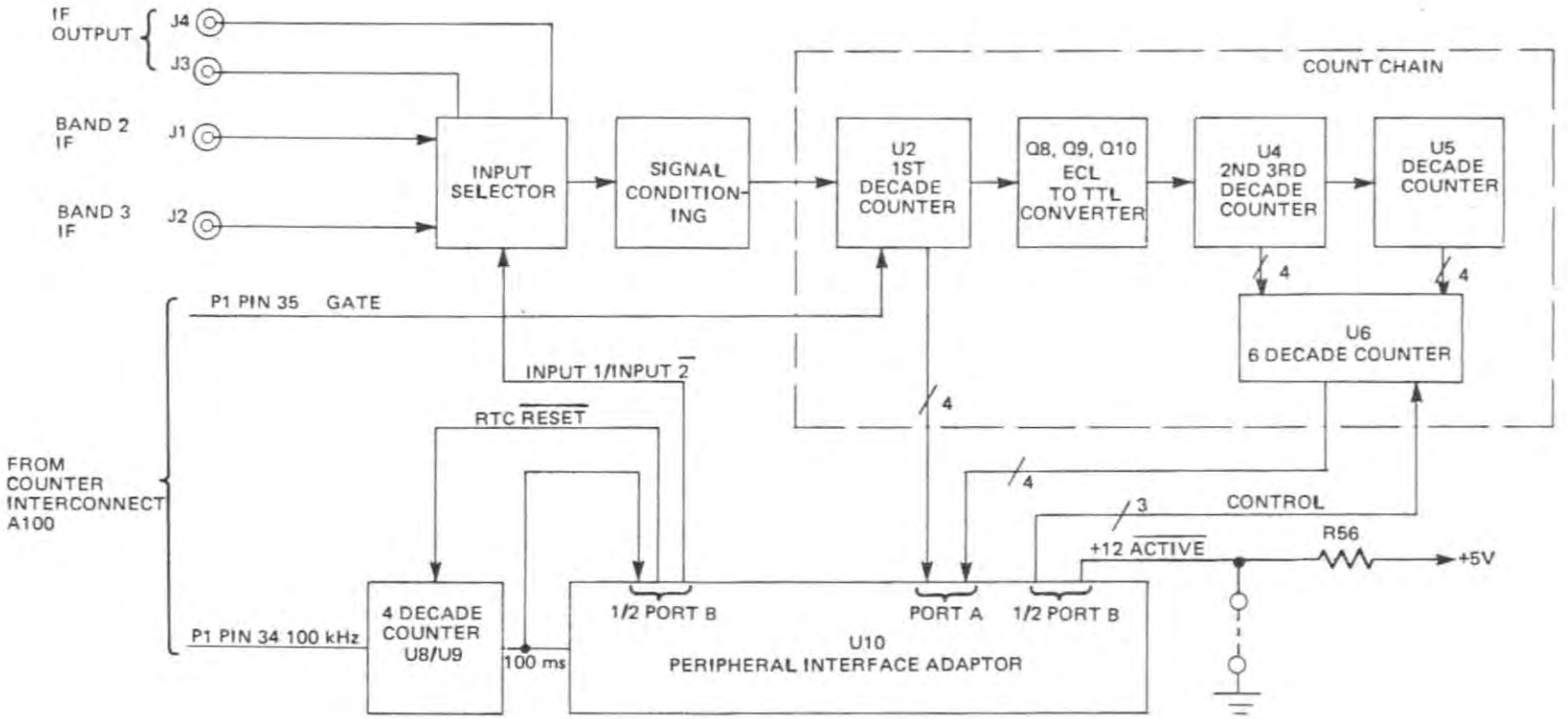


Figure 106-1. Count Chain Functional Diagram

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A106 COUNT CHAIN ASSY

2020136-03 B

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A106	Count Chain Assy	2020136	1	EIP	34257
C1	Tant, 33μF, 20%, 10V	2300015	5	TAG 20 - 33/10 - 50	14433
C2	Cer., .01μF, 20%, 100V	2150003-00	17	TG - S10	56289
C3	C2				
C4	C1				
C5	Mica, 10pF, 5%, 500V	2260012	1	CD100J03	72136
C6	Tant, 10μF, 20%, 25V	2300029	4	DF106M259	72136
C7	C2				
C8	C2				
C9	Cer., .001μF, 20%, 1KV	2150001	3	5GA - D10	56289
C10	C2				
C11	Not used				
C12	C9				
C13	C2				
C14	C6				
C15	C6				
C16	C2				
C17	C9				
C18	Not Used				
C19	Not Used				
C20	C1				
C21	C2				
C22	C1				
C23	Not Used				
C24 thru C28	C2				
C29	C1				
C30 thru C33	C2				
C34	C6				
CR1	Diode: Fast Sw	2704148	3	IN4148	07263
CR2	Zener, 6.2V	2705234	1	IN5234	04713
CR3	CR1				
CR4	Tunnel, Switching	2710033	1	G00010C	20754
CR5	Hot Carrier	2710004-00	1	5082 - 2835	28480
CR6	CR1				
L1	Part of Board				
L2	Inductor, 1μH	3510003	1	DD 1.0	72259
Q1	PNP, RF	4704959	1	2N4959	04713
Q2	NPN, Microwave	4710032	3	NE02137	33297
Q3	Q2				
Q4	PNP, RF	4710010	1	MPS - H81	04713
Q5	PND, RF GRADED	4710013	1	2N5179	34257
Q6	NPN, RF	4710026	1	NE73432B	0000S
Q7	Q2				
Q8	NPN, RF	4705179	3	2N5179	04713
Q9	Q8				
Q10	Q8				
Q11	PNP, General Purpose	4704126	2	2N4126	04713
Q12	Q11				

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A106 COUNT CHAIN ASSY, continued

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R1	Comp., 1.5K, 5%, 1/4 W	4010152	2	RC07GF152J	81349
R2	Comp., 6.2K, 5%, 1/4 W	4010622	2	RC07GF622J	81349
R3	Comp., 51 ohm, 2%, 1/4 W	4130510-00	2	C4/2%/51	24546
R4	Comp., 5.1K, 5%, 1/4 W	4010512	2	RC07GF512J	81349
R5	Comp., 2.7K, 5%, 1/4 W	4010272	2	RC07GF272J	81349
R6	Comp., 51 ohm, 5%, 1/4 W	4010510	1	RC07GF510J	81349
R7	Met Ox, 2K, 2%, 1/4 W	4130202	3	C4/2%/2K	24546
R8	Comp., 510 ohm, 5%, 1/4 W	4010511	1	RC07GF511J	81349
R9	Comp., 5.6 ohm, 5%, 1/4 W	4010569	5	RC07GF5R6J	81349
R10	R5				
R11	R9				
R12	Met Ox, 68 ohm, 2%, 1/4 W	4130680	1	C4/2%/68	24546
R13	Met Ox, 43 ohm, 2%, 1/4 W	4130430	1	C4/2%/43	24546
R14	Met Ox, 3.9K, 2%, 1/4 W	4130392	1	C4/2%/3.9K	24546
R15	R7				
R16	R4				
R17	R1				
R18	R2				
R19	Comp., 100 ohm, 5%, 1/4W	4010101	1	RC07GF101J	81349
R20	Met Ox, 56 ohm, 2%, 1/4 W	4130560	2	C4/2%/56	24546
R21	R9				
R22	R20				
R23	Comp., 360 ohm, 5%, 1/4 W	4010361	1	RC07GF361J	81349
R24	R9				
R25	Met Ox, S.A.T. (2K, 2% Nom)	4130999	1	C4/2%/XX	24546
R26	Met Ox, 39 ohm, 2%, 1/4 W	4130390	2	C4/2%/39	24546
R27	Met Ox, 200 ohm, 2%, 1/4 W	4130201	3	C4/2%/200	24546
R28	Met Ox, 270 ohm, 2%, 1/4 W	4130271	1	C4/2%/270	24546
R29	R3				
R30	Not used				
R31	Comp, 10 ohm, 5%, 1/4 W	4010100	1	RC07GF100J	81349
R32	Met Ox, 47 ohm, 2%, 1/4 W	4130470	1	C4/2%/47	24546
R33	Met Ox, 20 ohm, 2%, 1/4 W	4130200	1	C4/2%/20	24546
R34	Met Ox, 510 ohm, 2%, 1/3 W	4130511	1	C4/2%/510	24546
R35	R9				
R36	Met Ox, 1K, 2%, 1/4 W	4130102	3	C4/2%/1K	24546
R37	R26				
R38	Comp., 390 ohm, 5%, 1/4 W	4010391	1	RC07GF391J	81349
R39 thru R42	Comp, 10 K, 5%, 1/4 W	4010103	4	RC07GF103J	81349
R43	Met Ox, 20 K, 2%, 1/4 W	4130203	4	C4/2%/20K	24546
R44	R43				
R45	R36				
R46	R43				
R47	Met Ox, 18 ohm, 2%, 1/4 W (NOM) SAT	4130999	1	C4/2%/18	24546
R48	R43				
R49	Met Ox, 240 ohm, 2%, 1/4 W	4130241	1	C4/2%/240	24546
R50	R27				
R51	R27				
R52	R36				
R53	Met Ox, 430 ohm, 2%, 1/4W	4130431	1	C4/2%/430	24546

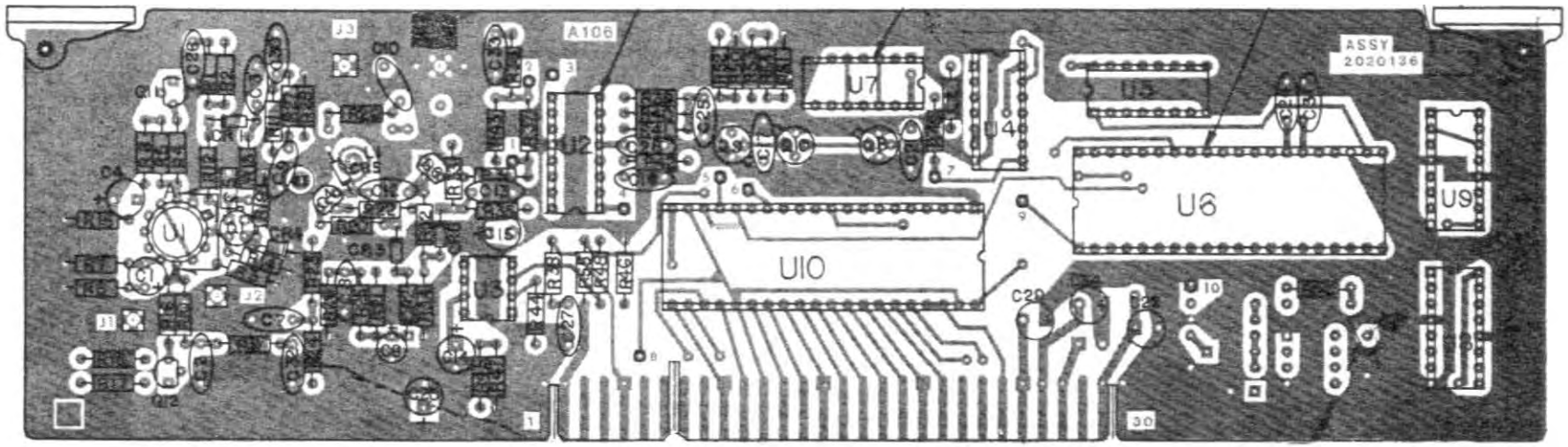
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A106 COUNT CHAIN ASSY, continued

2020136-03 B

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R54	R7				
R55	Comp., 1.8K, 5%, 1/4 W	4010182	1	RC07GF182J	81349
R56	Comp., 4.7K 5%, 1/4 W	4010472	1	RC07GF472J	81349
TP1 thru TP10	Conn., Pin, .040D	2620032	10	460-2970-0203	71279
U1	Dual/Diff Ampl	3043049	1	CA3049T	07263
U2	UHF, BCD, Decade Counter	3010637	1	SP8637B	58317
U2 Alt.	High Spd. Div.	3018636	Ref.	SP8636D	58317
U3	Op Amplifier	3040741	1	LM741CD	27014
U4	PST Decade Counter	3084196	1	SN74LS196N	01295
U5	4 Bit Decade Counter	3084160	1	SN74LS160N	01295
U6	6 Dec. Ctr/8 Dec. Latch	3057031	1	LS7031	01295
U7	Hex Inverter	3087404	1	SN 74LS04N	04713
U8	Decade Counter	3084490	2	74LS490N	01295
U9	U8				
U10	Periph. Interface Adapter	3086821	1	MC68B21P	04713

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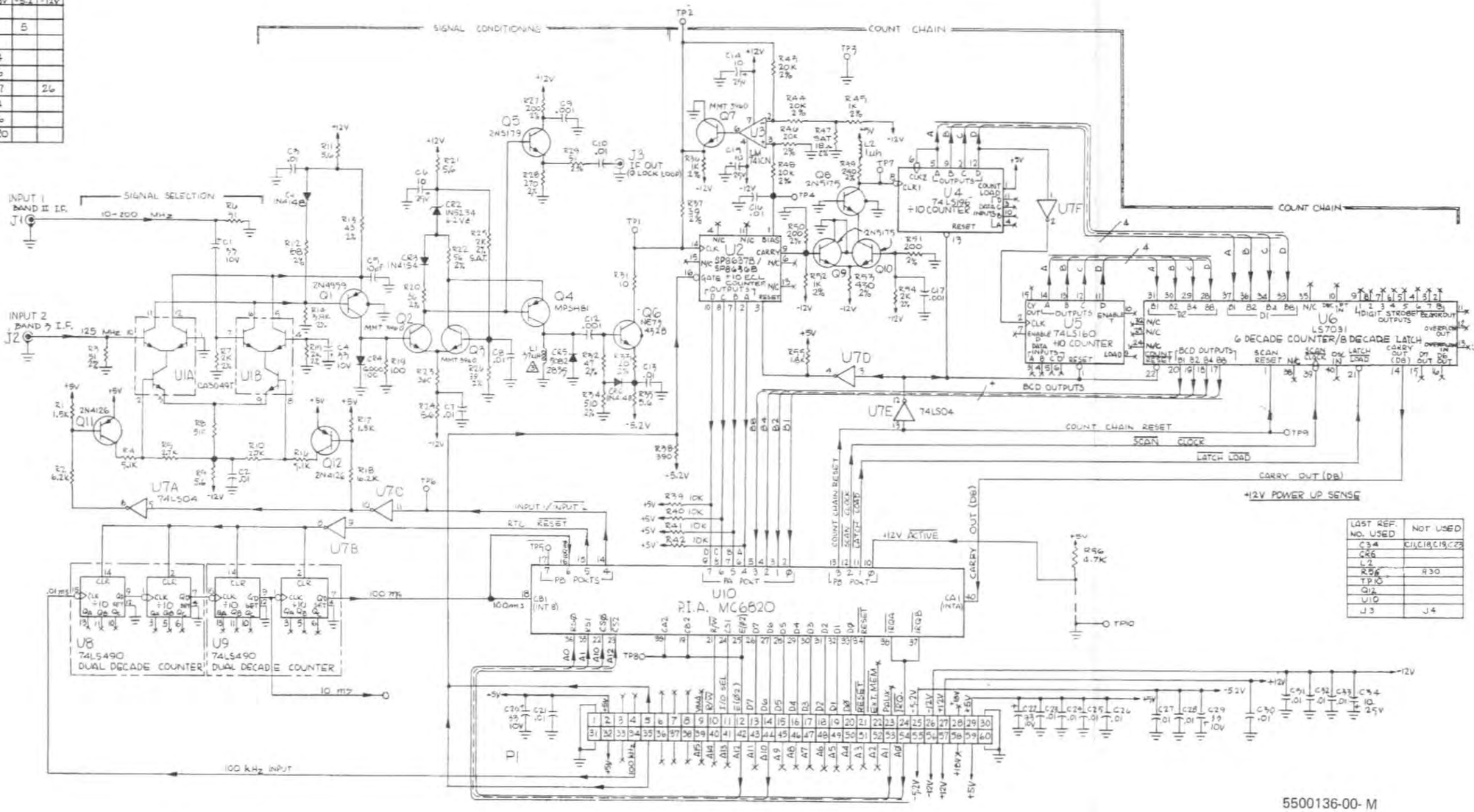
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Figure 106-2. Count Chain Component Locator

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I.C. NO	TYPE	PIN NO.			
		GND	+5V	-5.2	-12V
U1	CA3049T				
U2	SP8637B	12		5	
U3	LM741CN				
U4	74LS196	7	14		
U5	74LS160	8	16		
U6	74LS7031	25	27		26
U7	74LS04	7	14		
U8,U9	74LS490	8	16		
U10	MC6820	1	20		



LAST REF. NO. USED	NOT USED
C34	C1,C18,C19,C25
CR6	
L2	
R56	R30
TP10	
Q12	
U10	
J3	J4

5500136-00- M

Figure 106-3. Count Chain Schematic

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A107
GATE GENERATOR
(2020197)

This assembly performs the following functions.

- Reference Oscillator Control
- Gate Generation
- Band 3 Amplitude Determination
- Power Meter Control (Option 02 only)

REFERENCE OSCILLATOR CONTROL

This circuit selects, as the time base for the counter, either the internal reference oscillator or an external 10 MHz signal applied to the rear panel. This circuit provides a 100 kHz TTL level clock signal for the gate generator, a 10 MHz TTL level clock signal for the microwave converter and, in the internal oscillator mode, a 10 MHz signal (1 volt p-p into 50 ohms) to the rear panel.

The 10 MHz internal reference signal is applied to a switchable "analog to TTL" converter (Q1, Q2, Q3). When the Ref Int/Ext line is high the TTL converter is enabled. One output goes to drive Q4, giving a square wave (1V p-p into 50 ohms) on the 10 MHz Ref line. A second output goes to NAND gate U1 (also switchable for signal isolation. The output of U1 goes to J3 to be used by the microwave converter. The output of U1 also goes to the clock input of U2. U2 is a dual decade divider that divides by 100. The output of U2 is a 100 kHz TTL clock signal to the gate generator.

When the Reference Int/Ext line is set to external (low) the TTL converter (Q1, Q2, Q3) and driver (Q4) are disabled, TTL converter (Q5, Q6, Q7) is enabled, and U1 is set to select the external input. An external reference signal applied to the 10 MHz reference line is then converted to the input of U2.

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GATE GENERATOR

The Gate Generator must provide an accurate, stable, signal gate to the Count Chain. The gate must be switchable, in decade increments, between 100 micro sec and 1 sec. The gate generator consists of a programmable divide-by-N time base (U5), a dual flip-flop (U6A, U6B), and an ECL flip flop (U8). The divide ratio of U5, which determines the gate time, is set by U5 pins 12, 13, and 14 as follows.

Pin 12	Pin 13	Pin 14	Divide Ratio	Gate Time
0	0	1	10^1	100 μsec
0	1	0	10^2	1 Msec
0	1	1	10^3	10 Msec
1	0	0	10^4	100 Msec
1	0	1	10^5	1 sec

The outputs of U5 and U6 enable ECL flip-flop U8, but U8 is clocked directly from the 100kHz clock to insure gate accuracy.

When the gate is not active, U5 is permitted to free-run by holding U6B clear (T0). The gate is initialized by setting U6B. This clears U6A and clears U5 (T1). The next clock pulse sets U8 (T2). The gate is then enabled by momentarily clearing U6B (T3). The next clock sets U6A which enables U5 and U8 (T4). At T5 the gate is opened and U5 begins counting clocks (T5). Halfway through the gate, U5 pin 1 goes high (T6). After U5 has accumulated the proper number of clocks its output, pin 1, goes low. This sets U6B, which clears U6A, and sets U8 pin 7 high (T7). The next clock closes the gate (T8). The program next clears U6B (T9), which enables the gate to free-run again (T0). See figure 107-1.

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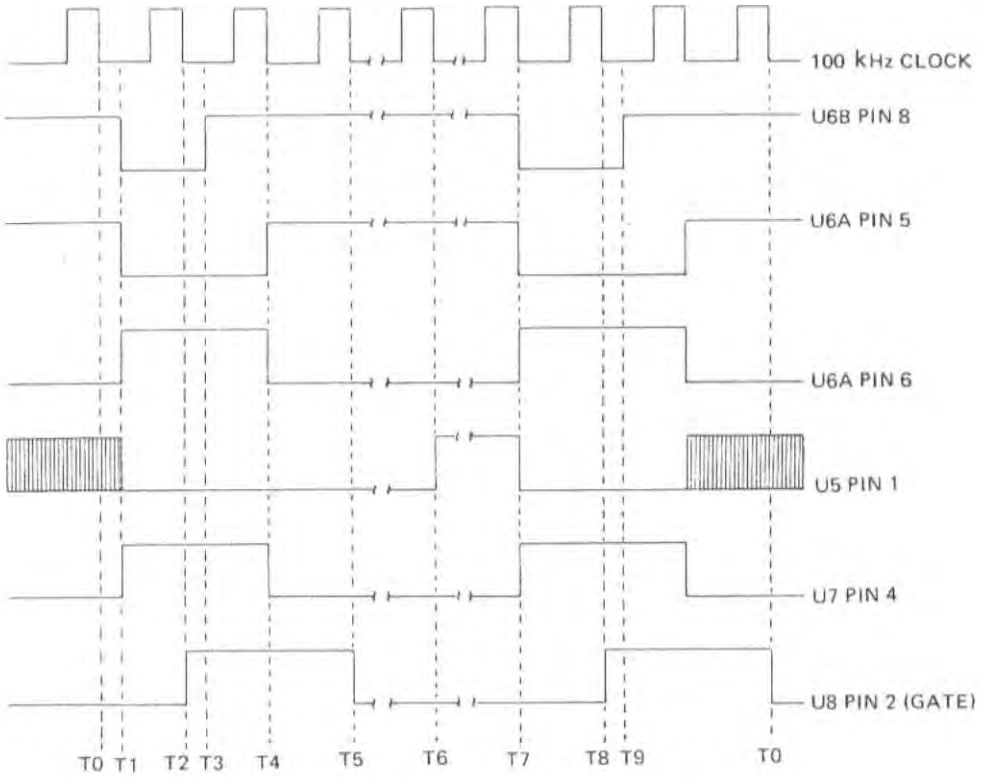


Figure 107-1. Gate Generator Timing Diagram

BAND 3 AMPLITUDE DETERMINATION

This circuit consists of three main parts.

- THE POWER METER ZERO DAC is used to automatically zero offsets in the Power Meter. It consists of two 8 bit latching DACs (U3, U4), and a comparator (U14A). All the latching DACs are driven in parallel by shift register U16, with the appropriate DAC being written to by the four write lines (U15, pins 2, 4, 6, 8). The coarse DAC (U3) has a range of ± 200 micro amps, and the fine DAC (U4) has a range of +1.5 micro amps. The Power Meter Zero DAC (U3) is adjusted so that on step 1 U14A is not set, but on the next step U14A is set. This adjusts the input to U14 to 0 volts, nulling any offsets in the power meter circuit.

- THE POWER METER consists of a 15 dB switchable gain stage (U9), an 8 bit DAC used as a variable attenuator (U10), a 100 mV comparator (U14B), and a latch (half of U17). Two variable attenuators are used, on counters equipped with the option 02 power meter, to provide greater resolution (U10, U12).

  When the detected signal from the microwave converter enters U9 the power meter is first set for maximum gain and minimum attenuation. Next the latch (U17) is reset. If the input to the comparator (U14B) is greater than 100mV, latch U17 will be set. The signal amplitude to the comparator is then reduced, and the process is repeated until latch U17 no longer gets set. The input amplitude can then be calculated from the switch and DAC settings. On counters without the power meter option the amplitude is calculated to a 3dB resolution. On counters with the power meter option the amplitude is calculated to a resolution of 0.1dB.

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- The POWER METER PROM (Option 02 only) contains a logic comparator (U21), a 2K X 8 prom (U20), and a bus driver (U19). The logic comparator is connected to the microprocessor address bus, and is configured to decode the 2K address range from 4000 Hex to 47FF Hex. The comparator output drives the chip select of the Prom, and the bus driver. The prom contains the Power Meter program as well as the power correction factors. Bus driver U19 is used as a buffer for driving the microprocessor data bus.

PERIPHERIAL INTERFACE ADAPTER (PIA)

The Peripherial Interface Adapter (U18) is used as the microprocessor I/O port. It has an address range from 9900 Hex to 9903 Hex. Peripheral Port A is at address 9900, and Peripheral Port B is at address 9902.

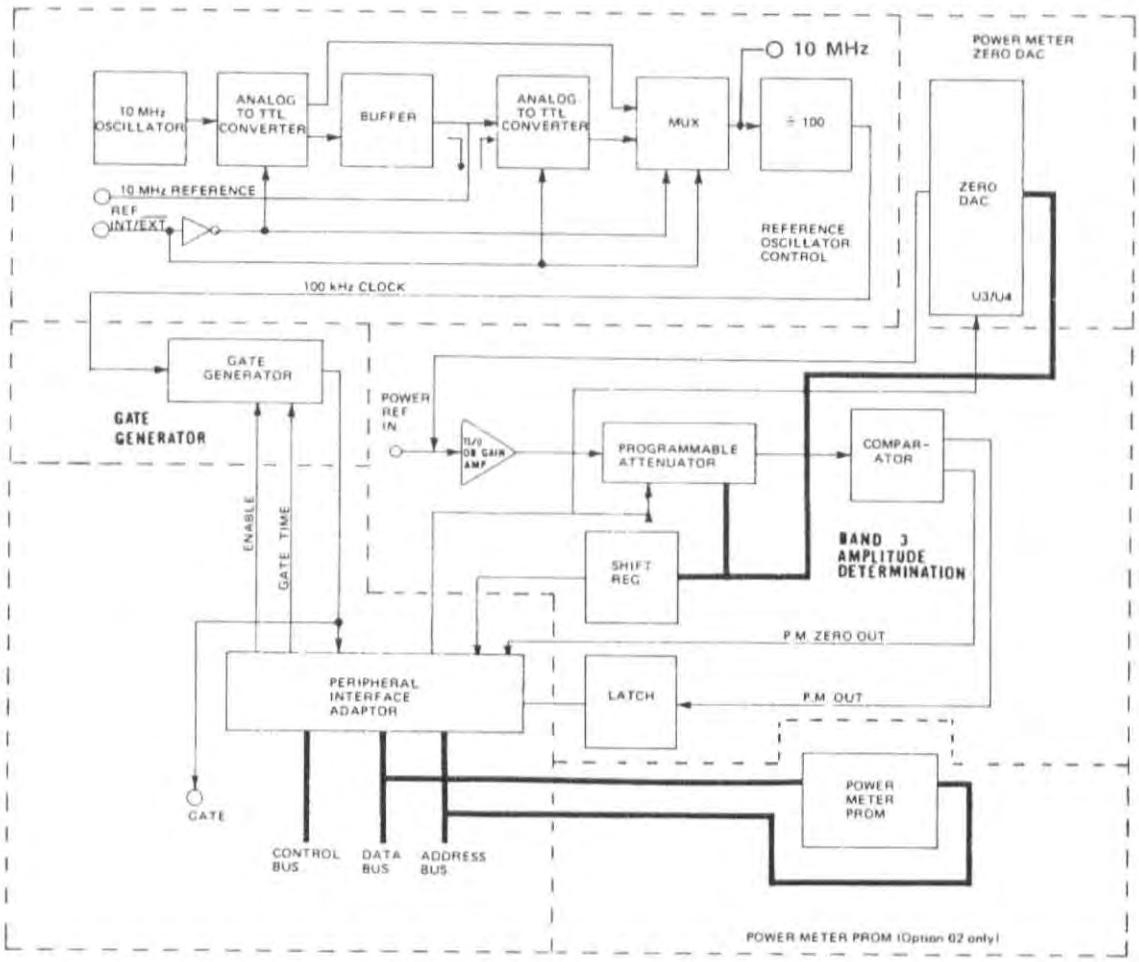


Figure 107-2. Gate Generator Block Diagram

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A107 GATE GENERATOR

2020197-09 A

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A107	Gate Generator Assy -05/06	2020197	1	EIP	34257
	A113 Crystal Osc	2030002	Ref		
C1	Cer, .01μF, 20%, 100V	2150003	15	TG-S10	72982
C2	C1				
C3	Tant, 33μF, 20%, 10V	2300015	4	TAPA33M10	14433
C4 thru C7	C1				
C8	Mica, 22pF, 5%, 500V	2269999	1	CD10ED220J03	72136
C9	Tant, 1μF, 20%, 35V	2300008	1	TAPA 1.0M35	14433
C10	Mica, 33pF, 5%, 500V	2260021	2	CD10ED330J03	72136
C11	Mica, 100pF, 5%, 500V	2260034	1	CD10FD101J03	72136
C12	C10				
C13 thru C15	C1				
C16	Tant, 10μF, 20%, 25V	2300029	2	DF106M25S	76718
C17	C1				
C18	C3				
C19	C3				
C20	C1				
C21	C1				
C22	C3				
C23	C1				
C24	C1				
C25	C16				
C26	C1				
CR1	Hot Carrier	2710004	1	5082-2835	28480
CR2	Hot Carrier	2710006	1	5082-2800	28480
CR3	CR1 - Option only				
CR4	Zener, 6.2V	2700827	1	IN827	
R1	Comp, 10 ohm, 5%, 1/4W	4010100	2	RC07GF100J	81349
R2	Comp, 1K, 5%, 1/4W	4010102	2	RC07GF102J	81349
R3	Comp, 620, 5%, 1/4W	4010621	2	RC07GF621J	81349
R4	Comp, 2.2K, 5%, 1/4W	4010222	3	RC07GF222J	81349
R5	Comp, 220, 5%, 1/4W	4010221	2	RC07GF221J	81349
R6	Comp, 510, 5%, 1/4W	4010511	2	RC07GF511J	81349
R7	Comp, 200, 5%, 1/4W	4010201	1	RC07GF201J	81349
R8	Comp, 27, 5%, 1/4W	4010270	1	RC07GF270J	81349
R9	Comp, 300, 5%, 1/4W	4010301	1	RC07GF301J	81349
R10	Comp, 4.7K, 5%, 1/4W	4010472	6	RC07GF472J	81349
R11	R1				
R12	Comp, 2K, 5%, 1/4 W	4010202	2	RC07GF202	81349
R13	R10				
R14	R4				
R15	R5				
R16	R6				
R17	R3				
R18	Met Ox, 5.6K, 2%, 1/4W	4130562	1	C4/2%/5.6K	24546
R19	Met Ox, 3.3K, 2%, 1/4W	4130332	1	C4/2%/3.3K	24546
R20	Met Ox, 27, 2%, 1/4W	4130270	1	C4/2%/27	24546
R21	Comp, 2.7K, 5%, 1/4W	4010272	1	RC07GF272J	81349
R22	R10				
R23	R10				
R24	R2				

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A107 GATE GENERATOR continued

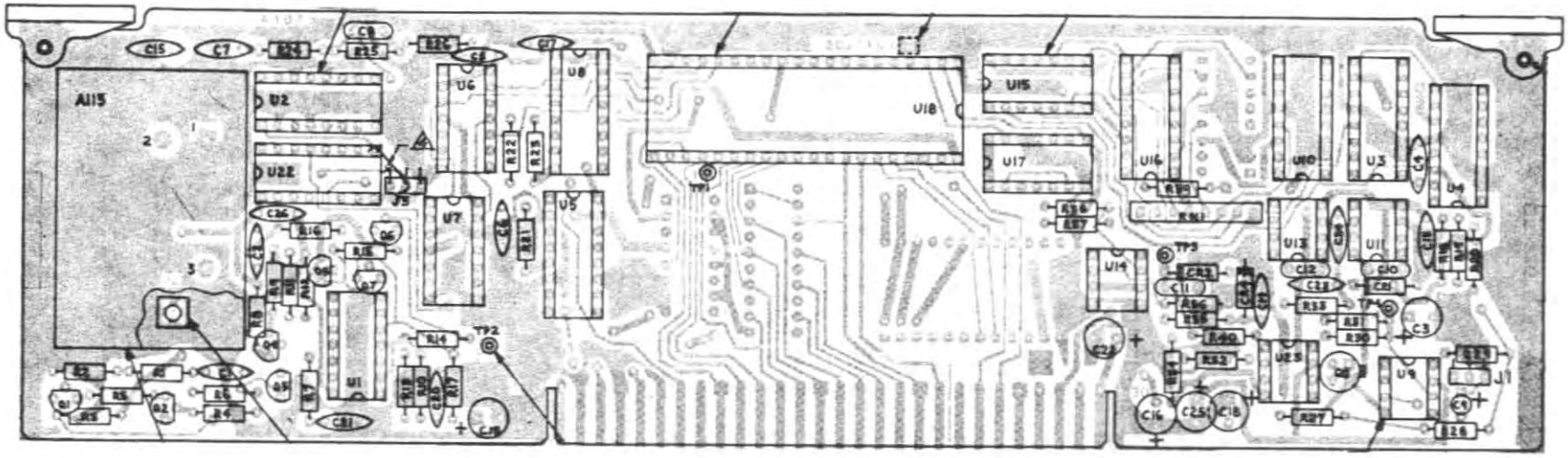
2020197-09 A

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R25	R12				
R26	R4				
R27	Met Ox, 30K, 2%, 1/4W	4130303	1	C4/2%/30K	24546
R28	Met Ox, 39K, 2%, 1/4W	4130393	1	C4/2%/39K	24546
R29	Prec, 1.69K, 1%, 1/10W	4051691	1	RN55C1691F	81349
R30	Prec, 1.82K, 1%, 1/10W	4051821	1	RN55C1821F	81349
R31	Prec, 57.6K, 1%, 1/10W	4055762	1	RN55C5762F	81349
R32	Comp, 36K, 5%, 1/4W	4010363	1	RC07GF363F	81349
R33	Comp, 15K, 5%, 1/4W	4010153	1	RC07GF153F	81349
R34	Met Ox, 750, 2%, 1/4W	4130751	1	C4/2%/750	24546
R35	Prec, 6.19K, 1%, 1/10W	4056191	1	RN55C6191F	81349
R36	Prec, 100, 1%, 1/8W	4051000	1	RN55C1000F	81349
R37	R10				
R38	R10				
R39	Met Ox, 10K, 2%, 1/4W	4130103	2	C4/02/10K	24546
R40	R39				
*R41	Comp, 10K, 5%, 1/4W	4010103	1	RC07GF103J	81349
RN1	Network, 5 X 10 K, 0.3W, 2%	4170005	1	4608X-101-682	80740
Q1	NPN - General Purpose	4704124	4	2N4124	
Q2	PNP - General Purpose	4704126	3	2N4126	
Q3	Q1				
Q4	Q2				
Q5	Q1				
Q6	Q2				
Q7	Q1				
Q8	DMOS, FET SW	4710031	1	SD215	18324
U1	Quad NAND	3084132	1	DM74LS132	01295
U2	Dual Decade Counter	3084490	1	SN74LS490N	01295
U3	8 Bit DAC	3057524	3	AD7524JN	
U4	U3				
U5	Digital P Chan. MOS Divider	3035009	1	MK5009P	
U6	D Type Pos Flip-flop	3087474	2	DM74LS74N	01295
U7	Quad 2-1 NP NOR Gate	3087402	1	DM74LS02N	01295
U8	Digital Dual D Flip-flop	3110131	1	MC10131L	04713
U9	Dual Low Noise Op Amp	3045534	1	NE5534N	
U10	8 Bit DAC Buff	3057525	2	AD7524LN	
U10	U3				
U11	Op Amplifier	3040308	2	LM308AN	27014
U12	U10 Buff				
U13	U11				
U14	Comparator Dual Low Pwr/Volt	3050393	1	LM393N	27014
U15	Hex Buffer/Driver	3007407	1	DM7407N	27014
U16	Dual 4 Bit Static S/R	3034015	1	MC4015B	04713
U17	U6				
U18	Periph. To MC6800	3086821	1	68B21P	01295
U19	Oct. Buffer (Option* 02 Only)	3084244	1	SN74LS244 (6400002-04)	01295
U20	PROM Set (Option* 02 Only)	2060002-03	1	TI-TM2516	04713
U21	6 Bit Comparator Bus (Option* 02 Only)	3078136	1	DM8136	27014
U22	Quad Dual Flip-flop	3084175	1	SN74LS175	01295
U23	Op Amp/Lin	3040741	1	LM741CN	27014
TP1-4	PC, Pin .040D	2620032	4	460-2970-02-03	71279

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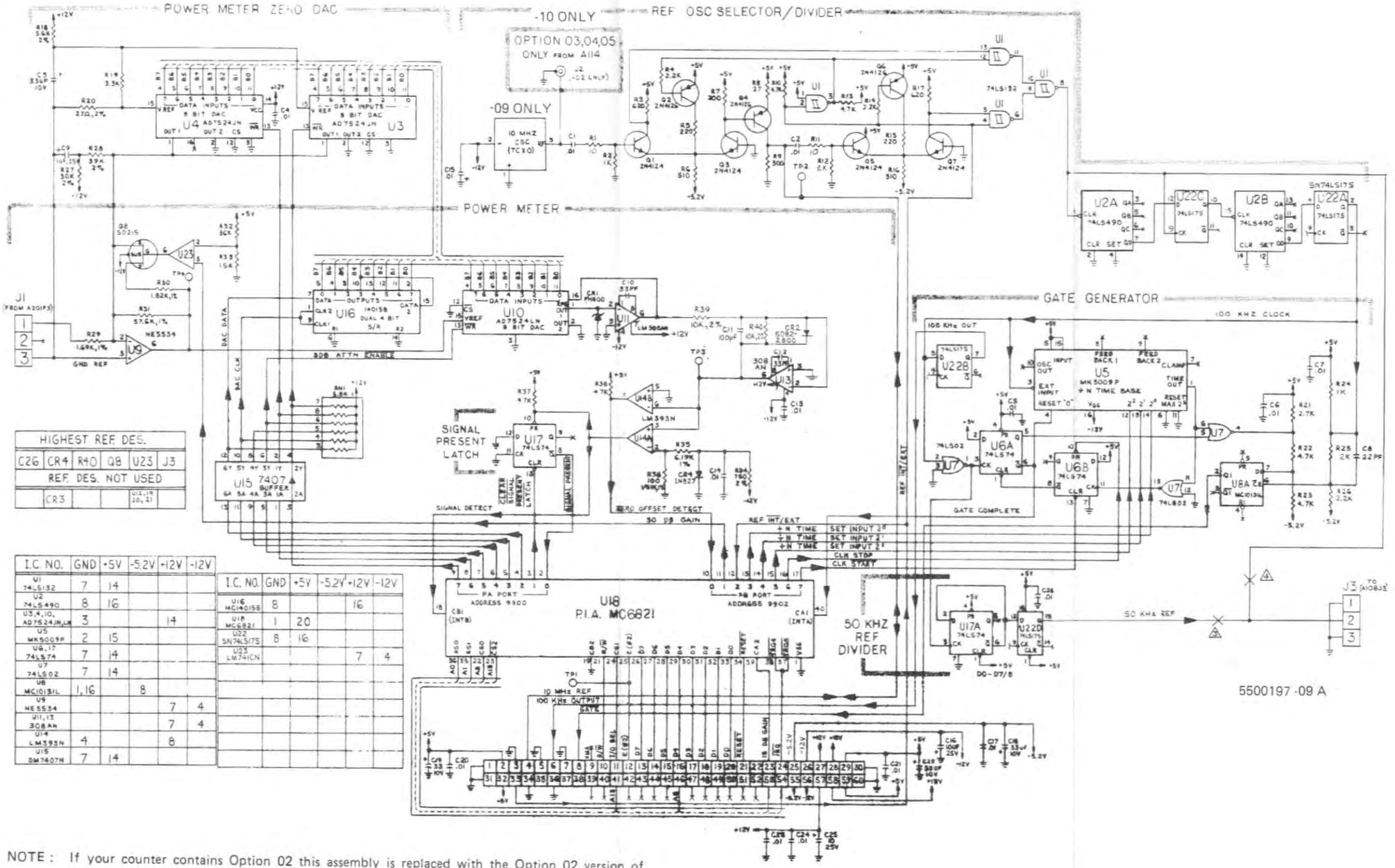


2020197-09-A

Figure 107-3. Gate Generator Component Locator

NOTE : If the counter contains Option 02 this board is replaced with 2020197-03/04. Refer to Section 10, Option 02 for the 03/04 version of this assembly.

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I.C. NO.	GND	+5V	-5.2V	+12V	-12V
U1 74LS132	7	14			
U2 74LS490	8	16			
U3,4,10, AD7524JN,LN	3			14	
U5 MK5009P	2	15			
U6,17 74LS74	7	14			
U7 74LS02	7	14			
U8 MC10131L	1,16		8		
U9 NE5534				7	4
U11,13 308AN				7	4
U14 LM393N	4			8	
U15 DM7407N	7	14			

I.C. NO.	GND	+5V	-5.2V	+12V	-12V
U16 MC14015B	8			16	
U18 MC6821	1	20			
U22 SN74LS175	8	16			
U23 LM741CN				7	4

NOTE : If your counter contains Option 02 this assembly is replaced with the Option 02 version of the Gate Generator part number 5500197-03/04. See Section 10 for Option 02.

5500197 -09 A

Figure 107-4. Gate Generator Schematic

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A108
CONVERTER CONTROL
(2020200)

The Converter Control performs two major functions. One of the functions is to provide a precise yig tuning current which is controlled by the microprocessor via P.I.A. U4. The other function is to phase lock the VCO in the microwave converter to a selected harmonic of a 50 kHz reference signal to provide a synthesized L.O. The converter control also permits the microprocessor to control the L.O. power amplifier and provides the microprocessor input for the I. F. threshold signal.

YIG FREQUENCY CONTROL DAC and DRIVERS

The yig tuning current is supplied by the yig driver (U3, Q1, Q2, & Q3) which is controlled by the DAC. The DAC is composed of a 12 bit monolithic DAC (U2), summing amplifier (U1) and resistors to provide a total resolution of 14 bits. PA ports 0 and 1 of the P.I.A. (U4) are used to drive the 2 least significant bits of the DAC directly. A change in the least significant bit of the DAC corresponds to a yig frequency change of 2 MHz. A voltage analog of yig current appears across R25 and is compared to the DAC output at the summing junction of U3, with resistors R1 and R19.

The slope of yig current vs DAC voltage is compensated with corrections through software.

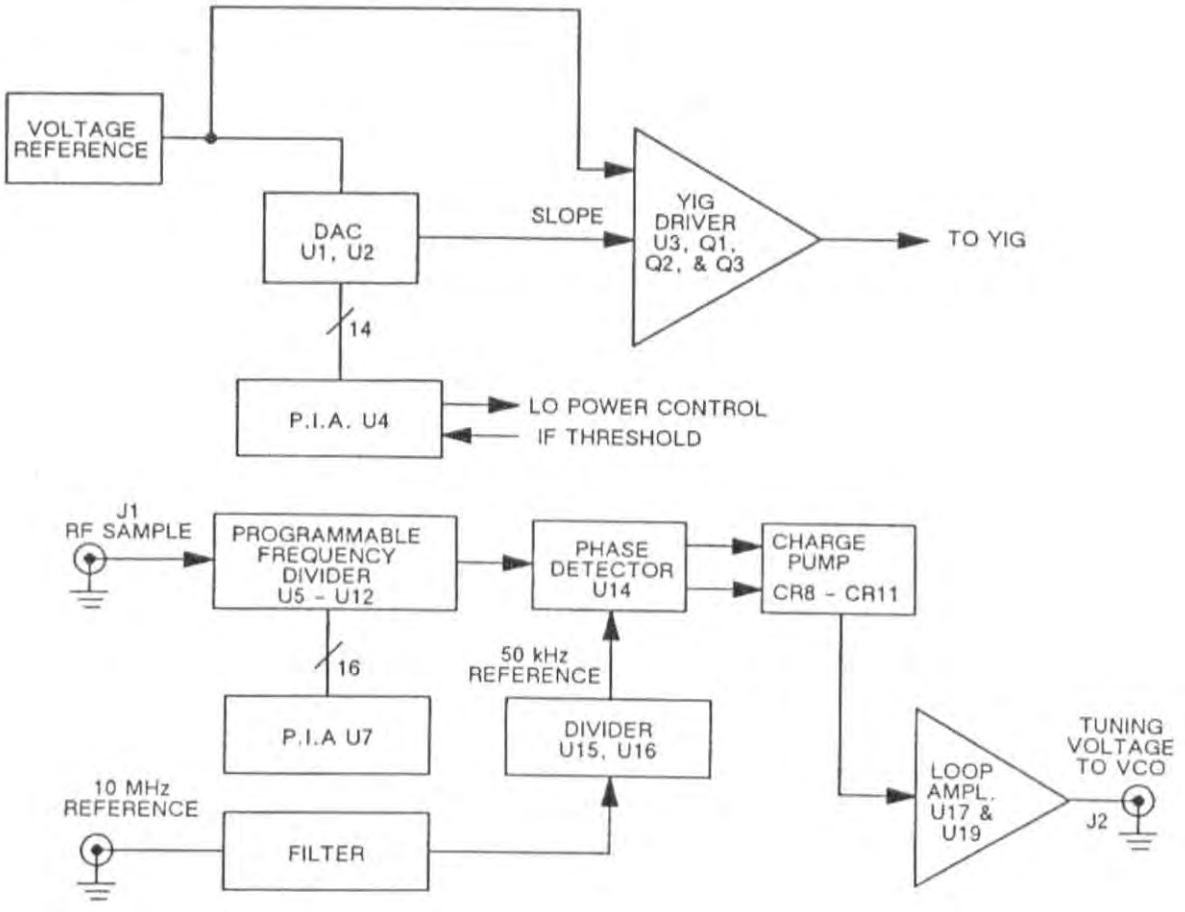


Figure 108-1. Converter Control Diagram

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VCO CONTROL

The VCO control, together with the VCO, form a phase lock loop frequency synthesizer. The frequency range over which the synthesizer is used is from 370 MHz to 500 MHz.

An output of the VCO (via a buffer amplifier, U2, on the Band 2 converter board) is applied to the programmable frequency divider (U5-U13). The programmable frequency divider is programmed by the microprocessor via P.I.A. U7. The output of the programmable frequency divider is compared to the 50 kHz reference (derived from a 10 MHz clock from the gate generator board) in the phase detector U14. A phase difference between the divided down VCO and the 50 kHz reference will result in an output from the phase detector. The phase detector has two output ports, a pump-up port and a pump-down port. Pump-down is U14, pin 2. Pump-down is normally high and goes low to reduce the VCO frequency. Pump-up is U18, pin 3. Pump-up is normally low and goes high to increase the VCO frequency. The outputs of the phase detector go to the charge pump, which converts them to a single tri-state output. The charge pump output is open with no pump command, sources current with pump-up, and sinks current with pump-down. The output of the charge pumps is connected to the input of the loop amplifier U19 and U17. The loop amplifier provides the proper gain and filtering to achieve the desired loop response. The output of the loop amplifier is the VCO tuning voltage.

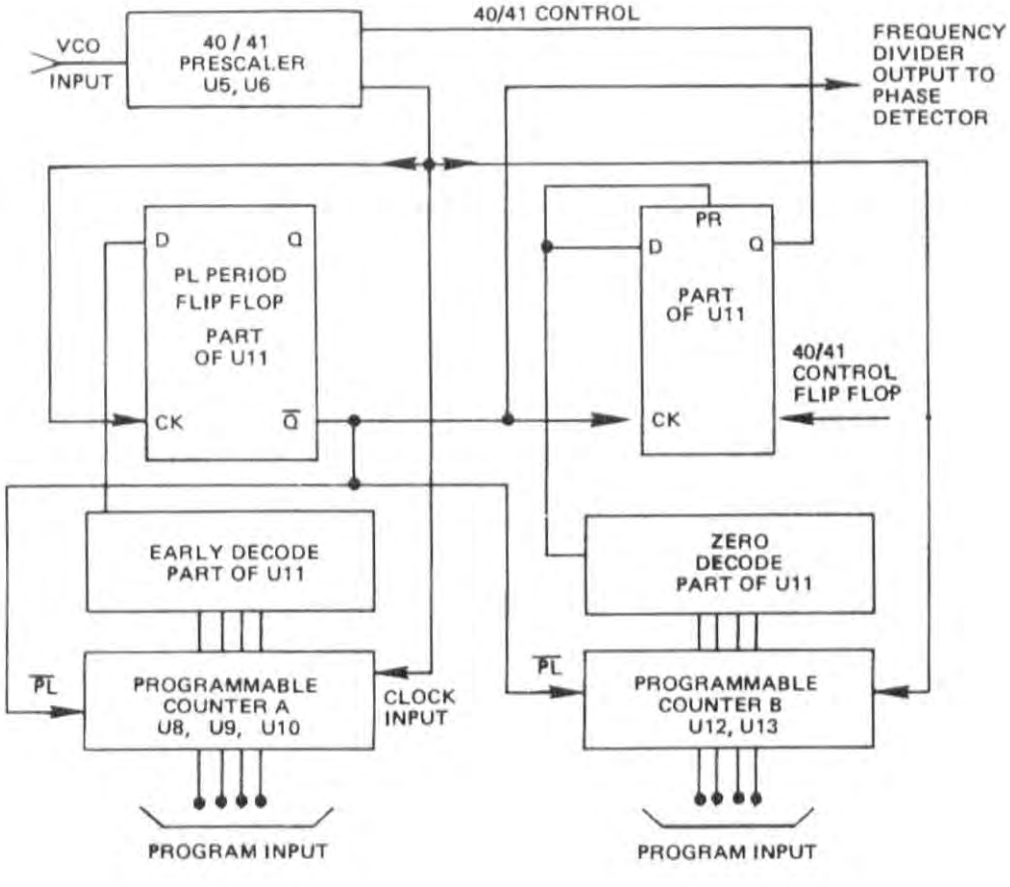


Figure 108-2. Programmable Frequency Divider Diagram

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