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CPV5370 Single Board Computer and CPTM04 Transition Module

Installation and Use

CPV5370A/IH3

September 2004 Edition

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The safety precautions listed below represent warnings of certain dangers of which Motorola is aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

Ground the Instrument.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. If the equipment is supplied with a three-conductor AC power cable, the power cable must be plugged into an approved three-contact electrical outlet, with the grounding wire (green/yellow) reliably connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards and local electrical regulatory codes.

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Do not operate the equipment in any explosive atmosphere such as in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment could result in an explosion and cause injury or damage.

Keep Away From Live Circuits Inside the Equipment.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified service personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Service personnel should not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, such personnel should always disconnect power and discharge circuits before touching components.

Use Caution When Exposing or Handling a CRT.

Breakage of a Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, do not handle the CRT and avoid rough handling or jarring of the equipment. Handling of a CRT should be done only by qualified service personnel using approved safety mask and gloves.

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Observe Warnings in Manual.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.



Warning

To prevent serious injury or death from dangerous voltages, use extreme caution when handling, testing, and adjusting this equipment and its components.

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All Motorola PWBs (printed wiring boards) are manufactured with a flammability rating of 94V-0 by UL-recognized manufacturers.

EMI Caution



Caution

This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference (EMI) if not installed and used with adequate EMI protection.

Lithium Battery Caution

This product contains a lithium battery to power the clock and calendar circuitry.



Caution

Danger of explosion if battery is replaced incorrectly. Replace battery only with the same or equivalent type recommended by the equipment manufacturer. Dispose of used batteries according to the manufacturer's instructions.



Attention

Il y a danger d'explosion s'il y a remplacement incorrect de la batterie. Remplacer uniquement avec une batterie du même type ou d'un type équivalent recommandé par le constructeur. Mettre au rebut les batteries usagées conformément aux instructions du fabricant.



Vorsicht

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EN55024 “Information technology equipment—Immunity characteristics—Limits and methods of measurement”

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About This Manual

This *CPV5370 Single Board Computer and CPTM04 Transition Module Installation and Use* manual describes the installation, components, and configurations of the CPV5370 Single Board Computer and CPTM04 Rear Transition Module. The CPV5370 uses an optional transition module for peripheral and network connections required at the rear of the chassis. Use this guide for general and technical information about the CPV5370 CompactPCI System CPU. These tables describe the configurations available for the CPV5370, CPTM04, and CPMEZZ Memory Mezzanine models.

CPV5370 Configurations

Model Numbers	Description
CPV5370-700-01	700 MHz CPU, 256MB SDRAM, 1 PMC site, CompactFlash™ connector
CPV5370-700-03	700 MHz CPU, 512MB SDRAM, 1PMC site, CompactFlash™ connector
CPV5370-700-04	700 MHz CPU, 512MB SDRAM, 1 PMC site, hard drive site
CPV5370-700-05	700 MHz CPU, 1GB SDRAM, 1 PMC site, CompactFlash™ connector
CPV5370-1G-05	1.0 GHz CPU, 1GB SDRAM, 1 PMC site, CompactFlash™ connector
CPV5370-1G-06	1.0 GHz CPU, 1GB SDRAM, 1 PMC site, hard drive site
CPTM04 Rear Transition Module	
CPTM04	RTM with front panel keyboard/mouse, dual Ethernet, video, COM2, and optional PIM module knockout
CPMEZZ Memory Mezzanine	
CPMEZZ-256B	256MB Memory Mezzanine, bottom installation
CPMEZZ-256T	256MB Memory Mezzanine, top installation

Summary of Changes

The following changes have been made since the last release of this manual.

Date	Changes	Replaces
September 2004	Added current configurations. Updated to current MCG publication standards.	CPV5370A/IH2
November 2003	Incorporates information in support of the 1 GHz versions of the CPV5370 that are available.	CPV5370A/IH1

Overview of Contents

This section contains a short description of the content of each chapter and appendix in this manual.

Chapter 1, *Hardware Preparation and Installation*, provides a product description, input/output interfaces and special functions and a block diagram.

Chapter 2, *CPTM04 Installation*, discusses the CPTM04 and provides installation instructions and pin assignments.

Chapter 3, *Starting Up the CPV5370*, provides information about ESD, board installation and power up, replacement of lithium batteries, locations of connectors and indicators.

Chapter 4, *Functional Description*, describes the functional characteristics of the CPV5370 including information about the PCI Bus and the watchdog timer.

Chapter 5, *Memory Maps and Programming Information*, contains the memory maps and FPGA registers.

Chapter 6, *Connector Pin Assignments*, provides pin assignments for the CPV5370.

Appendix A, *Specifications*, provides physical, electrical, and mechanical board specifications.

Appendix B, *Thermal Analysis*, discusses the information necessary to conduct thermal evaluations of your board in specific system configurations.

Appendix C, *Related Documentation*, lists publications that provides more information on this product.

Who Should Use This Guide

The information in this guide is written for system installers, original equipment manufacturers (OEM) and technicians. The procedures assume familiarity with the safety practices and regulatory compliance required for using and modifying electronic equipment. Personnel who install CompactPCI systems should be trained and experienced with the installation of computers and computer equipment.

Comments and Suggestions

In all your correspondence, please list your name, position, and company. Be sure to include the title and part number of the manual and tell how you used it. Then tell us your feelings about its strengths and weaknesses and any recommendations for improvements.

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Reader Comments DW164
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Conventions Used in This Manual

The following typographical conventions are used in this document:

bold

is used for user input that you type just as it appears; it is also used for commands, options and arguments to commands, and names of programs, directories and files.

italic

is used for names of variables to which you assign values. Italic is also used for comments in screen displays and examples, and to introduce new terms.

`courier`

is used for system output (for example, screen displays, reports), examples, and system prompts.

<**Enter**>, <**Return**> or <**CR**>

<**CR**> represents the carriage return or Enter key.

CTRL

represents the Control key. Execute control characters by pressing the Ctrl key and the letter simultaneously, for example, **Ctrl-d**.

Hardware Preparation and Installation

1

This chapter includes information about:

- Features and functions of the CPV5370
- Basic preparation and installation
- ESD precautions
- Replacing lithium batteries

Note This document treats the CPV5370 as a component of a system, and assumes that you install it in a CompactPCI backplane that is PICMG-compliant.

Introduction

The CPV5370 Single Board Computer (SBC) is a hot swap, single-slot, CompactPCI® compliant computer. It is powered by an Intel Pentium® III BGA2 processor and an Intel 440GX chip set. The single board computer supports 64-bit CompactPCI bus add-in cards and 32-bit host initiated/targeted transactions. Hot swap and Motorola high availability (HA) extensions are also supported. It serves as a standard CompactPCI system controller.

The Pentium® III processor provides two USB ports, PCI EIDE, an on-board Frame AGP graphics controller, dual on-board Ethernet controllers, and standard PC I/O plus a PMC site for expansion. The CPV5370 supports up to 1GB of on-board DRAM memory.

The CPV5370 meets the needs of embedded application developers. Typical applications include broadband data or intelligent network switching, CTI server, industrial control and automation, military and aerospace, and medical, scientific, or imaging products.

The optional CPTM04 Rear Transition Module provides backplane I/O for the PCI Mezzanine Card (PMC) sites and on-board devices. See *CPTM04 Installation* for detailed information on the CPTM04.

On-Board and Front Panel Components on the CPV5370

The CPV5370's front panel has connectors and switches for:

- Ethernet 1 and 2
- COM1 asynchronous serial port
- One PMC panel (keyed for +5.0V PCI)
- Video port
- Keyboard/mouse
- Board reset (push button switch)

LED indicator lights on the front panel display of the CPV5370 include:

- Left LED - Power (green)/Alarm (red)
- Right LED - Hard Disk Drive (green)

Input/Output Interfaces

Refer to Table 1-1 for brief descriptions of the input/output interfaces on the CPV5370 Single Board Computer and CPTM04 Rear Transition Module.

Note When the identical function is available through the CPV5370's front panel and the rear transition module, you can use either the front or the rear, not both.

Table 1-1. Input/Output Interfaces on the CPV5370 and the CPTM04

Function	CPV5370		CPTM04 Transition Module	
	Front Panel	On-board	Rear Panel	On-board
Ethernet 1	RJ45	-	RJ45	-
Ethernet 2	RJ45	-	RJ45	-
COM1 (Serial Port 1)	9-pin D-sub	-	-	10-pin shrouded
COM2 (Serial Port 2)	-	-	9-pin D-sub	-
PMC Panel	PMC 1 Device	-	PMC 1 Device	-
PMC Panel	-	-	-	-
Keyboard/Mouse	6-pin mini-DIN	-	6-pin mini-DIN	12-pin connector
Floppy	-	-	-	34-pin connector
Parallel	-	-	-	26-pin shrouded
USB 0 and USB 1	-	-	-	2-stacked 4-pin
Video	15-pin D-sub	-	15-pin D-sub	-
Primary IDE [1]	-	40-pin connector	-	-
Secondary IDE	-	-	-	40-pin connector
CompactFlash [2]	-	50-pin connector	-	50-pin connector

[1] Primary IDE available on CPV5370-700-04 and CPV5370-1G-06

[2] CompactFlash available on CPV5370-700-01, -03, and -05; CPV5370-1G-05

❑

Refer to Figure 1-1 for the location of the CPV5370 front panel components.

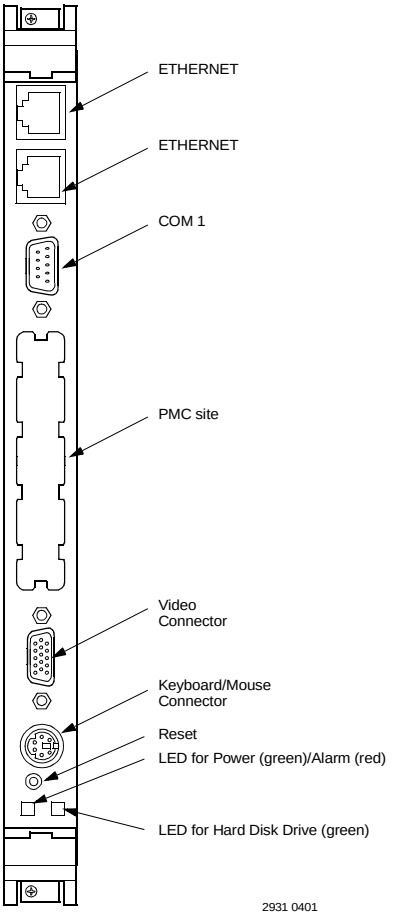


Figure 1-1. CPV5370 Single Board Computer Front Panel

The CPV5370 carries components on both sides. Table 1-2 lists the connectors available to support devices. Also refer to Chapter 6, *Connector Pin Assignments*.

Table 1-2. CPV5370 Connectors and Components

Connector	Description
J1	CompactPCI Bus Connector
J2	CompactPCI Bus Connector
J3	Rear I/O CompactPCI Connector
J4	Rear I/O CompactPCI Connector
J5	Rear I/O CompactPCI Connector
J7	Keyboard/mouse
J9	Ethernet 2 connector
J10	Ethernet 1 connector
J11	PMC bus signal connector
J12	PMC I/O connector
J13	PMC bus signal connector
J14	PCI64 bit PCI extension on PMC2 connector
J16	Memory Mezzanine
J17	Video connector
J18	Primary IDE connector
J19	COM1 (asynchronous serial port)
J21	Debug port
J23	Primary IDE CompactFlash

Refer to Figure 1-2 for the location of CPV5370 on-board components. There are no on-board configuration jumpers.

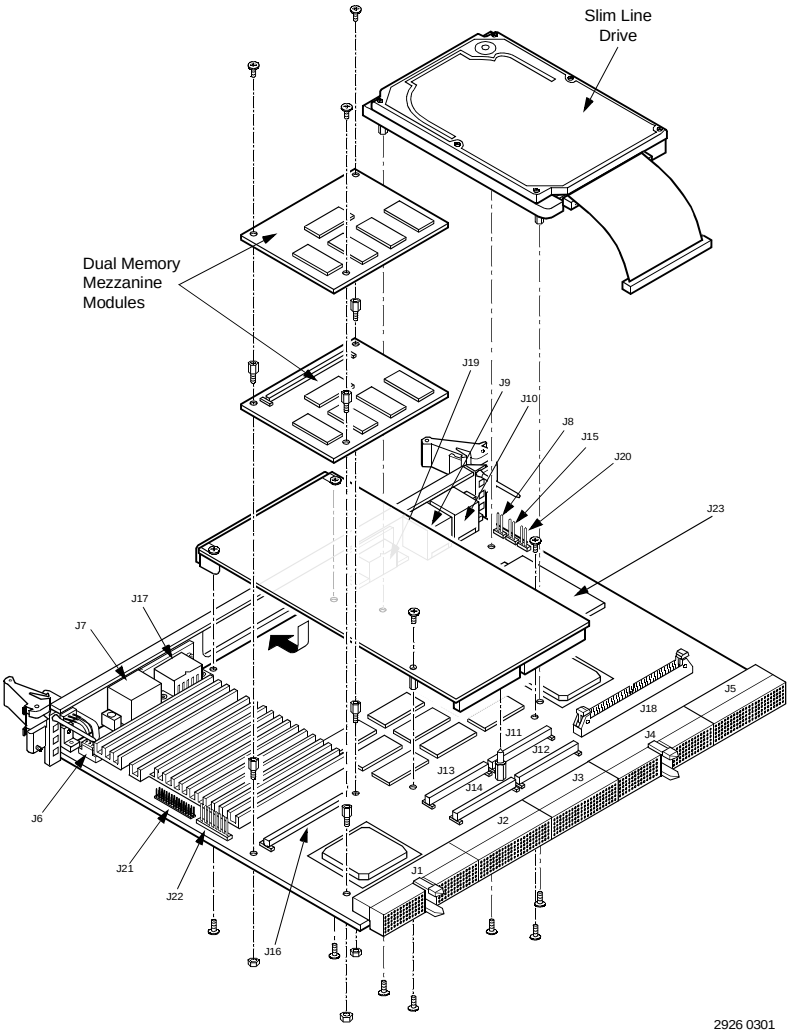


Figure 1-2. Location of CPV5370 On-Board Components and Connectors

Equipment Required

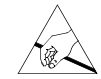
A CPV5370 system requires this equipment:

- CompactPCI system enclosure
- System console terminal
- Operating system
- Disk drives
- Transition Module (CPTM04) and connecting cables.

Unpacking Instructions

Note If the shipping carton is damaged upon receipt, request that the carrier's agent be present during the unpacking and inspection of the equipment.

Unpack the equipment from the shipping carton. Refer to the packing list and verify that all items are present. Save the packing material for storing and reshipping of equipment.



Caution Avoid touching areas of integrated circuitry. Static discharge can damage circuits.

Before Installing the CPV5370

After removing the CPV5370 from its packaging:

- Check for obvious physical damage
- Verify that the coin cell battery is in its holder and inserted correctly

Overview of Startup Procedures

The following table lists the things you need to do before you can use this board. It also tells you where to find the information you need to perform each step.

Table 1-3. Startup Overview

For information about:	Go to:
Hardware Configuration	*Hardware Configuration* on page 1-8
Connecting peripherals	*Connecting to Board Connectors* on page 1-8
Mounting memory mezzanine cards	*Mounting Memory Mezzanine Cards* on page 1-10
Mounting PCI Mezzanine Cards (PMC)	*Mounting PCI Mezzanine Cards* on page 1-10
Hard drive mounting	*Mounting the Slim Line EIDE Hard Drive* on page 1-11
Installing the CPV5370	*Before You Install or Remove a Board* on page 1-12
Installing the CPTM04	
Powering-up the system	*Applying Power to the System* on page 3-1

Hardware Configuration

To produce the necessary hardware configuration and to make sure the CPV5370 operates properly, you may need to make certain modifications by setting bits in control registers after installing the module in a system.

The CPV5370 control registers are described in Chapter 4, *Functional Description*.

Connecting to Board Connectors

The CPV5370 and CPTM04 give you board connectors for attaching peripheral devices. Before installing either module, you may want to connect your peripheral cables to the connectors. Refer to Chapter 6, *Connector Pin Assignments*.

Notes When the identical function is available through the CPV5370 front panel and CPTM04 rear panel, you can use either the front or the rear, **not both**.

Warning

Always remove power from the system before connecting peripherals to the boards. To reduce the risk of personal injury, disconnect the power cord from the power source. Only qualified, experienced electronics personnel should access the interior of a chassis.

Caution

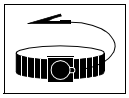
The components of the CPV5370 and CPTM04 are sensitive to static discharge. While out of the unit, place the modules on a static-dissipative surface or into a static-shielding bag.

Caution

Current revisions of the CPV5370 do not support PMC Interface Modules (PIMs) requiring +12.0V. Plugging a PIM that requires +12.0V into the CPTM04 with a CPV5370 could damage the PIM. Please see your PIM documentation for the voltage requirements of your module.

Antistatic Precautions

Use ESD



Wrist Strap

Motorola strongly recommends that you use an antistatic wrist strap and a conductive foam pad when installing or upgrading a system. Electronic components, such as disk drives, computer boards, and memory modules, can be extremely sensitive to electrostatic discharge (ESD). After removing the component from its protective wrapper or from the system, place the component flat on a grounded, static-free surface (and, in the case of a board, component side up). Do not slide the component over any surface.

If an ESD station is not available, you can avoid damage resulting from ESD by wearing an antistatic wrist strap (available at electronics stores) that is attached to an active electrical ground. Note that a system chassis may not be grounded if it is unplugged.



Warning

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.



Caution

Avoid touching areas of integrated circuitry. Static discharge can damage these circuits.

Mounting Memory Mezzanine Cards

You can mount one or two 256MB Memory Mezzanine Modules on the CPV5370. Refer to *Antistatic Precautions* on page 1-9 before beginning installation. Refer to Figure 1-2.

1. Attach three standoffs to the CPV5370 board and secure with three nuts on the secondary side of the board.
2. Place one Memory Mezzanine Module on top of the three standoffs and gently press onto the J16 connector on the CPV5370, working from the center of the connector to the outsides of the module. This will ensure a tight connection.
3. Secure with three screws.

   If mounting a second Memory Mezzanine Module use a second set of three standoffs instead of three screws.
4. Place the second Memory Mezzanine Module on top of the three standoffs and press onto the connector on the first Memory Mezzanine Module, again working from the center to the outsides of the module.
5. Secure with three screws.

Mounting PCI Mezzanine Cards

You can mount one 32 bit, +5.0V PCI Mezzanine Card (PMC) on the PMC site. The PMC expansion runs at 33 MHz. The I/O signals are routed to the rear transition module. Refer to *Antistatic Precautions* on page 1-9 before beginning installation. The PMC site is keyed for +5.0V PCI bus interface.

Note You cannot install PMCs that are only compatible with +3.3V PCI.

The PMC module I/O connects to J3.

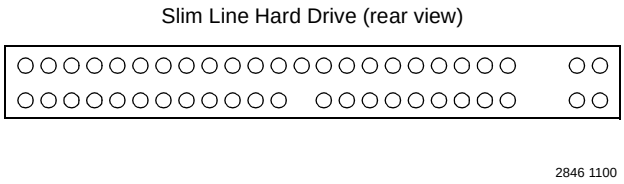
1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. Keep the ESD secured throughout this procedure.
2. Shut down the operating system.

Warning

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

Mounting the Slim Line EIDE Hard Drive

You can mount a Slim Line EIDE hard drive on the CPV5370. Refer to Figure 1-2. No configuration is required. The drive is configured as master with no jumpers installed.



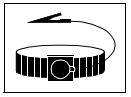
1. Connect the Slim Line EIDE drive cable to the J18 connector on the CPV5370.
2. Position the drive on the CPV5370.
3. Connect the drive cable to the drive.
4. Secure the drive to the CPV5370 using three screws.

Before You Install or Remove a Board

Boards may be damaged if improperly installed or handled. Please read and follow the guidelines in this section to protect your equipment.

Observe ESD Precautions

Use ESD



Wrist Strap

Motorola strongly recommends that you use an antistatic wrist strap and a conductive foam pad when installing or upgrading a system. Electronic components, such as disk drives, computer boards, and memory modules, can be extremely sensitive to electrostatic discharge (ESD). After removing the component from its protective wrapper or from the system, place the component flat on a grounded, static-free surface (and, in the case of a board, component side up). Do not slide the component over any surface.

If an ESD station is not available, you can avoid damage resulting from ESD by wearing an antistatic wrist strap (available at electronics stores) that is attached to an active electrical ground. Note that a system chassis may not be grounded if it is unplugged.

Watch for Bent Pins or Other Damage



Caution

Bent pins or loose components can cause damage to the board, the backplane, or other system components. Carefully inspect your board and the backplane for both pin and component integrity before installation

MCG and our suppliers take significant steps to ensure there are no bent pins on the backplane or connector damage to the boards prior to leaving our factory. Bent pins caused by improper installation or by boards with damaged connectors could void the MCG warranty for the backplane or boards.

If a system contains one or more crushed pins, power off the system and contact your local sales representative to schedule delivery of a replacement chassis assembly.

Use Caution When Installing or Removing Boards

When first installing boards in an empty chassis, we recommend that you start at the left of the card cage and work to the right when cards are vertically aligned; in horizontally aligned cages, work from bottom to top.

When inserting or removing a board in a slot adjacent to other boards, use extra caution to avoid damage to the pins and components located on the primary or secondary sides of the boards.

Preserve EMI Compliance



Caution

To preserve compliance with applicable standards and regulations for electromagnetic interference (EMI), during operation all front and rear openings on the chassis or board faceplates must be filled with an appropriate card or covered with a filler panel. If the EMI barrier is open, devices may cause or be susceptible to excessive interference.

Understand Hot Swap



Caution

Inserting or removing non-hot swap cards or transition modules with power applied may result in damage to module components. Make sure that your board manufacturer identifies your module as hot swap ready.

The PICMG 2.1 Hot Swap specification defines varying levels of hot swap. A board that is compliant with the specification can be inserted and removed safely with system power on without damage to on-board circuitry. *If a module is not hot swap compliant, you should remove power to the slot or system before inserting or removing the module.*

To facilitate hot swap, PICMG 2.1 specifies a blue LED on the faceplate. This LED is under software control.

If your system is using software that provides full hot swap capabilities, the software will illuminate the blue hot swap LED on the faceplate when software has stopped and it is safe to remove the board.

If your system does not have hot swap-aware software running, behavior of the blue LED may be indeterminate. In this case, you may need to manually shut down applications or operating systems running on the board prior to board removal, even if the blue LED is lit.

Caution

Powering down or removing a board before the operating system or other software running on the board has been properly shut down may cause corruption of data or file systems.

Refer to the documents listed in Appendix C, *Related Documentation* for more information about hot swap and the PCI Industrial Computer Manufacturers Group (PICMG) Hot Swap Specification.

Recognize Different Injector/Ejector Lever Types

The modules you install may have different ejector handles and latching mechanisms. The following illustration shows the typical board ejector handles used with MCG payload cards: (A) Elma Latching, (B) Rittal Type II, (C) Rittal Type IV. All handles are compliant with the CompactPCI specification and are designed to meet the IEEE1101.10 standards.

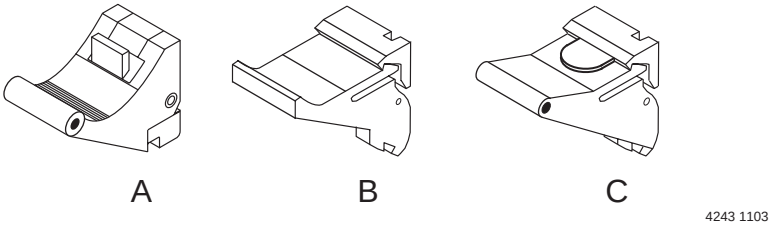


Figure 1-3. Injector/Ejector Lever Types

Each lever type has a latching mechanism to prevent the lever from being opened accidentally. You must press the lever release before you can open the lever. *Never force the lever*. If the lever does not open easily, you may not have pressed firmly enough on the release. If the lever does not close easily, the board may not be properly seated in the chassis.

To open a lever, press the release and move the lever outward away from the faceplate.

To close a lever, move the lever inward toward the faceplate until the latch engages.

Verify Slot Usage

Caution

Prevent possible damage to module components by verifying the proper slot usage for your configuration.

In most cases, connector keying will prevent insertion of a board into an incompatible slot. However, as an extra precaution, you should be familiar with the glyphs and colored card rails used to indicate slot purpose.

The following table lists the colors common to MCG chassis.

Table 1-4. Slot Usage Indicators

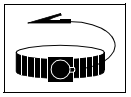
Card Rail Color	Glyph	Usage
Tan	None	**MXP:** Alarm Management Controller slot
		**CPX:** Hot Swap Controller or Bridge slot
Red		**MXP:** Fabric Switch Card slot
		**CPX:** System Controller slot
Black		**MXP:** Payload Card slot
		**CPX:** Non-system Controller or I/O Card slot

Installing a Module

This section describes a recommended procedure for installing a board module in a chassis.

Before you install your module, please read all cautions, warnings, and instructions presented in this section and the guidelines explained in *Before You Install or Remove a Board* on page 1-12.

Use ESD



Wrist Strap

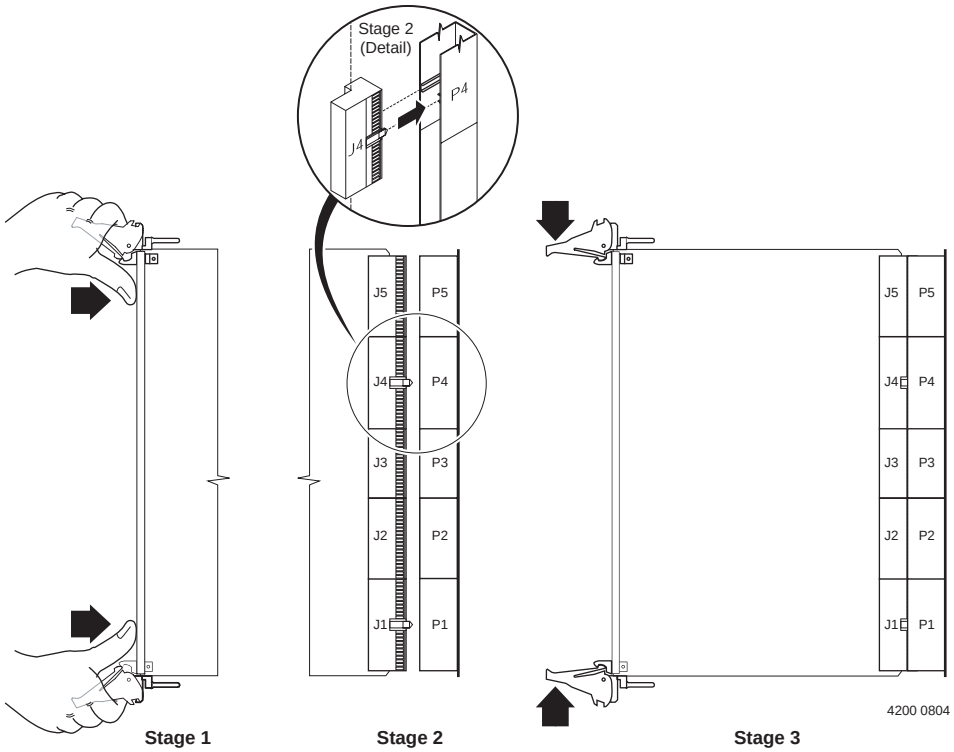
Handling modules and peripherals can result in static damage. Use a grounded wrist strap, static-dissipating work surface, and antistatic containers when handling and storing components.

Caution

Insert the board by holding the injector levers—do not exert unnecessary pressure on the faceplate.

Hot swap compliant modules may be installed while the system is powered on. If a module is not hot swap compliant, you should remove power to the slot or system before installing the module. See *Understand Hot Swap* on page 1-13 for more information.

Refer to the following illustration and perform these steps when installing modules. Note that this illustration is for general reference only and may not accurately depict the connectors and handles on the board you are installing.



1. Open the injector levers on your board (see *Recognize Different Injector/Ejector Lever Types* on page 1-14).
2. Verify the proper slot for the module you are inserting (see *Verify Slot Usage* on page 1-15). Align the edges of the module with the card cage rail guides in the appropriate slot.
3. Using your thumbs, apply equal and steady pressure as necessary to carefully slide the module into the card cage rail guides (Stage 1). Continue to gently push until the prealignment guide pegs engage with the backplane connector (Stage 2) and the injector levers make contact with the chassis rails. *DO NOT FORCE THE BOARD INTO THE BACKPLANE SLOT.*

4. Use the injector levers to seat the module in the slot by closing the levers until they latch into the locked position (Stage 3). If the levers do not completely latch, remove the module from the chassis and visually inspect the slot to ensure there are no bent pins.

5. When the module you are installing is completely latched, secure it by tightening the captive screws at both ends of the faceplate.

Removing a Hot-Swap Module

This section describes a recommended procedure for removing a board module from a chassis.

Before you remove your module, please read all cautions, warnings, and instructions presented in this section and the guidelines explained in *Before You Install or Remove a Board* on page 1-12.

Hot swap compliant modules may be removed while the system is powered on. If a module is not hot swap compliant, you should remove power to the slot or system before removing the module. See *Understand Hot Swap* on page 1-13 for more information.

To remove a board module, follow these steps:

1. Loosen the module's captive screws at both ends of the faceplate.

2. Begin to remove your module by unlatching the ejector lever closest to the blue LED (the lower lever on vertically mounted boards). See *Recognize Different Injector/Ejector Lever Types* on page 1-14. *Do not remove the module immediately.*



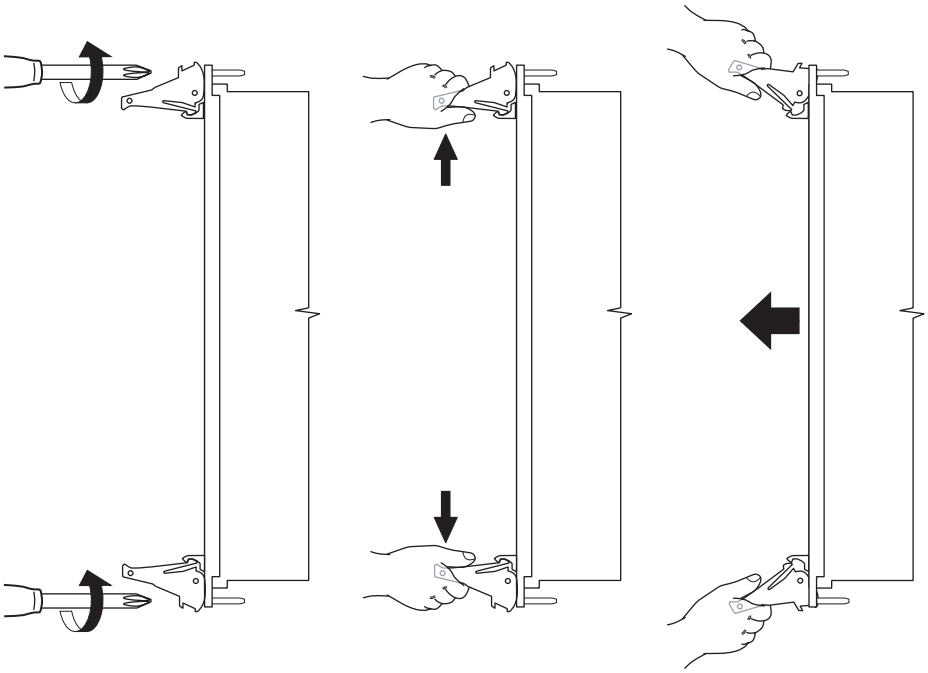
Caution

Powering down or removing a board before the operating system or other software running on the board has been properly shut down may cause corruption of data or file systems.

If your module is hot swap compliant and you are running fully functional hot swap-aware software, unlatching this ejector lever will start the shutdown process on the board. Software will illuminate the blue hot swap LED on the faceplate when it is safe to remove the board.

If your board or system is not running hot swap-aware software, the blue LED may illuminate without regard to software processes still running on the board. Be sure to manually shut down applications or operating systems running on the board prior to board removal. See *Understand Hot Swap* on page 1-13 for more information.

3. Once the applications and operating system running on the board have stopped and it is safe to remove the board, open both ejector levers to partially unseat the module from the backplane connectors.



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4. Carefully pull the module from the chassis.

Replacing Lithium Batteries

Follow these safety rules for proper battery operation and to reduce equipment and personal injury hazards when handling lithium batteries. Use the battery for its intended application only.

Note **Do not** recharge, open, puncture or crush, incinerate, expose to high temperatures or dispose of in your general trash collection.

To replace the lithium battery, observe the following guidelines and follow the steps below.

Note When replacing the battery, you must apply power to the board to prevent data loss.

To prevent serious injury or death from dangerous voltages, use extreme caution when handling, testing, and adjusting this equipment and its components.



Warning

Lithium batteries incorporate flammable materials such as lithium and organic solvents. If lithium batteries are short-circuited or exposed to high temperature or pressure, they may burst open and ignite, possibly resulting in injury and/or fire. When dealing with lithium batteries, carefully follow the precautions listed below to prevent accidents.

- ❏ Do not short-circuit
- ❏ Do not disassemble, deform or apply excessive pressure
- ❏ Do not heat or incinerate
- ❏ Do not apply solder directly
- ❏ Do not use different models, or new and old batteries together
- ❏ Do not charge
- ❏ Always check proper polarity

To replace the on-board backup battery, follow the steps below.



Caution

Danger of explosion if battery is replaced incorrectly.

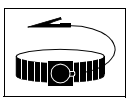
Replace only with the same or equivalent type recommended by the equipment manufacturer. Dispose of used batteries according to the manufacturer's instructions.



Caution

Avoid touching areas of integrated circuitry; static discharge can damage circuits.

Use ESD



Wrist Strap

Attach an ESD strap to your wrist. Attach the other end of the ESD strap to an electrical ground. (Note that the system chassis may not be grounded if it is unplugged.) Secure the ESD strap to your wrist and to ground throughout the procedure.

1. To remove the battery from the module, carefully pull the battery from the socket.
2. Before installing a new battery, make sure that the battery pins are clean.
3. Note the battery polarity and press the new battery into the socket.

Note No soldering is required when the battery is in the socket.

4. Recycle or dispose of the old battery according to local regulations and manufacturer's instructions.

CPTM04 Installation 2

This chapter discusses how to prepare and install the CPTM-01 rear transition module. Pin assignments are located at the end of this chapter.

Preparation

This section outlines hardware configuration and installation considerations.

Hardware Configuration

There are no on-card jumpers or switches.

Connecting to Peripheral Devices

The CPTM04 Transition Module has board connectors for attaching peripheral devices. Before installing this module, you may want to connect your peripheral cables to the connectors. Refer to Chapter 6, *Connector Pin Assignments* for pin assignment information.

Note When the identical function is available through the CPV5370 (front panel) or the CPTM-01 (rear panel), you can use either the front or the rear, not both.

Features

The CPTM04 Transition Module gives you these features:

- Rear panel connections for:
  - PS/2 keyboard/mouse
  - Video

  - COM2 (serial port 2)
  - Ethernet 1 and 2
  - PIM 1

- On-board connectors for:
  - PS/2 keyboard/mouse
  - Floppy
  - USB0 and USB1
  - Secondary IDE
  - COM1 (serial port 1)
  - Parallel port

Input/Output Interfaces

Refer to *Input/Output Interfaces* on page 1-3 for brief descriptions of the input/output interfaces on CPTM04.



Caution

When the identical function is available through the CPV5370's front panel and the rear transition module, you can use either the front or the rear, **not both**.

On-Board and Rear Panel Components on the CPTM04

Table 2-1 lists the connectors available to support devices on the CPTM04 Rear Transition Module.

Table 2-1. Connectors, and Components on the CPTM04

Connector	Description
J1	IPMI System Management Bus Connector
J3	Rear I/O CompactPCI Connector
J4	Rear I/O CompactPCI Connector
J5	Rear I/O CompactPCI Connector
J10	PIM (64-pin PMC I/O connector - power)
J14	PIM (64-pin PMC I/O connector - signals)
J15	USB (8-pin connector)
J16	CompactFlash (master/slave jumper)
J17	Power On LED, EIDE Activity LED, Push button reset (12-pin header)
J18	Ethernet 2 connector
J19	Ethernet 1 connector
J20	Video (15-pin high density D-sub)
J21	Floppy connector (34-pin connector)
J22	COM2 (serial port 2 - 9-pin D-sub)
J23	COM1 (serial port 1 - 10-pin shrouded)
J24	Keyboard/Mouse connector (external, 6-pin PS/2 female)
J25	Parallel connector (26-pin shrouded)
J26	Secondary EIDE (40-pin shrouded)
J27	CompactFlash (50-pin)

The following figure shows the location of on-board components and rear panel connectors on the CPTM04.

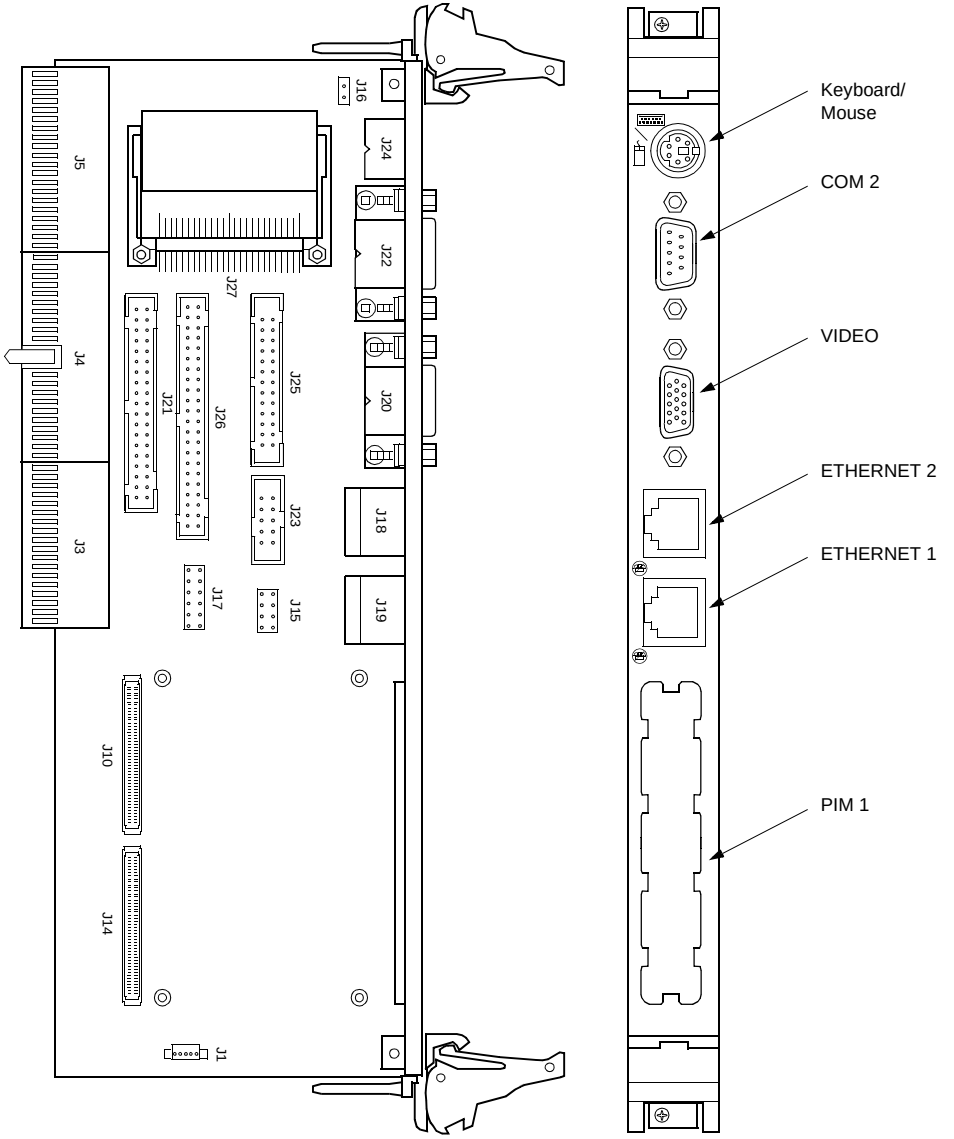


Figure 2-1. component and Connector Layout of the CPTM04

Installing the CPTM04

The CPTM04 transition module may be required to complete the configuration of your particular CPV5370 system. If so, perform the following steps to install this board.

Please read all cautions, warnings and procedures before installing the CPTM04 into your chassis.

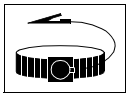


Caution

Inserting or removing modules in a non-hot swap chassis with the power applied may result in damage to the module components. The CPTM04 is not a hot swap board, but may be installed in a hot swap chassis with power applied only if the corresponding CPV5370 is removed before the transition module is installed.

ESD

Use ESD



Wrist Strap

Motorola strongly recommends that you use an antistatic wrist strap and a conductive foam pad when installing or upgrading a system. Electronic components, such as disk drives, computer boards, and memory modules, can be extremely sensitive to ElectroStatic Discharge (ESD).

After removing the component from the system or its protective wrapper, place the component flat on a grounded, static-free surface (and in the case of a board, component side up). Do not slide the component over any surface.

If an ESD station is not available, you can avoid damage resulting from ESD by wearing an antistatic wrist strap (available at electronics stores) that is attached to an unpainted metal part of the system chassis.

Warning



Warning

Avoid touching areas of integrated circuitry; static discharge can damage these circuits.

Warning



Warning

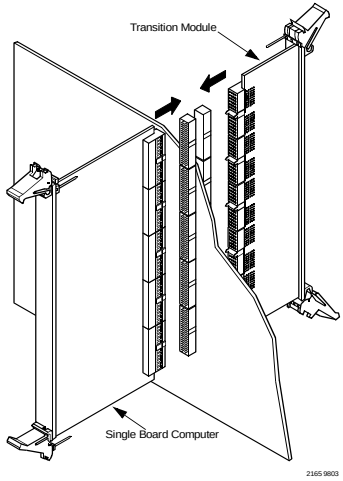
Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

Before installing the transition module, you should install the CompactFlash memory card.

To install a rear transition module in the chassis, follow these steps:

1. Attach an ESD strap to your wrist. Attach the other end of the strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Perform an operating system shutdown if you are **not** removing the CPV5370. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. If you are **not** powering off the system, first remove the CPV5370 before installing the RTM.
3. Remove chassis or system cover(s) as necessary for access to the chassis backplane.
4. With the transition module in the correct vertical position that matches the pin positioning of the corresponding CPV5370 board, carefully slide the transition module into the appropriate slot and

seat tightly into the backplane. Refer to the next figure for the correct connector orientation.



5. Secure in place with the screws provided, making good contact with the transverse mounting rails to minimize RF emissions.
6. Replace the chassis or system cover(s), making sure no cables are pinched.
7. Cable the peripherals to the panel connectors, reconnect the system to the AC or DC power source, and turn the equipment power on.
8. Replace the chassis or system cover(s), reconnect the system to the AC or DC power source, and turn the equipment power on, or if hot swapping, you may now install the CPV5370.

2

Pin Assignments for the CPTM04

The following tables describe the pin assignments and signal descriptions for the rear I/O and other connectors on the CPTM04 Rear Transition Module.

Rear I/O Connectors (J3 and J5)

The following tables provide the pin assignments and signal descriptions for the rear I/O connectors on the CPTM04.)

Table 2-2. CPTM04 Rear I/O Connector Pin Assignments (J3)

Pin #	F	E	D	C	B	A
19	GND	V_DDCCLK	V_DDCDAT	V_BLU	V_GRN	V_RED
18	GND	GND	V_VSYNC	V_HSYNC	GND	HS_REQ
17	GND	LANB RD-	LANB TD-	LANB TD+	GND	HS_GNT
16	GND	LANB RD+	LANA RD-	LANA RD+	GND	HS_FLT
15	GND	VCC-12	LANA TD-	LANA TD+	GND	HS_EJ
14	GND	VCC5	VCC5	VCC3.3	VCC3.3	VCC3.3
13	GND	PMC1	PMC2	PMC3	PMC4	PMC5
12	GND	PMC6	PMC7	PMC8	PMC9	PMC10
11	GND	PMC11	PMC12	PMC13	PMC14	PMC15
10	GND	PMC16	PMC17	PMC18	PMC19	PMC20
9	GND	PMC21	PMC22	PMC23	PMC24	PMC25
8	GND	PMC26	PMC27	PMC28	PMC29	PMC30
7	GND	PMC31	PMC32	PMC33	PMC34	PMC35
6	GND	PMC36	PMC37	PMC38	PMC39	PMC40
5	GND	PMC41	PMC42	PMC43	PMC44	PMC45
4	GND	PMC46	PMC47	PMC48	PMC49	PMC50
3	GND	PMC51	PMC52	PMC53	PMC54	PMC55
2	GND	PMC56	PMC57	PMC58	PMC59	PMC60
1	GND	PMC61	PMC62	PMC63	PMC64	VCC3.3

Table 2-3. Signal Descriptions for I/O Connector J3

Signal	Signal Mnemonic	Signal Description
Ethernet (1 and 2)	LANn_RD+, LANn_RD-	Differential receive lines
	LANn_TD+, LANn_TD-	Differential transmit lines
Video Signal Definitions	V_RED	Red signal
	V_GRN	Green signal
	V_BLU	Blue signal
	V_HSYNC	Horizontal synchronization
	V_VSYNC	Vertical synchronization
	V_DDCCLK	Display Data Channel, clock signal for DDC2 support
	V_DDCDAT	Display Data Channel, data signal for DDC2 support
General	GND	Ground
	+5V	+5 Volts dc power
	+3.3V	+3.3 Volts dc power
	N/C	Not connected
	-12V	- 12 Volts dc power
PMC I/O	PMCIO [1 to 64]	PMC channel 1 I/O signals 1 through 64
High Availability Hot Swap	HS_REQ	Hot Swap Request
	HS_GNT	How Swap Grant
	HS_FLT	Hot Swap Float
	HS_EJ	Hot Swap Eject

Table 2-4. CPTM04 Rear I/O Connector (J5)

Pin #	F	E	D	C	B	A
22	N/C	SPKR	+5V	N/C	GND	PBRESET
21	GND	MCLK	MDAT	+5V	KBDCLK	KBDDAT
20	N/C	SMBALRT	GND	SMBCLK	SMBDAT	+5V
19	GND	USB0-	USB0+	+5V	GND	STB-
18	N/C	+5V	GND	USB1-	USB1+	AFD-
17	GND	PD0	ERR-	PD1	INIT-	PD2
16	N/C	SLIN-	PD3	PD4	PD5	PD6
15	GND	PD7	ACK-	BUSY	PE	SLCT
14	N/C	DTR1	GND	RI1	CTS1	RTS1
13	GND	TXD1	DSR1	RXD1	+5V	DCD1
12	N/C	DTR2	+5V	RI2	CTS2	RTS2
11	GND	TXD2	DSR2	RXD2	GND	DCD2
10	N/C	DSKCHG-	HDSEL-	RDATA-	WPROT-	TR0-
9	GND	WGATE-	WDATA-	STEP-	DIR-	MTR1-
8	N/C	DS0-	DS1-	MTR0-	INDEX-	DRVDENS1-
7	GND	DRVDENS0-	+12.0V	DA1	CS3-	CS1-
6	N/C	DA2	DA0	ATA66-	GND	RSRVD N/C
5	GND	DIOR-	DMACK-	DIOW-	IORDY	DMRQ
4	N/C	IRQ	DD15	GND	DD0	DD14
3	GND	DD1	DD13	DD2	DD12	DD3
2	N/C	DD11	DD4	DD10	DD5	DD9
1	GND	DD6	DD8	DD7	IDERST-	GND

Table 2-5. CPTM04 Ethernet Connector Pin Assignments (J18, J19)

Pin #	Signal Mnemonic	Signal Description
1	TX+	Differential transmit lines
2	TX-	Differential transmit lines
3	RX+	Differential receive lines
4	-	-
5	-	-
6	RX-	Differential receive lines
7	-	-
8	-	-

Table 2-6. CPTM04 COM1 Serial Port Connector Pin Assignments (J23)

Pin #	Signal Mnemonic	Signal Description	Pin #	Signal Mnemonic	Signal Description
1	DCD	Data set has detected the data carrier	2	DSR	Data set is ready to establish a communications link
3	RX	Receives serial data input from communication link	4	RTS	UART is ready to exchange data
5	TX	Sends serial data to communication link	6	CTS	Data set is ready to exchange data
7	DTR	Data set is ready to establish a communication link	8	RI	Modem has received a telephone ringing signal
8	GND	Ground	10	GND	Ground

Table 2-7. CPTM04 COM2 Serial Port Connector Pin Assignments (J28)

Pin #	Single Mnemonic	Signal Description
1	DCD	Data set has detected the data carrier
2	RX	Receives serial data input from communication link
3	TX	Sends serial output to communication link
4	DTR	Indicates that a data terminal is ready to establish a communication link
5	GND	Ground
6	DSR	Indicates that a data set is ready to establish a communication link
7	RTS	Indicates to data set that UART is ready to exchange data
8	CTS	Indicates that a data set is ready to exchange data
9	RI	Indicates that a modem has received a telephone ringing signal

Table 2-8. CPTM04 Video Connector Pin Assignments (J20)

Pin #	**Signal Mnemonic**	**Signal Description**
1	RED	Red signal
2	GREEN	Green signal
3	BLUE	Blue signal
4	NC	no connection
5	DACVSS	Video return
6	DACVSS	Video return
7	DACVSS	Video return
8	DACVSS	Video return
9	NC	no connection
10	DACVSS	Video return
11	NC	no connection
12	DDCDAT	Display Data Channel data signal for DDC2 support
13	HSYNC	Horizontal synchronization
14	VSYNC	Vertical synchronization
15	DDCCLK	Display Data Channel clock signal for DDC2 support

Table 2-9. CPTM04 Keyboard/Mouse P/S2 Pin Assignments (J24)

Pin #	Signal Mnemonic	Signal Description
1	KBDDAT	Data line for keyboard
2	MDAT (AUXDAT) [1]	Data line for mouse
3	GND	Keyboard Ground
4	KBDVCC	Keyboard Power
5	KBDCLK	Clock for keyboard
6	MCLK (AUXCLK) [2]	Clock for mouse
7	CGND	Common Ground

[1] AUXDAT is Data line for mouse for the CPTM04

[2] AUXCLK is Clock for mouse for the CPTM04

Table 2-10. CPTM04 Keyboard/Mouse/Power LED Pin Assignments

Pin #	Signal Mnemonic	Signal Description	Pin #	Signal Mnemonic	Signal Description
1	PWRLED	Power LED Indicator	2	KBDCLK	Clock for keyboard
3	GND	Ground	4	KBDDAT	Data line for keyboard
5	GND	Ground	6	AUXDAT	Data line for mouse
7	-	-	8	GND	Ground
9	GND	Ground	10	KBDVCC	Keyboard power
11	-	-	12	AUXCLK	Clock for mouse

Table 2-11. CPTM04 USB Connector Pin Assignments (J15)

Pin #	Signal Mnemonic	Signal Description	Pin #	Signal Mnemonic	Signal Description
1	+5V	+5V dc power (current limited to 1.0A)	2	+5V	+5V dc power (current limited to 1.0A)
3	DATA1-	USB serial communication differential pair	4	DATA0-	USB serial communication differential pair
5	DATA1+	USB serial communication differential pair	6	DATA0+	USB serial communication differential pair
7	GND	USB port common	8	GND	USB port common

Table 2-12. CPTM04 Parallel Connector Pin Assignments (J25)

Pin #	Signal Mnemonic	Signal Description	Pin #	Signal Mnemonic	Signal Description
1	STROBE-	Indicates data at parallel port is valid	2	AFD-	Causes printer to add a line feed
3	D0	Parallel data lines	4	ERR-	Set low when an error is detected
5	D1	Parallel data lines	6	INIT-	Initializes the printer
7	D2	Parallel data lines	8	SLIN-	Selects the printer
9	D3	Parallel data lines	10	GND	Ground
11	D4	Parallel data lines	12	GND	Ground
13	D5	Parallel data lines	14	GND	Ground
15	D6	Parallel data lines	16	GND	Ground
17	D7	Parallel data lines	18	GND	Ground

Table 2-12. CPTM04 Parallel Connector Pin Assignments (J25) (Continued)

Pin #	Signal Mnemonic	Signal Description	Pin #	Signal Mnemonic	Signal Description
19	ACK-	Input is pulsed by the peripheral to acknowledge data retrieval	20	GND	Ground
21	BUSY	Printer cannot accept any more data	22	GND	Ground
23	PE	Printer is out of paper	24	GND	Ground
25	SELECT	Set high when selected	26	-	-

Table 2-13. CPTM04 EIDE Connector Pin Assignments (J26)

Pin #	Signal Mnemonic	Signal Description	Pin #	Signal Mnemonic	Signal Description
1	RESET-	Reset signal to drive	2	GND	Ground
3	DD7	Drive data line	4	DD8	Drive data line
5	DD6	Drive data line	6	DD9	Drive data line
7	DD5	Drive data line	8	DD10	Drive data line
9	DD4	Drive data line	10	DD11	Drive data line
11	DD3	Drive data line	12	DD12	Drive data line
13	DD2	Drive data line	14	DD13	Drive data line
15	DD1	Drive data line	16	DD14	Drive data line
17	DD0	Drive data line	18	DD15	Drive data line
19	GND	Drive data line	20	-	-
21	DMARQ	Drive DMA request	22	GND	Ground
23	IOW-	Drive I/O write	24	GND	Ground
25	IOR-	Drive I/O read	26	GND	Ground
27	IORDY	Drive is ready for I/O cycle(s)	28	CSEL-	Cable select
29	DMACK-	Drive DMA acknowledge	30	GND	Ground
31	INTRQ	Drive interrupt request	32	IOCS16-	Indicates a 16 bit register is decoded

Table 2-13. CPTM04 EIDE Connector Pin Assignments (J26) (Continued)

Pin #	Signal Mnemonic	Signal Description	Pin #	Signal Mnemonic	Signal Description
33	DA1	Drive register and data port address line	34	PDIAG-	Output from drive 1 and monitored by drive 0
35	DA0	Drive register and data port address line	36	DA2	Drive register and data port address line
37	CS1-	Chip select drive 0, also command register block select	38	CS3-	Chip select drive 1, also command register block select
39	DASP-	Drive active/slave present	40	GND	Ground

Table 2-14. CPTM04 CompactFlash Connector Pin Assignments (J27)

Pin #	Signal Mnemonic	Signal Description	Pin #	Signal Mnemonic	Signal Description
1	GND	Ground	26	-	-
2	DD3	Drive data line	27	DD11	Drive data line
3	DD4	Drive data line	28	DD12	Drive data line
4	DD5	Drive data line	29	DD13	Drive data line
5	DD6	Drive data line	30	DD14	Drive data line
6	DD7	Drive data line	31	DD15	Drive data line
7	CS1-	Chip select drive 0, also command register block select	32	CS3-	Chip select drive 1, also command register block select
8	GND	Ground	33	-	-
9	GND	Ground	34	IOR-	Drive I/O read
10	GND	Ground	35	IOW-	Drive I/O write
11	GND	Ground	36	VCC	+5 Volts
12	GND	Ground	37	INTRQ	Drive interrupt request
13	VCC	+5 Volts	38	VCC	+5 Volts
14	GND	Ground	39	CSE:L-DD3	Cable select
15	GND	Ground	40	-	-
16	GND	Ground	41	RESET-	Reset signal to drive

Table 2-14. CPTM04 CompactFlash Connector Pin Assignments (J27)

Pin #	Signal Mnemonic	Signal Description	Pin #	Signal Mnemonic	Signal Description
17	GND	Ground	42	IORDY	Drive is ready for I/O cycle(s)
18	DA2	Drive register and data port address lines	43	-	-
19	DA1	Drive register and data port address lines	44	VCC	+5 Volts
20	DA0	Drive register and data port address lines	45	DASP-	Drive active/slave present
21	DD0	Drive data line	46	PDIAG-	Output from drive 1 and monitored by drive 0
22	DD1	Drive data line	47	DD8	Drive data line
23	DD2	Drive data line	48	DD9	Drive data line
24	-	-	49	DD10	Drive data line
25	-	-	50	GND	Ground

Table 2-15. CPTM04 Floppy Connector Pin Assignments (J21)

Pin #	Signal Mnemonic	Signal Description	Pin #	Signal Mnemonic	Signal Description
1	GND	Ground	2	DRVDENS0	Disk density select communication
3	GND	Ground	4	N/C	not connected
5	GND	Ground	6	DRVDENS1	Disk density select communication
7	GND	Ground	8	INDEX-	Indicates the beginning of a track
9	GND	Ground	10	MTR0-	Motor enable outputs
11	GND	Ground	12	DS1-	Drive select 1
13	GND	Ground	14	DS0-	Drive select 0
15	GND	Ground	16	MTR1-	Motor enable outputs

Table 2-15. CPTM04 Floppy Connector Pin Assignments (J21) (Continued)

Pin #	Signal Mnemonic	Signal Description	Pin #	Signal Mnemonic	Signal Description
17	GND	Ground	18	DIR-	Controls the direction of the FDD head during seek operations
19	GND	Ground	20	STEP-	Supplies step pulses to move head during seek operations
21	GND	Ground	22	WDATA-	Writes serial data to disk drive
23	GND	Ground	24	WGATE-	Enables head of disk drive to write to disk
25	GND	Ground	26	TR0-	Indicates that head of FDD is at track 0
27	GND	Ground	28	WPROT-	Indicates a disk is write protected
29	GND	Ground	30	RDATA-	Raw read data from disk drive
31	GND	Ground	32	HDSEL-	Determines side of the floppy disk being accessed
33	GND	Ground	34	DSKCHG-	Notifies the disk drive controller that the drive door is open

Table 2-16. CPTM04 Indicator LED/Miscellaneous Pin Assignments (J2)

Pin #	Signal Mnemonic	Signal Description	Pin #	Signal Mnemonic	Signal Description
1	IDE_LED	EIDE primary channel activity LED. Connect LED between pins 5 and 6	2	+5V	+5VDC power
3	PWR_LED	Power ON indicator.	4	GND	Ground
5	PBRESET	Push button system reset. Connect switch between pins 5 and 6	6	GND	Ground
7	N/C	not connected	8	N/C	not connected
9	SPKR	Speaker	10	+5V	+5VDC power

Table 2-17. CPTM04 PMI SMB Connector Pin Assignments (J1)

Pin #	Signal Mnemonic	Signal Description
1	SMBCLK	System Management Bus Clock
2	GND	Ground
3	SMBDAT	System Management Bus Data
4	+5V	+5V dc power
5	N/C	not connected

Table 2-18. CPTM04 CompactFlash Master/Slave Connector (J16) [1]

Pin #	Signal	Pin #	Signal
1	GND	2	M_S_JMP

[1] Jumper installed defines CompactFlash as master device on EIDE primary channel

Starting Up the CPV5370 3

This chapter provides information on the power-up procedure and the CPV5370 switches and indicator LEDs.

Note This document treats the CPV5370 as a component of a system, and assumes that it is being installed in a CompactPCI backplane that is PICMG compliant.

Applying Power to the System

Before applying power to the system verify that:

- All necessary hardware preparation is complete
- All connections are correct
- The voltage setting for the chassis power supply matches the voltage present in the country of use (if the power supply in your system is not auto-sensing).

When power is applied, the CPV5370 displays the PhoenixBIOS banner and then runs a memory test.

Switches and Indicators

A push button reset switch is located on the front panel of the CPV5370. The switch is not programmable.

There are two LED indicators on the CPV5370 front panel:

- Left - Power (green)/Alarm (red)
- Right - Hard Disk Drive (green) indicates hard drive activity on the primary IDE channel

Functional Description

4

This chapter provides a functional description of all major components and devices on the CPV5370 Single Board Computer. Refer to the following figure for a block diagram of the CPV5370.

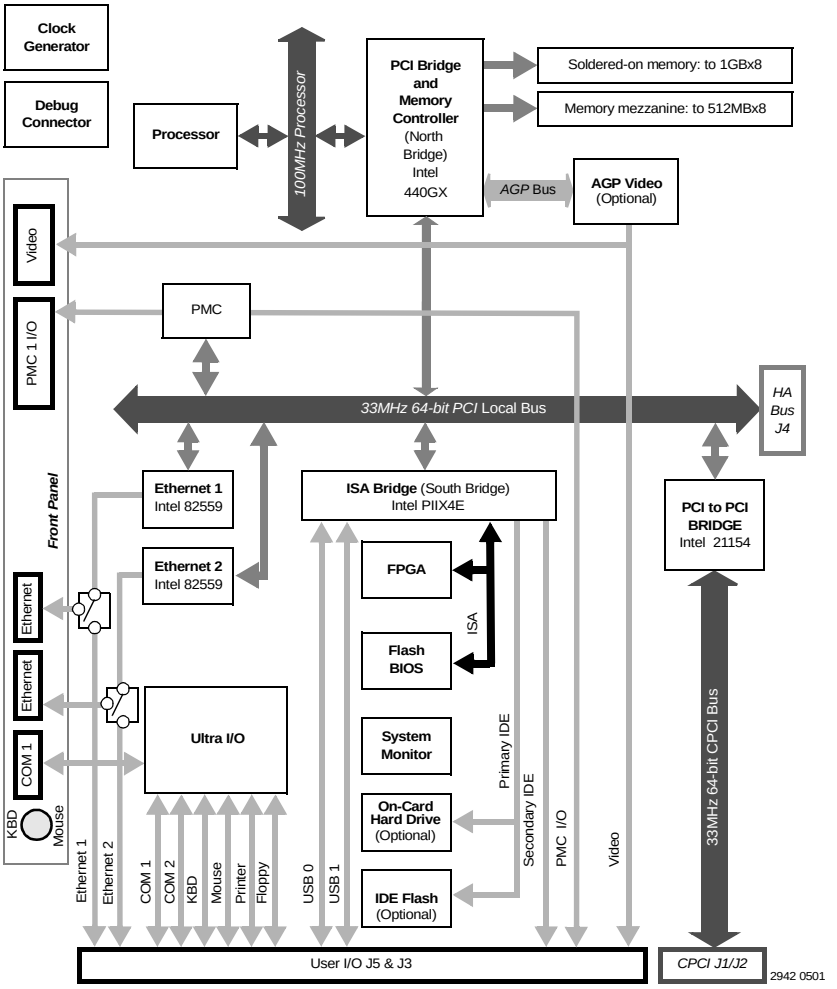


Figure 4-1. CPV5370 Block Diagram

Processor

The CPV5370 supports a single Intel Pentium III BGA2 processor. The Pentium III is a 32-bit super scalar processor. The maximum external processor bus speed is 100 MHz. The internal core frequency is 700 MHz or 1 GHz. The Pentium III embedded processor is packaged in a BGA2 ball grid array package, while the PIIX4E south bridge includes the L2 cache and tag RAM.

New capabilities added to the Pentium III processor (over previous Intel processors) are: streaming SIMD instructions for faster 3D multimedia applications, and processor serial number for security and system configuration management.

Cache

The Pentium III has an internal L1 cache. The L1 data and instruction caches are separate and 16KB each. The L1 caches are 4-way set associative and support write-back or write-through modes. The data cache uses the MESI protocol while the code cache uses the SI subset of the MESI protocol. The L2 cache included on the processor die is a unified, direct mapped cache that is available in 256KB, and supports caching of up to the 4GB boundary of system memory space.

440GX Chipset

The CPV5370 uses the Intel 440GX chipset for bridging capabilities. The 440GX consists of the 82443GX North Bridge, and the 82371EB PIIX4E South Bridge. The north bridge serves as a DRAM controller and AGP bridge, as well as a bridge to the PCI bus. The PIIX4E includes support for legacy ISA peripherals.

82443GX North Bridge

The 82443GX is a 492-pin BGA. It provides the processor interface to the system DRAM memory and the AGP bus. It also provides the local PCI bus interface.

Memory

Memory is implemented in four rows of on-board SDRAM that allows configurations up to 1GB. Memory devices used are unbuffered, +3.3V, SDRAM. Onboard memory operates at 100 MHz. Memory is auto-sized at power-on of the CPV5370 by the system BIOS.

Up to 1GB of memory can be soldered onto the board, and another 512MB of memory can be added by installing mezzanine memory modules.

Memory soldered on to the CPV5370 is implemented with one or two rows of 32MBx8 devices or 64MBx8 devices. The board layout has 18 SDRAM positions, which support the installation of either nine or 18 standard devices for either 256MB, 512MB or 1GB. These choices are a build option. A memory mezzanine connector allows the installation of either one or two 256MB or 512MB memory mezzanine modules. Each mezzanine module provides one row of (9) 32MBx8 or 64MBx8 SDRAM devices.

The memory mezzanine connector is a 140-pin AMP 0.6mm free height receptacle.

Frame AGP Interface

A single Advanced Graphics Port (AGP) device is supported by the 440GX through the use of a dedicated AGP bus. The interface is capable of AGP bandwidths of up to 1GB per second.

The Intel 69030 chip set is used for on-board 2D and 3D accelerated video. The 69030 contains 4MB of built-in video RAM and provides high performance on-card video including hardware 3D rendering, hardware 3D texturing, and Advanced Graphics Port interface. A video connection is available on the front panel, as well as the rear I/O via a transition module.

PCI Interface

The 440GX provides arbitration and bus control for the local PCI bus. The 64-bit peer-to-peer transactions are supported; however, the processor to the PCI interface is limited to 32-bits. On-card peripherals connect directly

to this bus. Off-card access is supported through the Intel 21154 PCI-to-PCI Bridge. The PCI interface has a measured read and write bandwidth of a least 120MB per second.

PIIX4E South Bridge

The 82371EB PIIX4E South Bridge is a 324-pin BGA. It provides the Xbus (ISA) interface, legacy peripheral support, USB, IDE, and real time clock.

Universal Serial Bus

The PIIX4E supports two USB ports. Additional ports can be added through the use of an external USB hub. USB allows for the easy addition of peripherals such as a mouse, keyboard, speaker, joystick, etc. Transfer rates of 1.5 Mb/s and 12 Mb/s are supported. High-speed connections (12Mb/s) require shielded cable. The 1.5 Mb/s transfer rate may require shielded cable for EMI compliance. The CPV5370 provides the standard 0.5A at +5V power to the peripherals connected to its USB ports. The power is protected by 1.10A polyswitches to allow for inrush currents.

Both USB ports are available on the rear I/O transition module.

Ultra 33 EIDE

The IDE interface of the PIIX4E supports two channels (up to four devices) of industry standard EIDE. The secondary channel is available via the rear I/O connector. The primary channel is used for on-card peripherals, such as the CompactFlash disk and hard drive, and does not exit the card.

The IDE interface supports ATAPI modes 0 to 4 and Ultra 33 synchronous DMA mode (33MB per second). Each IDE channel supports two IDE devices (master and slave). The IDE interface supports disk drives up to 8.2GB and CD-ROM drives.

An on-card 2.5” hard drive can be mounted and connected to the primary EIDE interface.

Real-Time Clock and Non-volatile Memory

The PIIX4E has a DS1287 compatible battery backed up real time clock. It provides a century calendar, as well as time of day function. In addition, 256 bytes of battery backed up RAM are available for use by the BIOS.

The battery back up is provided by a separate 3V battery. The backup battery is socketed and has a series resistor and diode to conform to industry safety requirements. The battery is rated at 180 mA-Hrs, and has an expected shelf life of five years.

Peripheral Component Interconnect (PCI) Local Bus Interface

The PCI local bus is a high-performance, 32-bit bus with multiplexed address and data lines. Use it as an interconnect mechanism between highly-integrated peripheral controller components, peripheral add-in boards, and processor/memory systems.

The CPV5370 supports a 32-bit local PCI bus interface. On-board devices connect directly to the local PCI bus.

CompactPCI Bus Interface

The CPV5370 supports a single 64-bit CompactPCI bus interface (2.1 compliant) through an Intel 21154 PCI-to-PCI bridge. You can insert the physical connector into a 64-bit high availability CompactPCI backplane and make connection to off-card CompactPCI peripherals through the PCI-to-PCI bridge. The interface is also available to a high availability companion card through the J4 connector.

IDE Flash

The CPV5370 supports IDE compatible flash memory. This memory is implemented using removable CompactFlash memory cards. Once configured, the memory appears as a standard ATA (IDE) disk drive. There is a limit to the number of times that a write can be performed on CompactFlash memory, so it should not be used in a paging environment.

Ethernet Interface

The CPV5370 provides dual Ethernet transceiver support via two Intel 82559 devices. The Ethernet interfaces are routed to either the front panel or the rear transition module, and the connection can be controlled by user through a question in the system BIOS setup menu.

Every board is assigned two Ethernet Addresses, one for each controller. The address is 08003E2XXXXXh where XXXXX is the unique number assigned to each controller. The Ethernet addresses are clearly displayed on the board by a label. The Ethernet address is stored in a 93C46A CMOS SEEPROM.

PMC Expansion

The CPV5370 provides one 64-bit PMC site for user expansion. The PMC expansion runs at 33 MHz. The PMC I/O signals are routed to the rear transition module through the J3 connector. One PMC device can be installed onto the CPV5370. The PMC site is keyed for +5.0V PCI.

Value Add FPGA

The CPV5370 provides one value-add FPGA to support a two-level watchdog function. The Atmel AT17C128 SEEPROM is used to store the FPGA configuration.

Super I/O Device

The CPV5370 Ultra I/O provides two asynchronous serial ports, a parallel port, a floppy interface, a PS/2 keyboard interface, and a PS/2 mouse interface. Each of these features is described in the following subsections.

Asynchronous Serial Ports

Two serial ports are supported on the CPV5370. The EIA232 drivers and receivers reside on board. Both ports are configured as DTE.

Firmware initializes the two serial ports as COM1 and COM2 with I/O base addresses of 3F8h and 2F8h respectively. This default configuration also assigns COM1 to IRQ4 and COM2 to IRQ3. The user can change the default configuration via options in the BIOS setup utility. The serial ports are ESD protected to 15kV.

The connector for COM1 is available on the front panel as well as through the rear of the board via a transition module. COM2 is only available through the rear transition module.

Printer Interface

The parallel port on the CPV5370 supports the full IEEE-1284 capability. The port provides standard, ECP and EPP modes of operation.

Firmware initializes the parallel port as LPT1 with I/O base address of 378h. This default also assigns the parallel port interrupt to IRQ7 of the PIC. The user can change the default via options in the BIOS setup utility.

The parallel port connector is available on the rear transition module only.

Floppy Interface

The floppy port is configured for PS/2 compatibility. The interface signals are routed to the rear I/O and are accessible either via a special header on the backplane, or via a rear transition module.

The floppy interface supports up to two floppy drives. Both 5 1/4” and 3 1/2” drives are supported.

Keyboard/Mouse Interface

The CPV5370 provides a standard PS/2 style keyboard and mouse interface via a circular mini din connector on the front panel. A PS/2 keyboard may be connected directly to the front panel. A mouse may be connected using a splitter cable. The keyboard and mouse connections are also routed to the rear I/O and are available via a transition module.

The power provided to the keyboard and mouse is protected by a polyswitch rated at 1.1A.

Special Functions

The CPV5370 uses these functions designed for certain applications. Refer to Chapter 5, *Memory Maps and Programming Information* for programmer’s reference information.

Watchdog Timer

You can program the watchdog timer via registers in the ISA I/O memory map. The watchdog timer is protected from being accidentally enabled. The timer supports a range of count down time-outs up to eight minutes.

The watchdog timer can operate in these modes:

- Disabled
- Sets the timeout flag in the Watchdog Strobe/Status port in ISA I/O memory map
- Sets the timeout flag in the Watchdog Strobe/Status port in ISA I/O memory map + Assert a selectable interrupt (ISA IRQ)
- Sets the timeout flag in the Watchdog Strobe/Status port in ISA I/O memory map + Assert NMI followed by a system Reset or Soft Reset

Advanced System Monitoring

The CPV5370 monitors the following system events:

- On-card temperature
- BGA2 thermal fault
- On-card voltages +5V, +3.3V, +12V, and the processor core voltages
- System Management Bus (SMBUS) alert signal
- Chassis power supply loss of regulation

Power Management

The CPV5370 supports the following power down modes: Pentium III deep sleep, Green PC standby and suspend, Video standby and suspend, and IDE standby and suspend. Processor Speed Step is supported through the PIIX4 interface.

PCI Arbitration

PCI arbitration is performed by the North bridge and the PCI-to-PCI bridge. This arbitration maintains fairness and prevents bus lockouts. The arbitration also is completely transparent to any software running on the system. Refer to *Memory Maps and Programming Information* for PCI arbitration assignment information.

PhoenixBIOS Description

The CPV5370 BIOS is similar to the CPV5350 BIOS. Refer to Chapter C, *Related Documentation* for information about how to access the *CPV5350 CompactPCI BIOS and Programmer's Reference Guide*. Refer to *Jump to User Code in Alternate Flash Bank* on page 5-25.

The CPV5370 uses the PhoenixBIOS to provide initial hardware configuration for local devices and local operating system boot. The BIOS supports Intel Speed-Step for the CPU.

The on-board BIOS is stored in a 4Mx8 Flash ROM. The Flash ROM is reprogrammable in the system for BIOS updates. The PROM is accessible through a 512K byte window. The standard BIOS resides in the default 512k window. The PROM banks are selected through the FPGA register (refer to the FPGA description for more detail). The board has a catastrophic flash recovery process in case a portion of the BIOS becomes corrupted. Unused banks may be usable for other features such as RTOS boot images. An Intel 28F320J5 StrataFlash memory device is used to store the BIOS.

Soft Reset

You can generate a “soft reset” from your keyboard and the watchdog timer. The BIOS preserves as much of the system memory state as possible.

A CPV5370 circuit monitors system power and provides the PWROK signal to the 82371EB PIIX4E South Bridge. The PIIX4E South Bridge distributes the reset to the rest of the board by generating the CPU, PCI, and IDE resets. You can also reset the board using the front panel reset switch and the FPGA watchdog timer. You can program the Watchdog Timer to generate a soft reset. Refer to *Field Programmable Gate Array Registers* on page 5-9 for programming information.

Headless Operation

The BIOS can operate with no keyboard or display. You do, however, need a keyboard and display to change setup options unless you use the remote setup feature.

Remote Setup

You can change setup options remotely through the BIOS Setup - Advanced Menu using a COM port. The default settings for a terminal are:

- 19200 baud (bps)
- 1 stop bit
- No parity
- No flow control

Network Boot

The Intel PXE (Pre-boot Execution Environment) 82559 BIOS extension module is included to provide operating system boot via one of the 82559 ports. This module is built into the BIOS. You can enable the PXE for either port through the BIOS Setup-Advanced-PCI Configuration Menu.

Memory Maps and Programming Information

5

Memory Address Mapping

Refer to the following table for memory address information.

Table 5-1. Memory Addresses and Descriptions

Address	Size	Description
0xFFF80000 - 0xFFFFFFFF	512KB	High BIOS Area
0xFEE01000 - 0xFFF7FFFF	17.5MB	Available for PCI
0xFEE00000 - 0xFEE00FFF	4KB	Local APIC Configuration Space
0xFEC10000 - 0xFEDFFFF	1.94MB	Available for PCI
0xFEC00000 - 0xFEC0FFFF	64KB	I/O APIC Configuration Space
0x00100000 - 0xFEDFFFFF	3.98GB	Available for PCI when not used for system memory
0x000F0000 - 0x000FFFFF	64KB	System BIOS Area
0x000E0000 - 0x000EFFFF	64KB	Extended BIOS Area
0x000C0000 - 0x000DFFFF	128KB	Expansion ROM Area
0x000A0000 - 0x000BFFFF	128KB	Video Buffer Area
0x00000000 - 0x0009FFFF	640KB	DOS Applications/Compatibility Region

I/O Address Map

Table 5-2 shows I/O addressing. You can use BIOS Setup or special utilities to enable or relocate these features from their default values.

Table 5-2. I/O Addresses and Descriptions

Address (hex)	Size	Description
0000 - 000F	16 bytes	PIIX4E DMA, channels 0 - 3
0020 - 0021	2 bytes	PIIX4E Interrupt Controller 1
0040 - 0043	4 bytes	PIIX4E - Timer 1
005B	2 bytes	FPGA Watchdog Strobe/Status Register
005D	2 bytes	FPGA Index Register
005F	2 bytes	FPGA Data Register
0060	1 byte	Keyboard Controller
0061	1 byte	PIIX4E - NMI, Speaker Control
0064	1 byte	Keyboard Controller
0070 - 7	1 bit	PIIX4E NMI Enable
0070-6:0	7 bits	PIIX4E RTC
0071	1 byte	PIIX4E RTC
0072-0073	2 bytes	PIIX4E RTC (extended registers)
0080 - 008F	16 bytes	PIIX4E DMA Page Register
0092	1 byte	PIIX4E Port 92 Register
00A0 - 00A1	2 bytes	PIIX4E Interrupt Controller 2
00B2 - 00B3	2 bytes	APM reserved
00C0 - 00DE	31 bytes	PIIX4E DMA, channels 4 - 7
00EA	1 byte	Ultra I/O General Purpose I/O Index Register
00EB	1 byte	Ultra I/O General Purpose I/O Data Register
00F0	1 byte	Reset Numeric Error
0170 - 0177	8 bytes	Secondary IDE Channel
01F0 - 01F7	8 bytes	Primary IDE Channel
02F8 - 02FF	8 bytes	COM2
0376	1 byte	Secondary IDE Channel Command Port

Table 5-2. I/O Addresses and Descriptions (Continued)

Address (hex)	Size	Description
0377	1 byte	Secondary IDE Channel Status Port
0378 - 037F	8 bytes	LPT1
03F0 - 03F5	6 bytes	Floppy
03F6	1 byte	Primary IDE Channel Command Port
03F7-7	1 bit	Floppy Disk Change Channel 1
03F7-6:0	7 bits	Primary IDE Channel Status Port
03F7 (write)	1 byte	Floppy Channel 1 Command
03F8 - 03FF	8 bytes	COM 1
04D0 - 04D1	2 bytes	Interrupt Controller Edge/Level Register
0CF8 - 0CFB	4 bytes	PCI CONFADD (DWORD Access Only)
0CFC - 0CFF	4 bytes	PCI CONFDATA
0CF9	1 byte	PIIX4E Reset Control Register
FF00 - FF07	8 bytes	IDE Bus Master Register
FFA0 - FFA7	8 bytes	Primary Bus Master IDE Registers
FFA8 - FFAF	8 bytes	Secondary Bus Master IDE Registers
FF80 - FF9F	32 bytes	USB

PCI Configuration Bus Mapping

The following table shows PCI configuration mapping of all the devices on the CPV5370.

Table 5-3. PCI Configuration Bus Map

PCI Bus Number	Device Number Field	PCI Address Line	Function Number	IDSEL Connection
0	0	AD11	0	440GX North Bridge, Memory, and PCI Interface
0	1	AD12	0	440GX AGP Bridge
0	8	AD19	0	Ethernet A
0	9	AD20	0	Ethernet B
0	7	AD18	0	PCI to LPC Bridge
0	7	AD18	1	IDE Controller
0	7	AD18	2	USB Controller
0	7	AD18	3	Power Management Controller
0	6	AD22	0	Hot Plug Controller (Motorola HA Board)
0	13	AD24	0	Bridge (Motorola HA Board)
0	10	AD21	0	Bridge to CompactPCI
0	16	AD27	0	PMC Site
1	1	NA	0	Video Controller
2	9	AD25	X	CompactPCI Slot8
2	10	AD26	X	CompactPCI Slot7
2	11	AD27	X	CompactPCI Slot6
2	12	AD28	X	CompactPCI Slot5
2	13	AD29	X	CompactPCI Slot4
2	14	AD30	X	CompactPCI Slot3
2	15	AD31	X	CompactPCI Slot2

Interrupt Routing

The following subsections show how interrupts are routed on the CPV5370.

ISA (Legacy) Interrupts

The following table shows the assignments of the ISA (Legacy) hardware interrupts.

Table 5-4. ISA (Legacy) Interrupts

IRQ	Edge/ Level	Polarity	Interrupt Source
IRQ0	Edge	High	Interval Timer
IRQ1	Edge	High	Keyboard
IRQ2	Edge	High	Cascade interrupt for PIC2
IRQ3	Edge	High	Asynchronous Serial Port 2 (COM2)
IRQ4	Edge	High	Asynchronous Serial Port 1 (COM1)
IRQ5	Level	Low	Available for PCI/PnP
IRQ6	Edge	High	Floppy Disk Controller
IRQ7	Edge	High	Parallel Port (LPT1)
IRQ8	Edge	Low	Real Time Clock
IRQ9	Edge	High	System Control Interrupt (SCI)
IRQ10	Level	Low	Available for PCI/PnP
IRQ11	Level	Low	Available for PCI/PnP
IRQ12	Edge	High	PS/2 Mouse
IRQ13	Edge	High	Reserved for Floating Point Error
IRQ14	Edge	High	Primary IDE Controller
IRQ15	Edge	High	Secondary IDE Controller

PCI Interrupt Routing

The following table shows how the interrupt pins on each PCI device are routed to the PCI interrupts on the PIIX4E.

Table 5-5. PCI Interrupt Routing

Device	INTA	INTB	INTC	INTD
Power Management (PIIX4E)	PIRQA	-	-	-
Ethernet Controller A	PIRQA	-	-	-
Ethernet Controller B	PIRQC	-	-	-
Video Controller	PIRQD	-	-	-
USB Controller	PIRQD	-	-	-
PMC Card	PIRQA	PIRQB	PIRQC	PIRQD
CompactPCI Slot 8	PIRQB	PIRQC	PIRQD	PIRQA
CompactPCI Slot 7	PIRQC	PIRQD	PIRQA	PIRQB
CompactPCI Slot 6	PIRQD	PIRQA	PIRQB	PIRQC
CompactPCI Slot 5	PIRQA	PIRQB	PIRQC	PIRQD
CompactPCI Slot 4	PIRQB	PIRQC	PIRQD	PIRQA
CompactPCI Slot 3	PIRQC	PIRQD	PIRQA	PIRQB
CompactPCI Slot 2	PIRQD	PIRQA	PIRQB	PIRQC

SMBUS (System Management Bus)

The SMBUS controller is located within the PIIX4E chip. In addition to the PIIX4, there are several devices that reside on the SMBUS on the CPV5370. The following table lists the addresses of all of the devices on the SMBUS.

Table 5-6. SMBUS Resident Slave Devices/Addresses

Device	Address
MAX1617 CPU Thermal Monitor	1001 110b
PI6C180 SDRAM Clock Buffer	1101 001b
I82371EB PIIX4E South Bridge Chip	0000 001b
On-board Memory Serial Presence Detect (AT24C08-2.7) - Row 0/Row 1	1010 100b
Mezzanine Memory Serial Presence Detect - Row 2/Row 3	N/A[1]
GD82559 Ethernet B	0000 011b
GD82559 Ethernet A	0000 100b
J5 User I/O Connector	N/A[1]
LM81 System Monitor Chip	0101 101b

Note [1]These addresses are determined by the devices that are plugged into the CPV5370.

PCI Arbitration

PCI arbitration is performed by the North Bridge and the Intel 21154 PCI-to-PCI bridge. This arbitration maintains fairness and prevents bus lockouts. The arbitration also is completely transparent to any software running on the system.

Since the CPV5370 has two PCI bus segments, the request/grant assignments for each segment are shown in the following two tables.

Table 5-7. PCI Arbitration Assignments (On-Board Segment)

PCI Bus Request	PCI Master
REQ0	PMC Site
REQ1	Ethernet B
REQ2	Ethernet A
REQ3	21154 PCI-to-PCI Bridge
REQ4	J4 connector (for HA systems)

Table 5-8. PCI Arbitration Assignments (CompactPCI Segment)

PCI Bus Request	PCI Master
REQ0	CPCI Slot 2
REQ1	CPCI Slot 3
REQ2	CPCI Slot 4
REQ3	CPCI Slot 5
REQ4	CPCI Slot 6
REQ5	CPCI Slot 7
REQ6	CPCI Slot 8

Field Programmable Gate Array Registers

The Field Programmable Gate Array (FPGA) is used for add-on features and control, and connects to the internal ISA bus. It consists of a group of I/O registers for control of features such as a Watchdog Timer, I/O switching control, and system management functions.

When a system management event occurs, the input causing the event latches and remains latched until cleared by the system software. The system management hardware notifies the system of the event depending on the mode selected by the user.

Table 5-9. System Management Modes

Mode:	Behavior:
IRQ Mode	ISA interrupt generates - You can set the interrupt by writing to the IRQ select register.
SCI Mode	SCI generates - The FPGA's SCI output connects to the PIIX4 Therm input GPI8.
NMI Mode	NMI generates
ALARM Mode	ALARM generates

FPGA Register Descriptions

This section describes how to access the various FPGA register sets. The bit description tables below show bits 0 through 7 on the top line and bit functions on the second line.

You can access the FPGA registers by an index register at offset 05h from the base address of the FPGA (0x5Dh). The data register is located at offset 07h (0x5Fh). Refer to Table 5-10. To access an FPGA register, write to the

index register first and then read/write from the data register. The BIOS sets the default FPGA Base address to 58h.

Table 5-10. Index and Data Register Address and Function

Port	Offset Address	Function
Index	05h	Register Index Port - selects the device register
Data	07h	Data Port - read/write data to selected register
Watchdog Strobe/Status	03h	Watchdog Strobe and Status register

The following table shows a map of the FPGA register set.

Table 5-11. Map of the FPGA Register Set

Device 00h System	Device 10h LAN A Ctrl	Device 11h LAN B Ctrl	Device 14h Flash Ctrl
00 Status			
	01 LAN A	01 LAN B	01 FLASH
03 Watchdog			
04 INT Sel			
05 SCI Mask			
06 NMI Mask			
07 IRQ Mask			
08 Alm Mask			
09 FLT Latch			
0B Power On			
0F DEV SEL	0F DEV SEL	0F DEV SEL	0F DEV SEL

Status Register

The Status Register (STAT) is a read only register. Reads of the unused bits produce indeterminate values. Writes have no effect. The Temp Alarm, SMB Alert, Alarm B, and Alarm A are all latched when active. You must initiate a write to the LEN register to clear the latched signals.

Table 5-12. Bit Descriptions for the STAT Register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
ALARM	FAL-	DEG-	ENUM-	LM81 ALARM A (NMI)	LM81 ALARM B (SMI)	SMB ALERT	CPU TEMP ALARM

CPU TEMP ALARM (Bit 0)

This signal connects to the CPU thermal monitor chip alert (MAX1617) output. The input is latched when active and cleared via the LEN register. A read of this bit returns the latched status of the input.

SMB ALERT (Bit 1)

This bit reflects the level of the SMBus Alert signal.

LM81 ALARM A (Bit 3) and LM81 ALARM B (Bit 2)

The LM81 output functions feed these signals. The input is latched when active and cleared via the LEN register. A read of these bits returns the latched status of the input.

ENUM (Bit 4)

ENUM comes from the CPCI bus and signals the insertion of a new device. The input is latched when active (low) and cleared via the LEN register. A read of this bit returns the latched status of the input.

DEG (Bit 5)

DEG comes from the CPCI bus and signals a power supply deregulation condition. A read of this bit returns the current state of the input.

FAL (Bit 6)

This signal comes from the CPCI bus and signals a power failure condition. A read of this bit returns the current state of the input.

ALARM (Bit 7)

This signal comes from Device 0 Index Register 08h Alarm Enable.

Watchdog Timer Register

Refer to the next table for Watchdog Timer Register (WDCFG) bit descriptions.

Table 5-13. Bit Descriptions for the Watchdog Timer Register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
CLR_STATUS	ALARM_EN	SOFT RST	WD1	WD0	SEL2	SEL1	SEL0

SEL0 (Bit 0), SEL1 (Bit 1) and SEL2 (Bit 2)

Use SEL0, SEL1 and SEL2 to select the watchdog timeout time. Writing to these bits does not clear or reset the watchdog timer.

Table 5-14. Bit Values for Selecting Watchdog Timeout Time

Period	SEL2	SEL1	SEL0
.46 seconds	0	0	0
.93 seconds	0	0	1
3.73seconds	0	1	0
14.91seconds	0	1	1
29.82 seconds	1	0	0
1.98 minutes	1	0	1
3.97 minutes	1	1	0
7.95 minutes	1	1	1

WD0 (Bit 3) and WD1 (Bit 4)

Use these bits to define the event that occurs on a watchdog timeout and to disable the watchdog timer. Reading these bits returns the last value written.

Table 5-15. Bit Values Defining Watchdog Timeout and Disabling

WD1	WD0	Description
0	0	DISABLED - Resets watchdog
0	1	POLLED
1	0	FPGA IRQX
1	1	NMI followed by reset or soft reset (7.28ms delay before SBC Reset)

SOFTRST (Bit 5)

Use this bit to change the Watchdog Reset function to Soft reset. This bit clears on power-up reset.

Table 5-16. SOFT_RST Bit 5 Settings

Set bit to:	For:
0 (default)	hard reset
1	soft reset

ALARM_EN (Bit 6)

This bit controls whether an FPGA alarm generates on a watchdog timeout event.

- Write a logic 1 to cause an alarm signal to become active on a watchdog timeout event
- Write a logic 0 to cause the alarm signal not to become active on a watchdog timeout event
- Read this bit to return the last written value

CLR_STATUS (Bit 7)

Use this bit to reset the watchdog timer output latch.

- Write a logic 1 to hold the watchdog timer output latch in a reset state
- Write a logic 0 to permit a watchdog timer event to be latched

Reading this bit returns the last written value.

Interrupt Selection Register

Use the Interrupt Selection Register (INTUM) to select the desired IRQ line. This IRQ can then be generated by a watchdog Timeout or ENUM-.

Table 5-17. Bit Descriptions for the INTUM Register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
RES	RES	RES	RES	IRQSL3	IRQSL2	IRQSL1	IRQSL0

IRQSL0 (Bit 0), IRQSL1 (Bit 1), IRQSL2 (Bit 2) and IRQSL3 (Bit 3)

These bits determine which IRQ is driven when an IRQ event triggers.

Table 5-18. Bit Values for Determining Driven IRQ Lines

Interrupt Line	IRQSEL3	IRQSEL2	IRQSEL1	IRQSEL0
No IRQ Selected	0	0	0	0
No IRQ Selected	0	0	0	1
No IRQ Selected	0	0	1	0
No IRQ Selected	0	0	1	1
No IRQ Selected	0	1	0	0
Select IRQ5	0	1	0	1
No IRQ Selected	0	1	1	0
Select IRQ7	0	1	1	1
No IRQ Selected	1	0	0	0
Select IRQ9	1	0	0	1
Select IRQ10	1	0	1	0
Select IRQ11	1	0	1	1
No IRQ Selected	1	1	0	0
No IRQ Selected	1	1	0	1
No IRQ Selected	1	1	1	0
No IRQ Selected	1	1	1	1

SCI Enable Register

The SCI Enable Register (SCIEN) defines the type of events that can generate an SCI.

Table 5-19. Bit Descriptions for the SCIEN Register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
ENABLE	RES	RES	ENUM-	ALARM_A-	ALARM_B-	TEMP-	SMB-

SMB (Bit 0)

- Set to a logic 1 to allow generation of an SCI when SMB Alert is active. SMB ALERT is active when logic 0
- Write a logic 0 to this bit to disable an SCI for this event

TEMP (Bit 1)

- Set to a logic 1 to allow generation of an SCI when TEMP is active
- Write a logic 0 to this bit to disable an SCI for this event

ALARM_A (Bit 3) and ALARM_B (Bit 2)

- Set to a logic 1 to allow the generation of an SCI when the ALARM_A or ALARM_B go active
- Write a logic 0 to these bits to disable an SCI for this event

ENUM (Bit 4)

- Set to a logic 1 to allow generation of an SCI when the ENUM event occurs.
- Write a logic 0 to this bit to disable an SCI for this event

ENABLE (Bit 7)

- Set to a logic 1 to allow generation of an SCI by one of the events above

- Write a logic 0 to prevent the events from generating an SCI

NMI Enable Register

The NMI Enable Register (NMIEN) defines the events that can generate an NMI.

Table 5-20. Bit Descriptions for the NMIEN Register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
ENABLE	RES	RES	ENUM	ALARM_A	ALARM_B	TEMP	SMB

SMB_ALERT (Bit 0)

- Set to a logic 1 to allow the generation of an NMI when the SMB Alert is active
- Write a logic 0 to this bit to disable an NMI for this event

TEMP (Bit 1)

- Set to a logic 1 to allow the generation of an NMI when TEMP is active
- Write a logic 0 to this bit to disable an NMI for this event

ALARM_A (Bit 3) and ALARM_B (Bit 2)

- Set to a logic 1 to allow the generation of an NMI when the ALARM_A or ALARM_B go active
- Write a logic 0 to this bit to disable an NMI for this event

ENUM (Bit 4)

- Set to a logic 1 to allow the generation of an NMI when the ENUM event occurs
- Write a logic 0 to this bit to disable an NMI for this event

ENABLE (Bit 7)

- Set to a logic 1 to allow the listed events to generate an NMI
- Write a logic 0 to prevent the events from generating an NMI

IRQ Enable Register

The IRQ Enable Register (IRQEN) defines the events that can generate an IRQ. The IRQ generated is set by IRQ Select Register (IRQNUM).

Table 5-21. Bit Descriptions for the IRQEN Register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
ENABLE	RES	RES	ENUM	ALARM_A	ALARM_B	TEMP	SMB

SMB (Bit 0)

- Set to a logic 1 to allow the generation of an IRQ when the SMB Alert is active
- Write a logic 0 to this bit to disable an IRQ for this event

TEMP (Bit 1)

- Set to a logic 1 to allow the generation of an IRQ when TEMP is active
- Write a logic 0 to this bit to disable an IRQ for this event

ALARM_A (Bit 3) and ALARM_B (Bit 2)

- Set to a logic 1 to allow the generation of an IRQ when the ALARM_A or ALARM_B go active
- Write a logic 0 to this bit to disable an IRQ for this event

ENUM (Bit 4)

- Set to a logic 1 to allow the generation of an IRQ when the ENUM event occurs

- Write a logic 0 to this bit to disable an IRQ for this event

ENABLE (Bit 7)

- Set to a logic 1 to allow the listed events to generate an IRQ
- Write a logic 0 to prevent the events from generating an IRQ

Alarm Enable Register

The Alarm Enable Register (ALEN) defines the events that generate an alarm output.

Table 5-22. Bit Descriptions for the ALEN Register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
ENABLE	RES	RES	ENUM	ALARM_A	ALARM_B	TEMP	SMB

SMB (Bit 0)

- Set to a logic 1 to allow the generation of an Alarm when the SMB Alert is active
- Write a logic 0 to this bit to disable an Alarm for this event

TEMP (Bit 1)

- Set to a logic 1 to allow the generation of an Alarm when TEMP is active
- Write a logic 0 to this bit to disable an Alarm for this event

ALARM_A (Bit 3) and ALARM_B (Bit 2)

- Set to a logic 1 to allow the generation of an Alarm when the ALARM_A or ALARM_B go active
- Write a logic 0 to this bit to disable an Alarm for this event

ENUM (Bit 4)

- Set to a logic 1 to allow the generation of an Alarm when the ENUM event occurs
- Write a logic 0 to this bit to disable an Alarm for this event

ENABLE (Bit 7)

- Set to a logic 1 to allow the listed events to generate an Alarm
- Write a logic 0 to prevent the events from generating an Alarm

Latch Enable Register

The Latch Enable Register (LEN) resets latches in the FPGA for the FAN, TEMP, ALARM_B, ALARM_B and ENUM alarms. This register is write only. Write a logic 1 to clear the latch for that bit position. Writing a logic 0 has no effect on the latch.

Table 5-23. Bit Descriptions for the LEN Register

7 (most significant bit)	6	5	4	3	2	1	0
RES	RES	RES	ENUM	ALARM_A	ALARM_B	TEMP	SMB_ALERT

SMB_ALERT (Bit 0) - SMB Alert Signal

This bit is set automatically when a SMB_ALERT event is signaled by an SM bus device.

- Write a logic 1 to clear the SMB_ALERT input latch
- Writing a logic 0 has no effect

TEMP (Bit 1) - CPU Temperature Signal

This bit is set automatically when a TEMP event is signaled by an off-card thermostat device.

- Write a logic 1 to clear the TEMP input latch

- Writing a logic 0 has no effect

ALARM_B (Bit 2) - LM81 Alarm B Signal

This bit is set automatically when an ALARM_B event is signaled by the on-card LM81.

- Write a logic 1 to clear any latched ALARM_B events
- Writing a logic 0 has no effect

ALARM_A (Bit 3) - LM81 Alarm A Signal

This bit is set automatically when an ALARM_A event is signaled by the on-card LM81

- Write a logic 1 to clear any latched ALARM_A events
- Writing a logic 0 has no effect

ENUM (Bit 4) - Bus Enumeration Signal

This bit is set automatically when an ENUM event occurs.

- Write a logic 1 to clear any ENUM latched events
- Writing a logic 0 has no effect

Power-On Status Register

The Power-On Status Register (POS) checks for power-on condition. You can also read back written bits.

Table 5-24. Bit Descriptions for the Power-On Status Register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
PBSOFT	RES	RES	RES	FLAG1	FLAG0	PWRON1	

PWRON0 (Bit 0) and PWRON1 (Bit 1)

The BIOS uses this bit to determine if it is booting from a power-up condition. It clears at power-on only. The BIOS may set it (write a 1) to flag subsequent resets.

FLAG0 (Bit 2) and FLAG1 (Bit 3)

Applications use these bits to flag boot states to the BIOS on the next reset. These bits clear at power-on and are not affected by reset. Software may set these bits by writing 1s to them.

PBSOFT (Bit 7)

Use this bit to program the function of the reset pushbutton switch. By default the front panel pushbutton switch causes a hard reset. Set this bit to a 1 to cause a soft reset. Clear the bit to 0 to program the switch to cause a hard reset. The default state is 0.

LAN A Control Register

Use the LAN A Control Register (LNACTRL) to control the on-card LAN A controller. Bits written can also read back.

Table 5-25. Bit Descriptions for the LAN A Register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
ENABLE	FRONT	RES	RES	RES	RES	RES	RES

FRONT (Bit 6)

The BIOS uses this bit to route LAN A signals to either the front or the rear connectors.

- Write a logic 0 to this bit to route LAN A signals to the front connector
- Write a logic 1 to this bit to route LAN A signals to the rear connector

The BIOS sets this bit according to CMOS setup.

ENABLE (Bit 7)

The BIOS uses this bit to enable LAN A.

- Write a logic 1 to this bit to disable LAN A
- Write a logic 0 to enable LAN A so that the operating system and application code can use it

The BIOS sets this bit according to CMOS setup.

LAN B Control Register

Use the LAN B Control Register (LNBCTRL) to control the on-card LAN B controller. Bits written can also read back.

Table 5-26. Bit Descriptions for the LAN B Register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
ENABLE	FRONT	RES	RES	RES	RES	RES	RES

LAN B ENABLE (Bit 7)

The BIOS uses this bit to enable LAN B.

- Write a logic 1 to this bit to disable LAN B
- Write a logic 0 to this bit to enable LAN B so the operating system and application code can use it

The BIOS sets this bit according to CMOS setup.

FRONT (Bit 6)

The BIOS uses this bit to route the LAN B signals to either the front or the rear connectors.

- Write a logic 1 to this bit to route LAN B signals to the rear connector
- Write a logic 0 to this bit to route LAN B signals to the front connector

The BIOS sets this bit according to CMOS setup.

Flash BIOS Control Register

Use the Flash BIOS Control Register (FLBCTRL) to control which bank on the BIOS flash memory part is to be accessed. Bits written can also read back.

Table 5-27. Bit Descriptions for the Flash BIOS Control Register

7 (most significant bit)	6	5	4	3	2	1	0 (least significant bit)
RES	RES	RES	RES	RES	BC2	BC1	BC0

BC0 (Bit 0), BC1 (Bit 1) and BC2 (Bit 2)

Use the Bank Control bits to control the Flash BIOS device. Reset selects Bank 0 as the default. The next table shows the Bank Control bit settings.

Table 5-28. Bit selections for the Flash BIOS Device Bank Control

512K BANK	Flash Offset	Window	BC2	BC1	BC0
Bank 0*	000000h	FFF80000h	0	0	0
Bank 1	080000h	FFF80000h	0	0	1
Bank 2	100000h	FFF80000h	0	1	0
Bank 3	180000h	FFF80000h	0	1	1
Bank 4	200000h	FFF80000h	1	0	0
Bank 5	280000h	FFF80000h	1	0	1
Bank 6	300000h	FFF80000h	1	1	0
Bank 7	380000h	FFF80000h	1	1	1
*Default Reset state					

Jump to User Code in Alternate Flash Bank

The flash device for the BIOS is a 4MB part consisting of eight 512K banks. The BIOS occupies Bank 0 only.

From the boot screen in the BIOS setup, you can select an alternate 512K flash bank to load and execute instead of booting from standard devices in the boot menu. If you select one of the alternate banks (banks 1 - 7), the BIOS looks for the five character signature "_MOT_" in the last five bytes of the selected 512K bank. If found, the BIOS disables interrupts, timers, and the watchdog. Then it reads the top 64K of the selected bank into segment 0F000h and jumps to 0F000:FFF0h. If the signature is not found, the BIOS proceeds normally and attempts to boot from standard floppy and hard drive devices.

Note When the bank switch and jump occurs, it happens very late in POST after all hardware is initialized.

Connector Pin Assignments

6

This chapter provides connector pin assignments and signal descriptions for the CPV5370 Single Board Computer. Pin assignments for the CPTM04 can be found in *CPTM04 Installation* on page 2-1.

CompactPCI Connector Pinouts (J1 and J2)

The CPV5370 provides a 64-bit CompactPCI interface on connectors J1 and J2.

- J1 is a 110-pin ERNI ERmet 2mm hard metric type A connector with keying for +3.3V or +5V
- J2 is a 110-pin ERNI ERmet 2mm hard metric type B connector

Each of these connectors conforms to the Hot Swap CompactPCI specification. The pin assignments for both connectors J1 and J2 are implemented as defined in the Hot Swap CompactPCI specification for a 64-bit system slot board. Note that no reserved or bussed pins are used by the CPV5370..

Table 6-1. CompactPCI Connector J1

Pin #	F	E	D	C	B	A	Z
25	GND	VCC	VCC3	ENUM#	REQ64#	VCC	GND
24	GND	ACK64#	AD[0]	VIO_LP	VCC	AD[1]	GND
23	GND	AD[2]	VCC_LP	AD[3]	AD[4]	VCC3	GND
22	GND	AD[5]	AD[6]	VCC3_LP	GND	AD[7]	GND
21	GND	C/BE[0]#	GND	AD[8]	AD[9]	VCC3	GND
20	GND	AD[10]	AD[11]	VIO	GND	AD[12]	GND
19	GND	AD[13]	GND	AD[14]	AD[15]	VCC3	GND
18	GND	C/BE[1]#	PAR	VCC3	GND	SERR#	GND
17	GND	PERR#	GND	RSV	RSV	VCC3	GND
16	GND	LOCK#	STOP#	VIO	GND	DEVSEL#	GND

Table 6-1. CompactPCI Connector J1

Pin #	F	E	D	C	B	A	Z
15	GND	TRDY#	BD_SEL#	IRDY#	FRAME#	VCC3	GND
KEY							
11	GND	C/BE[2#]	GND	AD[16]	AD[17]	AD[18]	GND
10	GND	AD[19]	AD[20]	VCC3_LP	GND	AD[21]	GND
9	GND	AD[22]	GND	AD[23]	IRSV	C/BE[3]#	GND
8	GND	AD[24]	AD[25]	VIO	GND	AD[26]	GND
7	GND	AD[27]	GND	AD[28]	AD[29]	AD[30]	GND
6	GND	AD[31]	CLK7	VCC3	GND	REQ7#	GND
5	GND	GNT7#	GND	RST#	BRSVP1B5	BRSVP1A5	GND
4	GND	INTS	INTP	VIO_LP	HLTY	BRSVP1A4	GND
3	GND	INTD#	VCC_LP	INTC#	INTB#	INTA#	GND
2	GND	RSV	RSV	RSV	VCC	RSV	GND
1	GND	VCC	+12V	RSV	-12V	VCC	GND

Table 6-2. CompactPCI Connector J2

Pin #	F	E	D	C	B	A	Z
22	GND	RSV	RSV	RSV	RSV	RSV	GND
21	GND	RSV	RSV	RSV	GND	CLK6	GND
20	GND	RSV	GND	RSV	GND	CLK5	GND
19	GND	RSV	RSV	RSV	GND	GND	GND
18	GND	BRSVP2E18	GND	BRSVP2C18	BRSVP2B18	BRSVP2A18	GND
17	GND	GNT6#	REQ6#	PRST#	GND	BRSVP2A17	GND
16	GND	BRSVP2E16	GND	DEG#	BRSVP2B16	BRSVP2A16	GND
15	GND	GNT5#	REQ5#	FAL#	GND	BRSVP2A15	GND
14	GND	AD[32]	GND	AD[33]	AD[34]	AD[35]	GND
13	GND	AD[36]	AD[37]	VIO	GND	AD[38]	GND
12	GND	AD[39]	GND	AD[40]	AD[41]	AD[42]	GND
11	GND	AD[43]	AD[44]	VIO	GND	AD[45]	GND

Table 6-2. CompactPCI Connector J2

Pin #	F	E	D	C	B	A	Z
10	GND	AD[46]	GND	AD[47]	AD[48]	AD[49]	GND
9	GND	AD[50]	AD[51]	VIO	GND	AD[52]	GND
8	GND	AD[53]	GND	AD[54]	AD[55]	AD[56]	GND
7	GND	AD[57]	AD[58]	VIO	GND	AD[59]	GND
6	GND	AD[60]	GND	AD[61]	AD[62]	AD[63]	GND
5	GND	PAR64	C/BE[4]#	VIO	GND	C/BE[5]#	GND
4	GND	C/BE[6]#	GND	C/BE[7]#	BRSVP2B4	VIO	GND
3	GND	GNT4#	REQ4#	GNT3#	GND	CLK4	GND
2	GND	REQ3#	GNT2#	SYSEN#	CLK3	CLK2	GND
1	GND	REQ2#	GNT1#	REQ1#	GND	CLK1	GND

CompactPCI Rear I/O Connectors (J3, J4, J5)

Table 6-3. CPV5370 Rear I/O Connector J3

Pin #	F	E	D	C	B	A	Z
19	GND	VDDCCLK	VDDCDAT	V_BLU	V_GRN	V_RED	GND
18	GND	GND	V_VSYN	V_HSYN	GND	HS_REQ	GND
17	GND	LANB RD-	LANB TD-	LANB TD+	GND	HS_GNT	GND
16	GND	LANB RD+	LANA RD-	LANA RD+	GND	HS_FLT	GND
15	GND	VCC-12	LANA TD-	LANA TD+	GND	HS_EJ	GND
14	GND	VCC	VCC	VCC3	VCC3	VCC3	GND
13	GND	PMC1	PMC2	PMC3	PMC4	PMC5	GND
12	GND	PMC6	PMC7	PMC8	PMC9	PMC10	GND
11	GND	PMC11	PMC12	PMC13	PMC14	PMC15	GND
10	GND	PMC16	PMC17	PMC18	PMC19	PMC20	GND
9	GND	PMC21	PMC22	PMC23	PMC24	PMC25	GND
8	GND	PMC26	PMC27	PMC28	PMC29	PMC30	GND
7	GND	PMC31	PMC32	PMC33	PMC34	PMC35	GND
6	GND	PMC36	PMC37	PMC38	PMC39	PMC40	GND
5	GND	PMC41	PMC42	PMC43	PMC44	PMC45	GND
4	GND	PMC46	PMC47	PMC48	PMC49	PMC50	GND
3	GND	PMC51	PMC52	PMC53	PMC54	PMC55	GND
2	GND	PMC56	PMC57	PMC58	PMC59	PMC60	GND
1	GND	PMC61	PMC62	PMC63	PMC64	VCC3	GND

Table 6-4. CPV5370 Signal Descriptions for J3

Signal	Signal Mnemonic	Signal Description
Ethernet	RD+, RD-	Differential receive lines
	TD+, TD-	Differential transmit lines

Table 6-4. CPV5370 Signal Descriptions for J3

Signal	Signal Mnemonic	Signal Description
Video Signal Definitions	V_RED	Red signal
	V_GREEN	Green signal
	V_BLU	Blue signal
	V_HSYNC	Horizontal synchronization
	V_VSYNC	Vertical synchronization
	VDDCCLK	Display Data Channel clock signal for DDC2 support
	VDDCDAT	Display Data Channel data signal for DDC2 support
General	GND	Ground plane
	VCC-12	-12Vdc power
	VCC5	5Vdc power
	VCC3.3	3.3Vdc power
Hot Swap Control Signals	HS_REQ	Hot Swap Request
	HS_GNT	Hot Swap Grant
	HS_FLT	Hot Swap Float
	HS_EJ	Hot Swap Eject
PMC2 I/O	PMC [1 to 64]	PMC I/O signals 1 through 64

Connector J4 contains floppy, printer port and miscellaneous functions. J4 is an optionally installed connector.))

Table 6-5. CPV5370 Rear I/O Pin Assignments (J4

Pin #	F	E	D	C	B	A	Z
25	GND	AD[32]	AD[33]	AD[34]	AD[35]	AD[36]	GND
24	GND	AD[37]	GND	AD[38]	AD[39]	AD[40]	GND
23	GND	AD[41]	AD[42]	AD[43]	AD[44]	AD[45]	GND
22	GND	AD[46]	AD[47]	AD[48]	VCC3	AD[49]	GND
21	GND	AD[50]	GND	AD[51]	AD[52]	AD[53]	GND
20	GND	AD[54]	AD[55]	AD[56]	VCC3	AD[57]	GND
19	GND	AD[58]	GND	AD[59]	AD[60]	AD[61]	GND
18	GND	AD[62]	AD[63]	PAR64	VCC3	C/BE[4]#	GND
17	GND	C/BE[5]#	GND	C/BE[6]#	C/BE[7]#	REQ64#	GND
16	GND	ACK64#	AD[0]	AD[1]	VCC3	AD[2]	GND
15	GND	AD[3]	GND	AD[4]	AD[5]	AD[6]	GND
KEY							
11	GND	AD[7]	GND	C/BE[0]#	AD[8]	AD[9]	GND
10	GND	AD[10]	AD[11]	AD[12]	VCC	AD[13]	GND
9	GND	AD[14]	GND	AD[15]	C/BE[1]#	PAR	GND
8	GND	SERR#	PERR#	LOCK#	VCC	STOP#	GND
7	GND	DEVSEL#	GND	TRDY#	IRDY#	FRAME#	GND
6	GND	C/BE[2]#	AD[16]	AD[17]	VCC	AD[18]	GND
5	GND	AD[19]	GND	AD[20]	CLK	AD[21]	GND
4	GND	AD[22]	AD[23]	RSV	VCC	C/BE[3]#	GND
3	GND	AD[24]	AD[25]	AD[26]	AD[27]	AD[28]	GND
2	GND	AD[29]	AD[30]	AD[31]	REQ#	GNT#	GND
1	GND	RST#	INTD#	INTC#	INTB#	INTA#	GND

Table 6-6. CPV5370 Rear I/O Pin Assignments (J5)

Pin #	F	E	D	C	B	A	Z
22	NC	SPKR-	VCC	ALARM-	GND	PBRESET-	GND
21	GND	MCLK	MDAT	VCC [1]	KBDCLK	KBDDAT	GND
20	NC	SMBLART	GND [1]	SMBCLK	SMBDATA	VCC [1]	GND
19	GND	UDATA0-	UDATA0+	VCC [1]	GND [1]	STB-	GND
18	NC	VCC [1]	GND [1]	UDATA1-	UDATA1+	AFD-	GND
17	GND	PD0	ERR-	PD1	INIT-	PD2	GND
16	NC	SLIN-	PD3	PD4	PD5	PD6	GND
15	GND	PD7	ACK-	BUSY	PE	SLCT	GND
14	NC	DTR(1)	GND	RI(1)	CTS1	RTS(1)	GND
13	GND	TXD(1)	DSR1	RXD(1)	VCC	DCD(1)	GND
12	NC	DTR(2)	VCC	RI(2)	CTS2	RTS(2)	GND
11	GND	TXD(2)	DSR(2)	RXD(2)	GND	DCD(2)	GND
10	NC	DSKCHG-	HDSEL-	RDATA-	WPROT-	TR0-	GND
9	GND	WGATE-	WDATA-	STEP-	DIR-	MTR1-	GND
8	NC	DS0-	DS1-	MTR0-	INDEX-	DRATE	GND
7	GND	RPM_LC	+12.0V	DA1	CS3-	CS1-	GND
6	NC	DA2	DA0	RSVD	GND	RSVD	GND
5	GND	DIOR-	DMACK-	DIOW	IORDY	DMARQ	GND
4	NC	INTRQ	DD15	GND	DD0	DD14	GND
3	GND	DD1	DD13	DD2	DD12	DD3	GND
2	NC	DD11	DD4	DD10	DD5	DD9	GND
1	GND	DD6	DD8	DD7	DRESET-	RESET-	GND

[1] These lines may be current limited and/or EMI filtered for direct cabling

Table 6-7. CPV5370 Signal Descriptions for Connector J5

Signal	Signal Mnemonic	Signal Description
General	VCC	5V power supply
	GND	Digital signal ground plane
Keyboard/Mouse Device, TTL Levels	MCLK	Clock for PS/2 mouse
	MDAT	Serial data line for PS/2 mouse
	KBDCLK	Clock for PC/AT or PS/2 keyboard
	KBDDAT	Serial data line for PC/AT or PS/2 keyboard
Miscellaneous Signals	SPKR	PC/AT speaker output, open collector
	DIAG	Diagnostic/alarm output, open collector
	PBRESET	Pushbutton system reset input (pulled up, filtered, and debounced on host card)
	RESET	System reset output, TTL totem-pole
SM Bus Signals	SMBDATA	System Management Bus signals
	SMBCLK	
	SMBALRT	

Table 6-7. CPV5370 Signal Descriptions for Connector J5 (Continued)

Signal	Signal Mnemonic	Signal Description
EIDE (ATA-2), Secondary Channel, TTL levels	IOCS16-	Indicates a 16 bit register is decoded
	DMARQ	Drive DMA request
	DMACK-	Drive DMA acknowledge
	DIOR-	Drive I/O read
	DIOW-	Drive I/O write
	DASP-	Drive active/slave present
	IORDY	Indicates drive is ready for I/O cycle(s)
	DD[15:0]	Drive data lines, bits 15--0
	DRESET-	Reset signal to drive
	CS1-	Chip select drive 0, also command register block select
	CS3-	Chip select drive 1, also command register block select
	DA[2:0]	Drive register and data port address lines
	INTRQ	Drive interrupt request
	PDIAG-	Output from drive 1 and monitored by drive 0
Parallel LPT Port, TTL levels [1]	ACK-	Pulsed by peripheral to acknowledge data sent
	BUSY	Indicates that the printer cannot accept more data
	ERR-	Peripheral detected an error
	PD[7:0]	Parallel data lines, bits 7--0
	PE	Paper end, indicates the printer is out of paper
	AFD-	Auto feed, causes printer to line feed
	INIT-	Initializes the printer
	SLIN-	Select in, selects the printer
	STB-	Data strobe, indicates data is valid
	SLCT	Select, peripheral indicates it is selected

Table 6-7. CPV5370 Signal Descriptions for Connector J5 (Continued)

Signal	Signal Mnemonic	Signal Description
Serial COM Ports (1 and 2), RS232 levels	CTS	Clear to send
	DCD	Data carrier detected
	DSR	Data set ready
	DTR	Data terminal ready
	RI	Ring indicator
	RTS	Request to send
	RXD	Serial receive data
	TXD	Serial transmit data
Floppy Disk Drive, TTL levels	DSKCHG-	Indicates the drive door is open
	DIR-	Controls direction of the head during step operations
	DRVDENS[1:0]	Disk density select communication
	DS[1:0]-	Drive selects
	HDSEL-	Selects top or bottom side head
	INDEX-	Indicates the beginning of a track
	MTR[1:0]	Motor enables
	RDATA-	Data read
	STEP-	Step, pulses move head in or out
	TR0-	Indicates that head is positioned above track 00
	WDATA-	Write data to drive
	WGATE-	Enables head write circuitry of drive
	WPROT-	Indicates disk is write-protected
Universal Serial Bus (USB) (0 and 1), USB levels	UDATAn+	(+) Signal of differential data pair for USB channel
	UDATAn-	(-) Signal of differential data pair for USB channel
[1] Some signals are redefined when used in EPP/ECP modes		

Table 6-8. CPV5370 Ethernet Connector Pin Assignments (J10, J9)

Pin Number	Signal Mnemonic	Signal Description
1	TX+	Differential transmit lines
2	TX-	Differential transmit lines
3	RX+	Differential receive lines
4	-	-
5	-	-
6	RX-	Differential receive lines
7	-	-
8	-	-

Table 6-9. CPV5370 COM 1 Serial Port Connector (J19)

Pin Number	Single Mnemonic	Signal Description
1	DCD	Data set has detected the data carrier
2	RX	Receives serial data input from communications link
3	TX	Sends serial output to communications link
4	DTR	Indicates that a data terminal is ready to establish a communications link
5	GND	Ground
6	DSR	Indicates that a data set is ready to establish a communications link
7	RTS	Indicates to data set that UART is ready to exchange data
8	CTS	Indicates that data set is ready to exchange data
9	RI	Indicates that a modem has received a telephone ringing signal

Table 6-10. CPV5370 Video Connector Pin Assignments (J17)

Pin Number	Signal Mnemonic	Signal Description
1	RED	Red signal
2	GREEN	Green signal
3	BLUE	Blue signal
4	NC	no connection
5	DACVSS	Video return
6	DACVSS	Video return
7	DACVSS	Video return
8	DACVSS	Video return
9	NC	no connection
10	DACVSS	Video return
11	NC	no connection
12	DDCDAT	Display Data Channel data signal for DDC2 support
13	HSYNC	Horizontal synchronization
14	VSYNC	Vertical synchronization
15	DDCCLK	Display Data Channel clock signal for DDC2 support

Table 6-11. CPV5370 Keyboard/Mouse/PS2 Connector Pin Assignments (J7)

Pin Number	Signal Mnemonic	Signal Description
1	KBDDAT	Data line for keyboard
2	MDAT (AUXDAT) [1]	Data line for mouse
3	GND	Keyboard Ground
4	KBDVCC	Keyboard Power
5	KBDCLK	Clock for keyboard
6	MCLK (AUXCLK) [2]	Clock for mouse
7	CGND	Common Ground

[1] AUXDAT is Data line for mouse for the CPTM04

[2] AUXCLK is Clock for mouse for the CPTM04

Specifications A

This appendix provides general specifications including mechanical, environmental, and electrical for the CPV5370.

Table A-1. Power Requirements for the CPV5370 and CPTM04

Input power	Clock speed
+5V @ 2.9A	700 MHz with 256MB, 512MB, or 1GB SDRAM
+5V @ 4.25A	1 GHz with 256MB, 512MB, or 1GB SDRAM
+3.3V @ 2.0A	700 MHz with 256MB, 512MB, or 1GB SDRAM
+3.3V @ 2.3A	1 GHz with 256MB, 512MB, or 1GB SDRAM
+12V @ <25mA typical, <25mA maximum	700 MHz or 1 GHz
-12V @ .05A typical, .05A maximum	700 MHz or 1 GHz

Table A-2. Physical Characteristics of the CPV5370

Parameter	Description
Form Factor	CompactPCI Standard 6U (233mm x 160mm x 20mm) Conforms to PICMG 2.0, CompactPCI and PCI SIG 2.1 specifications
Dimensions	4 HP (.8 inches) wide

Table A-3. Lithium Battery Specifications

Rating	Shelf Life
180mA/hour	2 years

Table A-4. Environmental Specifications

Parameter	Condition	Specification
Temperature	Operating	0°C to 50°C (32°F to 122°F) [2]
	Nonoperating	-40°C to 70°C (°-40F to 158°F)
Humidity	Operating	5% to 90% @ 40°C, noncondensing
	Nonoperating	5% to 95% @40°C, noncondensing
Cooling	na	35 CFM over the Single Board Computer
MTBF (MIL-HDBK-217F)	Operating	300,000 hours at 30°C 100,000 hours at 50°C

[1] Environmental Specifications exclude the on-board hard drive option

[2] Derate the maximum operating temperature by 1°F (1.8°C) per 3280 feet (1000m) above sea level.

Thermal Analysis B

Ambient temperature, air flow, board electrical operation, and software operation affect board component temperatures. To evaluate the thermal performance of a circuit board assembly, you should test the board under actual operating conditions. These operating conditions vary depending on system design.

Motorola Computer Group performs thermal analysis in a representative system to verify operation within specified ranges. Refer to *Specifications*, Table A-2 on page A-1. You should evaluate the thermal performance of the board in your application.

To prevent damage, automatic clock throttling is supported by the hardware should the CPU junction temperature exceed 95 degrees Fahrenheit.

This appendix gives systems integrators the information necessary to conduct thermal evaluations of the board in a specific system configuration. It identifies thermally significant components and lists the corresponding maximum allowable component operating temperatures. It also provides example procedures for component-level temperature measurements.

Thermally Significant Components

Table B-1 summarizes components that show significant temperature rises. You should monitor these components to assess thermal performance. Table B-1 also supplies the component reference designator and the maximum allowable operating temperature.

B

You can find components on the board by their reference designators. Refer to Figure B-1 and Figure B-2. Versions of the board that are not fully populated may not contain some of these components.

The preferred temperature measurement location for a component may be:

- Junction - refers to the temperature measured by an on-chip thermal device
- Case - refers to the temperature at the top, center surface of the component
- Air - refers to the ambient temperature near the component

Table B-1. Thermally Significant Components on the CPV5370

Reference Designator	Generic Description	Maximum Allowable Component Temperature (degrees C) [1]	Measurement Location
U1	Pentium III CPU	100	Junction
U13	Host Bus to PCI Bus Bridge/Memory Controller Chip	105	Case
U32	AGP video chip	70	Air
[1] maximum temperature for reliable operation specified by the component manufacturer.			

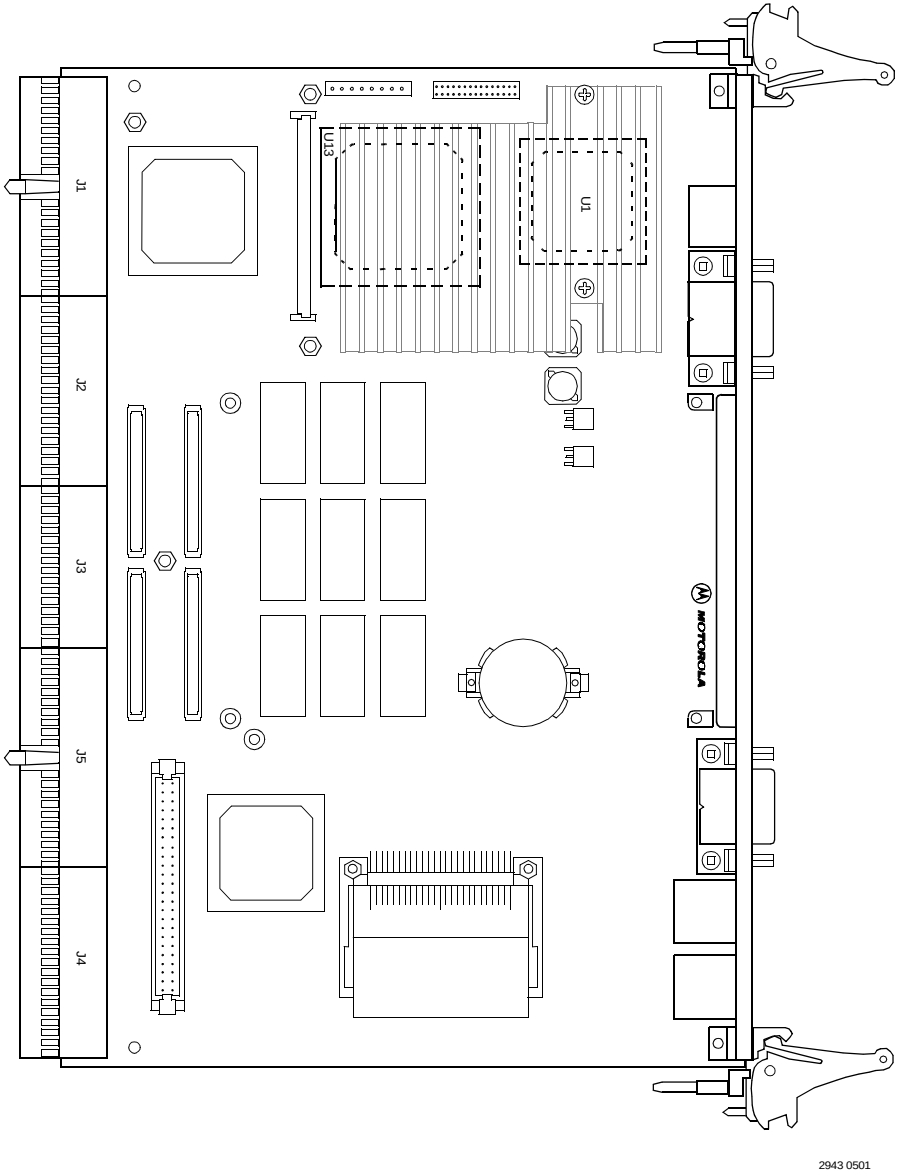


Figure B-1. Location of Thermally Significant Components - Primary Side

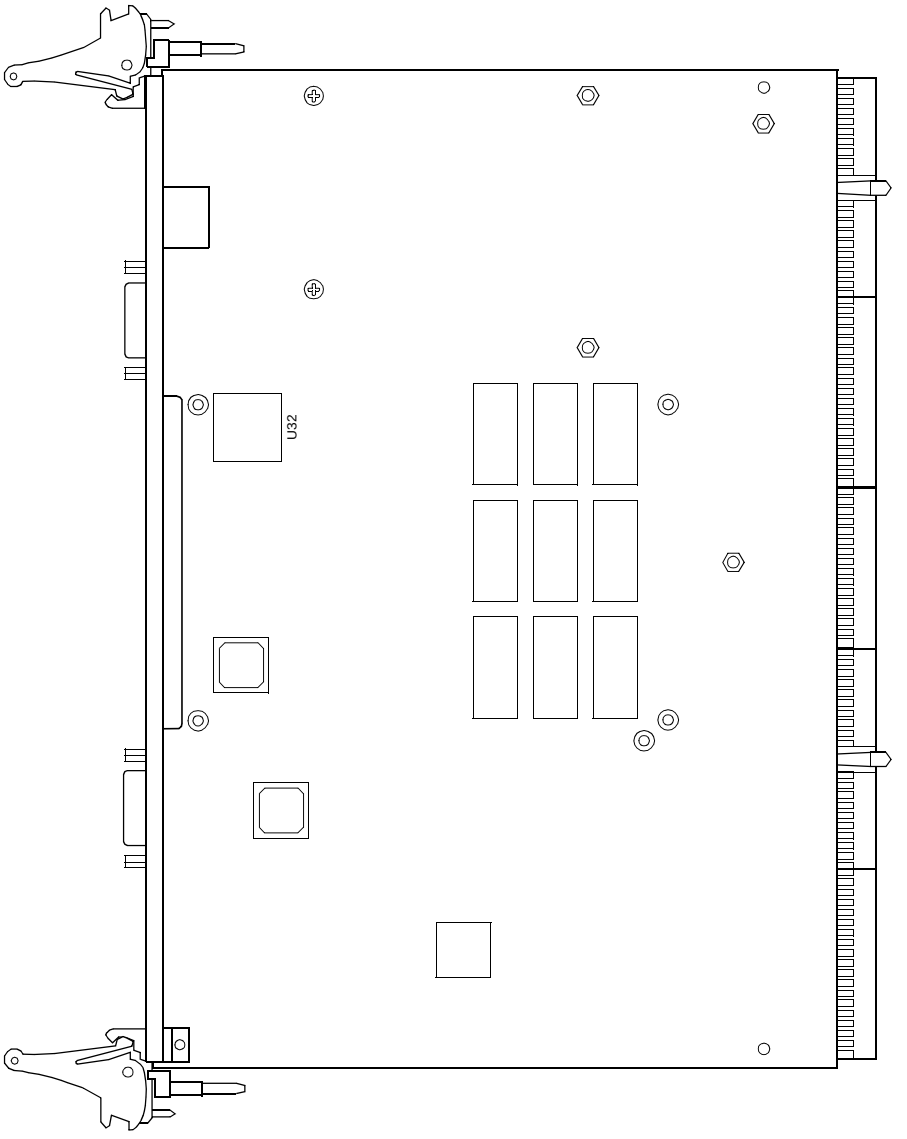


Figure B-2. Location of Thermally Significant Components - Secondary Side

Component Temperature Measurement

This section outlines general temperature measurement methods. For the specific types of measurements required for thermal evaluation of this board, see Table B-1.

Preparation

We recommend 40-gage thermocouples for all thermal measurements. Larger gage thermocouples can wick heat away from the components and disturb air flowing past the board.

Allow the board to reach thermal equilibrium before taking measurements. Most circuit boards reach thermal equilibrium within 30 minutes. After the warm up period, monitor a small number of components over time to assure that equilibrium is reached.

Measuring Junction Temperature

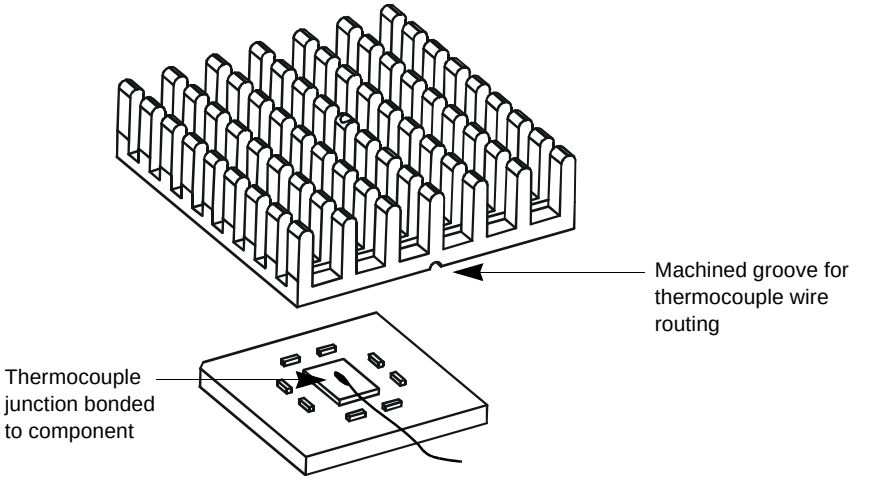
Some components have an on-chip thermal measuring device such as a thermal diode. For instructions on measuring temperatures using the on-board device, refer to the CPV5370 Single Board Computer Programmer's Reference Guide.

Measuring Case Temperature

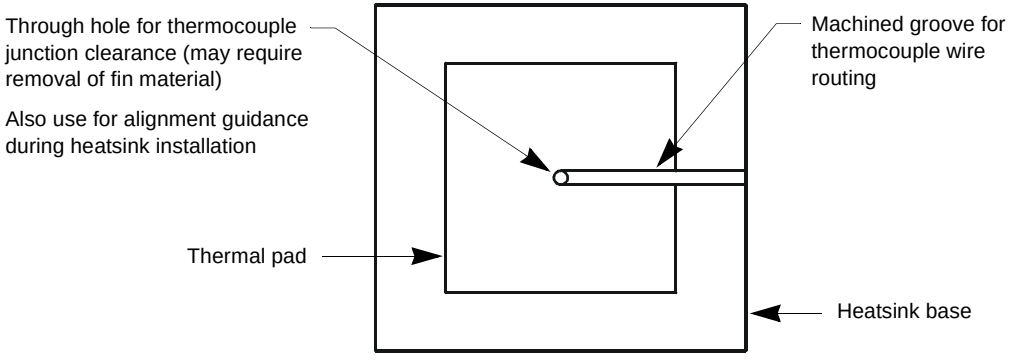
Measure the case temperature at the center of the top of the component. Make sure there is good thermal contact between the thermocouple junction and the component. We recommend you use a thermally conductive adhesive such as Loctite 384.

If components are covered by mechanical parts such as heatsinks, you need to machine these parts to route the thermocouple wire. Make sure that the thermocouple junction contacts *only* the electrical component. Also make sure that heatsinks lay flat on electrical components. Figure B-3 shows one method of machining a heatsink base to provide a thermocouple routing path.

Note Machining a heatsink base reduces the contact area between the heatsink and the electrical component. You can partially compensate for this effect by filling the machined areas with thermal grease. The grease should not contact the thermocouple junction.



ISOMETRIC VIEW



HEATSINK BOTTOM VIEW

Figure B-3. Mounting a Thermocouple Under a Heatsink

Measuring Local Air Temperature

Measure local component ambient temperature by placing the thermocouple downstream of the component. This method is conservative since it includes heating of the air by the component. Figure B-4 shows one method of mounting the thermocouple.

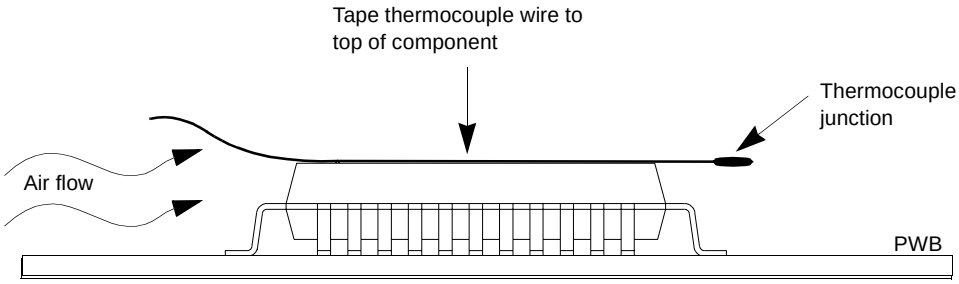


Figure B-4. Measuring Local Air Temperature

Related Documentation C

Motorola Computer Group Documents

The Motorola publications listed below are referenced in this manual, or apply to systems that use this product. You can obtain electronic copies of Motorola Computer Group publications by:

- Contacting your local Motorola sales office, or
- Visiting Motorola Computer Groups's World Wide Web literature site, http://www.motorola.com/computer/literature

Table C-1. Motorola Computer Group Documents

Document Title	Motorola Publication Number
CPV5350 CompactPCI BIOS and Programmer's Reference Guide	CPV5350A/PGx

To get the most up-to-date product information in PDF or HTML format, visit http://www.motorola.com/computer/literature.

Manufacturers' Documents

For additional information, refer to the following table for manufacturers' data sheets and user's manuals. For your convenience, a source for the listed document is also provided.

It is important to note that in many cases, the information shown is preliminary and the revision levels of the documents are subject to change without notice.

Table C-2. Manufacturers' Documents

Document Title and Source	Publication Number
Distributed Management Task Force, Inc. Go to **DMTF** to search for documentation	
System Management BIOS Reference Specification, v2.3.1	dsp0119.pdf
Intel Corporation Go to Literature Center for Search Engine	
Mobile Pentium III Processor in BGA2 and Micro-PGA2 Packages Data Sheet	245302.htm
Intel 82554GC 10/100Base-T Ethernet PCI Bus Controller Intel CompactPCI Transparent Bridge - 21154	82544.pdf 21154.pdf
Intel PIIX4E South Bridge 82371	290562.pdf
Intel 440GX AGPset: 82443GX Host Bridge/Controller	290638.pdf
Intel StrataFlash Memory 28F320J5	29060615.pdf
Intel 82559ER Fast Ethernet PCI Controller with Integrated PHY	82559.pdf
Intel AGP Video 69030	69030.pdf
Atmel, http://www.atmel.com/	
AT17C128 SEEPROM	
Maxim Corp., http://pdfserv.maxim-ic.com/	
MAX1617 Remote/Local Temperature Sensor with SMBus Serial Interface	1855.pdf
National Semiconductor, http://www.national.com/	

Table C-2. Manufacturers' Documents (Continued)

Document Title and Source	Publication Number
LM81 Microprocessor System Hardware Monitor National Semiconductor Corporation	LM81.html
PC97307VUL (Super I/O™ Enhanced Sidewinder Lite) Floppy Disk Controller, Keyboard Controller, Real-Time Clock, Dual UARTs, IEEE 1284 Parallel Port, and IDE Interface http://www.national.com/	PC87307.html
Phoenix Technologies, http://www.phoenix.com/pcuser	
PhoenixBIOS 4.0 Release 6 User's Manual Phoenix Technologies	userman.pdf
Standard Microsystems Corporation (SMSC) **Search for documentation at** http://www.smsc.com/	
Enhanced Super I/O Controller with Fast IR, FDC37C672 Data Sheet	fdc37c67x.html fdc37c672.pdf

Related Specifications

C

For additional information, refer to the following table for related specifications. For your convenience, a source for the listed document is also provided. It is important to note that in many cases, the information is preliminary and the revision levels of the documents are subject to change without notice

Table C-3. Related Specifications

Document Title and Source	Publication Number
IEEE Institue of Electrical and Electronics Engineers, Inc. http://standards.ieee.org/catalog/	
IEEE Standard for Compact Embedded PC Modules	IEEE P996.1
IEEE - Common Mezzanine Card Specification (CMC)	P1386 Draft 2.0
IEEE - PCI Mezzanine Card Specification (PMC)	P1386.1 Draft 2.0
Bidirectional Parallel Port Interface Specification	IEEE Standard 1284
Intel Corp. Go to Literature Center for Search Engine	
Accelerated Graphics Port Interface Specification, Revision 1.0 Universal Serial Bus (USB) Wired for Management, PXE (Preboot Execution Environment)	
PCI Industrial Manufacturers Group (PICMG) http://www.picmg.com/	
Compact PCI Specification	PICMG 2.0 Rev. 2.1 Dated 9/2/97
PCI-PCI Bridge Specification for Single Board Computers	PICMG 1.1 Rev. 1.02
CompactPCI Hot Swap Specification	PIMCG 2.1 R1.0
PCI Special Interest Group (PCI SIG) http://www.pcisig.com/	
Peripheral Component Interconnect (PCI) Local Bus Specification, Revision 2.0, 2.1, 2.2	PCI Local Bus Specification

Index

Numerics

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