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November, 1989

MIZAR

MZ 8115

NASA Custom CPU Module

User's Manual

Publication No. 4425237

If you have any technical questions about this product, call Mizar at
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Second Edition
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MZ 8115 Product Notes

UNPACKING

This board contains components that are susceptible to static discharge and should be handled with appropriate caution.

Upon receipt, inspect the board for missing, broken, or damaged components and for physical damage to the printed circuit board or connectors. This product was shipped in perfect condition. Any damage to the product is the responsibility of the shipping carrier and should be reported to the carrier's agent immediately.

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DIFFERENCES BETWEEN MZ 8115 NASA CUSTOM AND STANDARD MIZAR MZ 8115

1) S1 IRQ1, IRQ2 changed from autovectored interrupts to vectored.

2) New A/W, no. 6800-04414-0000.

3) RJ-11 jacks replaced standard 26-pin flat ribbon cables for both RS232 connections.

4) Customized NASA front panels were installed, identified by "LANC," "CPSM," and "68010/CPU" I.D. plates.

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CHAPTER 1

GENERAL INFORMATION

1.1 INTRODUCTION

This manual provides the necessary background information required to take full advantage of the MZ 8115. A general overview of the functional groups of the MZ 8115 is presented in this chapter. A complete configuration guide, found in Chapter 1 provides all the information required to configure the board to the users environment. A more detailed description on how the board works is offered in the operation guide in Chapter 3. Chapter 4 contains a brief discussion on programming considerations for the MZ 8115.

The MZ 8115 is a 3U x 160mm VMEbus, CPU module which has been designed to allow for easy customization to a full 6U x 160mm board. The MZ 8115 is designed to be installed in the P1 connector of the VMEbus. Installing the MZ 8115 into the P2 slot on any VMEbus system may cause damage to both the MZ 8115 and the P2 bus. Note that an MZ 8115 expanded board can be designed to be inserted into the P2 slot if required, with the original MZ 8115 portion of the board inserted into slot P1.

Board Specifications:

Processor

Speed: 10 or 12.5 MHz 68000 or 68010

RAM

512K Dynamic
Dual-Ported--Onboard/VMEbus
CPU Address: $0000
VMEbus Address: $E80000 (PAL Selectable)

ROM

16K, 32K, 64K or 128K
2764, 27128, 27256 or 27512
Intel Pinout
Base Address: $F80000

Serial Ports

68681-Dual RS232 Ports
18 Programmable Baud Rates
Baud Rate via 16-bit timer
Interrupt Request levels 3 and 5
Base Address: $FE8000

Address Map

$000000 - $07FFFF RAM
$080000 - $EFFFFF Off-board Standard Access
$F00000 - $F7FFFF Open
$F80000 - $F9FFFF ROM
$FA0000 - $FE7FFF Open
$FE8000 - $FEFFFF 68681 Serial Chip
$FF0000 - $FFFFFF Off-board Short I/O Access

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Data Transfer

A24:D16 Master
A16:D8 Master
A24:D16 Slave
A24:D8 Slave

Power

3.5A typical at 5 VDC
20mA typical at +12V
20mA typical at -12V

Environmental

Operating Temp.: 0 to 55° C inlet air temp, forced air cooling
Maximum Humidity: 90% noncondensing

Physical

3U x 160mm Eurocard

1.2 FUNCTIONAL DESCRIPTION

The MZ 8115 is a 3U x 160mm 68000/68010 CPU board with a special side connector (the S1 MXbus™ connector) that allows for custom expansion to a 6U x 160mm CPU card. The main functional groups of the MZ 8115 are described briefly in the following subsections. For more information, refer to the theory of operation section of this manual.

1.2.1 Bus Master Module

The MZ 8115 is designed to be a VMEbus master with complete interrupt handling and bus arbitration capabilities. The interrupt handler can be configured to respond to any or all of the seven VMEbus interrupt levels, as well as a number of onboard interrupts. The MZ 8115 can request bus control on any one of the four bus request levels.

1.2.2 System Controller

The MZ 8115 contains an onboard system controller which, when enabled, allows the MZ 8115 to be positioned in slot 1 and act as the VMEbus system controller. The onboard system controller can be configured to arbitrate in either priority or round robin arbitration modes. The system controller can be disabled if another CPU card with system controller capabilities is used in slot 1 or not used in slot one.

1.2.3 Serial Ports

Two asynchronous serial ports RS232 compatible are onboard. These serial ports are provided by a 68681 dual asynchronous communication chip which has fully programmable data generation and interrupt handling capabilities.

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1.2.4 EPROM

The MZ 8115 contains two EPROM sockets which can accept 2764, 27128, 27256 or 27512 EPROMs. Thus up to 128K of EPROM can be accessed. *Note that the upper socket houses the high byte of EPROM.* The starting address for ROM is selected by PAL's to be $F80000. Upon resetting the MZ 8115, the CPU is hardware configured to read the first eight bytes of ROM as the initial stack pointer and program counter, just as if ROM was located at $0000. Thus, the initial stack pointer will be located at $F80000 and the initial program counter at $F80004.

Recommended EPROM access times are 170 nsec for the 12.5 MHz CPU versions of the MZ 8115, and 200 nsec for the 10 MHz CPU version.

1.2.5 Time-of-Day Clock

An optional time-of-day clock is provided by the Dallas Semiconductor 1216E SmartWatch. The clock provides battery backed time information, including hundredths of seconds, seconds, minutes, days, date, month, and year. The clock automatically adjusts for months of less than 31 days, and for leap years, and operates in either 12 or 24 hour formats. Data is in BCD format for easy conversion. An internal lithium battery maintains time and date when the MZ 8115 is powered down for greater than 10 years.

1.2.6 Dual-Ported Ram

The MZ 8115 has 512K of dual-ported dynamic RAM which operates with zero wait states at both 10 and 12.5 MHz processor speeds. This RAM can be accessed from onboard or from any other master on the VMEbus. PAL's select RAM for addresses in the range of $0000 to $07FFFF. Off-board access to the dual-ported RAM is selected for addresses in the range of $E80000 to $EFFFFF and can be easily changed in PAL's if desired.

1.2.7 S1 MXbus Connector

The S1 MXbus side connector allows custom expansion of the CPU board. A full array of address lines, data lines and interrupt lines are passed through to the S1 connector. In addition, the microprocessor function codes, bus request and bus grant signals are also passed to the S1 connector.

Two modes of interrupt generation are available for boards designed for connection to the S1 connector. The first mode is to interrupt the MZ 8115 as an onboard local interrupt (via signals S1IRQ1 & 2). The second mode is to interrupt the VMEbus on any of the VME request lines IRQ1-7 (via signals BIRQ1 & 2).

Typical applications for the S1 connector would expand the MZ 8115 to include additional serial or parallel ports, floppy disk control, or additional memory. The expanded board can use the P2 connector to handle upper address and data lines, as well as for user defined lines. Mizar's MZ 8800 Series of MXbus expansion modules connect directly to the MZ 8115's S1 connector. Contact Mizar for additional expansion module information.

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1.2.8 Front Panel LED's and Switches

Two LED'S are positioned on the edge of the board and provide a visual indication of the state of the board. The lower LED is the HALT LED, and indicates whether the CPU has stopped. The LED, next to the switches, is the BUS MASTER LED, and indicates whether or not the MZ 8115 has control of the bus.

Two pushbutton switches provide for system reset and ABORT capabilities. The lower switch next to the LEDs, is the ABORT switch and generates an autovectored, level 7 interrupt to the CPU. The upper switch next to the serial port connector, is the RESET switch. This provides an onboard reset to the MZ 8115 and a system reset when the MZ 8115 is configured as the system controller.

1.3 WHERE TO CALL FOR HELP

Mizar staffs a technical support center to answer any questions you may have on any of our products. If you have any questions about programming, configuring, or general operation of the MZ 8115, or any of our other products, call Mizar at 800-635-0200 (in Texas, 214-446-264). Engineers are available to assist you.

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CHAPTER 2

CONFIGURATION GUIDE

2.1 INTRODUCTION

The MZ 8115 contains eight jumper blocks that must be configured to the user's enviroment. These jumpers specify EPROM type, parity mode check enable, system controller enable, bus arbitration type, bus request level and whether the IACK daisy chain is passed to the S1 connector.

2.2 K1 - PARITY MODE ENABLE

When enabled, the MZ 8115 will perform parity checking on RAM read cycles. This is a check to ensure that the number of high bits that were saved during a write cycle agree with the number that are read during a read cycle. If they don't agree, an error occurred and the MZ 8115 will issue a BERR (Bus error). *NOTE: Addition of parity checking will slow RAM access cycles by one to two wait states (80-160nsec at 12.5MHz).*

Parity checking is enabled by placing a jumper across K1. If K1 is left unjumpered, no parity checking is done.

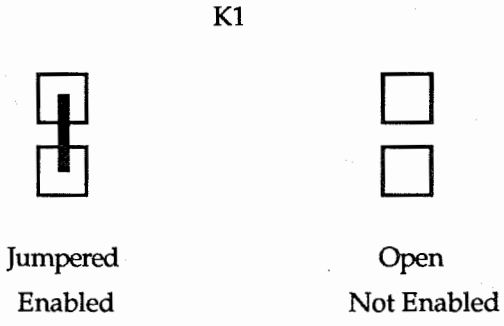


Figure 2.1 Parity Mode Enable

2.3 K2 - S1 IACK Daisy chain Jumper

During an interrupt cycle, an IACKIN/IACKOUT daisychain is passed through each board. For a slave to be acknowledged as the interrupter, it must receive IACKIN. Any board that receives IACKIN but does not generate an interrupt at the acknowledged level, must pass IACKOUT to the next slot.

The MZ 8115 itself does not generate interrupts on any of the VMEbus interrupt request levels. The S1 connector, however, allows for custom expansion boards that can generate VMEbus interrupts via the signals BIRQ1 and BIRQ2. These signals will pass through the S1 connector to the MZ 8115 where they are jumpered via K3 to the appropriate interrupt request level passing through to the P1 connector. K2 passes the IACKIN/IACKOUT daisy chain through the S1 connector to the expansion board.

If there is no S1 expanded board, or if the S1 expanded board only issues onboard MZ 8115 interrupts, then the IACKIN/IACKOUT daisy chain should be shorted, passing IACKIN directly to IACKOUT. This is accomplished by placing a jumper across jumper block K2.

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If the S1 expanded board does exist and generates interrupts on the VMEbus interrupt levels, then the IACK daisychain must pass through it. In this case, the jumper block K2 must be left unjumpered.

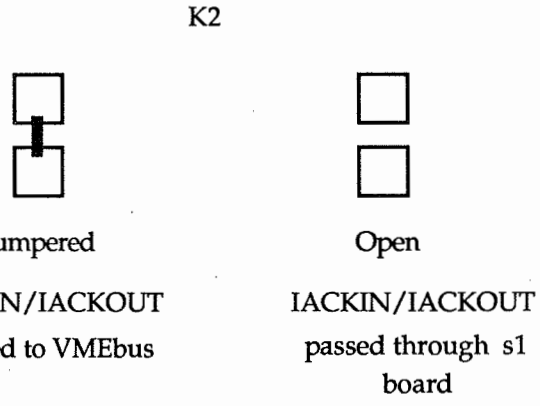


Figure 2.2 IACK Daisy Chain

2.4 K3-EPROM & IRQX SELECT

2.4 (a) K3 (PIN PAIRS 1 AND 2) EPROM SELECT

The two EPROM sockets on the MZ 8115 have provisions for accepting 2764, 27128, 27256 and 27512 EPROMS. The upper socket houses the high byte EPROM, and the lower socket houses the low byte. The upper portion of K3 allows for specific device configuration. Jumpering pins 1 and 11 connects address line A16 to pin 1 of the EPROM socket. Jumpering pins 2 and 12 connects address line A15 to the EPROM device through pin 17.

Jumpering both jumper pairs (1,11 and 2,12) selects the 27512. Jumpering only pair 2 (pins 2,12) selects the 27256. No jumper selects either the 2764 or 27128.

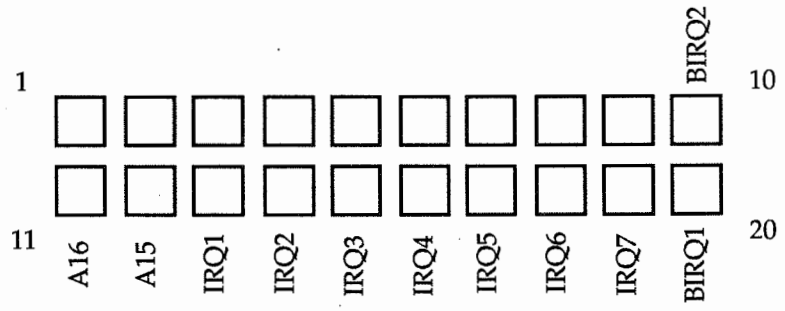
2.4 (b) K3 (LOWER SECTION OF JUMPER BLOCK, PIN PAIRS 3-10) IRQX SELECT

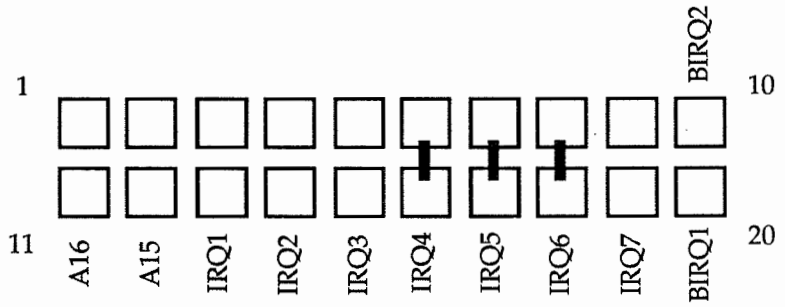
As a CPU master, the MZ 8115 can be configured to respond to any of the seven interrupt request levels. The lower portion of jumper block K3 is jumpered to select which interrupt levels the MZ 8115 will respond to. If no jumper is placed across a given pair on the jumper block, the MZ 8115 will not respond to that interrupt level. Note that any given interrupt level must only be handled by one master on the VMEbus.

K3 is used to configure the two S1 interrupt lines, BIRQ1 and BIRQ2, that interrupt via the VMEbus. To configure these two lines, wirewrap pins 10 or 20 (for BIRQ2 or BIRQ1 respectively) to any of the interrupt request pins 13-19 depending on the level desired. Note that since BIRQ1 and BIRQ2 are generated from the same board, they cannot be wirewrapped to the same request level. Also note that the MZ 8115 should not be allowed to respond to the interrupt levels selected for BIRQ1 and BIRQ2. These interrupts are intended for off-board interrupting only.

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K3

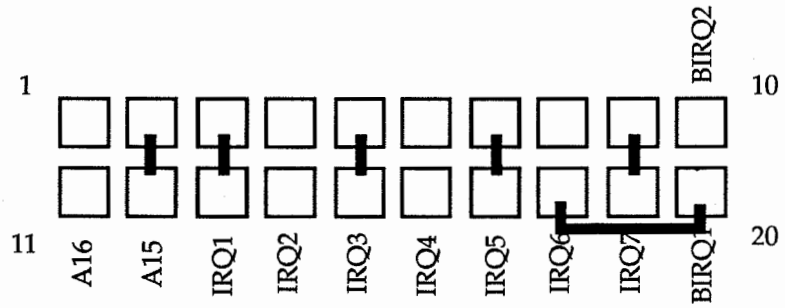




MZ 8115 responds to interrupt levels 4, 5 and 6.

2764 EPROMS are used.

BIRQ1 and BIRQ2 not used.



MZ 8115 responds to interrupt levels 1, 3, 5 and 7.

27256 EPROMS are used.

BIRQ1 selected at level 6, but is not responded to by the MZ 8115

Figure 2.3 EPROM and IRQx Select

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2.5 K4 - BUS TIMEOUT ENABLE

The system controller chip on the MZ 8115 has a built-in bus timeout mechanism which will generate BERR if a given bus cycle takes too long. The system controller monitors the two data strobe lines, DS0 and DS1, and generates BERR if either of these signals stay low for more than 64 usec. It may be desirable to disable this feature allowing the VMEbus to 'hang up' rather than generate BERR, especially during debugging. This allows the last address attempted to be examined, as well as the status of all of the control lines on the VMEbus.

To enable the bus timeout feature, a jumper should be placed across K4. To disable this feature, K4 should be left unjumpered.

NOTE: The system controller chip must be enabled ,and the MZ 8115 must reside in slot 1 of the VMEbus backplane for the bus timeout feature to have any affect.

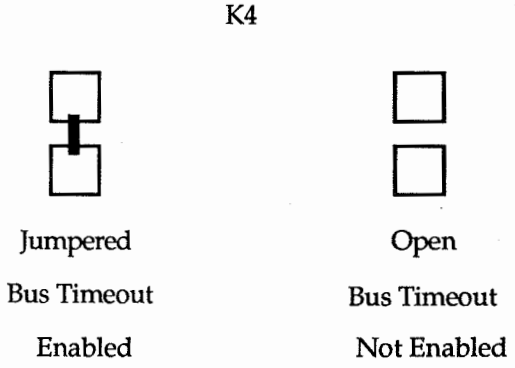


Figure 2.4 Bus Timeout Enable

2.6 K5 - SYSTEM CONTROLLER ENABLE

A jumper is placed across K5 to configure the MZ 8115 as the system controller. Note that when configured as the system controller, the MZ 8115 must be located in slot 1 of the VMEbus. If K5 is not jumpered, the MZ 8115 does not act as the system controller and can be placed in any slot but 1.

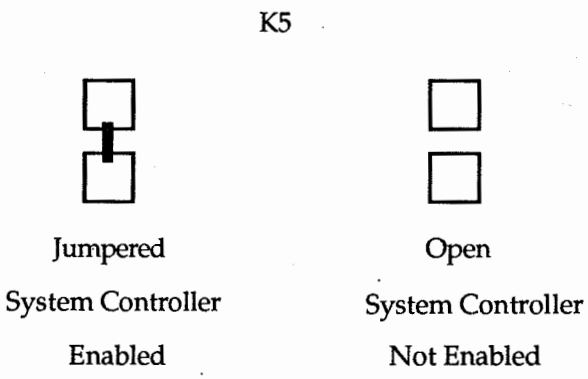


Figure 2.5 System Controller Enable

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2.7 K6 - BUS ARBITRATION TYPE

When configured a system controller, this jumper allows the MZ 8115, to be configured to arbitrate bus requests in either fixed priority or round robin arbitration modes. When K6 is jumpered, the MZ 8115s system controller arbitrates in priority mode. With no jumper, round robin mode is assumed.

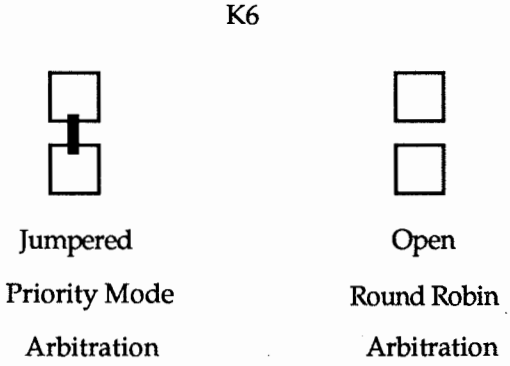


Figure 2.6 Bus Arbitration Type

2.8 K7 - BUS REQUEST LEVEL SELECTION

The MZ 8115 can request control of the VMEbus from the system controller on any one of the four bus request levels. Pin 1 of jumper block K7 is wirewrapped to the desired level as shown:

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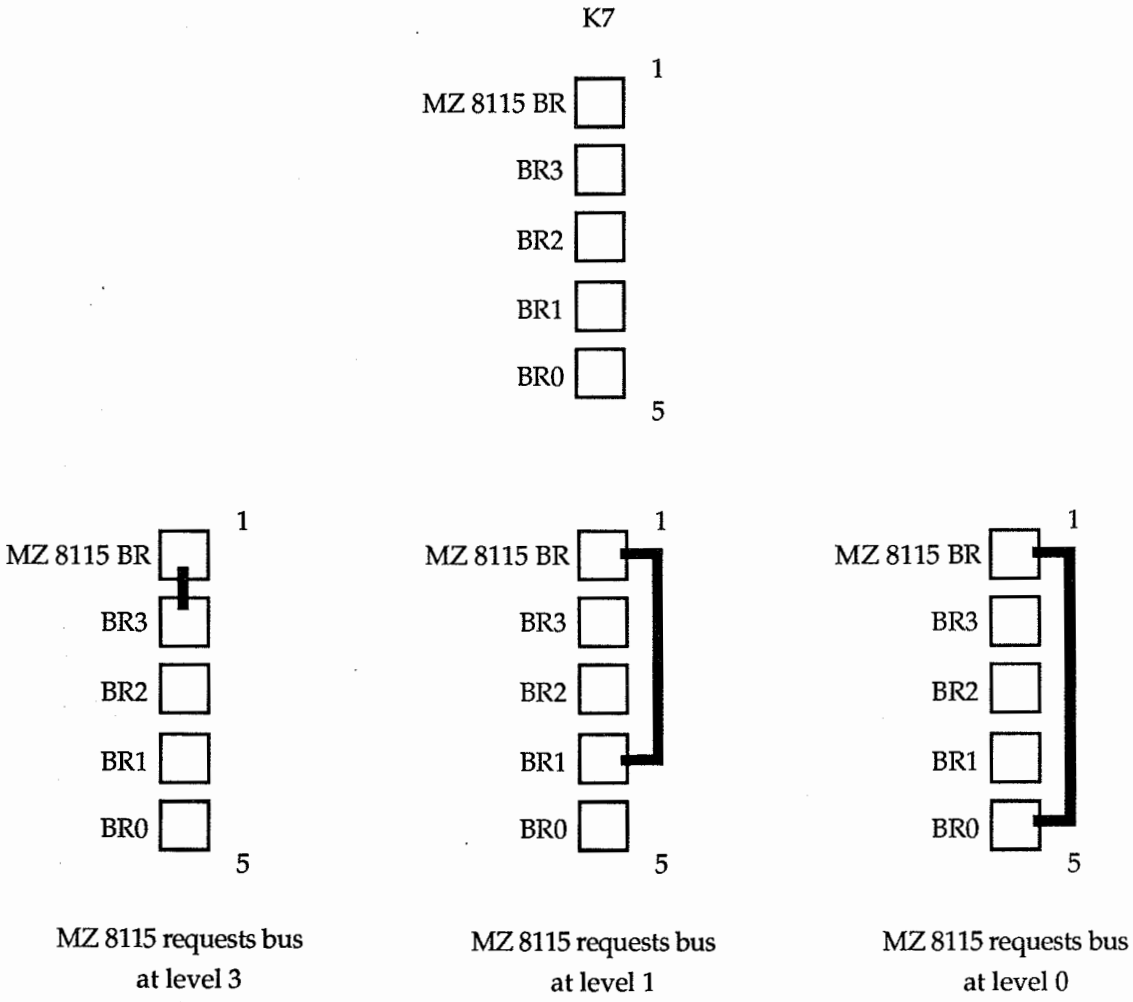


Figure 2.7 Bus Request Level Selection

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2.9 K8 - BUS GRANT DAISY CHAIN

The BGxin and BGxout lines that correspond to the bus request level of the MZ 8115 are wirewrapped to pins 1 and 2 respectively on jumper block K8. This allows the MZ 8115's onboard arbiter to decide whether or not the MZ 8115 is responsible for bus requests at that level. All other bus levels are jumpered from their respective BGxIN pin to their BGxOUT pin.

Note: The bus grant level wirewrapped to the MZ 8115's bus grant in and out pins here must correspond to the bus request level selected with K7.

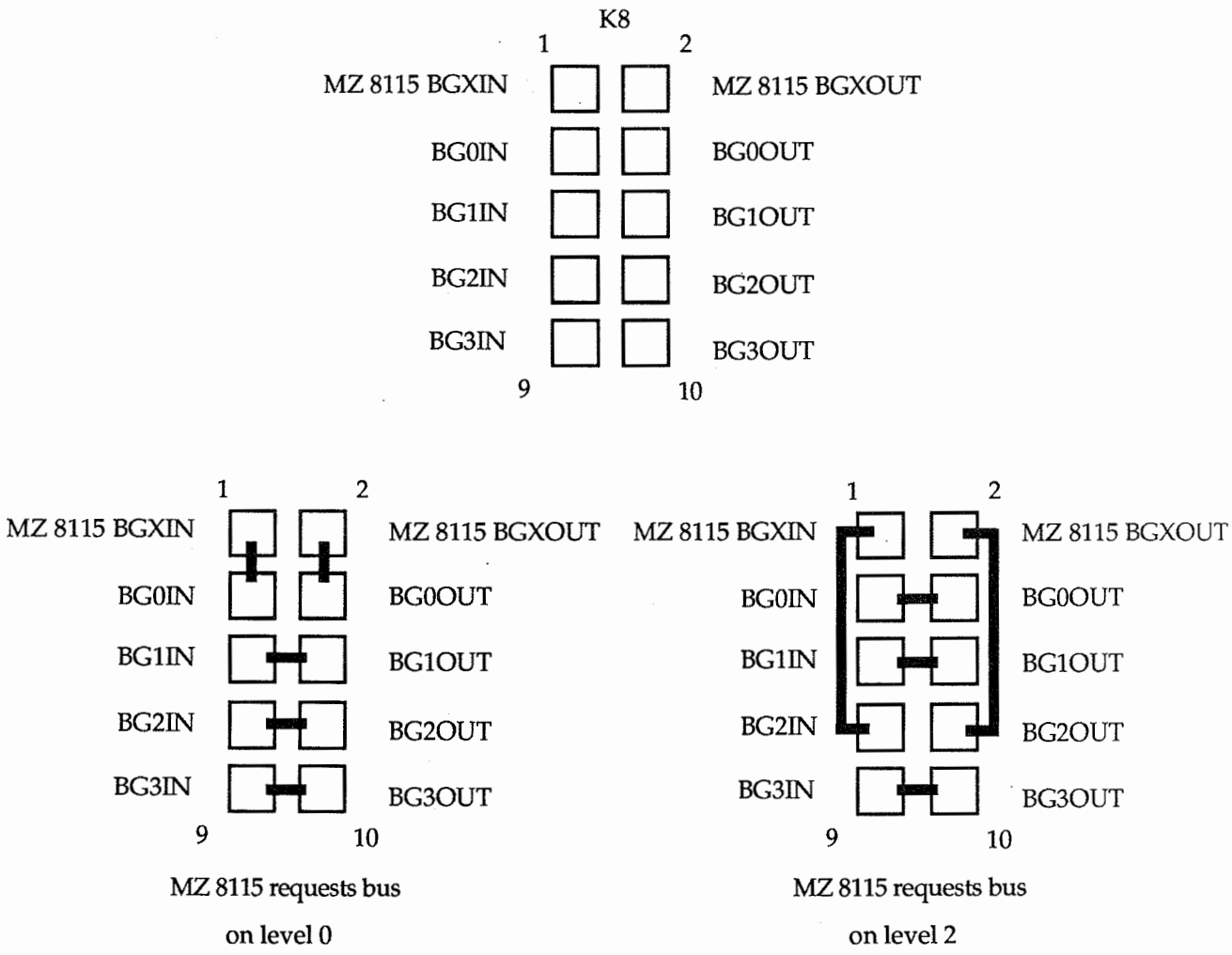


Figure 2.8 Bus Grant Daisy Chain

2.10 K9 - BUS CLEAR /TIRQ ENABLE

As of Revision A, the MZ 8115 has the ability to respond to BCLR when the system controller signals that another processor of higher priority is waiting to take control of the VMEbus. When enabled, BCLR is treated by the MZ 8115 as a level 5 autovectored interrupt. BCLR is usually enabled when the MZ 8115 is used in a programmed release mode. In this mode, the MZ 8115 is configured through software to keep the bus until its ready to give it up. When a BCLR interrupt occurs, the MZ 8115 will be programmed to release the bus.

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The BCLR interrupt line is shared with the 68681's secondary timer interrupt signal, TIRQ. K9 allows user selection of either BCLR or TIRQ to cause a level 5 autovectored interrupt. To enable the MZ 8115 to respond to BCLR as a level 5 autovectored interrupt, place a jumper between pins 1 and 2 of jumper block K9. To enable the MZ 8115 to respond to TIRQ as a level 5 autovectored interrupt, place a jumper between pins 2 and 3 of jumper block K9.

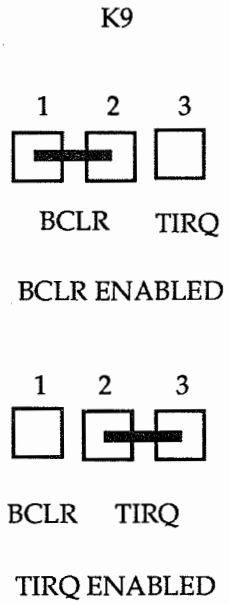


Figure 2.9 BCLR /TIRQ Enable

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CHAPTER 3

THEORY OF OPERATION

3.1 INTRODUCTION

This section offers a more detailed explanation on how the MZ 8115 operates than that found in the functional description. In addition to describing the main functional blocks, details of the underlying logic of each block is provided. The user is advised to refer to the schematic during the following discussion.

3.2 CPU MODULE

The MZ 8115 operates with a 10 or 12.5 MHz, 68000 or 68010 microprocessor. The board is intended for use as a VMEbus master with an onboard interrupt handler and an onboard bus arbiter to request and release control of the VMEbus. In addition, the MZ 8115 can also be treated as a slave module allowing its dual-ported RAM to be accessed from other masters on the VMEbus.

3.2.1 Address Decoding

Onboard address lines are decoded by two PAL's, U18 and U19. The dual-ported RAM is addressed from $0000 to $07FFFF, from the onboard processor. ROM is addressed from $F80000 to $F9FFFF. Note that upon resetting the system, the MZ 8115 is hardware configured so that the first eight bytes of ROM are loaded into the CPU as the initial stack pointer and program counter. The onboard serial chip, the 68681, is selected with addresses from $FE8000 to $FEFFFF. The locations at $FE801D and $FE801F are specifically used for programmed bus release disable and enable respectively.

U10 decodes the dual-ported RAM for VMEbus accesses in the address range $E80000 to $EFFFFF. This off-board access address is PAL selectable.

All other addresses generated on the CPU's 24-bit address lines select off-board locations, thus generate address modifier codes and require the MZ 8115 to take control of the VMEbus before data transfer can take place. The off-board accesses are either standard VMEbus addresses from $080000 to $EFFFFF, or short I/O addresses from $FF0000 to $FFFFFF. Short I/O addresses are 16-bit addresses that are used by I/O boards reducing the amount of address decoding circuitry they require. The user adds $FF0000 to the 16-bit address to access these boards. The standard VMEbus addresses generate address modifier codes 39, 3A, 3D or 3E, and the short I/O addresses generate address modifier codes 29 or 2D.

3.2.2 Interrupt Handler

The MZ 8115 can respond to any of the seven VMEbus interrupt request levels as well as onboard interrupts and two dedicated local interrupts coming from the S1 connector (S1IRQ1, S1IRQ2). The onboard interrupts are prioritized as follows:

ABORT	level 7
S1 interrupt 1	level 6
BCLR interrupt	level 5
S1 interrupt 2	level 4
68681 serial interrupt	level 3

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Several of these interrupts have been configured as autovectored interrupts which do not require a user vector to be sent to the processor via the data bus. The interrupt level itself points to the proper jump location in the exception table. These interrupts are: ABORT, BCLR interrupt and the two S1 interrupts.

Off-board interrupts require the MZ 8115 to gain control of the VMEbus before they can be acknowledged. Note that although the MZ 8115 and other masters are capable of responding to all of the VMEbus interrupt request levels. One and Only one master is allowed to respond to a specific level. In other words, no two masters may be configured to respond to the same interrupt level.

3.2.3 Onboard Bus Arbiter

The onboard bus arbiter, U16, controls when the MZ 8115 will drive the VMEbus. When the MZ 8115 requires the bus, either during an off-board address access or interrupt acknowledge cycle, it requests the bus from the system controller on one of four bus request levels. The bus request level is selected with jumper block K7 on the MZ 8115. The system controller grants permission for the master to control the bus by driving a bus grant line low for the level requested. The onboard arbiter decides whether or not the MZ 8115 was the master requesting the bus and if so, it takes control of the bus by driving BBSY (Bus Busy) active. The onboard arbiter then drives BAV (Bus Available) low, which enables the buffer/drivers that transmits the address lines, data lines and control signals onto the VMEbus.

The MZ 8115 can be configured to release the VMEbus on a 'release on request' or a 'Programmed Release ' basis. This applies whether the system controller is configured for round robin or fixed priority.In Release and Request mode the MZ 8115's onboard arbiter maintains control of the VMEbus until it receives a bus request from another master. The MZ 8115 gives up the bus at the completion of it's current cycle when AS (Address Strobe) is driven high by deactivating BBSY which disables BAV. If the MZ 8115 was programmed to disable the release mechanism, the MZ 8115 will continue to keep control of the bus. This will continue until the bus release mechanism is again enabled. Note that unless the MZ 8115 is programmed otherwise, the default condition is that it will release the bus upon request. Refer to Chapter 4 for specific programming details.

3.3 SYSTEM CONTROLLER

The MZ 8115 has an onboard system controller chip which, when enabled, allows this board to reside in slot 1 as the VMEbus system controller. *NOTE: There can only be one system controller on the VMEbus and it must be in slot 1.* If the MZ 8115 is not being used as the system controller, this chip must be disabled.

As system controller, the MZ 8115 monitors all bus request levels and arbitrates the new bus master by either round robin or priority mode. *NOTE: Even though the MZ 8115 may be enabled as the system controller, the MZ 8115 gains control of the bus only after sending a bus request signal onto the VMEbus and waiting for the resulting bus grant.* Since the MZ 8115 as system controller will reside in slot 1, it will have top priority for a given bus grant level.

3.4 DUAL-PORTED RAM

The MZ 8115 contains 512k of dual-ported dynamic RAM with no wait states at 12.5 MHz. The 512k of RAM is arranged as 256k of 16-bit words. The RAM is addressed from $0000 to $07FFFF through PAL U19 for onboard access and from $E80000 TO $EFFFFF through U10 for VMEbus access. This addressing range can be easily reconfigured if required by modifying the PAL equations.

There are three different RAM cycles that take place: RAM access from the onboard CPU, RAM access from an external processor on the VMEbus and a refresh cycle. No two cycles can exist at the same time.

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If an onboard RAM cycle is in progress, VMECLR will go low which through, flip-flop U36b, prevents any VMERQ (VMEbus request) signals from passing through to VMEGR (VMEbus grant). This prevents VAEN from going low disabling transceivers U25, U26, U29 and U30 cutting off the MZ 8115 from the VMEbus. Thus, a VMEbus access is prevented during an onboard RAM access.

Likewise, if a refresh cycle comes up (which occurs about every 10 usec) during a RAM cycle or a VMEbus access cycle, REFCLR will be low until these cycles are completed, disabling the REFGR signal in U37b from triggering the start of the refresh cycle. Note that U37a latches the refresh signal until after the refresh cycle has been completed. Thus when the RAM cycle (onboard or from the VMEbus) has been completed, the refresh cycle will proceed on.

And finally, the onboard RAM signal is not allowed to go low until neither VMEGR nor REFGR is active.

3.5 EPROM

The two EPROM sockets are configured to accept JEDEC pinouts for 2764, 27128, 27256 and 27512 EPROMs Thus, a total of 128k of EPROM may be accessed if using 27512 EPROMs. This memory is configured as 16-bit words, thus the 27512's will actually be configured as 64k of 16-bit words. The EPROM is addressed from $F80000 to $F9FFFF through PAL U18.

NOTE: The upper socket houses the low byte EPROM, and that the lower socket houses the high byte EPROM. (The VMEbus 96 pin connector is assumed to be at the bottom of the board). EPROM access times of 170 nsec for 12.5 MHz CPU's, and 200 nsec for 10 MHz CPU's are recommended.

3.6 SERIAL PORTS

Two onboard serial ports are provided by a 68681 dual asynchronous communication chip. The 68681 is provided with a 3.6864 MHz crystal which allows a variety of 18 standard asynchronous baud rates ranging from 50 to 38.4k. Also, a user defined baud rate can be established by using the internal 16-bit timer to generate that rate.

The 68681 is configured to generate an onboard serial interrupt at level 3. The interrupt vector must be programmed into the chip for the vectored interrupt function to work properly. See the 68681 users manual and Section 4.4 of this manual for further programming information.

The two serial ports provide TXData, RXData, RTS, CTS, Frame Ground, and Signal Ground on two RJ11 connectors labeled M1 and M2. The accompanying diagram provides the pinouts of these connectors.

RJ11 Pinouts

The pinout for the RJ11 modular serial port connectors are as follows:

Pin	Signal
1	CTS
2	RXD
3	FRAME GROUND
4	SIGNAL GROUND
5	TXD
6	RTS

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Pin 1 of the RJ11 connectors is on the left side on each connector when the MZ 8115 is vied from the component side of the board with the P1 connector at the bottom.

This pin numbering scheme applies only to boards equipped with the RJ11 modular connectors, in place of the standard 26-pin DIN connectors.

3.7 RAM PARITY CHECKING

The data lines that are read from or written to RAM are monitored by the two F280 parity generators U45 and U46. These F280's drive their outputs, LPDI and HPDI, high if the data lines contain an even number of high bits or low for an odd number of high bits.

During write cycles, these parity bits, LPDI and HPDI, are stored in RAM chips A9 and B9. During read cycles, these stored parity bits are read onto lines LPDO and HPDO while the F280's generate a new set of LPDI and HPDI based on the data lines read. If the parity check mode is enabled (by placing a jumper on jumper block K1), PAL U7 will generate a BERR if the parity bits SPDI and LPDO or HPDI and HPDO don't match. If the parity bits do match, DTACK will be generated as usual.

Note: The parity checking will only drive BERR on read cycles and is an indication that there is an error in the data that was stored.

3.8 S1 CONNECTOR

The 96-pin DIN connector, S1, located along the side of the MZ 8115 allows for custom expansion of the CPU board. The accompanying figure displays the signals available. As seen, all of the 68010's address and data lines, as well as all of the asynchronous control signals, are passed through to the S1 connector.

3.8.1 S1 Address Decoding

The MZ 8115 does not specify what addresses select the S1 connector. It is up to the designer of S1 interfaced boards to specify the addresses that will access that board. Two blocks of memory are left open in the MZ 8115s memory map that can be used for the S1 side board. These are the address ranges $F00000-$F7FFFF and $FA0000-$FE7FFF. Either of these two blocks can be used to select the S1 connector.

3.8.2 S1 Interrupts

Two interrupt methods are available for the expanded S1 board. The S1 board can either interrupt the MZ 8115's CPU as an onboard interrupter via signals S1IRQ1 and S1IRQ2, or it can interrupt an off-board master on any two of the VMEbus interrupt request levels IRQ1 to IRQ7, via signals BIRQ1 and BIRQ2. *NOTE: The BIRQ1 and BIRQ2 are not to be used to interrupt the MZ 8115, but off-board masters only.*

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Onboard S1 Interrupts (SIRQ1 and SIRQ2)

If onboard interrupts are used, either S1IRQ1 or S1IRQ2 should be driven low. These interrupts are treated as vectored interrupts and thus require an interrupt vector to be passed to the CPU.

Vectored interrupts are handled be the interruption device responding with a vectored address (the first address of the interrupt handling routine) to the exception routine. S1IRQ1 is a level 6 interrupt and S1IRQ2 is a level 4 interrupt.

NOTE: These interrupts do not involve the VMEbus. Thus in this case, the IACKIN/IACKOUT daisy chain is not required. Also note that for autovectored interrupts, the designer is responsible for assuring that the interrupt request gets reset after being acknowledged.

MZ 8115 NASA/MZ8115 Standard S1 Interrupt Variances

The PAL controlling these interrupts is equal to 270603 with S1IRQ1 and S1IRQ2 deleted from VPA equation. S1IRQ1 is irq from DMAC (HD63450); S1IRQ2 is irq from MPCC (68651). This permits using the vector generation capability built into those devices. The interrupt levels have not been changed.

Off-board Interrupts (BIRQ1 and BIRQ2)

If off-board interrupts are used, BIRQ1 or BIRQ2 should be driven low. These signals must be jumpered to the interrupt level desired with jumper block K3 as explained in the jumper configuration section of this manual. *NOTE: These signals do involve the VMEbus and require the IACKIN/IACKOUT daisy chain to be passed through to the S1 connector.*

These interrupts require an interrupt vector to be passed to the bus master being interrupted. The required interrupt vector is to be stored in one of the following eight locations located at the top of RAM:

Interrupt Level	Vector Location
1	$7FFF3
2	$7FFF5
3	$7FFF7
4	$7FFF9
5	$7FFFB
6	$7FFFD
7	$7FFFF

During the interrupt cycle, the S1 board waits for both BIACK and IACKIN to be asserted. When this occurs, the address lines BA1-BA3 are checked to see if they encode the interrupt request level selected with jumper block K3. For example, if request level 4 was selected, address lines BA1-BA3 will be encoded as LLH, with BA3 being the most significant bit. If the correct interrupt level appears on these address lines, the S1 board is to assert LIACK. This begins a memory cycle which uses BA1-BA3 to fetch the interrupt vector out of RAM and place it onto the VMEbus, and concludes the interrupt cycle by asserting DTACK low.

During an interrupt cycle, all address lines, with the exception of A1-A3, are pulled high with resistor network RN6. Thus, during the LIACK forced memory cycle, the interrupt vector is retrieved from the top of RAM at the address pointed to by the interrupt level encoded on A1-A3, with all other address lines high.

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The interrupt vector is written to RAM at the address designated for the desired interrupt level (see above chart). The S1 board asserts either BIRQ1 or BIRQ2. And upon verification that the S1 generated interrupt has been acknowledged by the interrupted master, the S1 board asserts LIACK.

3.8.3 S1 Extended Address Generation

Although the MZ 8115 has provisions for handling only 24 address lines with its 68000/68010 processors, provisions have been provided for the S1 side board to be designed with full 32-bit address line capabilities. To accomplish this, if addresses with greater length than 24 bits are generated, the S1 board must drive LONG low. This signal, located at A32 of the S1 connector, prevents the MZ 8115 from trying to decode the lower 24-bits as valid access to it's memory locations. In addition, the S1 board must also drive AM5 low for extended addresses.

The S1 board can be designed with a P2 connector that will plug into the P2 backplane on the VMEbus. This provides a means for the S1 board to pass upper address and data lines as well as user defined lines to the VMEbus.

3.8.4 S1 DMA Configuration

The S1 board can be designed for DMA control of the MZ 8115 by use of the microprocessor bus request and grant lines that are passed to the S1 connector. To hold up the processor while the S1 board takes control of the MZ 8115s data and address bus, the BR line is asserted. The CPU will respond with BG indicating that the side board can proceed to use its buses. The S1 board acknowledges this with BGACK. In addition, the S1 board can drive the three function codes FCO-FC2. Refer to a DMA user's manual for more specific information on how to set up the S1 board as a DMA controller with the signal lines provided on the S1 connector. *NOTE: Problems have been reported with using VLSI DMA chips at clock speeds other than the CPUCLK. This is due to the synchronization of the refresh arbitration with the CPUCLK.*

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Pin Number	Row A	Row B	Row C
1	A11	A10	BERR*
2	A16	A14	Vcc
3	A12	A13	SYSCLK
4	A15	A17	HALT*
5	A19	A18	CPUCLK
6	A7	A20	BR*
7	A9	A1	BGACK*
8	A8	A3	DTACK*
9	A4	A2	AS*
10	A21	A23	A5
11	A22	A6	GND
12	-12V	BG*	D0
13	D1	D2	D10
14	D3	D4	D9
15	RESET*	D5	GND
16	+12V	D6	D7
17	FC1	FC2	FC0
18	----	D8	GND
19	R/W*	LDS*	----
20	VMA*	UDS*	GND
21	E	Vcc	D15
22	----	D12	GND
23	D14	D11	D13
24	IPL2	BAV*	----
25	IPL0	BIRQ2*	BIRQ1*
26	Vcc	VDS0*	AM5
27	IPL1	VDS1*	BAS*
28	LIACK*	BIACK*	GND
29	BA1	LWORD*	GND
30	BA2	IACKOUT	S1IRQ2*
31	BA3	IACKIN	S1IRQ1*
32	LONG*	----	VPA*

---- Reserved for future use

MZ 8115 S1 Connector Pin Assignments

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CHAPTER 4

PROGRAMMING GUIDE

4.1 INTRODUCTION

This section offers a brief overview of some of the programming concerns of the MZ 8115. The topics covered include ROM/RAM mapping considerations, use of the ABORT switch in programming, programming the MZ 8115's bus release mechanism and basic 68681 programming. See Appendix A for programming examples.

4.2 ROM AND RAM MEMORY MAPPING CONSIDERATIONS

As noted earlier in this manual, the MZ 8115 maps ROM at $F80000 and RAM at $0000. Upon booting the MZ 8115, the CPU is hardware configured to read the first eight bytes of ROM as the initial stack pointer and program counter. Thus, the initial stack pointer should be placed at $F80000 and the initial program counter at $F80004.

The 68000/10 exception vector table resides in RAM on the MZ 8115 from $0008 to $400. The targeted jump address for each exception should be written into the vector table from ROM immediately after booting. With the vector table residing in RAM, each exception address can be easily changed from within the user's programs.

4.3 ABORT SWITCH

The ABORT switch on the front panel of the MZ 8115 generates a level 7 autovectored interrupt. The address of the ABORT handling routine should be written to offset $07C in the vector exception table in RAM. Pressing the ABORT switch will stop current program execution and cause the CPU to jump to the address loaded and begin executing the handling routine.

4.4 68681 PROGRAMMING

The 68681 consists of two serial ports, A and B, which are programmed by writing control words to the appropriate registers. The base address for the 68681 is $FE8000. The MZ 8115 will access the 68681 on low (odd) byte addresses only. This is consistent with the VMEbus specification for the short I/O space. The following lists the offset addresses for all of the 68681 registers. The offset addresses added to the base address gives the actual register location.

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OFFSET	Read	Write
$1	Mode Register A (MR1A,MR2A)	Mode Register A (MR1A, MR2A)
3	Status Register A	Clock-Select Register
5	—	Command Register A
7	Receiver Buffer A	Transmitter Buffer A
9	Input Port Change Register	Auxiliary Control Register
B	Interrupt Status Register	Interrupt Mask Register
D	Counter Mode: MSB	Counter/Timer Upper Register
F	Counter Mode: LSB	Counter/Timer Lower Register
11	Mode Register B (MR1B,MR2B)	Mode Register B (MR1B,MR2B)
13	Status Register B	Clock-Select Register B
15	—	Command Register B
17	Receiver Buffer B	Transmitter Buffer B
19	Interrupt-Vector Register	Interrupt-Vector Register
1B	Input Port	Output Port Configuration Reg.
1D	Start-Counter Command	OPR Bit Set Command
1F	Stop-Counter Command	OPR Bit Reset Command

4.4.1 68681 Register Offset Addresses

Programming the 68681 for normal operation consists of three phases: initialization, writing and reading. A brief discussion of these phases is presented in the following sections. A section on 68681 interrupts is also presented and programming examples are shown in Appendix A.

4.4.2 68681 Initialization

For normal transmit/receive operation, the mode registers (MR1A,MR2A), the clock select register (CSRA), the Command Register (CRA), and the Interrupt Mask Register (IMR) must be properly initialized. These registers configure the serial port for data length, parity and baud rate as well as enabling the proper operation mode.

For example, to configure port A for 8-bits, no parity and 9600 baud, the following control codes should be written to the appropriate register:

1. $13 to MR1A - sets no parity and 8-bit data length
2. $07 to MR2A - sets 1 stop bit length
3. $bb to CSRA - 9600 baud
4. $05 to CRA - enables Transmitter and Receiver
5. $00 to IMR - masks all interrupts

Note that MR1A and MR2A have the same address. An internal pointer in the 68681 points to MR1A after RESET* or after a $10 is written to CRA. The pointer points to MR2A after MR1A is accessed. Accessing MR2A does not change pointer position. From the above initialization values, no control lines, such as CTS or RTS, have been enabled. Refer to the 68681 user's manual for these set up values.

4.4.3 Transmitting Data

To transmit a character through the serial port, the user tests bit #2 of the status register (SRA) until the 68681 indicates that it is ready for transmission. After this bit is set, the user can then move the character to be transmitted into the transmitter buffer (TBA) where the 68681 sends it out to the serial port.

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4.4.4 Receiving Data

To receive a character from the serial port, the user tests bit #0 of the status register until the 68681 indicates that the data it received is valid. When this bit is set, the character can then be read from the receiver buffer (RBA).

4.4.5 Interrupt Operation

The MZ 8115 is configured to receive two interrupts from the 68681, SIRQ and TIRQ. The intended purpose for these interrupts is to provide counter/timer based interrupts as well as serial port receive and transmit interrupts.

SIRQ generates a level 3 interrupt, and requires an interrupt vector to be loaded into the 68681's interrupt vector register. Recall that the 68000/10 multiplies interrupt vectors by four before retrieving the appropriate jump address out of the vector table. For example, to retrieve the user vector 1's jump location positioned at $100 in the vector table, $40 should be loaded into the 68681's interrupt vector register.

To use SIRQ as a counter interrupt the following procedure is used:

1. Load the interrupt vector into the 68681.
2. Write the interrupt handling address to the vector table.
3. Set up the interrupt mask register (write $08 to IMR)
4. Select the counter clock source (write $90 to ACR).
5. Initialize upper and lower counter registers to beginning count.
6. Begin counter by reading Start-Counter command register.

TIRQ is configured to generate a level 5 autovectored interrupt. Thus, an interrupt vector is not required since the interrupt level itself points to the correct position in the exception vector table.

TIRQ is OP3 of the 68681 configured for counter/timer output. To use TIRQ as a counter interrupt the following procedure is used:

1. Load interrupt handling routine address at auto-vector level 5 in the vector table.
2. Set ACR and upper and lower counter registers as above.
3. Mask off all interrupts (since we're not using SIRQ).
4. Set OP3 for counter interrupt (write $04 to OPCR).
5. Begin counter by reading Start-Counter command register.

4.5 PROGRAMMED BUS RELEASE OPERATION

The MZ 8115 can be programmed to disable the bus release mechanism, allowing it to maintain control of the bus regardless or other VMEbus masters bus requests. Once the bus release mechanism has been disabled, bus release can only be accomplished by programming the MZ 8115 to enable the bus release mechanism. Note that when configuring the MZ 8115 in this 'programmed release' mode, the MZ 8115 should be operated with BCLR enabled, so that the MZ 8115 can be notified that a higher priority bus request is pending. BCLR, when enabled with jumper block K9, generates a level 5 autovectored interrupt. Also note that both BCLR and TIRQ cannot both be enabled at the same time.

The 68681 DUART is utilized to enable or disable the bus release mechanism via its programmable OP2 pin. To maintain control of the bus, the OP2 pin can be programmed low to disable the bus release feature by executing the following instruction where $1D is the offset for the OPR set register of the 68681:

```
move.b  #4,$FE801D    * Disable Bus release mechanism
```


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To enable the bus release mechanism, again allowing the MZ 8115 to release the bus, the OP2 pin can be programmed high by executing the following instruction, where $1F is the offset for the OPR reset register of the 68681. Note that $FE8000 is the 68681 base address:

```
move.b #4,$FE801F    * Enable Bus release mechanism
```


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APPENDIX A

```
* 68681 Programming Examples
*
* The following subroutines correspond to the programming discussion found in Section 4.4 of
* this manual.
*
*                    68681 Register Addresses:
*
              spbase:     = $fe000000          *  68681 base address
              modea:      = $01                *  mr1a, mr2a registers
              sra:        = $03                *  status register a
              csra        = $03                *  command register a
              cra:        = $05                *  command register a
              bufa:       = $27                *  rba, tba registers
              acr:        = $09                *  auxilliary control register
              imr:        = $0b                *  interrupt mask register offset
              isr:        = $0b                *  interrupt status register
              ctur:       = $0d                *  counter/timer upper register
              ctlr:       = $0f                *  counter timer lower register
              ivr:        = $19                *  interrupt vector register
              opcr        = $1b                *  output port config. register
              start       = $1d                *  start counter command
              stop        = $1f                *  stop counter command

*************************************************************************
* Procedure: pinit
* Action: initialize 68681 port A
* Input: none
* Output: port A set up for 8 bits, no parity and 9600 baud
*************************************************************************
pinit:        move.l      a0,-(sp)             *  push a0 onto stack
              lea         spbase,a0            *  load 68681 base address
              move.b      #$13,modea(a0)       *  sets mr1a for no parity, 8 bits
              move.b      #$07,modea(a0)       *  set mr2a for 1 stop bit
              move.b      #$bb,csra(a0)        *  select 9600 baud
              move.b      #$05,cra(a0)         *  enables transmitter and receiver
              move.b      #$00,imr(a0)         *  mask off all interrupts
              move.l      #$(sp)+,a0           *  pull a0 off of stack
              rts

*************************************************************************
* Procedure: putchr
* Action: transmit a character via the serial port
* Input: d0 contains character to be transmitted
* Output: none
*************************************************************************
putchr:       move.l      a0,-(sp)             *  push a0 onto stack
              lea         spbase,a0            *  load 68681 base address
put 1:        btst        #2,sra(a0)           *  test if 68681 ready to transmit
              beq         put 1                *  if not, repeat testing
              move.b      #$d0,bufa(a0)        *  else, send character
              move.l      #$(sp)+,a0           *  pull a0 off of stack
              rts
```


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```
*************************************************************************
* Procedure: getchr
* Action: Receive a character from the serial port
* Input:  none
* Output:  d0 will contain character received
*************************************************************************
getchr:     move.l      a0,-(sp)          *  push a0 onto stack
            lea         spbase,a0         *  load 68681 base address
get 1:      btst        #0,sra(a0)        *  test if 68681 has received anything
            beq         get 1             *  if not, repeat testing
            move.b      bufa(a0),d0       *  else, get character
            and.l       #$7f,d0           *  mask off upper bit
            move.l      (sp)+,a0          *  pull a0 off of stack
            rts
*************************************************************************
* Procedure: SIRQ interrupt generation
* Action: Initialize counter and generate interrupt on SIRQ.
*         Bit 0 of flag set if interrupt occurred in irq handling routine.
* Input: none
* Output: none
*************************************************************************
sirq:       movem.l     a0/d1,-(sp)       *  push a0 and d1 onto stack
            lea         spbase,a0         *  load 68681 base address
            move.b      #$40,ivr(a0)      *  write interrupt vector to 68681
            move.b      #inthand,$100     *  write jump target to exception table
            move.b      #08,imr(a0)       *  set up interrupt mask register
            move.b      #$90,acr(a0)      *  set auxilliary control register
            move.b      #$7f,ctur(a0)     *  initialize counter to $7fff
            move.b      #$ff,crtlr(a0)
            clr.b       flag

            move        #$2200,sr         *  Enable interrupt level 3 on the cpu
            move.b      start(a0),d1      *  read start register to start counter
count 1:    btst.b      0 flag            *  test if interrupt occurred yet
            beq         count 1           *  if not, repeat testing

            move        #$2700,sr         *  disable interrupts on the cpu
            move.l      #$(sp)+,a0/d0     *  pull a0 and d0 off of stack
            rts

*************************************************************************
* Procedure: interrupt handler
* Action: Sets bit 0 of flag when SIRQ interrupt occurs.
* Input: none
* Output: bit 0 of flag set
*************************************************************************
inthand:    move.b      stop(a0),d1       *  read start stop register to reset irq
            bset.b      #0, flag          *  set flag bit to indicate interrupt occurred
            rte

            .data
            flag:       .ds.b  1          *  flag used for interrupt examples
            rts
```


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APPENDIX B

MZ 8115 NASA Custom Parts List
Artwork Rev. A
Assembly Rev. B

Per Board	Industry Part Number	Description	
5	74F541D	U1,U21,U22,U24,U28	
1	74LS373D	U4	
6	74F245D	U14,U15,U25,U26,U29,U30	
2	74F244D	U23,U27	
1	1488D	U32	
1	1489D	U33	
1	74F164D	U31	
1	74LS393D	U38	
4	74F74D	U35,U36,U37,U52	
1	74F32D	U34	
2	74S38D	U39,U49	
1	74LS174D	U41	
1	74F10D	U40	
3	74F258D	U43,U45,U46	
2	74F280D	U47,U48	
2	74F08D	U44,U50	
2	74F00D	U42,U51	
1	74F243D	U53	
6	PAL16L8B	U2,U3,U7,U8,U16,U19	
1	PAL20R4	U9	
3	PAL20L8A	U6,U10,U18	
18	41256ZIP-10	A1-A9,B1-B9	100 nsec ZIP RAM Pa
1	68681	U5	DUART
Crystals:			
1	3.6864 MHz		
1	16 MHz		
Switches:			
2	TPD-11	SW1,SW2	RESET and Abort sw
LEDs:			
2	555-0506	LED 1,LED 2	90 degree LEDs
Resistors:			
7	43 OHM	R1-R7	43 ohm resistors
1	4308R101-682	RN1	8 pin 6.8k resistor net
1	4310R101-102	RN3	10 pin 1k resistor netv
1	4310R101-682	RN2	10 pin 6.8k resistor ne
2	431oR-A03-390	RN4,RN5	10 pin 39 ohm series n
2	S0MC1601-102G	RN6,RN7	16 pin SMD resistor n

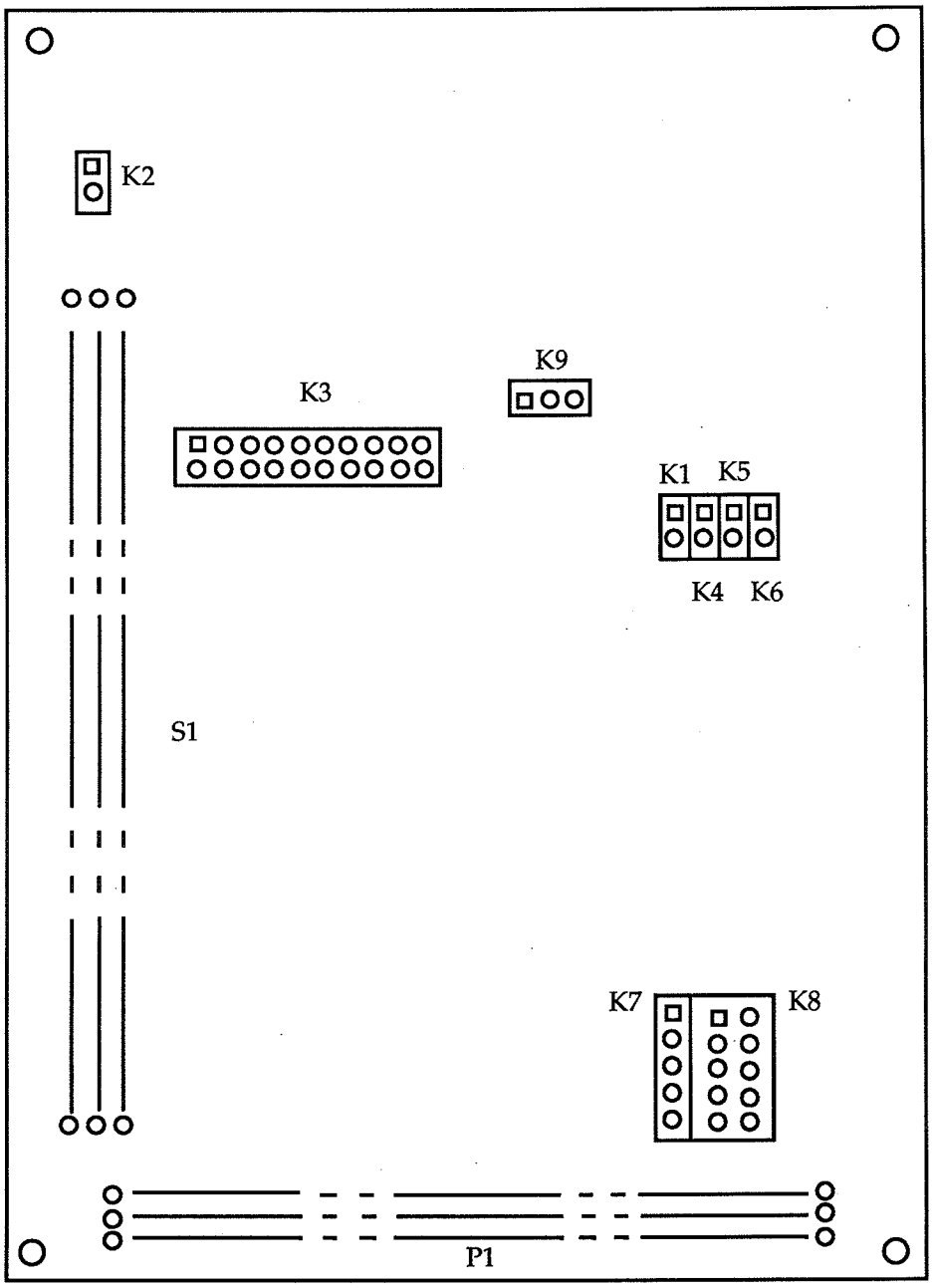
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Sockets:		
1	40021005	20 pin PAL sockets
4	40021007	24 pin sdip PAL sockets
1	40021013	68 pin grid array for 68010
2	40021009	28 pin EPROM sockets
Connectors:		
2	533-602	P1,P3 96 pin VME DIN connectors
2	RJ-11	J1,J2 serial output connectors
Capacitors:		
1		5 pf Disk Capacitors
1		10 pf Disk Capacitors
1		150 pf Tant Capacitor
3		15 uf Tantulum Capacitors
51		surface mount capacitors
Jumper Headers:		
1	1x3	K9
1	2x10	K3
5	1x2	K1,K2,K4,K5,K6
1	1x5	K7
1	2x5	K8

Pal Numbers	Equation Title	Address Range (if applicable)
8115002NASA1A	270204	---
8115006NASA1B	270603 (Modified)	---
8115008NASA1B	270800	---
8115018NASA1A	271800	---
8115003NASA1A	270303	---
8115007NASA1A	270700	---
81150009NASA1A	270902	---
8115016NASA1A	271602	---
8115019NASA1A	271901	---
8115010NASA100B	271000B	E80000-EFFFFF
8115010NASA101B	271001B	E00000-E7FFFF
8115010NASA102B	271002B	D80000-DFFFFF
8115010NASA103B	271003B	D00000-D7FFFF
8115010NASA104B	271004B	C80000-CFFFFF
8115010NASA105B	271005B	C00000-C7FFFF
8115010NASA108B	271028B	080000-0FFFFF

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APPENDIX C



MZ 8115 Module Header Location Diagram

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APPENDIX D

SCHEMATIC

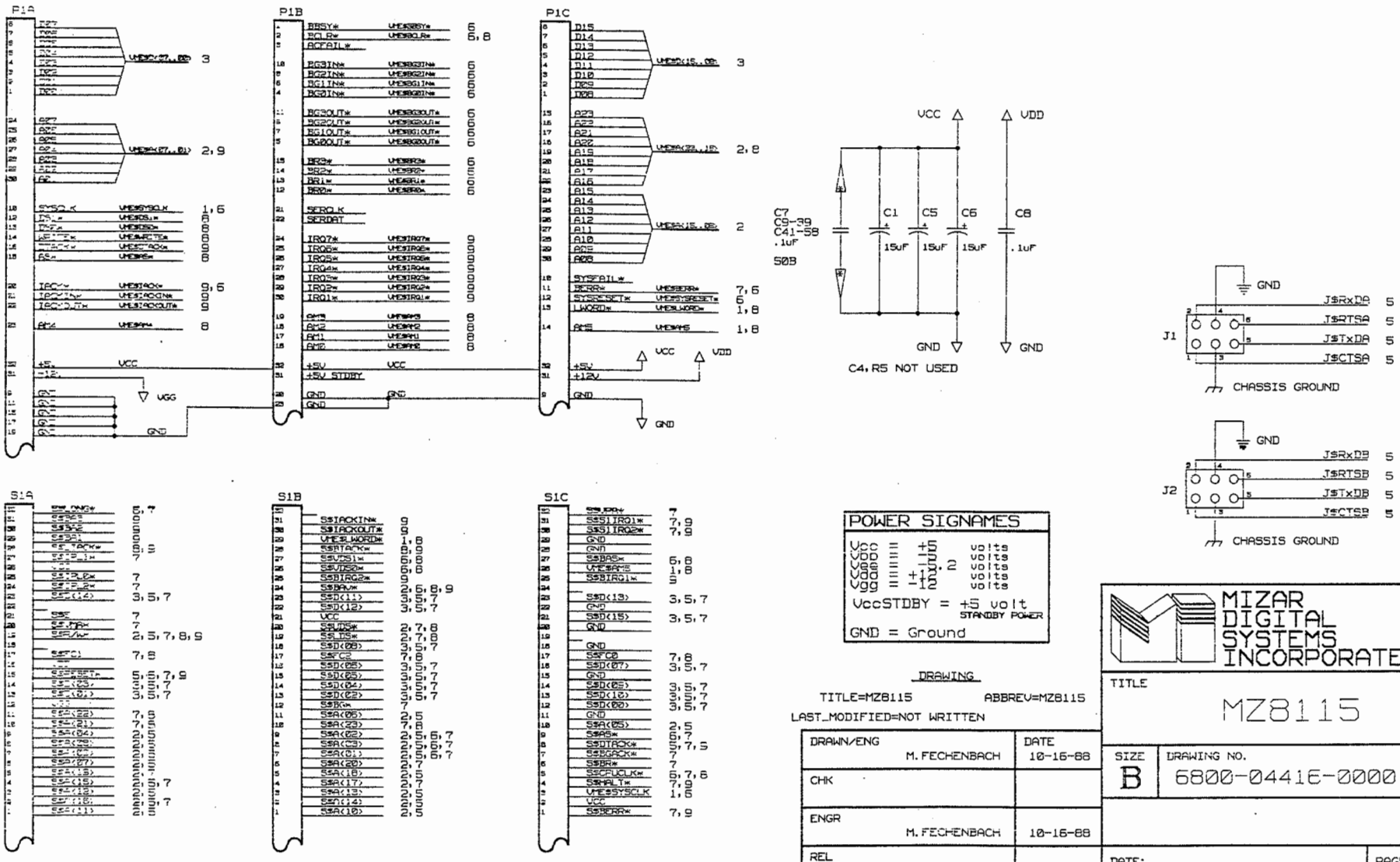
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REVISIONS

LTR	DESCRIPTION	APPD	DATE
A	INITIAL RELEASE XECN	M. FECHENBACH	12-18-87
B	INC CHANGE ECN [illegible]	M. FECHENBACH	~~10-16-88~~



POWER SIGNAMES

Vcc	+5	volts
VDD	+12	volts
Vgg	-12	volts

VccSTDBY = +5 volt (STANDBY POWER)

GND = Ground

DRAWING

TITLE=MZ8115 ABBREV=MZ8115

LAST_MODIFIED=NOT WRITTEN

DRAWN/ENG	M. FECHENBACH	DATE 10-16-88
CHK		
ENGR	M. FECHENBACH	10-16-88
REL		

MIZAR DIGITAL SYSTEMS INCORPORATED

TITLE: MZ8115

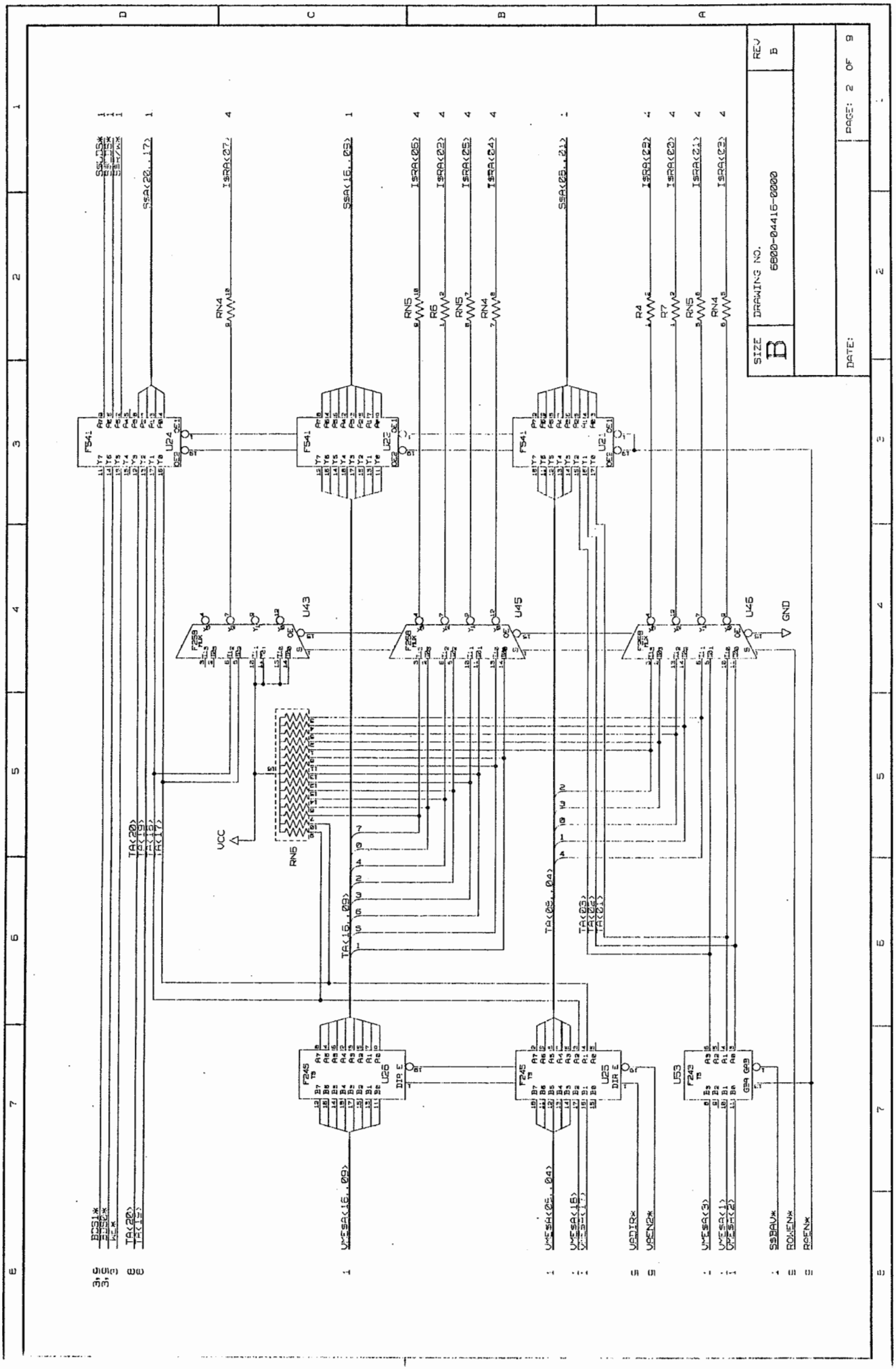
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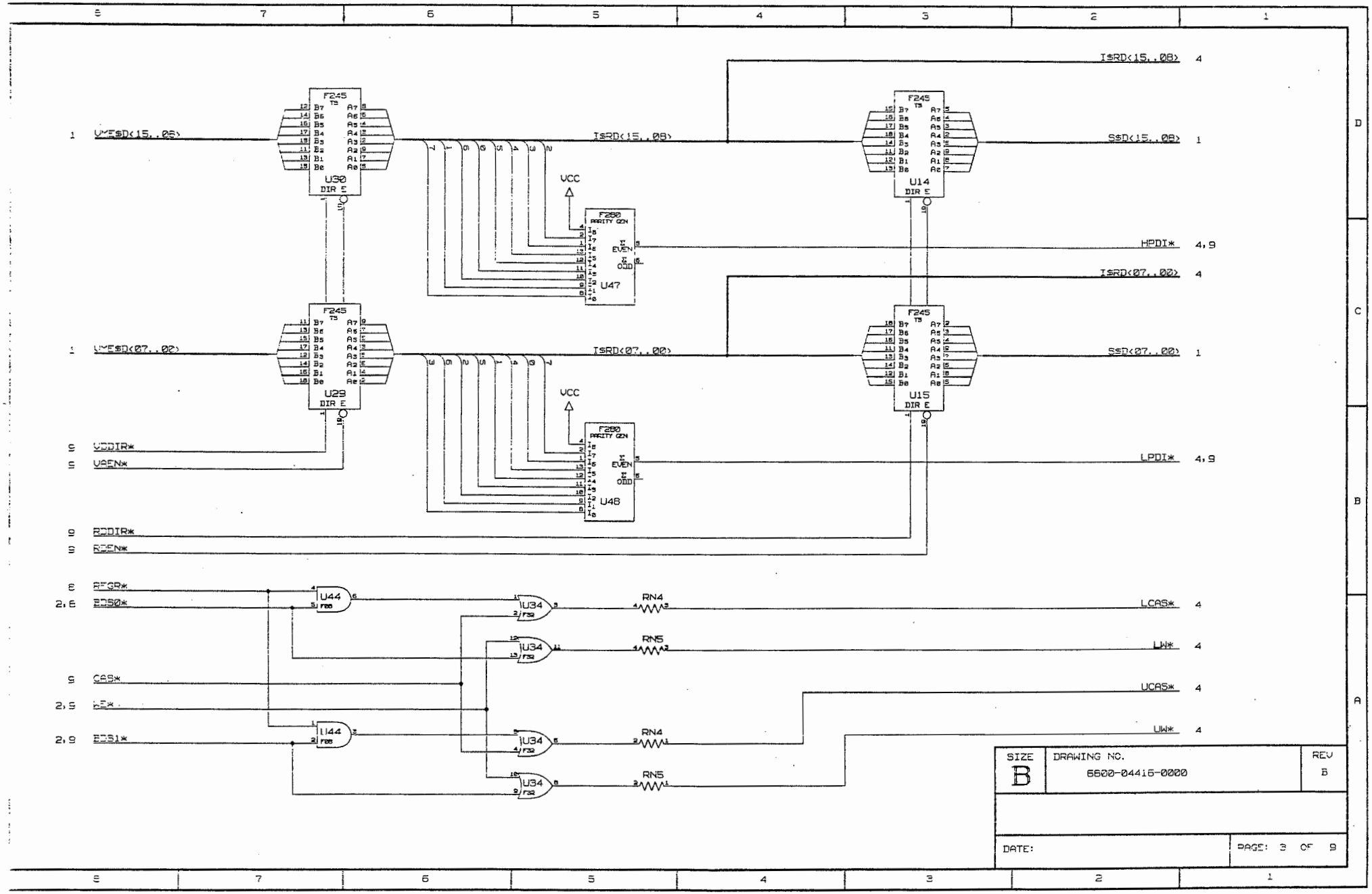
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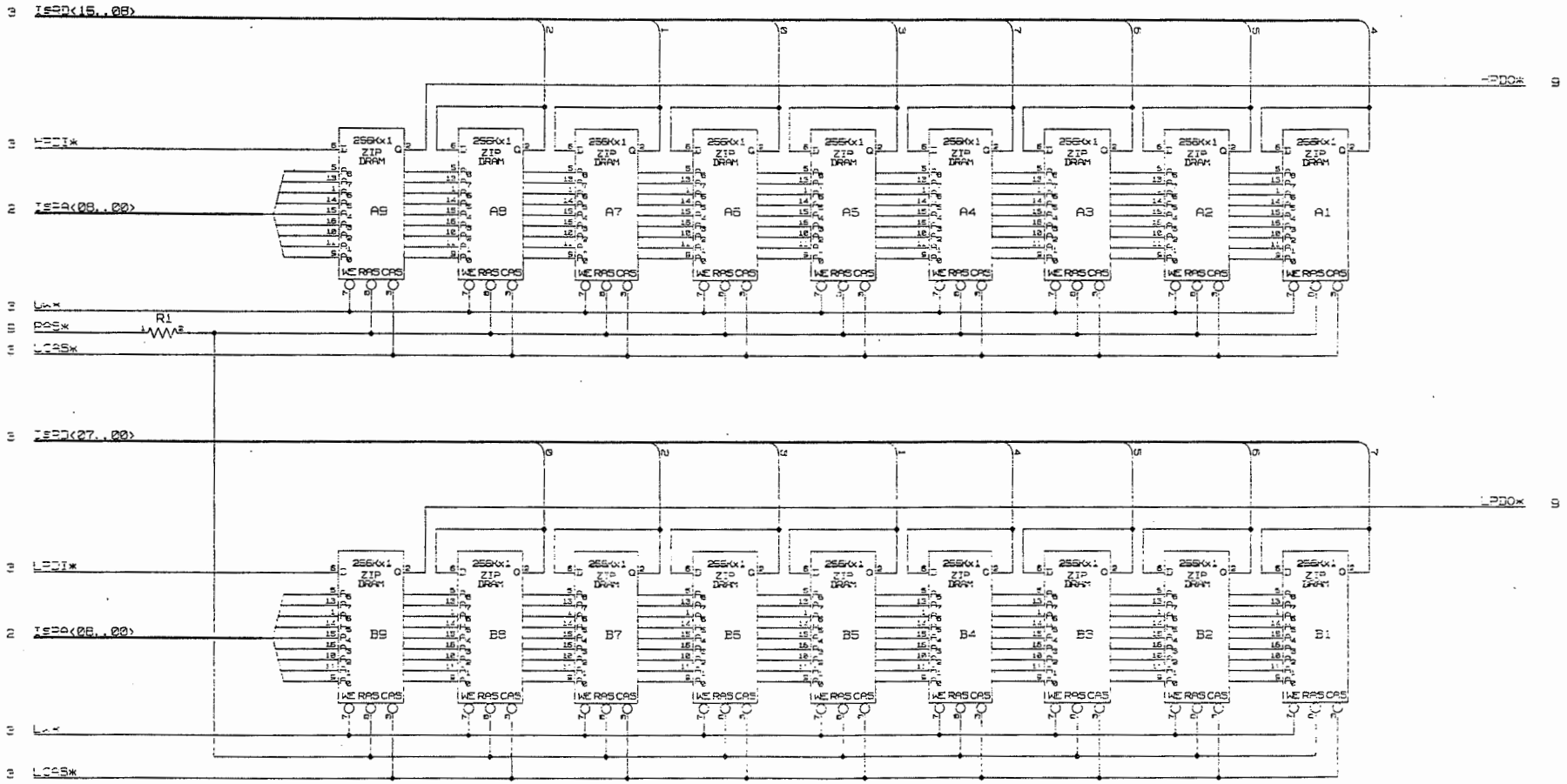
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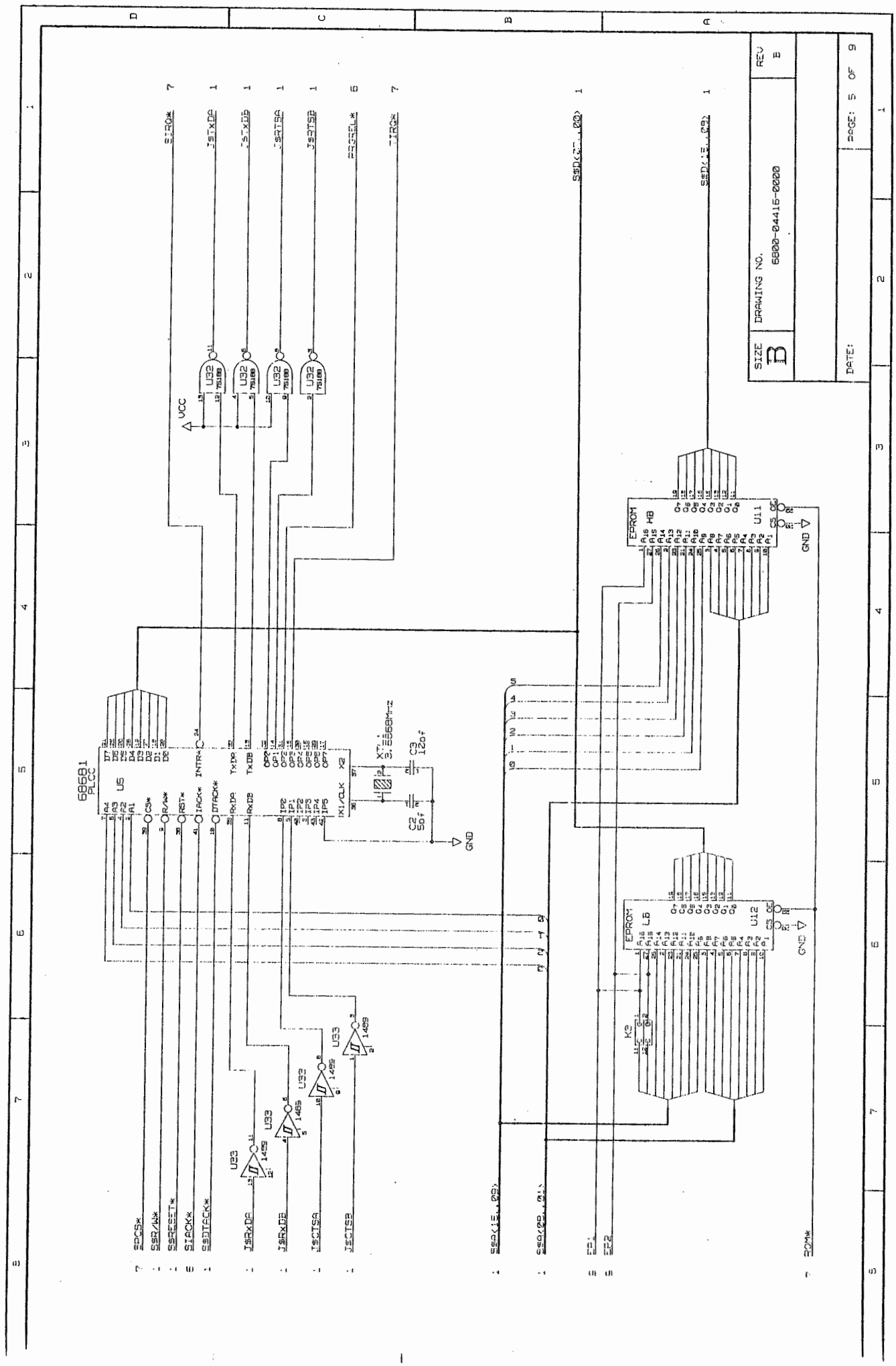
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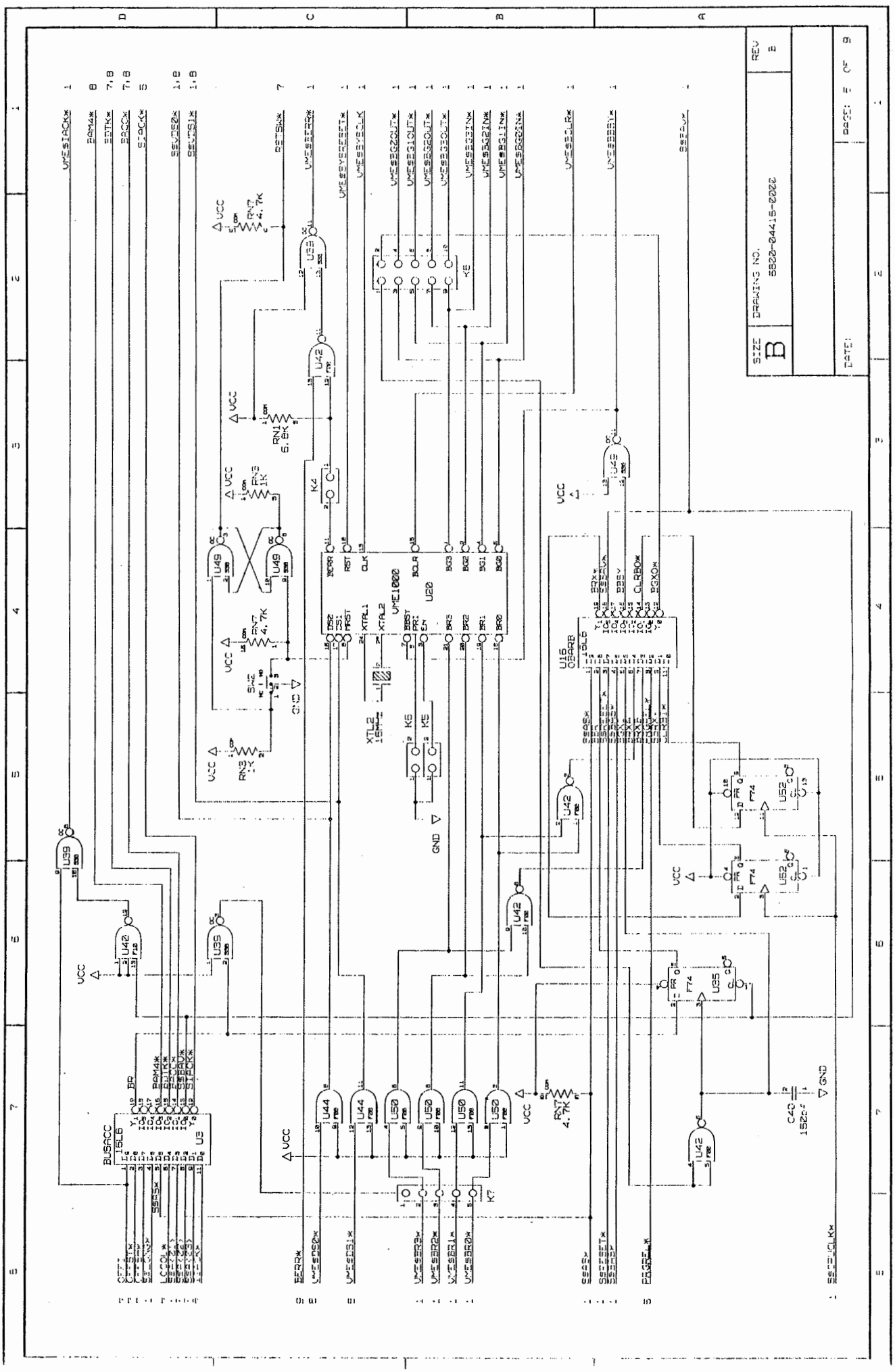
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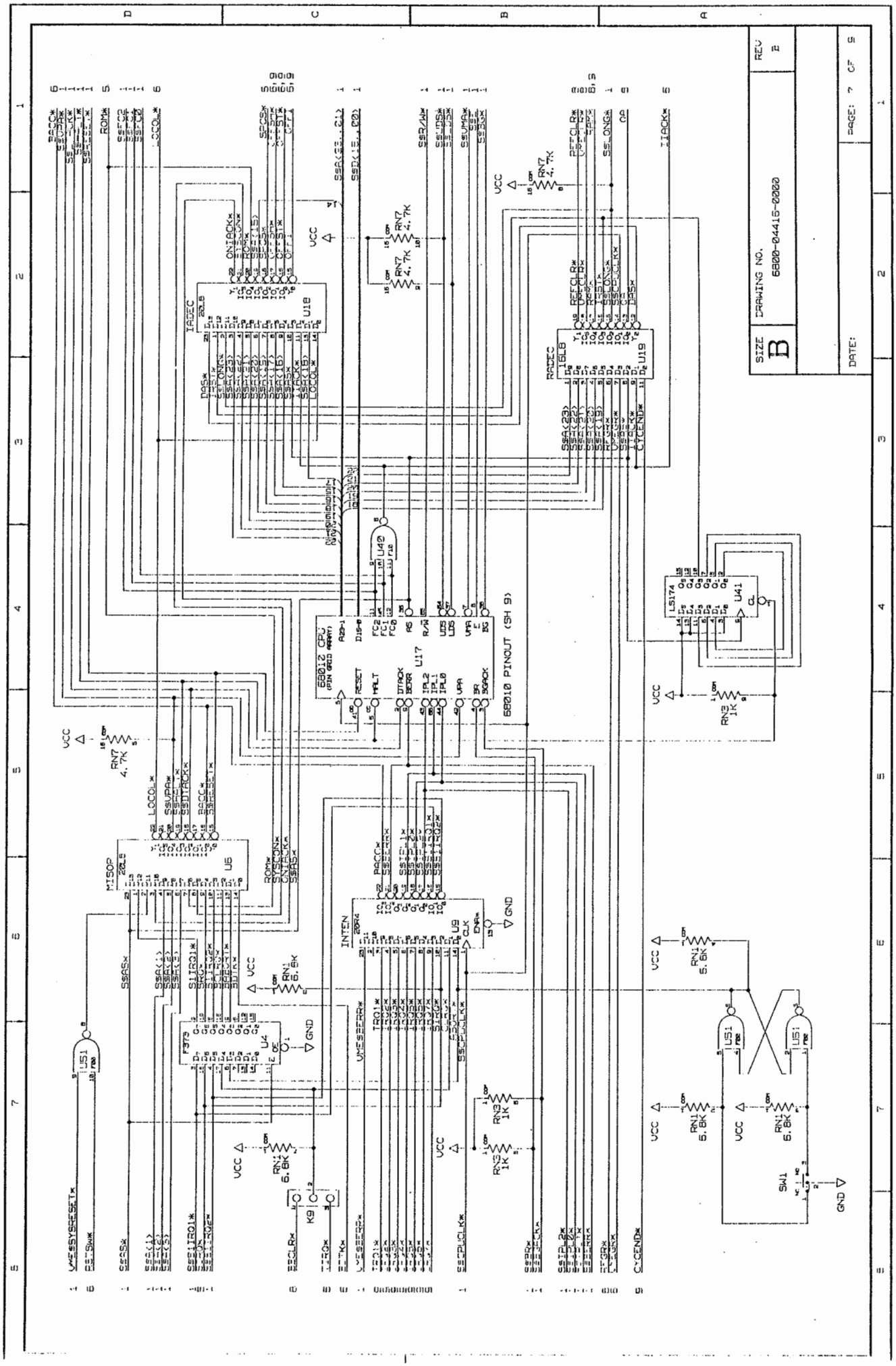
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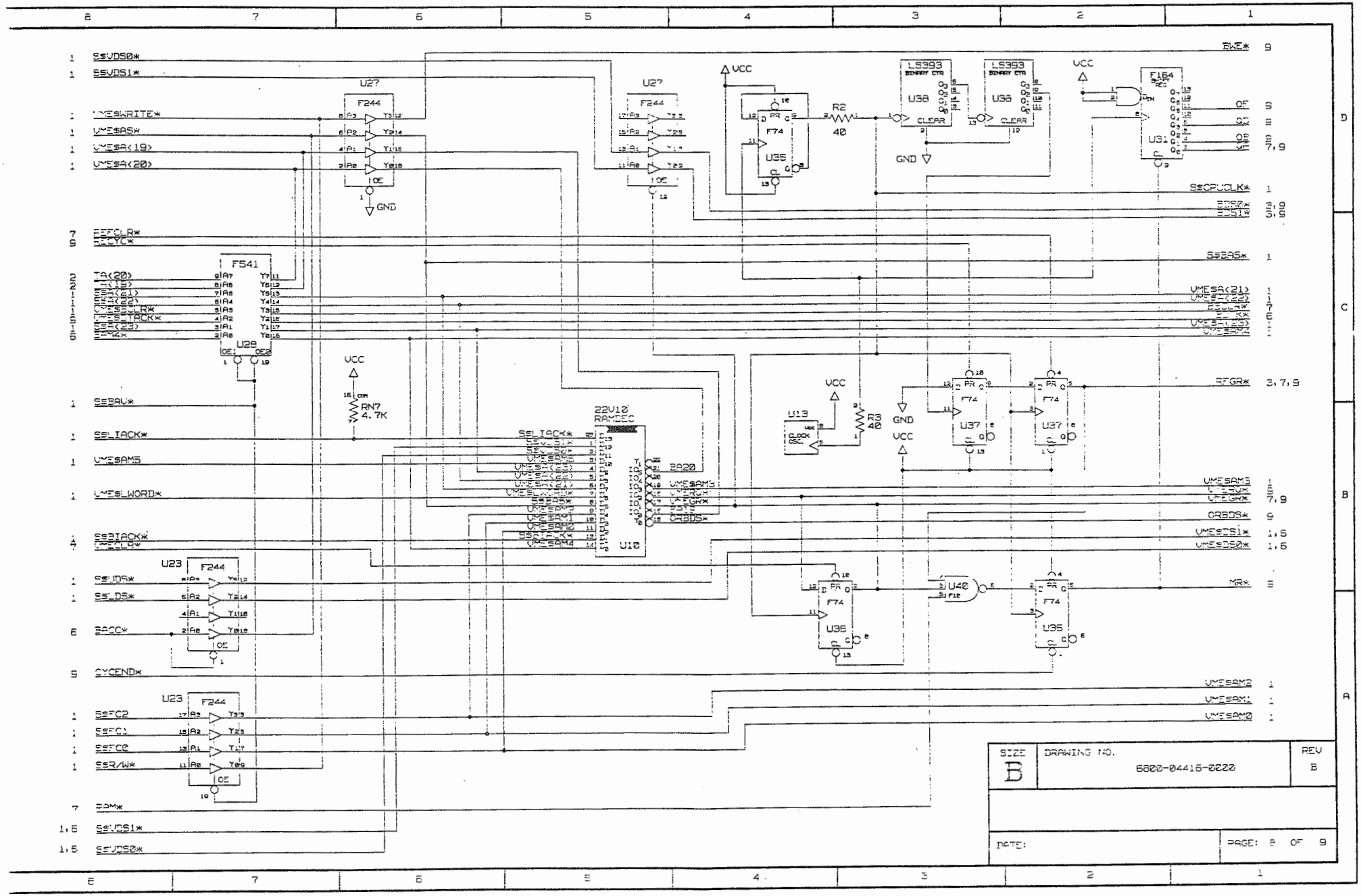
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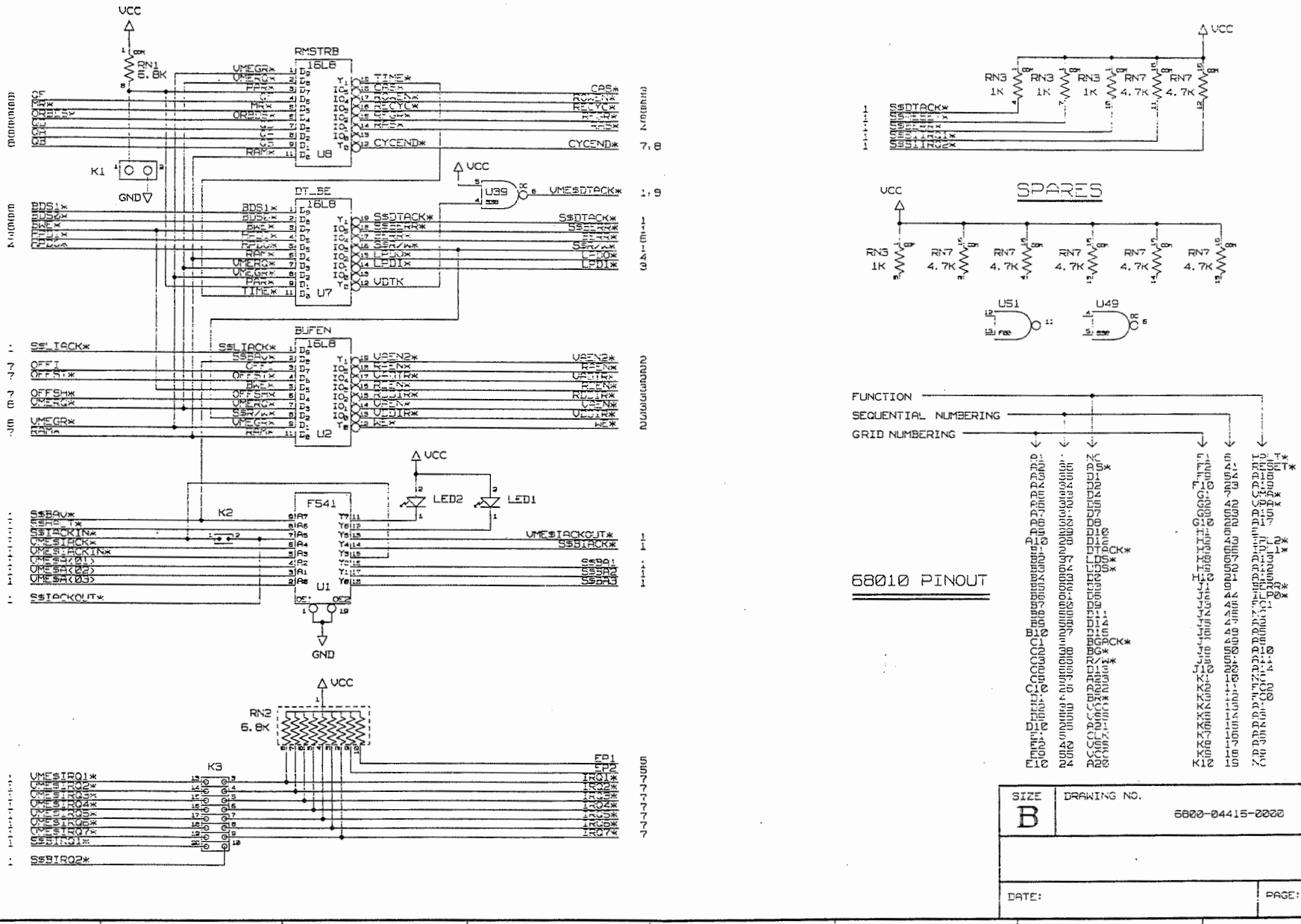
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