

ARTISAN®
TECHNOLOGY GROUP

Your **definitive** source for quality pre-owned equipment.

Artisan Technology Group
(217) 352-9330 | sales@artisantg.com | artisantg.com

Full-service, independent repair center
with experienced engineers and technicians on staff.

We buy your excess, underutilized, and idle equipment
along with credit for buybacks and trade-ins.

Custom engineering
so your equipment works exactly as you specify.

- Critical and expedited services
- In stock / Ready-to-ship
- Leasing / Rentals / Demos
- ITAR-certified secure asset solutions

Expert team | Trust guarantee | 100% satisfaction

All trademarks, brand names, and brands appearing herein are the property of their respective owners.

Find the *Emerson / Motorola / Force Computers CPU-1B* at our website: *Click HERE*

SYS68K / CPU-1B

User's Manual

First Edition
July 1984

FORCE COMPUTERS Inc./GmbH
All Rights Reserved

This document shall not be duplicated nor its contents used for any purpose unless express permission has been granted

Copyright by FORCE Computers

N O T E

The information in this document has been carefully checked and is believed to be entirely reliable. FORCE COMPUTERS makes no warranty of any kind with regard to the material in this document, and assumes no responsibility for any errors that may appear in this document. FORCE COMPUTERS reserves the right to make changes without notice to this, or any of its products, to improve reliability, performance or design.

FORCE COMPUTERS assumes no responsibility for the use of any circuitry other than circuitry which is part of a product of FORCE COMPUTERS GmbH/Inc.

FORCE COMPUTERS does not convey to the purchaser of the product described herein any license under the patent rights of FORCE COMPUTERS GmbH/Inc. nor the rights of others.

FORCE COMPUTERS Inc.
2041 Mission College Blvd.
Santa Clara, California 95054
U.S.A.

Phone: (409) 988-8686
Telex 172465
Telefax: (408) 980.93.31

FORCE COMPUTERS GmbH
Daimlerstrasse 9
D-8012 Ottobrunn/Muenchen
West-Germany

Phone: (089)6 09 20 33
Telex:5 24 190 forc-d
Telefax(0 89)6 09 77 93

Table of Contents

1.Ø	General Information	13
2.Ø	General Operation	15
3.Ø	Hardware Overview	19
3.1	The Microprocessor	19
3.1.1	The 68ØØØ Hardware Description	19
3.1.2	The 68Ø1Ø Hardware Description	22
3.2	The Dynamic RAM	22
3.2.1	The Refresh for the Dynamic RAM	22
3.2.2	Timings of the Dynamic RAM	24
3.2.3	The DRAM Summary	29
3.3	The PROM/EPROM Areas	3Ø
3.3.1	The SYSTEM Area	3Ø
3.3.2	The SYSTEM Area Summary	33
3.3.3	The USER Area	33
3.3.4	The USER Area Summary	36
3.3.5	The Access Speed Selector	36
4.Ø	Local I/O and Control Devices	38
4.1	The Serial I/O	38
4.1.1	The Terminal Interface	38
4.1.2	The Remote Interface	42
4.1.3	The Host Interface	46
4.1.4	The Baud Rate Selection	52
4.1.5	ACIA Access Times	56
4.1.6	Serial I/O Interface Summary	58
4.2	The Real Time Clock	59
4.2.1	Addressing of the RTC	59
4.2.2	Timing of the RTC	59

4.2.3 The RTC Interrupt Scheme 65

4.2.4 RTC Summary 65

4.3 The Parallel Interface and Timer Module (PI/T) 67

4.3.1 Addressing of the PI/T 69

4.3.2 The PI/T Interrupt Scheme 72

4.3.3 Centronics Parallel Interface 72

4.3.4 PI/T Summary 76

5.Ø The Interrupt Handling 77

5.1 The Interrupt Exception Sequence 77

5.2 The On-Board Interrupt Sources 81

5.3 The ACFAIL Interrupt Handling 82

5.4 The Software Abort Function Switch 85

5.5 The VMEbus Interrupt Handling 85

5.5.1 The Interrupt Acknowledge Daisy Chain on the VMEbus 89

5.5.2 The On-Board IACK Daisy Chain 94

6.Ø The VMEbus Arbitration 95

6.1 The Arbiter Options 95

6.1.1 The Global Bus Arbiter Function 96

6.2 The On-Board DTB Slave Bus Arbitration 99

6.3 The Bus Release Functions 1Ø3

6.4 The Single Level Bus Arbiter 1Ø5

6.5 The VMEbus Interface 1Ø7

6.6 The SYSCLK* Signal 112

6.7 The SYSRESET* Signal 112

6.8 The RESET* Function Switch 114

6.9 The SYSFAIL* Signal 114

6.1Ø The Address Modifier Codes 114

6.1Ø.1 The Function Codes 117

6.1Ø.2 The Short I/O Address Modifier 118

6.11 The Bus Error Function 112

7.0 Preparation for Use 126

APPENDIX A Specification of the SYS68K/CPU-1B,C,D A-1

APPENDIX B Memory Map of the SYS68K/CPU-1B,C,D B-1

APPENDIX C Address Assignment of I/O Devices C-1

APPENDIX D SYS68K/CPU-1B Component Part List D-1

APPENDIX E Circuit Schematics E-1

APPENDIX F Data Sheets - 68000 CPU F-7
- 68230 PI/T
- 6850 ACIA
- 58167A RTC

List of Figures

Fig. 1	Photo of Board	14
Fig. 2	The General Block Diagram of the SYS68K/CPU-1B	16
Fig. 3	The Global Refresh Timing Diagram	23
Fig. 4	Access Cycle without Refresh Request	26
Fig. 5	Double Access Cycle with Pending Refresh Request	28
Fig. 6	The Location Diagram of the SYSTEM Area	31
Fig. 7	Location Diagran of the USER Area	34
Fig. 8	Location Diagram of the Speed Selectors	37
Fig. 9	Hardware Diagram of the Terminal Interface	39
Fig.10	Location Diagram of the Termial Interface Parts	41
Fig.11	Hardware Diagram of the Remote Interface	44
Fig.12	Location Diagram of the Remote Interface Parts	45
Fig.13	Hardware Diagram of the Host Interface	48
Fig.14	Location Diagram of the Host Interface Parts	49
Fig.15	Configuration with a Host Computer	50
Fig.16	Interfacing to a Host Computer in the Transparent Mode	51
Fig.17	Hardware Drawing of the Baud Rate Selection Parts	54
Fig.18	Location Diagram of the Baud Rate Selection Parts	55
Fig.19	ACIA Timing Diagram (best case)	57
Fig.20	ACIA Timing Diagram (worst case)	57
Fig.21	RTC Write Cycle Timing Diagram	62
Fig.22	RTC Read Cycle Timing Diagram	64
Fig.23	Location Diagram of the RTC	66
Fig.24	PI/T Signal Assignment	68
Fig.25	Location Diagram of the PI/T Parts	73
Fig.26	The Centronics Interface Example	74
Fig.27	Timing Diagram of the Centronics Parallel Interface	75

Fig.28 The Global Interrupt Vector Acquisition 80

Fig.29 Location Diagram of the ACFAIL Jumper Field 83

Fig.30 The Power-Up/Power Down Timing Diagram 84

Fig.31 The VMEbus Interrupt Jumper Field 86

Fig.32 Location Diagram of the VMEbus Interrupt Parts 87

Fig.33 The Interrupt Acknowledge Daisy Chain 90

Fig.34 Functional Diagram of the Interrupt Acknowledge Daisy Chain Scheme 91

Fig.35 The Interrupt Vector Acquisition Timing 93

Fig.36 The Bus Grand Daisy Chain 97

Fig.37 Global DTB Arbitration Timing 98

Fig.38 The Jumper Fields for the Slave Bus Arbitration 100

Fig.39 The Location Diagram of the Slave Bus Arbitration 101

Fig.40 Bus Arbitration Timing Diagram 104

Fig.41 Timing Diagram of the One Level Bus Arbiter 106

Fig.42 Read Cycle followed by Write Cycle 109

Fig.43 Write Cycle followed by Read Cycle 111

Fig.44 Location Diagram of the Special Handling Signals 113

Fig.45 The Front Panel of the SYS68K/CPU-1B 115

Fig.46 The Short I/O Comparator 119

Fig.47 Location Diagram of the Short I/O Parts 121

Fig.48 Timing Diagram of a BERR* Cycle 123

Fig.49 Location Diagram of the BERR* Parts 125

List of Tables

Table 1	Vector Table of the 68000 CPU	21
Table 2	Time Values for an Access Cycle without Refresh Request	25
Table 3	Time Values for Double Access Cycle with Pending Refresh Request	27
Table 4	SYSTEM Area Jumper settings	32
Table 5	USER Area Jumper settings	35
Table 6	PROM Speed Selection	36
Table 7	Terminal Signal Assignments	40
Table 8	Remote Signal Assignments	43
Table 9	Host Signal Assignments	47
Table 10	The Baud Rate Selector (BR12-1-3)	52
Table 11	The Baud Rate Selector (BR12-1-2)	52
Table 12	ACIA Timing (best case)	56
Table 13	ACIA Timing (worst case)	56
Table 14	Register Model of the RTC	60
Table 15	RTC Write Time Values	61
Table 16	RTC Read Time Values	63
Table 17	Register Model of the PI/T	70
Table 18	The Interrupt Acknowledge Level Code	78
Table 19	The Interrupt Vector Conversion	78
Table 20	The Auto-Interrupt Vector Table	79
Table 21	The Interrupt Scheme of the On-Board Devices	81
Table 22	Time Values of the Power-Up/Power-Down Mechanism	84
Table 23	VMEbus Interrupt Jumper Settings	88
Table 24	Time Values of the Interrupt Vector Acquisition	92
Table 25	The Default Connections of the Slave Bus Arbitration	102
Table 26	Time Values of the Slave Bus Arbitration	105
Table 27	The One Level Bus Arbiter Option	105

Table 28 Time Values of the Single Level Bus Arbiter 105

Table 29 Read Cycle followed by Write Cycle 107

Table 30 Write Cycle followed by Read Cycle 110

Table 31 The SYSRESET* Jumper settings 112

Table 32 The Address Modifier Codes 116

Table 33 The Short I/O Jumper settings 120

Table 34 Jumper Settings of the Time-Out Counter 124

1.0 General Information

This high performance single board computer combines the powerful 16/32 bit microprocessor, the 68000, with 128/512K bytes of dynamic RAM, a maximum of 128K bytes of ROM/EPROM and powerful I/O devices.

The on-board real-time-clock, the three serial I/O interfaces, the parallel I/O and the timer offer a wide variety of functions for the SYS68K/CPU-1B.

Easy access to these devices is provided by the ROM resident SYSTEM MONITOR, called the SYS68K-1B monitor. This powerful software package can be used for program development and debugging.

The SYS68K/CPU-1B has been developed as a sophisticated VMEbus board which may be used in a multiprocessing environment as a number crunching unit, as a peripheral controller board or as a "stand-alone unit" because of its I/O and timer functions.

The usage of this board in critical real-time applications is enabled through the fast on-board dynamic RAM and the increasable microprocessor clock frequency (8 or 10 MHz).

This manual provides a general operating description of the SYS68K/CPU-1B,-1C,-1D,-1F hardware.

Follow manufacturer's installation instructions for usage and troubleshooting.

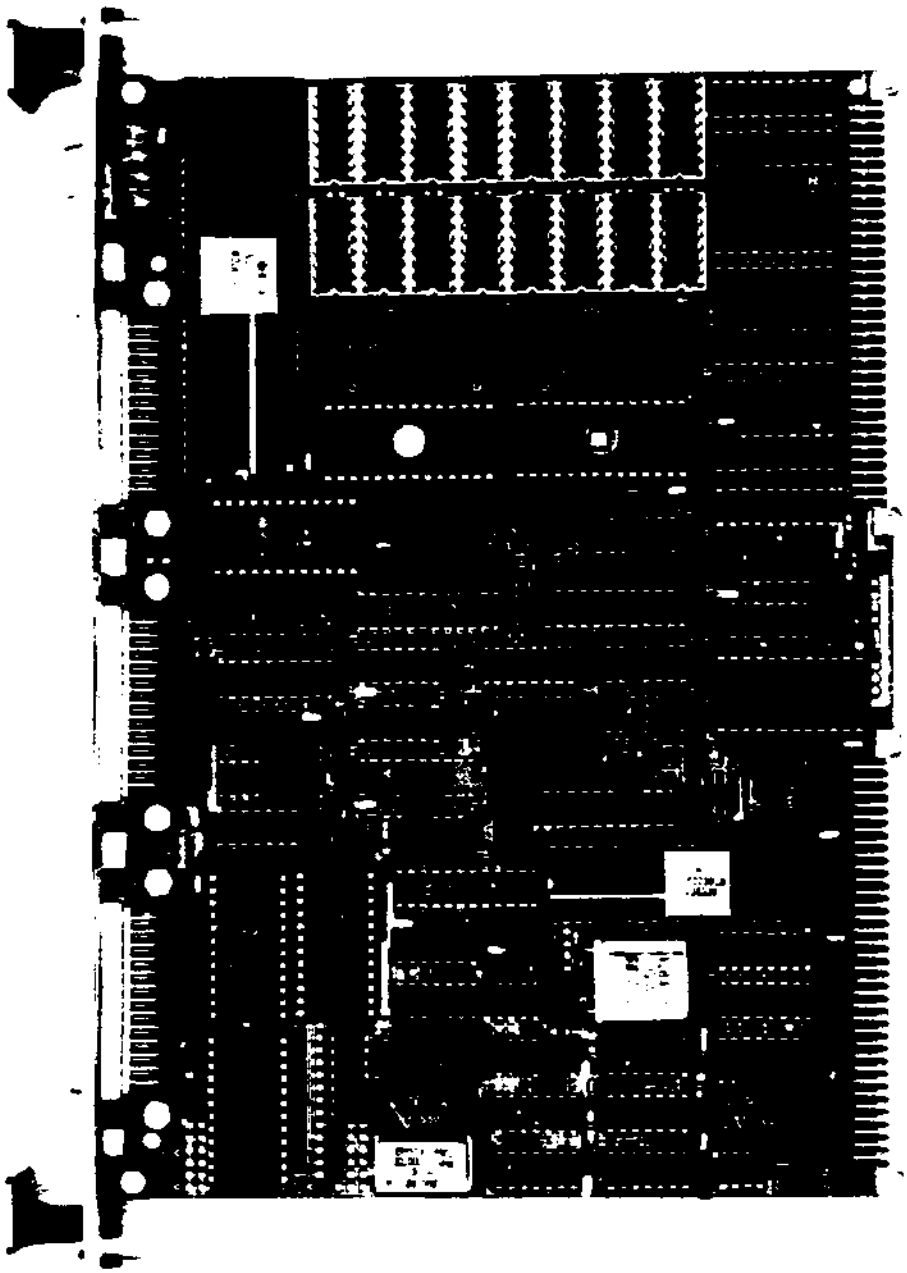


FIG. 1 PHOTO OF BOARD

2.0 General Operation

The SYS68K/CPU-1B board contains the powerful 68000 CPU with 128K bytes of dynamic RAM, a maximum of 128K bytes of EPROM, and several powerful I/O capabilities (see Fig.1).

One RS232 (C) interface (Port 1 connector P4) is used in conjunction with a standard terminal to enter and debug user programs under control of the monitor firmware.

A second RS232 (C) interface (Port 2 connector P3) may be used for up/down load of user programs and data, or in the transparent mode to interface the terminal connected to port 1 directly to a host computer.

The third RS232 (C) interface (Port 3 connector P5) is a universal port usable to support a serial printer, a floppy system, cartridge tape back-up, a second terminal (multi-user station), or an external user task.

The microprocessor-programmable Real Time Clock can be used in conjunction with a Multi User/Multi Tasking operating system and real time applications.

The parallel I/O port (68230 Parallel Interface Timer - PI/T) is accessible through the 64 PIN male connector P2. The PI/T adds 24 I/O lines and 4 control lines as well as a 24 bit timer with a 5 bit prescaler to the overall board capabilities.

The general block diagram of the SYS68K/CPU-1B board is shown in Fig. 2.

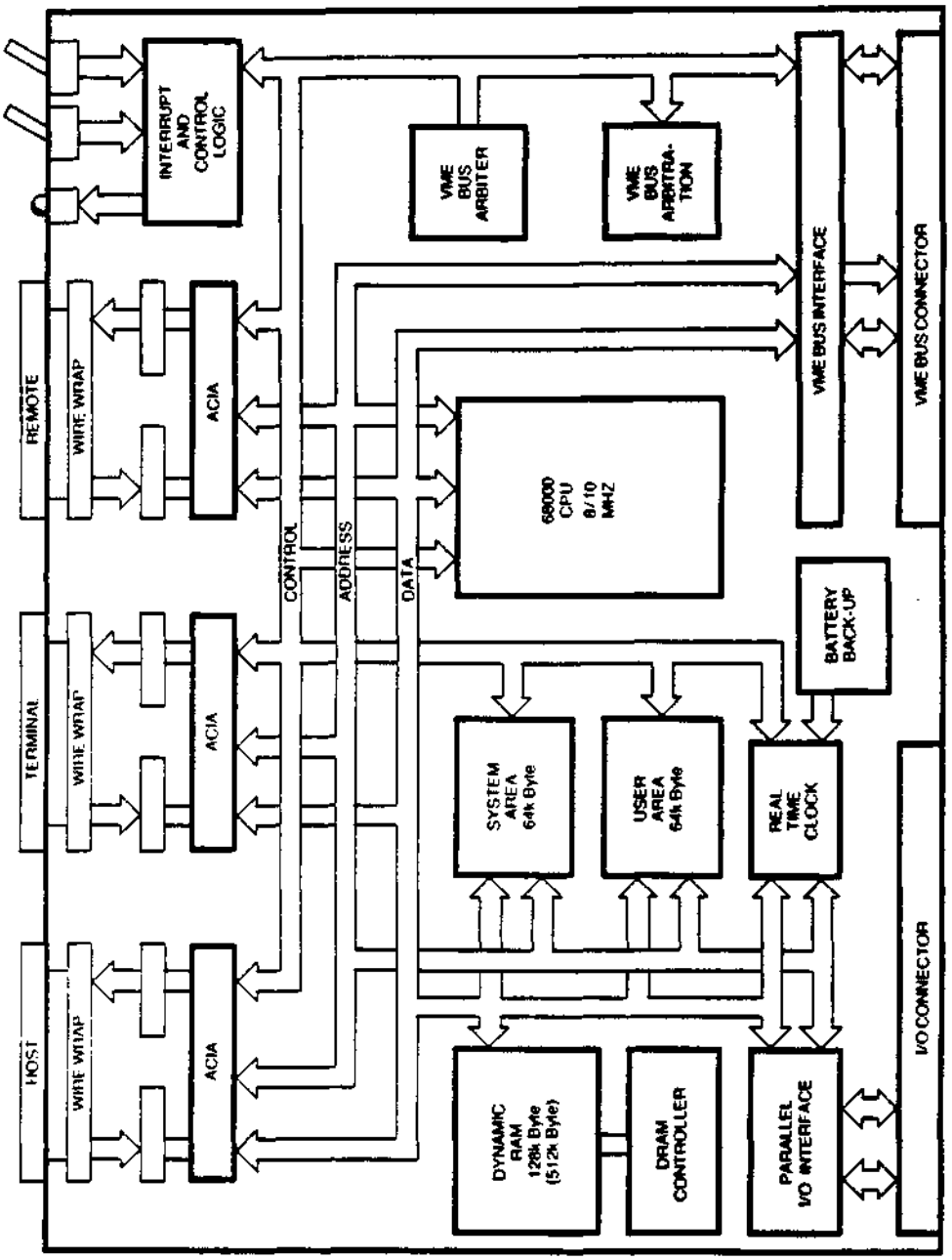


FIG. 2 BLOCK DIAGRAM OF THE SYS68K/CPU-1B

Features of the SYS68K/CPU-1B

- 68000 CPU with 8MHz clock frequency
- 128K bytes of DRAM arranged as 64K * 16 with an access time of 280ns (typ)
- Distributed Refresh (300ns maximum delay every 15us)
- 64K bytes (max) of ROM/EPROM for the system
- 64K bytes (max) of ROM/EPROM/SRAM for the user
- Real Time Clock with battery backup
- 3 RS232 Communication Interfaces (110-19200 Baud)
- Up/down-load to/from a host computer
- Transparent Mode
- Parallel Interface and Timer Chip provide I/O and Timer function
- Local Interrupt handling via auto-interrupt vectors
- Free jumper selectable address range for the short I/O address modifier (AM4)
- One level Bus Arbiter
- One level Slave Bus arbitration
- Fully VMEbus compatible
- RESET and SOFTWARE ABORT function switches

Features of the SYS68K/CPU-1C

- The SYS68K/CPU-1C contains the same features as the CPU-1B
- 68000 CPU with 10MHz clock frequency

Features of the SYS68K/CPU-1D

- The SYS68K/CPU-1D contains the same features as the CPU-1B
- 68000 CPU with 10MHz clock frequency
- 512K bytes of DRAM arranged as 256K * 16 with an access time of 280ns (typ)

Features of the SYS68K/CPU-1F

- The SYS68K/CPU-1F contains the same features as the CPU-1B
- 68000 CPU with 8MHz clock frequency
- 512K bytes of DRAM arranged as 256K * 16 with an access time of 280ns (typ)

All SYS68K/CPU-1B,-1C,-1D,-1F boards are available with the enhanced 68000 CPU, the 68010 (virtual machine). The features of the CPU-boards with the virtual processor are identical, only the CPU is changed, and a V identifies this version.

Virtual Processor Boards:

SYS68K/CPU-1VB

SYS68K/CPU-1VC

SYS68K/CPU-1VD

SYS68K/CPU-1VF

3.0 Hardware Overview

The heart of the SYS68K/CPU-1B board is the 68000 microprocessor unit (8 MHz) with its asynchronous 16 bit data bus and 23 bit address bus. The address bus provides a direct memory addressing range of 16 mega bytes. The memory and I/O devices communicate with the CPU via its local system bus. The address range from $000008 to $0FFFFF (1 Mega byte) is assigned to the on-board system memory and the I/O devices. All other addresses above $100000 are external addresses on the VMEbus.

The specifications of the SYS68K/CPU-1 boards are given in APPENDIX A.

3.1 The Microprocessor

Two different microprocessors can be used on the SYS68K/CPU-1 boards, the 68000 or the 68010. Both CPUs are described below.

3.1.1 The 68000 Hardware Description

The 68000 contains seventeen 32 bit registers, two 32 bit program counters, and a 16 bit status register. The first eight registers (D0 - D7) are used as data registers for byte (8 bit), word (16 bit) and long word (32 bit) operations. The set of seven address registers (A0 - A6) and the supervisor stack pointer may be used as software stack pointers and base address registers.

Additionally, all 17 registers may be used for word and long word address operations, or as index registers.

Table 1 shows the Vector Table Lay-Out of the 68000

Features of the 68000 CPU :

- 8 32 bit Data Registers
- 7 32 bit Address Registers
- 32 bit Supervisor Stack Pointer
- 32 bit User Stack Pointer
- 16 bit Status Register
- 16 Mbyte Direct Addressing Range
- 56 powerful Instruction Types
- 14 different Addressing Modes
- 5 main Data Types
- Memory Mapped I/O
- Asynchronous Bus Structure
- Transparent Hardware Handling

For further details see 68000 Data Sheet in APPENDIX F.

TABLE 1: 68000 CPU - Vector Table

Vector No.(s)	Address Dec	Hex	Space	Assignment
0	0	000	SP	Reset:Initial SSP
-	4	004	SP	Reset:Initial PC
2	8	008	SD	Bus Error
3	12	00C	SD	Address Error
4	16	010	SD	Illegal Instruction
5	20	014	SD	Zero Divide
6	24	018	SD	CHK Instruction
7	28	01C	SD	TRAPV Instruction
8	32	020	SD	Privilege Violation
9	36	024	SD	Trace
10	40	028	SD	Line 1010 Emulator
11	44	02C	SD	Line 1111 Emulator
12*	48	030	SD	(Unassigned,reserved)
13*	52	034	SD	(Unassigned,reserved)
14*	56	038	SD	(Unassigned,reserved)
15	60	03C	SD	Uninitialized Interrupt Vector
16-23	64	04C	SD	(Unassigned,reserved)
	95	05F		-
24	96	060	SD	Spurious Interrupt
25	100	064	SD	Level 1 Interrupt Autovector
26	104	068	SD	Level 2 Interrupt Autovector
27	108	06C	SD	Level 3 Interrupt Autovector
28	112	070	SD	Level 4 Interrupt Autovector
29	116	074	SD	Level 5 Interrupt Autovector
30	120	078	SD	Level 6 Interrupt Autovector
31	124	07C	SD	Level 7 Interrupt Autovector
32-47	128	080	SD	TRAP Instruction Vectors
	191	0BF		
48-63*	192	0C0	SD	(Unassigned,reserved)
	255	0FF		-
64-255	256	100	SD	User Interrupt Vectors
	1023	3FF		-

* Vector numbers 12,13,14,16 through to 23, and 48 through 63 are reserved for future enhancements by Motorola. No user peripheral devices should be assigned these numbers.

3.1.2 The 68010 Hardware Description

The 68010 CPU contains the same features as the 68000 CPU (code compatible) except for the following built-in enhancements.

A vector base register is used to determine the location of the exception vector table in memory to support multiple vector tables. Additionally, an alternate function code register allows the supervisor to access user data space of emulate CPU space cycles.

During a Bus Error exception processing sequence, the following information is placed on the supervisor stack:

1) Status Register

2) Program Counter (two to five words)

3) Frame format and vector offset

4) Internal register information (22 words)

3.2 The Dynamic RAM

The on-board RAM area is used for the CPU's exception vector table, as scratch pad for the system monitor, called SYS68K-1B, and for the user program/data. The dynamic RAM area consists of 128K bytes on the SYS68K/CPU-1B and on the SYS68K/CPU-1C.

The RAM area is expanded to 512K bytes on the SYS68K/CPU-1D and -1F. The DRAM has an access time of 280ns (typical) if no refresh cycle is under execution.

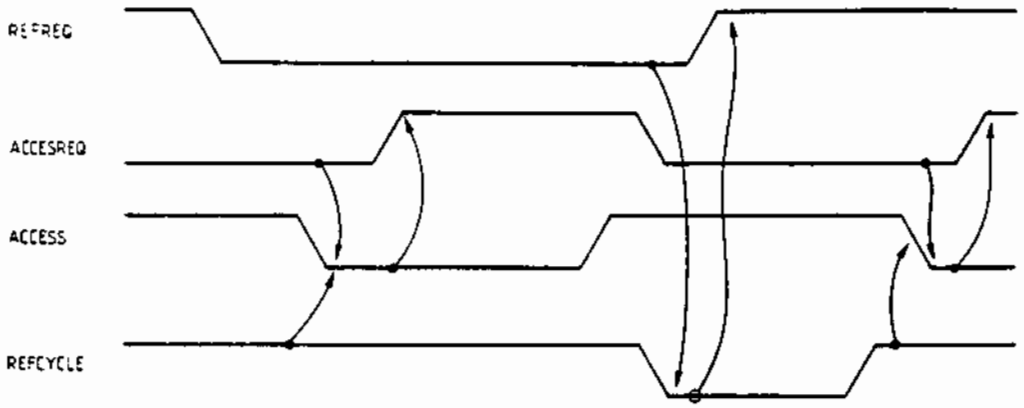
3.2.1 The Dynamic RAM Refresh

The Dynamic RAM refresh is accomplished by performing a memory cycle at each of the 128 row addresses at an interval of 2ms. The used "RAS Only Refresh " results in a substantial reduction of operating power. For real time operations, the refresh is fully asynchronous to the LOCAL and VMEbus accesses.

A maximum delay of 300ns for an access is required, when a refresh request is pending at the same time as an access request, because the refresh has the highest priority.

The refresh is organized in 128 steps every 2ms. This requires a minimum time delay, if access requests are pending and refresh is in process. The repetition rate for a refresh cycle is 15 microseconds.

The detailed timing diagram of the refresh is shown in Figure 3.



REFREQ = Refresh Request from Refresh Control Logic
ACCESREQ = Access Request from LOCAL bus
ACCESS = Pending Access from LOCAL bus
REFCYCLE = Pending Refresh Cycle for all RAM's

FIG. 3 THE GLOBAL REFRESH TIMING DIAGRAM

REFREQ = Refresh Request from Refresh Control Logic

ACCESREQ = Access Request from LOCAL bus

ACCESS = Pending Access from LOCAL bus

REFCYCLE = Pending Refresh Cycle for all RAMs

3.2.2 Timings of the Dynamic RAMs

This paragraph descibes all the timings to/from the DRAMs.

In general, the DRAMs are 150ns devices which operate at an effective access time of 180ns.

A fully asynchronous control logic drives the access cycles as well as the refresh cycles.

The refresh circuitry generates one refresh cycle every 15 micro-seconds. Therefore the board can be used to operate in high-end real time applications.

Table 2 Time Values for an Access Cycle without Refresh Request

SIGNAL DESCRIPTION	(ns) Min.	(ns) Max.
1. AS* active to Access Request active	10	33
2. AS* active to Access Cycle start	33	66
3. AS* active to DTACKOUT* asserted	285	328
4. AS* active to AS* inactive	285	14000
5. AS* inactive to DTACKOUT* inactive	30	45
6. AS* inactive to Access Cycle inactive	15	25
7. Data valid before DTACK* asserted	10	-

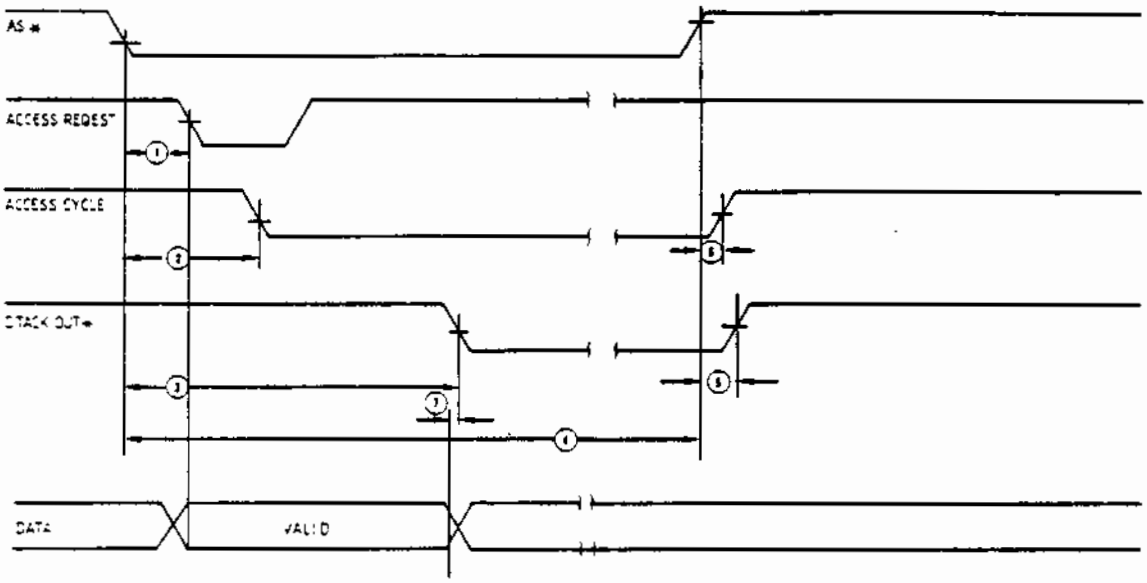
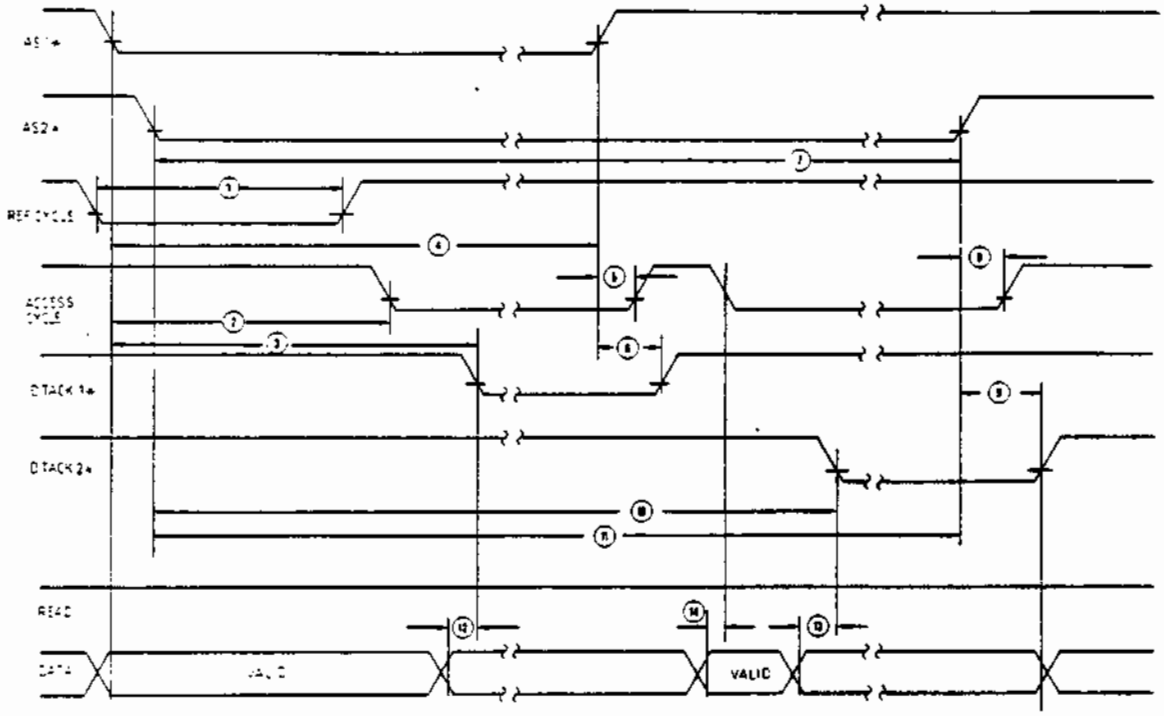


FIG. 4 ACCESS CYCLE WITHOUT REFRESH REQUEST

Table 3 Time Values for a Double Access Cycle with Pending Refresh Request

SIGNAL DESCRIPTION	(ns) Min.	(ns) Max.
1. REFCYCLE active	290	330
2. AS1* active to Access Cycle active	320	360
3. AS1* active to DTACK1* active	560	600
4. AS1* active to AS1* inactive	560	14000
5. AS1* inactive to Access Cycle inactive	15	25
6. AS1* inactive to DTACK1* inactive	30	45
7. AS2* active to AS2* inactive		
8. AS2* inactive to Access Cycle inactive	15	25
9. AS2* inactive to DTACK2* inactive	30	45
10. AS2* active to DTACK2* active	880	920
11. AS2* active to AS2* inactive	880	14000
12. Data valid to DTACK1* active	0	
13. Data invalid to DTACK2* active	0	
14. Data valid to start Access Cycle	0	



AS1*, DTACK1*: AS* and DTACK* for the first cyle
AS2*, DTACK2* : AS* and DTACK* for the second cycle

FIG. 5 DOUBLE ACCESS CYCLE WITH PENDING REFRESH REQUEST

3.2.3 The DRAM Summary

Start Address	$000008
End Address a)	$01FFFF (128K bytes)
End Address b)	$07FFFF (512K bytes)
Boundary a)	$020000
Boundary b)	$080000
Access Modes	Byte or Word
	Read or Write
Usable Data Bits	D0-D7 and D8-D15
Access Time	285ns (min)
	320ns (typ)
	600ns (max) with Refresh

3.3 The PROM/EPROM Areas

The SYS68K/CPU-1B consists of 4 sockets for JEDEC compatible devices. Two different memory banks (with 2 sockets each) are used - one for the boot-up and one for user application programs.

3.3.1 The SYSTEM Area

During the power-up phase the 68000 CPU reads two vectors from this EPROM area; one is the Initial Stack Pointer (Address $000000 - $000003) and one is the Intitial Program Counter (Address $000004 - $000007).

The data signals D0-D7 are used on the socket J40 (lower) and the data signals D8-D15 are connected to the socket J24 (upper).

For proper initialisation, the first eight addresses from the SYSTEM Area are down-mapped to this address range.

Fig.6 shows the location diagram of the SYSTEM Area.

The SYSTEM Area can be configured for the following devices:

EPROM	2732	4K * 8	8K bytes total
EPROM	2764	8K * 8	16K bytes total
EPROM	27128	16K * 8	32K bytes total
EPROM	27256	32K * 8	64K bytes total

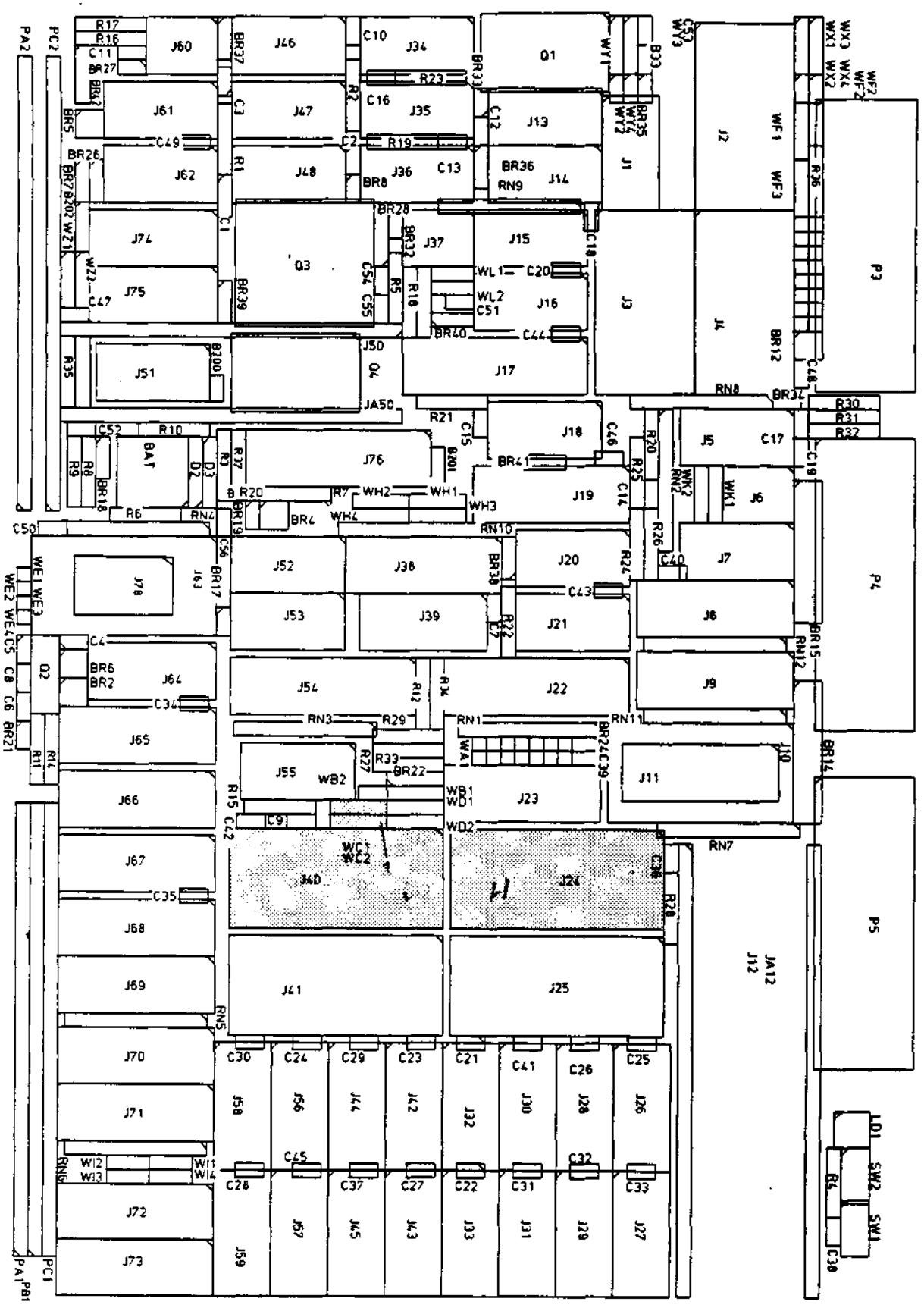


FIG. 6 LOCATION DIAGRAM OF THE SYSTEM AREA

The connection of the address and control signals between the different device types is provided through a wire-wrap area (WC1 and WC2)

The following table shows all the jumper settings which are required for the different devices:

Table 4 SYSTEM Area Jumper settings

Device Type	Connection between:
2732	WC1#1 - WC2#2
	WC1#2 - WC2#2
	WC1#4 - WC2#4
2764* and	WC1#1 - WC2#1
27128*	WC1#2 - WC2#2
	WC1#4 - WC2#4
27256	WC1#1 - WC2#1
	WC1#2 - WC1#3
	WC1#4 - WC2#4

* default condition during manufacturing

3.3.2 The SYSTEM Area Summary

Start Address	$080008
End Address	$09FFFF
Boundary	$020000
Boot Address	$000000 to $000007
Access Modes	Byte or Word
	Read Only
Access Time (jumper selectable)	60 - 375ns (min) 125 - 500ns (max)

3.3.3 The USER-Area

For user application programs or as a static RAM area, two 28 pin sockets are provided on the board.

The chip-selection for the upper- (D8-D15) and the lower socket (D0-D7) on the board is byte wide organized. This allows byte manipulation in the SRAM-mode.

Fig.7 shows the location diagram of the USER Area and the wire-wrap configuration area.

This wire-wrap configuration area defines which address/control signals are connected to the socket pairs.

The following device types are usable in the USER Area:

EPROM	2732	4K * 8	8K bytes total
EPROM	2764	8K * 8	16K bytes total
EPROM	27128	16K * 8	32K bytes total
EPROM	27256	32K * 8	64K bytes total
SRAM	6264	8K * 8	16K bytes total

Table 5 descibes the jumper settings required for the different devices.

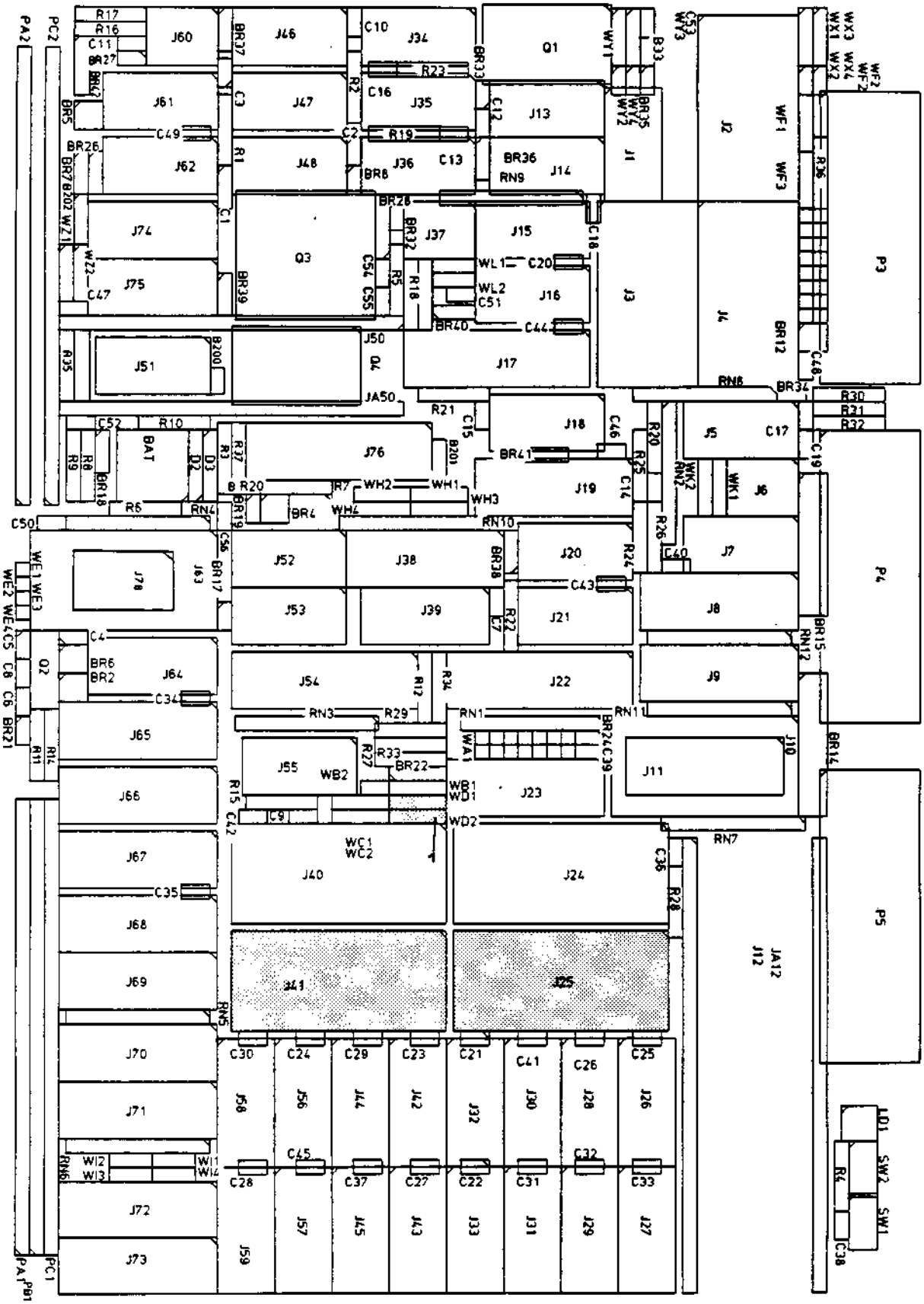


FIG. 7 LOCATION DIAGRAM OF THE USER AREA

Table 5 USER Area Jumper Settings

Device Type	Connection between:
2732	WD1#1 - WD2#2
	WD1#2 - WD2#2
	WD1#4 - WD2#4
2764	WD1#1 - WD2#1
27128	WD1#2 - WD2#2
	WD1#4 - WD2#4
27256	WD1#1 - WD2#1
	WD1#2 - WD1#3
	WD1#4 - WD2#4
6264*	WD1#1 - WD2#2
	WD1#2 - WD2#3
	WD1#4 - WD2#4

* default condition during manufacturing

3.3.4 The USER Area Summary

Start Address	$0A0000
End Address	$0BFFFF
Boundary	$020000
Access Modes	Byte or Word transfers
	Read or Write on SRAM
	Read only on EPROM
Usable Data Bits	D0-D7 and D8-D15
Access Time (jumper selectable)	60 - 375ns (min) 125 - 500ns (max)

3.3.5 The Access Speed Selector

To enable the use of fast and slow devices, the PROM/EPROM areas have a selectable access time speed selector.

This jumper field provides different jumper settings as listed in Table 6.

Fig.7 shows the location diagram of the speed selectors.

Table 6 PROM Speed Selection

Jumper Closed on BR7	Jumper Closed on BR6	Access Times (ns) Min.	Max.	Device Access Times (ns)
2 - 3	2 - 3	62	125	60
2 - 3	2 - 4	125	188	125
2 - 3	2 - 1	188	250	180
1 - 2	2 - 3	125	250	125
1 - 2	2 - 4	250	375	250
1 - 2	2 - 1	375	500	375

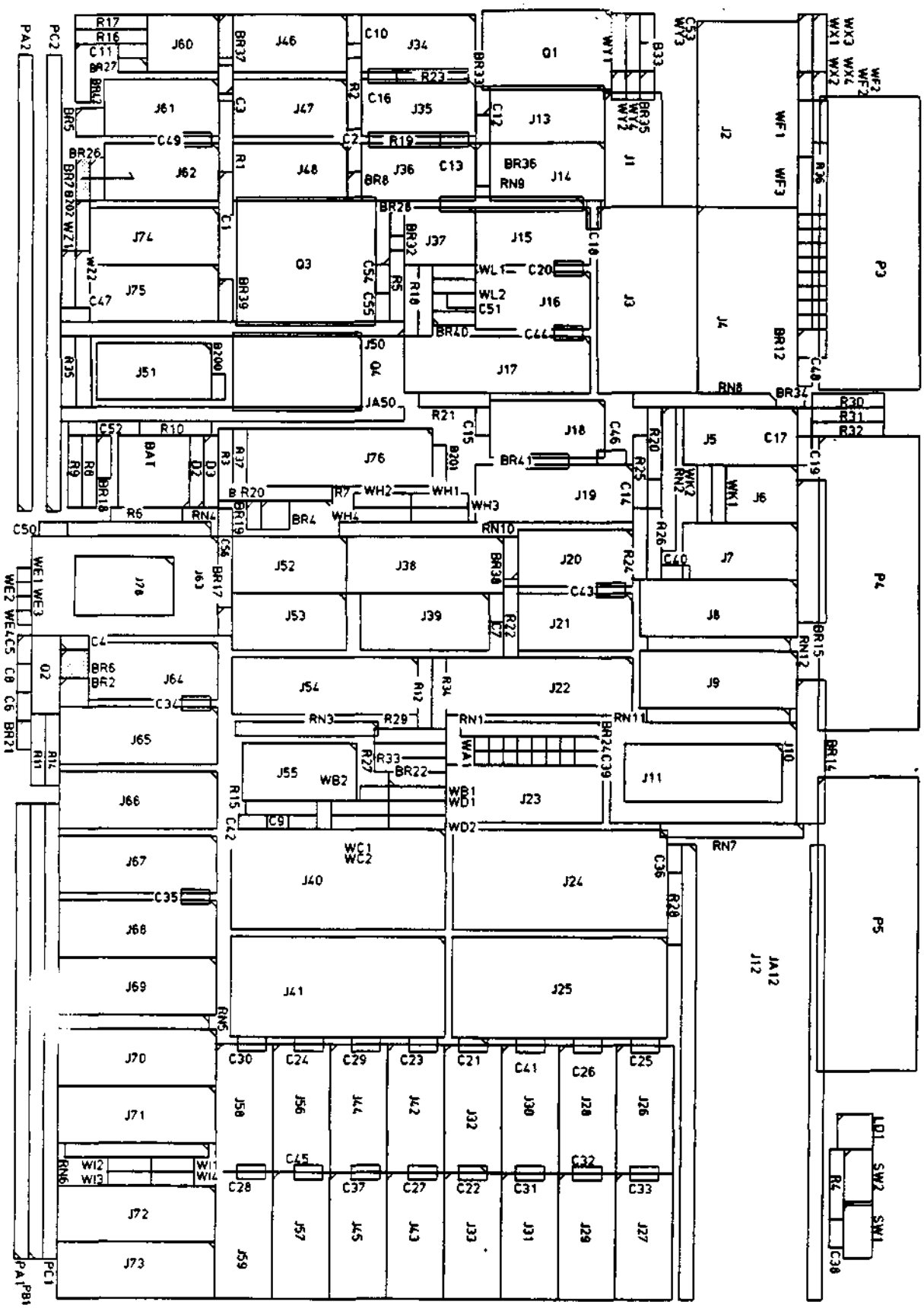


FIG. 8 LOCATION DIAGRAM OF THE SPEED SELECTORS

4.0 Local I/O and Control Devices

The SYS68K/CPU-1B board contains 3 serial I/O Communication Interfaces, a Real Time Clock with a battery back-up and a Parallel Interface and Time Module.

4.1 The Serial I/O

The board contains 3 independant serial I/O channels with a seperate strap selectable Baud Rate (110 to 19200 Baud). Each serial I/O interface has a jumper field for easy I/O signal assignment changes to the 25 pin D-sub connectors (female).

All serial I/O control chips are 6850 devices (Asynchronous Communication Interface Adapter - ACIA).

4.1.1 The Terminal Interface

The RS232 (C) interface is used to communicate via Port 1 (connector P4) with a standard terminal. The transmission format is initially preset as follows:

8 Data Bits

1 Stop Bit

No Parity

No Protocol

The terminal must be set to these conditions.

Further details of control functions and port format changes are shown in the Software Manual of the used system monitor. The detailed hardware diagram of the interface is given in Fig.9.

The terminal interface can interrupt the 68000 CPU on level 4. The forced interrupt vector is the auto interrupt vector (#28/$000070)

The default signal assignments during manufacturing are listed in Table 7.

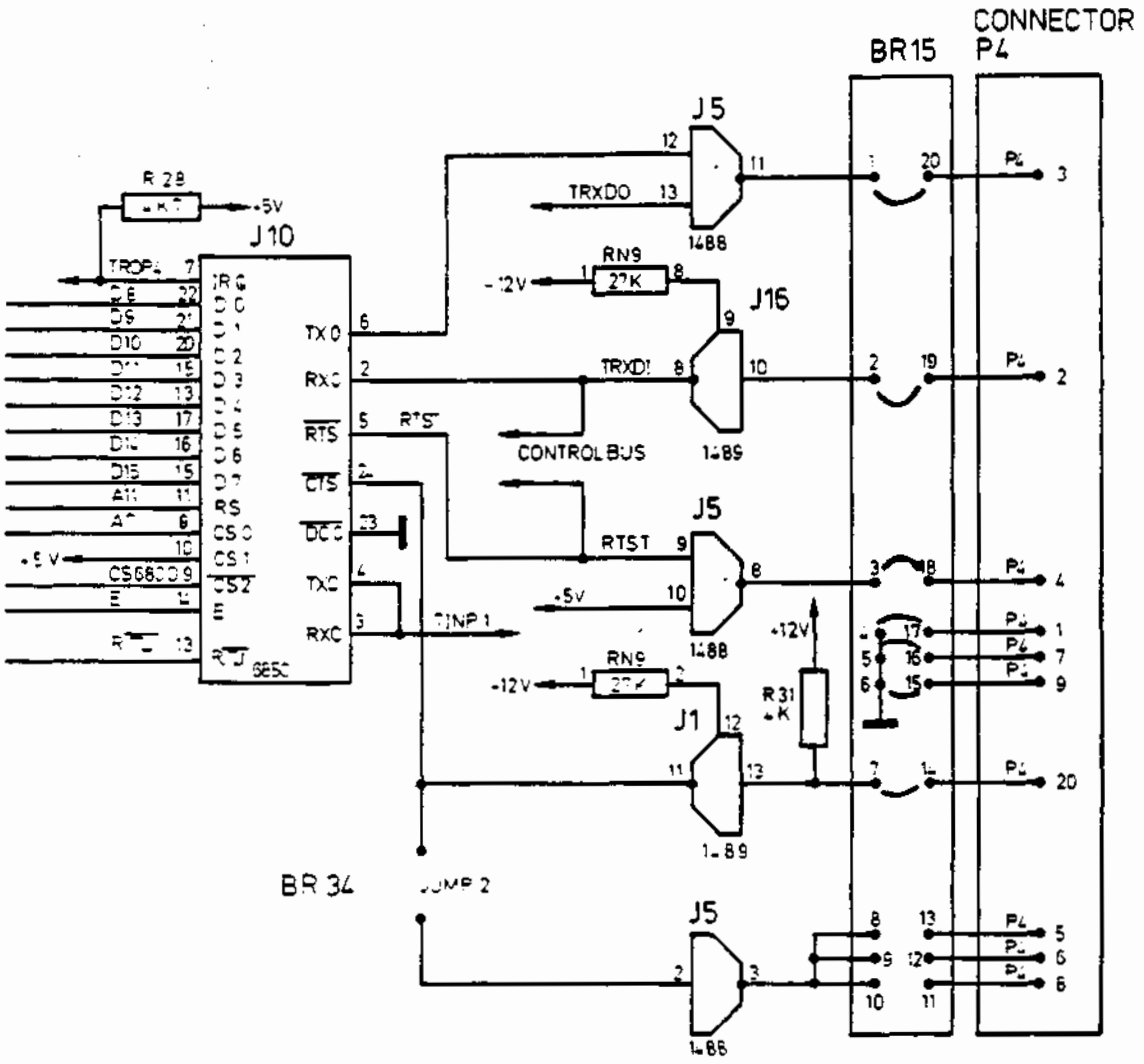


FIG. 9 HARDWARE DIAGRAM OF THE TERMINAL INTERFACE

Table 7 Terminal Signal Asignments

P4 PIN	INPUT	OUTPUT	SIGNAL
1	X	X	Protective GND connected to signal GND
2	X		Transmit Data (TXD)
3		X	Receive Data (RXD)
4		X	Request to Send (RTS)
5		X	Clear to Send (CTS)
6		X	Data Set Ready (DSR)
7	X	X	Signal GND
8		X	Data Carrier Detect (DCD)
9	X	X	Signal GND
20	X		Data Terminal Ready (DTR)

The location diagram of the Terminal Interface parts are outlined in Fig.10

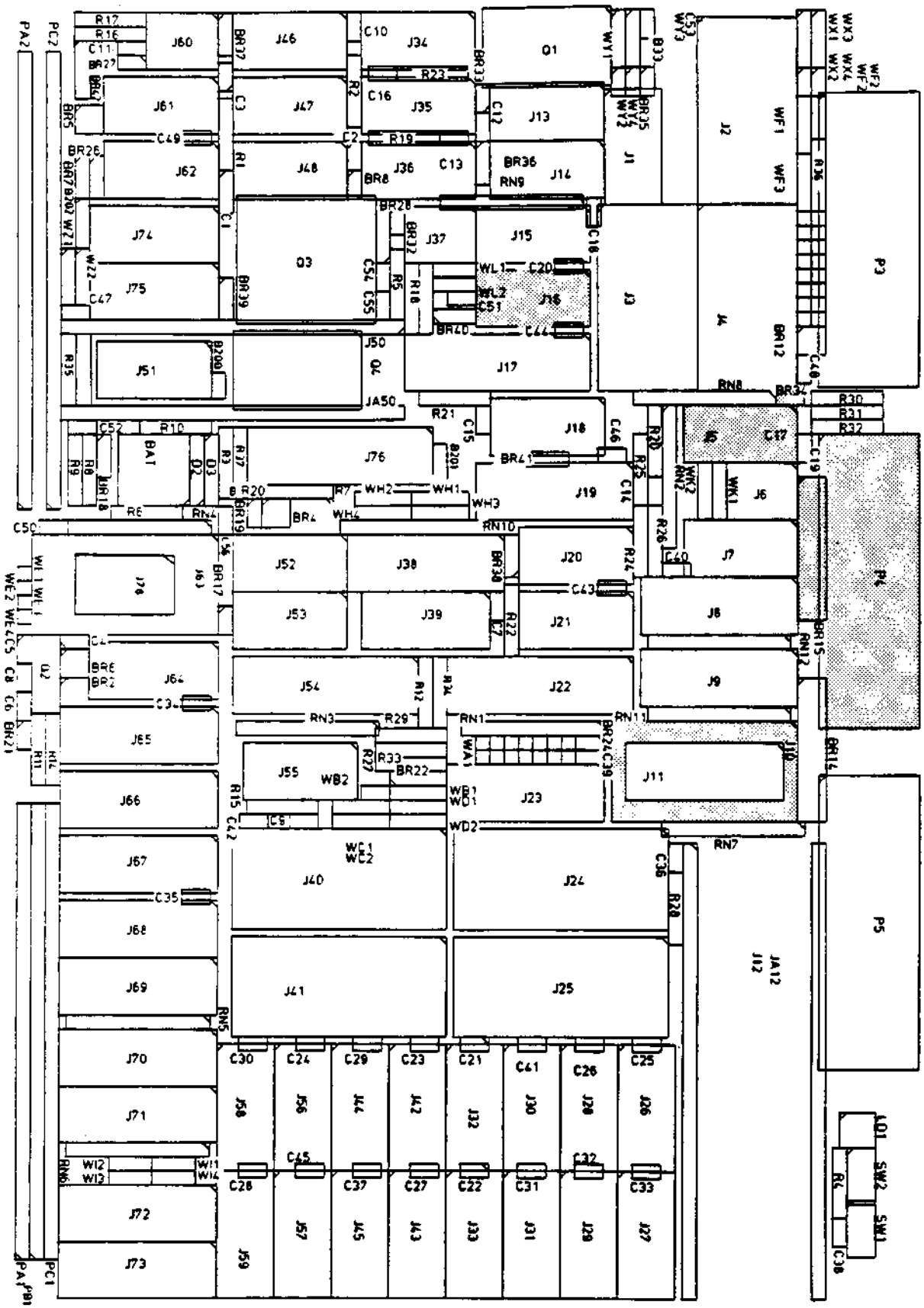


FIG. 10 LOCATION DIAGRAM OF THE TERMINAL INTERFACE PARTS

4.1.2 The Remote Interface

The second RS232 compatible interface is the Remote Interface.

The hardware drawing is shown in Fig.11, and the location diagram of the interface parts is outlined in Fig.12.

Typical applications for this interface are :

- Serial Printer
- Second Terminal (Multi-User Applications)
- Serial Link to a Back Up Medium.

The Remote Interface can interrupt the 68000 CPU on level 3. The forced interrupt vector is the autovector (#27/$0000006C)

Table 8 lists the default assignments during manufacturing :

Table 8 Remote Signal Assignments

P4 PIN	INPUT	OUTPUT	SIGNAL
1	X	X	Protective GND connected to signal GND
2	X		Transmit Data (TXD)
3		X	Receive Data (RXD)
4		X	Request to Send (RTS)
5		X	Clear to Send (CTS)
6		X	Data Set Ready (DSR)
7	X	X	Signal GND
8		X	Data Carrier Detect (DCD)
9	X	X	Signal GND
20	X		Data Terminal Ready (DTR)

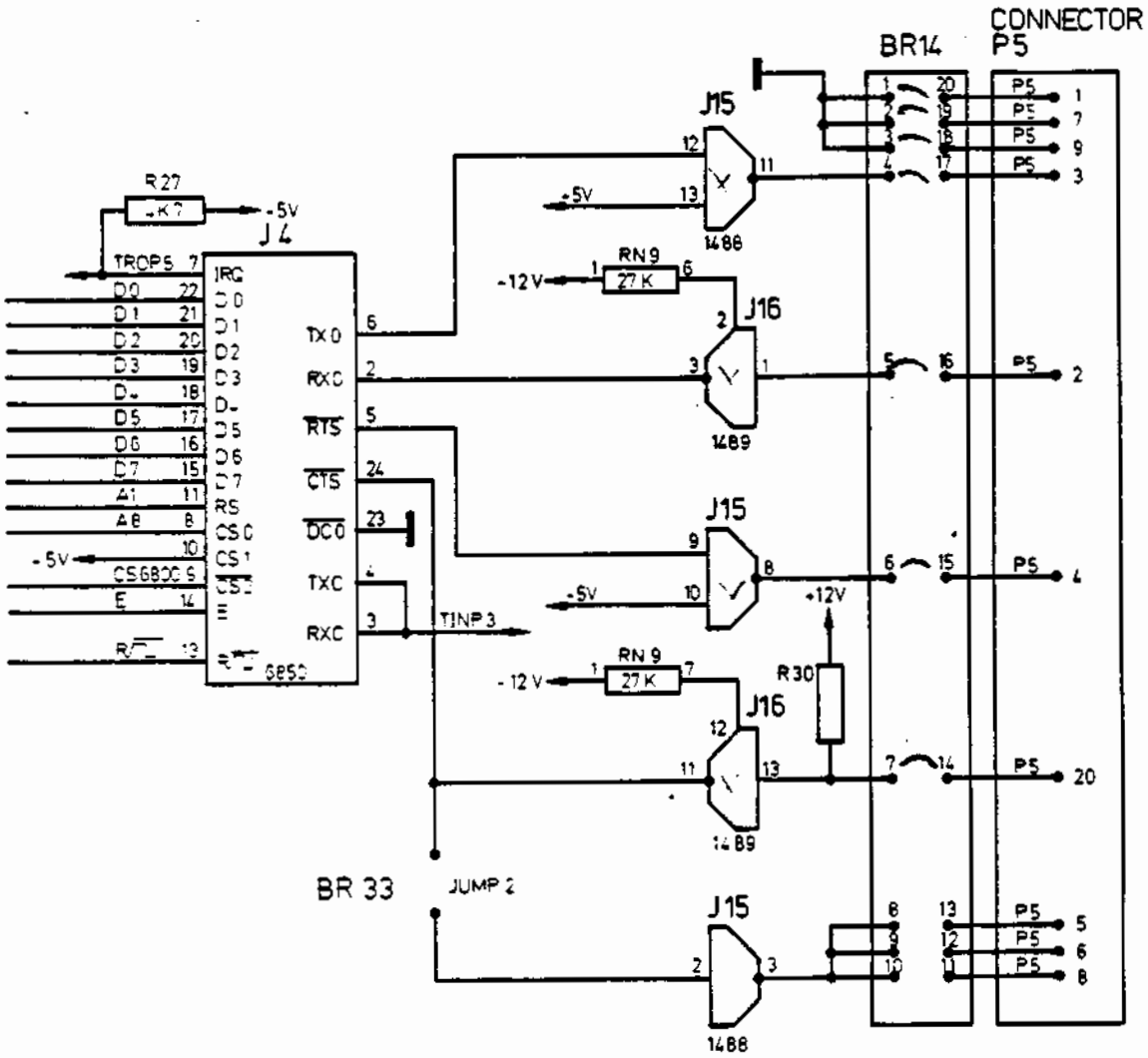


FIG. 11 HARDWARE DIAGRAM OF THE REMOTE INTERFACE

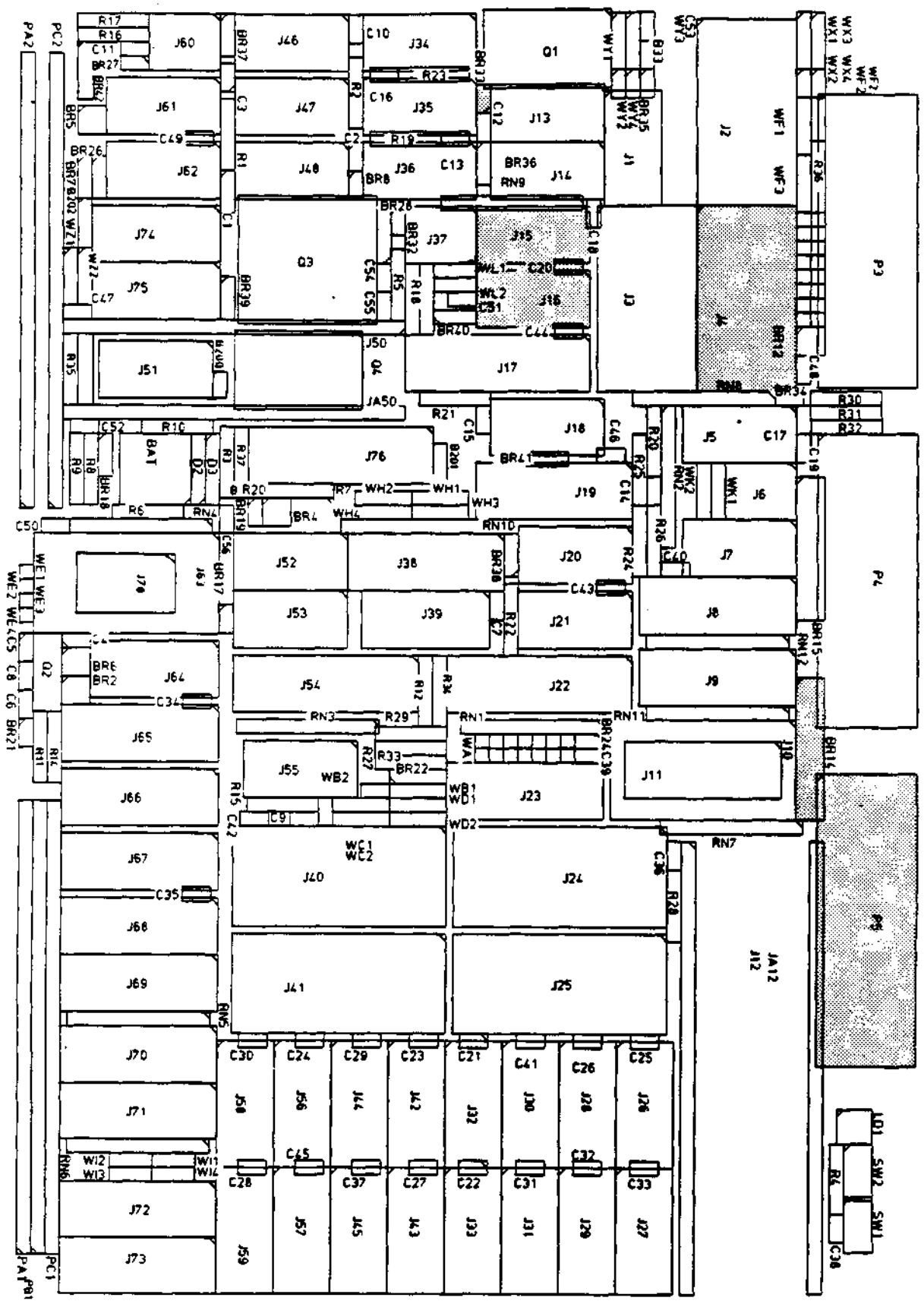


FIG. 12 LOCATION DIAGRAM OF THE REMOTE INTERFACE PARTS

4.1.3 The Host Interface

The third on-board RS232(C) interface can be used in conjunction with a host computer. The detailed schematic is given in Fig.16.

A standard communication method to communicate between a terminal (connector P4) and a host computer (connector P3) is the Transparent Mode. When the Transparent Mode is used, all transmitted characters are sent directly from the terminal to the host computer and no correction or modification is done by the SYS68K/CPU-1B board. In a configuration like the one shown in Fig.15, both computers are configured to receive data on the Transmit Data Line (TXD) from the terminal and echo is via the Receive Data Line (RXD) back to the terminal. The SYS68K/CPU-1B board polls the terminal ACIA registers in the Transparent Mode. When the user types in the valid stop character sequence, the CPU recognizes it, stops the transmission of the following characters from the terminal to the host computer, and returns to the system monitor program. The stop character sequence is the last character sequence that the SYS68K/CPU-1B board sends to the host computer.

If the connected device cannot drive the CTS signal to high state, a connection from P3 pin 5 to pin 20 has to be hard wired.

The baud rate of each module (Terminal, SYS68K/CPU-1B board terminal interface, and host computer interface) must be jumpered equally. The baud rate of the host ACIA remains unaltered because the Transparent Mode handling does not use this ACIA for the transfer.

A detailed description of the data format and the system monitor Dump/Load (DU/LO) commands is given in the manual.

The Host Interface can interrupt the 68000 CPU on level 2. The forced interrupt vector is the auto-interrupt vector (#26/$000068).

Table 9 lists the default signal assignments during manufacturing:

Table 9 Host Signal Assignments

P4 PIN	INPUT	OUTPUT	SIGNAL
1	X	X	Protective GND connected to signal GND
2		X	Transmit Data (TXD)
3	X		Receive Data (RXD)
5	X		Clear to Send (CTS)
7	X	X	Signal GND
9	X	X	Signal GND
20		X	Data Terminal Ready (DTR)

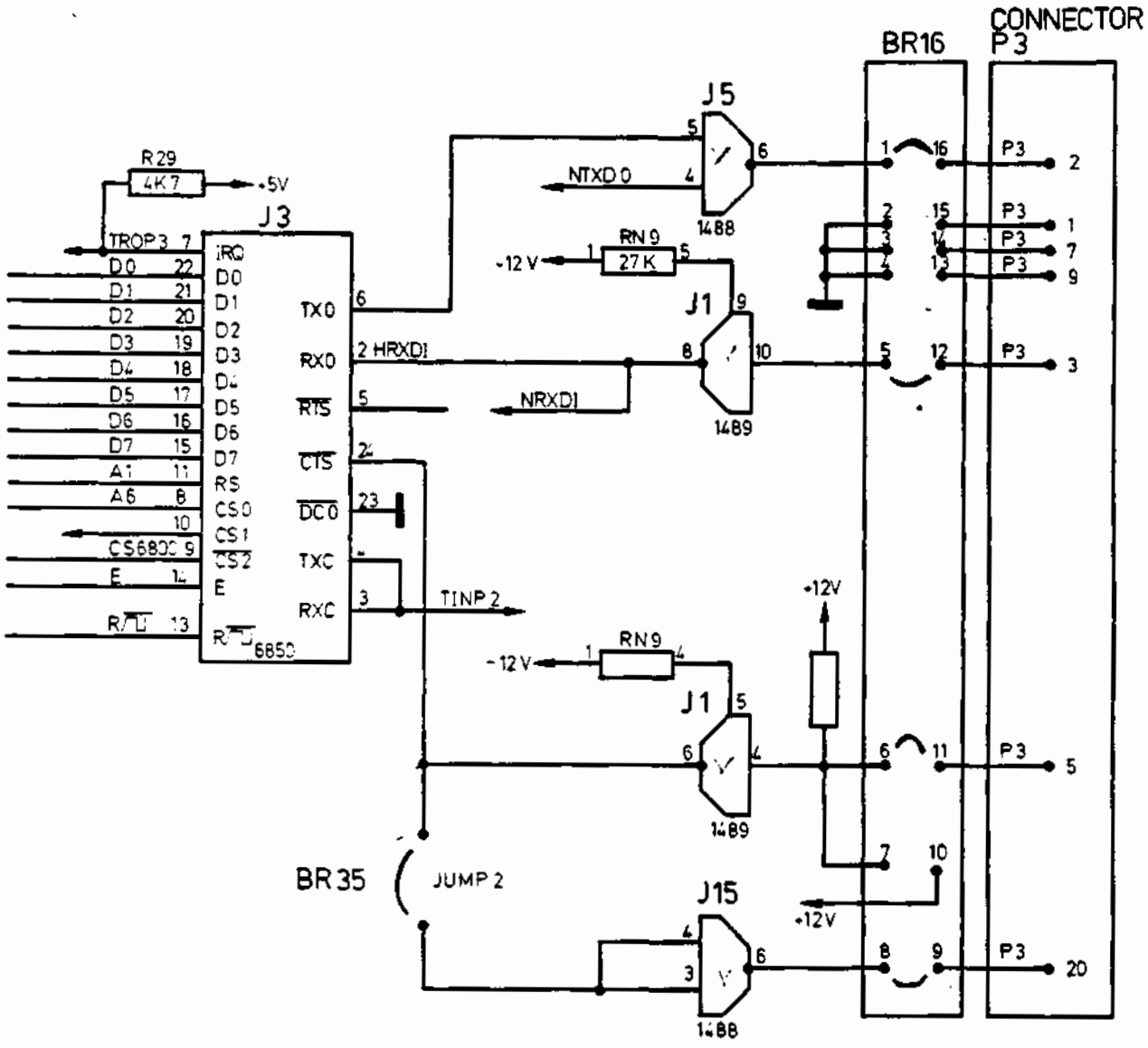


FIG. 13 HARDWARE DIAGRAM OF THE HOST INTERFACE

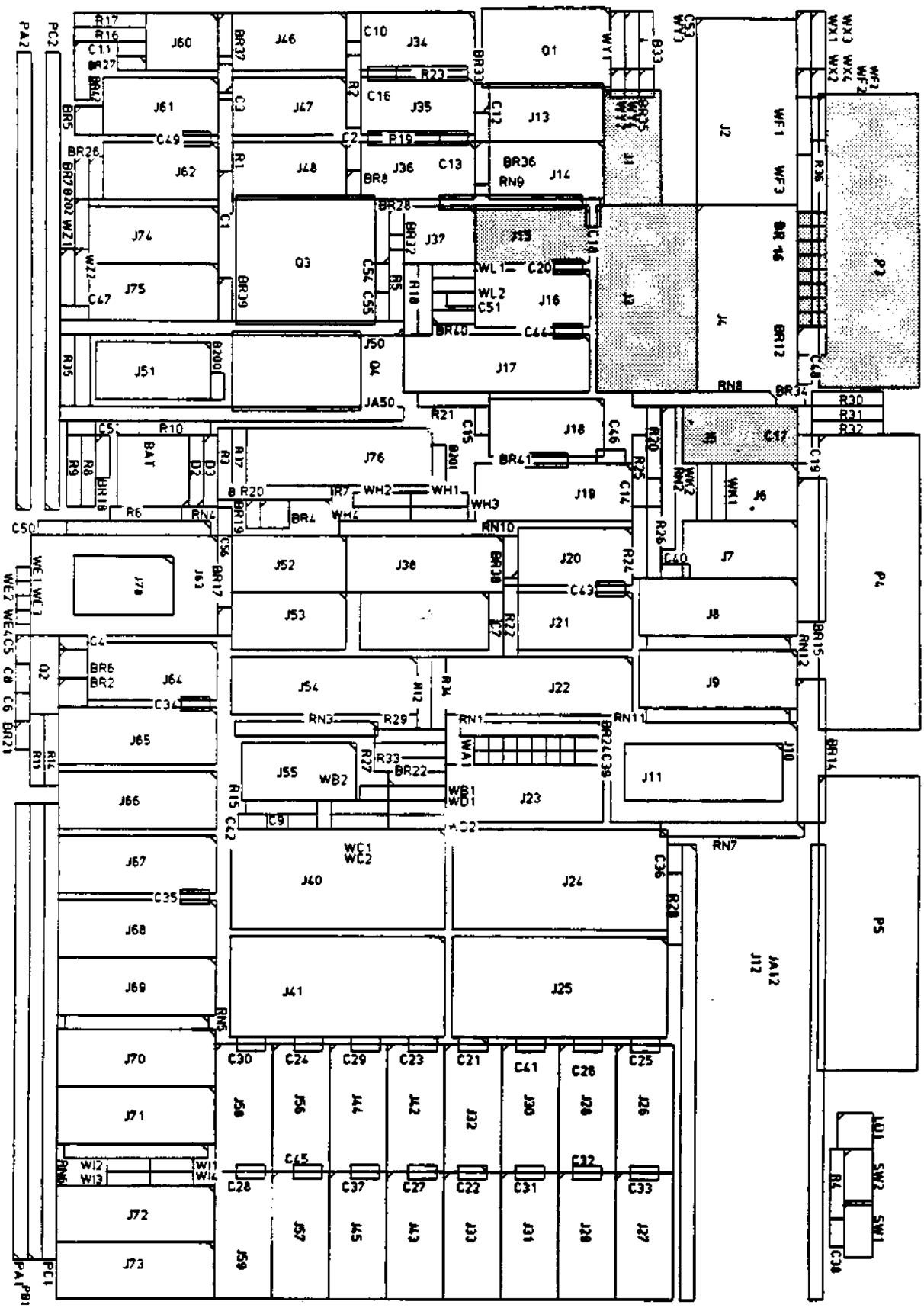


FIG. 14 LOCATION DIAGRAM OF THE HOST INTERFACE

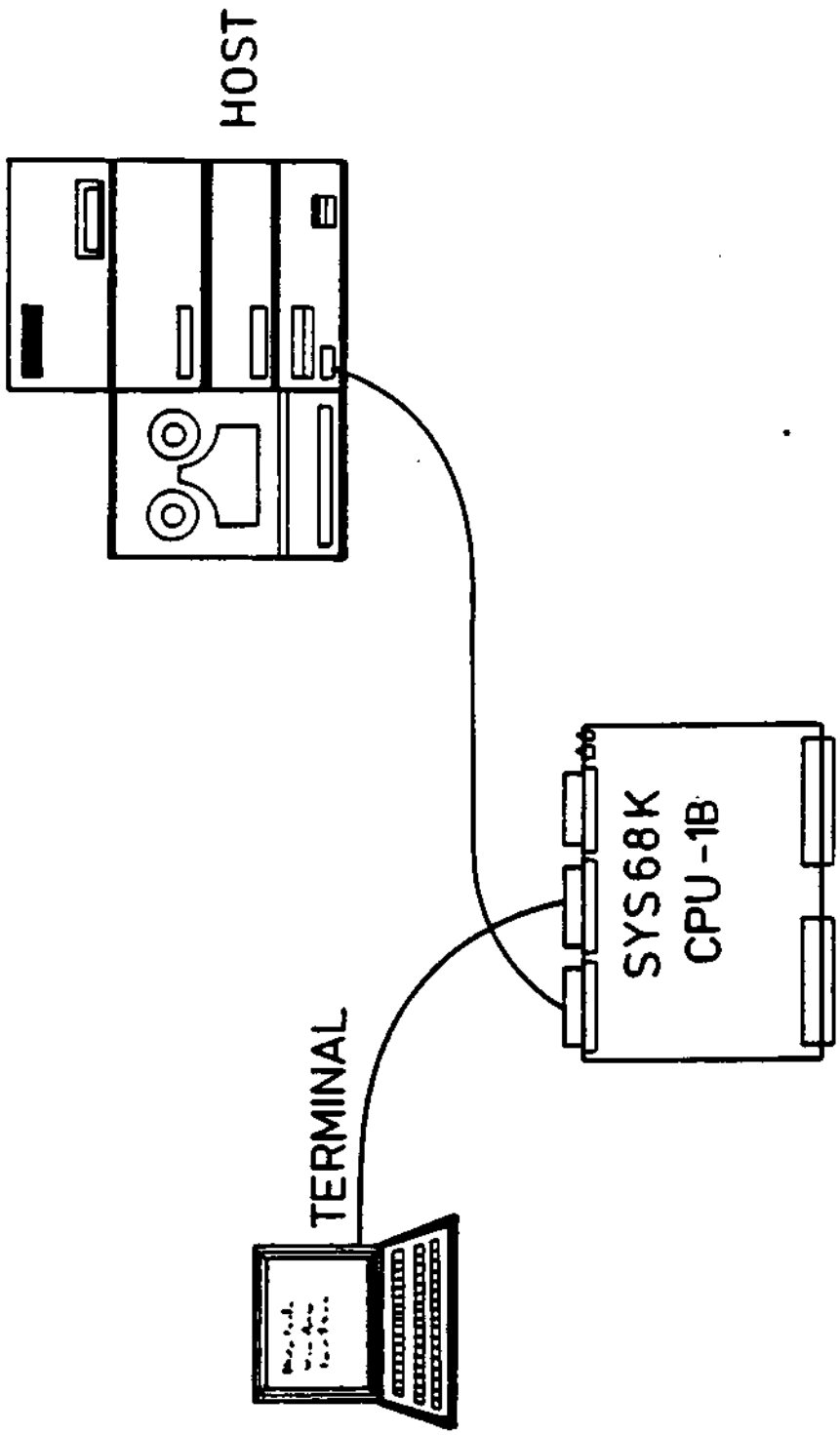


FIG. 15 CONFIGURATION WITH A HOST COMPUTER

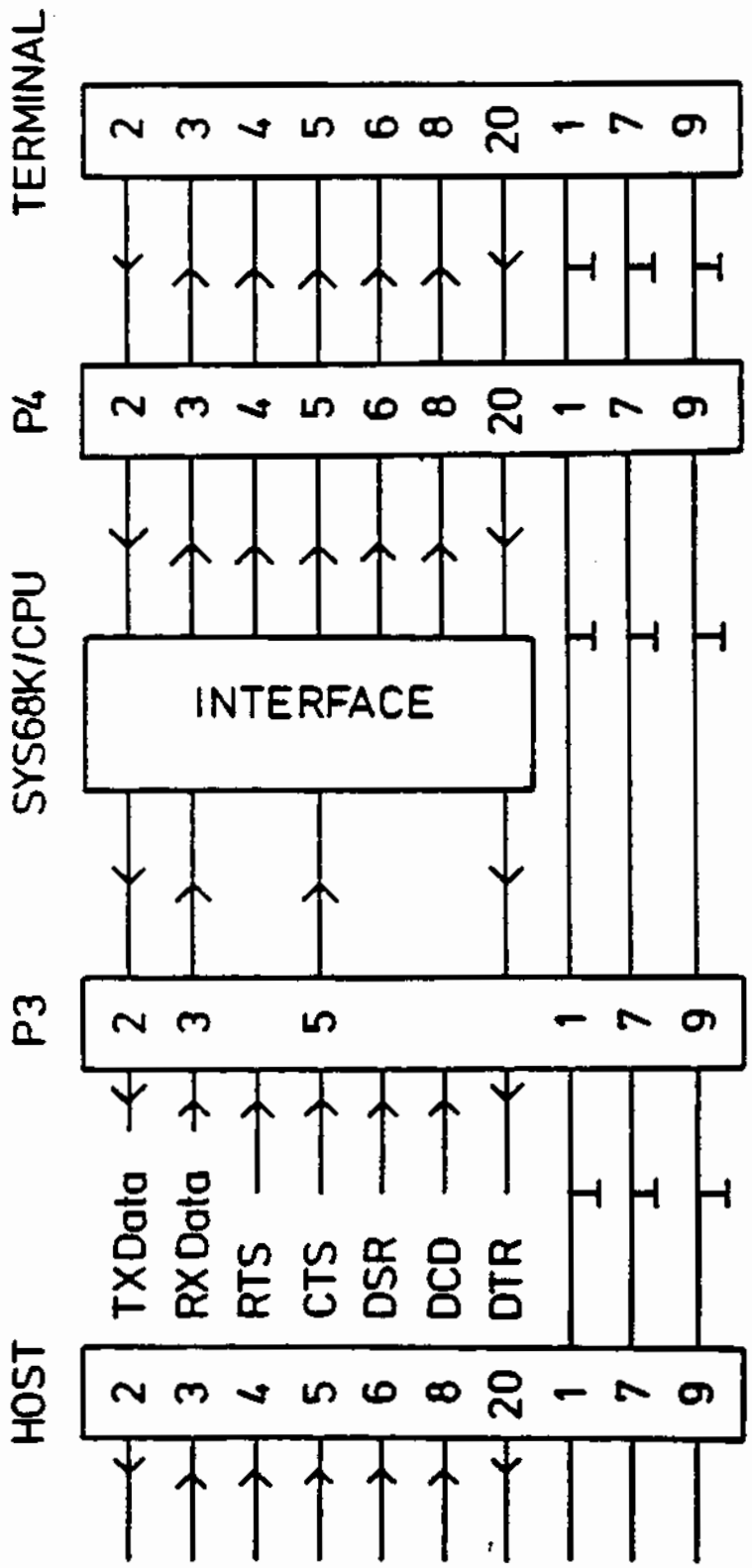


FIG. 16 INTERFACING TO A HOST COMPUTER IN THE TRANSPARENT MODE

4.1.4 The Baud Rate Selection

Each clock input for the transmit and receive baud rate of the three serial I/O channels is strap selectable to one of the 8 different baud rate clocks driven by the 14411.
Tables 10 and 11 define the values.

Table 10 The Baud Rate Selector (BR12-1-3)

Jumper PIN	Baud Rate	
WF1#1	9600	TINP1, TINP2, TINP3
WF1#2	4800	
WF1#3	2400	
WF1#4	1200	
WF3#1	600	
WF3#2	300	
WF3#3	150	
WF3#4	110	

Table 11 The Baud Rate Selector (BR12-1-2)

Jumper PIN	Baud Rate
WF1#1	38400
WF1#2	19200
WF1#3	9600
WF1#4	4800
WF3#1	2400
WF3#2	1200
WF3#3	600
WF3#4	440

The Baud Rates of the Terminal, Host and Remote Interface are, in default during manufacturing, connected to 9600 Baud.

The jumper field BR12 defines the ratio of the driven Baud Rate.

A jumper setting between pin 1 and pin 3 (default condition) results in the Baud Rates listed in Table 10, and a jumper setting between pin 1 and pin 2 results in the Baud Rates listed in Table 11.

Figs.17 and 18 show the detailed hardware drawing and the jumper location diagram.

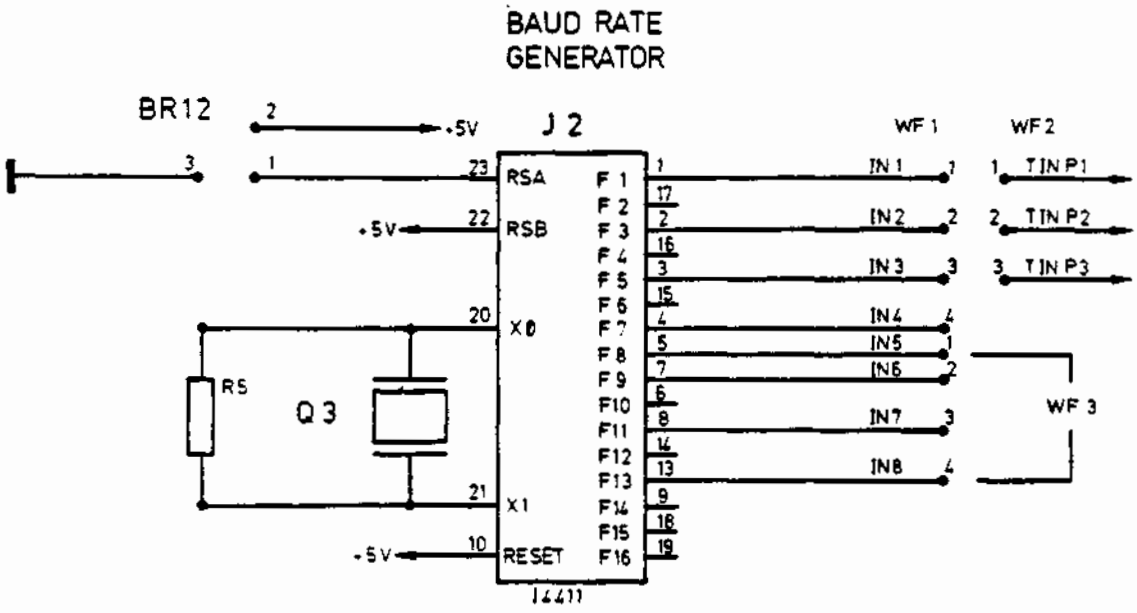


FIG. 17 HARDWARE DRAWING OF THE BAUD RATE SELECTION PARTS

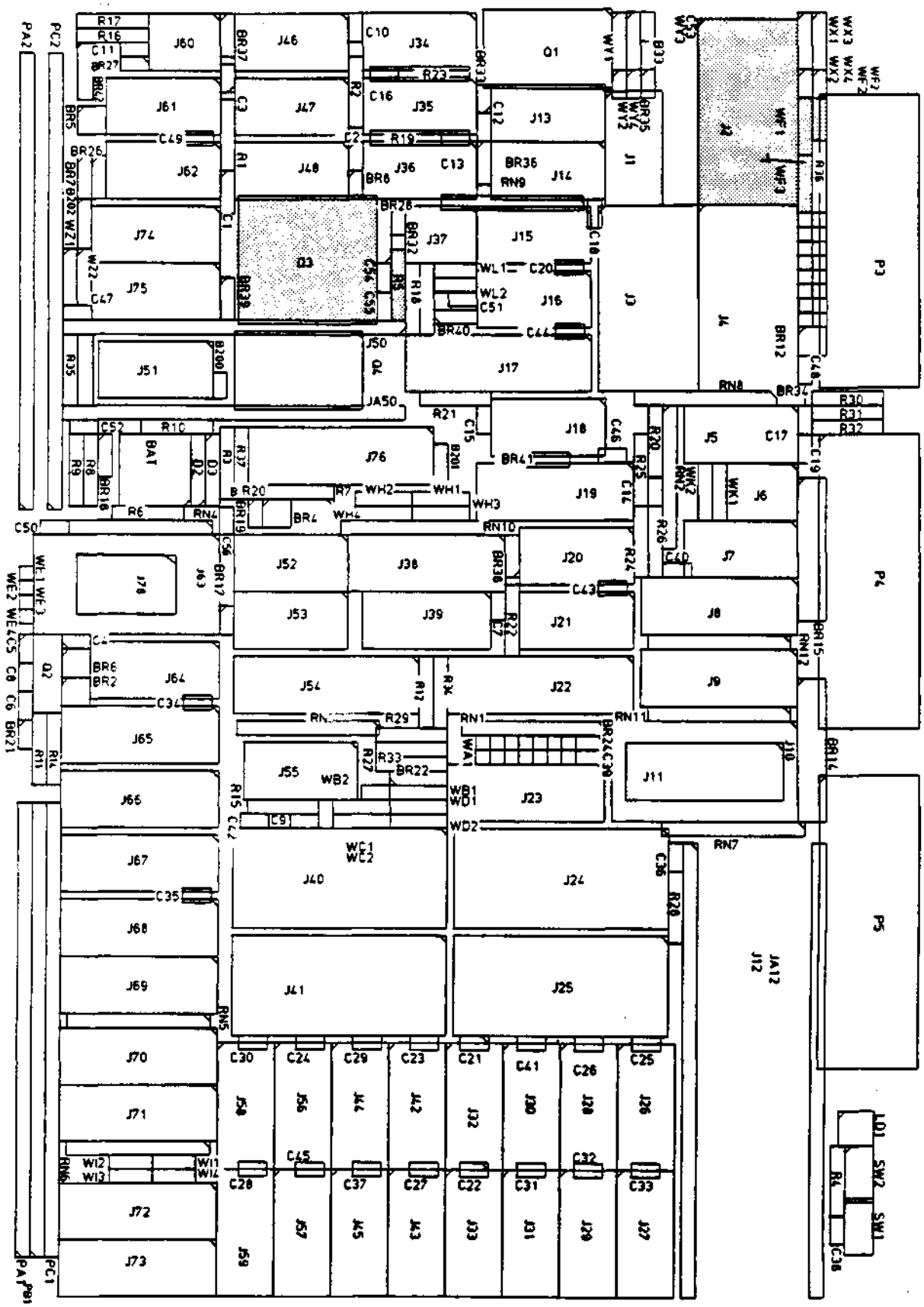


FIG. 18 LOCATION DIAGRAM OF THE BAUD RATE SELECTION PARTS

4.1.5 ACIA Access Times

The ACIA is a controller device from the synchronous 6800 family. Therefore, the access cycle is controlled by the Processor signals VMA*,VPA* and the E signal.

To initiate the transfer, the Processor must receive the VPA* signal from the decoding logic. When the CPU is synchronized to the E clock signal, the VMA* signal is asserted to signal the I/O devices that the transfer is beginning. The synchronization requires additional time (1000ns maximum).

The timing diagrams, illustrating the best and worst cases are shown in Figs. 19 and 20.

Tables 12 and 13 list the related values.

Table 12 ACIA Timing (best case)

No	Description	Min	Max	Unit
1	AS* low	800		ns
2	AS* asserted to VPA* asserted	30	80	ns
3	AS* inactive to VPA* inactive	30	80	ns
4a	VMA* asserted (8MHz Processor clock frequency)	850	1000	ns
4b	VMA* asserted (10MHz Processor clock frequency)	700	900	ns
5	VPA* to VMA* delay	-	150	

Table 13 ACIA Timing (worst case)

No	Description	Min	Max	Unit
1	AS* low	-	2000	ns
2	AS* asserted to VPA* asserted	30	80	ns
3	AS* inactive to VPA* inactive	30	80	ns
4a	VMA* asserted (8MHz Processor clock frequency)	850	1000	ns
4b	VMA* asserted (10MHz Processor clock frequency)	700	900	ns
5	VPA* to VMA* delay	-	1000	ns

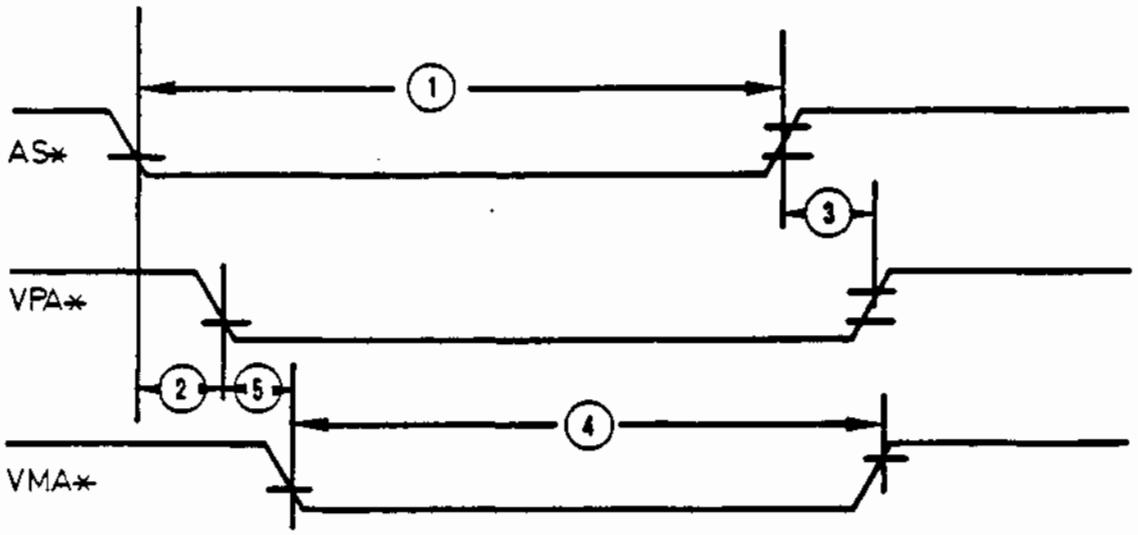


FIG. 19 ACIA TIMING DIAGRAM (best case)

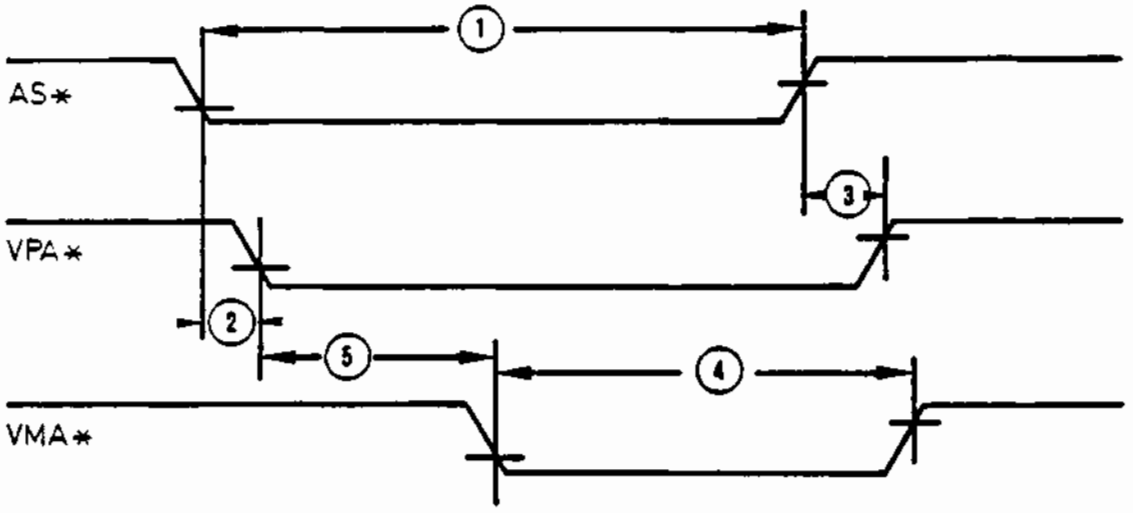


FIG. 20 ACIA TIMING DIAGRAM (worst case)

4.1.6 Serial I/O Interface Summary

Terminal

Start Address	$0C0080
End Address	$0C0082
Access Mode	Byte Only Read and Write
Usable Data Bits	D8-D15
Access Time	1000ns (min) 2000ns (max)
Interrupt Request Level	4
Interrupt Handling	fixed IRQ vector (#28) Address:$000070

Remote

Start Address	$0C0041
End Address	$0C0043
Access Mode	Byte Only Read and Write
Usable Data Bits	D0-D7
Access Time	1000ns (min) 2000ns (max)
Interrupt Request Level	3
Interrupt Handling	fixed IRQ vector (#27) Address:$00006C

HOST

Start Address	$0C0101
End Address	$0C0103
Access Mode	Byte Only Read and Write
Usable Data Bits	D0-D7
Access Time	1000ns (min) 2000ns (max)
Interrupt Request Level	2
Interrupt Handling	fixed IRQ vector (#26) Address:$000068

Table 15 RTC Write Time Values

Number	Parameter	(Note A) Min.	Max.
1	Axx valid and IACK* high to AS* low	10	
3	AS* high	30	
4	AS* low to CSRTC active	0	
5	AS* active	0	
6	AS* invalid to UDS* high	0	40
7	AS* inactive to CSRTC inactive	0	40
8	AS* low to LDS* low (WRITE)	10	130
9	AS* low to DTACK* low	1000	2000
11	AS* inactive to DTACK inactive	15	45
12	AS* active to WRITE* low	10	150
13	AS* inactive to WRITE* inactive	10	70
14	Data valid to Data Strobes active	10	
15	As* inactive to Data invalid	10	45

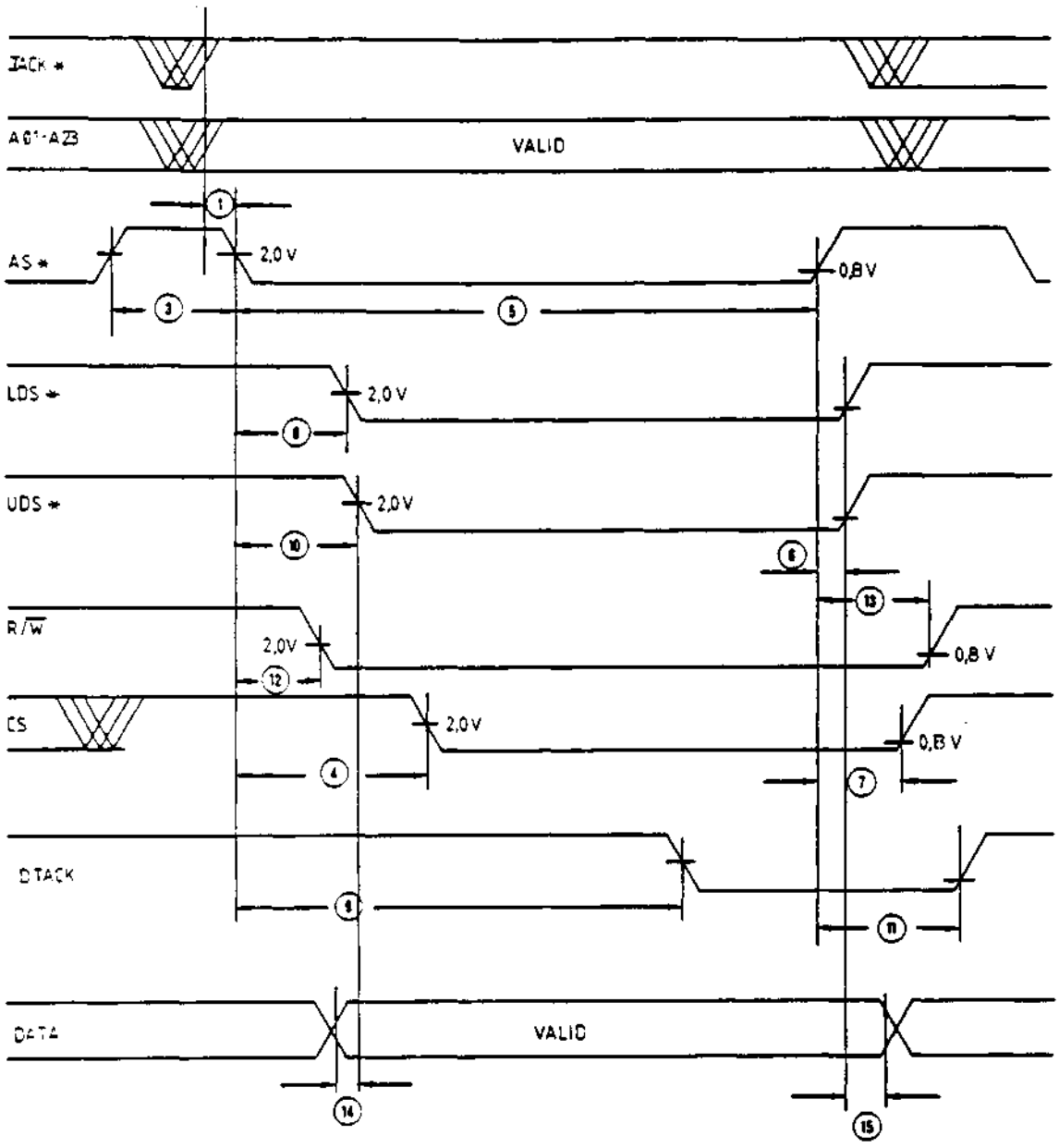


FIG. 21 RTC WRITE CYCLE TIMING DIAGRAM

Table 16 RTC Read Time Values

Number	Parameter	(Note A) Min.	Max.
1	Axx valid and IACK* high to AS* low	10	
3	AS* high	30	
4	AS* active to CSRTC low	30	60
5	AS* low	1800	2500
6	AS* inactive to UDS* inactive	10	60
7	AS* inactive to CSRTC inactive	0	40
8	AS* active to LDS* valid	10	130
9	AS* low to DTACK low	1800	2500
11	AS* inactive to DTACK inactive	15	45
12	WRITE* high to AS* active	10	
14	Data valid to DTACK active	10	
15	DTACK inactive to Data invalid	10	60

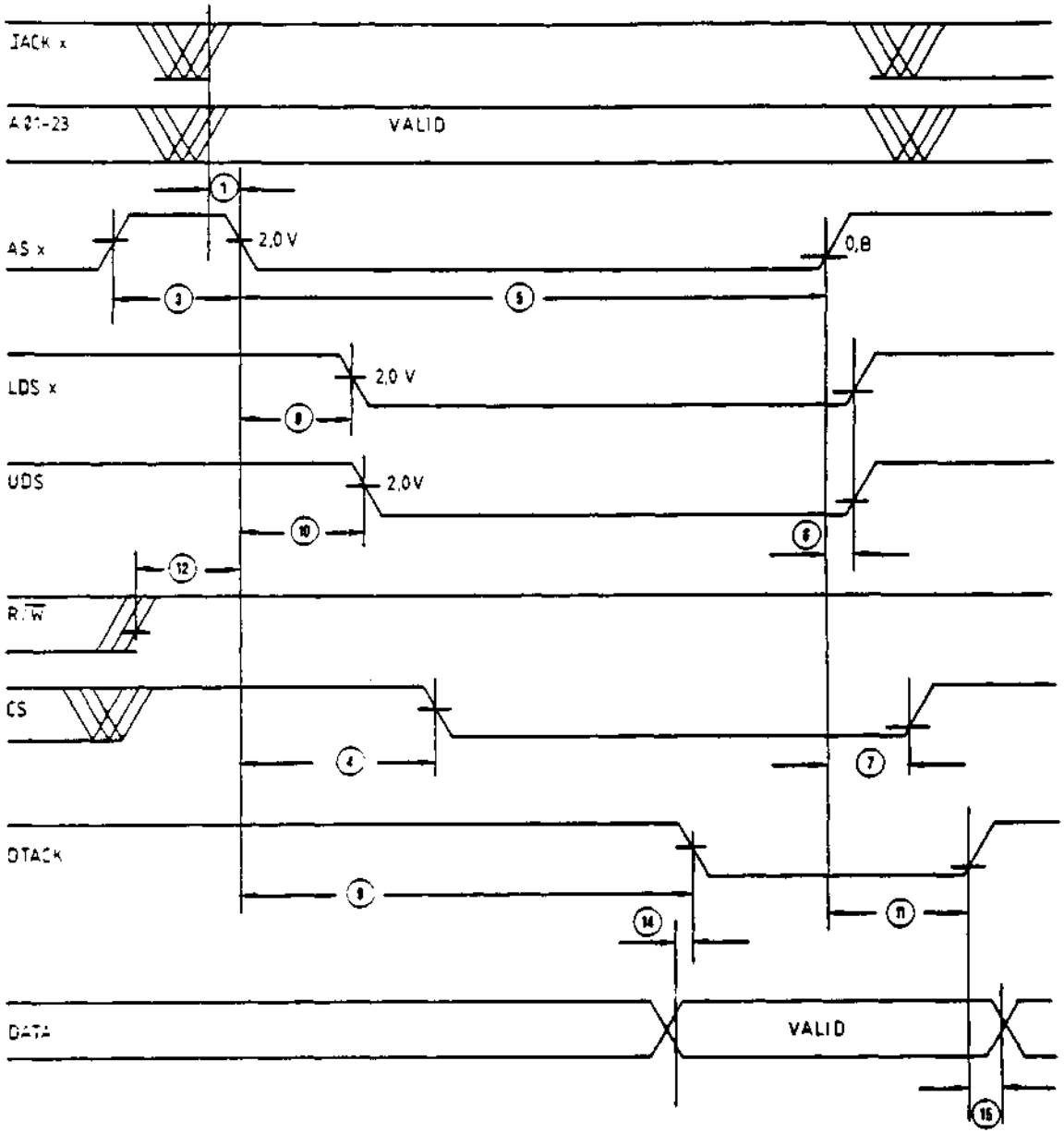


FIG. 22 RTC READ CYCLE TIMING DIAGRAM

4.2.3 The RTC Interrupt Scheme

The RTC can be used to force an interrupt to the on-board CPU. This is provided if a jumper is inserted in the jumper field B200. Otherwise, no interrupt can be forced and the interrupt request line is always disabled. The RTC interrupt request level is fixed at level 6, the highest maskable interrupt level.

The jumper location diagram of the interrupt request jumper field and the RTC circuit are shown in Figure 23.

The interrupt control logic on the board decodes the RTC Interrupt Request level (IRQ6) and forces the auto interrupt vector after the interrupt has been acknowledged on that level. This vector is fixed and reserved on the board specially for the RTC. The long word stored at address $000078 (vector no. 30) represents the RTC interrupt handling routine start address.

The RTC interrupt is enabled by default during manufacturing (jumper B200).

CAUTION: If the RTC interrupt is disabled (jumper at B200 then the interrupt must also be disabled on the chip

4.2.4 RTC Summary

Access Address	:	$0C0401 - $0C042F
Access Mode	:	Byte Mode (odd only)
Usable Data Bits	:	D0 - D7
Interrupt Level	:	6 (auto interrupt vectoring)
Interrupt Vector	:	Fixed: #30 Address: $000078

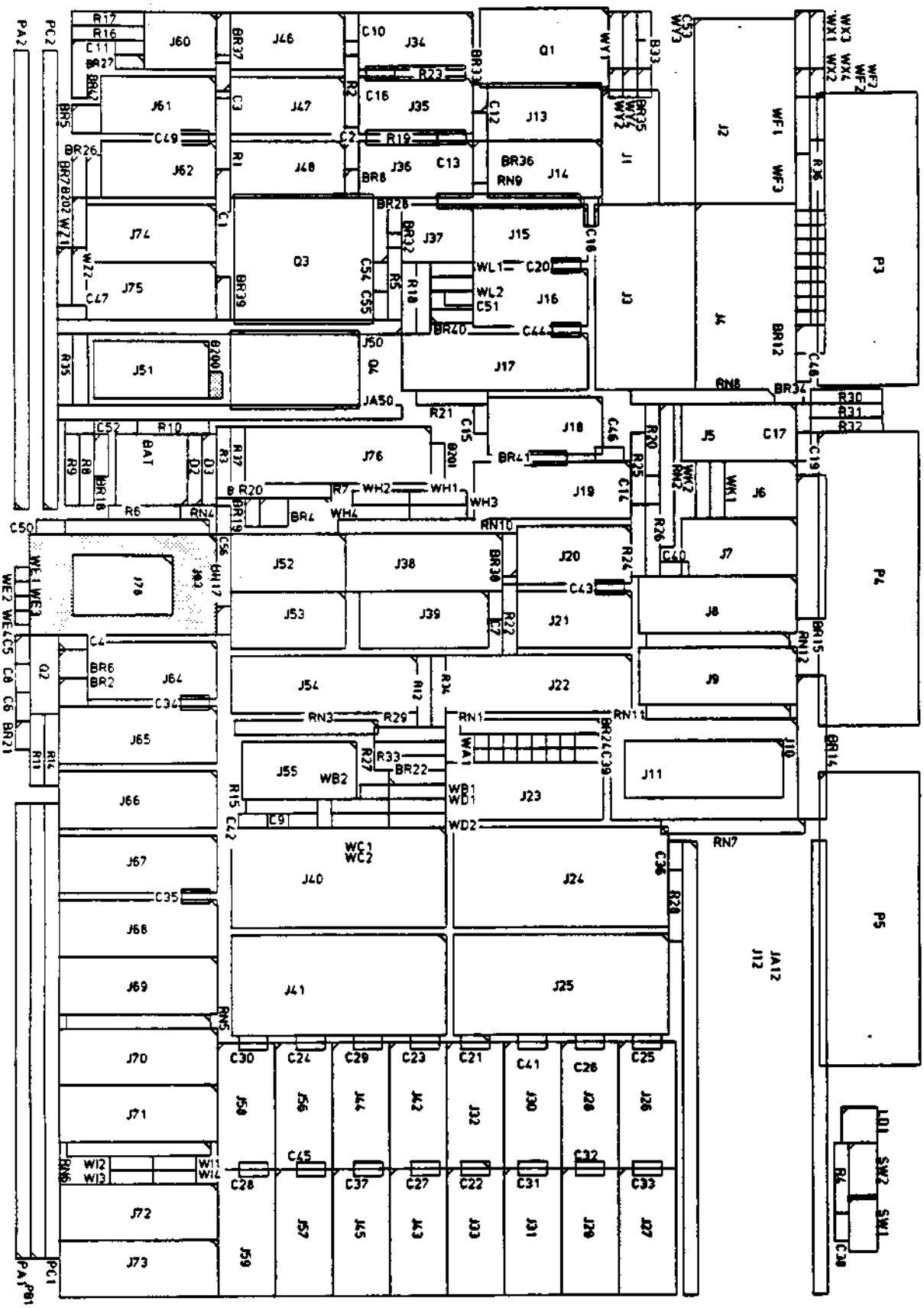


FIG. 23 LOCATION DIAGRAM OF THE RTC

4.3.1 PI/T Addressing

All of the PI/T registers are directly addressable and read/writeable as shown in Table 17.

The relative offset to the base address is $000801. Only single byte transfers to/from the PI/T on the Data bits D0-D7 are allowed (odd addresses).

The absolute access address of the first register under the default conditions during manufacturing is $F10801.

Caution: The Interrupt Vector Number Registers PIVR (address $F1080B) and TVIR (ADDRESS $0F0823) are programmable, but no interrupt vector can be forced because of the auto interrupt vectoring.

Table 17 Register Model of the PI/T

Address	Mode	Affected by Reset	Affected by Read Cycle	Descriptiption
ØE0001	R/W	Y	N	Port B Alternate Register (PBAR)
ØE0003	R/W	Y	N	Port C Data Register (PCDR)
ØE0005	R/W	Y	N	Port Status Register (PSR)
ØE0007	R/W	Y	N	Timer Control Register (TCR)
ØE0009	R/W	Y	N	Timer Interrupt Vector Register (TVIR)
ØE000B	R/W	Y	N	Counter and Preload Register High (CPRH)
ØE000D	R/W	Y	N	Counter Preload Register Middle (CPRM)
ØE000F	R/W	Y	N	Counter Preload Register Low (CPRL)
ØE0011	R/W	N	**	Count Register High (CNTRH)
ØE0013	R/W	N	**	Count Register Middle (CNTRM)
ØE0015	R	N	N	Count Register Low (CNTRL)

Table 17 Register Model of the PI/T

Address	Mode	Affected by Reset	Affected by Read Cycle	Descriptiption
ØE0017	R	N	N	Port B Alternate Register (PBAR)
ØE0019	R/W	N	N	Port C Data Register (PCDR)
ØE001B	R/W*	Y	N	Port Status Register (PSR)
ØE0021	R/W	Y	N	Timer Control Register (TCR)
ØE0023	R/W	Y	N	Timer Interrupt Vector Register (TVIR)
ØE0027	R/W	Y	N	Counter and Preload Register High (CPRH)
ØE0029	R/W	N	N	Counter Preload Register Middle (CPRM)
ØE002B	R/W	N	N	Counter Preload Register Low (CPRL)
ØE002F	R	N	N	Count Register High (CNTRH)
ØE0031	R	N	N	Count Register Middle (CNTRM)
ØE0033	R	N	N	Count Register Low (CNTRL)
ØE0035	R/W	Y	N	Timer Status Register (TSR)

* A write to this register may perform a special status resetting operation

** Mode Dependent

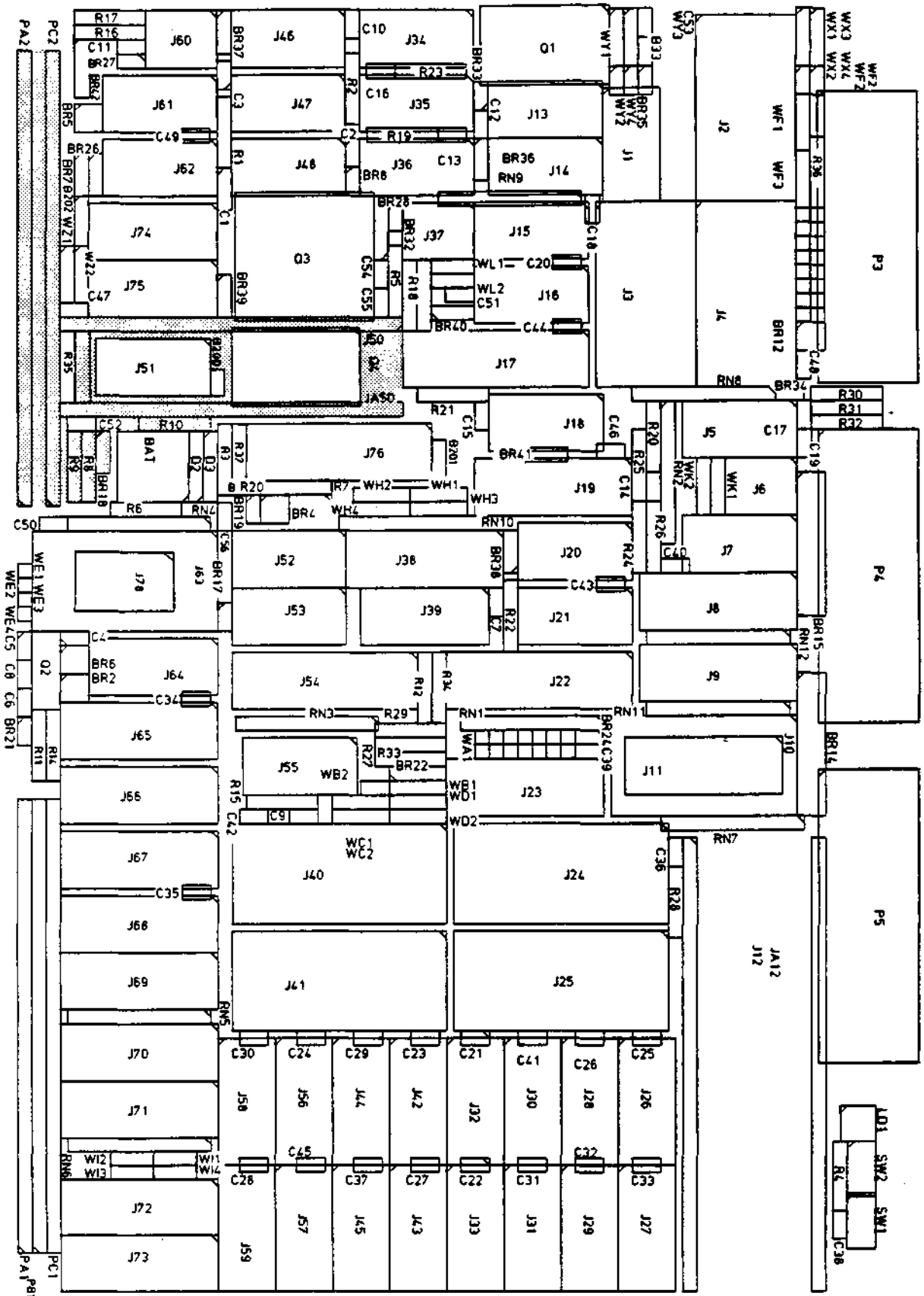


FIG. 25 LOCATION DIAGRAM OF THE PI/T PARTS

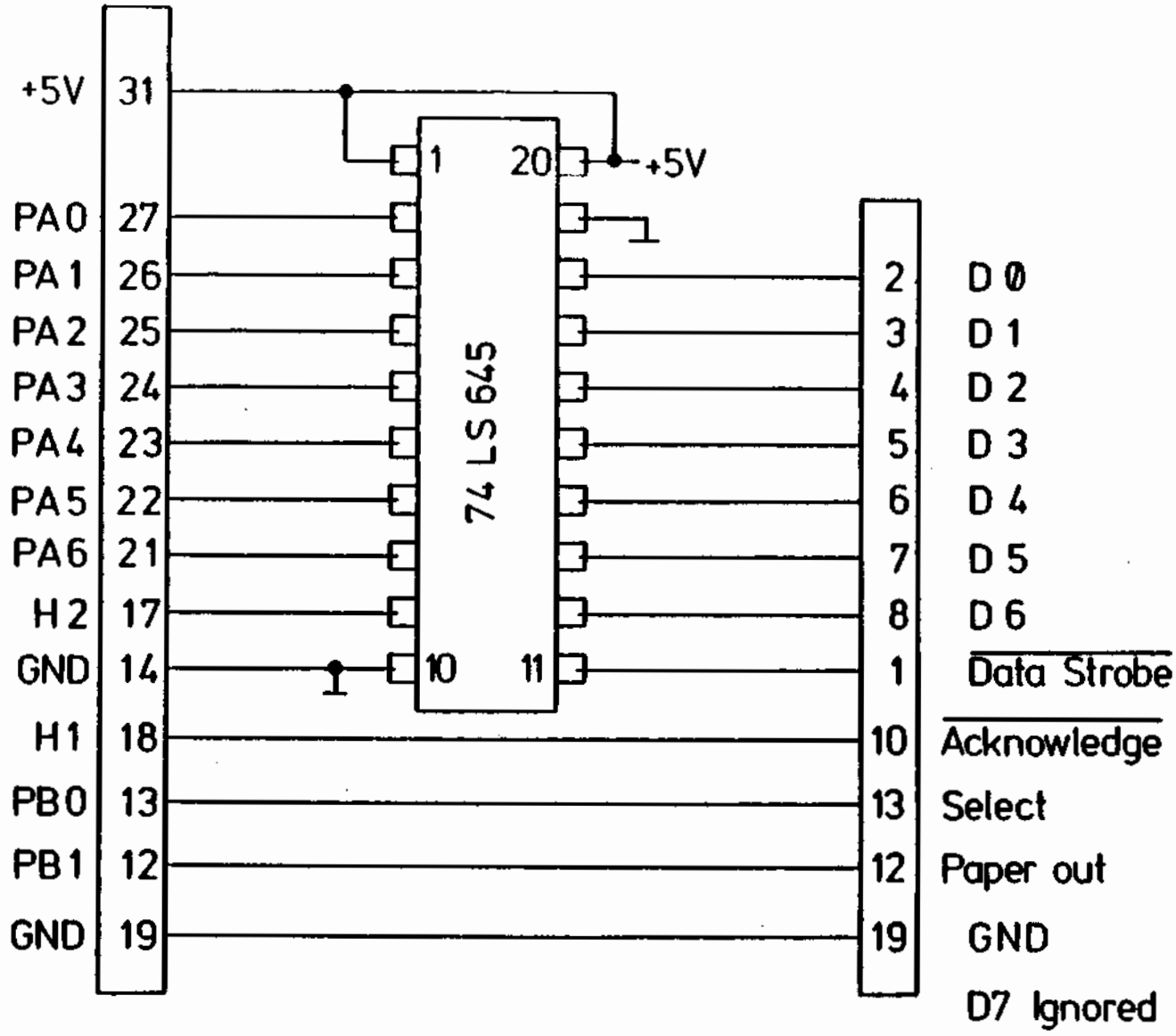


FIG. 26 THE CENTRONICS INTERFACE EXAMPLE

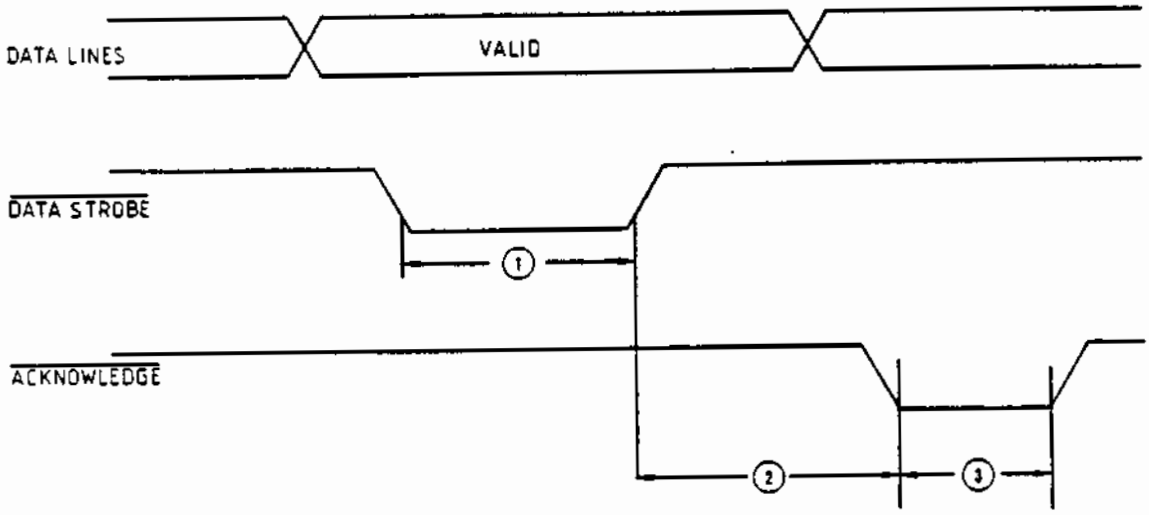


FIG. 27 TIMING DIAGRAM OF THE CENTRONICS PARALLEL INTERFACE

Time Values

No.		MIN	MAX
1	Data Strobe active	0.50 μs	
2	TOLY Delay Time	50 μs	1.0 ms
3	ACK Acknowledge Time	4 μs	50 μs

5.Ø The Interrupt Handling

The on-board CPU is able to handle 7 different prioritized interrupt request levels. The interrupt daisy-chain on the VMEbus allows an unlimited number of peripheral devices to interrupt the CPU.

Interrupt priority levels are numbered from one to seven, level seven being the highest priority. The status register contains a three bit mask which indicates the current priority of the processor. Interrupts for all priority levels less than or equal to the current processor priority are ignored.

Interrupt requests arriving at the processor do not force immediate exception processing. Pending interrupts are detected between instruction executions. If the priority of the pending interrupt request is lower than or equal to the current processor priority, the execution continues with the next instruction and no interrupt exception processing is started.

If the priority of the pending interrupt is greater than the current processor priority, then the exception processing sequence is started.

5.1 The Interrupt Exception Sequence

After the start of the interrupt exception sequence, a copy of the Status Register (SR) is saved on the stack, the privilege state of the processor is set to supervisor, and the processor priority level is set to the level of the interrupt being acknowledged.

The processor fetches the vector number from the interrupting device, classifying the reference as an interrupt acknowledge and displaying the level number of the interrupt being acknowledged on the address bus using the address signals A1, A2 and A3 as listed in Table 18.

Table 19 shows the conversion of the interrupt vector into the address under which the start address of the interrupt service routine is stored.

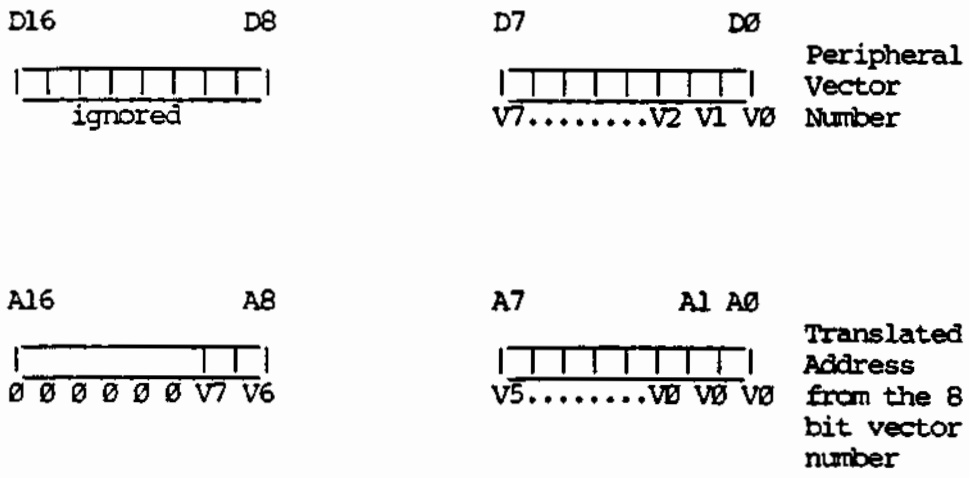
Table 18 The Interrupt Acknowledge Level Code

IRQ Level	A3	A2	A1	FC0	FC1	FC2
7	1	1	1	1	1	1
6	1	1	0	1	1	1
5	1	0	1	1	1	1
4	1	0	0	1	1	1
3	0	1	1	1	1	1
2	0	1	0	1	1	1
1	0	0	1	1	1	1
-	0	0	0	1	1	1 a)

a) Not assigned.
The content of the interrupt vector whose vector number was fetched and transleted is loaded into the program counter to start the interrupt handling routine. The normal vector Table of the CPU is given in Table 1.

The vector that was moved from the interrupting device onto the data bits D0-D7 is translated by the CPU into an address which contains the start address of the interrupt handling routine.

Table 19 The Interrupt Vector Conversion



If the external logic requests automatic vectoring, the processor generates a vector number internally,which is determined by the interrupt level number.

If external logic indicates a bus error, the interrupt is taken to be spurious, and the generated vector number is the spurious interrupt vector. The exception sequence in this case is listed in the CPU data sheet.

Table 20 lists the vector numbers for the auto interrupt scheme and the spurious interrupt.

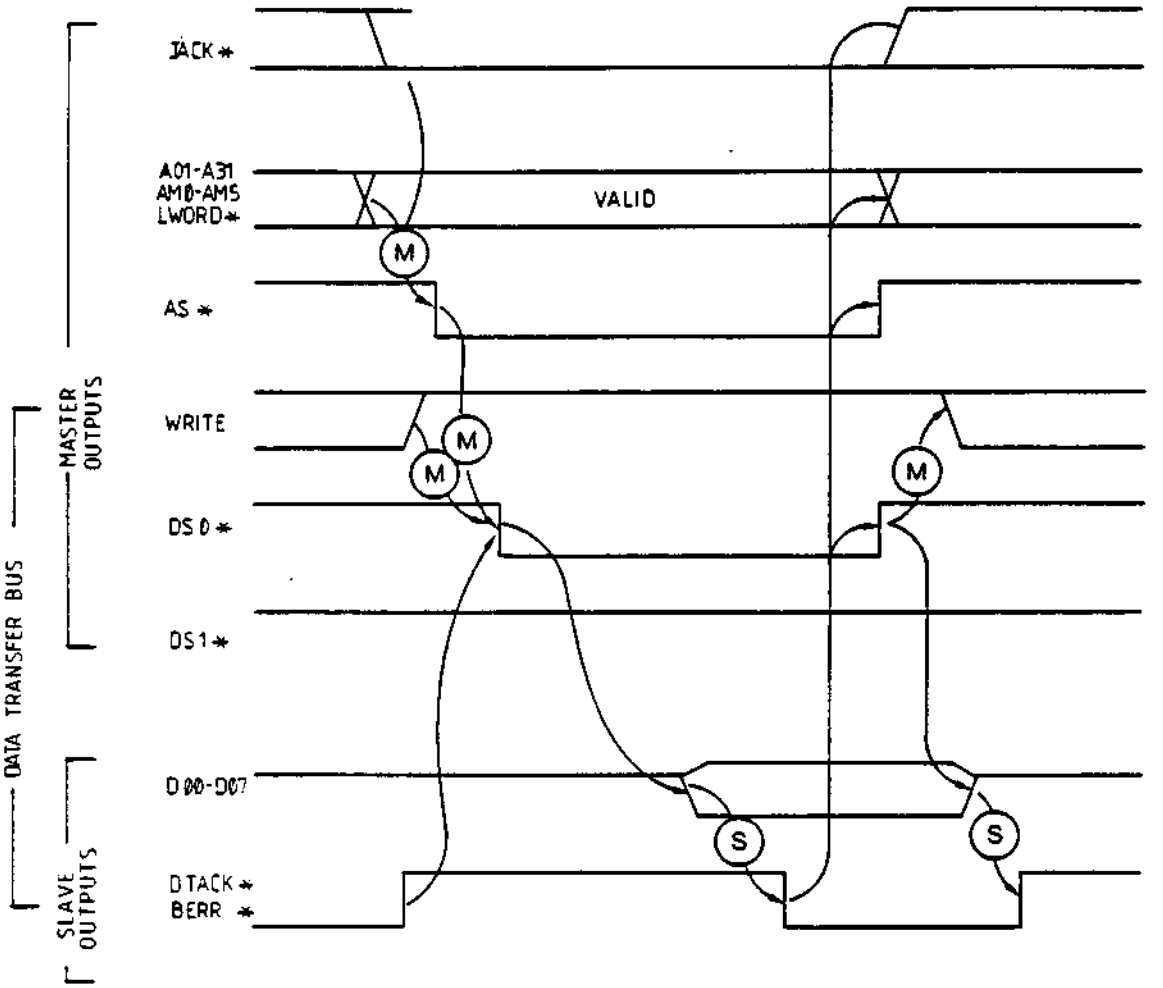
Table 20 The Auto-Interrupt Vector Table

Absolute Address	Vector Number	Corresponding Interrupt Level
$000060	# 24	Spurious Interrupt
$000064	# 25	Level 1 Interrupt Autovector
$000068	# 26	" 2 " "
$00006C	# 27	" 3 " "
$000070	# 28	" 4 " "
$000074	# 29	" 5 " "
$000078	# 30	" 6 " "
$00007C	# 31	" 7 " "

A global timing diagram of the interrupt vector acquisition is shown in Figure 28.

The priority level 7 is a special case. Level seven interrupts cannot be disabled by the interrupt priority mask. The IRQ 7 is a "non-maskable interrupt"

Caution: The level 7 interrupt may still be caused by the level comparison, if the request level is seven and the processor priority is set to a lower level by an instruction.



NOTE
The interrupt vector aquisition is only used during IRQ's from the VMEbus

FIG. 28 THE GLOBAL INTERRUPT VECTOR ACQUISITION

5.2 The On-Board Interrupt Sources

The SYS68K/CPU-1B board contains six on-board sources, the three serial I/O Controllers (ACIAs), the ABORT function switch, the Parallel Interface and the Real Time Clock.

Table 21 lists the combinations of the on-board devices and the corresponding interrupt level as well as the default set auto-interrupt vectors (if required).

Table 21 The On-Board Devices Interrupt Scheme

On-Board Device	Interrupt Level	Auto-Interrupt Vectoring	Default Vector	Address
ABORT Switch	7	YES	31	$00007C
RTC 58167A	6 a)	YES	30	$000078
PI/T 68230	5	YES	29	$000074
ACIA Terminal	4	YES	28	$000070
ACIA Remote	3	YES	27	$00006C
ACIA Host	2	YES	26	$000068
ACFAIL	6 b)	NO	30	$000078

Notes

a) These two Interrupt Request Signals (IRQ) are tied together.

b) On Request, this signal from the VMEbus can be used to generate an Interrupt.

The RTC interrupt and, if required, the ACFAIL Signal are tied together. According to the forced Auto-Interrupt Vector #30, this results in an easy software controlled interrupt scheme. The RTC includes an Interrupt Status Register which indicates the interrupt source.

5.3 The ACFAIL Interrupt Handling

The VMEbus ACFAIL signal is driven low if the main power is not in the valid voltage range or has dropped.

If an ACFAIL is detected during power-down or power-up, then an interrupt may be generated if a connection between PIN1 and PIN2 is made in the Jumper Field BR2Ø. Figure 29 outlines the Jumper Location Diagram for this jumper field. The detailed Timing Diagram of the VMEbus Power-Up/Power-Down mechanism is given in Figure 3Ø.

The ACFAIL Interrupt Scheme can be used to save critical data before the power becomes unstable. In the default conditions on the CPU-1B, the ACFAIL signal is disabled and no interrupt is forced during power failures. Therefore in the Jumper Field BR2Ø a connection between PIN2 and PIN3 is provided.

BR2Ø	Connection to
1	IRQ6
2	ACFAIL (from Receiver)
3	HALT (of 68ØØØ CPU)

If a connection between pin2 and pin3 is provided, the on-board CPU will stop all activities immediately after the ACFAIL signal has been asserted. The red HALT LED on the front panel is then lit.

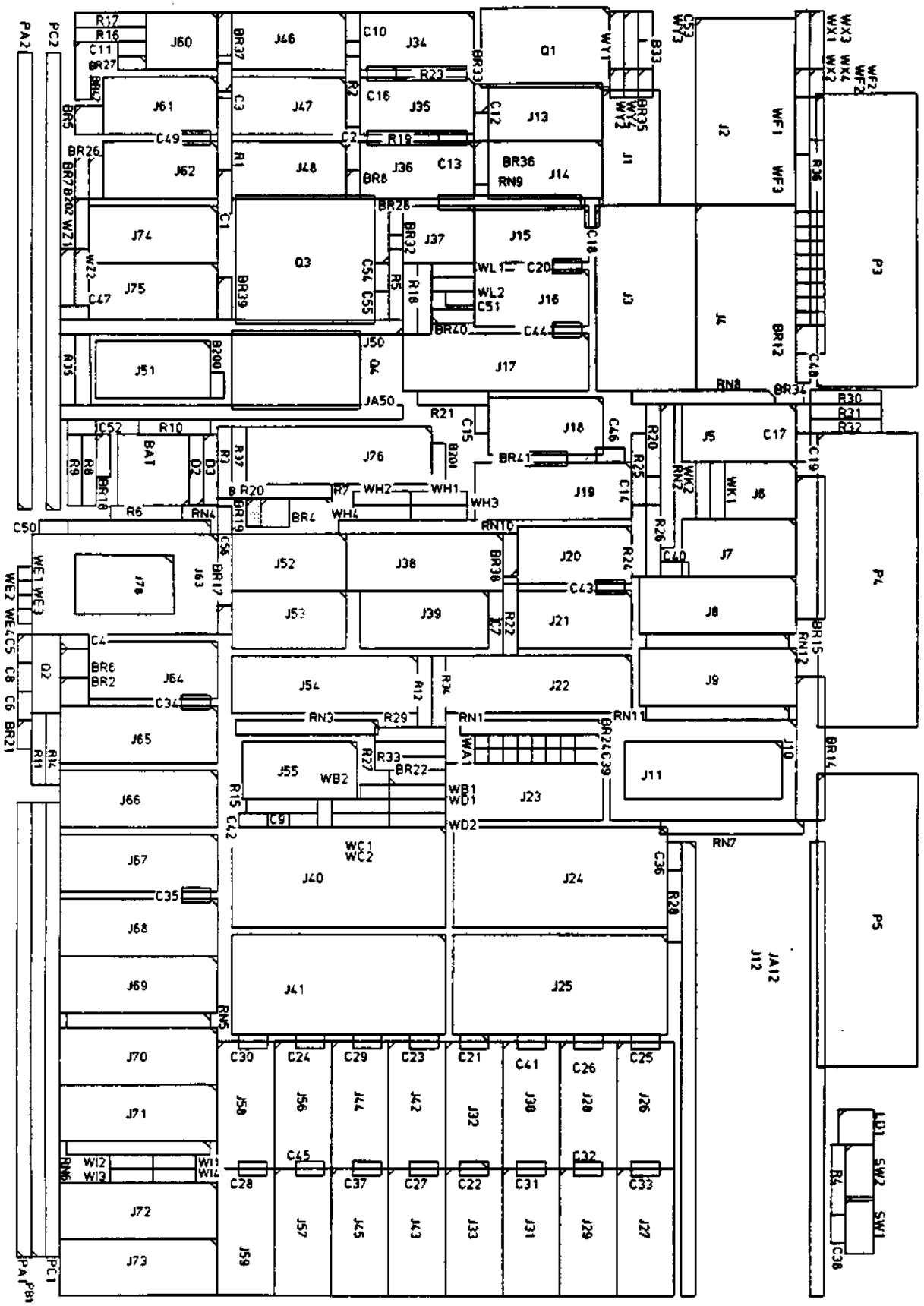


FIG. 29 LOCATION DIAGRAM OF THE ACFAIL JUMPER FIELD

5.4 The Software ABORT Function Switch

The second switch on the front panel of the SYS68K/CPU-1B is used to generate a non-maskable interrupt at level 7 to the 68000 CPU.

This interrupt forces the auto-interrupt vector (#31).

The switch can be used for debug purposes (please refer to the MONITOR User's Manual) or for self tests, if special routines are built in.

5.5 The VMEbus Interrupt Handling

All of the on-board interrupts have a higher priority in the internal interrupt acknowledge daisy chain than the VMEbus interrupts at the same interrupt level.

The VMEbus interrupt signals IRQ1-IRQ7 from the VMEbus are received continuously. A special jumper field WA1-WA7 as shown in Figure 31 (Figure 32 outlines the location diagram) is used to enable/disable each IRQ signal seperately.

Table 23 shows the combinations of the jumper settings.

An inserted jumper means that the incoming IRQ signal from the VMEbus will be acknowledged by the on-board CPU. Therefore a non-inserted jumper is equivalent to a disabled IRQ signal.

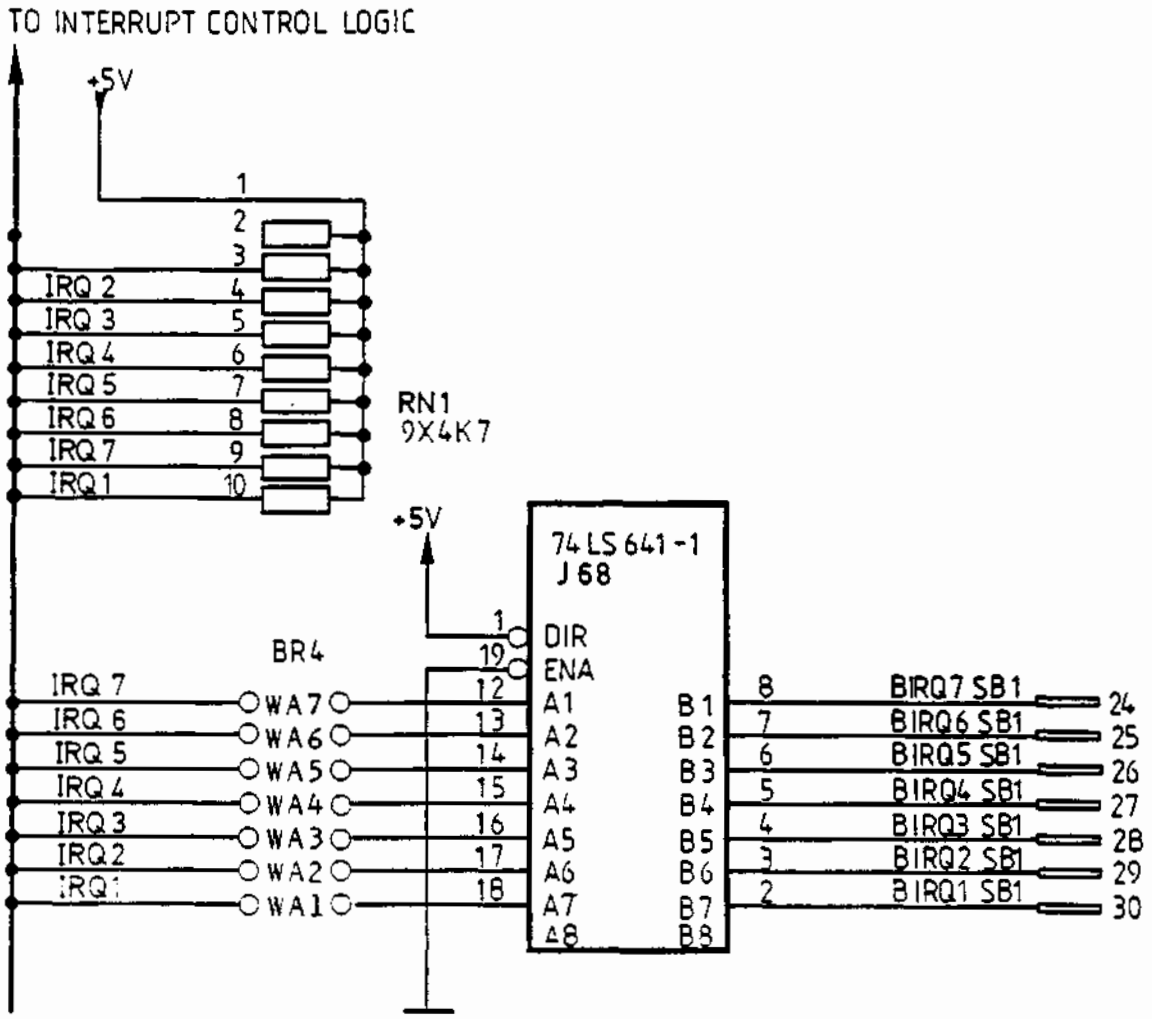


FIG. 31 THE VMEbus INTERRUPT JUMPER FIELD

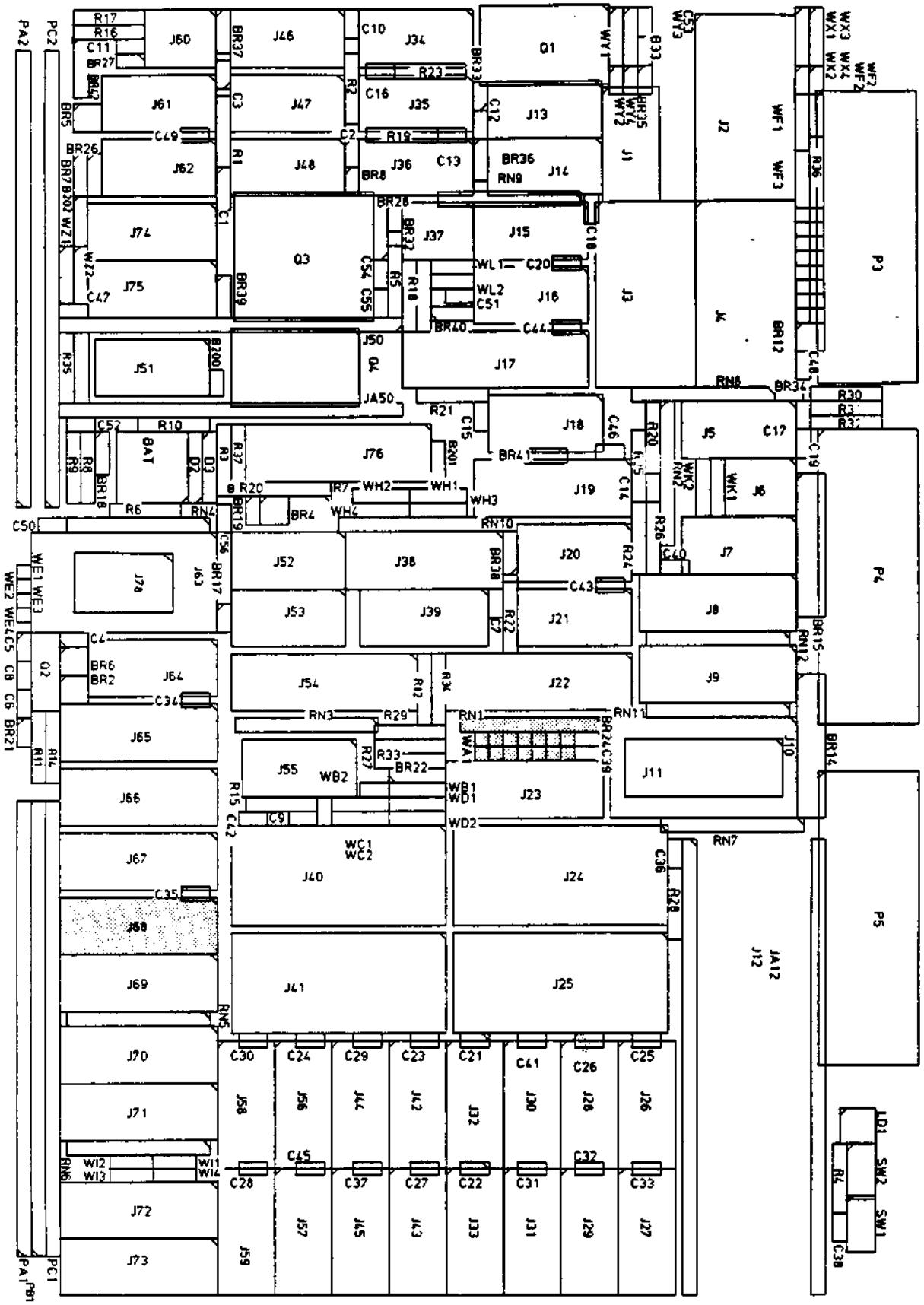


FIG. 32 LOCATION DIAGRAM OF THE VMEbus INTERRUPT PARTS

Table 23 The VMEbus Interrupt Jumper Settings

Jumper WA	Interrupt Request Level	Default Jumper Setting
WA7	IRQ7	IN
WA6	IRQ6	IN
WA5	IRQ5	IN
WA4	IRQ4	IN
WA3	IRQ3	IN
WA2	IRQ2	IN
WA1	IRQ1	IN

NA = Not Asserted

Note: In the default conditions, all IRQ signals from the VMEbus will be acknowledged by the on-board CPU.

5.5.1 the Interrupt Acknowledge Daisy Chain on the VMEbus

The VMEbus specification defines 7 interrupt request signals (IRQ1* - IRQ7*) and 3 special control signals which allow an unlimited number of interrupt sources in the system.

Each of the seven VMEbus IRQ signals may be shared by two or more interrupter modules. The Interrupt Acknowledge (IACK-) Daisy Chain is used to ensure that only one of the unlimited number of interrupt modules places its interrupt vector onto the data bits D0-D7.

An active Interrupt Acknowledge signal (IACK*) informs all of the VMEbus cards in the system that the current read cycle is an interrupt vector acquisition of the current VMEbus master. This signal is connected at slot 1 to the Interrupt Acknowledge - In signal (IACKIN*) as shown in Figure 33. The IACKIN* signal passes through each board on the VMEbus. If a board receives an active IACKIN* signal and has not produced an interrupt on the decoded IRQ level, the board control logic must bypass the IACKIN* signal through its own IACKOUT* signal to inform the next board (if it is the interrupt requester), that it can place the interrupt vector onto the data bus.

A function diagram of the Interrupt Acknowledge Daisy Chain is given in Figure 34, and a global signal timing of an Interrupt Acknowledge Cycle with an Interrupt Vector Acquisition is given in Figure 35. The related time values are given in Table 24.

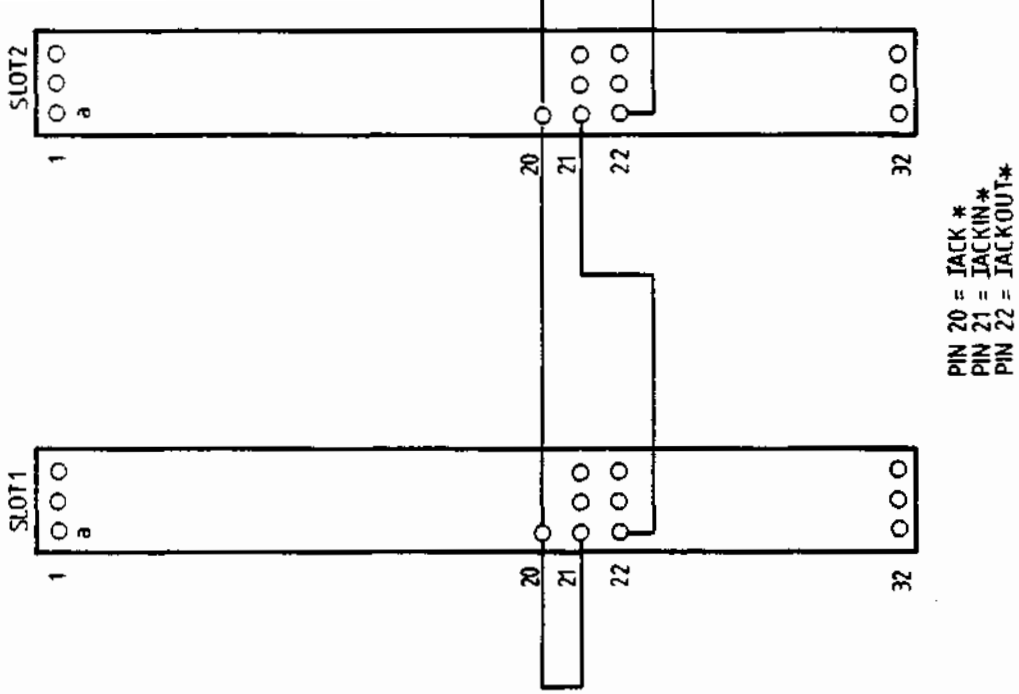
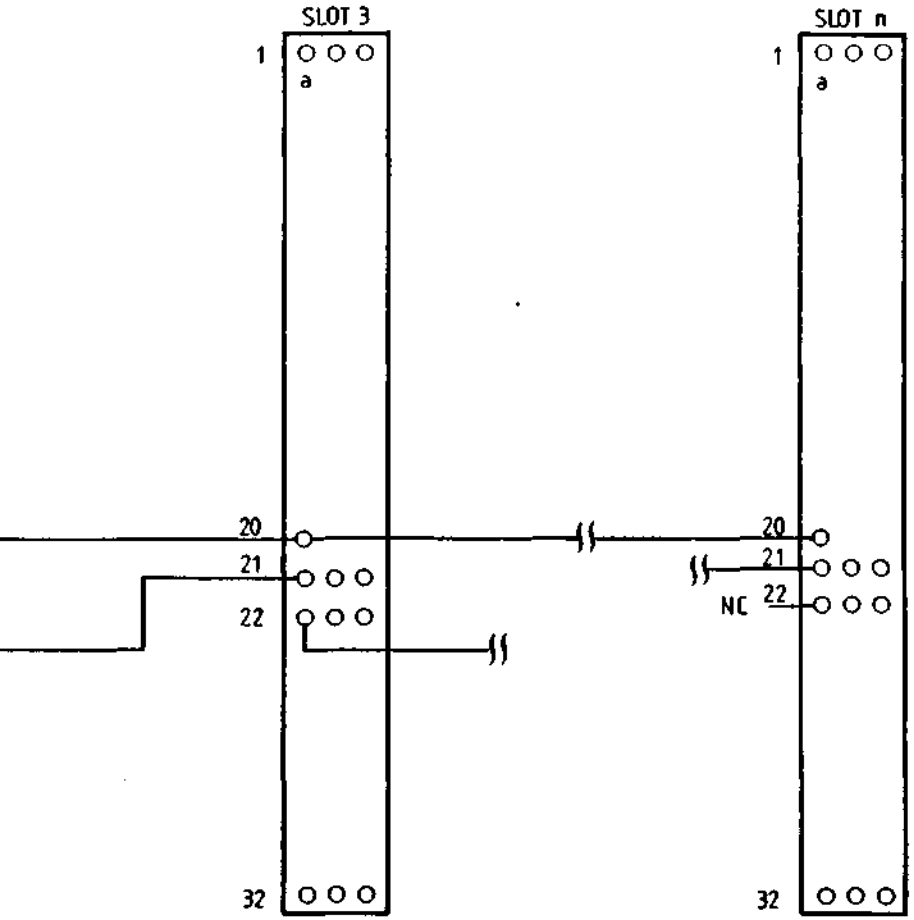


FIG. 33 THE INTERRUPT ACKNOWLEDGE DAISY CHAIN


SLOT 3
1
a
20
21
22
32
SLOT n
1
a
20
21
22
NC
32

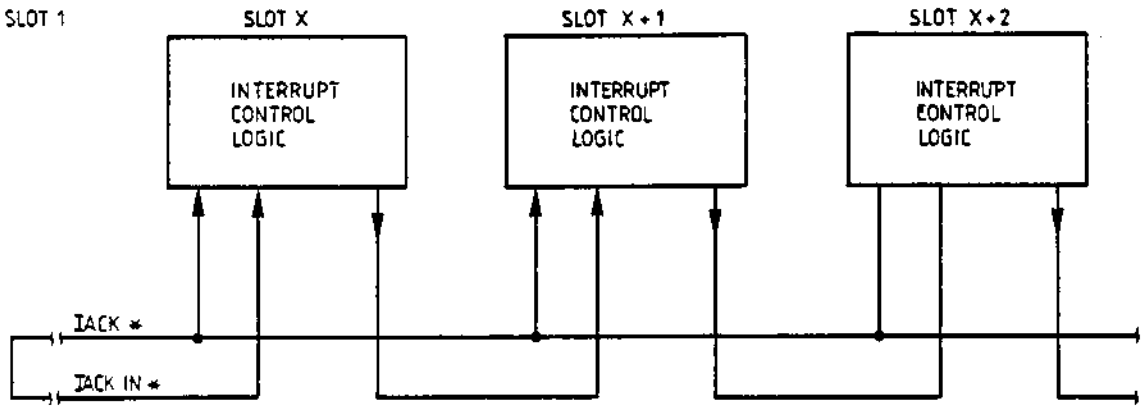


FIG. 34 FUNCTIONAL DIAGRAM OF THE INTERRUPT ACKNOWLEDGE DAISY CHAIN SCHEME

Table 24 Time Values of the Interrupt Vector Acquisition

NUMBER	PARAMETER	NOTE MIN.	NOTE MAX.	NOTES
1	Axx valid and IACK* low to AS* low	35		B
2	DTACK* low to invalid address or IACK* high	Ø		C
3	AS* high	40		B
4	DTACK* low to AS* high	Ø		C
5	AS* to DSØ* skew	Ø		B
6	WRITE* valid to DSØ* low	35		B
7	DSØ* high to invalid WRITE*	10		B
8	Data release to DTACK* high	Ø		E
9	Dxx valid to DTACK* low	-25		E
10	DTACK* low to DSØ* high	Ø		C
11	DSØ* high	40		B
12	DSØ* high to invalid data	Ø		D
13	DTACK* high to DSØ* low	Ø		C
14	DSØ* high to AS* low	30		B

NOTES:

A. All times given in nanoseconds.

B. The INTERRUPT HANDLER must guarantee this timing between two of its outgoing signal transitions.

C. The INTERRUPT HANDLER must wait for the incoming signal edge from the INTERRUPTER before changing the level of its outgoing signal.

D. This is a guarantee that the INTERRUPTER will not change the incoming signal until the INTERRUPT HANDLER changes its outgoing signal.

E. The INTERRUPT HANDLER is guaranteed this timing between two of its incoming signal transitions.

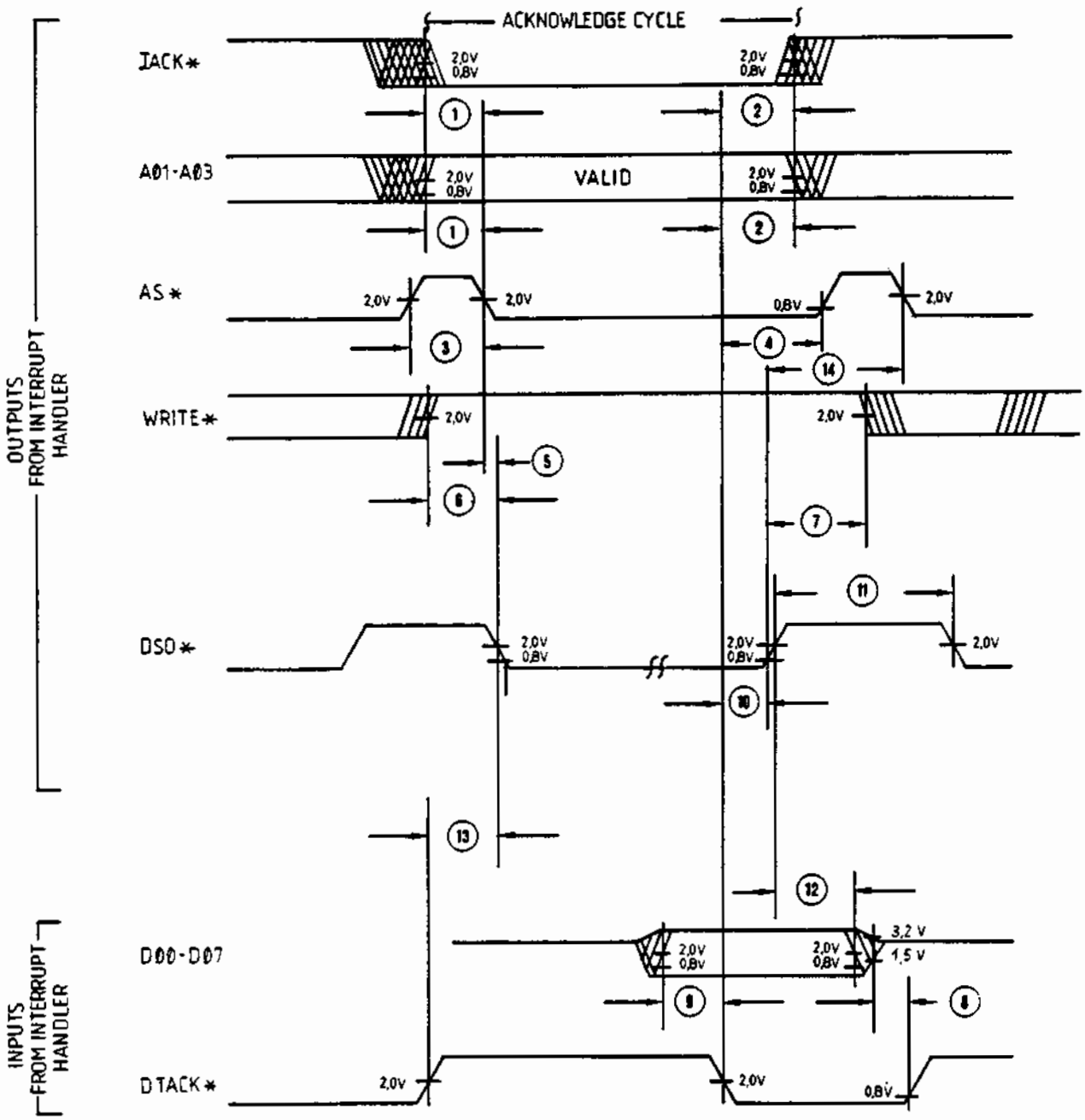


FIG. 35 THE INTERRUPT VECTOR AQUISITION TIMING DIAGRAM

5.5.2 The On-Board IACK Daisy Chain

To provide full VMEbus compatibility, the IACK* signal is driven as an output signal if the SYS68K/CPU-1B board is the current VMEbus master, and if no on-board interrupt is pending. This allows full multi-processing in high performance systems because of the transparent interrupt handling of the on-board and off-board IRQs.

The low driven IACK* signal is wired to slot one of the VME motherboards and runs down the IACK daisy-chain.

6.Ø The VMEbus Arbitration

The VMEbus is designed to allow multi-master and multi-processor application. Only the current VMEbus master is able to force read or write transfers to and from other VME modules. This requires a special handshake scheme to control which VME module receives bus mastership.

This controller module is the VMEbus Arbiter. The Arbiter resides only in slot number one of each VMEbus environment, because the bus arbitration is daisy chained from slot 1 to 2 to 3 etc. Each system has only one arbiter. The arbiter may be on a special card or it may be located on a CPU.

To provide a minimal system overhead, there are three different arbiters defined in the VMEbus specification.

a) The Four Level Bus Arbiter with a Priority Scheme

b) The Four Level Bus Arbiter with a Round Robin Scheme

c) The One Level Bus Arbiter

A global description of an arbitration scheme is given in Chapter 6.1.

6.1 The Arbiter Options

The Arbiter is used to control the DTB arbitration system. There are three options :

a) An option PRI (Priority) Arbiter always assigns the bus on a fixed priority basis where each of the four different Bus Request (BRX*) signals are assigned fixed priorities from the highest (BR3*) to the lowest (BRØ*).

b) An option RRS (Round Robin Select) Arbiter assigns the bus on a rotating priority basis. If the current DTB Master is level "n", then the highest priority will be given to level "n-1" and proceed sequentially from there.

c) An option ONE (Single Level) Arbiter only honours requests on BR3* and relies on the daisy chain structure for priority determination.

The first two arbitration types may have two types of DTB Masters, i.e.

1) Variable length bursts.

2) Variable frequency DTB requests.

When a module uses variable burst length, it adjusts the number of transfer cycles per bus grant to reduce bus overheads and get higher data throughputs. A typical example of this method is a module which contains a 40 word FIFO (First In, First Out) register. The control logic on this module requests the bus whenever eight or more words exist in the FIFO and empties the FIFO before relinquishing the DTB control.

A typical example of a variable frequency request would be a module containing a FIFO with an 80 word stage capacity. The module control logic may request the DTB control, even if 20 or more words are stored, and transfer 20 words per DTB mastership. All of these modes are described briefly in the VMEbus specifications.

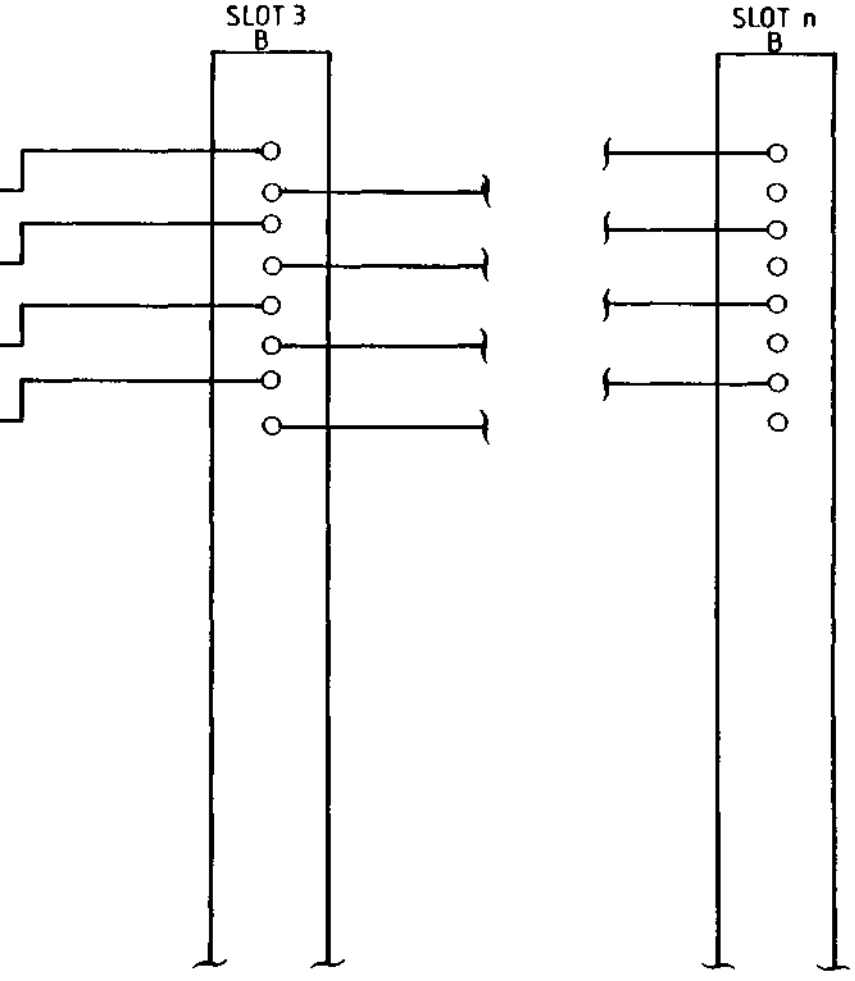
6.1.1 The Global Bus Arbiter Function

A bus arbitration scheme with a minimal overhead can be built with four signals called "BUS REQUEST*", "BUS GRANT IN/OUT*", "BUS CLEAR*" and "BUS BUSY*". The "BUS REQUEST*" (BR*) signal is driven low from a VME module to inform the Arbiter that this card wants to get the Data Transfer Bus (DTB) control. The DTB is the transport medium for data including the address, address modifier, strobe control and acknowledge signals.

If the Arbiter reacts to the BR* signal and another card is the current bus master a "BUS CLEAR" (BCLR*) signal may be generated. This BCLR* signal informs the current bus master that the DTB control must be released. After release, the "BUS BUSY" signal is inactive. The Arbiter can start the Bus Grant Daisy Chain (BGDC). The global BGDC on a motherboard is outlined in Figure 36. The DTB Arbiter forces a BUS GRANT OUT (BGxOUT*) signal on the level 0-3 equivalent to the Bus Request Level. This Bus Grant signal is the BGxIN* signal of the next slot and informs this board that it can become Bus Master if it has requested the DTB control on the same level. If this board has not requested the DTB control, it must bypass the BGxIN* signal to the next slot, etc. If the DTB requester receives the correct BGxIN* signal, it acquires the DTB control with a low driven BUS BUSY (BBSY*) signal.

After the arbitration logic has acquired the DTB control, the Bus Request signal must be disactivated to inform the Arbiter that the DTB acquisition is finished. The global timing diagram of a DTB arbitration scheme is shown in Figure 37.

FIG. 36 THE BUS GRAND DAISY CHAIN


SLOT 3
B
SLOT n
B

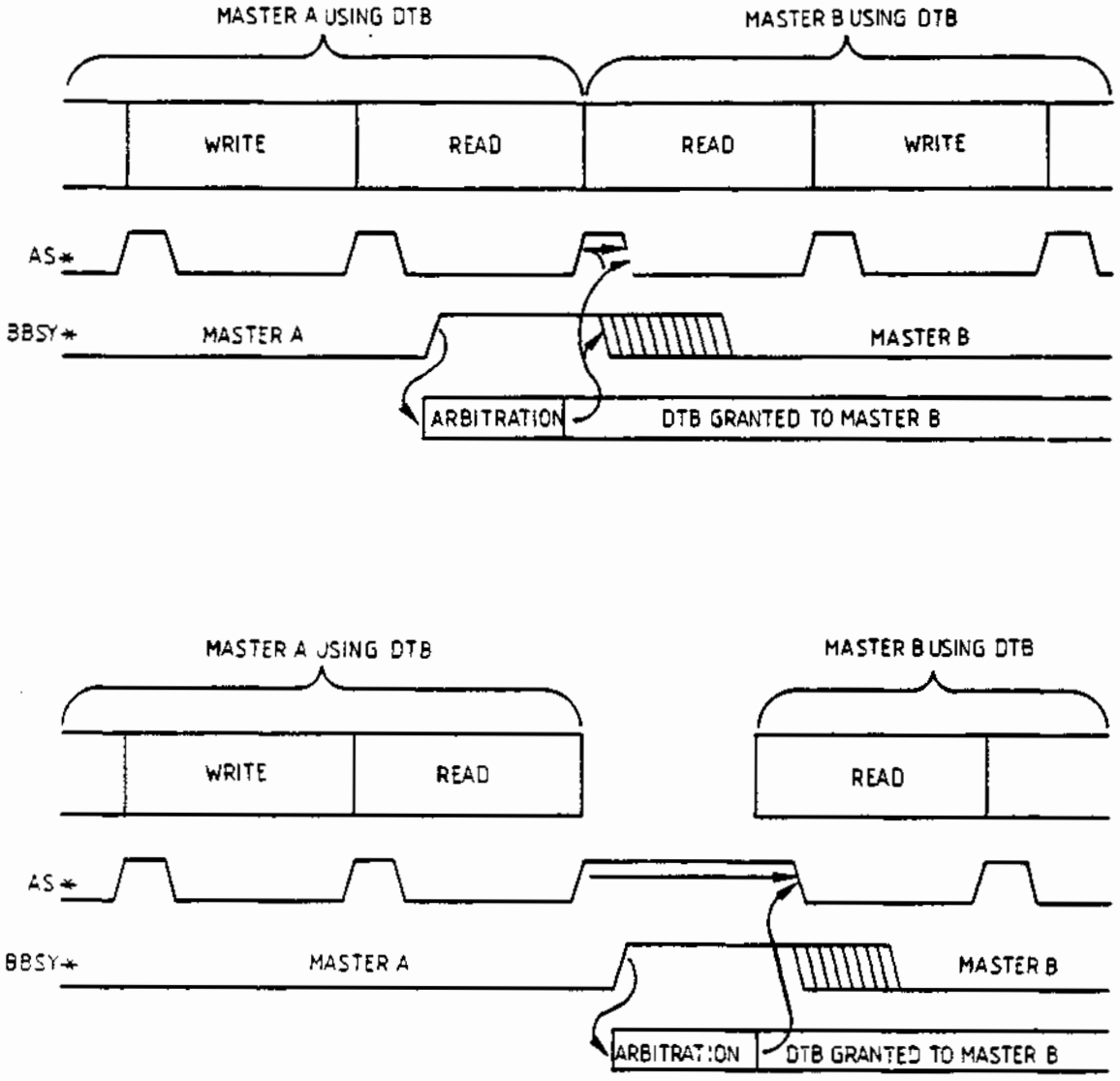


FIG. 37 GLOBAL DTB ARBITRATION TIMING

6.2 The On-Board DTB Slave Bus Arbitration

A full DTB slave arbitration is provided on the board to allow the usage of the SYS68K/CPU-1B in multi-master and multi-processor environments. The board control logic generates a Bus Request (BRx*) on a selectable level (Ø-3) if an off-board transfer is initiated and the board is not the current DTB master.

After a received BGIN* signal at the equivalent level, the control logic drives the BBSY* signal low to inform the Bus Arbiter that the arbitration is completed, and releases its Bus Request signal.

Figure 38 outlines the BRx*, BGxIN* and BGxOUT jumper fields and Figure 39 shows the location diagram.

The Bus Request level and the Bus Grant level must be equal for proper operation. The default Bus Request level during manufacturing is 3. Therefore, the connections to be made are as listed in Table 25.

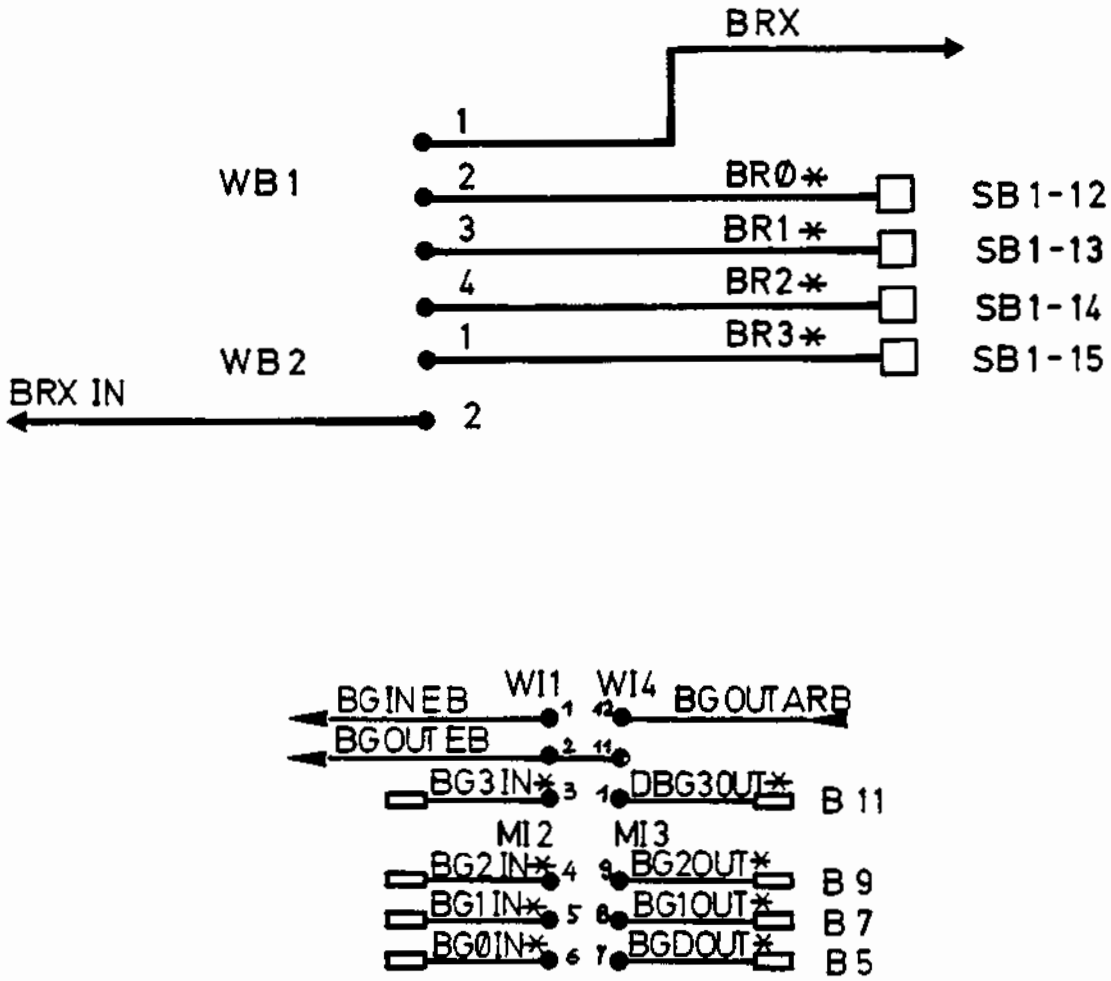


FIG. 38 THE JUMPER FIELDS FOR THE SLAVE BUS ARBITRATION

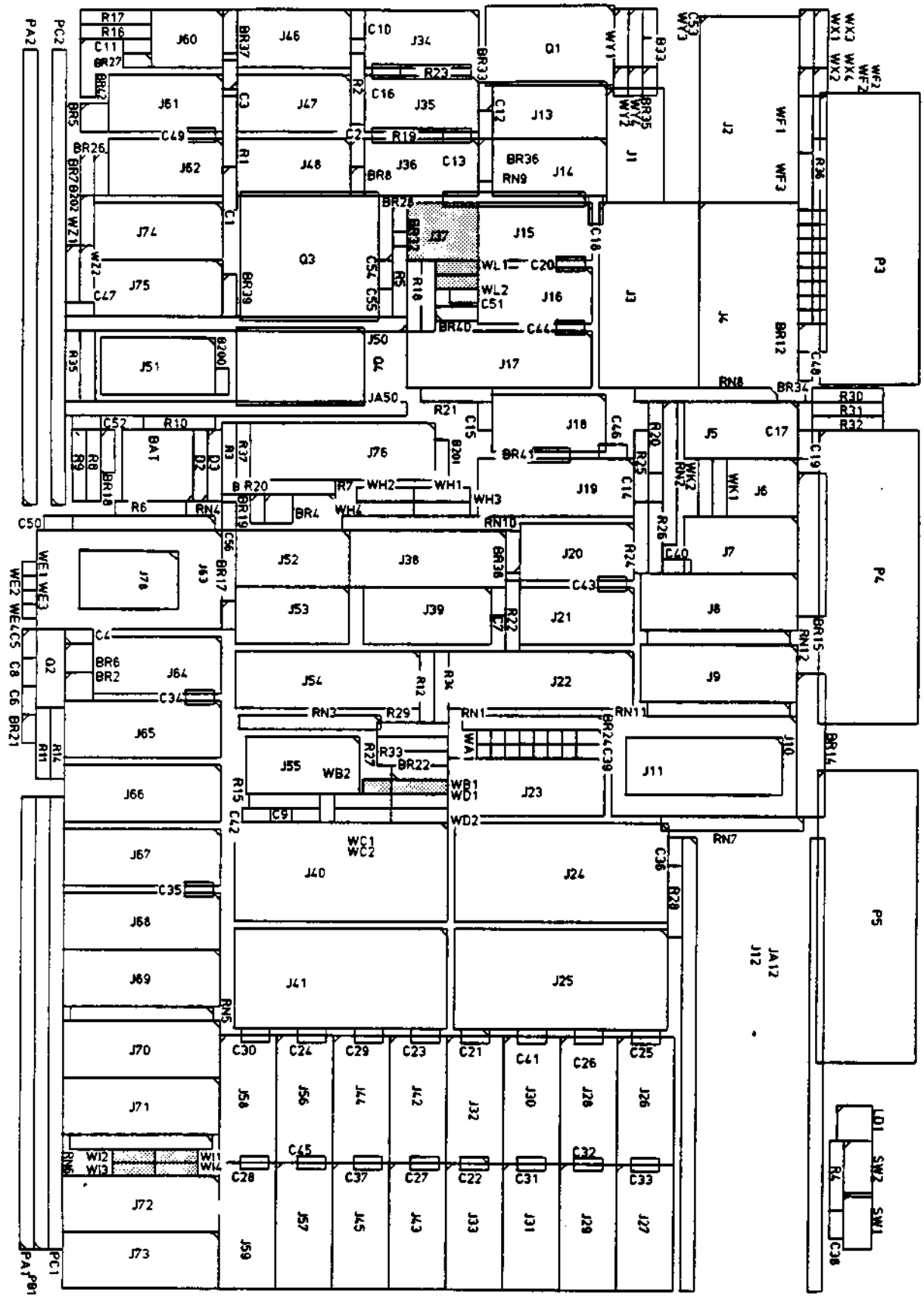


FIG. 39 THE LOCATION DIAGRAM OF THE SLAVE BUS ARBITRATION

Table 25 The Slave Bus Arbitration Default Connections

Connections between:

WI1 PIN 1 AND WI4 PIN 1

WI1 PIN 2 AND WI1 PIN 3

WB1 PIN 1 AND WB2 PIN 1

WB2 PIN 1 AND WB2 PIN 2

In a four level bus arbitration scheme with an external Arbiter, the different bus request levels require the following connections:

BRØ* : WB1-1 to WB1-2

WI1-1 to WI2-6

WI1-2 to WI3-7

BR1* : WB1-1 to WB1-3

WI1-1 to WI2-5

WI1-2 to WI3-8

BR2* : WB1-1 to WB1-4

WI1-1 to WI2-4

WI1-2 to WI3-9

BR3* : WB1-1 to WB2-1

WI1-1 to WI1-3

WI1-2 to WI4-1Ø

6.3 The Bus-Release Functions

Two different release functions are defined in the VMEbus specifications :

RWD Release When Done

ROR Release On Request

The SYS68K/CPU-1B contains the ROR function as well as a RAT (Release after Time-Out) function.

The maximum contiguous time available for the bus master state is defined by jumper settings at the jumper fields WL1 and WL2 (BR32 must be closed).

Time Out (typ)	Connection between	
30 Us	WL1-1	WL2-1
60 Us	WL1-2	WL2-2
300 Us	WL1-3	WL2-3

If the WL2 pin 1 is directly connected to high level (+5V), then every transfer on the VMEbus causes an arbitration cycle.

The jumper location diagram of the Time-Out counter is given in Fig.39.

The detailed timing diagram of an arbitration cycle is outlined in Fig.40. Table 26 lists the time values.

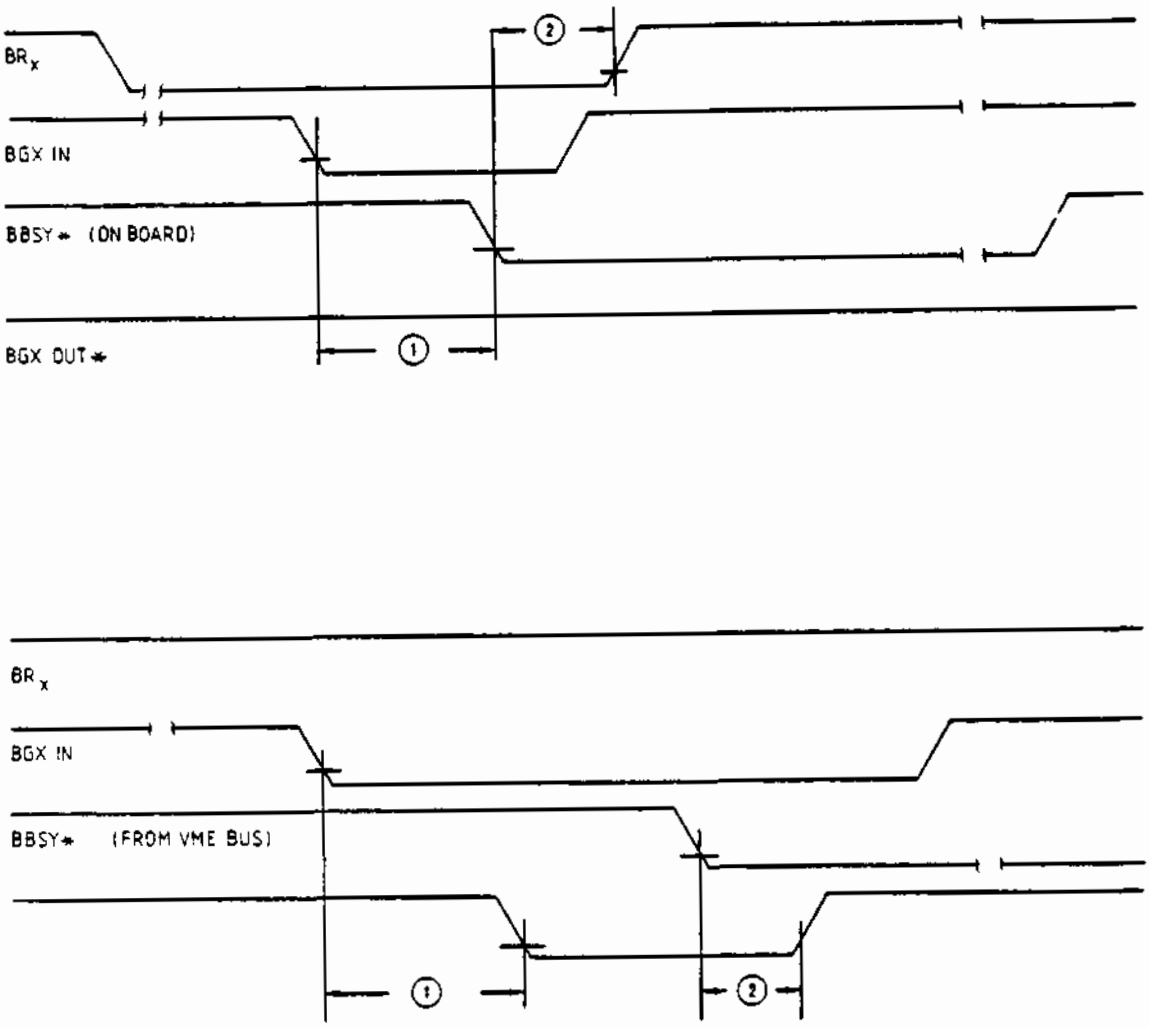


FIG. 40 BUS ARBITRATION TIMING DIAGRAM

Table 26 Time Values of the Slave Bus Arbitration

No.	Description	Min.	Max.
1	BGXIN* low to BBSY* active	25	65
2	BBSY* low to BRX active	10	65
3	BBSY* low to BGOUT* inactive	10	45
4	BGXIN* low to BGXOUT* low	35	50

NOTE : All times given in nanoseconds.

6.4 The Single Level Bus Arbiter

The SYS68K/CPU-1B board contains a Single Level Bus Arbiter for multi-master environments.

The timing diagram of the on-board single level bus arbiter is shown in Figure 41.

Table 28 lists the time values.

In the default condition during manufacturing, the board is configured to use the on-board single level Bus Arbiter. This requires the following connections:

Table 27 The One Level Bus Arbiter Option

Required Connections:

WI1-1 to WI4-16

WB1-1 to WB2-1

Table 28 Time Values of the Single Level Bus Arbiter

No.	Description	Min.	Max.
1	BR3* active to AS* inactive	10	-
2	AS* high to BGOUTARBITER	25	55

NOTE : All times given in nanoseconds.

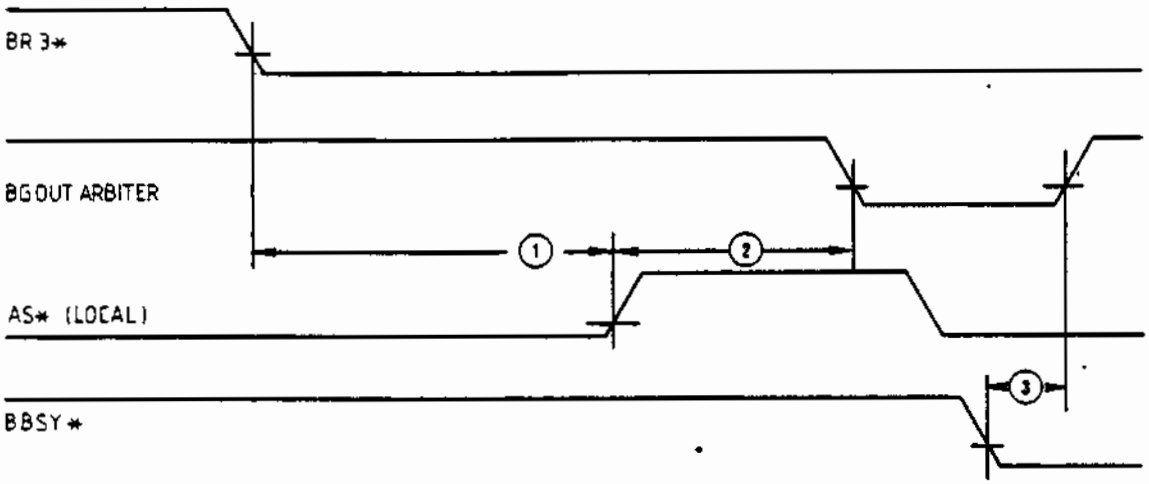


FIG. 41 TIMING DIAGRAM OF THE ONE LEVEL BUS ARBITER

6.5 The VMEbus Interface

If this board is the current VMEbus master (low driven BBSY* signal) and the current access address is higher or equal to $100.000, then a VMEbus transfer is initiated. Figures 42 and 43 show the detailed timing diagrams of a read cycle and a write cycle. Tables 29 and 30 list all of the time values.

Table 29 Read Cycle followed by Write Cycle

NUMBER	PARAMETER	NOTE MIN.	NOTE MAX.	NOTES
1	Axx and AMx valid and IACK* high to AS* low	35		B
2	DTACK* low to invalid address or IACK* low	0		C
3	AS* high	40		B
4	DTACK* low to AS* high	0		C
5	AS* to DS"A"* skew	0		B
6	WRITE* valid to DS"A"* low	35		B
7	DS"B"* high to invalid WRITE*	10		B
8	DTACK* high to active data bus	0		C
9	Dxx valid to DS"A"* low	35		B
10	DTACK* low to invalid data	0		C
11	DS"A"* to DS"B"* skew	0	10	B
12	DTACK*/BERR* low to DS"A"* high	0		C
13	DS"A"* high	40		B
14	DS"B"* high to DS"A"* low	40		B
15	DS"B"* high	40		B
16	DS"B"* high to DTACK* high	0		D
17	DTACK*/BERR* low to DS"B"* high	0		C

NOTES:

A. All times given in nanoseconds.

B. The MASTER must guarantee this timing between two of its outgoing signal transitions.

C. The MASTER must wait for the incoming signal edge from the SLAVE before changing the level of its outgoing signal.

D. This is a guarantee that the SLAVE will not change the incoming signal until the SLAVE changes its outgoing signal.

E. The MASTER is guaranteed this timing between two of its incoming signal transitions.

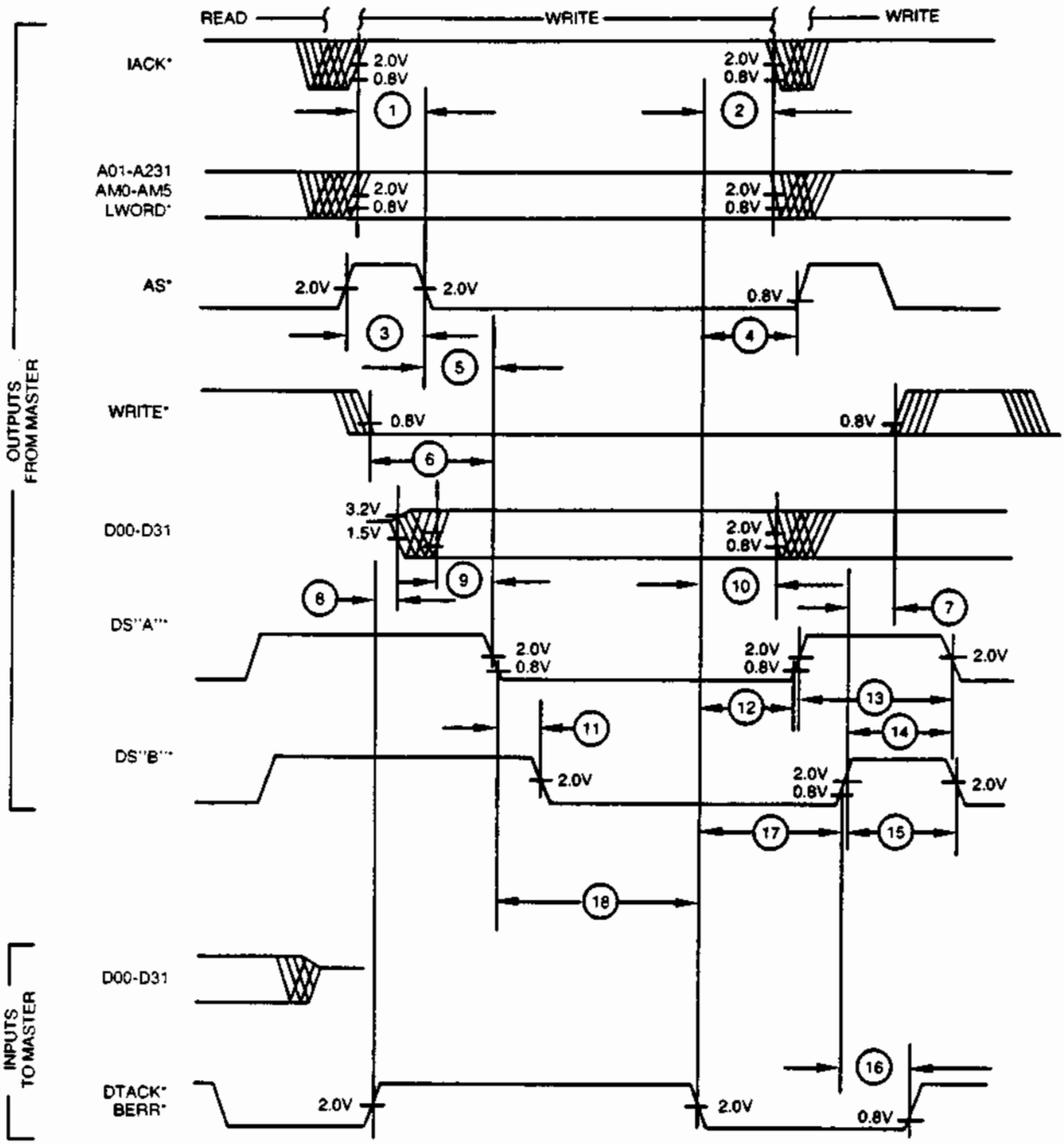


FIG. 42 READ CYCLE FOLLOWED BY WRITE CYCLE

Table 30 Write Cycle followed by Read Cycle

NUMBER	PARAMETER	NOTE MIN.	NOTE MAX.	NOTES
1	Axx and AMx valid and IACK* high to AS* low	35		B
2	DTACK* low to invalid address or IACK* low	Ø		C
3	AS* high	40		B
4	DTACK* low to AS* high	Ø		C
5	AS* to DS"A"* skew	Ø		B
6	WRITE* valid to DS"A"* low	35		B
7	DS"B"* high to invalid WRITE*	10		B
8	Data release to DS"A" low	Ø		B
9	DS"A"* to DS"B" skew		10	B
10	DTACK* low to DS"A"* high	Ø		C
11	DS"A"* high	40		B
12	DS"B"* high to DS"A" low	40		B
13	DTACK*/BERR* high to DS"A"* low	Ø		C
14	DTACK* low to DS"B"* high	Ø		C
15	DS"A"* high to invalid data	Ø		D
16	DS"B"* high	40		B
17	Dxx valid to DTACK* low	-25		E
18	Data released to DTACK*/BERR* high	Ø		E
17	DS"B"* high to DTACK*/BERR* high	30		B

NOTES:

A. All times given in nanoseconds.
B. The MASTER must guarantee this timing between two of its outgoing signal transitions.
C. The MASTER must wait for the incoming signal edge from the SLAVE before changing the level of its outgoing signal.
D. This is a guarantee that the SLAVE will not change the incoming signal until the MASTER changes its outgoing signal.
E. The MASTER is guaranteed this timing between two of its incoming signal transitions.

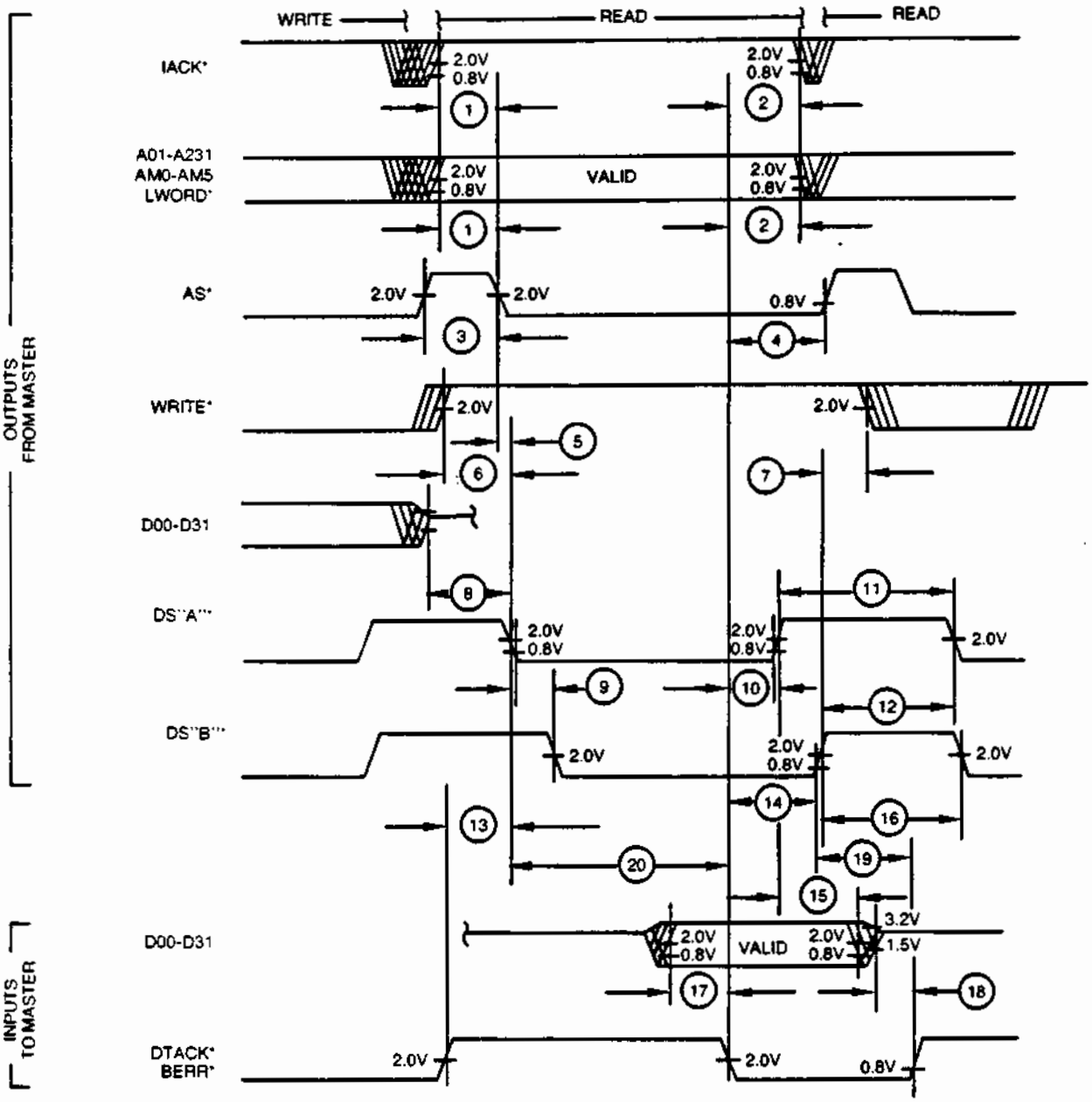


FIG. 43 WRITE CYCLE FOLLOWED BY READ CYCLE

6.6 The SYSCLK* Signal

A 74S241 driver has been installed (J65) to provide the 16MHz SYSCLK* VMEbus signal

For multimaster/multiprocessor environments, the SYSCLK driver can be disabled to the VMEbus via a jumper on position BR21.

Jumper Inserted	Driving SYSCLK signal
No Jumper	No SYSCLK signal

Fig.44 outlines the locations diagram for the jumper field BR21.

6.7 The SYSRESET* Signal

Jumper field BR2 defines whether the board drives, receives or ignores the VMEbus SYSRESET* signal.

Table 31 lists all permitted jumper settings and the corresponding modes.

Table 31 The SYSRESET* Jumper Settings

BR2 connection between	Description
1-2 , 3-4	Receiving SYSRESET*
1-3 , 2-4	Driving SYSRESET* (Default cond.)
No connection	SYSRESET* ignored

Figure 44 outlines the Location Diagram of the SYSRESET Jumper Field

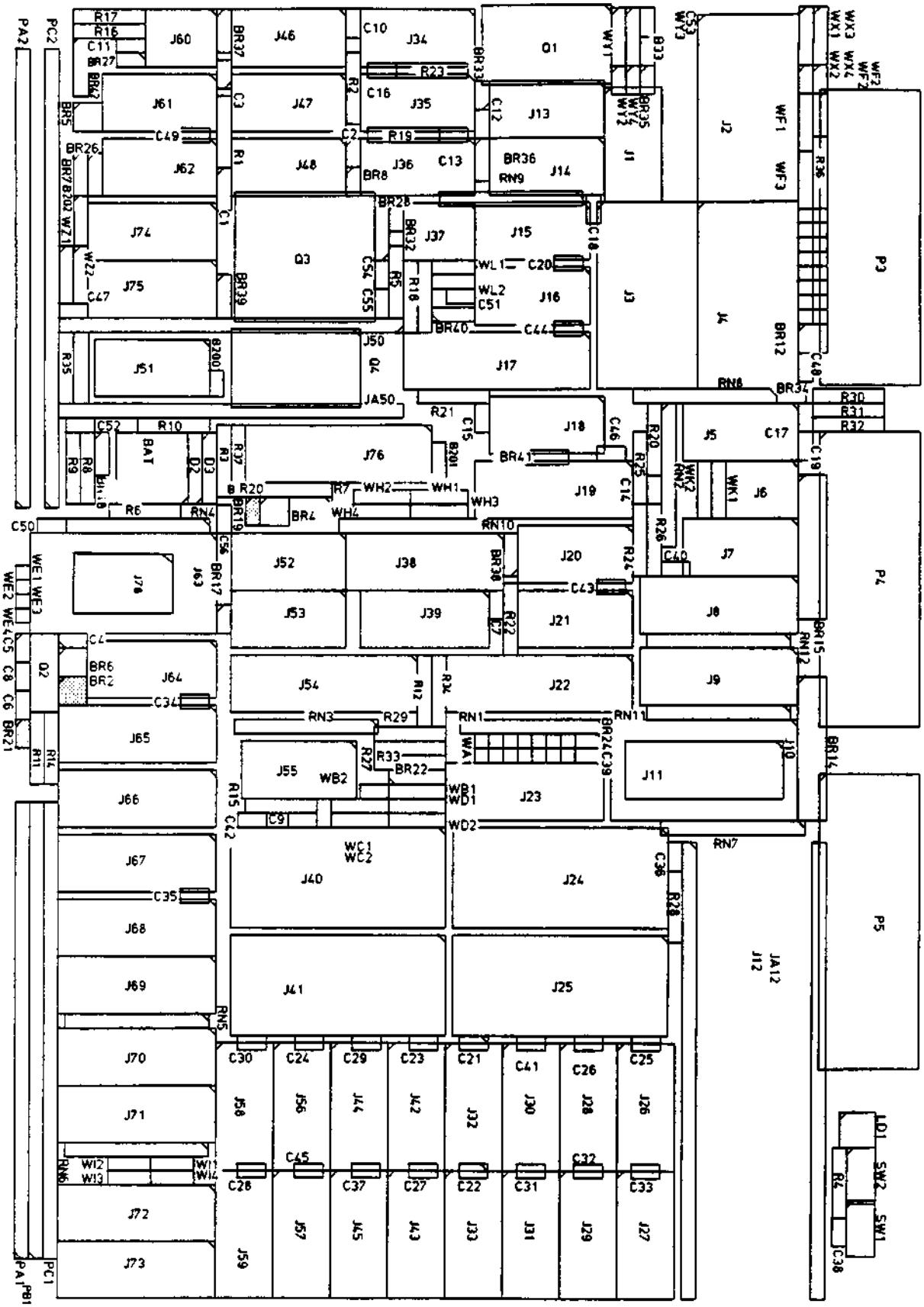


FIG. 44 LOCATION DIAGRAM OF THE SPECIAL HANDLING SIGNALS

6.8 The RESET Function Switch

The first switch on the front panel (see Fig.45) can be used to force a RESET of all of the on-board devices (CPU,PI/T, ACIA, RTC). Chapter 6.7 describes the VMEbus SYSRESET* jumper setting signal.

In the default condition the internal RESET signal is used to force the SYSRESET* signal. This allows a general RESET of all peripheral boards and devices in the system.

6.9 The SYSFAIL* Signal

The VMEbus specification defines a SYSFAIL* signal which informs all cards that one (or more) card in the complete system has failed.

This signal is directly connected to the jumper field BR19, for easy installation.

If a jumper is installed at this position and the SYSFAIL signal has been activated, then the 68000 CPU jumps directly into the HALT state. In this case, the red HALT LED on the front panel is lit.

If no jumper has been inserted, then the SYSFAIL* signal is ignored.

6.10 The Address Modifier Codes

The VMEbus defines the address modifier signal, which in turn defines which access type is under execution.

Table 32 lists the Address Modifier Codes.

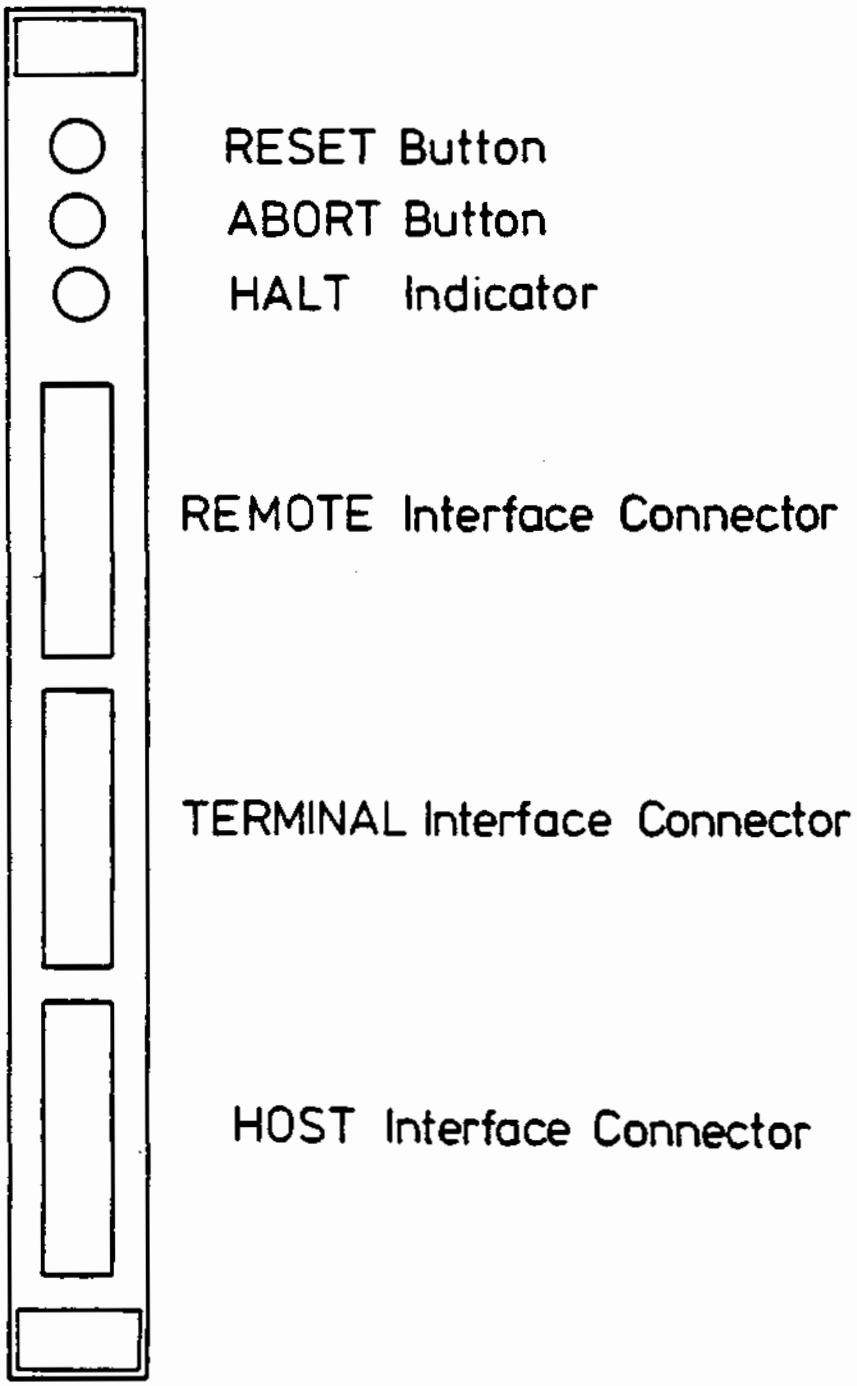


FIG. 45 THE FRONT PANEL ON THE SYS68K/CPU-1B

HEXADECIMAL CODE	ADDRESS MODIFIER 5	4	3	2	1	0	FUNCTION	DEFINED BY
3F	H	H	H	H	H	H	Standard Supervisory Ascending Access	VMEbus Spec.
3E	H	H	H	H	H	L	Standard Supervisory Program Access	VMEbus Spec.
3D	H	H	H	H	L	H	Standard Supervisory Data Access	VMEbus Spec.
3C	H	H	H	H	L	L	Undefined	Reserved
3B	H	H	H	L	H	H	Standard Non-Privileged Ascending Access	VMEbus Spec.
3A	H	H	H	L	H	L	Standard Non-Privileged Program Access	VMEbus Spec.
39	H	H	H	L	L	H	Standard Non-Privileged Data Access	VMEbus Spec.
38	H	H	H	L	L	L	Undefined	Reserved
30–37	H	H	L	X	X	X	Undefined	Reserved
2F	H	L	H	H	H	H	Undefined	Reserved
2E	H	L	H	H	H	L	Undefined	Reserved
2D	H	L	H	H	L	H	Short Supervisory I/O Access	VMEbus Spec.
2C	H	L	H	H	L	L	Undefined	Reserved
2B	H	L	H	L	H	H	Undefined	Reserved
2A	H	L	H	L	H	L	Undefined	Reserved
29	H	L	H	L	L	H	Short Non-Privileged I/O Access	VMEbus Spec.
28	H	L	H	L	L	L	Undefined	Reserved
20–27	H	L	L	X	X	X	Undefined	Reserved
10–1F	L	H	X	X	X	X	Undefined	User
0F	L	L	H	H	H	H	Extended Supervisory Ascending Access	VMEbus Spec.
0E	L	L	H	H	H	L	Extended Supervisory Program Access	VMEbus Spec.
0D	L	L	H	H	L	H	Extended Supervisory Data Access	VMEbus Spec.
0C	L	L	H	H	L	L	Undefined	Reserved
0B	L	L	H	L	H	H	Extended Non-Privileged Ascending Access	VMEbus Spec.
0A	L	L	H	L	H	L	Extended Non-Privileged Program Access	VMEbus Spec.
09	L	L	H	L	L	H	Extended Non-Privileged Data Access	VMEbus Spec.
08	L	L	H	L	L	L	Undefined	Reserved
00–07	L	L	L	X	x	X	Undefined	Reserved

Table 32 The Address Modifier Codes

6.10.1 The Function Codes

The 68000 CPU contains 3 function code signals which indicate the state of the processor (USER ot SUPERVISOR mode) and the cycle type currently being executed (PROGRAM or DATA access).

The next table lists all the states and types of the 68000 CPU.

The CPU Function Codes

FC2	FC1	FC0	CYCLE TYPE
LOW	LOW	LOW	Reserved
LOW	LOW	HIGH	User Data
LOW	HIGH	LOW	User Program
LOW	HIGH	HIGH	Reserved
HIGH	LOW	LOW	Reserved
HIGH	LOW	HIGH	Supervisor Data
HIGH	HIGH	LOW	Supervisor Program
HIGH	HIGH	HIGH	Interrupt Acknowledge

6.10.2 The Short I/O Address Modifier Code

To select a 16K byte range out of the on-board 68000 CPU's 16M byte address space, an address comparator IC (J38) is used on the board.

This 16K byte range is jumper selectable in the range from $100.000 to $FFFFFF. The jumper fields WH1, WH2, WH3 and WH4 are used to define the address range.

Fig.46 outlines the AM4 decoder in detail.

For valid decoding, the following jumper settings are possible:

OUT means that the corresponding address signal must be high (1)

IN means that the corresponding address signal must be low (0)

Table 33 lists the jumper positions and the corresponding address signals as well as the jumper settings in the default conditions during manufacturing.

Fig.47 outlines the location diagram of the Short I/O parts.

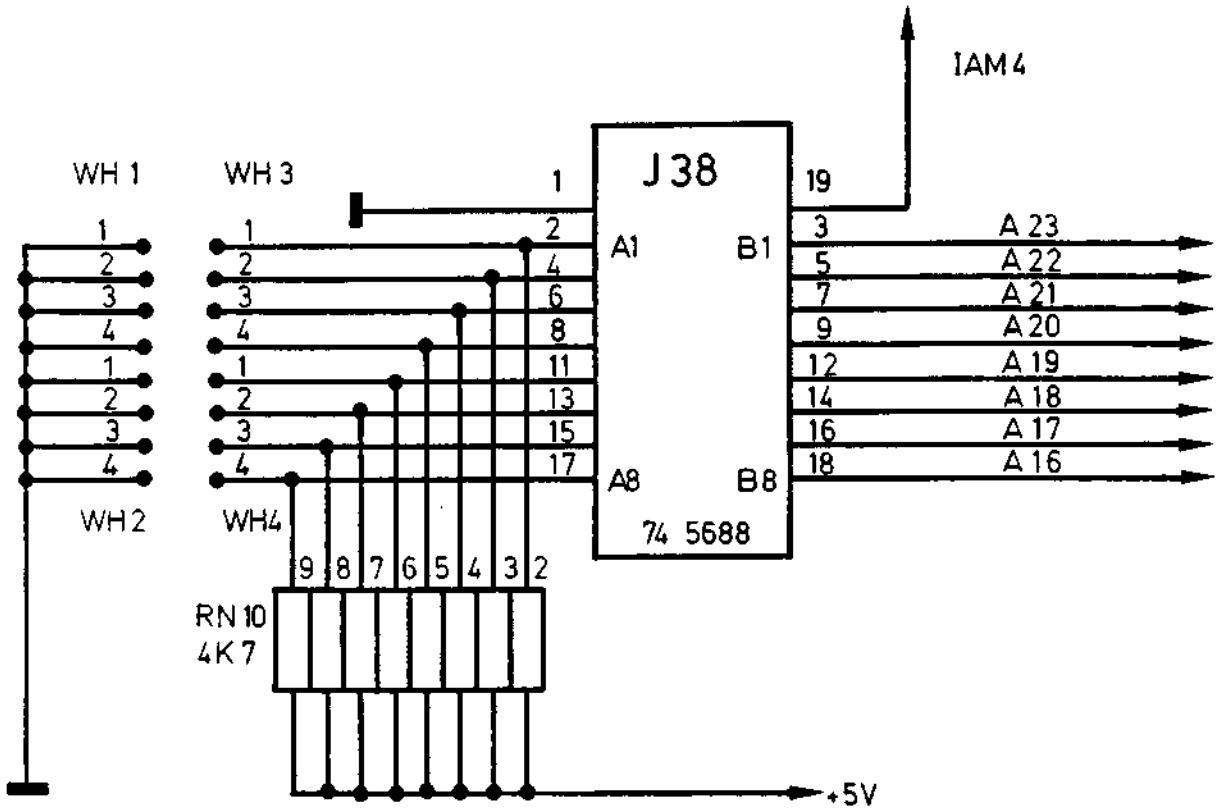


FIG. 46 THE SHORT I/O COMPARATOR

Table 33 The Short I/O Jumper Settings

Jumper Positions	Corresponding Address Signal	Default Jumper Setting
WH1-1 / WH3-1	A23	OUT
WH1-2 / WH3-2	A23	OUT
WH1-3 / WH3-3	A23	OUT
WH1-4 / WH3-4	A23	OUT
WH2-1 / WH4-1	A23	OUT
WH2-2 / WH4-2	A23	OUT
WH2-3 / WH4-3	A23	OUT
WH2-4 / WH4-4	A23	OUT

Start Address Short I/O	$ FF0000
End Address Short I/O	$ FFFFFF

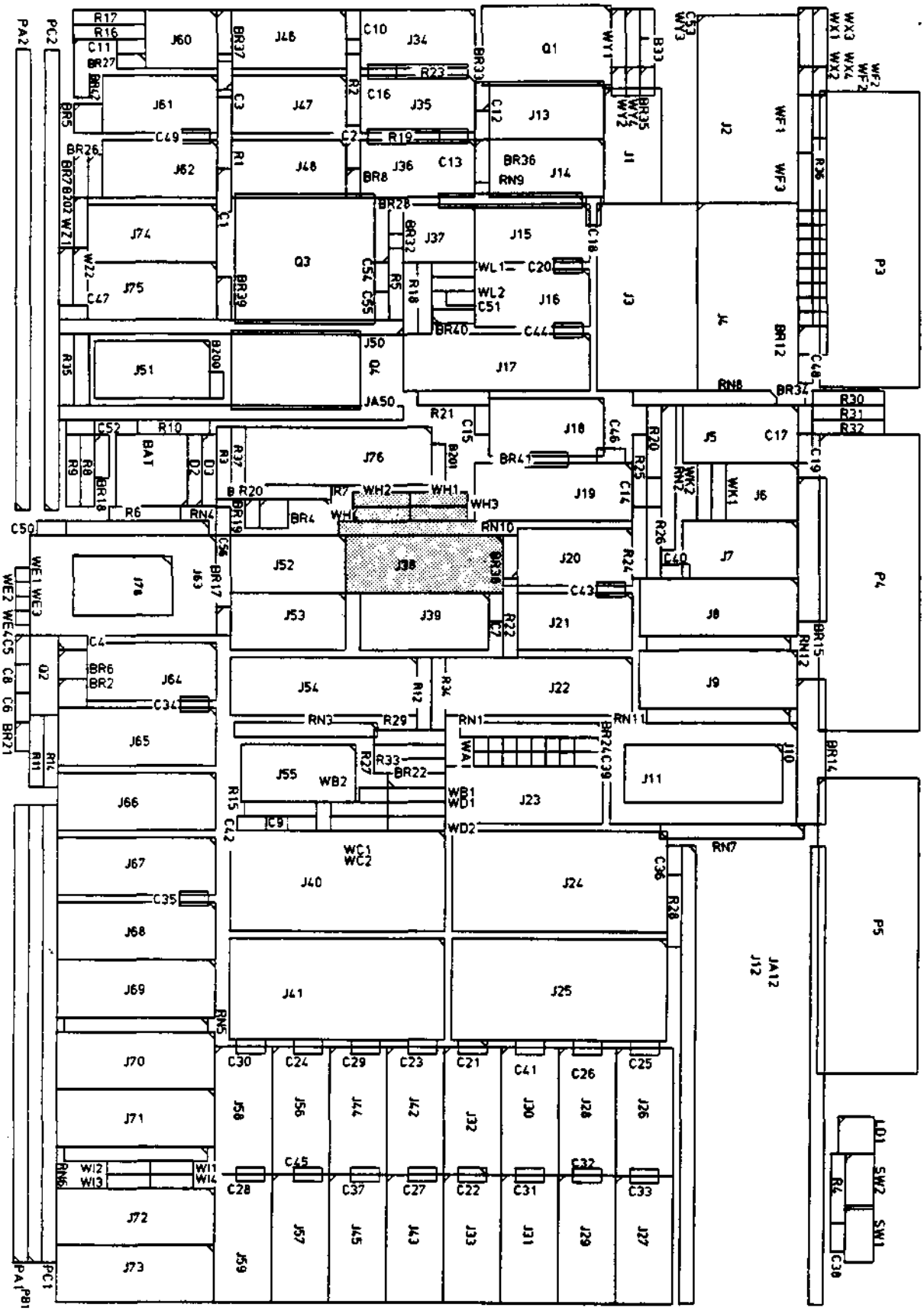


FIG. 47 LOCATION DIAGRAM OF THE SHORT I/O PARTS

6.11 The Bus Error Function

To provide an error function, if a device or memory on the bus has not responded within a maximum time, a time-out counter is used on the board.

This time-out counter generates a Bus Error Signal (BERR*) after a user-supplied time limit (up to 15ms). The CPU aborts the current cycle if the BERR* signal has been recognised, and forces the exception routine.

Figure 48 shows the detailed diagram of an access cycle aborted via BERR* with the default set values.

Table 34 lists the usable time-out values and the equivalent jumper settings. Figure 49 outlines the location diagram of the jumper fields.

If the board is the current VMEbus master, and an external VMEbus card generates a BERR*, then the cycle will be aborted in the same way, because the VMEbus BERR* signal is ANDed with the internal time-out counter BERR* signal.

For example, an external BERR* signal can be generated by a dynamic memory card by using an Error Detection and Correction Logic (EDC) and detection of a non-correctable data pattern.

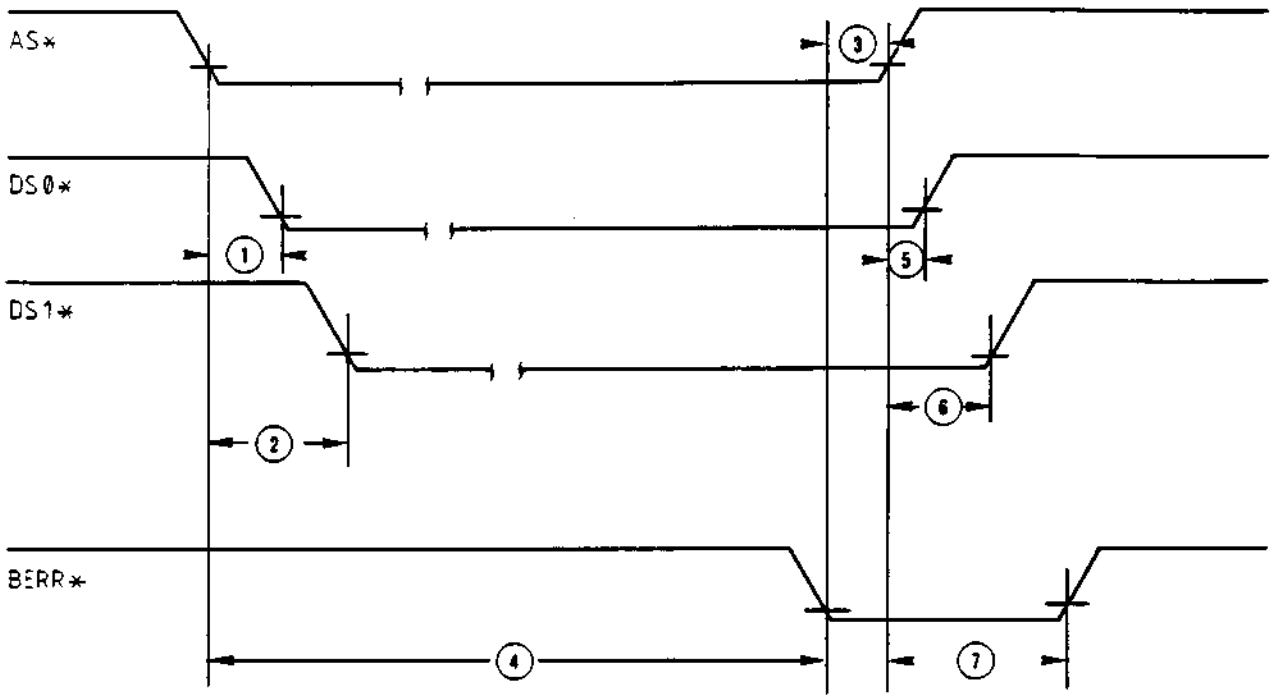


FIG. 48 TIMING DIAGRAM OF A BERR* CYCLE

Table 34 Jumper Settings of the Time-Out Counter

Time-Out (in microsec)	Connection Between WK1		WK2
150	3	-	3
300	2	-	2
1500	4	-	4
	5-8		

Time-out modifications are only made possible by changing these jumpers.

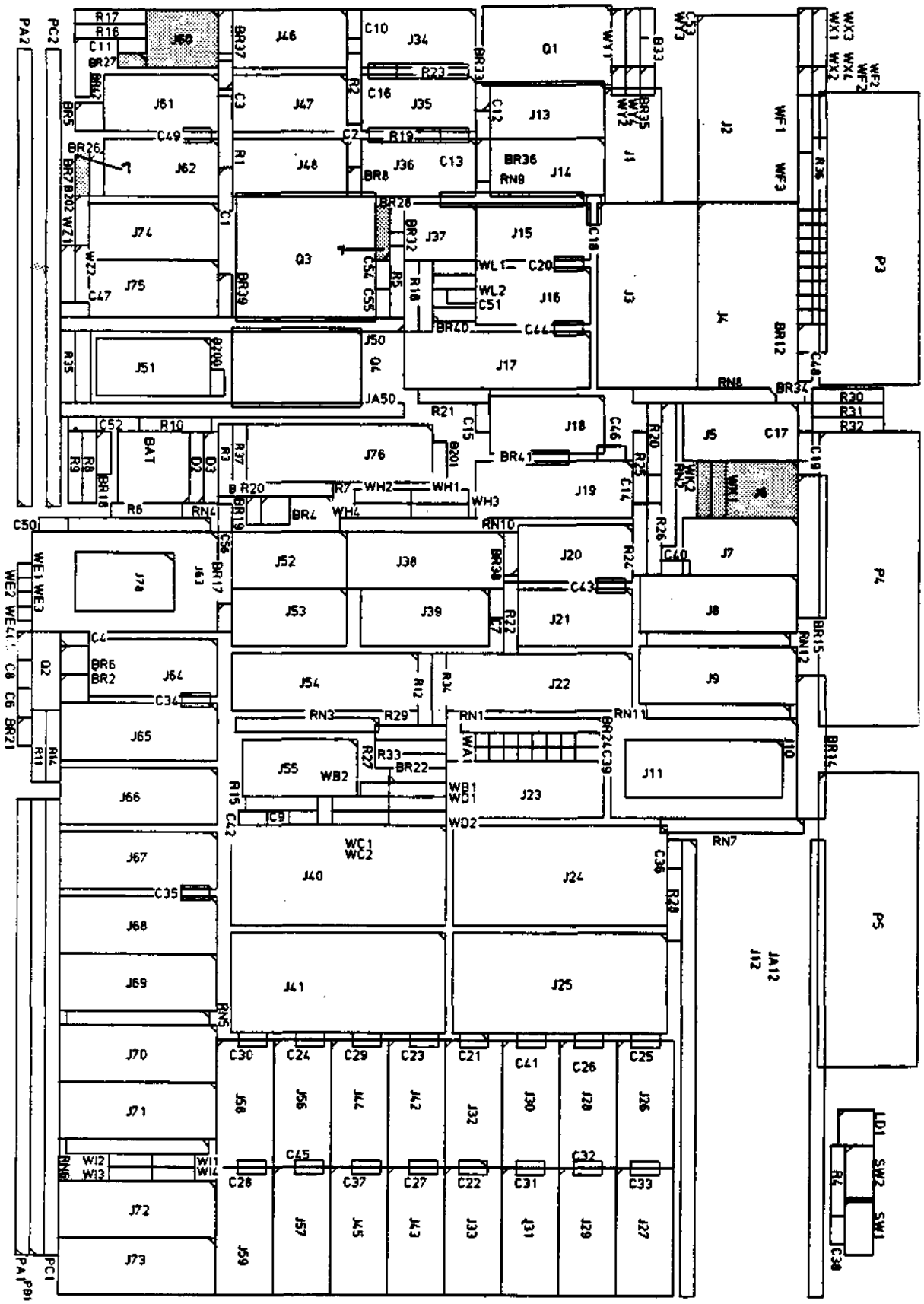


FIG. 49 LOCATION DIAGRAM OF THE BERR* PARTS

APPENDIX A

Specifications of the SYS68K/CPU-1B,C,D

Specifications of the SYS68K/CPU-1B / CPU-1VB

Microprocessor	68000 (8MHz) / 68010 (8MHz)
Parallel I/O	68230 PI/T, 16 data lines and 8 control lines configurable as a Centronics parallel interface
Serial I/O	3 R232C interface strap selectable baud rate from 110-9600 or 600-19200 baud
Timer	One 24-bit timer with a 5-bit prescaler
Real Time Clock	Programmable real time clock with battery back-up
Memory	128K bytes of DRAM, 64K bytes of SYSTEM Area, 64K bytes of USER Area
Firmware	16K bytes of monitor called SYS68K-1B MONITOR including a one-line assembler/disassembler
Power Requirements	+5V/2.8A, +12V/220mA -12V/200mA
Operating Temp.	0 to 60 degrees C
Storage Temp.	-50 to 85 degrees C
Relative Humidity	0-95% (non-condensing)
Board Dimensions	Double Eurocard 234x160mm (9.2x6.3")

Specifications of the SYS68K/CPU-1C / CPU-1VC

Microprocessor	68000 (10MHz) / 68010 (10 MHz)
Parallel I/O	68230 PI/T, 16 data lines and 8 control lines configurable as a Centronics parallel interface
Serial I/O	3 R232C interface strap selectable baud rate from 110-9600 or 600-19200 baud
Timer	One 24-bit timer with a 5-bit prescaler
Real Time Clock	Programmable real time clock with battery back-up
Memory	128K bytes of RAM, 64K bytes of SYSTEM Area, 64K bytes of USER Area
Firmware	16K bytes of monitor called SYS68K-1B MONITOR including a one-line assembler/disassembler
Power Requirements	+5V/2.8A, +12V/220mA -12V/200mA
Operating Temp.	0 to 60 degrees C
Storage Temp.	-50 to 85 degrees C
Relative Humidity	0-95% (non-condensing)
Board Dimensions	Double Eurocard 234x160mm (9.2x6.3")

Specifications of the SYS68K/CPU-1D / CPU-1VD

Microprocessor	68000 (10MHz) / 68010 (10 MHz)
Parallel I/O	68230 PI/T, 16 data lines and 8 control lines configurable as a Centronics parallel interface
Serial I/O	3 R232C interface strap selectable baud rate from 110-9600 or 600-19200 baud
Timer	One 24-bit timer with a 5-bit prescaler
Real Time Clock	Programmable real time clock with battery back-up
Memory	512K bytes of DRAM, 64K bytes of SYSTEM Area, 64K bytes of USER Area
Firmware	16K bytes of monitor called SYS68K-1B MONITOR including a one-line assembler/disassembler
Power Requirements	+5V/2.8A, +12V/220mA -12V/200mA
Operating Temp.	0 to 60 degrees C
Storage Temp.	-50 to 85 degrees C
Relative Humidity	0-95% (non-condensing)
Board Dimensions	Double Eurocard 234x160mm (9.2x6.3")

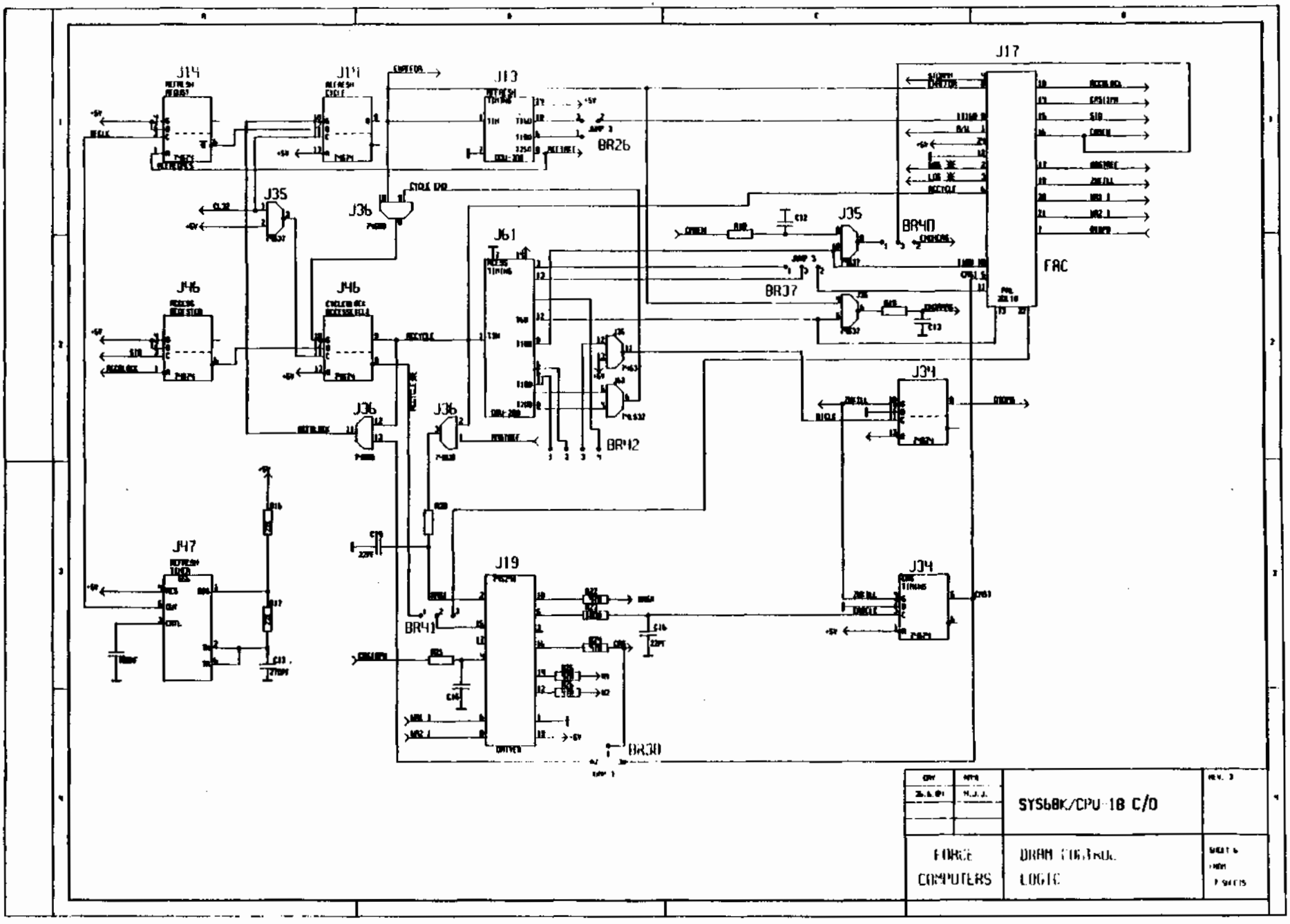
Specifications of the SYS68K/CPU-1F / CPU-1VF

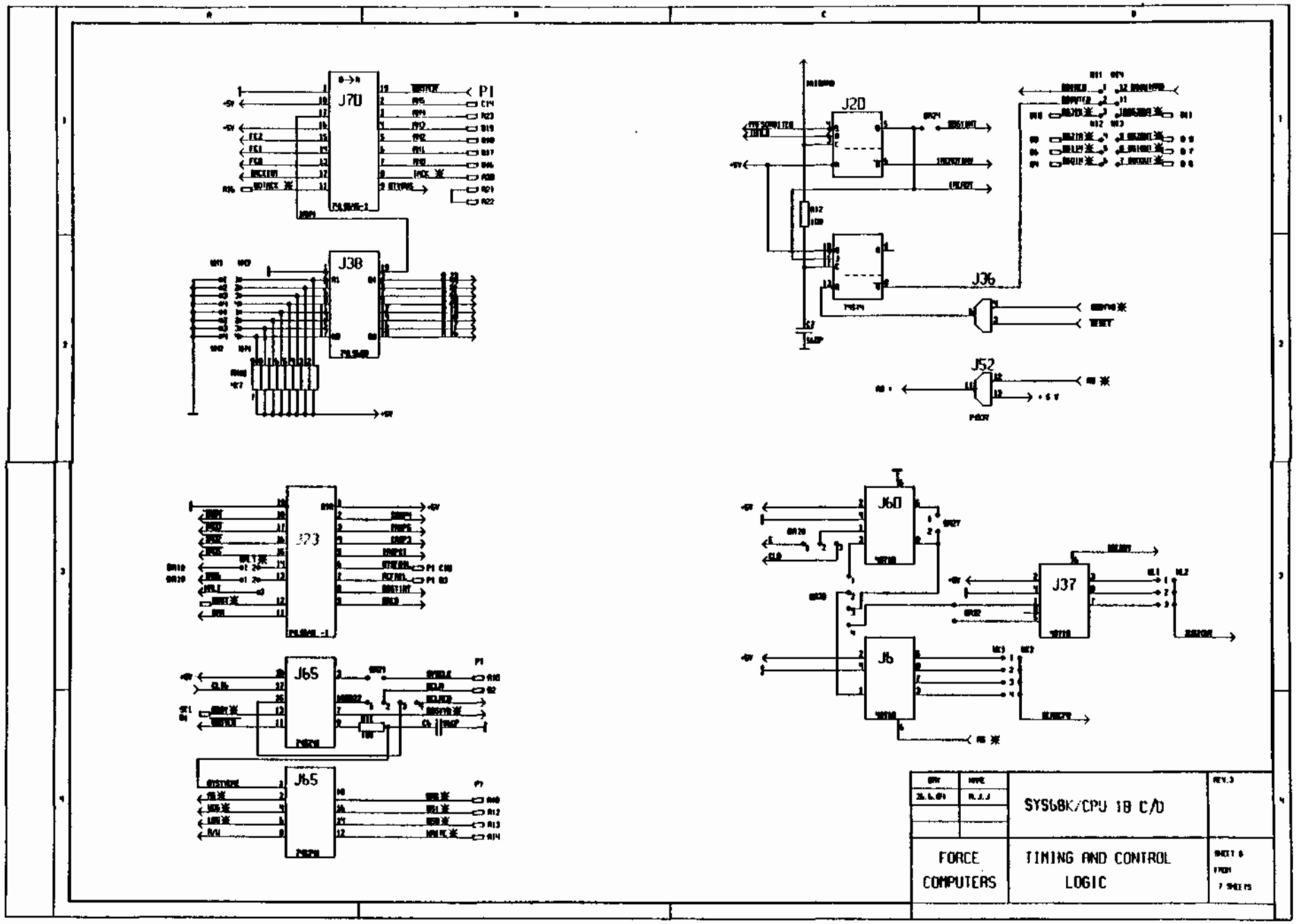
Microprocessor	68000 (8MHz) / 68010 (8 MHz)
Parallel I/O	68230 PI/T, 16 data lines and 8 control lines configurable as a Centronics parallel interface
Serial I/O	3 R232C interface strap selectable baud rate from 110-9600 or 600-19200 baud
Timer	One 24-bit timer with a 5-bit prescaler
Real Time Clock	Programmable real time clock with battery back-up
Memory	512K bytes of DRAM, 64K bytes of SYSTEM Area, 64K bytes of USER Area
Firmware	16K bytes of monitor called SYS68K-1B MONITOR including a one-line assembler/disassembler
Power Requirements	+5V/2.8A, +12V/220mA -12V/200mA
Operating Temp.	0 to 60 degrees C
Storage Temp.	-50 to 85 degrees C
Relative Humidity	0-95% (non-condensing)
Board Dimensions	Double Eurocard 234x160mm (9.2x6.3")

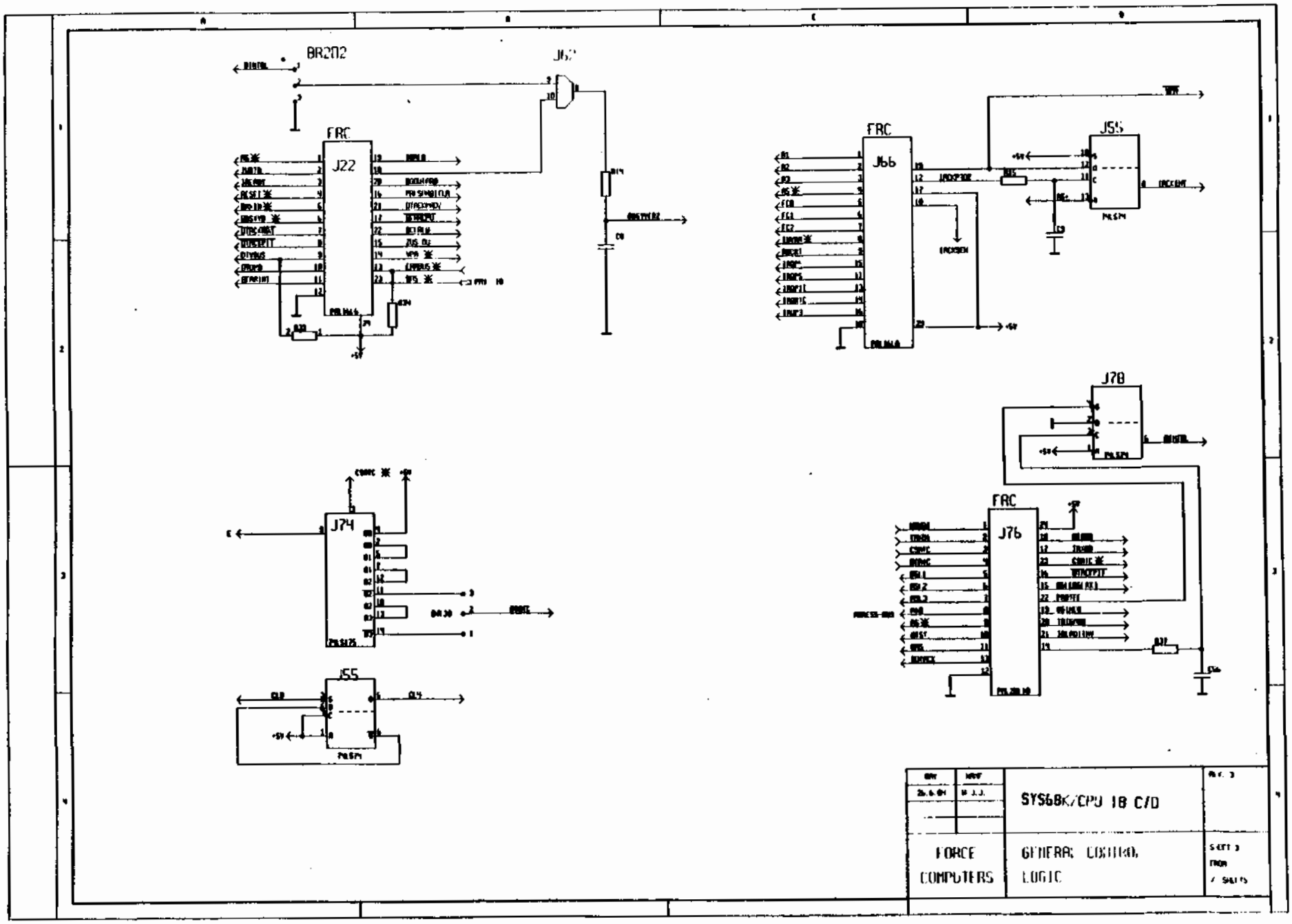
APPENDIX B

MEMORY MAP FOR THE SYS68K/CPU-1B

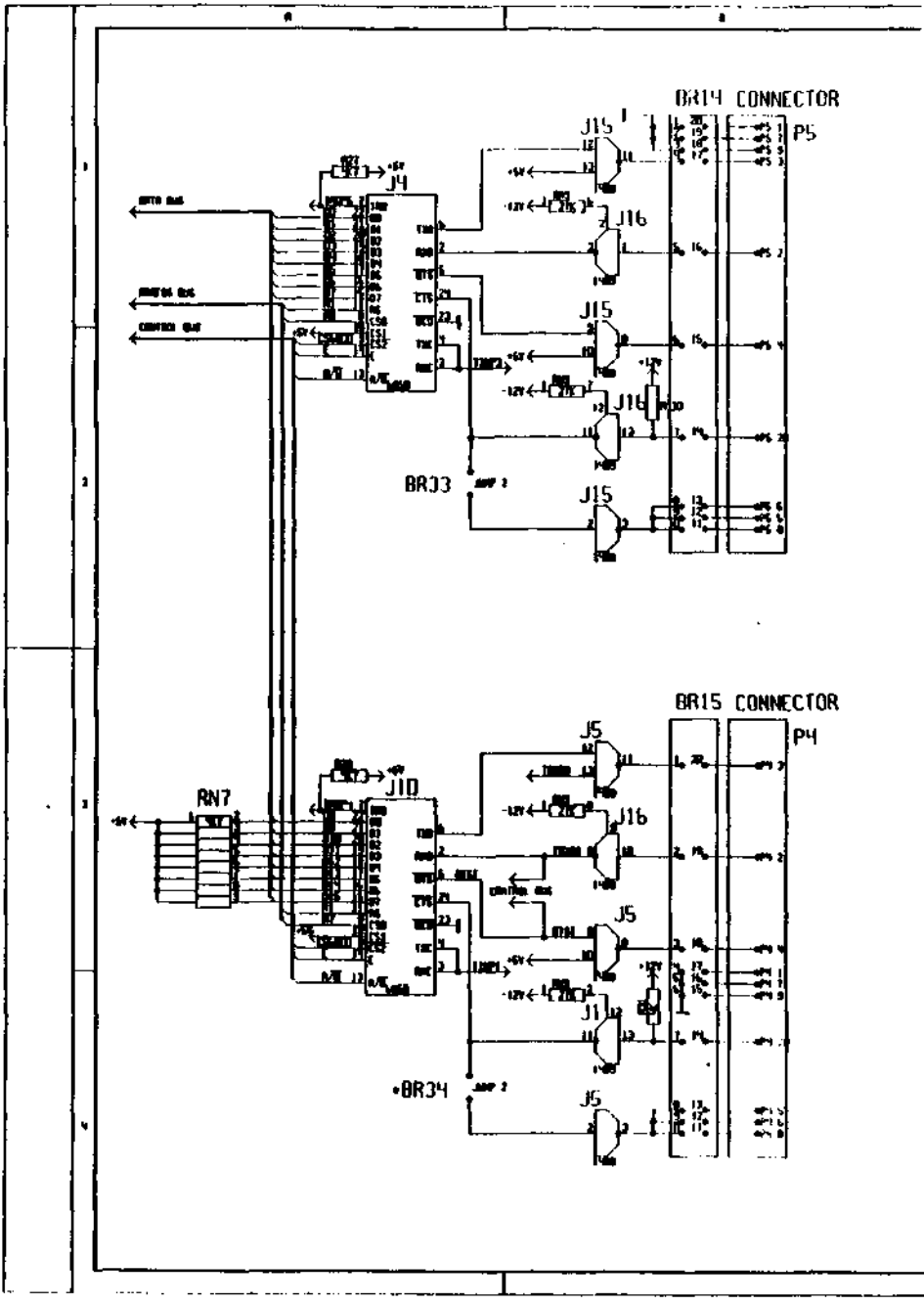
000 000 : 000 007	ROM Initialisation Vectors from SYSTEM EPROM
000 008 : 000 FFF	SYSTEM DRAM Area (Reserved)
001 000 : 01F FFF	USER DRAM Area (128K byte)
001 000 : 080 007	USER DRAM Area (512K byte)
080 008 : 09F FFF	SYSTEM EPROM Area (64K byte)
0A0 000 : 0BF FFF	USER EPROM Area (64K byte)
0C0 041 : 0C0 043	RS 232 Interface (Host)
0C0 080 : 0C0 090	RS 232 Interface (Terminal)
0C0 101 : 0C0 103	RS 232 Interface (Remote)
0C0 401 : 0C0 42F	RTC (Real Time Clock)
0E0 001 : 0E0 035	PI/T (Parallel Interface/Timer)

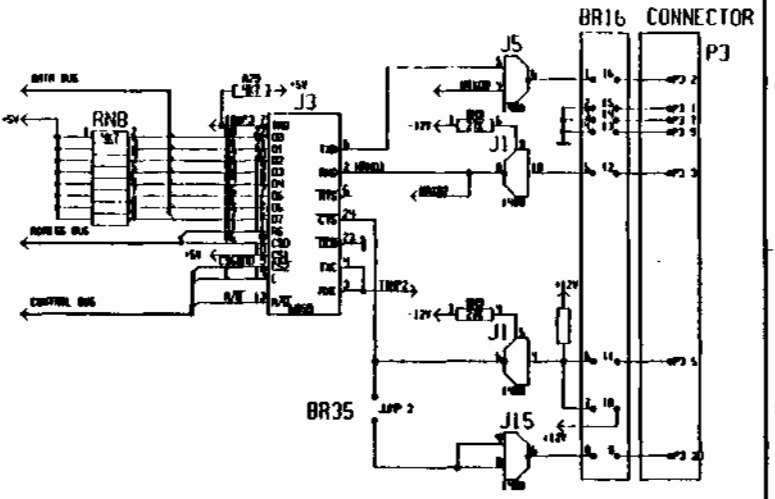

J17
J14
J11
J13
BR26
J35
J36
J61
J46
J46
J35
BR40
BR37
FAC
J34
J36
J36
BR42
J47
J19
J34
BR41
BR30
SYS68K/CPU-18 C/O
FORCE
COMPUTERS
DRAM CONTROL
LOGIC

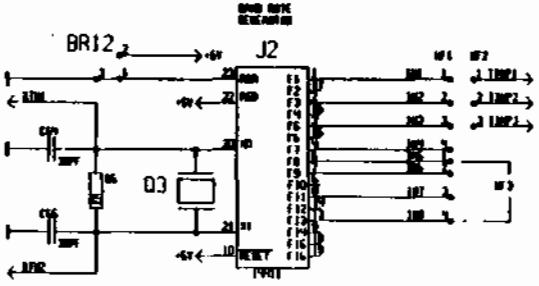

J70
J38
J20
J36
J52
J23
J60
J37
J65
J65
J6
SYS68K/CPU 1B C/D
FORCE COMPUTERS
TIMING AND CONTROL LOGIC


BR202
J67
FRC
J22
FRC
J66
J55
J78
J74
J55
FRC
J76
SYS68K/CPU 18 C/D
FORCE
COMPUTERS
GENERAL CONTROL
LOGIC

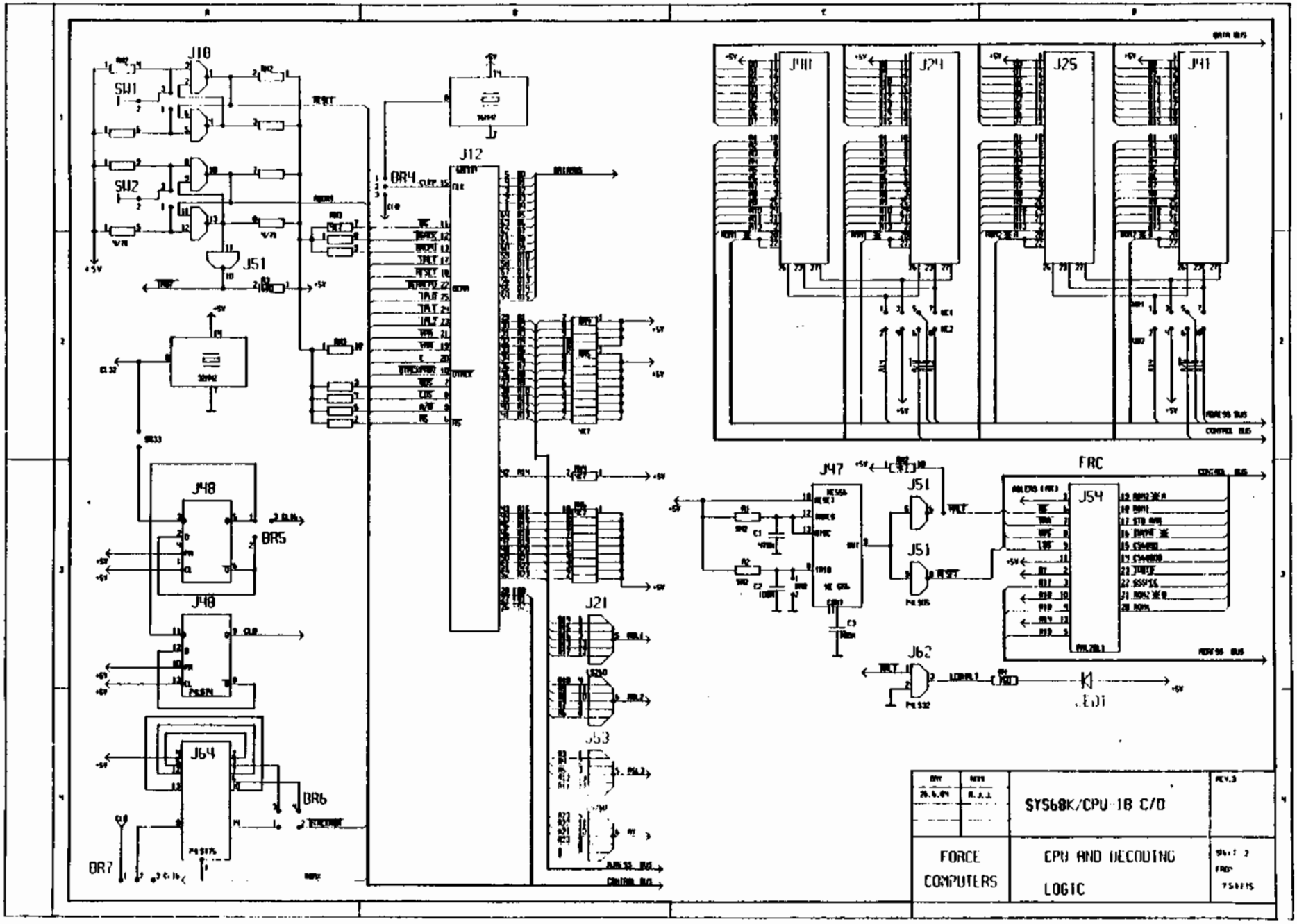
P1
J71
J68
P1
WA1
BR2
J69
J67
J72
J73
J39
CONTROL BUS
DATA BUS
+12V
-12V
J27
J31
J40
J32
J29
J43
J26
J44
J57
J33
J28
J56
J59
J45
J30
J58
SYS68K/CPU-1B C/D
FORCE COMPUTERS
THE DYNAMIC RISK

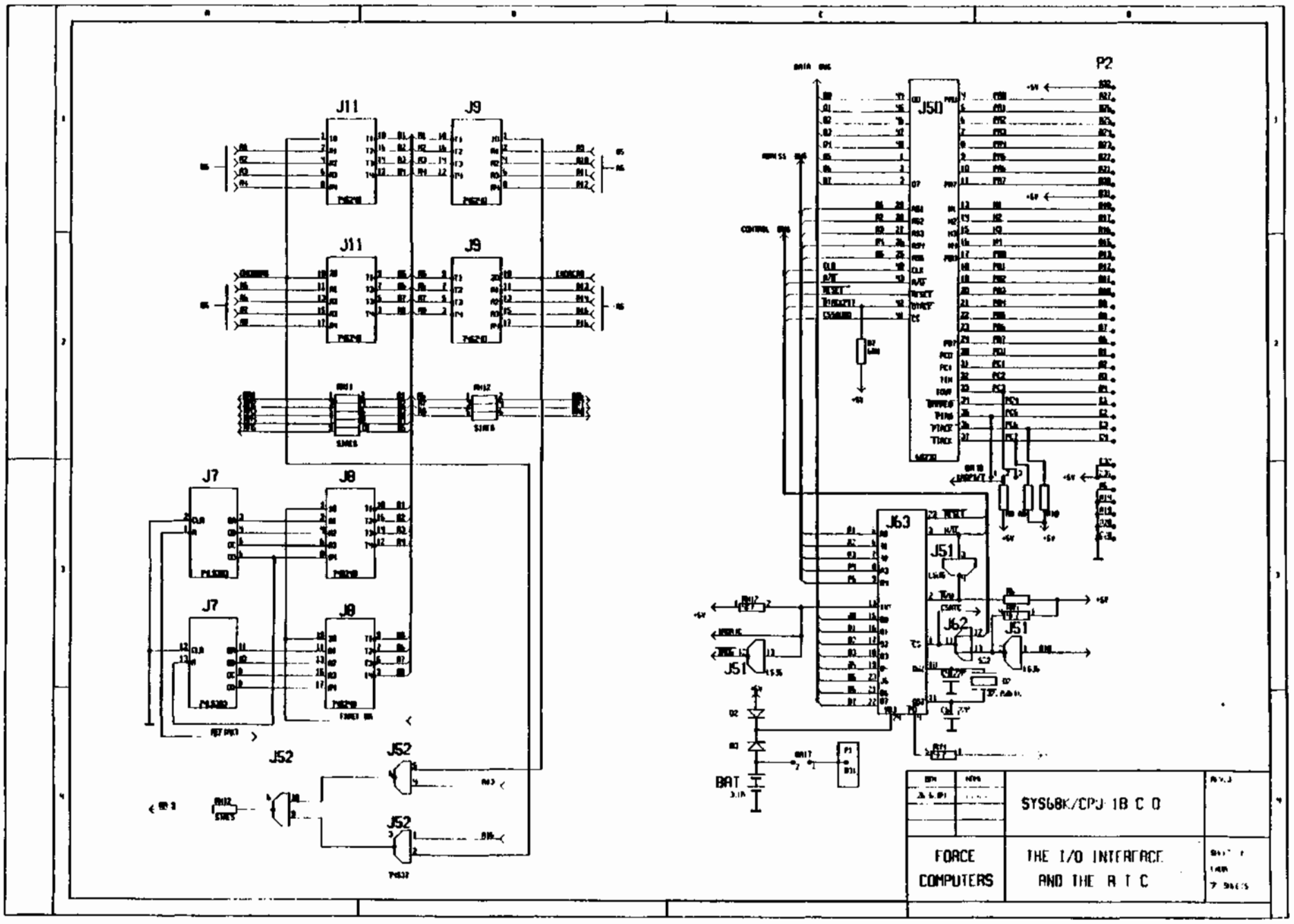

BR14 CONNECTOR
P5
J15
J16
J4
BR33
BR15 CONNECTOR
P4
J5
J16
J10
RN7
BR34
J1





		SYS68K/CPU 1B C/D	
FORCE COMPUTERS		THE SERIAL I/O INTERFACES	


J10
SW1
SW2
J51
J12
BR4
J11
J24
J25
J31
J47
J51
J51
FRC
J54
J48
BR5
J48
J21
J64
BR6
BR7
J53
J62
SYS68K/CPU-1B C/D
REV.3
FORCE COMPUTERS
CPU AND DECODING LOGIC


J11
J9
J11
J9
J7
J8
J7
J8
J52
J52
J52
P2
J50
J63
J51
J62
J51
J51
BAT
SYS68K/CPU 1B C 0
FORCE
COMPUTERS
THE I/O INTERFACE
AND THE R T C

APPENDIX C

ADDRESS ASSIGNMENT OF I/O DEVICES:

DEVICE: 6850 ACIA (Terminal)

Address	Mode	Description
ØC0080	R	Status Register
ØC0080	W	Control Register
ØC0082	R	Receive Data Register
ØC0082	W	Transmit Data Register

DEVICE: 6850 ACIA (Host)

Address	Mode	Description
ØC0041	R	Status Register
ØC0041	W	Control Register
ØC0043	R	Receive Data Register
ØC0043	W	Transmit Data Register

DEVICE: 6850 ACIA (REMOTE)

Address	Mode	Description
ØC0101	R	Status Register
ØC0101	W	Control Register
ØC0103	R	Receive Data Register
ØC0103	W	Transmit Data Register

DEVICE: 58167A RTC (Real Time Clock)

Address	Mode	Description
0C0401	R/W	Counter - Ten Thousands of Seconds
0C0403	R/W	Counter - Hundredths and Tenths of Sec.
0C0405	R/W	Counter - Seconds
0C0407	R/W	Counter - Minutes
0C0409	R/W	Counter - Hours
0C040B	R/W	Counter - Days of the Week
0C040D	R/W	Counter - Days of the Month
0C040F	R/W	Counter - Month
0C0411	R/W	RAM - Ten Thousands of Sec.
0C0413	R/W	RAM - Hundredths and Tenths of Sec
0C0415	R/W	RAM - Seconds
0C0417	R/W	RAM - Minutes
0C0419	R/W	RAM - Hours
0C041B	R/W	RAM - Days of the Week
0C041D	R/W	RAM - Days of the Month
0C041F	R/W	RAM - Month
0C0421	R	Interrupt Status Register
0C0423	R/W	Interrupt Control Register
0C0425	W	Counters Reset
0C0427	W	RAM - Reset
0C0429	R/W	Status Bit
0C042B	W	GO Command
0C042D	W	Standby - Interrupt
0C042F	W	Test Mode

APPENDIX D

COMPONENT PART LIST / SYS68K/CPU-1B

IC's

Location	Type	Manufacturer	Package	Function
J 1	75189	TI,MOT	J	RS 232 LINE RECEIVER
J 2	14411	MOT	J	BAUD RATE GENERATOR
J 3	6850	HIT,MOT	J	ACIA
J 4	6850	HIT,MOT	J	ACIA
J 5	75188	TI,MOT	J	RS 232 LINE DRIVER
J 6	49LS710	TI	J	BINARY COUNTER
J 7	74LS393	TI	J	4 BIT BINARY COUNTER (2)
J 8	74S240	TI,MOT	J	OCTAL BUFFERS/LINE DRIVERS/RECEIVERS
J 9	74S240	TI,MOT	J	OCTAL BUFFERS/LINE DRIVERS/RECEIVERS
J10	6850	HIT,MOT	J	ACIA
J11	74S240	TI,MOT	J	OCTAL BUFFERS/LINE DRIVERS/RECEIVERS
J12	68000L8	HIT,MOT,ROCK	K	CPU
J13	DDU-4-5300	DATA DEL.,TOKO	J	DIGITAL DELAY UNIT
J14	74S74	TI,MOT	J	D-FF (2)
J15	75188	TI,MOT	J	RS 232 LINE DRIVER
J16	75189	TI,MOT	J	RS 232 LINE RECEIVER
J17	FRC 37	MMI	J	PAL 12L10
J18	74LS01	TI,MOT	J	2 INPUT NAND GATE (OC) (4)
J19	74S241	TI,MOT	J	OCTAL BUFFERS/LINE DRIVERS/RECEIVERS
J20	74S74	TI,MOT	J	D-FF (2)

APPENDIX

COMPONENT PART LIST / SYS68K/CPU-1B

IC's

Location	Type	Manufacturer	Package	Function
J21	74LS260	TI,MOT,NSC	J	5 INPUT NOR GATES (2)
J22	FRC 35	MMI	J	PAL 16L6
J23	74LS641-1	TI,MOT	J	OCTAL BUS TRANSCEIVER
J24	2764	HIT,SEEQ,FUJ	K	EPROM
J25				EMPTY SOCKET
J26	4164-15	NEC,HIT	J	64K * 1 DRAM
J27	4164-15	NEC,HIT	J	64K * 1 DRAM
J28	4164-15	NEC,HIT	J	64K * 1 DRAM
J29	4164-15	NEC,HIT	J	64K * 1 DRAM
J30	4164-15	NEC,HIT	J	64K * 1 DRAM
J31	4164-15	NEC,HIT	J	64K * 1 DRAM
J32	4164-15	NEC,HIT	J	64K * 1 DRAM
J33	4164-15	NEC,HIT	J	64K * 1 DRAM
J34	74S74	TI,MOT	J	D-FF (2)
J35	74S37	TI,MOT	J	2 INPUT NAND BUFFER (4)
J36	74S08	TI,MOT	J	2 INPUT AND GATES (4)
J37	49LS710	TI	J	BINARY COUNTER
J38	74LS688	TI,MOT	J	8 BIT COMPARATOR
J39	74LS148	TI	J	8 TO 3 LINE OCTAL PRIORITY ENCODERS
J40	2764	HIT,SEEQ,FUJ	K	EPROM

APPENDIX

COMPONENT PART LIST / SYS68K/CPU-1B

IC's

Location	Type	Manufacturer	Package	Function
J41				EMPTY SOCKET
J42	4164-15	NEC,HIT	J	64K * 1 DRAM
J43	4164-15	NEC,HIT	J	64K * 1 DRAM
J44	4164-15	NEC,HIT	J	64K * 1 DRAM
J45	4164-15	NEC,HIT	J	64K * 1 DRAM
J46	74S74	TI,MOT	J	D-FF (2)
J47	556	TI,NSC	J	TIMER (2)
J48	74S74	TI,MOT	J	D-FF (2)
J50	68230L8	MOT,ROCK	K	PI/T
J51	74LS05	TI,MOT	J	HEX INVERTERS (OC)
J52	74S37	TI,MOT	J	2 INPUT NAND BUFFERS(4)
J53	74LS260	TI,MOT	J	5 INPUT NOR GATES (2)
J54	FRC 34	MMI	J	PAL 20L10
J55	74S74	TI,MOT	J	D-FF (2)
J56	4164-15	NEC,HIT	J	64K * 1 DRAM
J57	4164-15	NEC,HIT	J	64K * 1 DRAM
J58	4164-15	NEC,HIT	J	64K * 1 DRAM
J59	4164-15	NEC,HIT	J	64K * 1 DRAM
J60	49LS710	TI	J	BINARY COUNTER

APPENDIX

COMPONENT PART LIST / SYS68K/CPU-1B

IC's

Location	Type	Manufacturer	Package	Function
J61	DDU-7J-200	DATA DEL.,TOKO	J	DIGITAL DELAY UNIT
J62	74LS32	TI,MOT,NSC	J	2 INPUT OR GATES
J63	58167A	NSC	J	REAL TIME CLOCK
J64	74LS175	TI,MOT,NSC	J	D-FF (4)
J65	74S241	TI,MOT	J	OCTAL BUFFERS/LINE DRIVERS/RECEIVERS
J66	FRC36	MMI	J	PAL 16L8
J67	74LS645-1	MMI,TI	J	OCTAL BUS TRANSCEIVER
J68	74LS641-1	MMI,TI	J	OCTAL BUS TRANSCEIVER
J69	74LS645-1	MMI,TI	J	OCTAL BUS TRANSCEIVER
J70	74LS645-1	MMI,TI	J	OCTAL BUS TRANSCEIVER
J71	74LS645-1	MMI,TI	J	OCTAL BUS TRANSCEIVER
J72	74LS645-1	MMI,TI	J	OCTAL BUS TRANSCEIVER
J73	74LS645-1	MMI,TI	J	OCTAL BUS TRANSCEIVER
J74	74LS175	TI,MOT,NSC	J	D-FF (4)
J76	FRC 38	MMI	J	PAL 20L10
J78	74LS74	TI,MOT,NSC	J	D-FF (2)

J = STANDARD DIL PACKAGE IN PLASTIC

K = STANDARD DIL PACKAGE IN CERAMIC

APPENDIX

COMPONENT PART LIST / SYS68K/CPU-1B

Crystals

Location	Type	Manufacturer	Package	Function
Q1	32.Ø MHz	SE		QUARZ OSCILLATOR MODULE
Q2	32.768KHz	SE		QUARZ
Q3	1.8432MHz	SE		QUARZ

Diodes

Location	Type	Manufacturer	Package	Function
LD1	24Ø6	DIALIGHT		LED RED
D2	1N4148	VARIOUS	1Ø.16	DIODE
D3	1N4148	VARIOUS	1Ø.16	DIODE

Battery

Location	Type	Manufacturer	Package	Function
BAT	CR 1/3 N	VARTA		LITHIUM BATTERY 3.ØV

APPENDIX

COMPONENT PART LIST / SYS68K/CPU-1B

Resistors (in Ohm)

Location	Type	Manufacturer	Package	Function
R 1	4.7M	VARIOUS	10.16	
R 2	4.7M	VARIOUS	10.16	
R 3	680	VARIOUS	10.16	
R 4	47	VARIOUS	10.16	
R 5	1M	VARIOUS	10.16	
R 6	820	VARIOUS	10.16	
R 7	680	VARIOUS	10.16	
R 8	680	VARIOUS	10.16	
R 9	4.7K	VARIOUS	10.16	
R10	4.7K	VARIOUS	10.16	
R11	100	VARIOUS	10.16	
R12	100	VARIOUS	10.16	
R15	100	VARIOUS	10.16	
R16	22K	VARIOUS	10.16	
R17	22K	VARIOUS	10.16	
R18	100	VARIOUS	10.16	
R19	100	VARIOUS	10.16	
R20	100	VARIOUS	10.16	

APPENDIX

COMPONENT PART LIST / SYS68K/CPU-1B

Resistors (in Ohm)

Location	Type	Manufacturer	Package	Function
R21	100	VARIOUS	10.16	
R22	47	VARIOUS	10.16	
R23	100	VARIOUS	10.16	
R24	47	VARIOUS	10.16	
R25	100	VARIOUS	10.16	
R26	47	VARIOUS	10.16	
R27	680	VARIOUS	10.16	
R28	4.7K	VARIOUS	10.16	
R29	4.7K	VARIOUS	10.16	
R30	4.7K	VARIOUS	10.16	
R31	4.7K	VARIOUS	10.16	
R32	4.7K	VARIOUS	10.16	
R33	4.7K	VARIOUS	10.16	
R34	4.7K	VARIOUS	10.16	
R35	4.7K	VARIOUS	10.16	
R37	100	VARIOUS	10.16	

APPENDIX

COMPONENT PART LIST / SYS68K/CPU-1B

Resistor Networks

Location	Type	Manufacturer	Package	Function
RN1	9*4.7K	VARIOUS	SIL	
RN2	9*4.7K	VARIOUS	SIL	
RN3	9*4.7K	VARIOUS	SIL	
RN4	9*4.7K	VARIOUS	SIL	
RN5	9*4.7K	VARIOUS	SIL	
RN6	9*4.7K	VARIOUS	SIL	
RN7	9*4.7K	VARIOUS	SIL	
RN8	9*4.7K	VARIOUS	SIL	
RN9	7*27K	VARIOUS	SIL	
RN10	9*4.7K	VARIOUS	SIL	
RN11	5*47	VARIOUS	SIL	
RN12	5*47	VARIOUS	SIL	

APPENDIX

COMPONENT PART LIST / SYS68K/CPU-1B

Capacitors

Location	Type	Manufacturer	Package	Function
C1	470nF	VARIOUS	5.08	
C2	100nF	VARIOUS	2.54	
C3	100nF	VARIOUS	2.54	
C4	33pF	VARIOUS	2.54	
C5	33pF	VARIOUS	2.54	
C7	680pF	VARIOUS	2.54	
C8	560pF	VARIOUS	2.54	
C9	470pF	VARIOUS	2.54	
C10	100nF	VARIOUS	2.54	
C11	270pF	VARIOUS	2.54	
C12	150pF	VARIOUS	2.54	
C14	220pF	VARIOUS	2.54	
C17	100nF	VARIOUS	2.54	
C19	100nF	VARIOUS	2.54	
C21-C48	100nF	VARIOUS	2.54	
C56	1nF	VARIOUS	2.54	
C50-C53	100nF	VARIOUS	2.54	

APPENDIX

COMPONENT PART LIST / SYS68K/CPU-1B

Mechanical Parts

Location	Type	Manufacturer	Package	Function
SW1	AT-1F	KNITTER		SWITCH
SW2	AT-1F	KNITTER		SWITCH
J2		VARIOUS		24 PIN SOCKET
J3		VARIOUS		24 PIN SOCKET
J4		VARIOUS		24 PIN SOCKET
J10		VARIOUS		24 PIN SOCKET
J12		VARIOUS		64 PIN SOCKET
J17		VARIOUS		24 PIN SLIM SOCKET
J22		VARIOUS		24 PIN SLIM SOCKET
J24		VARIOUS		28 PIN SOCKET
J25		VARIOUS		28 PIN SOCKET
J26-J33		VARIOUS		16 PIN SOCKET
J40		VARIOUS		28 PIN SOCKET
J41		VARIOUS		28 PIN SOCKET
J42-J45		VARIOUS		16 PIN SOCKET
J50		VARIOUS		2X24 PIN SIL SOCKET
J54		VARIOUS		24 PIN SLIM SOCKET
J56-J59		VARIOUS		16 PIN SOCKET
J63		VARIOUS		24 PIN SOCKET
J66		VARIOUS		20 PIN SOCKET
J76		VARIOUS		24 PIN SLIM SOCKET

APPENDIX

COMPONENT PART LIST / SYS68K/CPU-1B

Mechanical Parts

Location	Type	Manufacturer	Package	Function
P1		VARIOUS		VG MALE CONNECTOR 96 PIN 90 DEGREES
P2		VARIOUS		VG MALE CONNECTOR 64 PIN 90 DEGREES
P3-P5		VARIOUS		D FEMALE CONNECTOR 90 DEGREES
	CPU-1-PC	VARIOUS		PC BOARD
	CPU-1-F	VARIOUS		FRONT PANEL
BR2+BR6	DW8	VARIOUS		HEADER
BR4+BR19 +BR20	EW6+EW2	VARIOUS		HEADER
BR5	EW2+EW1	VARIOUS		HEADER
BR7+B202	EW6	VARIOUS		HEADER
BR8	EW2	VARIOUS		HEADER
BR14	DW20	VARIOUS		HEADER
BR15	DW20	VARIOUS		HEADER
BR17	EW2	VARIOUS		HEADER
BR18	EW3	VARIOUS		HEADER
BR21	EW2	VARIOUS		HEADER
BR22	EW4	VARIOUS		HEADER
BR24	EW2	VARIOUS		HEADER
BR26	EW3	VARIOUS		HEADER
BR27	EW2	VARIOUS		HEADER
BR28	EW4	VARIOUS		HEADER
BR32	EW2	VARIOUS		HEADER
BR33	EW2	VARIOUS		HEADER
BR34	EW2	VARIOUS		HEADER

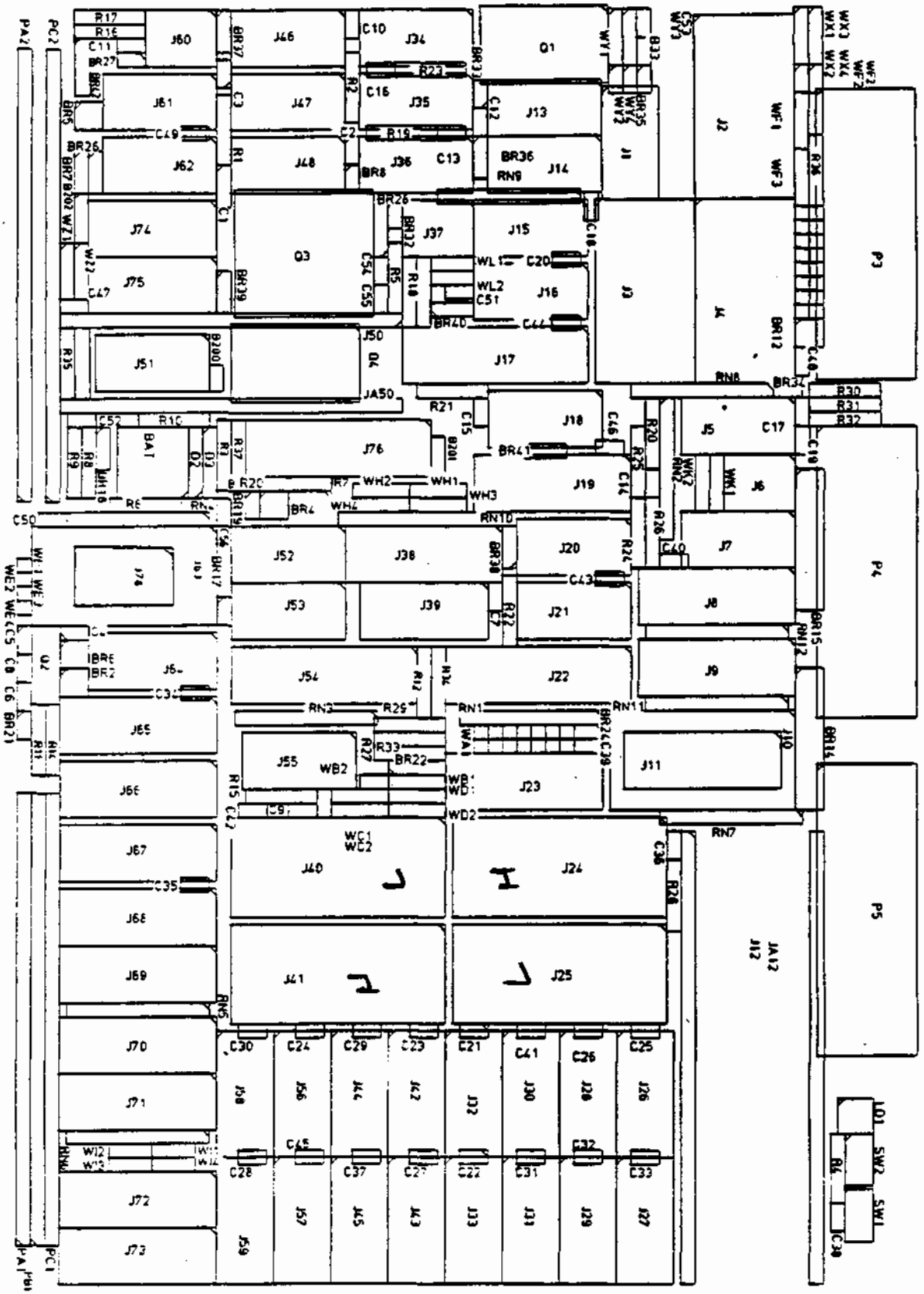
APPENDIX

COMPONENT PART LIST / SYS68K/CPU-1B

Mechanical Parts

Location	Type	Manufacturer	Package	Function
BR35+B33	EW4	VARIOUS		HEADER
BR36	EW3	VARIOUS		HEADER
BR37	EW3	VARIOUS		HEADER
BR38	EW3	VARIOUS		HEADER
BR39	EW3	VARIOUS		HEADER
BR40	EW3	VARIOUS		HEADER
BR41	EW3	VARIOUS		HEADER
BR42	EW4	VARIOUS		HEADER
B201	EW3	VARIOUS		HEADER
WA1	DW14	VARIOUS		HEADER
WB1+WB2	EW6	VARIOUS		HEADER
WC1+WC2 +WD1+WD2	DW16	VARIOUS		HEADER
WH1-WH4	DW16	VARIOUS		HEADER
WI1-W14	DW12	VARIOUS		HEADER
WK1+WK2	DW8	VARIOUS		HEADER
WL1+WL2	DW6	VARIOUS		HEADER
WX1+WX2 +WF1+WF3 +BR12	EW23+EW9	VARIOUS		HEADER HEADER
WX3+WX4	EW8	VARIOUS		HEADER
WZ1+WZ2	DW8	VARIOUS		HEADER
	JUMPERS A	VARIOUS		JUMPERS FOR HEADERS (76)

APPENDIX E



LOCATION DIAGRAM

Artisan Technology Group is an independent supplier of quality pre-owned equipment

Gold-standard solutions

Extend the life of your critical industrial, commercial, and military systems with our superior service and support.

We buy equipment

Planning to upgrade your current equipment? Have surplus equipment taking up shelf space? We'll give it a new home.

Learn more!

Visit us at **artisantg.com** for more info on price quotes, drivers, technical specifications, manuals, and documentation.

Artisan Scientific Corporation dba Artisan Technology Group is not an affiliate, representative, or authorized distributor for any manufacturer listed herein.

We're here to make your life easier. How can we help you today?

(217) 352-9330 | sales@artisantg.com | artisantg.com

ARTISAN® TECHNOLOGY GROUP