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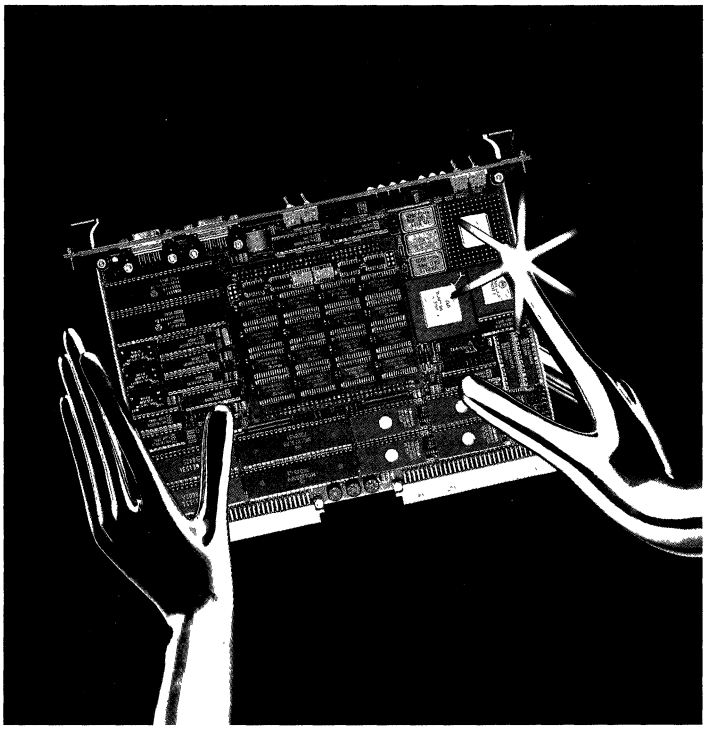
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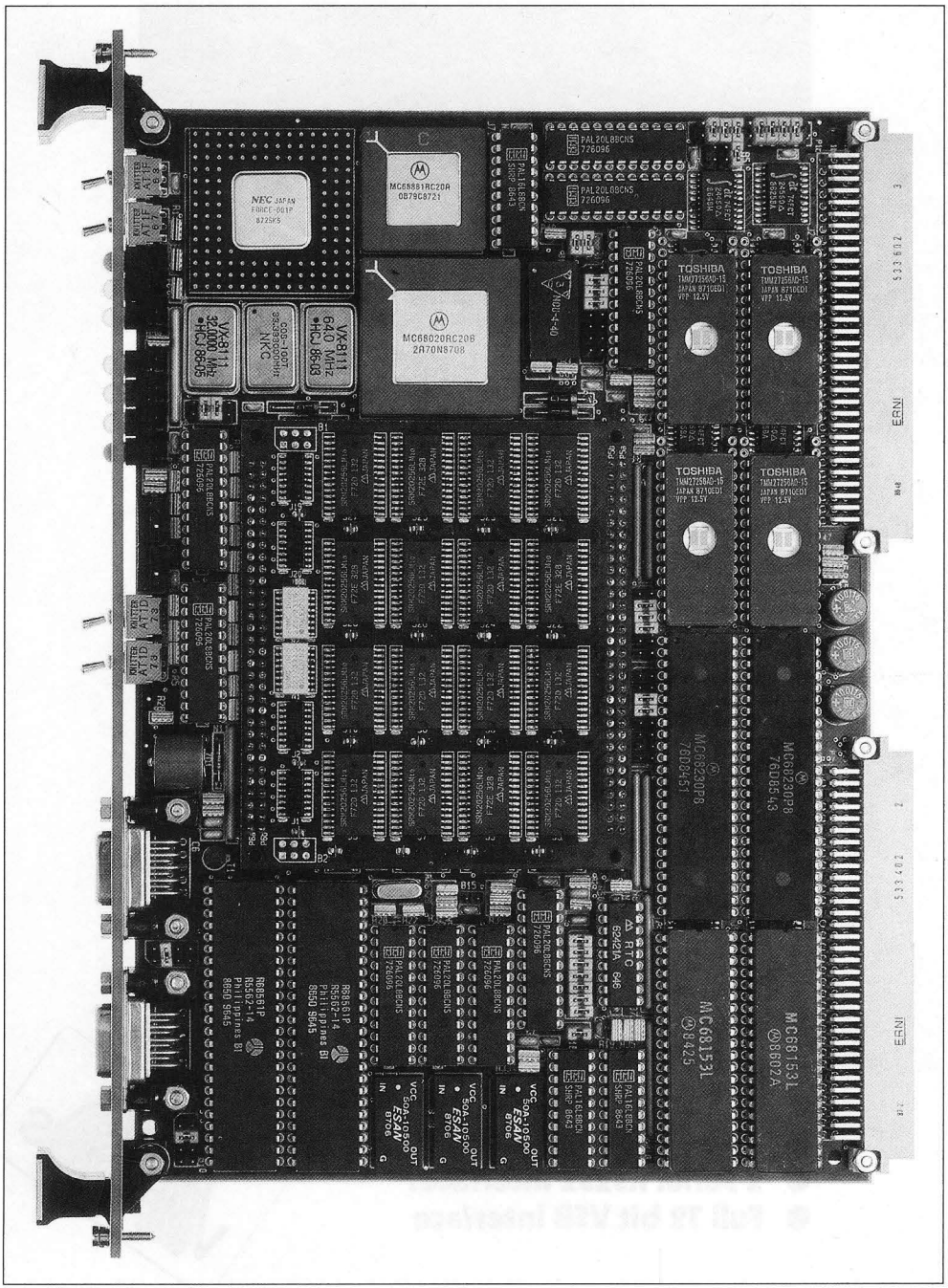
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System 68000 VME SYS68K/CPU-29

High Performance 68020 Multiprocessor CPU Board with VSB Interface

- 12.5 MHz to 30 MHz 68020 CPU
- 1 Mbyte 0 Wait State SRAM
- 2 Serial RS232 Interfaces
- Full 32 bit VSB Interface

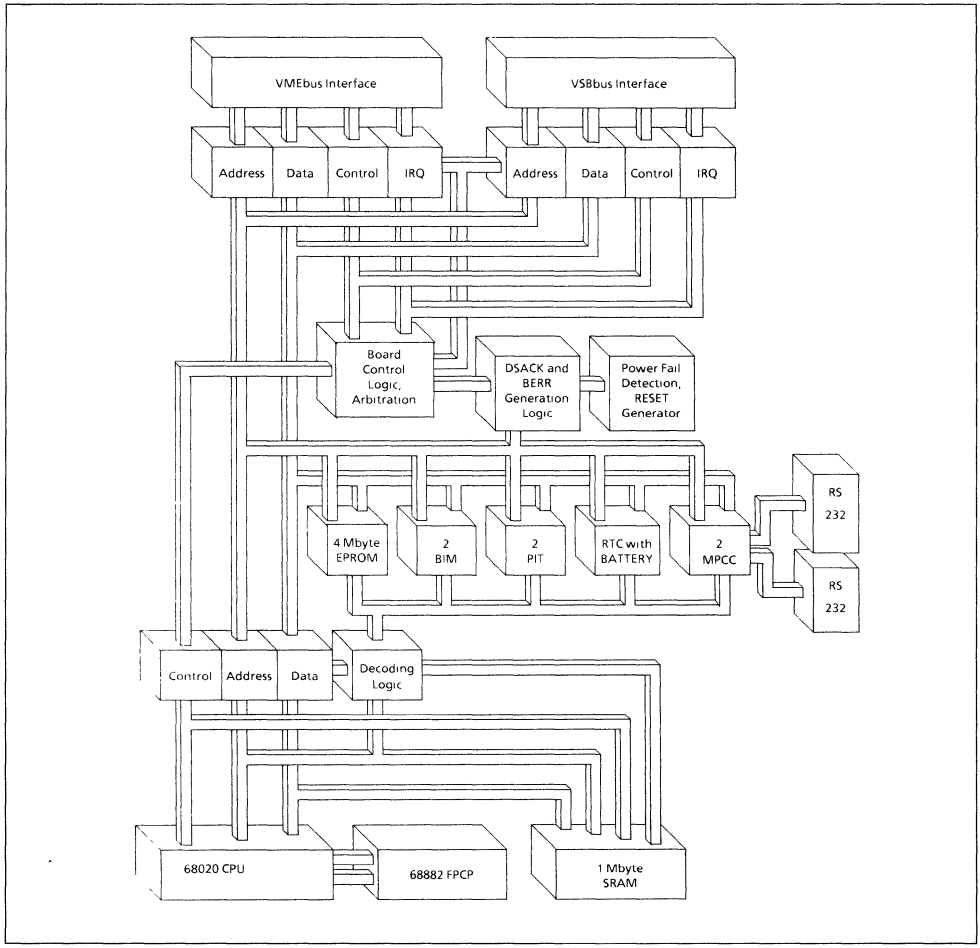


1. General Description

The SYS68K/CPU-29 is an ultra high speed CPU board using a 68020 with a clock frequency of up to 30 MHz. The SYS68K/CPU-29 is fully software compatible to the SYS68K/CPU-21 board. The SYS68K/CPU-29 uses only a single VMEbus slot while the SYS68K/CPU-21 uses 2 to 3 slots.
A static RAM of up to 1 Mbyte capacity can be accessed from the CPU (30 MHz clock frequency) without the insertion of wait states for all read and write cycles. A full 32 bit VSB interface including bus arbitration and interrupt handling is installed on all CPU-29 board versions.

Two serial I/O interfaces (RS232 compatible) provide asynchronous and synchronous data transfer rates of up to 38400 baud or 2 Mbit/sec.
The EPROM area consists of 4 devices supporting the 28 and 32 pin JEDEC standard providing a maximum capacity of 4 Mbyte.
Two fully independent 24 bit timers, a Real Time Clock with an on-board battery backup and the full 32 bit VMEbus master interface complete the board.
In addition, VMEPROM, the PDOS* compatible multi-user real time monitor/debugger is installed on the SYS68K/CPU-29 boards.

BLOCK DIAGRAM OF THE SYS68K/CPU-29XC.



2. Features of the SYS68K/CPU-29

- 68020 CPU (12.5 MHz) on CPU-29XS
  (16.7 MHz) on CPU-29X
  (25.0 MHz) on CPU-29XB
  (30.0 MHz) on CPU-29XC
- 68882 FPCP (12.5 MHz) on CPU-29XS
  (16.7 MHz) on CPU-29X
  (20.0 MHz) on CPU-29XB
  (25.0 MHz) on CPU-29XC
- 68561 Multi Protocol Communication Controllers (2x) for serial I/O data transfers (RS232 compatible)
- 68230 Parallel Interface and Timer devices (2x) for local control and timer function
- 68153 Bus Interrupter Modules (2x) for all local interrupt management
- 1 Mbyte of constant zero wait state static RAM
- Up to 4 Mbyte of EPROM using 4 EPROMs (28 and 32 pin JEDEC standard) building a 32 bit data path
- VSB interface (full 32 bit) with single level arbiter
  A32, A24, A16: D(0), D8, D16, D32
  Unaligned transfers
  Read-modify-write transfers
  Interrupt Handler
- VMEbus interface (full 32 bit) with single level arbiter
  A32, A24, A16: D(0), D8, D16, D32
  Unaligned transfers
  Read-modify-write transfers
- Bus timer
- Power monitor
- SYSRESET generator
- RUN/HALT/CACHE and TEST function switches
- Status indication LEDs
- 2 HEX rotary switches
- Fully software compatible to the SYS68K/CPU-21 CPU board
- VMEPROM installed

3. Hardware Description

3.1 The 68020 CPU

The 68020 with its 32 bit address and data paths is installed on the SYS68K/CPU-29 board.
The CPU includes a 256 byte instruction cache which significantly reduces the number of bus cycles needed for program fetches. A CACHE switch on the front panel allows the user to enable or disable the on-chip cache for software debugging purposes.
The 68020 CPU accesses the static RAM with 30 MHz clock frequency constantly without the insertion of wait states. This allows the design to take full advantage of the throughput of the CPU.

The EPROM area, the Floating Point Coprocessor, the SRAM and the VSB interface are directly connected to the CPU data and address bus interface (as shown in the block diagram of the SYS68K/CPU-29). The clock frequency of the CPU ranges from 12.5 to 30 MHz. This offers, in combination with the SRAM, a real computing rate of 2-6 MIPs.

3.2 The Floating Point Coprocessor

The SYS68K/CPU-29 is fitted with the enhanced 68882 Floating Point Coprocessor (FPCP). The clock frequency of the CPU and the FPCP is identical. The FPCP conforms to the IEEE Floating Point standard 754 (draft 10.0).
Easy floating point operation control to the coprocessor is provided because the intercommunication between the CPU and the FPCP is built in silicon.
An internal register set inside the FPCP of 8 general purpose registers (80 bit wide) yields fast execution times.

Features of the FPCP

- 8 general purpose registers (80 bit, 64 bit Mantissa, 15 bit exponent and one sign bit)
- 67 bit on-chip ALU
- 67 bit barrel shifter
- 46 instruction types including 35 arithmetic operations
- IEEE 754 standard (draft 10.0)
- Full support of trigonometrical and logarithmic functions such as:
  SINE and COSINE
  TANGENT and COTANGENT
  Hyperbolic functions (TANGENT, ARC TANGENT, SINE and COSINE)
  Logarithmic functions (4)
  Square root and exponential functions (4)
- The 68882 is fully software compatible to the 68881 FPCP

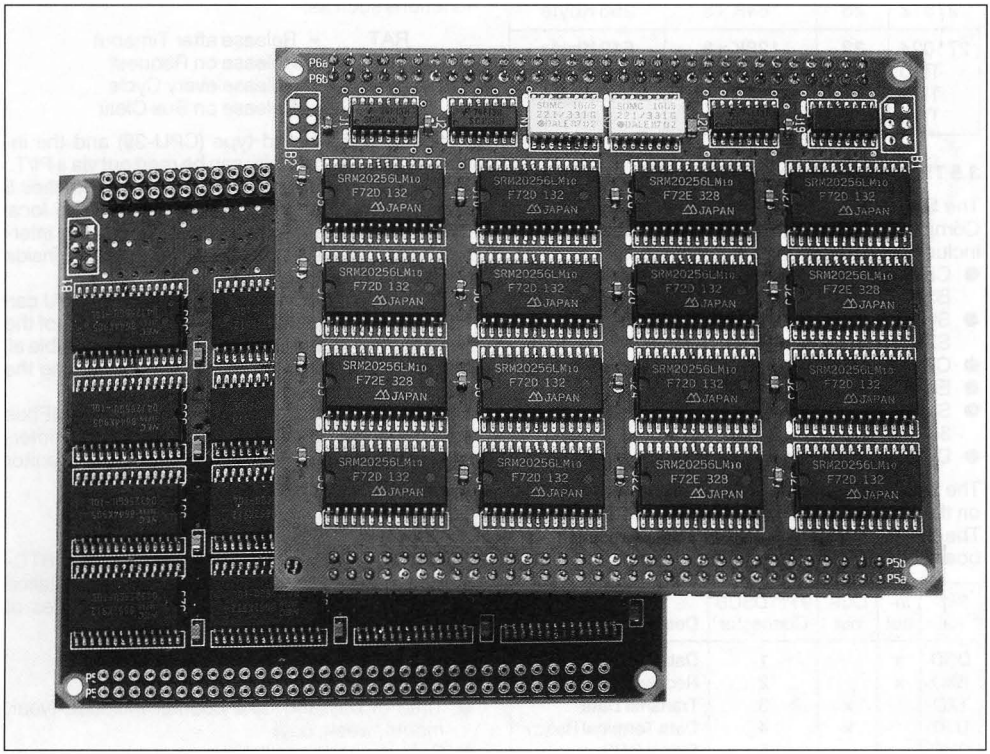
3.3 The Static RAM

The SYS68K/CPU-29 contains a high speed static RAM offering constant no wait state access of all CPU access cycles. This 32 bit wide memory allows to take full advantage of the CPU execution speed. An upgrade to 4 Mbyte RAM is possible, as the RAM is located on a memory module which can easily be replaced if higher density modules become available.
The memory bandwidth of the SYS68K/CPU-29 reaches 40 Mbyte/sec in the 30 MHz version without any need for refresh because static RAMs are used.

The low cost 12.5 and 16.7 MHz versions (SYS68K/CPU-29XS and -29X) access the static RAM (1 M-byte) constantly without the insertion of wait states. On the 25.0 MHz version (SYS68K/CPU-29XB) 100 ns devices (32 K x 8) are installed providing a constant one wait state access to the RAM.
The 30 MHz board version uses 256 K x 1 oriented devices with an access time of 35 ns to guarantee the constant zero wait state operation of the CPU.
The following table lists the CPU board type, the memory capacity as well as the required number of wait states for accessing the SRAM area. In addition, the memory module with the 32 K x 8 oriented devices, together with the on-board control logic, supports a battery backup through the +5V STDBY line.

Board Type	CPU Clock Frequency (MHz)	SRAM Capacity (byte)	No. of Wait States	External Battery Backup Supported
CPU-29XS	12.5	1 M	0	Yes
CPU-29X	16.7	1 M	0	Yes
CPU-29XB	25.0	1 M	1	Yes
CPU-29XC	30.0	1 M	0	No

PHOTO OF THE MEMORY MODULE



3.4 The EPROM Area

The SYS68K/CPU-29 contains four user EPROM sockets supporting 28 or 32 pin EPROM devices. Maximum data throughput to the 68020 CPU is provided through the fast decoding logic and separate data transceivers supporting one wait state operation if 100 ns devices are used. The following table lists the supported device types and the memory capacity.

Supported Device Types in the User EPROM Area:

Device Type	Pins	Organization	Total Memory Capacity
2764	28	8K x 8	32 Kbyte
27128	28	16K x 8	64 Kbyte
27256	28	32K x 8	128 Kbyte
27512	28	64K x 8	256 Kbyte
271024	32	128K x 8	512 Kbyte
TBD	32	256K x 8	1 Mbyte
TBD	32	512K x 8	2 Mbyte
TBD	32	1M x 8	4 Mbyte

3.5 The Serial I/O Channels

The SYS68K/CPU-29 contains two Multi Protocol Communication Controllers (MPCC 68561) which include the following protocol features:

- Character oriented protocols
  BSC, DDCMP, X3.28, X.21, ECMA16
- Synchronous bit oriented protocols
  SDLC, HDLC, X.25
- CRC check selectable
- Eight character receiver and buffer registers
- Software programmable baud rate from 110 to 38400 baud
- DC data rate of up to 2 Mbit/s

The two RS232 compatible interfaces are installed on the front panel via two 9 pin D-Sub connectors. The following I/O signals are supported with on-board driver/receiver circuits:

Signal	Input	Output	9 Pin DSUB Connector	Description
DCD	x		1	Data Carrier Detect
RXD	x		2	Receive Data
TXD		x	3	Transmit Data
DTR		x	4	Data Terminal Ready
GND			5	Signal GND
DSR	x	x	6	Data Set Ready
RTS		x	7	Request to Send
CTS	x		8	Clear to Send
–	–	–	9	Not Connected

Each MPCC is able to interrupt the local CPU on a software programmable level. The interrupt vector is also software programmable.

3.6 The Local Control Devices

The SYS68K/CPU-29 contains two independent Parallel Interface and Timer devices (PI/T 68230), for local control and status display.
The clock frequency of each PI/T is 8.064 MHz on all different board versions. Eight control bits can be read via the PI/T port A. These control bits can be set via two HEX rotary switches available on the front panel for manipulation. In addition, 8 status bits can be read out via the second PI/T. The status bits can be used for setting different configurations, defining the slot number in a VMEbus multiprocessor system etc.
The PI/T also allows to program the bus release functions such as:

RAT = Release after Timeout
ROR = Release on Request
REC = Release every Cycle
RBCLR = Release on Bus Clear

In addition, the board type (CPU-29) and the installed memory capacity can be read out via a PI/T.
The two fully independent 24 bit timers with their 5 bit pre-scaler can be used to interrupt the local CPU on a software programmable level. The interrupt vector is also software programmable inside the Bus Interrupter Module.
All of the 7 interrupt request levels of the CPU can be separately enabled or disabled via port B of the first PI/T. For example, this allows you to disable all interrupts on a certain IRQ level by debugging the application software.
The SYSFAIL and ACFAIL signals of the VMEbus are connected to the first PI/T to eventually interrupt the local CPU (if programmed) or to monitor the status of these signals.

3.7 The Real Time Clock

A software programmable Real Time Clock (RTC-62421) with on-board battery backup is installed on the SYS68K/CPU-29 boards. The features of the Real Time Clock are listed below.

Features of the Real Time Clock

- Time of day and date counter included (year, month, week, day)
- Built-in quartz oscillator
- 12hr/24hr clock switchover
- Automatic leap year setting
- Interrupt masking
- C-MOS design provides low power consumption during power down mode.

The Real Time Clock is able to interrupt the local CPU on a software programmable level (1 to 7).

3.8 The Local Interrupt Sources

Two Bus Interrupter Modules (BIM 68153) are installed on the SYS68K/CPU-29 to manage all the local interrupts.
Each local interrupt source can be routed to one of the seven different IRQ levels of the CPU. The interrupt vector is also software programmable.

Local Interrupt Sources:

1) Test Switch
2) MPCC 1
3) MPCC 2
4) PI/T 1 Timer
5) PI/T 2 Timer
6) RTC
7) VSB-IRQ
8) ACFAIL
9) SYSFAIL

The SYS68K/CPU-29 will only request bus mastership for interrupt acknowledge cycles if the interrupt request was a VMEbus IRQ.

4. The VSB Interface

The SYS68K/CPU-29 board is delivered with a full 32 bit VSB master interface.
Maximum data throughput is provided on the VSB interface by supporting 32 bit of data via the 4 Gbyte address range. The VSB address range is decoded out of the 4 Gbyte address space of the 68020.
The following data transfer types are supported:

A32 : D8, D16, D32
Unaligned Transfers
Address Only Cycles
Read Modify Write Transfers

The VSB interface allows to build contiguous memory beyond the local SRAM. The local control logic provides an access cycle to the VSB interface before addressing the VMEbus. This technique allows an increase of the overall throughput of systems using the secondary bus. If the VSB interface is not required, a jumper setting allows to disable it and forces VMEbus accesses if there is no on-board access cycle detected.
The serial arbiter and the IHP Interrupt Handler complete the VSB interface.

5. The VMEbus Interface

The SYS68K/CPU-29 includes a full 32 bit VMEbus interface, thereby taking full advantage of the VMEbus specification.
The address modifier codes for A16, A24 and A32 addressing are fully supported.

The following data transfer types are supported:

Transfer Type	D31-D24	D23-D16	D15-D8	D7-D0
Byte			x	x
Word			x	x
Long Word	x	x	x	x
Unaligned Transfers	x 	x x x	x x x	 x
Read Modify Write	 x	 x	x x	x x x

The SYS68K/CPU-29 includes the following bus arbitration modes:

RWD	Release when done
ROR	Release on request
RBCLR	Release on Bus Clear
RAT	Release after Timeout

Each of the listed modes is software programmable inside the Gate Array. The bus request level of the SYS68K/CPU-29 is jumper selectable (BR0-3). A single level arbiter, a power monitor, a SYSRESET generator and support for ACFAIL and SYSFAIL complete the VMEbus interface.

6. The VMEPROM

6.1 General Description

VMEPROM is an EPROM based real time monitor. The complete package resides in 128 Kbyte of EPROM and uses a minimum of 32 Kbyte of RAM.
VMEPROM is composed of the powerful PDOS Real Time Kernel and the PDOS file manager. Thus the package provides support of a highly sophisticated Real Time Kernel and an interface to floppy and hard disk drives.
The user interface contains more than 50 commands perfectly suited for program debugging, host computer communications, as well as task- and file management. In addition, it includes a powerful line assembler and disassembler for the 68020 and the 68881.

VMEPROM features:

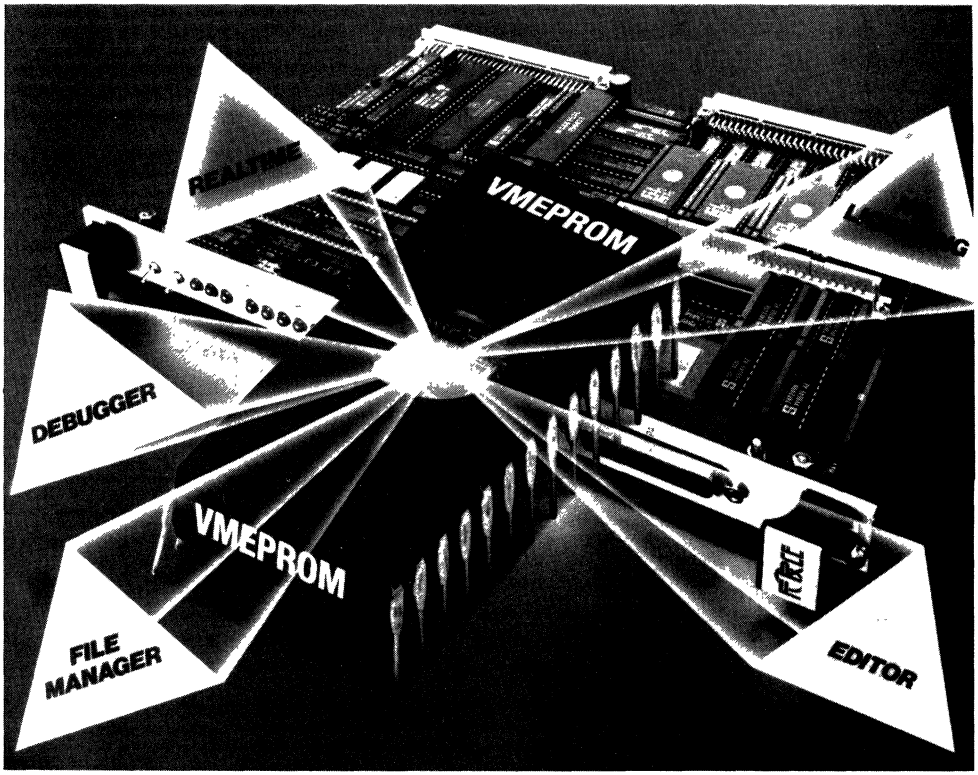
- Real Time Multitasking Kernel supporting up to 64 tasks.
- File management support for sequential, random and shared files. Up to 64 files may be opened at the same time.
- Line assembler/disassembler with full support of all 68020/68882 instructions.

- Over 20 commands for program debugging, including breakpoints, tracing, processor register display and modify.
- S-record up/downloading from any port defined in the system.
- Disk support for RAM disk, floppy and Winchester disks. Either a SYS68K/WFC-1 or a SYS68K/ISCSI-1 mass memory controller may be used. VMEPROM also allows disk formatting and initialization.
- Serial I/O support for up to two SIO or ISIO-1/2 boards in the system.
- EPROM programming utility using the SYS68K/RR-2/3 boards.
- Full screen editor.
- I/O redirection to files or ports from the command line.
- Over 100 system calls to the kernel are supported.

6.2 Description of the User Interface of VMEPROM

The user interface of VMEPROM allows I/O redirection to files or to any port defined within the system. Multiple command lines may be entered on a single command line. The user console input is interrupt driven and allows type-ahead. Over 60 commands are built into the VMEPROM user interface and are directly accessible without destroying memory. The command set covers functions such as program execution, breakpoints, tracing and a powerful line assembler/disassembler. Also resident are file system functions such as append, delete, copy, rename and show file. These are applicable for RAM disk, floppy or hard disk. The task management functions cover create task, kill task, alter task priority and list tasks.

VMEPROM



6.3 Description of the Kernel Functions

The kernel of VMEPROM is written in 68020 assembly language for fast and efficient execution. It provides multitasking, system clock,event processing and memory management. Ready tasks are scheduled with a prioritized round-robin method. Up to 64 tasks may be defined simultaneously.
Semaphores and events provide a low overhead facility for one task to signal another. Messages and mailboxes are used in conjunction with task lock, unlock, suspend and event primitives.

6.4 Description of the File Manager Functions

The file manager module provides sequential, random, read only and shared access to named files on RAM disk, floppy or hard disk. New files are automatically defined contiguously to improve access speed.

6.5 Supported VMEbus Hardware

Upon power up, VMEPROM checks the VMEbus for the availability of several controller boards. Supported are up to two serial I/O boards and one disk controller.
In addition, EPROM programming is supported by VMEPROM utilizing the SYS68K/RR-2/3 board family.

6.6 Target System Support

VMEPROM can easily be used in target systems. For these systems, the application program can be put into EPROM with or without the user interface. The application programs can be started either by a command line or directly after reset without user input.
The minimum EPROM space required by the VMEPROM kernel and file manager is about 40 Kbyte. Small romable applications can be put in EPROMS easily without the overhead of the user interface.

6.7 Development Systems

Currently either one of the FORCE PDOS* or UNIX* System V development stations may be used for software development for VMEPROM.
Compilers, assemblers, and libraries are available together with utilities for program downloading. These tools are well suited to help in program development and debugging.
The support of VMEPROM through other development systems like the IBM-AT or the VAX is under development. These cross-software development packages will include C-compiler, assemblers for the 68020 and libraries to generate codes to run under control of VMEPROM.

6.8 Licensing

No license is required for VMEPROM. VMEPROM is delivered free of charge with every CPU-29 board. For more detailed information please refer to the SYS68K/VMEPROM Data Sheet.

Specifications of the SYS68K/CPU-29

Functions	
68020 CPU Frequency on: CPU-29XS CPU-29X CPU-29XB CPU-29XC	 12.5 MHz 16.7 MHz 25.0 MHz 30.0 MHz
68881/2 FPCP Clock Frequency on: CPU-29XS CPU-29X CPU-29XB CPU-29XC	 12.5 MHz 16.7 MHz 20.0 MHz 25.0 MHz
Local RAM Type Data Path Memory Capacity External Battery backup for SRAMs No. of Wait States – CPU-29XA No. of Wait States – all others	SRAM 32 bit 1 Mbyte Yes (+5V STDBY) 1 (all cycles) 0 (all cycles)
No. of EPROM Sockets Data Path Max. Capacity No. of Wait States (min/max)	4 32 bit 4 Mbyte 1/8
Serial I/O Interfaces Used Controller RS232 compatible	2 2 x 68561 Yes
Real Time Clock (Typ) On-Board Battery Backup	62421 Yes
24 bit Timer	2
VSB Master Interface A32 : D(0), D8, D16, D32 Arbiter Interrupt Handler	Yes Yes Serial IHP
VMEbus Master Interface A32, A24, A16: D(0), D8, D16, D32 Unaligned Data Transfers Read-Modify-Write Cycles Single Level Bus Arbiter VMEbus Interrupt Handler	 Yes Yes Yes Yes IH 1 to 7
RESET, TEST, CACHE, HALT Function Switches	Yes
VMEPROM Firmware on all Board Versions	128 Kbyte
Power Requirements + 5V typ/max +12V typ/max -12V typ/max	 4.3/5.7A 0.1/0.2A 0.1/0.2A

Specification (cont'd)

Function		
Operating Temperature	(Degrees C)	0 to 50
Storage Temperature	(DegreesC)	−40 to 85
Relative Humidity	(noncondensing %)	0 to 95
Board Dimensions	(mm) (in)	234 x 160 9.2 x 6.3
No. of Slots used		1

Ordering Information

SYS68K/CPU-29XS Part No. 101150	12.5 MHz 68020 CPU board with 1 Mbyte zero wait state SRAM, FPCP and VMEPROM. Documentation included.
SYS68K/CPU-29X Part No. 101152	16.7 MHz 68020 CPU board with 1 Mbyte zero wait state SRAM, FPCP and VMEPROM. Documentation included.
SYS68K/CPU-29XB Part No. 101153	25.0 MHz 68020 CPU board with 1 Mbyte one wait state SRAM, FPCP and VMEPROM. Documentation included.
SYS68K/CPU-29XC Part No. 101154	30.0 MHz 68020 CPU board with 1 Mbyte zero wait state SRAM, FPCP and VMEPROM. Documentation included.
SYS68K/VMEPROM/UM Part No. 800140	User's Manual of VMEPROM
SYS68K/CPU-29/UM Part No. 800145	User's Manual for all SYS68K/CPU-29 board versions. VMEPROM documentation included.

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