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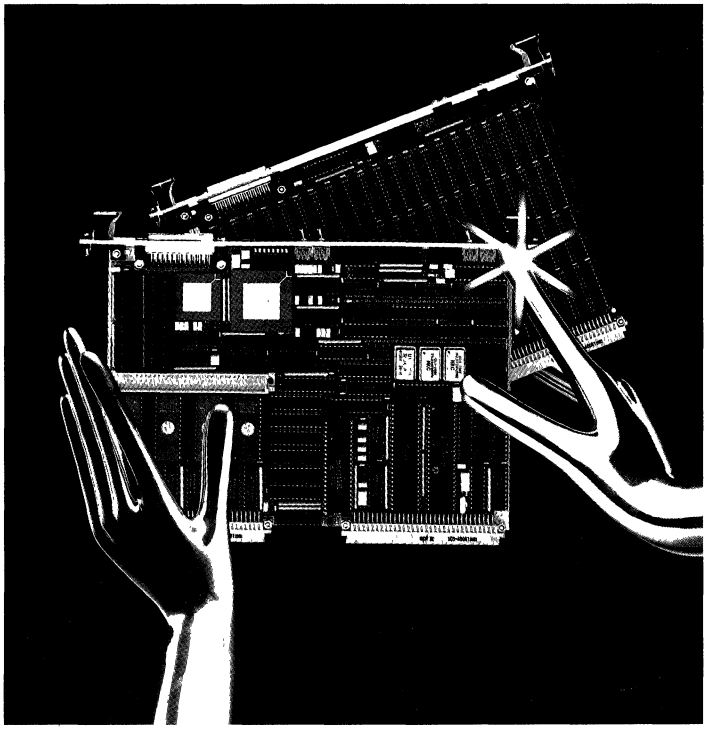
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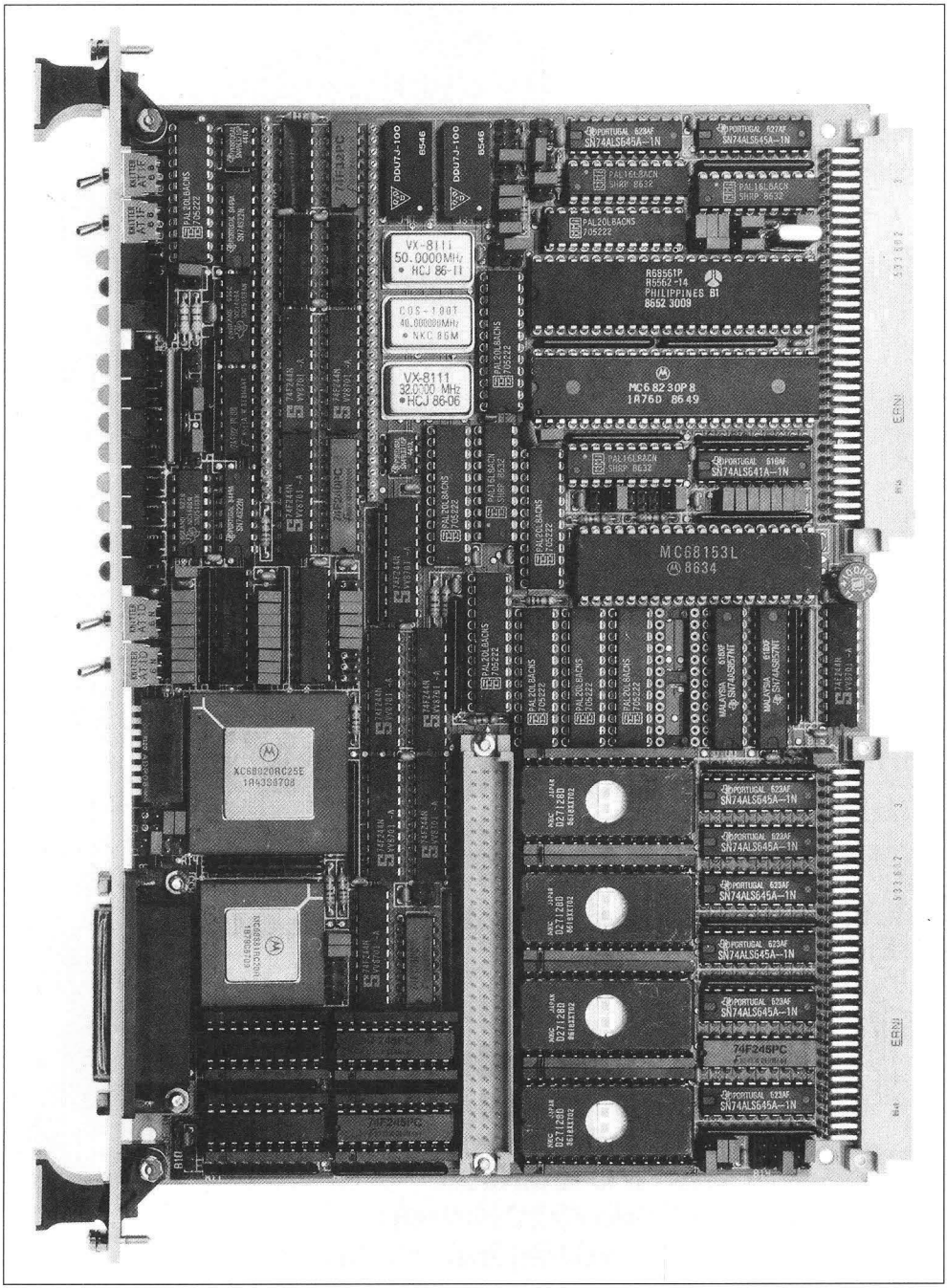
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System 68000 VME SYS68K/CPU-21

68020 Real Time Multi Processor CPU Board

- No Wait State 25 MHz 68020
- 512 K/2 Mbyte Static RAM
- 68881 Floating Point Co-Processor
- 2 Serial I/O Interfaces
- 32 bit wide EPROM Areas
- VMEbus and VMXbus Interface

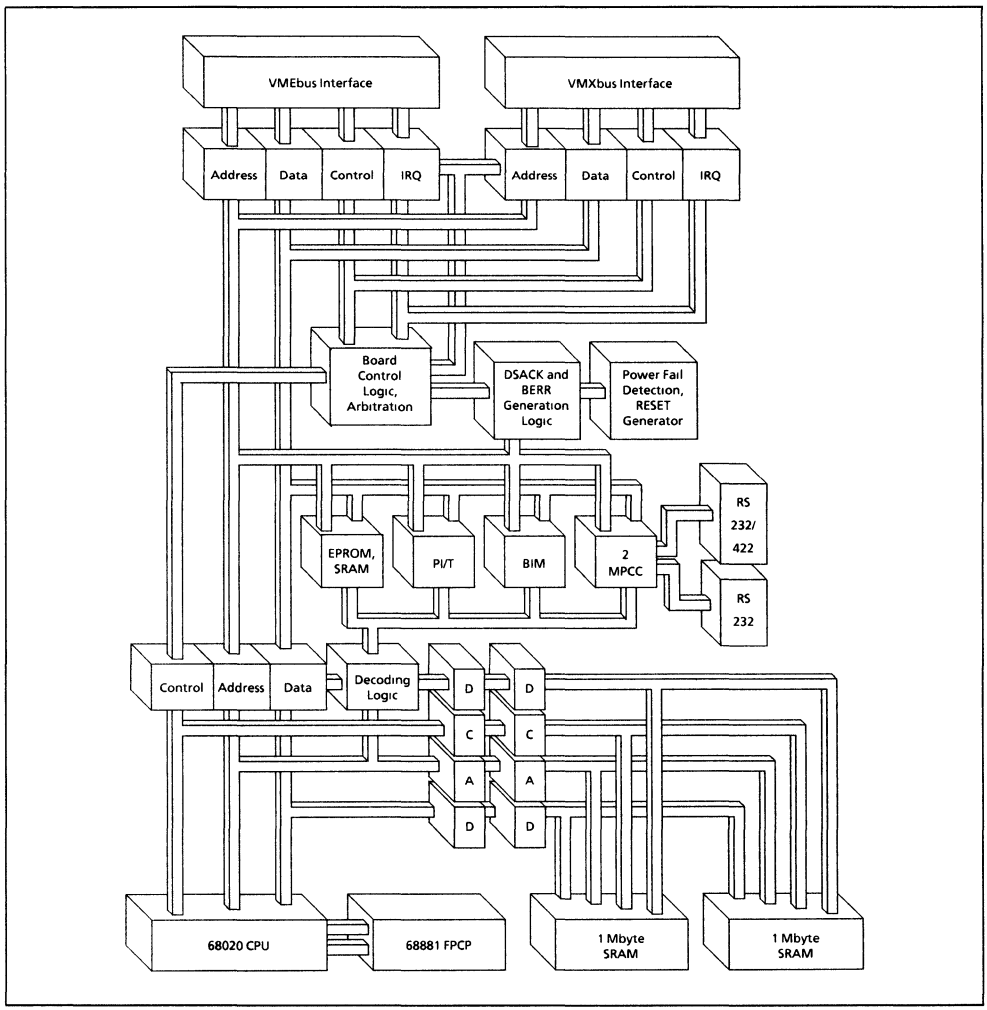

VX-8111
50.0000MHz
• HCJ 86-11
COS-100T
40.000000MHz
• NKC 86M
VX-8111
32.0000 MHz
•HCJ 86-06
R65561P
R5562-14
PHILIPPINES B1
8652 3009
MC68230P8
1A76D 8649
MC68153L
8634
XC68020RC25E
1A4338703
SN74ALS645A-1N
74F245PC

General Description

The SYS68K/CPU-21 is an ultra high speed CPU board designed around the true 32 bit 68020 CPU. The board is built for the VMEbus/IEEE 1014 standard environment and offers 8 sockets for JEDEC compatible devices (EPROMs or SRAMs), two serial ports, a local control device as well as the advanced floating point co-processor 68881 (CPU-21).
A static RAM (512 Kbyte) is installed on the CPU-21 to provide zero wait state operation at 12.5 to 25 MHz on read and write cycles.

The SYS68K/CPU-21A with its 20 MHz CPU runs without the insertion of wait states out of 512 Kbyte SRAM and the SYS68K/CPU-21B with its 25 MHz CPU runs also without the insertion of wait states out of 512 Kbyte SRAM.
A powerful real time multitasking monitor called VMEPROM is included. It features over 50 commands for debugging, task management, file management 68020/68881 line assembler/disassembler.
A photo of the SYS68K/CPU-21 is shown on the left page while the block diagram of the SYS68K/CPU-21Y is shown below.

BLOCK DIAGRAM OF THE SYS68K/CPU-21Y



Features of the SYS68K/CPU-21

- 68020 CPU (12.5 MHz) on CPU-21S
  68020 CPU (16.7 MHz) on CPU-21
  68020 CPU (20.0 MHz) on CPU-21A
  68020 CPU (25.0 MHz) on CPU-21B
- 68881 Floating Point Co-Processor
- 68561 Multi-Protocol Communications Controllers for Serial I/O (one RS232 and one RS232/RS422 compatible interface)
- 68230 Parallel Interface and Timer for local control, interrupt level control and timer function
- 68153 Bus Interrupter Module for all local interrupts
- 512 Kbyte or 2 Mbyte of zero wait state static RAM via the FLME interface (jumper selectable access address)
- 4 Sockets for EPROMs (32 bit wide) for 8K x 8 to 64K x 8 organized devices
- 4 stacked DIP sockets for EPROMs/SRAMs (32 bit wide) for 8K to 64K x 8/8K x 8 to 32K x 8 devices. The maximum EPROM capacity is 512 Kbyte by using eight 27512 devices, the maximum SRAM capacity is 128 Kbyte by using four 32K x 8 SRAMs
- Fully buffered local address and data bus
- VMX Primary Master Interface (32 bit)
- VME IEEE 1014 interface (VMEbus) supporting unaligned transfers (32 bit)
- Single level bus arbiter
- Software selectable bus release functions (6)
- Interrupt handler (1-7 static)
- Bus Timer for BERR generation on local bus, VME IEEE 1014 bus and VMXbus
- Power Fail Detector and RESET generator
- RESET and TEST switch
- RUN/HALT switch
- CACHE enable/disable switch
- RUN/HALT/Bus Master/SRAM Access and Wait State indication LEDs
- Powerful real time monitor/debugger, called VMEPROM, included.

1.0 Hardware Description

1.1 The 68020 CPU

The 68020 with its 32 bit address and data bus is implemented on the board to take full advantage of the 32 bit VME IEEE 1014 bus structure.
A cache of 256 words is installed on the CPU to reduce bus overhead by eliminating op-code fetches. A CACHE switch is installed on the front panel to provide easy software debugging through enabled or disabled CACHE via hardware (the switch overrides the software commands).

The 68020 offers additional instructions to the 68010 such as string manipulations, extended branches over the whole 4 Gbyte addressing space, check and set instructions as well as enhanced exception handling (3rd stack pointer for interrupts) etc.
Dynamic bus sizing (8, 16 or 32 bit ports are defined) and the 32 bit structure offers maximum throughput in conjunction with the 32 bit wide memory such as the connectable static RAM boards which provide zero wait state operation on read and write cycles (CPU clock frequency is 16.7 MHz). In this case 2-3 MIPs computing power are available.
The CPU communicates to the local I/O and memory through a full buffered address and data bus.

1.2 The Floating Point Co-Processor

The SYS68K/CPU-21 is fitted with a 68881 FPCP. The clock frequency of the CPU and the FPCP are identical. The FPCP conforms to the IEEE Floating Point standard 10.0.
Easy Floating Point operation control to the Co-Processor is provided because the intercommunication between the CPU and the FPCP is built in silicon.
An internal register set of 8 general purpose registers (80 bit wide) yields fast execution times.
The performance of the FPCP can be easily upgraded by changing the quartz oscillator frequency (as faster versions become available).

Features of the FPCP:

- 8 General purpose Registers (80 bit, 64 bit Mantissa, 15 bit Exponent and one Sign bit)
- 67 bit on chip ALU
- 67 bit barrel shifter
- 46 Instruction Types including 35 Arithmetic Operations
- IEEE P754 standard (draft 10.0)
- Full support of trigonometrical and logarithmic functions such as:
  sine and cosine
  tangent and cotangent
  Hyperbolic functions (tangent, arc tangent, sine and cosine)
  Logarithmic functions (4)
  Square Root and Exponential functions (4)

1.3 The Serial I/O Channels

The SYS68K/CPU-21 board contains two Multi Protocol Communications Controllers (68561 MPCC) which support the following protocols:

- Character Oriented Protocols
  BSC, DDCMP, X3.28, X.21
  ECMA16
- Synchronous Bit Oriented Protocols
  SDLC, HDLC, X.25
- Even, Odd or no Parity check
- CRC check selectable
- Eight character receiver and buffer register
- Software Programmable Baud Rate from 110 to 38400 Baud
- DC data Rate up to 4 Mbit/s

An RS232 compatible interface (first port) is installed on the board to provide direct connection to standard terminals. The user can select between a RS232 and a RS422 compatible interface on the 2nd serial port.
The I/O signal assignment of the 4 input and output signals per port to the two 25 pin D-sub connectors on the front panel is jumper selectable.
Each MPCC is able to issue an interrupt on a software programmable level to the CPU. The interrupt vectors are also software programmable.

1.4 The Local Control PI/T

A Parallel Interface and Timer Module (68230 PI/T) with 8 MHz clock frequency is installed on the board to provide timer function as well as local control.
All interrupt levels of the CPU (1 to 7) can be separately enabled or disabled via port B of the PI/T.
Eight DIP-switches for data input and configuration selection (memory size, baud rate etc.) are installed on the front panel and readable via port A of the PI/T.
The SYSFAIL and ACFAIL signal of the VMEbus is routed to the handshake pins of the PI/T to generate an interrupt or exception. The interrupt request signal of the VMXbus is also routed to one handshake input to generate an interrupt to the 68020.
The availability of the Floating Point Co-Processor can be sensed through the PI/T.
The bus release functions of the VMEbus (ROR, RAT, RATAR, RATBCLR, RORAT, RORRAT) are SOFTWARE selectable through port C of the PI/T.
The PI/T includes a 24 bit programmable timer with 5 bit prescaler. The Timer can be used for time measurement or as a time base for operating systems. The Timer as well as the signals, connected to the handshake port can issue an interrupt to the CPU on a software programmable level. The interrupt vector is also software programmable.

1.5 The Local Interrupt Handler

A Bus Interrupter Module (68153 BIM) is installed on the board to provide a software programmable interrupt level for each of the on-board interrupt sources.

Local Interrupt Sources

Interrupter	Device
TEST SWITCH	Switch
Serial Channels	MPCC
Timer	PI/T
ACFAIL	PI/T
SYSFAIL	PI/T
VMX-IRQ	PI/T

The CPU-21 will only request VMEbus mastership if the access address is within the VMEbus range or if a VMEbus interrupt has to be acknowledged.

1.6 Local Memory

The local memory consists of 8 sockets for JEDEC compatible devices, 4 SYSTEM EPROM sockets as well as 4 USER sockets. The memory organization is 32 bit wide for the SYSTEM and the USER area to provide maximum throughput of the 68020 CPU.

The following device types are supported:

Device Type	Organization	SYSTEM Area capacity	USER Area capacity	TOTAL capacity
2764	8K x 8	32 Kbyte	32 Kbyte	64 Kbyte
27128	16K x 8	64 Kbyte	64 Kbyte	128 Kbyte
27256	32K x 8	128 Kbyte	128 Kbyte	256 Kbyte
27512	64K x 8	256 Kbyte	256 Kbyte	512 Kbyte
6264	8K x 8	–	32 Kbyte	32 Kbyte
62256	32K x 8	–	128 Kbyte	128Kbyte

The board is fitted with the VMEPROM (in 4 EPROMs 27256) and 4 SRAMs 6264 for standalone operations. If the exception vectors can be stored in another address (i.e. $0) the USER area can be used for additional EPROMs.
The access time of the SYSTEM and the USER area are independently jumper selectable between 100 and 400 ns.

1.7 The Local Memory Extension

The CPU-21 contains a local extension (FLME) interface (32 bit wide) for ultra high speed static RAM connection. This fully buffered local memory extension bus is connected to the 3rd 96 pin DIN connector in the middle of the board.
The access address and the capacity of the RAM area is jumper selectable in the whole 4 Gbyte address space. All of the decoding and driver/receiver logic is installed on the CPU-21 board.
512 Kbyte of SRAMs is installed on the CPU-21 and 2 Mbyte is installed on the SYS68K/CPU-21Y series of boards.
The access time of 35ns allows to operate at 25 MHz CPU clock frequency without insertion of any wait states. The FLME Memory can be extended by using a SRAM-22 board.
CPU-21A memory extention is supported by the SRAM-22A and for CPU-21B memory extension is supported by the SRAM-22B.

1.8 The Local Control

A local RESET generator is installed on the board to provide a RESET to all of the on-board devices. The RESET is generated, if the Power Fail detector detects a supply voltage of lower than 4.75V, if the RESET switch on the front panel is pushed or if the SYSRESET from the VMEbus is active.
A TEST switch is installed to provide self test or application dependent interrupt handling. The DEBUGGER of the CPU-21 supports the TEST switch as level 7 interrupt (Software Abort).
Additionally a RUN/HALT function switch is installed for easy multi-processor software debugging.
RUN/HALT, VME Bus Master, Local RAM extension access and EPROM access are shown on the front panel through LEDs.
6 LEDs on the front panel show the number of wait states inserted by the 68020 CPU.

1.9 The VMEbus Interface

A full 32 bit VMEbus/IEEE 1014 standard interface is implemented on the CPU-21 to communicate to global RAM – and I/O cards.
The 4 Gbyte address space of the 68020 is fully decoded and 8, 16, 24 and 32 bit data transfers are supported as listed below:

Transfer Type	D31 – D24	D23 – D16	D15 – D8	D7 – D0	Note
Byte			x		
				x	
Word			x	x	
Long-Word	x	x	x	x	
Unaligned	x	x	x		1
Transfers		x	x		1
		x	x	x	1
Read Modify Write				x	1
			x	x	1
	x	x	x	x	1

Note 1: According to the VMEbus specification Rev.C and the IEEE 1014 specification.

The support of the unaligned transfer allows the 68020 CPU to operate with its maximum throughput because a 16 bit transfer to an odd address is now legal and needs only 1 bus cycle. If the unaligned transfer is not supported, 2 bus cycles are needed because the single transfer has to be split into 2 cycles.
To enable the support of 16 bit memory boards, the size of the VMEbus address space is programmable (16 or 32 bit wide) via the PI/T.
A single level arbiter is installed on the CPU-20/21 to build small environments without the need for a special system controller. The arbitration level on which the board requests the VMEbus mastership is jumper selectable to level 0, 1, 2, and 3.
Powerful software programmable bus release functions are installed on the board such as:

a) RAT	Release after Time-Out
b) RATAR	Release after Time-Out if Request is pending
c) RATBCLR	Release after Time-Out if bus clear is active
d) ROR	Release on Request
e) RORAT	Release on Request after Time-Out
f) RORRAT	Release on Request and Release after Time-Out

The VMEbus Interrupt Request Signals (IRQ 1-7) are jumper selectable to provide full multiprocessing.
A bus timer for BERR generation during VMEbus accesses is installed. Additionally a Power FAIL detector and a SYSRESET generator is provided on the board.

1.10 The VMXbus Interface

A full 32 bit VMX Interface is installed to allow high end configurations for multi-processing applications as shown below:
The Primary Master Interface allows the connection of up to 5 other VMXbus boards which may be RAM boards, special I/O boards as well as proprietary boards (i.e. Graphics Controller).
The 32 bit data path (D32NA) allows the following transfer types:

WRT	Write Cycles
RD	Read Cycles
RMW	Read Modify Write Cycles
ADDR	Address Only Cycles

Aligned and Non-Aligned Transfers are supported from the CPU-21.
The Slave Boards may respond to the CPU as follows:

SD	Standard Data
SDE	Standard Data Error Response
LD	Late Data Response
LDE	Late Data Error Response

The VMXbus Interrupt request is supported and handled through the on board PI/T. The IRQ level and the IRQ vector are software programmable.

2.0 Software Description

VMEPROM is an EPROM based real-time monitor. The complete package resides in 128 Kbyte of EPROM and uses a minimum of 32 Kbyte of RAM. VMEPROM is composed of the powerful PDOS real-time kernel and the PDOS file manager. Thus the package provides support of a highly sophisticated real-time kernel and an interface to floppy and hard disk drives.
The user interface contains more than 50 commands perfectly suited for program debugging, host computer communications, as well as task- and file management. In addition it includes a powerful line assembler and disassembler for the 68020 and the 68881.

2.1 Features of the VMEPROM

- Real-Time Multitasking Kernel supporting up to 64 tasks.
- File Management support for sequential, random and shared files. Up to 64 files may be opened at the same time.
- Line assembler/disassembler with full support of all 68020/68881 instructions.
- Over 20 commands for program bedugging, including breakpoints, tracing, processor register display and modify.
- S-record up/downloading from any port defined in the system.
- Disk support for RAM-disk, floppy and winchester disks. Either a SYS68K/WFC-1 or a SYS68K/ISCSI-1 mass memory controller may be used. VMEPROM also allows disk formatting and initialisation.
- Serial I/O support for up to two SIO-2 or ISIO-1/2 boards in the system.
- EPROM programming utility using the SYS68K/RR-2/3 boards.
- Full Screen Editor.
- I/O redirection to files or ports from the command line.
- Over 100 system calls to the kernel are supported.

2.2 Description of the User Interface of VMEPROM

The user interface of VMEPROM allows I/O redirection to files or to any port defined within the system. Multiple command lines may be entered on a single command line. The user console input is interrupt driven and allows type-ahead. Over 60 commands are built into the VMEPROM user interface and are directly accessible without destroying memory. The Command set covers functions such as program execution, breakpoints, tracing and a powerful line assembler/disassembler. Also resident are file system functions such as append, delete, copy, rename and show file. These are applicable for RAM disk, floppy or hard disk. The task management functions cover create task, kill task, alter task priority and list tasks.

2.3 Description of the Kernel Functions

The kernel of VMEPROM is written in 680 x 0 assembly language for fast and efficient execution. It provides multitasking, system clock, event processing and memory management. Ready tasks are scheduled with a prioritized round-robin method. Up to 64 tasks may be defined simultaneously.
Semaphores and events provide a low overhead facility for one task to signal another. Messages and mailboxes are used in conjunction with task lock, unlock, suspend and event primitives.

2.4 Description of the File Manager Functions

The file manager module provides sequential, random, read only and shared access to named files on RAM disk, floppy or hard disk. New files are automatically defined contiguously to improve access speed.

2.5 Supported VMEbus Hardware

Upon power up, VMEPROM checks the VMEbus for the availability of several controller boards. Supported are up to two serial I/O boards, and one disk controller.
In addition, EPROM programming is supported by VMEPROM utilising the SYS68K/RR-2/3 board family.

2.6 Target System Support

VMEPROM can easily be used in target systems. For these systems, the application program can be put into EPROM with or without the user interface. The application programs can be started either by a command line or directly after reset without user input.
The minimum EPROM space required by the VMEPROM kernel and file manager is about 40 Kbytes. Small romable applications can be put in EPROMS easily without the overhead of the user interface.

2.7 Development Systems

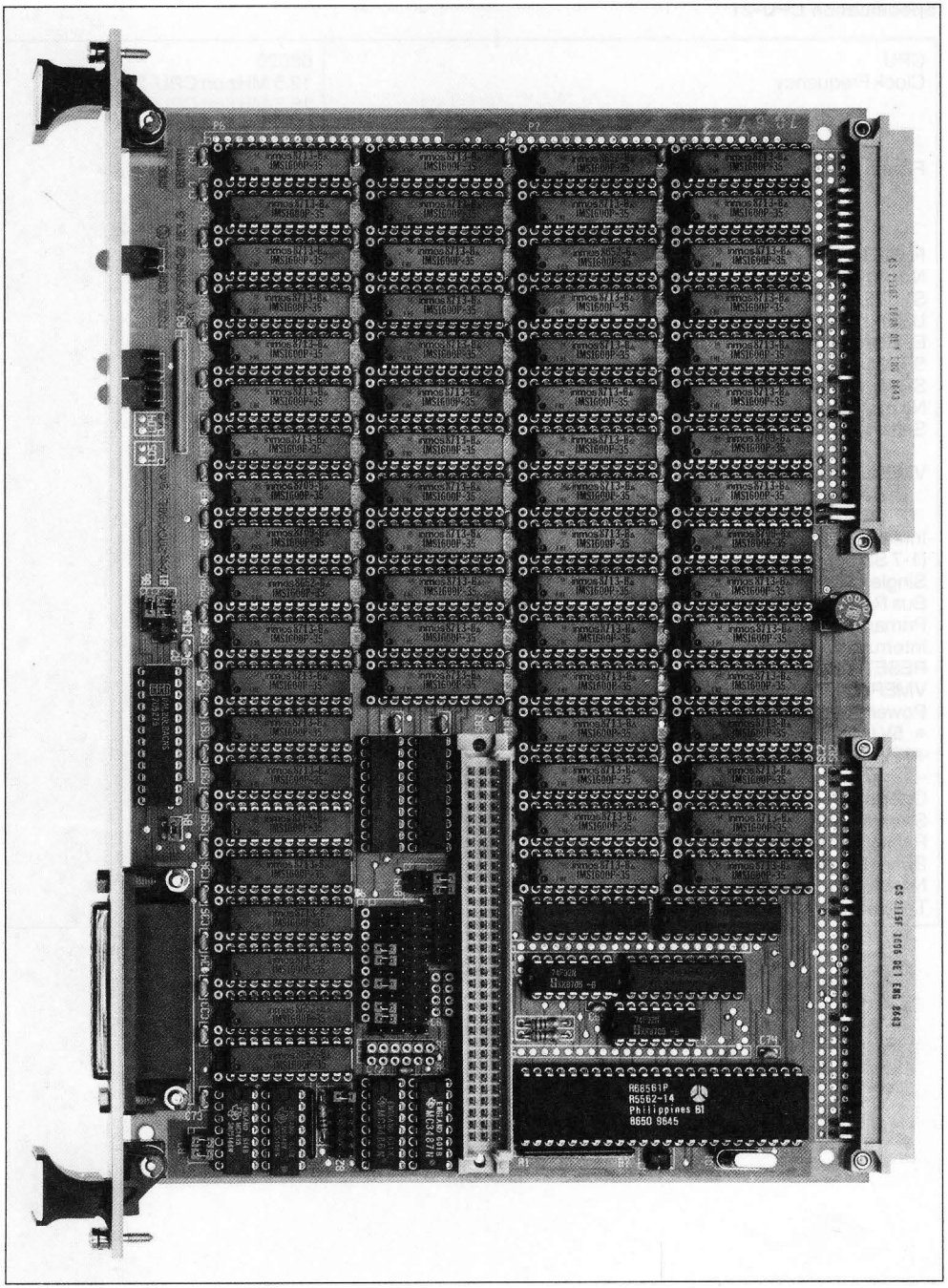
Currently either one of the FORCE PDOS* or UNIX System V* development stations may be used for software development for VMEPROM.
Compilers, Assemblers, and Libraries are available together with utilities for program downloading. These tools are well suited to help in program development and debugging.

2.8 Licensing

No license is required for VMEPROM. VMEPROM is delivered free of charge with every CPU-21 board.

Specification CPU-21

CPU	68020
Clock Frequency	12.5 MHz on CPU-21S 16.7 MHz on CPU-21 20.0 MHz on CPU-21A 25.0 MHz on CPU-21B
Floating Point Co-processor	12.5 MHz on CPU-21S 16.7 MHz on CPU-21 20.0 MHz on CPU-21A 20.0 MHz on CPU-21B
FLME Memory	512 Kbyte
No of Wait States	0
SYSTEM EPROM sockets	4
USER EPROM sockets	4
EPROM capacity (max)	512 Kbyte
SRAM capacity (max)	128 Kbyte
SRAM capacity at delivery for VMEPROM	32 Kbyte
No of Wait States	2
Serial I/O Interfaces	1 RS232 1 RS232/RS422
VMEbus Interface IEEE 1014	
A32, A24, A16	x
D32, D24, D16, D8	x
Interrupt Handler	
(1-7 Stat)	x
Single Level Arbiter	x
Bus Release Functions	6
Primary VMXbus Interface (D32NA)	x
Interrupt Handler	x
RESET, TEST, RUN and CACHE switch	x
VMEPROM Firmware	128 Kbyte
Power Requirements	
+ 5V (max)	5.3A (2x)
+12V (max)	0.2A (1x)
−12V (max)	0.2A (1x)
Operating Temperature (degree C)	0 to 50
Storage Temperature (degree C)	−40 to 85
Relative Humidity (Non-condensing)	0 to 95 %
Board Dimensions 234 x 160 mm (9.2 x 6.3")	x
No. of Slots used	2
Thickness	38 mm (1.39")


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General Description
The SYS68K/SRAM-22 is an ultra high speed static RAM board designed for the 68020 processor board, CPU-21.
The static memories are 64K x 1 oriented and have an access time of as low as 45ns. This allows operation of the 68020 at a clock frequency of up to 20MHz without any wait states. Therefore, maximum throughput is provided using the SRAM-22 board.

1.0 Hardware Description

1.1 The Static RAM
The memory organisation is 32 bit wide (512 Kbyte in total) to allow maximum throughput for the 68020. Aligned and unaligned transfers are supported because each byte strobe is separately controlled via a decoding logic on the local memory expansion. Zero Wait State operation of 16.7 MHz processor clock frequency is provided using 55ns devices.

Two banks (32 chips each) are associated with one SRAM board. 2 LEDs show if an access is pending to one of the two memory banks.
To support the higher clock frequency of CPU-21A, the SRAM-22A is equipped with 45ns devices.
The RAM extension for CPU-21A can only be made with SRAM-22A.

1.2 Serial I/O Interface
A Multi Protocol Communications Controller (68561 MPCC) is installed on the SRAM-22 to provide an additional serial communication channel. The interface type is jumper selectable between RS232 and RS422 driver/receiver circuits.
A jumperfield offers flexible I/O signal assignment to the 25 pin D-sub connector on the front panel.

Specification SRAM-22

Memory Capacity	512 Kbyte
Access Time of SRAMs	70ns on SRAM-22S 55ns on SRAM-22 45ns on SRAM-22A 35ns on SRAM-22B
No. of SRAMs	64 (64K x 1)
Serial I/O Channel	1
RS232 interface	x
RS422 interface	x
Power Requirements	
+ 5V (max)	2.8A
+12V (max)	0.1A
−12V (max)	0.1A
Operating Temperature (degree C)	0 to 50
Storage Temperature (degree C)	−40 to 85
Relative Humidity (non-condensing)	0 – 95 %
Board Dimensions	
234 x 160 x 18 mm (9.2 x 6.3 x 0.71")	x

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