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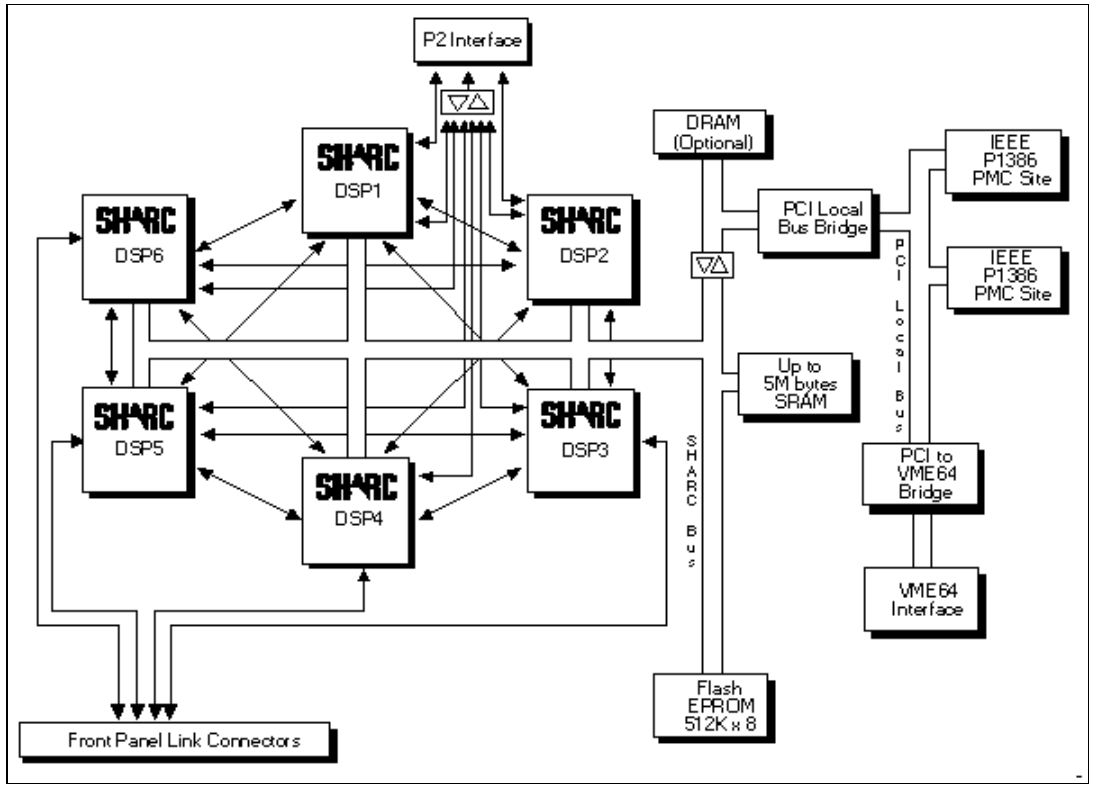
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Find the *Emerson / Motorola / Loughborough DBV66/0P6-033* at our website: ***Click HERE***

DBV66 720 MFLOPS 6U VME Board

- **Six ADSP-2106x (SHARC) DSP processors arranged in a single cluster**
- **720 MFLOPS (peak) in a single 6U VME slot**
- **VME64 Master/Slave interface**
- **Two IEEE P1386 standard PMC sites, accessed via 64 bit PCI Local Bus**
- **Up to 512K x 48 global shared 0ws SRAM, plus optional 512K x 32 global shared 0ws SRAM**
- **512K x 8 global Flash EPROM**
- **Option of up to 64M bytes DRAM (available on 1 PMC site)**
- **Comprehensive software support**



Description

The DBV66 is part of Loughborough Sound Images' DBV6x family of 6U VME boards. These boards provide a complete real-time multi-processing solution for advanced signal processing applications.

The foundation of the DBV6x family is Analog Devices ADSP-2106x (SHARC) DSP. Each processor is capable of 120 MFLOPS peak performance at 40 MHz and includes a large on-chip SRAM (up to 4M bits). This memory is dual-ported to support the 10 internal DMA engines which concurrently drive the six 40M bytes/sec link-ports and 160M bytes/sec external bus.

On-chip multi-processor arbitration allows the ADSP-2106x's on the DBV66 to be grouped together in a cluster coupled via shared memory, with each SHARC processor able to access the internal memory of the others in the cluster. The processors on the DBV66 are arranged in a single optimum cluster of six that exploits to the maximum the on-chip multi-processing support present in the ADSP-2106x.

Global shared memory is provided to all processors, offering up to 512K x 48 0ws SRAM for program or data memory, with an optional 512K x 32 data memory area and 512K x 8 flash EPROM for boot code.

For access to larger areas of memory, LSI offer an optional DRAM mezzanine which occupies an extended PMC site, providing up to 64M bytes of DRAM onto the ADSP-2106x external bus.

The DRAM module is buffered from the ADSP-2106x external bus to allow download of data via the host or PMC I/O peripherals into the DRAM store without adversely affecting the ADSP-2106x bus bandwidth.

A key feature of the board is the integrated open standard I/O provided. The DBV66 has two IEEE P1386 compliant PMC sites, which offer a physical interface to the board's front panel. Access to a wide variety of off-the-shelf solutions including signal I/O, memory upgrades, standard bus interfaces and further processor upgrades is provided via the PCI Local Bus to ADSP-2106x bus bridge.

ADSP-2106x link ports (40M bytes/sec each) are the principle vehicle for multi-processor inter-connections. The block diagram shows the innovative inter-connection of link ports on the DBV66, with each processor connected to its nearest 4 neighbours in the ring. One link port from each processor is routed off-board, four via the front panel and two via the VME P2 connector. The six remaining link ports (one from each processor) are wired together to form a single link port bus and buffered off-board via P2. This provides a high speed multi-processor boot/program download facility. Scaleable multi-board systems can be built up by interconnecting the link ports between any DBV6x family VME board.

Each ADSP-2106x processor has two serial ports, SPORT0 and SPORT1. On the DBV66, SPORT0 and SPORT1 from each processor are connected to SPORT0 and SPORT1 on all other processors to form two TDM serial channels. These serial channels are both available on the P2.

The DBV66 has a VME64 Master/Slave interface capable of operating at peak 70M bytes/sec. This is accessed from the processor cluster via the 64 bit PCI Local Bus, which has a peak data rate of 264M bytes/sec.

DBV66 Specification Summary

Processor	720 MFLOPS peak performance (40 MHz processors) from six ADSP-2106x processors. Chip features include up to 4M bits on-chip 0ws SRAM, six 40M bytes/sec inter-processor communication link ports and direct support for up to six processor global shared memory systems.
Shared Memory	Up to 512K x 48 0ws SRAM, plus optional 512K x 32 0ws SRAM, shared memory between each processor and the VMEbus interface. 512K x 8 flash EPROM.
DRAM	Up to 64M bytes of 1ws DRAM available on ADSP-2106x external bus via extended PMC mezzanine.
VMEbus Interface	VME64 Master/Slave interface operating at up to peak 70M bytes/sec.
Serial Ports	Two TDM serial ports available on the P2.

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System Expansion	Four ADSP-2106x link ports available on front panel and two link ports plus the one common link port available on the P2.
I/O Expansion	Two IEEE P1386 PMC sites on-board, remaining within single slot 6U size.

Software Support

A complete range of software support is available for the DBV66. Development tools are PC-based or SPARC-based: a debugger, C compiler, optimised signal processing library and DSP operating system support are available. Support is also provided for host communications from the ADSP-2106x via an extension to the C compiler and there is device driver and host interface library support for a range of VME operating systems.

Complete Development Tool Set from ADI

- Most efficient C compiler available for DSP
- Simulator and C source-level debugger
- DSP/C Numeric C extension (ANSI X3J11.1)
- Intuitive Assembly language

Multi-processor Target Debuggers

- EZ-ICE/ICEPAC: JTAG In-Circuit-Emulator

C-callable Runtime Libraries

- Optimised vector/math functions
- ADI's Runtime library of ANSI-standard functions

Host Support

- Host monitor, drivers, libraries and utilities
- Range of VME operating systems to be supported (initially SunOS 4.1.x)

3rd Party Software Support

- Multi-processing OS support (SPOX, Virtuoso, etc.)

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