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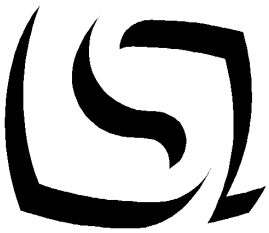
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ADSP-2106x Carrier Board

Technical Reference Manual

Version 1.04 April 1998

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1 Introduction

This Technical Reference Manual describes the features and functions of Loughborough Sound Images' (LSI's) DBV66 board. DBV66 provides a systems-level solution to a diverse range of real-time data acquisition and signal processing applications. The features of DBV66 include:

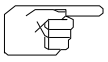
- Up to six Analog Devices ADSP-2106x (SHARC) Digital Signal Processors.
- The SHARC external ports are interconnected providing each SHARC with access to the internal resources of all SHARCs on DBV66. Each SHARC also has shared access to external banks of SRAM, Flash Memory and optional DRAM. The DRAM is provided on LSI DRAM66 modules providing a flexible memory upgrade facility.
- DBV66 provides an on-board PCI bus which allows up to two single width or one double width PCI Mezzanine Card (PMC) to be located on-board. PMC modules provide DBV66 with optional processing, I/O and memory facilities.
- DBV66 provides a full VME master/slave interface. Each SHARC or PMC module can access the VMEbus via the on-board PCI bus. VME masters have access to all resources on DBV66.
- The SHARC parallel link ports are implemented for bidirectional inter-processor communication both on and off-board.
- The SHARC synchronous serial ports are grouped together to form two Time Division Multiplexed ports. These ports are routed off-board providing access to a wide variety of serial communication protocols.
- A standard RS-232 serial port is provided supporting full-duplex asynchronous operation.
- Support for Analog Devices' ICEPAC and EZ-ICE systems for non-intrusive software debug.
- Extensive software support is available for DBV66 including a graphical software configuration tool, host interface library software and SHARC utility functions.

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1.1 Conventions

This manual uses the following conventions:

- Analog Devices' ADSP-21060 and ADSP-21062 range of DSPs are referred to as the 'SHARC' throughout this manual unless a reference is specific to a device.
- SHARC and VME active low signals are indicated by '/' preceding the signal name; for example, /GRESET. PCI active low signals are indicated by '#' following the signal name; for example, INTA#.
- Hexadecimal numbers are followed by 'h'; for example, the address 2000 0000h.
- SHARC addresses are distinguished from PCI bus and VMEbus addresses by giving them in italics; for example, SHARC external memory begins at *0040 0000h*.
- PCI addresses given in this manual for accesses to DBV66 local resources from the PCI bus assume the default remappings which are described in Section 4.5.1.
- The SHARC I/O Processor registers are indicated by 'IOP' preceding the register name. The SHARC Core Processor registers are indicated by 'Core' preceding the register name.
- Names of SHARC registers and register bits are given in italics to differentiate between them and those of DBV66; for example, the SHARC IOP *WAIT Register*.
- Hypertext links in this manual are shown in green.
- Throughout this manual references are made to the March 1995 edition of Analog Devices' ADSP-2106x SHARC User's Guide.



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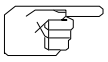


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1.2 Using This Manual

This Technical Reference Manual (TRM) describes the features and functions of Loughborough Sound Images' (LSI's) DBV66 board. The contents of each chapter are summarised below.



This TRM is also provided in an online format which can be viewed and printed using the Adobe Acrobat Reader software provided. Refer to Section 2.4 for more details.

Chapter 1 provides overview material for users new to the SHARC processor and DBV66 board. Each of the main features of the board are outlined along with references to more detailed information later in the manual.

Chapter 2 describes how to install PMC, DRAM66 and ICEPAC modules onto DBV66 and then install the board into a VME rack.

Chapter 3 details the resources accessible to the SHARCs on DBV66.

Chapter 4 covers the implementation of the PCI bus on DBV66. This includes information on using PMC modules with DBV66.

Chapters 5 and **6** describe the DBV66 VME slave and master interfaces respectively.

Chapter 7 provides information on the implementation of the SHARC link ports on DBV66.

Chapter 8 describes the implementation of the SHARC serial ports on DBV66.

Chapter 9 covers the interrupt facilities provided on DBV66.

Chapter 10 outlines the use of the JTAG emulation system on DBV66 for non-intrusive software debug.

Chapter 11 describes the various hardware and software reset sources on DBV66.

Chapter 12 focuses on the software debug features provided on DBV66 in addition to the JTAG emulation system.

Appendix A provides a short tutorial on allocating the internal memory of the SHARCs for program and data storage.

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Appendix B provides the default settings of the PCI9060 registers on DBV66. These settings are provided for the advanced configuration required if LSI's DBV66 support software is not used.

Appendix C provides details on how DBV66 transfers individual bytes of data between the board and the VMEbus.

Appendix D details the optional P2 Breakout Board which allows the easy routing of signals to/from DBV66 via the VME P2 connector.

In addition to this TRM, DBV66 is supplied with the documentation listed below. Section 1.4 provides details on how to obtain the PCI bus and VMEbus specification documents.

- Any software support packages purchased with DBV66 are documented in separate User Guides.
- Any PMC module purchased from LSI will be accompanied by a separate User Manual.
- The manufacturer's documentation for the SHARC, PCI9060, Universe and UART devices on DBV66. These manuals/data sheets are supplied in an online format which can be installed, viewed and printed as described in Section 2.4.

Your distributor can provide you with up to date information on LSI's range of related hardware and software products.

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1.3 Overview

DBV66 forms part of a range of boards available from Loughborough Sound Images (LSI) based around Analog Devices' ADSP-2106x Super Harvard ARchitecture Computer (SHARC) Advanced Digital Signal Processor. Figure 1.1 illustrates the basic architecture of DBV66.

DBV66 incorporates either two, four or six SHARC processors, the external ports of which have been interconnected to form a shared parallel bus referred to as the Interconnect bus. This bus provides each SHARC with direct memory-mapped access to the internal resources of the other SHARCs. These internal resources consist of on-chip SRAM blocks and I/O Processor registers.

In addition to the internal SHARC resources, each SHARC has memory-mapped access to the following resources on the Interconnect bus:

- Two banks of SRAM for code and data storage.
- A bank of DRAM on an optional LSI DRAM66 module.
- A bank of Flash Memory for embedded code and data storage.
- An RS-232 serial port for communication with peripherals connected to DBV66 via the VME P2 connector or an on-board header.
- DBV66 registers for control, status and simple I/O.

DBV66 provides a further on-board bus, a Peripheral Component Interconnect bus (PCI bus). The purpose of this bus is to allow up to two PCI Mezzanine Cards (PMC) to be located on-board. PMC modules are compact plug-in modules which typically provide I/O, processing and memory facilities. The provision of the PMC sites allows the functionality of DBV66 to be easily upgraded and altered to suit the application requirements. DBV66 requires a single VME slot whether or not modules are fitted to the board.

The Interconnect bus is interfaced to the PCI bus using a PLX PCI9060 bridge device. The PCI bus is itself interfaced to the VMEbus using a Tundra Universe bridge. By interfacing the Interconnect bus, PCI bus and VMEbus in this way, access is provided between the following devices:

- The SHARCs can access VME slaves and slave PMC modules.
- PMC masters can access the Interconnect bus and VME slaves.
- VME masters can access the Interconnect bus and PMC slaves.

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This architecture also allows the SHARCs to access resources on the Interconnect bus at the same time as accesses are made between a PMC module and the VMEbus. This feature can be exploited by application software to increase system efficiency.

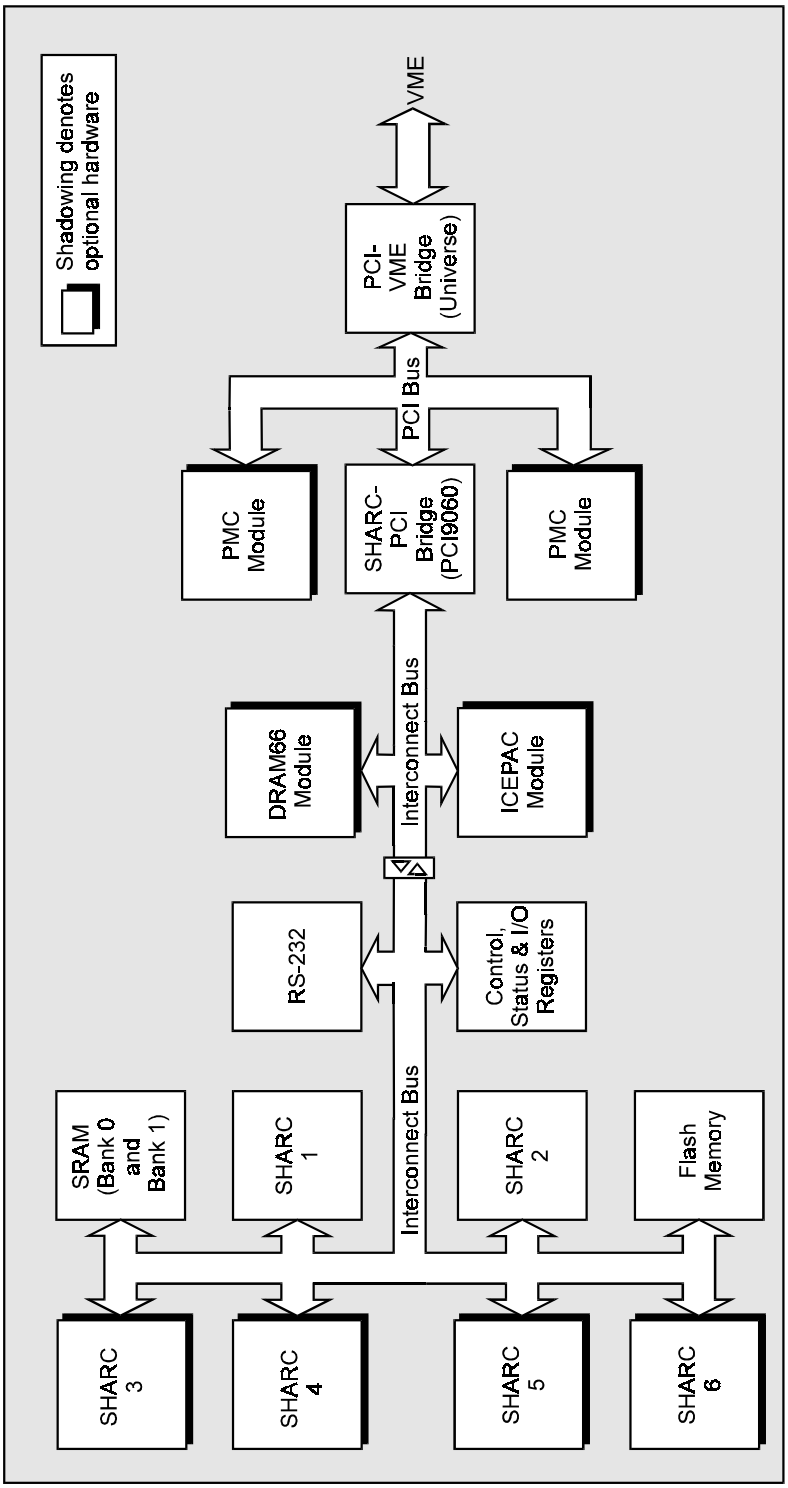
Transparent arbitration is implemented for accesses to the Interconnect bus and PCI bus. In addition to these buses, DBV66 provides the following data transfer routes:

- SHARC-SHARC communication can take place via link port connections. These are either dedicated on-board connections or are routed off-board via the front panel connectors or via user-defined pins on the VME P2 connector.
- The SHARC synchronous serial ports can be routed off-board via user-defined pins on the VME P2 connector for communication with any compatible circuitry.
- The optional PMC Jn4 connector has been provided for each site on DBV66. The connector provides each module with access to user-defined pins on the VME P2 connector.
- The SHARCs, PMC modules and VME masters are provided with access to an RS-232 asynchronous serial port. This port can be routed to compatible circuitry via an on-board header or via user-defined pins on the VME P2 connector.

The following subsections outline each of the main features of DBV66 and provide references to more detailed information.

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Figure 1.1: DBV66 Functional Block Diagram



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1.3.1 ADSP-2106x (SHARC) DSP

Analog Devices' Super Harvard ARchitecture Computer (SHARC) range of processors consists of the ADSP-21060 and ADSP-21062. Variants of DBV66 are available with either two, four or six ADSP-21060 or ADSP-21062 processors.

The only functional difference between the two SHARC variants is the size of on-chip SRAM they provide. The ADSP-21060 provides a total of 4M bits SRAM and the ADSP-21062 provides a total of 2M bits SRAM. This internal memory can be used to store 48 bit instructions and 40, 32 and 16 bit data. Direct program execution from this memory greatly increases processor performance.

The SHARC incorporates three on-chip buses, a program memory bus (PM bus), data memory bus (DM bus) and an I/O bus. The PM bus can be used to access both instructions and data. Therefore, during a single cycle, the processor can access two operands, one over the PM bus and one over the DM bus, an instruction from the cache and perform a DMA transfer over the I/O bus. The architecture of the SHARC is illustrated in Figure 1.2 below.

The DMA controller is part of the I/O Processor which functions independently of the Core Processor. It provides 10 channels for transferring data between external devices and the internal SHARC SRAM. External devices can be connected to the SHARC via the external port, the bidirectional link ports or the serial ports as outlined below:

- **External Port**

  The external ports of all SHARCs on DBV66 are directly interconnected. This provides each SHARC with memory-mapped access to the internal resources of the other SHARCs and a number of other resources on DBV66.

- **Link Ports**

  The I/O Processor incorporates six 4 bit bidirectional link ports. These are provided for high speed interprocessor communication. A number of these link ports have been implemented as dedicated on-board links on DBV66. Others are available off-board via front panel connectors and the VME P2 connector. Each port can operate at twice the processor clock frequency to transfer 8 bits of data/clock cycle.

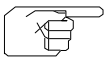
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- **Serial Ports**

  The I/O Processor also provides two synchronous serial ports, SPORT0 and SPORT1. These can be employed on DBV66 for connection to a wide variety of digital and mixed-signal devices via user-defined pins on the VME P2 connector.

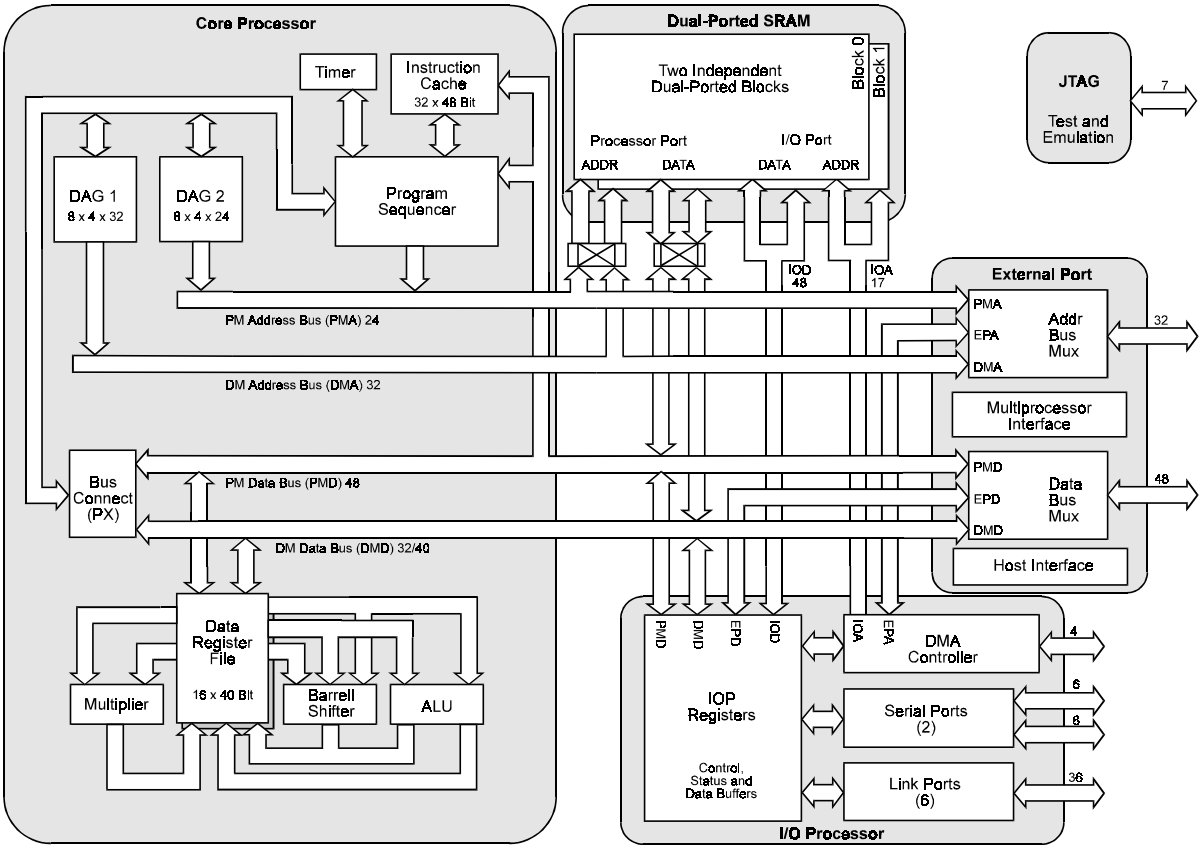
The SHARCs on DBV66 operate from a 40 MHz clock, achieving a performance of 40 Million Instructions Per Second and 120 Million Floating-Point Operations Per Second.

The SHARC provides a JTAG Test Access Port which can be implemented by a JTAG controller, such as an ICEPAC on DBV66, for non-intrusive software debug. DBV66 routes a JTAG scan chain through all six SHARCs and optionally to the PMC sites.



Control and status for the SHARC is provided by a number of internal registers. These registers are located in either the Core Processor or I/O Processor.

Figure 1.2: SHARC Internal Architecture



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1.3.2 Interconnect Bus

The external ports of all SHARCs on DBV66 have been interconnected to form a shared parallel bus referred to as the Interconnect bus. The following resources on the Interconnect bus are accessible from PMC modules and the VMEbus as well the SHARCs:

- **SHARC Internal Resources**

  These consist of two SRAM blocks and a block of 256 I/O Processor (IOP) registers. Accesses can be targeted at specific processors or broadcast to all SHARCs. The internal SRAM blocks are designed to accommodate 48 bit instructions and 16, 32 and 40 bit data. The IOP registers provide control and status for SHARC system configuration and the DMA controller, serial ports and link ports.

- **External Memory**

  The following memory banks are external to the SHARCs and are available on the Interconnect bus:

  - A bank of 128K x 48 or 512K x 48 SRAM for data or temporary instruction storage (Bank 0).
  - A bank of 128K x 32 or 512K x 32 SRAM for data storage (Bank 1).
  - 512K x 8 Flash Memory for embedded instruction or data storage.
  - Up to 16M x 32 of optional DRAM for bulk data storage. This DRAM is available on LSI DRAM66 modules.

- **RS-232 Serial Port**

  An Universal Asynchronous Receiver/Transmitter (UART) device provides DBV66 with an interface to peripheral RS-232 compatible circuitry.

- **DBV66 Registers**

  Four registers are provided for DBV66 control, status and I/O functions.

- **Analog Devices ICEPAC Site**

  An ICEPAC can be located on DBV66 which can be used by host software to control the JTAG circuitry on DBV66. Note that the ICEPAC registers are inaccessible from the SHARCs. This removes the possibility of SHARC code accidentally interfering with JTAG emulation.

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A section of the Interconnect bus is isolated from the SHARCs by transparent buffers. The optional DRAM and ICEPAC registers are interfaced to this section of the bus. The SHARCs access the DRAM as though the buffers were not present. However, accesses from the PCI bus are isolated from the main section of the Interconnect bus. Therefore, for example, the DRAM can be accessed from the PCI bus at the same time as a SHARC makes an access to an external SRAM bank.

The Interconnect bus is interfaced to the PCI bus using a PLX Technology PCI9060 device. This device functions as a bridge between the two buses allowing bidirectional communication between them.

Chapter 3 provides further details on the Interconnect bus.

1.3.3 PCI Bus

An on-board 32 bit PCI bus forms an intermediate bus between the Interconnect bus on DBV66 and the VMEbus. This bus offers transfer rates of up to 132M bytes/sec and is provided to allow PCI Mezzanine Cards (PMC modules) to be located on-board.

The Interconnect bus is interfaced to the PCI bus using a PLX PCI9060 bridge. This software programmable interface allows bidirectional communication between the PCI bus and Interconnect bus. The VMEbus is interfaced to the PCI bus using a Tundra Universe bridge. This is also a software programmable interface which allows bidirectional communication between the PCI bus and VMEbus.

A double width or up to two single width PMC modules can be located on DBV66. These modules are compact plug-in cards and their functionality is module-specific but will typically comprise I/O, processing or memory facilities.

The architecture described above allows the PMC module sites to be accessed from the SHARCs and VME masters. PMC modules with a PCI master capability can access the Interconnect bus and VMEbus. In addition to this, PMC Site 1 on DBV66 has the optional PMC Jn4 connector providing the module with access to user-defined pins on the VME P2 connector.

The facilities provided for use by PMC modules are summarised in Section 4.12.

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1.3.4 VME Master/Slave Interface

DBV66 provides a full master/slave interface to the VMEbus that complies with the VME64 Specification. The VMEbus interface is implemented using Tundra's Universe single chip PCI-VME bridge.

The Universe provides a software programmable VME slave image for DBV66 which can be used to access the PMC sites and the Interconnect bus resources listed below:

- Internal SHARC resources, these consist of two SRAM blocks and a block of I/O Processor registers.
- DBV66 registers, which provide access to various features such as the Broadcast Link Port, which provides a SHARC to SHARC broadcast facility independent of the Interconnect bus.
- The optional ICEPAC registers which can be used to control the DBV66 JTAG scan path circuitry.
- Banks of SRAM and optional DRAM which provide a data transfer system to/from the SHARCs.
- A bank of Flash Memory for embedded code/data storage.
- An RS-232 asynchronous serial port.

DBV66's VME slave interface is discussed in Chapter 5.

The Universe also provides a software programmable VME master interface for DBV66. This allows the SHARCs and PMC modules to make master accesses to the VMEbus via the PCI bus memory and I/O maps. The DBV66 VME master interface is described in Chapter 6.

DBV66 supports D8, D16, D32, D32 block transfers (BLTs) and D64 multiplexed block transfers (MBLTs) VME master and slave accesses. However, due to fundamental differences in the way in which the VME and PCI buses handle individual bytes of data, care must be taken to ensure that data is interpreted correctly once it has been transferred. When making the following transfers, data will always be interpreted correctly by both the SHARCs on DBV66 and the processors on the target board:

- Any transfer between DBV66 and another DBV66 board.
- 32 bit data types transferred using D32 accesses between DBV66 and any another VME board.
- D8 accesses between DBV66 and any another VME board.

If another access type is required then consideration must be made of how bytes of data are transferred between DBV66 and the VMEbus. Refer to Appendix C for more details.

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1.3.5 SHARC Parallel Link Ports

DBV66's parallel processor system can support optimum performance by distributing tasks between two or more processors. High performance multi-processing requires rapid transfer of data between processors. DBV66 achieves this by utilising the SHARC's high speed parallel link ports. Each SHARC provides six 4 bit link ports, each of which can be configured to transfer 8 bits of data per clock cycle. Therefore, at 40 MHz each port can transfer data at up to 40M bytes/s.

DBV66 routes a number of dedicated link ports across the board for on-board SHARC-SHARC communication. A single port from each SHARC is combined to form a Broadcast Link Port (BLP). This port provides each SHARC with the facility to broadcast data to a link port on the other SHARCs. The BLP can also be routed off-board providing a system-wide broadcast facility. In addition to this, individual link ports are accessible off-board via the VME P2 connector and front panel connectors.

The on-board and off-board routing of the link ports is discussed in Chapter 7. The detailed use of the SHARC link ports is discussed in Chapter 9 of the SHARC User's Manual.

1.3.6 SHARC Serial Ports

The SHARC provides two asynchronous serial ports, SPORT0 and SPORT1. The SPORT0 port from each SHARC is combined on DBV66 to form a single Time Division Multiplexed (TDM) port. The SPORT1 ports are also combined to form a further TDM port. Both TDM ports, TDM0 and TDM1, are routed off-board via user-defined pins on the VME P2 connector.

Each TDM port supports up to 32 independent data channels. The SHARCs can be configured to receive/transmit data on any or all of these channels. This allows an external data stream to be automatically shared between processors.

The SHARC serial ports are discussed in Chapter 8 of this TRM and Chapter 10 of the SHARC User's Manual.

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1.3.7 RS-232 Serial Port

DBV66 provides an RS-232 compatible serial interface. This interface is accessible from the SHARCs, PMC modules and VMEbus. The primary purpose of the RS-232 port is to allow DBV66 to be connected, via an on-board header or the VME P2 connector, to a monitor during software debug.

The RS-232 port is implemented using a Philips SCC2691 Universal Asynchronous Receiver/Transmitter (UART) device. The details specific to using this device on DBV66 are provided in Section 3.6. General details on using the device are provided in the Philips Product Specification for the UART, see Section 2.4.

1.3.8 Interrupts

DBV66 provides the SHARCs, PMC modules, VMEbus and ICEPAC modules with the following interrupt capabilities:

- The SHARCs can generate VME interrupts.
- PMC modules can interrupt the SHARCs and generate VME interrupts.
- VME interrupts can be monitored and routed to the SHARCs.
- The RS-232 port can generate interrupts to the SHARCs and the VMEbus.
- Internal sources in the PCI9060 can generate interrupts to the SHARCs or the VMEbus.
- Internal sources in the Universe can generate interrupts to the PMC modules, the SHARCs or the VMEbus.
- An interrupt can be generated to the SHARCs via a user-defined pin on the VME P2 connector.
- An ICEPAC can generate VME interrupts.

In order to allow interrupts to be routed on and off-board on DBV66, a number of interrupt lines are interconnected. The lines are either directly interconnected or connected via the PCI9060 and Universe devices. Refer to Chapter 9 for more details.

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1.3.9 JTAG Emulation System

A JTAG emulation system can be set up to download and develop parallel multi-processor software. DBV66 provides support for Analog Devices' EZ-ICE and ICEPAC systems which can be used to control the JTAG system. Note that only one of these systems can be used with DBV66 at any particular time.

The EZ-ICE system consists of a PC-resident card which is connected to DBV66 via ribbon cable. PC-hosted software is also provided which is used for downloading and debugging SHARC code.

The ICEPAC system consists of a module which is located on DBV66. Software is also provided which runs on a VME host and employs the ICEPAC to control the JTAG circuitry.

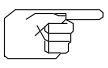
Chapter 10 provides further information on the use of EZ-ICE and ICEPAC with DBV66.

1.3.10 LSI Support Software

LSI's support software for DBV66 performs all of the low-level software configuration required to use the board. The functions performed by the software are outlined below:

- Initialises the Universe and PCI9060 devices and the PCI bridge on any PMC modules on DBV66 at power-up/system reset. This provides DBV66 with PCI memory and I/O maps.
- Boots the SHARCs from a host workstation.
- Provides simplified easy access to all DBV66 features from a host workstation.
- Provides the SHARCs with functions to access the VMEbus and RS-232 port. Functions are also provided to allow the SHARCs to generate and receive VME interrupts.

Only experienced engineers should attempt the process of configuring and using DBV66 without the support software. In particular, you must be highly competent in the use of PCI-based systems.

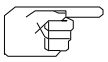


The documentation supplied with DBV66, including this TRM, provides all of the information needed to use DBV66 without the support software. However, the support software will greatly reduce the system development time and we strongly recommend that you use it.

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1.3.11 P2 Breakout Board

An optional P2 breakout board is available from LSI for use with DBV66. This connects to the P2 connector on the reverse side of the VME back-plane and features a number of connectors which allow a variety of signals to be easily routed to/from DBV66. These include SHARC link port signals, SHARC serial port signals, RS-232 serial port signals, debug signals as well as user-defined signals to/from PMC Site 1 on DBV66.



If you wish to purchase the P2 Breakout Board for DBV66, please contact your LSI sales office or your local distributor.

The P2 Breakout Board is detailed in Appendix D.

1.4 PCI and VME Specification Contact Details

DBV66 is designed to the PCI Specification Rev 2.1, the VME64 Draft Specification Rev 1.10 and the VME64 Extensions Draft Specification Rev 0.8. These documents provide detailed information on the respective buses and can be obtained from the following addresses:

- **VME Specifications**

  VITA
  10229 N. Scottsdale Rd.
  Suite B
  Scottsdale
  AZ 85253
  USA

- **PCI Specification**

  PCI Special Interest Group
  P.O. Box 14070
  Portland
  OR 97214
  USA

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2 Board Layout and Installation

This chapter describes how to install DBV66 into a VME rack. The contents of each section are summarised below.

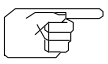
- Section 2.1 describes the DBV66 board layout and summarises the board's hardware selectable functions.
- Section 2.2 lists the DBV66 functionality which is unavailable if the board is installed in a VME rack which has 3 row (rather than 5 row) J1/J2 connectors.
- Section 2.3 describes how to install PMC, DRAM66 and ICEPAC modules onto DBV66. It outlines each of the connectors on DBV66 for off-board communication. It then goes on to describe how to initially configure and install DBV66 into a VME rack.
- Section 2.4 describes how to install the online documentation provided with the board.



All LSI hardware must be protected against static discharge. Appropriate precautions, such as wearing the anti-static wrist strap supplied, must be taken at all times when handling the hardware.

2.1 Board Layout and Hardware Selectable Functions

The layout of the DBV66 board is given in Figure 2.1. This diagram indicates the location of a number of hardware links and front panel LEDs. The function of each hardware link is described in Table 2.1 with the default settings and references to more detailed descriptions. Any alterations to the default settings should be made before installing the board. The function of each of the LEDs on the front panel is outlined in Table 2.2.



Note that a number of links on DBV66 are grouped together on the board. This group of links is referred to as the 'link bank'. The links in the link bank are numbered 1 to 10 on the board, with no prefix. In this manual the same links are prefixed by LB, for example, LB1.

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Table 2.1: DBV66 Hardware Links

Link	Function	Default	Reference
LK1	**SHARC Boot Mode** a - Flash Memory boot b - Link port boot No jumper - Host processor boot Note that all DBV66 SHARCs boot from the same source. LSI's device driver software requires the SHARCs to boot from host processor.	No jumper (host processor)	Section 3.8
LK2	**Flash Memory Write Enable** OUT - Writes to Flash Memory disabled IN - Writes to Flash Memory enabled Note that an additional protection feature for the Flash Memory is implemented in software.	IN (writes enabled)	Section 3.5
LK3	**Enable Live Insertion** a - Live insertion enabled b - Live insertion disabled No jumper - Board will not function. There must always be a jumper in place on LK3. Note that the live insertion feature is only available when DBV66 is used with a 5 row P1/P2 VME rack.	b (live insertion disabled)	Section 2.3.5
LK12	**PMC Site 1 JTAG Bypass** OUT - JTAG not routed to PMC Site 1 IN - JTAG routed to PMC Site 1	OUT (JTAG not routed)	Section 10.3
LK13	**PMC Site 2 JTAG Bypass** OUT - JTAG not routed to PMC Site 2 IN - JTAG routed to PMC Site 2	OUT (JTAG not routed)	
LB1	**VME64 Auto-ID Slave Enable** OUT - Auto-ID slave functionality disabled IN - Auto-ID slave functionality enabled	OUT (Auto-ID disabled)	Universe User Manual
LB2	**Universe A24 Access Enable** OUT - Universe registers cannot be accessed in A24 space at power-up/system reset IN - Universe can be accessed in A24 space at power-up/system reset LSI's DBV66 software requires A24 access to be enabled.	IN (A24 access enabled)	Section 2.3.4
LB3-LB10	**Universe A24 Base Address** These links set the base address of the Universe registers in A24 space. The base address can be rigidly configured or partially set via geographic addressing.	800000h	Section 2.3.4

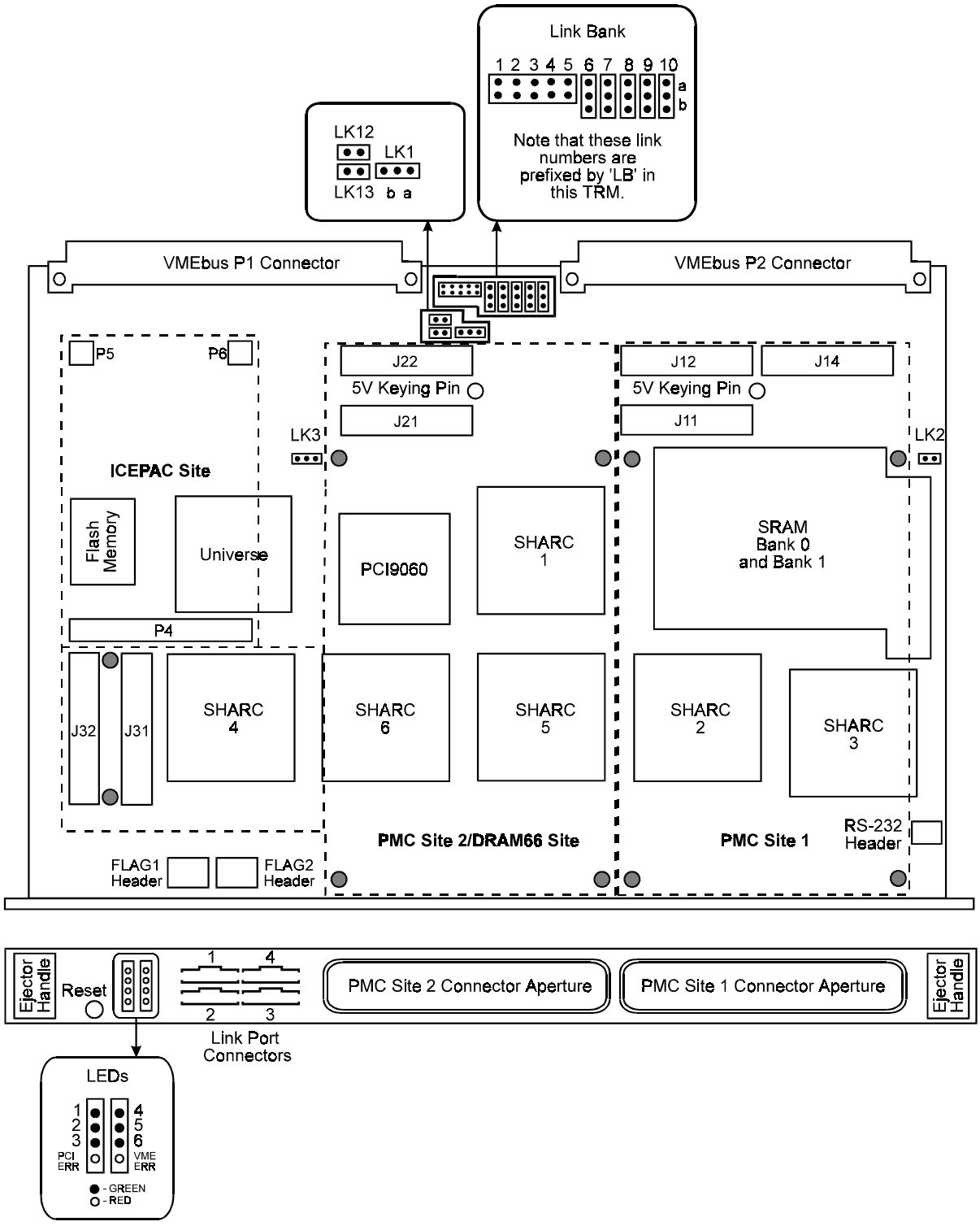
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Table 2.2: Front Panel LED Functions

LED	Function	Reference
1 **2** **3** **4** **5** **6**	**SHARC FLAG0 Status** The status of the FLAG0 signal from each SHARC (when configured as an output) is indicated on the corresponding green LED on the front panel. Note that the function of the FLAG0 signal is user-defined. LED ON - FLAG0 configured as output and high LED OFF - FLAG0 configured as input and/or low	SHARC User's Manual, Section 11.2.5
PCI_ERR	**PCI Bus Error Status** Any PCI PERR# or SERR# error is reflected by the red PCI_ERR LED. LED ON - Either a PERR# or SERR# error has occurred LED OFF - Neither a PERR# nor SERR# has occurred This LED can be turned off by reading the DBV66 Peripheral Status Register.	Section 12.2
VME_ERR	**VMEbus Error Status** Any VME error occurring while DBV66 is acting as VME master is reflected by the red VME_ERR LED. LED ON - VME error has occurred LED OFF - No VME error has occurred This LED can be turned off by reading the DBV66 Peripheral Status Register.	Section 12.3

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Figure 2.1: DBV66 Board Layout and Front Panel



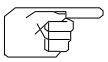
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2.2 VME Rack-Specific DBV66 Functionality

DBV66 has 5 row VME P1/P2 connectors as defined in the VME64 Extensions Specification. The board can be located in VME racks with either 5 or 3 row VME J1/J2 connectors.

However, if DBV66 is located in a VME rack with 3 row connectors then a number of board functions are unavailable. These are listed below with references to descriptions of the relevant functionality. This information is provided to help in selecting whether a 3 or 5 row J1/J2 VME rack is most suitable for your system.

- Live insertion, see Section 2.3.5.
- The LSI proprietary method of slot-dependent addressing, see Section 2.3.4.
- 3.3 V supply to PMC modules, see Section 4.12.
- Link ports on P2, see Chapter 7.
- Time Division Multiplexed serial ports on P2, see Chapter 8.
- Access to the DBV66 RS-232 interface via P2, see Section 3.6.
- Simple I/O implemented using DBV66 I/O Register, see Section 3.3.4.
- VME P2 to SHARC interrupt line, see Section 9.6.



Note that DBV66 does not support the following optional VME64 facilities:

- **Geographic addressing.**
- **Mechanical board identification.**
- **Double edge transfers.**
- **P2 serial and test buses.**

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2.3 Hardware Installation

All LSI hardware must be protected against static discharge. Appropriate precautions, such as wearing the anti-static wrist strap supplied, must be taken at all times when handling the hardware.

2.3.1 PMC Installation

Due to the high density of components on DBV66, the PMC module sites violate the IEEE P1386 Common Mezzanine Card standard in the area of power dissipation. The maximum power dissipation under Site 1 will be 11.5 W and under Site 2 will be 15.0 W. In order to ensure correct DBV66 operation, forced air cooling should be implemented when PMC modules are located on the board.

If a PMC module is supplied with DBV66 then it will already be located on the board. The instructions for installing a PMC module yourself are provided below.

Note that DBV66 only accepts PMC modules which support 5 V signalling. 5 V keying pins protrude from DBV66 near the connectors for each PMC module. These prevent a module being fitted which only supports 3.3 V signalling.

DBV66 can only accept the following combinations of PMC and DRAM66 modules:

- **Two single width PMC modules.**
- **One double width PMC module.**
- **One single width PMC module in Site 1 and a DRAM66 module.**

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Any hardware configuration required by the PMC module will be detailed in the documentation accompanying the module. This should be performed before proceeding with the installation instructions given below.

- ❑ Ensure that DBV66 is removed from the VME rack.
- ❑ Remove the relevant blanking plate from the DBV66 front panel to accommodate the PMC module's bezel.
- ❑ Align the stand-off posts on the PMC module with the relevant holes on DBV66.
- ❑ Carefully slot the PMC module into the relevant connectors. these are labelled J11, J12 and J14 for Site 1 and J21 and J22 for Site 2. Note that the J14 connector carries optional signals which are routed to user-defined pins on the VME P2 connector on DBV66. A particular PMC module may provide not provide this connector.

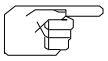
> **! Double-check the installation of the PMC module. Failure to align and push home the connectors correctly may damage both the module and the DBV66 board.**

- ❑ Secure the PMC module using washers and nuts on the four stand-off post threads protruding through DBV66.

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2.3.2 DRAM66 Module Installation

If a DRAM66 module is supplied with DBV66 then it will already be located on the board. The instructions for installing a DRAM66 module yourself are provided below.



Note that DBV66 can only accept the following combinations of PMC and DRAM66 modules:

- **Two single width PMC modules.**
- **One double width PMC module.**
- **One single width PMC module in Site 1 and a DRAM66 module.**

- ❑ Ensure that DBV66 is removed from the VME rack.
- ❑ Align the stand-off posts on the DRAM66 module with the relevant holes on DBV66.
- ❑ Carefully slot the DRAM66 module into the connectors labelled J31 and J32.

Double-check the installation of the DRAM66 module. Failure to align and push home the connectors correctly may damage both the module and the DBV66 board.

- ❑ Secure the DRAM66 module using washers and nuts on the six stand-off post threads protruding through DBV66.

2.3.3 ICEPAC Installation

Three connectors are provided on DBV66 for an Analog Devices ICEPAC module. There are two 4 pin connectors labelled P5 and P6 and a 36 pin connector labelled P4. In order to install the ICEPAC module, it is fitted into these connectors on DBV66.

Note that the P4 connector can also be used to accept the probe of an EZ-ICE system as described in Section 9.2.

The location of the above connectors is illustrated in Figure 2.1.

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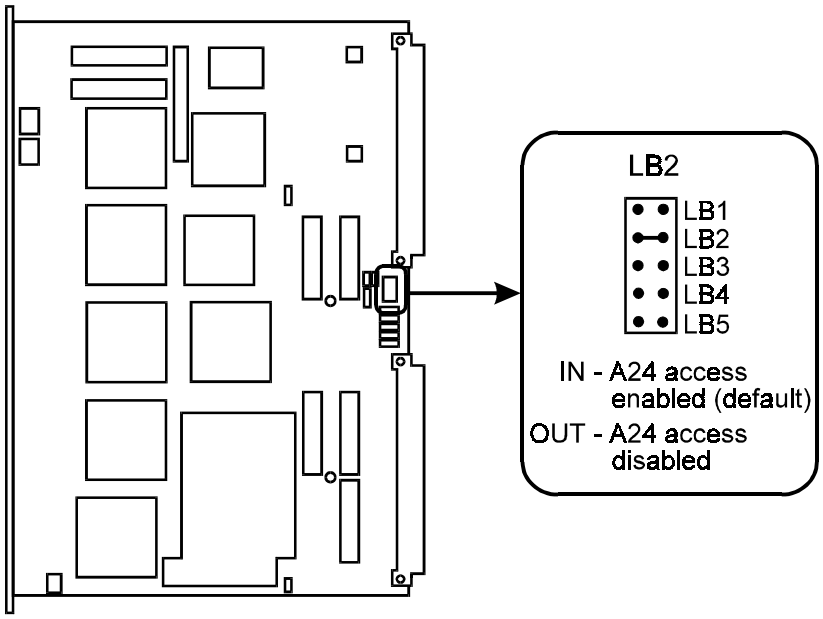
2.3.4 Initial VME Base Address Configuration

DBV66 can be configured to allow access to the registers of the Universe bridge at power-up/system reset in VME A24 space. The purpose of this is to allow DBV66 to be configured from the VMEbus. If this mapping is disabled then DBV66 must be initialised by SHARC bootcode.

LSI's support software for DBV66 configures the board from the VMEbus. Therefore, A24 access must be enabled when using the software.

Figure 2.2 below illustrates how to configure hardware link LB2 to enable/disable A24 access to the Universe registers.

Figure 2.2: Enabling A24 Access to Universe - LB2



If A24 access to the Universe registers is enabled then the base address of the registers in A24 space must be configured using hardware links LB3 to LB10. These links can be set to fully configure the base address, such that the address does not vary from slot to slot. Alternatively, they can be set such that part of the address is configured using the VME64 geographic addressing pins on the VME backplane.

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Note that DBV66 employs the geographic addressing pins in a different way to that described in the VME64 Specification. Instead of using the pins as part of the CR/CSR space configuration process, they are used for an LSI proprietary method of 'slot-dependent addressing' as described below.

If the geographic addressing pins are implemented then the address of the board will vary from slot to slot. Note that the board occupies 64K bytes of A24 space (although only the first 4K bytes are actually used).

Slot-dependent addressing is only available if DBV66 is to be installed into a VME rack with 5-row J1/J2 backplane connectors.

The following notes describe how hardware links LB3 to LB10 are implemented:

- Considering the A24 base address in binary format, bits A0 to A15 are all automatically set to ‘0’ and bits A16 to A23 are set using hardware links LB3 to LB10.
- Links LB3 to LB5 rigidly set bits A16 to A18 respectively of the A24 address. Inserting a jumper across any of the links sets the corresponding bit to ‘1’ and removing a link sets the bit to ‘0’.
- Links LB6 to LB10 can be configured to set bits A19-A23 respectively of the A24 address. Alternatively, they can be set to force the bits to be set via the geographic addressing pins. Inserting a jumper in position ‘a’ sets the corresponding bit to ‘1’ and removing the jumper sets the bit to ‘0’. If the jumper is inserted in position ‘b’ then the corresponding bit is set via the geographic addressing pin of the VME backplane. Table 2.3 lists the slot-dependent addressing settings imposed on A19-A23 for each VME rack slot.

Figure 2.3 below illustrates the general configuration of links LB3 to LB10. Figure 2.4 illustrates the default configuration of LB3 to LB10 which provides a base address of 800000h.

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Figure 2.3: A24 Base Address Configuration - LB3 to LB10

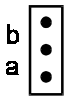
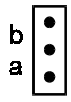
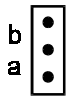
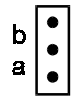
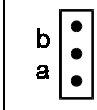
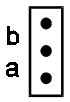
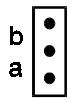
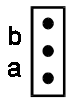
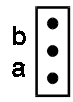
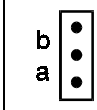
Link Number	LB10	LB9	LB8	LB7	LB6	LB5	LB4	LB3
Link Diagram								
Address Line	A23	A22	A21	A20	A19	A18	A17	A16
Link Configuration	a - Address line set to ‘1’ b - Address line set via geographic addressing pins, see Table 2.3. No jumper - Address line set to ‘0’					IN - Address line set to ‘1’ OUT - Address line set to ‘0’		

Figure 2.4: A24 Base Address Configuration - Default

Link Number	LB10	LB9	LB8	LB7	LB6	LB5	LB4	LB3
Link Diagram								
Address Line	A23	A22	A21	A20	A19	A18	A17	A16
Binary Settings	1	0	0	0	0	0	0	0
Hexadecimal Address	800000h							

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Table 2.3: Slot-Dependent Address Configuration

Slot Number	A23 (LB10)	A22 (LB9)	A21 (LB8)	A20 (LB7)	A19 (LB6)
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1
8	0	1	0	0	0
9	0	1	0	0	1
10	0	1	0	1	0
11	0	1	0	1	1
12	0	1	1	0	0
13	0	1	1	0	1
14	0	1	1	1	0
15	0	1	1	1	1
16	1	0	0	0	0
17	1	0	0	0	1
18	1	0	0	1	0
19	1	0	0	1	1
20	1	0	1	0	0
21	1	0	1	0	1

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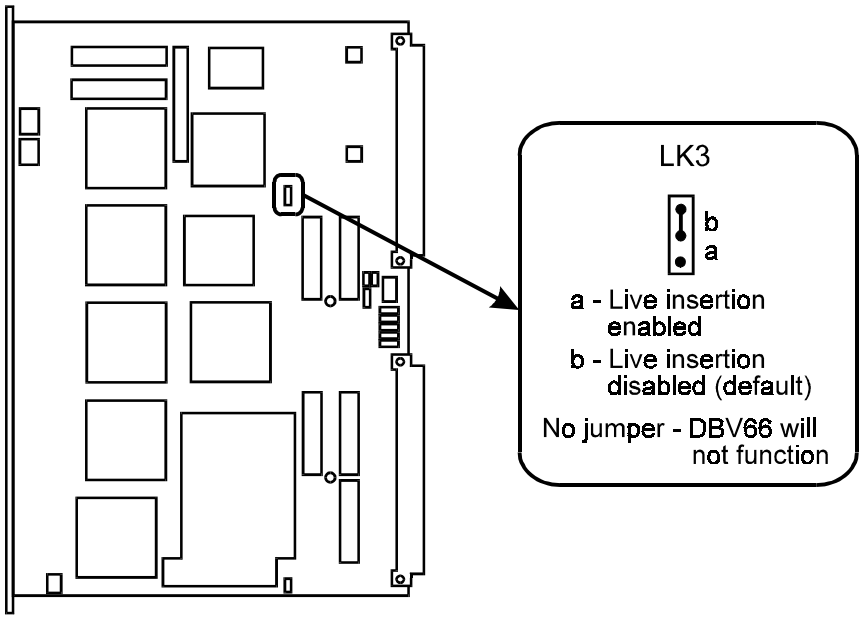
2.3.5 Live Insertion Configuration

DBV66 can be directly plugged into a VME rack with 5 row J1/J2 connectors without switching off the rack. This is referred to as 'live insertion'. LK3 on DBV66 must be correctly configured to enable/disable this functionality as required, see Figure 2.5 below.

The live insertion feature is not available with VME racks with 3 row J1/J2 backplane connectors. If the feature is enabled and DBV66 is located in such a rack then the board will fail to function.

If LSI's SunOS or Solaris support software is used with DBV66 then the board should not be live inserted into a VME rack in which it was not present at system boot. This is due to the fact that the SunOS and Solaris operating systems only detect boards at system boot.

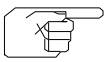
Figure 2.5: Live Insertion Configuration - LK3



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2.3.6 Connectors Overview

DBV66 provides a number of connectors for off-board communication. This section outlines the connectors provided and their functions for reference during the installation process. The location of each connector is illustrated in Figure 2.1.



References to more detailed information are provided below and these should be consulted before making any connections to DBV66.

- **Link Port Connectors**

  Four link port connectors are provided on the DBV66 front panel. These allow the DBV66 SHARCs to directly communicate with peripheral SHARCs. In addition to this, ports are available over the VME P2 connector. See Chapter 7 for more details.

- **FLAG Headers**

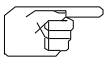
  Two 10-pin on-board headers provide access to the FLAG1 and FLAG2 signals of each SHARC on DBV66. The use of these signals is application-specific. Each signal can be employed as either an input or output under software control. Section 12.1 provides more details on the FLAG1 and FLAG2 connectors.

- **RS-232 Connector**

  The DBV66 RS-232 serial port can be routed off-board via the 6-pin on-board header or via the VME P2 connector. Refer to Section 3.6 for more details.

- **ICEPAC/EZ-ICE Connector**

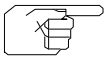
  A connector is provided to allow an Analog Devices' ICEPAC or EZ-ICE system to be employed with DBV66, see Section 10.2.



In addition to the above connectors, DBV66 routes a number of signals off-board via the user-defined pins of the 5 row VME P2 connector. These signals are outlined in Section 2.2. LSI supply a P2 breakout board which can be used to easily access the user-defined pins, allowing high integrity connections to be made. This is described in Appendix D.

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2.3.7 DBV66 Installation



If you wish to alter the default setting of any of the hardware links on DBV66 then you should do so before installing the board. Table 2.1 provides an overview of the links and provides references to more detailed information in this manual.

DBV66 is a double Eurocard (6U) board which occupies a single slot in the VMEbus backplane. Your host VMEbus system must comply with the VMEbus Specification Rev C.1.

The DBV66 board typically draws 4.0A (with no DRAM66 module and 4.6A (with a DRAM66 module) from the +5 V VME supply rail, and 0A from the ±12 V rail. The additional current drawn from the +5 V and ±12 V rails by any modules sited on the board must also be taken into account. This is detailed in the appropriate module User Manuals.

Before installing DBV66 you must ensure that the Interrupt Acknowledge and Bus Grant daisychains on the VMEbus backplane are complete.

To install DBV66 in your system:

- ❑ Unless your VME rack has 5-row J1/J2 backplane connectors you must ensure that power to the VMEbus system is turned off at all appropriate mains power outlets.
- ❑ Make any necessary connections to the on-board headers.
- ❑ Make any necessary front panel connections.
- ❑ Gently, but firmly, press-fit the DBV66's P1 and P2 male connectors into the VMEbus connectors on the backplane.
- ❑ Once the board is firmly in place secure the two retaining screws.
- ❑ If you previously disconnected power from the system then you can now re-apply power.

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2.4 Online Documentation

A number of documents, including this TRM, are provided with the DBV66 board in Adobe's Portable Document Format (PDF). These PDF files are the manuals/data sheets provided by the manufacturers of the following devices on DBV66:

- Analog Devices SHARC DSP
- PLX PCI9060 Bridge Device
- Tundra Universe Bridge Device
- Philips UART (RS-232)

This online documentation provides the detailed information required to access the devices directly. With the exception of the SHARC User's Manual, it is not necessary to consult this information if LSI's software is used with DBV66 as this software configures the devices.

The files are provided on a CD-ROM and can be read using the Adobe Acrobat Reader supplied. This can be run under Windows 3.1x, 95 and NT, SunOS and Solaris. Section 2.4.1 below provides installation instructions for the data sheets and the Adobe Acrobat Reader software required to view them. Section 2.4.2 provides useful notes on using the Acrobat Reader to print PDF files.

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2.4.1 Installation Instructions

To install the Acrobat Reader software, follow the instructions below.

Windows 3.1x

- ❑ From within Windows File Manager, make your CD-ROM drive the current drive.
- ❑ Move to the **acro_v3\acrowin\16bit** directory.
- ❑ Select **Run** from the **File** menu and enter:

  ```
  ar16e30.exe
  ```

  This will invoke Adobe's installation utility for the Acrobat Reader.

- ❑ Follow all on-screen instructions.

The online documents (**.pdf** files) are supplied in subdirectories under the **lsi_docs\hardware** directory. These files can either be copied to your hard drive or can be viewed directly from the CD-ROM.

Note that an online QuickStart Guide, describing the basic functionality of the Adobe Acrobat Reader, is also provided in the file **olquick.pdf** in the **lsi_docs** directory.

Windows 95 or NT

- ❑ From within Windows File Manager, make your CD-ROM drive the current drive.
- ❑ Move to the **acro_v3\acrowin\32bit** directory.
- ❑ Select **Open** from the **File** menu and enter:

  ```
  ar32e30.exe
  ```

  This will invoke Adobe's installation utility for the Acrobat Reader.

- ❑ Follow all on-screen instructions.

The online documents (**.pdf** files) are supplied in subdirectories under the **lsi_docs\hardware** directory. These files can either be copied to your hard drive or can be viewed directly from the CD-ROM.

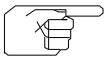
Note that an online QuickStart Guide, describing the basic functionality of the Adobe Acrobat Reader, is also provided in the file **olquick.pdf** in the **lsi_docs** directory.

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SunOS/Solaris

Full instructions on installing the Acrobat Reader are supplied in the file **instguid.txt** in the **acro_v3/acrounix/acroread** directory on the CD-ROM.

The online documents (**.pdf** files) are supplied in subdirectories under the **lsi_docs/hardware** directory. These files can either be copied to your hard drive or can be viewed direct from the CD-ROM.



If you have purchased a software support package for use with DBV66, it is recommended that you copy the hardware documentation to the lsi_docs directory of your software installation.

Note that an online QuickStart Guide, describing the basic functionality of the Adobe Acrobat Reader, is also provided in the file **olquick.pdf** in the **lsi_docs** directory.

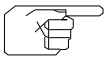
2.4.2 Printing PDF Documents

As well as providing an online viewer, the Acrobat Reader also allows you to print PDF documents. The following notes should be considered when doing this:

- If possible, you should use a PostScript printer when printing PDF documents. Adobe's PDF format is very close to PostScript and therefore documents can be printed very quickly. It can take a long time to print a large PDF document on a non-PostScript printer.
- If you use an HP LaserJet 4 printer, the Acrobat Reader has the following requirement. In order to correctly print a PDF document, 'Raster' must be selected as the 'Graphics Mode' for your printer. This does not affect the quality of the printout but enables the document to be printed correctly. From Acrobat Reader, select the **Print Setup...** option from the **File** menu, and select Raster as your Graphics Mode.

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3 Interconnect Bus



This chapter describes the Interconnect bus as accessed by the SHARCs. The Interconnect bus can also be accessed via the PCI bus as described in Chapter 4.

3.1 Introduction

The SHARC architecture allows its external port to be directly connected to the external port of up to five other SHARCs. This allows the interconnected SHARCs to access the internal SRAM banks and I/O Processor (IOP) registers of the other SHARCs.

The memory map for each SHARC provides regions for:

- Accessing its own internal resources.
- Accessing the internal resources of any other interconnected SHARC.
- Performing broadcast writes to itself and all other interconnected SHARCs.
- Accessing any additional resources connected to the bus formed by interconnecting the memory interfaces.

On DBV66, the external memory interfaces of the SHARCs are all interconnected. The resulting shared parallel bus is referred to as the 'Interconnect bus'. Since each SHARC can access the same resources on the Interconnect bus, the memory map is the same for all SHARCs on DBV66 and is given in Figure 3.1.

Note that a section of the Interconnect bus is isolated from the SHARCs via transparent buffers as illustrated in Figure 1.1. If a DRAM66 module is located on DBV66 then the DRAM is accessed via this isolated section. The SHARCs access the DRAM as though the buffers were not present. However, accesses to the DRAM from the PCI bus do not disrupt transfers across the rest of the bus. This feature can be exploited to increase system efficiency.

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Figure 3.1: DBV66 SHARC Memory Map

SHARC Address	Resource	Reference
0000 0000h	I/O Processor Registers	Appendix A of this TRM and Chapter 5 of the SHARC User's Manual
0002 0000h	Internal SRAM[1] Normal Word Addressing	
0004 0000h	Internal SRAM[1] Short Word Addressing	
0008 0000h	SHARC 1 Internal Memory Space	
0010 0000h	SHARC 2 Internal Memory Space	
0018 0000h	SHARC 3 Internal Memory Space	
0020 0000h	SHARC 4 Internal Memory Space	
0028 0000h	SHARC 5 Internal Memory Space	
0030 0000h	SHARC 6 Internal Memory Space	
0038 0000h	Broadcast Write Space	
0040 0000h	External SRAM[2] Bank 0 (48 bit wide)	Section 3.4
0440 0000h	External SRAM[2] Bank 1 (32 bit wide)	Section 3.4
0840 0000h	Reserved	-
0900 0000h	DRAM66 Module[2]	Section 3.7.1
0A00 0000h	Reserved	-
0C40 0000h	Flash Memory[2] (512K x 8 on D23-D16)	Section 3.5
0E00 0000h	Peripheral Control Register	Section 3.3.1
0E00 0001h	Peripheral Status Register	Section 3.3.2
0E00 0002h	Interrupt Status Register	Section 3.3.3
0E00 0003h	I/O Register	Section 3.3.4
0E00 0004h	Reserved	-
0E00 0008h	UART (RS-232) Registers	Section 3.6
0E00 0010h	Reserved	-
1800 0000h	PCI9060 Registers	Section 3.7.2
2000 0000h	PCI Memory Master Access Space	Section 4.7
3000 0000h	PCI I/O Master Access Space	
4000 0000h *FFFF FFFFh*	Reserved	-

Note:

[1]The ADSP-21060 provides two 2M bit blocks of on-chip SRAM. The ADSP-21062 provides two 1M bit blocks of on-chip SRAM.

[2]The External SRAM, DRAM and Flash Memory are reflected to fill the address space allocated to each resource.

The SHARC memory map is 48 bits wide from *0000 0000h* to *00FF FFFFh. The region* from *0100 0000h* to *FFFF FFFFh* is 32 bits wide.

The SHARC IOP *WAIT* and *SYSCON* registers must be correctly initialised before any accesses are made to external memory resources, see Section 3.9 and Section 3.10.

If the DBV66 board has less than six SHARC processors then the spaces which correspond to the SHARCs which are not fitted are unused. Note that on DBV66 variants with two SHARCs, the processors are referred to as SHARCs 1 and 2. On variants with four SHARCs, they are referred to as SHARCs 1, 2, 3 and 4.

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3.2 SHARC Internal Resources

Each SHARC has access to its own internal resources and the internal resources of the other SHARCs via the Interconnect bus. These resources consist of the I/O Processor registers and the two internal SRAM blocks. These resources are outlined in Section 3.2.1 and Section 3.2.2 respectively.

Note that each SHARC can access SHARC internal resources via three regions in the SHARC memory map:

- The first region is from *0000 0000h* to *0007 FFFFh* and is referred to as the ‘internal memory space’. This space provides each SHARC with exclusive access to its own internal resources.
- The second region is from *0008 0000h* to *0037 FFFFh*. This region is subdivided into six spaces, each space being dedicated to one SHARC. All six spaces can be accessed by any SHARC on the Interconnect bus.
- The third region is from *0038 0000h* to *003F FFFFh*. Writes to this region are broadcast to all SHARCs on the Interconnect bus.

The second and third regions are collectively referred to as the 'multiprocessor memory space'.

3.2.1 I/O Processor Registers

The I/O Processor (IOP) Registers of each SHARC consist of 256 memory-mapped registers providing SHARC system configuration and control/status for the on-chip IOP. The IOP incorporates a 10 channel DMA controller, six parallel link ports and two serial ports. Appendix E of the SHARC User’s Manual describes each of the IOP registers in detail.

Section 3.9 and 3.10 of this TRM provide DBV66-specific information on configuring the SHARC IOP *WAIT* and *SYSCON Registers* respectively.

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3.2.2 Internal SRAM

The two variants of the SHARC each provide two blocks of internal SRAM. The ADSP-21060 provides two 2M bit blocks and the ADSP-21062 provides two 1M bit blocks.

Both instructions (48 bit) and data (40, 32 and 16 bit) can be addressed in the internal SRAM blocks. The Normal Word Addressing space in the SHARC memory map is provided for making 32 and 48 bit accesses to the internal SRAM. The Short Word Addressing space is used for making 16 bit accesses. Note that 48 bit accesses are required for 40 bit data.

For further details on accessing the SHARC internal SRAM, refer to Appendix A of this TRM and Section 5.3 of the SHARC User's Manual.

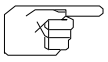
3.3 DBV66 Control/Status Registers

The SHARCs have access to four DBV66 registers on the Interconnect bus. These registers are outlined in the following subsections. References are provided to later sections which further describe their use.

3.3.1 Peripheral Control Register

The 8 bit read/write Peripheral Control Register is located at *0E00 0000h* in the SHARC memory map. Its main function is to provide control over the DBV66 Broadcast Link Port (BLP). The register is set to 0000 0000h on power-up/reset and the individual bit functions are described in Table 3.1 below.

Section 7.3 provides further information on the BLP and Section 4.12.2 describes how to use bits 7 to 5 to test for the presence of a PMC module in software.



Before any access can be made to a PMC module, bits 7 to 5 of the Peripheral Control Register must be set to '110'.

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Table 3.1: Peripheral Control Register

D31-D8	D7-D5	D4-D2	D1	D0
Not Used	**PMC_TEST**	**BLP_TRANS**	**BLP_DIR**	**BLP_OB**

Bit	Name	Function
0	BLP_OB	Broadcast Link Port off-board routing. '0' - BLP routed on-board only. '1' - BLP routed on-board and off-board via VME P2 connector.
1	BLP_DIR	Broadcast Link Port off-board direction. '0' - BLP input from another board. '1' - BLP output to another board. If the BLP is not routed off-board then the setting of this bit has no effect.
4-2	BLP_TRANS	Must be set to indicate which SHARC will be transmitting on the Broadcast Link Port. Only one SHARC can transmit on the BLP at any one time. The individual bit settings are given below. **Bit 4 Bit 3 Bit 2** 0 0 0 BLP input from another board. 0 0 1 SHARC 1 transmitting. 0 1 0 SHARC 2 transmitting. 0 1 1 SHARC 3 transmitting. 1 0 0 SHARC 4 transmitting. 1 0 1 SHARC 5 transmitting. 1 1 0 SHARC 6 transmitting. 1 1 1 Reserved. If less than six SHARCs are fitted to the board then the relevant bit settings are reserved.
7-5	PMC_TEST	Used to initiate a test for PMC modules in Sites 1 and 2. If these bits are set to '110' then bits 0 and 1 in the Peripheral Status Register (PMC1 and PMC2) can be read to determine if a PMC is present in Sites 1 and 2 respectively. This bit setting also enables access to the PMC modules from the PCI bus. If these bits are set to '111' then a PMC test is initiated as described above but access to the PMC modules is disabled. If these bits are set to '000' (default) then the PMC modules are disabled. They will not be accessible from the PCI bus unless the value '110' is later written to the same bits. All other bit settings are reserved.

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3.3.2 Peripheral Status Register

The 8 bit read only Peripheral Status Register is located at *0E00 0001h* in the SHARC memory map and provides DBV66 status information. The individual bit functions are described in Table 3.2 below. Note that reading this register clears bits 7-5 to '0' and switches off the red PCI_ERR and VME_ERR LEDs on the front panel.

Table 3.2: Peripheral Status Register

D31-D8	D7	D6	D5	D4-D3	D2	D1	D0
Not Used	**PCI_PERR**	**PCI_SERR**	**VME_ERR**	**S_COUNT**	**WS512**	**PMC2**	**PMC1**

Bit	Name	Function
0 1	PMC1 PMC2	Used to determine if a PMC is present in Sites 1 and 2 respectively. Before reading these bits, bits 7-5 (PMC_TEST) of the Peripheral Control Register must have been set to '110' or '111'. PMC1 will read '1' if a PMC is present in Site 1 or '0' otherwise. PMC2 will read '1' if a PMC is present in Site 2 or '0' otherwise. Note that if a double width PMC or a DRAM66 module is fitted then the PMC2 bit will indicate that Site 2 is empty.
2	WS512	DBV66 variants with 512K x 48 and 512K x 32 SRAM banks will be provided with the fastest memory available at production, either 0ws or 1ws. This bit can be read to determine the number of wait states required. This can then be used to determine the correct setting for the SHARC IOP *WAIT Register* as described in Section 3.9. '0' - 512K SRAM banks require 0ws. '1' - 512K SRAM banks require 1ws. Note that 128K SRAM banks always operate at 0ws.
4-3	S_COUNT	Used to indicate the number of SHARCs on the Interconnect bus. The individual bit settings are given below. **Bit 4 Bit 3** 0 0 Six SHARCs on Interconnect bus. 0 1 Four SHARCs on Interconnect bus, SHARCs 1 to 4. 1 0 Two SHARCs on Interconnect bus, SHARCs 1 and 2. 1 1 Reserved.
5	VME_ERR	Used to indicate if a VME error occurs while DBV66 is acting as VME master. '0' - No VME error occurred. '1' - VME error occurred. Note that if VME_ERR reads '1' then the red VME_ERR LED on the front panel will be lit.
6	PCI_SERR	Used to indicate if a PCI system error has occurred. '0' - No PCI system error occurred. '1' - PCI system error occurred. Note that if either PCI_SERR or PCI_PERR reads '1' then the red PCI_ERR LED on the front panel will be lit.
7	PCI_PERR	Used to indicate if a PCI parity error has occurred. '0' - No PCI parity error occurred. '1' - PCI parity error occurred. Note that if either PCI_SERR or PCI_PERR reads '1' then the red PCI_ERR LED on the front panel will be lit.

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3.3.3 Interrupt Status Register

The 8 bit read only Interrupt Status Register is located at *0E00 0002h* in the SHARC memory map and provides status information for a number of DBV66 interrupts. The individual bit functions are described in Table 3.3 below.

Interrupts can be generated on the SHARC /IRQ0 interrupt line from the PCI INTA# to INTD# interrupt lines, the RS-232 port and the PCI9060 device. Upon receipt of an /IRQ0 interrupt this register can be read to determine which of these is the interrupt source. Chapter 9 provides more details on DBV66 interrupts.

Table 3.3: Interrupt Status Register

D31-D8	D7	D6	D5	D4	D3	D2	D1	D0
Not Used	**DRAM66**	**LINTo#**	**RS232**	**LSERR#**	**INTD#**	**INTC#**	**INTB#**	**INTA#**

Bit	Name	Function
0	INTA#	Indicates the status of the PCI INTA# interrupt line. ‘1’ - INTA# active. ‘0’ - INTA# not active.
1	INTB#	Indicates the status of the PCI INTB# interrupt line. ‘1’ - INTB# active. ‘0’ - INTB# not active.
2	INTC#	Indicates the status of the PCI INTC# interrupt line. ‘1’ - INTC# active. ‘0’ - INTC# not active.
3	INTD#	Indicates the status of the PCI INTD# interrupt line. ‘1’ - INTD# active. ‘0’ - INTD# not active.
4	LSERR#	Indicates the status of the PCI9060 LSERR# interrupt. ‘1’ - LSERR# interrupt active. ‘0’ - LSERR# interrupt not active. Note that the PCI9060 generates an LSERR# interrupt on a master/target abort or if a PCI parity error occurs. Refer to the PCI9060 data sheet for further details.
5	RS232	Indicates the status of the RS-232 interrupt from the UART device. ‘1’ - RS-232 interrupt active. ‘0’ - RS-232 interrupt not active.
6	LINTo#	Indicates the status of the PCI9060 LINTo# interrupt. ‘1’ - PCI9060 LINTo# interrupt active. ‘0’ - PCI9060 LINTo# interrupt not active. Note that a number of internal PCI9060 sources generate LINTo# interrupts, including the internal PCI to Local Doorbell Register. Refer to the PCI9060 data sheet for further details.
7	DRAM66	Used to indicate the presence of a DRAM66 module. '0' - No DRAM66 module fitted to DBV66. '1' - DRAM66 module fitted to DBV66.

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3.3.4 I/O Register

The 8 bit read/write I/O Register is located at *0E00 0003h* in the SHARC memory map and provides an easy way of passing status information to/from DBV66. The bits provide access to user-defined pins on the VME P2 connector as described in Table 3.4 below.

Table 3.4: I/O Register

D31-D8	D7	D6	D5-D4	D3	D2	D1	D0
Not Used	**IN1**	**IN0**	**Reserved**	**OUT3**	**OUT2**	**OUT1**	**OUT0**

Bit	Name	Function
0	OUT0	Allows Pin d27 on the VME P2 connector to be implemented as an output flag for user-defined purposes. This bit is write only, reading the bit will return either '0' or '1'.
1	OUT1	Allows Pin d28 on the VME P2 connector to be implemented as an output flag for user-defined purposes. This bit is write only, reading the bit will return either '0' or '1'.
2	OUT2	Allows Pin d29 on the VME P2 connector to be implemented as an output flag for user-defined purposes. This bit is write only, reading the bit will return either '0' or '1'.
3	OUT3	Allows Pin d30 on the VME P2 connector to be implemented as an output flag for user-defined purposes. This bit is write only, reading the bit will return either '0' or '1'.
5-4	-	Reserved. Writing these bits has no effect. A read will return an indeterminate value.
6	IN0	Allows Pin d24 on the VME P2 connector to be implemented as an input flag for user-defined purposes. This bit is read only, writing the bit will have no effect.
7	IN1	Allows Pin d25 on the VME P2 connector to be implemented as an input flag for user-defined purposes. This bit is read only, writing the bit will have no effect.

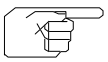
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3.4 External SRAM

In addition to the SHARC internal SRAM blocks, DBV66 provides two external banks of SRAM, Banks 0 and 1. DBV66 variants are available with these banks factory-fitted with the following memory options:

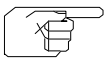
- DBV66-S11 has 128K x 48 Bank 0 plus 128K x 32 Bank 1.
- DBV66-S22 has 512K x 48 Bank 0 plus 512K x 32 Bank 1.

Bank 0 is reflected to fill the space from *0040 0000h* to *0440 0000h* and Bank 1 is reflected to fill the space from *0044 0000h* to *0840 0000h* in the SHARC memory map.



The SHARC IOP *WAIT Register* must be correctly initialised before making any accesses to the SRAM from the SHARCs, see Section 3.9.

The SHARCs can access 48 bit instructions and 32 or 40 bit data in Bank 0. However, Bank 0 is employed most efficiently when used to store 48 bit instructions. This is due to the fact that a 32 or 40 bit data word occupies an entire 48 bit memory location.



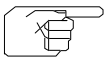
We recommend that instructions are not executed directly from the external SRAM Bank 0 but are first loaded into internal SRAM. This will reduce the load on the Interconnect bus, increasing system efficiency.

The SHARCs incorporate on-chip arbitration for accesses across the Interconnect bus, including accesses to the external SRAM. Refer to Section 3.11 for more information. The SRAM banks are also accessible from the PCI bus as described in Section 4.9.

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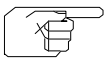
3.5 Flash Memory

DBV66 provides a 512K x 8 bank of Flash Memory on the Interconnect bus for embedded code storage. The Flash Memory is reflected to fill the space from *0C40 0000h* to *0E00 0000h* in the SHARC memory map. The device is located on data lines D23 to D16.



The SHARCs can be configured to boot from the Flash Memory via hardware link LK1, see Section 3.8.

The SHARCs incorporate on-chip arbitration for accesses across the Interconnect bus, including accesses to the Flash Memory. Refer to Section 3.11 for more information.



The SHARC IOP *WAIT Register* must be correctly initialised before making any accesses to the Flash Memory from the SHARCs (except during Flash Memory booting), see Section 3.9.

The support software supplied with LSI's DBV66 software development packages contains a Flash Memory programming tool. If you do not have this software or wish to perform a Flash Memory programming function not covered by the tools, then the method for doing this is detailed in this section.

To protect the Flash Memory from accidental programming, there are two protection features that must be overcome before programming the Flash Memory is possible.

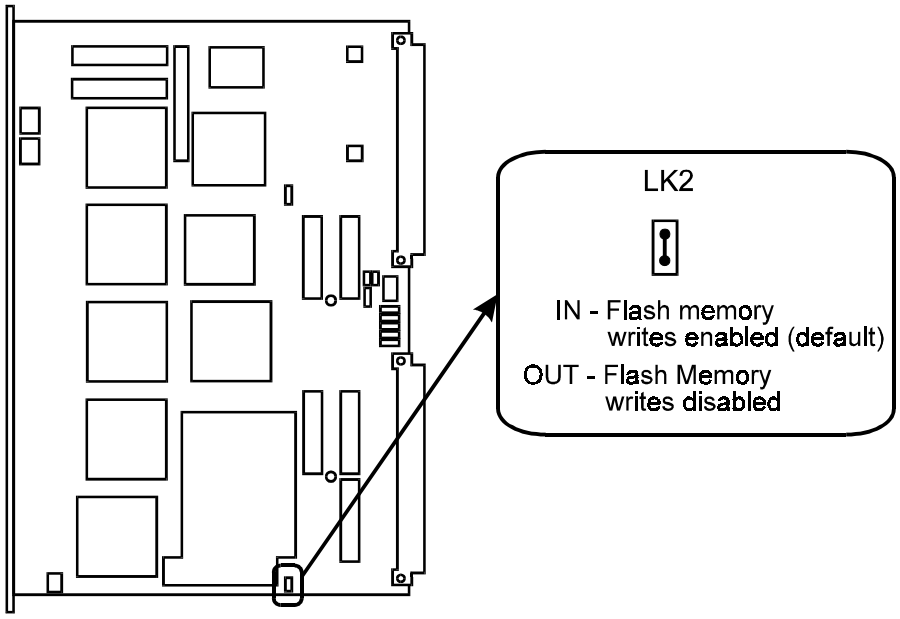
The first of these is a hardware link which must be configured to enable write accesses to the Flash Memory. The location and setting of this link, LK2, is illustrated in Figure 3.2.

Once LK2 has been configured to enable writes to the Flash Memory, a second protection feature must be overcome. This feature consists of software data protection algorithms which are present on the Flash Memory. There are three such algorithms, one for programming the device and two for erasing it. The relevant algorithm must be executed if you wish to write to the Flash Memory.

The data protection algorithms and the methods for erasing and programming the Flash Memory are explained in Section 3.5.1 below.

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Figure 3.2: Flash Memory Write Enable Link - LK2



3.5.1 Software Data Protection Algorithms

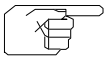
There are three types of programming which can be performed on the Flash Memory, these are:

- Byte Programming, this involves writing program data to the Flash Memory one byte at a time.
- Full Erase, this sets all locations in the Flash Memory to the value FFh.
- Sector Erase, this sets all locations in 64K byte pages or ‘sectors’ of the Flash Memory to the value FFh.

Each of these types of programming has an associated software data protection algorithm. These algorithms each consist of a series of program commands to specific addresses with specific data, see Figure 3.3.

In order to perform any Flash Memory programming, each of the commands in the relevant algorithm must be executed. In the case of Byte Programming, the algorithm must be repeated for each byte of program data to be written to the Flash Memory. Executing the Full Erase or Sector Erase algorithms will automatically clear the Flash Memory, no further programming is required. At the end of each algorithm, the Flash Memory is automatically returned to its protected state.

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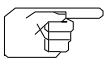


It is not possible to use Byte Programming to alter the setting of any bit in the Flash Memory from '0' to '1'. Therefore, the 64K byte sector containing the location to be programmed must first be erased by executing either a Sector Erase or Full Erase algorithm.

Figure 3.4 gives a general flow chart which shows the steps necessary to write program data to the Flash Memory. Figure 3.5 provides general flow charts which show the steps necessary to erase all, or a sector of, the Flash Memory.

Both Figure 3.4 and Figure 3.5 refer to the data polling flow chart illustrated in Figure 3.6. The data polling method implemented on the Flash Memory provides a method of determining when, or if, an attempt to program it has been successful. The steps illustrated by the flow chart in Figure 3.6 are described below:

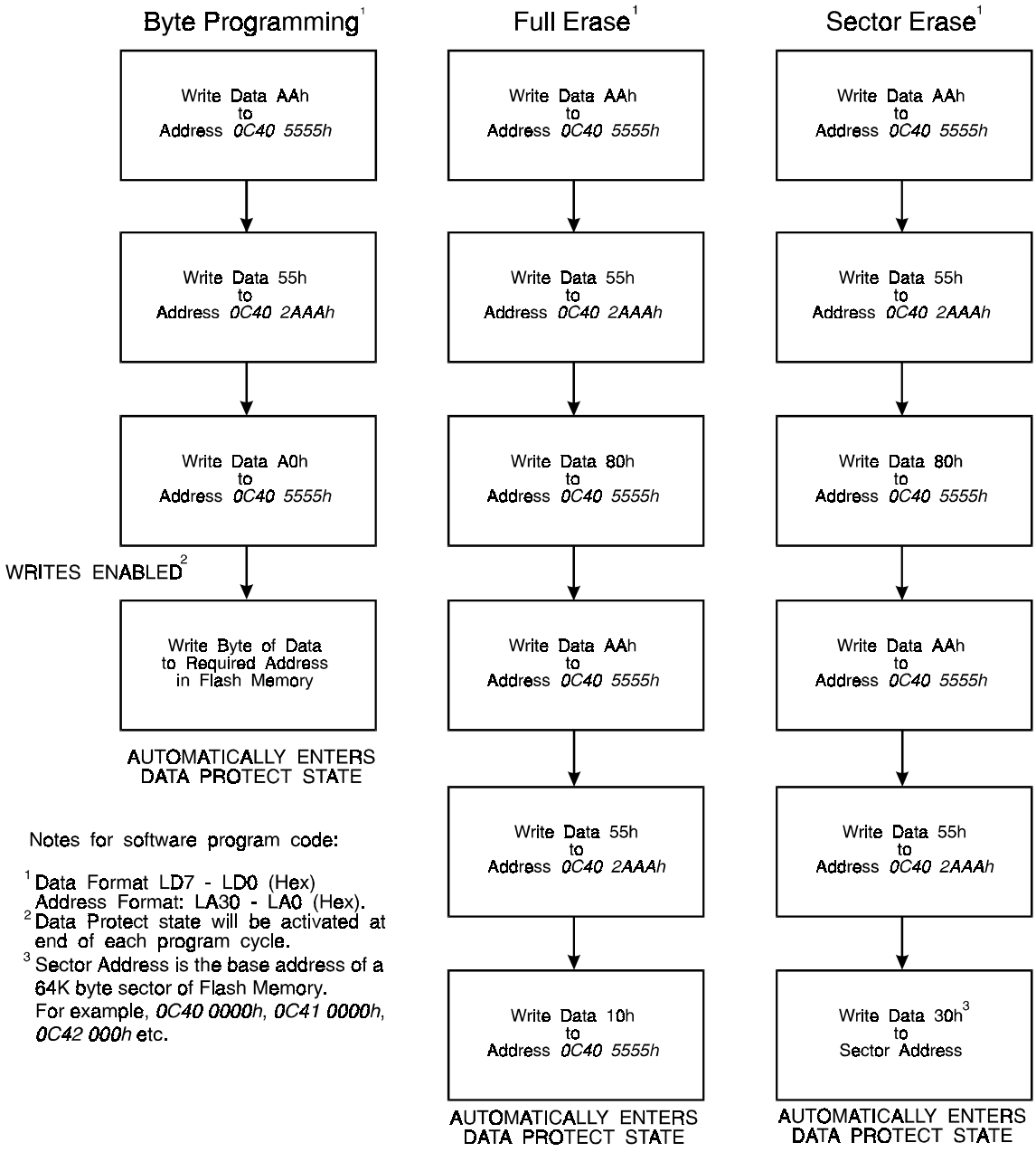
- There is a delay between the time when a value is written to the device and when it is actually programmed into the storage matrix. In order to determine whether or not the value has actually been programmed, the last byte written to the Flash Memory is read back. When erasing the Flash Memory, a location from any sector which is being erased can be read.
- Bit 7 of the returned value will be read as the complement of the value written to Flash Memory until the value is actually programmed into the matrix. It will then read as the correct value. Therefore, if bit 7 reads the same as bit 7 of the value written to the device, the program cycle has been successful.
- Bit 5 of the returned value will read as '1' if a time-out condition has occurred. This condition would occur if an attempt is made to program a sector of the device which is bad. This bit is implemented to avoid the infinite loop which might occur if it was impossible to program a sector of the device, such that bit 7 never returned the correct value.
- If bit 5 reads as '1' during data polling then the byte is read again and bit 7 is checked to see if it now reads as the correct value. This read, after a time-out condition has been indicated, is performed as there is a possibility of a successful write just after the time-out was indicated.



Due to the properties of the Flash Memory device, data integrity can only be assured up to 100 000 programming cycles.

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Figure 3.3: Software Data Protection Algorithms



Notes for software program code:

[1] Data Format LD7 - LD0 (Hex)
Address Format: LA30 - LA0 (Hex).
[2] Data Protect state will be activated at end of each program cycle.
[3] Sector Address is the base address of a 64K byte sector of Flash Memory.
For example, *0C40 0000h*, *0C41 0000h*, *0C42 000h* etc.

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Figure 3.4: Flow Chart For Programming the 512K Flash Memory

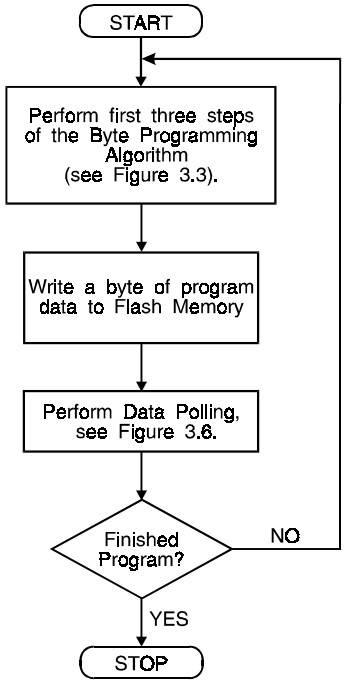
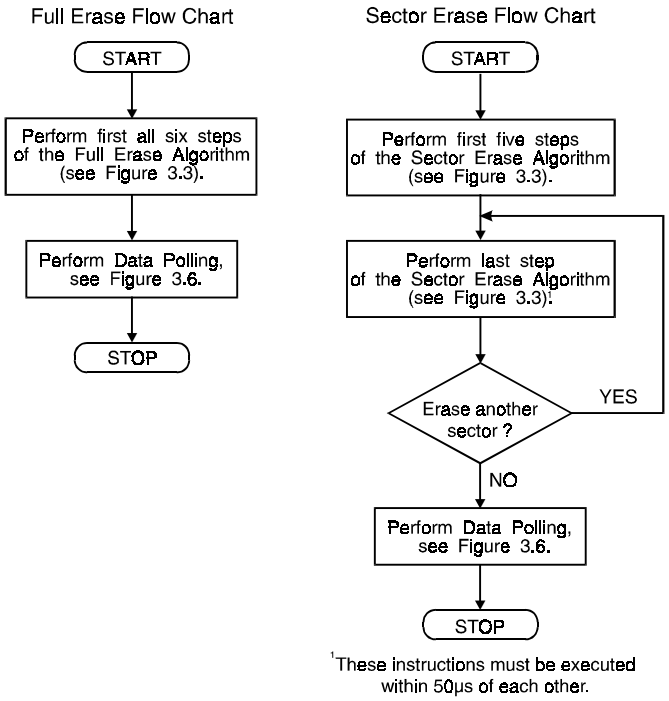
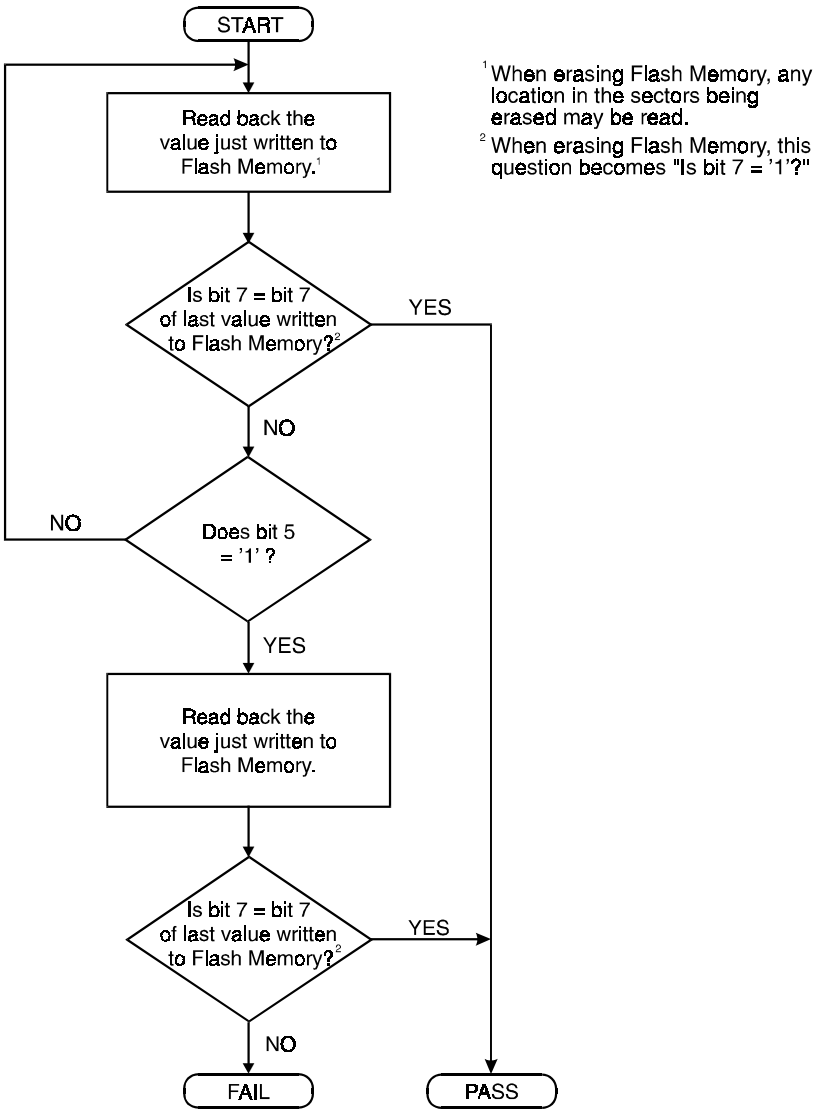


Figure 3.5: Flow Charts For Erasing the 512K Flash Memory



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Figure 3.6: Data Polling Flow Chart

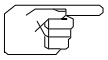


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3.6 RS-232 Serial Port

DBV66 incorporates an RS-232 compatible interface which is accessible via the Interconnect bus. The primary purpose of this interface is to provide communication between DBV66 and a terminal during software debug.

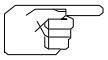
The interface is implemented using a Philips SCC2691 UART device which supports full-duplex asynchronous operation. Transfer rates of between 50 and 38400 bits/s are available with data lengths of 5, 6, 7 or 8 bits per character with a variety of stop bit lengths.



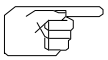
LSI's DBV66 support software includes SHARC functions for transferring data over the RS-232 serial port. If you are using this software and it provides all of the required functionality then you do not need to access the UART directly.

This section provides details on using the UART specifically with DBV66. Full details on the UART device are provided in the UART data sheet provided in an online format with this TRM, see Section 2.4.

The UART internal 3.6864 MHz clock and baud rate generator is employed on DBV66. The UART register set is located in the SHARC memory map from *0E00 0008h* to *0E00 000Fh* and in PCI space from S0_BASE+0E00 0020h to S0_BASE+0E00 003Eh. Note that S0_BASE is the base address of Space 0 in PCI space, see Section 4.5. The individual positions of the registers are indicated in Figure 3.7 below.



Each UART register is located on data lines D23-D16.



Consecutive accesses to the UART register set must be separated by a delay of 150 ns, with the exception of the Command Register. Consecutive accesses to this register must be separated by a delay of 2 µs. If more than one device is accessing the UART then care must be taken to ensure that these requirements are still met. When accessing the UART from the PCI bus, the 150 ns delay is automatically introduced. However, your code must still introduce the 2 µs delay for Command Register accesses.

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Figure 3.7: UART Register Set

SHARC Address	Read Only Register	Write Only Register	PCI Byte Address*
			S0_BASE+
0E00 0008h	Mode Register 1 or Mode Register 2	Mode Register 1 or Mode Register 2	0E00 0020h
0E00 0009h	Channel Status Register	Clock Select Register	0E00 0024h
0E00 000Ah	Reserved	Command Register	0E00 0028h
0E00 000Bh	Receive Holding Register	Transmit Holding Register	0E00 002Ch
0E00 000Ch	Reserved	Auxiliary Control Register	0E00 0030h
0E00 000Dh	Interrupt Status Register	Interrupt Mask Register	0E00 0034h
0E00 000Eh	Counter/Timer Upper	Counter/Timer Upper Register	0E00 0038h
0E00 000Fh	Counter/Timer Lower	Counter/Timer Lower Register	0E00 003Ch

* S0_BASE is the base address of Space 0 in PCI space, see Section 4.5.

The UART can generate interrupts upon a variety of conditions. These interrupts are routed to the SHARC /IRQ0 interrupt line and the Universe device as described in Chapter 9.

The RS-232 port is available off-board via either user-defined pins on the VME P2 connector or an on-board header. The pins on the P2 connector used to implement the RS-232 port are given in Table 3.5 and the pinout of the on-board header is given in Figure 3.8.

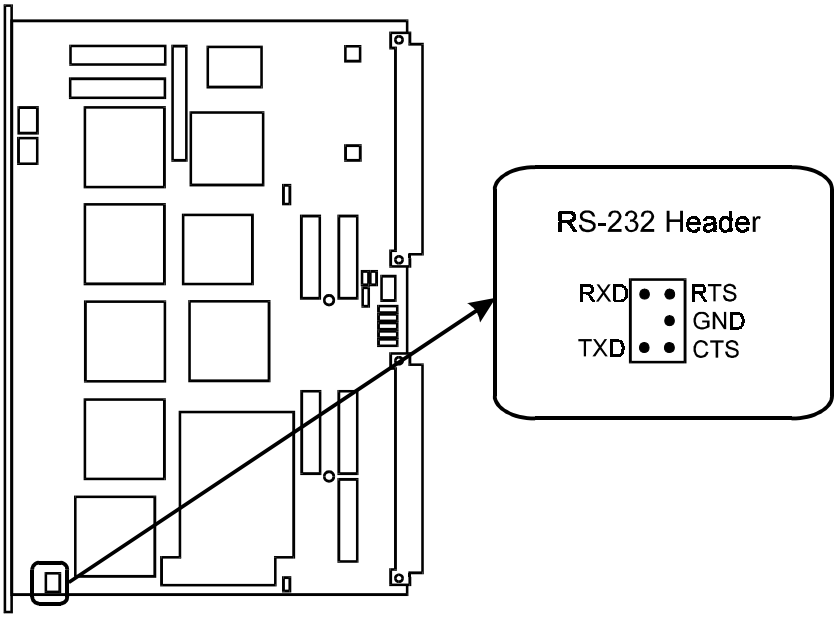
External circuitry must not be connected to the RS-232 port via both P2 and the on-board header at the same time. This can cause damage to both DBV66 and the peripheral RS-232 interface.

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Table 3.5: RS-232 Pins on VME P2 Connector

Signal	P2 pin
TXD	z11
RXD	z15
RTS	z17
CTS	z19

Figure 3.8: RS-232 On-Board Header Pinout



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3.7 Isolated Resources from the SHARCs

The SHARCs have access to the following resources on the section of the Interconnect bus isolated via transparent buffers:

- 32 bit DRAM on a DRAM66 module, see Section 3.7.1.
- PCI9060 Registers, see Section 3.7.2.
- Universe Registers, see Section 3.7.3.

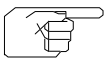
The SHARCs access these resources as though the buffers were not present. However, accesses to these resources from the PCI bus do not involve the rest of the Interconnect bus. Therefore, for example, a VME master could write a block of data to DRAM on a DRAM66 module without affecting accesses between the SHARCs and an external SRAM bank. Refer to Chapter 4 for details on the DBV66 PCI bus.

3.7.1 DRAM

DBV66 can be provided with DRAM by locating an LSI DRAM66 module on the board. The DRAM66 modules available provide 4, 8 or 16M x 32 of DRAM. This memory is reflected to fill the space from *0900 0000h* to *0A00 0000h* in the SHARC memory map and S0_BASE+0800 0000h to S0_BASE+0C00 0000h in the Interconnect bus PCI map (see Section 4.5). If no DRAM66 module is fitted then this space is reserved.

The DRAM is organised as 1M x 32 banks. Each bank has a page size of 1K x 32 with separate page fault detection. Therefore, when both the SHARCs and the PCI bus are attempting to access the DRAM at the same time, system efficiency can be increased by using buffers located in different banks. For example, the SHARCs could use a buffer in one bank while the host uses a buffer in another bank. When a page boundary is crossed in one bank, it will not incur an overhead on accesses to the other bank.

The DRAM66 module automatically inserts 1ws for accesses within a page and 5 ws for accesses across a page boundary. Note that DRAM66 automatically generates DRAM refresh cycles.



The SHARC *WAIT Register* must be correctly initialised before making any accesses to the DRAM from the SHARCs, see Section 3.9.

The SHARCs incorporate on-chip arbitration for accesses across the Interconnect bus, including accesses to the DRAM. Refer to Section 3.11 for more information.

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3.7.2 PCI9060 Registers

The PCI9060 provides a number of registers starting at *1800 0000h* in the SHARC memory map. These registers are used for the following functions:

- To allocate PCI memory and I/O spaces to the Interconnect bus.
- To hold identification information.
- To transfer data between the PCI bus and the Interconnect bus.
- To generate interrupts to the SHARCs or PCI bus.
- A number of other miscellaneous functions.

The PCI9060 registers must be correctly initialised at power-up/reset. This initialisation process involves accessing the registers via the PCI Configuration Space and reconfiguring a subset of the registers. This is not a trivial task and requires detailed knowledge of a number of concepts and registers.

The PCI9060 registers are subdivided into four groups. The names and locations in the SHARC memory map of these groups is given below:

- The PCI Configuration Registers are located from *1800 0000h* to *1800 000Fh*.
- The Local Configuration Registers are located from *1800 0020h* to *1800 002Bh*.
- The Shared Runtime Registers are located from *1800 0030h* to *1800 003Bh*.
- The Local DMA Registers are located from *1800 0040h* to *1800 004Ch*.

On DBV66, an EEPROM device is used to automatically initialise the PCI and Local Configuration Registers and two of the Mailbox Registers from the Shared Runtime Registers. This EEPROM device requires no user programming, the default register settings are provided in Appendix B of this TRM. The remaining PCI9060 register configuration is performed by LSI's device driver software for DBV66. When this software is used, there is no need to access the PCI9060 registers directly.

The PCI9060 registers are described in detail in the PCI9060 data sheet. This data sheet is provided in an online format, see Section 2.4.

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3.7.3 PCI Bus Resources

The space from *2000 0000h* to *3FFF FFFFh* in the SHARC memory map is available for performing direct master PCI accesses. Accesses to this space can be configured using the PCI9060 to access PCI configuration, memory or I/O space. The EEPROM defaults assigned to the PCI9060 registers subdivide this space into two regions:

- The space from *2000 0000h* to *2FFF FFFFh* is mapped to the start of the PCI memory map.
- The space from *3000 0000h* to *3FFF FFFFh* is mapped to the start of the PCI I/O map.

In order to allow access to the entire PCI memory and I/O maps, these blocks are relocatable. The location of the master access space in memory and/or I/O space is configured using the PCI9060 Local Configuration Registers.

The SHARCs can access PCI configuration space if bit 31 of the PCI9060 PCI Configuration Address Register for Direct Master to PCI IO/CFG is set to '1'. This register is located at *1800 002Bh* in the SHARC memory map. This will configure the PCI9060 to remap accesses to *3000 0000h* in the SHARC memory map to the PCI configuration space.

An alternative data transfer method, which does not require SHARC intervention, is to employ the PCI9060 two channel DMA controller. The DMA channels are configured, and transfers initiated, using the PCI9060 Local DMA Registers. These registers can be accessed from either the SHARCs or the PCI bus. Section 4.7 provides further details on making transfers across the PCI bus.

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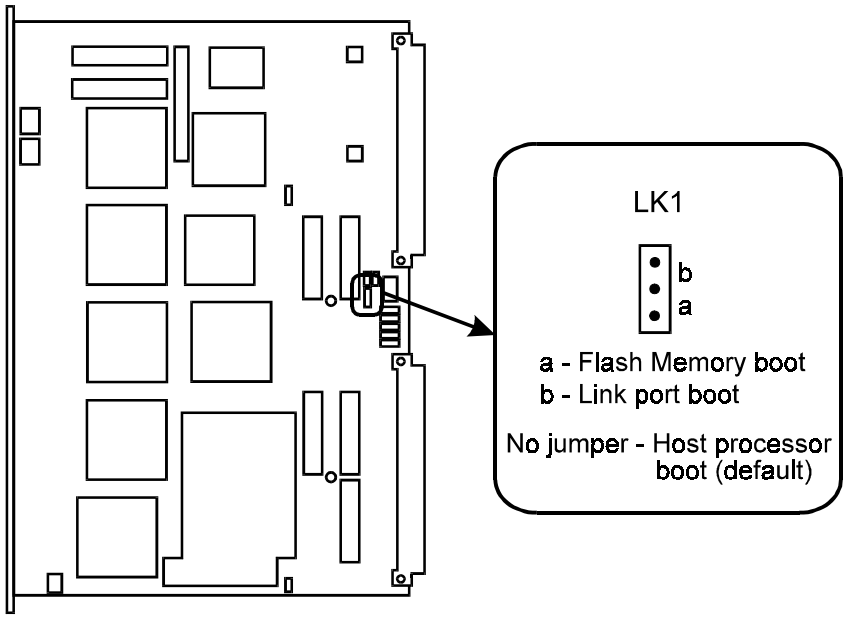
3.8 SHARC Boot Mode

The SHARCs on DBV66 can be configured to boot from link port, Flash Memory or a host processor (over the VMEbus) using hardware link LK1, see Figure 3.9. All SHARCs on DBV66 boot from the same source.

The subsections below outline each of the boot methods. Section 11.6 of the SHARC User's Manual provides full details on SHARC booting.

When using LSI's DBV66 support software, the board must be configured to boot from host processor.

Figure 3.9: SHARC Boot Mode Link - LK1



3.8.1 Host Processor Booting

When configured for host processor booting the SHARC automatically enters an idle state after reset and the program counter is set to *0002 0005h* in internal memory. The host processor, a VME master, must then write 256 user-defined instructions to the SHARC IOP *EPB0 Register*. DMA channel 6 is used to transfer these instructions to internal memory. Once the DMA transfer is complete, the SHARC executes these instructions.

On DBV66 all SHARCs can be booted simultaneously by writing to the *EPB0 Register* via the broadcast write space in the Interconnect bus PCI map. This register is located at S0_BASE+00E0 0010h, where S0_BASE is the base address of Space 0 in PCI space, see Section 4.5.

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3.8.2 Link Port Booting

When configured for link port booting the SHARC automatically enters an idle state after reset and the program counter is set to *0002 0005h* in internal memory. The SHARC configures itself to boot from link buffer 4 (the IOP *LBUF4 Register*), which is assigned to link port 4. This buffer must then receive 256 user-defined instructions from either a peripheral SHARC connected to link port 4 or by a device with access to the *LBUF4 Register* via the Interconnect bus. DMA channel 6 is used to transfer these instructions to internal memory. Once the DMA transfer is complete, the SHARC executes these instructions.

On DBV66 link port 4 from SHARC 1 is routed to a link port connector and port 4 from each of the other SHARCs is routed to the Broadcast Link Port. This enables the following booting mechanisms to be employed:

- SHARC 1 is booted from an external SHARC via the link port connector. SHARC 1 then simultaneously boots the rest of the SHARCs via the Broadcast Link Port.
- SHARC 1 is booted from an external SHARC via the link port connector. SHARC 1 then boots the rest of SHARCs by writing to the IOP *LBUF4 Register* in the Interconnect bus.
- SHARCs 2 to 6 are simultaneously booted from an external SHARC via the Broadcast Link Port. One of these SHARCs then boots SHARC 1 by writing to the IOP *LBUF4 Register* in the Interconnect bus.

3.8.3 Flash Memory Booting

When configured for Flash Memory (EPROM) booting the SHARC automatically enters an idle state after reset and the program counter is set to *0002 0005h* in internal memory. DMA channel 6 then automatically reads in 256 user-defined instructions from the Flash Memory. Once the DMA transfer is complete, the SHARC executes these instructions.

On DBV66 the SHARCs sequentially read the same instructions from the Flash Memory. SHARC 1 boots first and SHARC 6 last (SHARCs 4 and 2 boot last on four and two processor variants). Once the last SHARC has finished booting it can inform the other SHARCs that booting is complete. It could do this, for example, by using a software semaphore in the external SRAM.

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3.9 SHARC IOP *WAIT Register*

The SHARC IOP *WAIT Register* is located at *0000 0002h* in the SHARC memory map and is used to set up external memory wait states. It must be configured before the processor makes any accesses to external memory. If this is not done then the board will not function correctly. The only time when this rule does not apply is during Flash Memory booting. Note that the SHARC IOP *SYSCON Register* must also be set up as described in Section 3.10.

The value to be written to the *WAIT Register* is dependent on the memory configuration of DBV66. Table 3.6 details the individual bit settings for the *WAIT Register* for the different memory configurations of DBV66. The bit settings equate to the hexadecimal values given below.

- If DBV66 has 128K external SRAM banks then set the *WAIT Register* to 000C 9821h.
- If DBV66 has 512K external SRAM banks then bit 2 (WS512) of the Peripheral Status Register at *0E00 0001h* must be read to determine the number of wait states required by the SRAM:
  - If bit 2 reads ‘0’ then the SRAM requires 0ws and 000C 9821h should be written to the *WAIT Register*.
  - If bit 2 reads ‘1’ then the SRAM requires 1ws and 000C 98A5h should be written to the *WAIT Register*.

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Table 3.6: SHARC IOP *WAIT Register*

D31	D30	D29	D28	D27-D25	D24-D22	D21-D20
Reserved	**HIDMA**	**MMSWS**	**PAGEIS**	**PAGSZ**	**UBWS**	**UBWM**

D19-D17	D16-D15	D14-D12	D11-D10	D9-D7	D6-D5	D4-D2	D1-D0
EB3WS	**EB3WM**	**EB2WS**	**EB2WM**	**EB1WS**	**EB1WM**	**EB0WS**	**EBOWM**

Bit	Name	Function
1-0	EBOWM	External Bank 0 wait state mode[1] Set to '01' for internal wait state generation.
4-2	EB0WS	External Bank 0 number of wait states[1] For 128K x 48 or 0ws 512K x 48 Bank 0 SRAM, set to '000' for 0 ws, no Bus Idle and no Hold Time cycle. For 1ws 512K x 48 Bank 0 SRAM, set to '001' for 1ws, a Bus Idle cycle and no Hold Time cycle.
6-5	EB1WM	External Bank 1 wait state mode[2] Set to '01' for internal wait state generation.
9-7	EB1WS	External Bank 1 number of wait states[2] For 128K x 48 or 0ws 512K x 48 Bank 1 SRAM, set to '000' for 0 ws, no Bus Idle and no Hold Time cycle. For 1ws 512K x 48 Bank 1 SRAM, set to '001' for 1ws, a Bus Idle cycle and no Hold Time cycle.
11-10	EB2WM	External Bank 2 wait state mode[3] Set to '10' for internal and external acknowledge.
14-12	EB2WS	External Bank 2 number of wait states[3] Set to '001' for 1 ws, a Bus Idle cycle and no Hold Time cycle.
16-15	EB3WM	External Bank 3 wait state mode[4] Set to '10' for internal and external acknowledge.
19-17	EB3WS	External Bank 3 number of wait states[4] Set to '110' for 6 ws, no Bus Idle cycle and a Hold Time cycle.
21-20	UBWM	Unbanked memory wait state mode Set to '00' for external acknowledge only.
24-22	UBWS	Unbanked memory number of wait states Set to '000' for 0 ws, no Bus Idle and no Hold Time cycle.
27-25	PAGSZ	Page size for DRAM Reserved, set to '000'.
28	PAGEIS	Single idle cycle on DRAM page boundary crossing Reserved, set to '0'.
29	MMSWS	Single wait state for multiprocessor memory space access Set to '0' for no wait state between multiprocessor memory space accesses.
30	HIDMA	Single idle cycle for DMA handshake Set to '0' for no idle cycle after a read from an external DMA latch.
31	-	Reserved, set to '0'.

[1] Bank 0 is allocated to external SRAM Bank 0 on DBV66.

[2] Bank 1 is allocated to external SRAM Bank 1 on DBV66.

[3] Bank 2 is allocated to the optional DRAM on DBV66. Note that DBV66 does not employ the SHARC PAGE signal for DRAM accesses. This explains why the external DRAM is not located in Bank 0 as indicated in the SHARC User's Manual.

[4] Bank 3 is allocated to Flash Memory on DBV66.

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3.10 SHARC IOP *SYSCON Register*

The SHARC IOP *SYSCON Register* is located at *0000 0000h* in the SHARC memory map and is used for SHARC system configuration. A number of bits in this register must be correctly configured at power-up/reset:

- Bits 5-4 (*HPM*) must be set to ‘00’ before 32 bit accesses can be made to the SHARC IOP registers from the PCI bus. This setting ensures that no data packing is applied to transfers from the PCI bus to the Interconnect bus. Note that the default reset configuration of *HPM* configures the SHARCs to pack 16 bit accesses to 32 bit words. Therefore, if this register is configured from the host then initially two 16 bit accesses must be made to *SYSCON* in order to fully configure the register.
- We strongly recommend that bits 9-8 (*IMDW1* and *IMDW0*) are set to '00'. This configures the SHARC internal memory blocks for 32 bit data rather than 40 bit data. When using LSI's support software for DBV66, these bits must be set to '00'.
- Bit 10 (*ADREDY*) must be set to '1' to change the REDY signal to an active drive output.
- Bits 15-12 (*MSIZE*) must be set to ‘1101’ before the SHARC attempts any accesses to external memory. This sets the size of the external memory banks to 64M words.

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3.11 Interconnect Bus Arbitration

Arbitration is used to ensure that there is only one Interconnect bus master at any one time. Access is granted to competing bus master devices, the SHARCs and the PCI9060, according to the arbitration algorithm described in this section. Note that all accesses to the Interconnect bus from the PCI bus (from PMC modules and the VMEbus) employ the PCI9060.

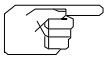
The arbiter is completely transparent. It recognises when the Interconnect bus is being accessed and accepts requests to read from or write to the bus from any of the bus master devices. The information in this section is provided to allow system performance to be optimised when making Interconnect bus accesses.

The arbiter will grant Interconnect bus access when a request is made, once the current access is completed. However, the arbitration algorithm dictates an order of preference for granting access permission if access to the Interconnect bus is requested by more than one device.

The DBV66 arbitration algorithm has two priority levels. The PCI9060 has highest priority and the SHARCs have equal priority below the PCI9060. Access is granted to the processors on a round-robin basis.

The order of preference for the SHARCs forms a chain from SHARC 1 to SHARC 2 etc. and back to SHARC 1 again. As each SHARC completes its access, one of the following will occur:

- If one or more of the other SHARCs is requesting the bus, it will pass control of the bus to the next SHARC in a round-robin sequence.
- If no other device is requesting the bus, it will hold it until one does.
- If the PCI9060 requests the bus, it will receive it once the current SHARC has completed its access. If no other SHARC is requesting the bus when it has completed its access, control is passed back to the original SHARC.



The signals requesting and granting the use of the bus to specific bus master devices are built in to the design of the arbitration system. These signals do not need to be considered during software development.

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Note that the arbitration algorithm described in this section applies to both the main and isolated sections of the Interconnect bus. However, there is one exceptional circumstance when the arbitration is slightly different. If the PCI9060 is the only device attempting to master the isolated section of the bus then it will be given the bus as normal. However, the PCI9060 will not master the main section of the bus during the access to the isolated section and the SHARCs will arbitrate for accesses to the main section as normal. Therefore, for example, the PCI9060 could make an access to the DRAM at the same time as a SHARC makes an access to the external SRAM.

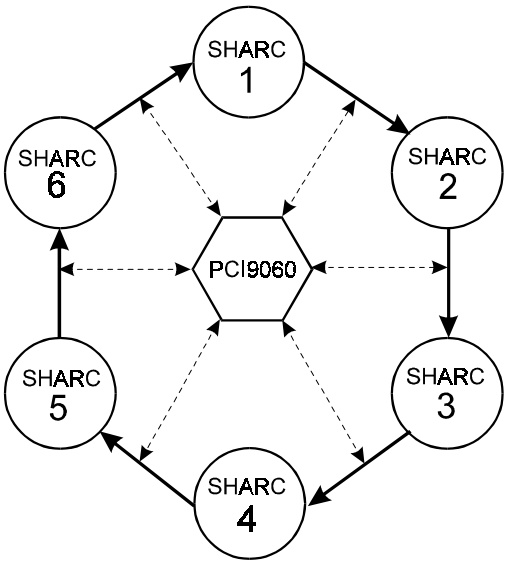
Figure 3.10 and Table 3.7 illustrate the example described below:

- SHARC 1 has use of the Interconnect bus.
- SHARC 3 makes a request for the Interconnect bus.
- SHARC 2 makes a request for the Interconnect bus.
- The PCI9060 makes a request for the Interconnect bus.
- When SHARC 1 completes its access it releases the Interconnect bus.
- The PCI9060 gains control of the Interconnect bus as it has higher priority than the processors.
- When the PCI9060 completes its Interconnect bus access, access is granted to SHARC 2 even though SHARC 3 made a request before SHARC 2.
- Once SHARC 2 gains the Interconnect bus, the priority of the SHARCs rotates so that SHARC 2 has highest priority under the PCI9060.
- Once SHARC 2 has completed its access, SHARC 3 gains the bus and the priority of the SHARCs rotates again.

Any number of request signals can be made at any one time, but only one device can be granted the Interconnect bus.

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Figure 3.10: Interconnect Bus Arbitration



The priority of each SHARC rotates as different SHARCs master the Interconnect bus. Throughout this process the PCI9060 maintains highest priority. If the PCI9060 requests the bus then it will be granted as soon as the master SHARC releases the bus.

Table 3.7 below illustrates the arbitration scheme using the example in the text.

Table 3.7: Interconnect Bus Arbitration Example

Current	Priority						
Master	**Highest**						**Lowest**
SHARC 1	PCI9060 (RM)	SHARC 1	SHARC 2 (RM)	SHARC 3 (RM)	SHARC 4	SHARC 5	SHARC 6
PCI9060	PCI9060	SHARC 1	SHARC 2 (RM)	SHARC 3 (RM)	SHARC 4	SHARC 5	SHARC 6
SHARC 2	PCI9060	SHARC 2	SHARC 3 (RM)	SHARC 4	SHARC 5	SHARC 6	SHARC 1
SHARC 3	PCI9060	SHARC 3	SHARC 4	SHARC 5	SHARC 6	SHARC 1	SHARC 2

Note that (RM) indicates that a device is currently requesting to master the Interconnect bus.

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3.12 Deadlock Resolution

DBV66 provides arbitration to prevent deadlock when a SHARC attempts to access the PCI bus at the same time as a PCI bus device attempts to access the Interconnect bus.

If the SHARC is attempting to access a different PCI device to the one which is attempting to access the Interconnect bus, then the SHARC is given priority.

If the SHARC is trying to access a PCI device which is itself attempting an access to the Interconnect bus then the PCI device is given priority. However, the arbitration mechanism cannot be guaranteed to operate correctly, resulting in erroneous board operation, in either of the following situations:

- The Interconnect bus has been locked by setting the *BUSLK* bit in the SHARC Core *MODE2 Register*.
- The SHARC access is initiated by a DMA controller in the I/O Processor rather than the Core Processor itself.

Note that since the Universe is a PCI device on DBV66, possible deadlock can occur if a SHARC is attempting to access a VME board at the same time as ANY VME board attempts to access the Interconnect bus.

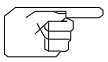
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4 PCI Bus

DBV66 provides a 32 bit PCI bus which forms an intermediate bus between the Interconnect bus and the VMEbus. The purpose of the bus is to allow PCI Mezzanine Cards (PMC) to be located on DBV66. These modules are compact plug-in cards which typically provide processing, I/O or memory facilities. DBV66 can accommodate up to two single width or one double width PMC module. This allows the functionality of the board to be easily altered/upgraded to meet application requirements.

The PCI bus is inherently highly software configurable. PCI configuration software must initialise the PCI devices on the bus before any accesses can be made over the PCI bus.

In general, the PCI configuration software can be integrated into the host system, such as in a PC where the PCI BIOS fulfils this function. Alternatively, the software may be custom code which is written for a particular system. In the case of DBV66, custom code is required to configure the board. LSI supplies VME host software which fulfils this function.



LSI's support software for DBV66 greatly increases the ease of use of the board by providing custom code to configure the on-board PCI bus. Unless you are experienced in using PCI systems then we strongly recommend that the software is used with the board.

If LSI's software is not used then you must generate the PCI configuration software yourself. All of the documentation required to do this is provided with the board, with the exception of the PCI Specification (see Section 1.4). This TRM provides details specific to DBV66 and the third party data sheets supplied describe the third party PCI devices on the board in more detail.

Note that the support software also provides functions for accessing the Interconnect bus from the VME host, accessing the RS-232 port from the SHARCs and accessing the VMEbus from the SHARCs.

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4.1 PCI Overview

The features of the PCI bus are listed and outlined below.

- **High Transfer Rates**

  The PCI bus provides a ‘burst’ data transfer mechanism in which a single address cycle is used for multiple data cycles. When using the burst mode, transfer rates of up to 132 Mbytes/sec can be achieved.

- **Memory, I/O and Configuration Space**

  Communication across the PCI bus takes place using three separate spaces. The memory and I/O spaces provide access between PCI devices while the configuration space is used specifically for configuring PCI resources on DBV66 at system initialisation.

- **PCI Bus Resource Allocation in Software**

  The regions allocated to PCI devices in the PCI memory and I/O maps are configured in software by accessing the PCI configuration space at system initialisation. This allows conflict free maps to be built up.

- **PCI Bridge Devices**

  Each PCI device must present a standard interface to the PCI bus. This is achieved using PCI bridge devices which interface a local bus on the PCI device to the PCI bus. These bridge devices include a standard register set, the PCI Configuration Registers, used for device configuration.

- **Device Identification in Software**

  The PCI Configuration Registers also include registers which can be read to identify the PCI device in software.

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4.2 PCI Data Transfer Overview

This section outlines how data transfers are made from one PCI device to another over the PCI bus. This information is applicable to all PCI systems and is provided as background information for users unfamiliar with the PCI bus.

The PCI bus forms an intermediate bus between local buses on the PCI devices attached to it. In order to transfer data from a resource on one PCI device to a resource on another the following steps must take place:

- Data must be transferred from one PCI device to the PCI bus.
- This data must then be transferred to the target PCI device.

There are two basic methods by which data can be transferred from a PCI device to the PCI bus. Either a direct, processor controlled, access can be made or a DMA controller can be used, if available. These methods are outlined in the following subsections.

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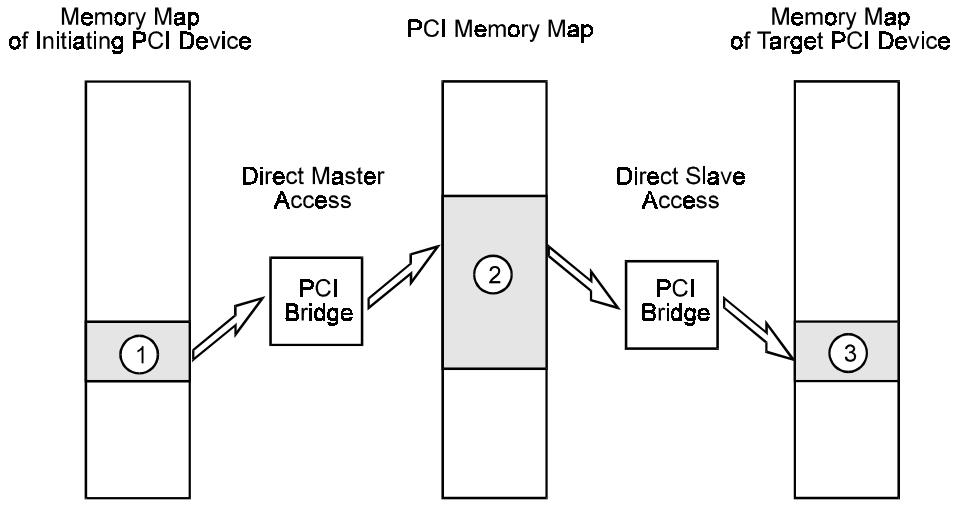
4.2.1 Direct Data Transfers

When making a direct data transfer, a processor on a PCI device writes the data to be transferred to a memory-mapped region provided for making PCI accesses. This data is then transferred to the PCI bus by the PCI bridge associated with the device. The data must then be transferred from the PCI bus to the target PCI device using the PCI bridge on the target PCI device. This process is illustrated in Figure 4.1.

The initial access is referred to as the ‘direct master access’ and the transfer of data from the PCI bus to the target is referred to as the ‘direct slave access’. When making a direct master access, it is necessary to know where a PCI resource can be accessed on the PCI bus. An access can then be made to that location.

The spaces on the PCI bus used to make data transfers are allocated to the devices at power-up/system reset. These spaces can then be configured such that direct master accesses to them are transferred to the required resource on the target.

Figure 4.1: PCI Data Transfer Using Direct Master/Slave Accesses



1. A memory-mapped space is accessed by a processor on the initiating PCI device. This access is then transferred to the PCI bus. This is the direct master access and is configured using the bridge on the initiating PCI device.
2. The space in the PCI memory map to which the access is transferred must correspond to a space allocated to the target PCI device at power-up/system reset.
3. The PCI access is finally transferred to the resource on the target PCI device. This is the direct slave access and is configured using the bridge on the target PCI device.

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4.2.2 DMA Transfers

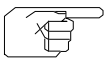
DMA controlled transfers across the PCI bus are similar to the direct master/slave accesses described in Section 4.3.1. However, when using a DMA controller, there is no need for a processor on the initiating PCI device to control the transfer of data to the PCI bus. The DMA controller is configured and the transfer initiated. The controller then moves the data between the resource on the initiating PCI device and the PCI bus. The target PCI device to/from which data is transferred must still set up a slave mapping.

4.3 DBV66 PCI Implementation

DBV66 provides up to four PCI devices on the PCI bus. These are the Interconnect bus, PMC module Sites 1 and 2 and the VMEbus. Depending on the software configuration of the PCI memory and I/O spaces, the following accesses are possible across the PCI bus:

- The SHARCs can access resources on the PMC modules and the VMEbus.
- The PMC modules can access resources on the Interconnect bus and the VMEbus. Note that in order to do this, a PMC module must have the capability to perform master accesses to the PCI bus.
- VME masters can access resources on the Interconnect bus and the PMC modules.

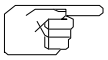
In order to make these accesses, the PCI bridges associated with the PCI devices must be correctly configured. The PCI bridges used on DBV66 are outlined in the following subsections.



PCI bridge configuration is not a trivial task and should only be attempted by experienced users. We recommend that LSI's support software is used with the board as this software performs all required bridge configuration.

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4.3.1 PLX PCI9060



The PCI9060 data sheet provides full details on the bridge's register set. Section 2.4 of this TRM describes how to install and view the data sheet.

A PLX PCI9060 device is used to interface the Interconnect bus to the PCI bus. It provides the standard PCI Configuration Registers needed to configure the Interconnect bus as a PCI device. It also incorporates three additional sets of registers as outlined below:

- **Local Configuration Registers**

  These registers are used to map accesses to the PCI bus to resources on the Interconnect bus (direct slave accesses). They also allow the SHARCs to make direct reads/writes to the PCI bus (direct master accesses).

- **Shared Runtime Registers**

  These include eight 32 bit Mailbox Registers and two 32 bit Doorbell Registers. These can be accessed from both the SHARCs and the PCI bus. The Mailbox Registers are available for general purpose message passing and the Doorbell Registers can be used to generate interrupts to the SHARCs or PCI bus.

- **Local DMA Registers**

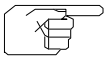
  The PCI9060 includes an on-chip two channel DMA controller which is configured using these registers.

These registers are always accessible from the SHARCs. The PCI9060 can also be configured via the PCI configuration space to provide access to them from the PCI bus.

On DBV66, an EEPROM device is used to initialise the PCI and Local Configuration Registers and two of the Mailbox Registers from the Shared Runtime Registers. The default EEPROM settings are provided in Appendix B of this TRM. The remaining PCI9060 register configuration is performed by LSI's device driver software for DBV66. When this software is used, there is no need to access the PCI9060 registers directly.

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4.3.2 Tundra Universe



The Universe User's Manual provides full details on the bridge's register set. Section 2.4 of this TRM describes how to install and view the data sheet.

A Tundra Universe device is used to interface the PCI bus to the VMEbus. It provides a standard VME64 interface and a PCI interface. As well as the PCI Configuration Registers, it incorporates two additional sets of registers as outlined below:

- **Universe Device Specific Registers (UDSR)**

  These registers are used to configure the DBV66 VME master/slave maps. They also include registers for implementing the Universe DMA controller, generating and routing interrupts etc.

- **VMEbus Control and Status Registers (VCSR)**

  These registers are used to implement the VME64 CR/CSR space.

4.3.3 PMC Bridges

Each PMC module located on DBV66 will provide a device which bridges the local bus on the module to the PCI bus. This bridge must provide the standard PCI Configuration Registers and may also provide additional registers.

The functionality of the PMC bridge should be described in the documentation accompanying the PMC module.

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4.4 PCI Configuration Space

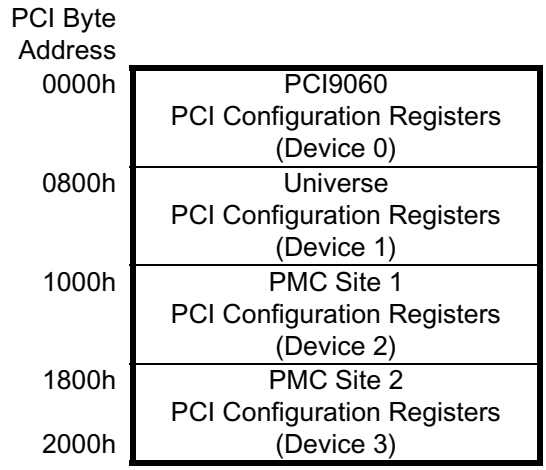
The PCI configuration space provides access to the PCI Configuration Registers of the PCI9060, Universe and PMC bridges. These registers are used to configure the PCI memory and I/O maps. They also fulfil additional functions such as identifying the types of resource in the system.

The location of the PCI Configuration Registers of the PCI9060, Universe and PMC module bridges in the PCI configuration space on DBV66 is set up in hardware. The regions allocated to each set of registers are indicated in Figure 4.2 below. The location (offsets) of the actual PCI Configuration Registers of each bridge within these regions are provided in the data sheet for the bridge.

LSI's support software for DBV66 uses the PCI configuration space at system initialisation to set up conflict-free PCI memory and I/O maps for DBV66. These maps are provided in the appropriate software User Guide. If you have this software then there is no need to access the PCI configuration space directly.

In order to access the PCI configuration space directly, bit 31 of the PCI9060 PCI Configuration Address Register for Direct Master to PCI IO/CFG must be set to '1'. This register is located at *1800 002Bh* in the SHARC memory map. This will configure the PCI9060 to remap accesses to *3000 0000h* in the SHARC memory map to PCI configuration space.

Figure 4.2: PCI Configuration Space

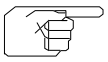


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4.5 PCI Slave Memory and I/O Maps

Each PCI device in the system can provide one or more spaces in the PCI memory and I/O maps. These spaces are used to make direct slave accesses to resources on the device from the PCI bus. For example, the PCI9060 provides two spaces, Space 0 and the expansion ROM space, for accessing resources on the Interconnect bus. The PCI9060 also provides two spaces for accessing its internal registers.

In order to allocate the size and base address of each space in the PCI memory and I/O maps, registers in the PCI bridges are used. In the case of the PCI9060, the PCI Configuration Registers fulfil this role. In the case of the Universe, a subset of the Universe Device Specific Registers are provided for this purpose. For a PMC module bridge, refer to the PMC module documentation.



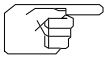
LSI's support software for DBV66 provides the board with PCI memory and I/O maps. Note that these are different from the defaults described below. Refer to the relevant LSI User Guides for further details.

4.5.1 Default Space 0 and Expansion ROM Remapping

The PCI9060 provides two spaces which can be placed in PCI memory or I/O space and mapped to resources on the Interconnect bus. These are referred to as 'Space 0' and the 'Expansion ROM' space, see Section 3.5 of the PCI9060 Data Sheet.

The EEPROM default values for the PCI9060 set up the following remapping. This remapping should not be altered.

- An access to the base address of Space 0 (S0_BASE) remaps to the start of the SHARC internal resources. However, note that the region S0_BASE+0000 0000h to S0_BASE+001F FFFFh, which corresponds to the 'internal memory space' in the SHARC memory map, is reserved.
- An access to an address 100h from the base address of the Expansion ROM space (E_BASE) remaps to the start of the PCI9060 Local DMA Registers.

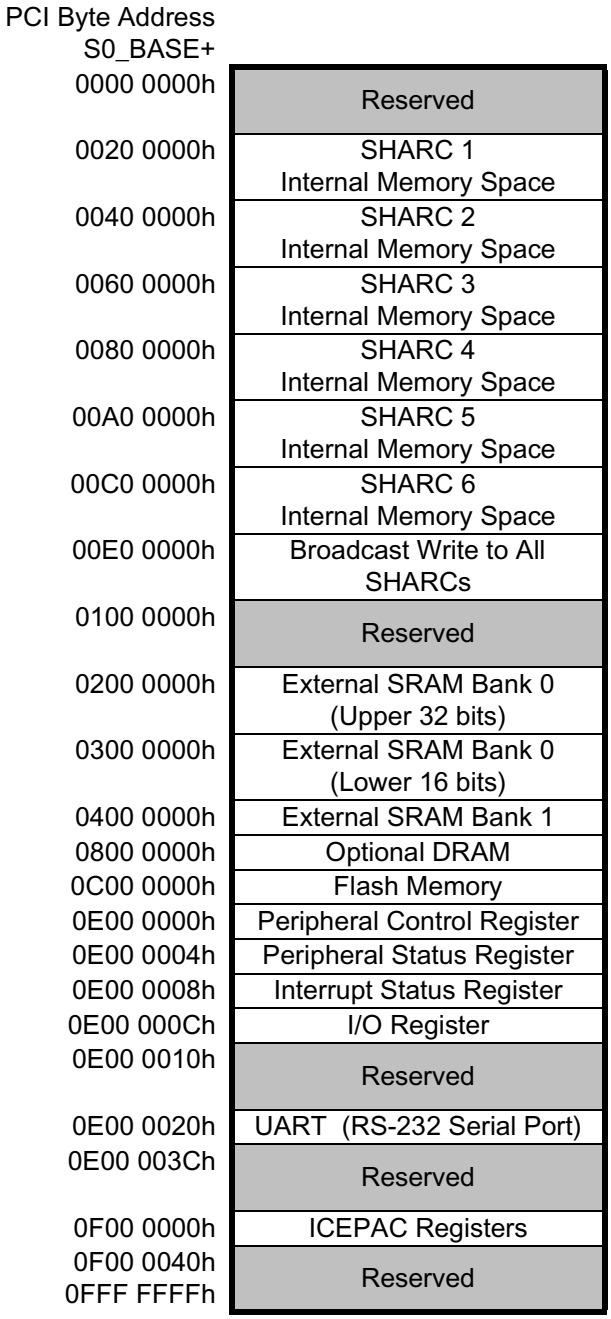


The PCI addresses provided in this manual for direct slave accesses from the PCI bus to the Interconnect bus and PCI9060 resources assume the above default remappings of Space 0 and Expansion ROM space.

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Figure 4.3 below illustrates the PCI offset addresses from S0_BASE used to access resources on the Interconnect bus. Figure 4.4 illustrates the PCI offset addresses from E_BASE used to access the PCI9060 Local DMA Registers.

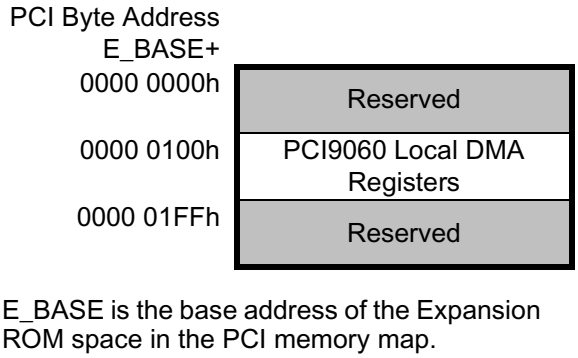
Figure 4.3: Interconnect Bus PCI Map



S0_BASE is the base address of Space 0 in the PCI memory or I/O map.

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Figure 4.4: PCI9060 DMA PCI Map



E_BASE is the base address of the Expansion ROM space in the PCI memory map.

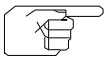
4.5.2 Allocating PCI Spaces to the VMEbus

The Universe provides up to five spaces in the PCI memory map which can be used to access the VMEbus. Four of these spaces are referred to as 'PCI Slave Images' and are each configured using four Universe registers. The fifth space is referred to as the 'Special PCI Slave Image' and is configured using a single Universe Register.

These spaces provide master access to the VME A16, A24 and A32 address regions. Refer to Section 6.2 of this TRM and Chapter 2 of the Universe User Manual for further details.

4.6 DBV66 PCI Initialisation

At power-up/system reset, the PCI devices on DBV66 must be initialised before accesses can be made across the PCI memory and/or I/O maps. This initialisation process will involve accessing the PCI Configuration Registers of each PCI device on DBV66 and configuring them as required.



The initialisation process is complex and should only be attempted by experienced users. LSI's DBV66 support software performs all of the required DBV66 initialisation from a host workstation.

The PCI Configuration Registers of each device are accessible via the DBV66 PCI configuration space. The addresses of the registers in this space are configured in hardware, see Section 4.4.

The device configuration process must allocate PCI memory and I/O spaces to the PCI devices. These spaces are then used to make direct slave accesses across the PCI bus. This process can be performed from either the VMEbus or from the SHARCs as outlined below.

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4.6.1 From the VMEbus

If the PCI bus is to be configured from the VMEbus then the following steps must be taken:

Step 1 A24 Access

DBV66 must be configured to allow access to the Universe register set via VME A24 space at power-up/reset. The VME A24 slave map used to access the Universe registers is referred to as the 'VMEbus Register Access Image' (VRAI), see Section 2.9.2 of the Universe User's Manual.

Hardware links LB2-LB10 are used to enable the VRAI and configure its A24 base address. Section 2.3.4 of this TRM provides further details on configuring these links.

Step 2 Universe PCI Configuration Registers

The Universe PCI Configuration Registers must then be set up by accessing them via the VRAI.

Figure 4.2 illustrates the location of the PCI Configuration Registers of the DBV66 devices in PCI configuration space.

Step 3 Universe Device Specific Registers

The Universe Device Specific Registers must be configured via the VRAI to provide access to the DBV66 PCI configuration space from the VMEbus. One of the four Universe VME slave images can be used for this purpose, see Section 2.4.1 of the Universe User's Manual.

Step 4 PCI9060 and PMC Bridge Configuration Registers

The PCI Configuration Registers of the PCI9060 and PMC bridges can then be configured from the VMEbus via the PCI configuration space.

The PCI9060 data sheet provides detailed descriptions on the PCI9060 register set including the PCI Configuration Registers.

Step 5 Universe Device Specific Registers

Finally, the Universe Device Specific Registers should be configured to provide VME master and slave memory maps for DBV66. Note that VME master accesses from the SHARCs and PMC modules on DBV66 are made via PCI bus slave images in the PCI memory or I/O maps. Section 2.2.4 of the Universe User's Manual provides further details on PCI bus slave images.

Once Steps 1 to 5 have been performed, DBV66 will have complete PCI memory and I/O maps.

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4.6.2 From the SHARCs

If the PCI bus is to be configured from the SHARCs then they must be configured to boot from the Flash Memory at power-up/system reset. The bootcode must perform the following steps to set up PCI memory and I/O maps:

Step 1 PCI9060 PCI Configuration Registers

The PCI9060 PCI Configuration Registers must be set up by accessing them in the SHARC memory map from *1800 0000h*.

Step 2 Universe and PMC PCI Configuration Registers

The PCI Configuration Registers of the Universe and the bridge on any PMC modules must be configured via the PCI configuration space. This space can be accessed as follows:

Set bit 31 of the PCI9060 PCI Configuration Address Register for Direct Master to PCI IO/CFG to '1'. This register is located at *1800 002Bh* in the SHARC memory map. This will configure the PCI9060 to remap accesses to *3000 0000h* in the SHARC memory map to PCI configuration space.

Figure 4.2 illustrates the location in PCI configuration space of the PCI Configuration Registers of the devices on DBV66.

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4.7 SHARC-PCI Single Accesses

The SHARCs on the Interconnect bus can access the PCI bus via the PCI9060 bridge. The region from *2000 0000h* to *3FFF FFFFh* in the SHARC memory map is provided for this purpose. Accesses to this region can be configured to access PCI configuration, memory or I/O space.

The values assigned to the PCI9060 Local Configuration Registers by the EEPROM split the region from *2000 0000h* to *3FFF FFFFh* into two equally sized spaces. The first region from *2000 0000h* to *2FFF FFFFh* (PCI Memory Master Access Space) maps to the start of the PCI memory map. The second region from *3000 0000h* to 3*FFF FFFFh* (PCI I/O Master Access Space) maps to the start of the PCI I/O map.

4.8 Interconnect-PCI DMA Accesses

In addition to making single accesses via the PCI master access space described in Section 4.10, the PCI9060 DMA controller can be used to transfer data to/from the Interconnect bus. The DMA controller can be programmed by accessing the PCI9060 Local DMA Registers from either the SHARCs, PCI bus or the VMEbus.

Note that DMA controlled transfers also incorporate an interrupt facility.

4.9 PCI Accesses to External SRAM Bank 0

SRAM Bank 0 on the Interconnect bus can be accessed from the PCI bus via the PCI9060 bridge. However, the bridge is only 32 bits wide and the SRAM in Bank 0 is 48 bits wide. To allow 40 bit data or 48 bit instructions to be accessed in external SRAM from the PCI bus the following solution is implemented. Note that a single 40 bit data word will require an entire 48 bit memory location.

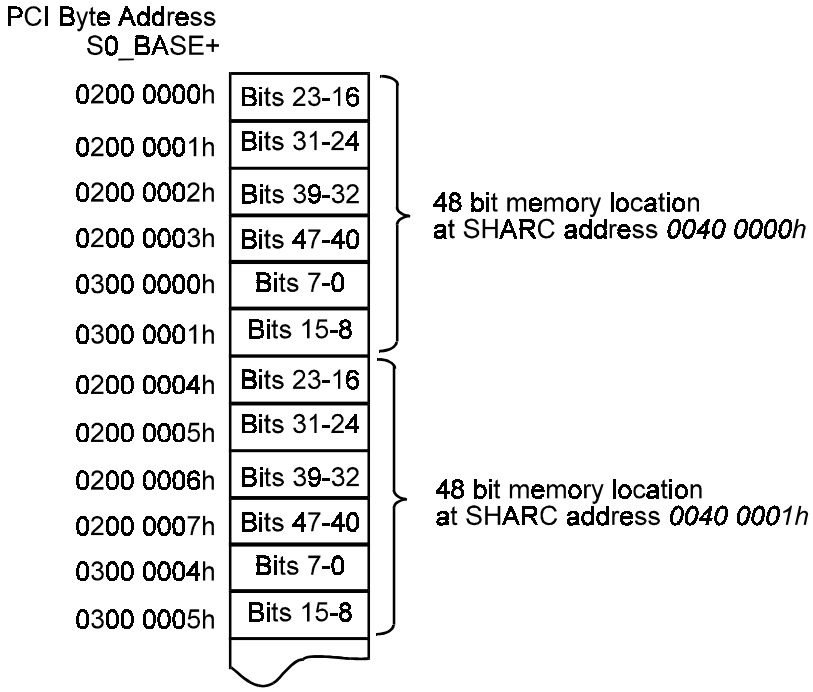
The Interconnect bus PCI map illustrated in Figure 4.3 provides two spaces for accessing SRAM Bank 0. The first of these spaces, from S0_BASE+0200 0000h to S0_BASE+02FF FFFFh, provides access to the most significant 32 bits of the SRAM (on data lines D47-D16). The second, from S0_BASE+0300 0000h to S0_BASE+03FF FFFFh, provides access to the least significant 16 bits of the SRAM (on data lines D15-D0). Note that S0_BASE is the base address of Space 0 in the PCI memory or I/O map, see Section 4.5.1.

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To access a full 48 bit location from the PCI bus, the access made to the two spaces can be combined to form the full 48 bit word. For example, to access a 48 bit word at SHARC address *0040 0000h* in the external SRAM, four byte accesses can be made from S0_BASE+0200 0000h and two byte accesses from S0_BASE+0300 0000h. Figure 4.5 below illustrates the PCI addresses used to access the two 48 bit memory locations at *0040 0000h* and *0040 0001h* in the SHARC memory map.

Note that it is not necessary to access an entire 48 bit word. For example, if only a 32 bit word at the start of Bank 0 needs to be accessed then a single 32 bit access can be made to S0_BASE+0200 0000h.

Figure 4.5: PCI Addressing for External SRAM Bank 0



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4.10 PCI Bus Arbitration

Arbitration is used to ensure that there is only one PCI bus master at any one time. Access is granted to competing bus master devices, the PCI9060, Universe and PMC module PCI bridges, according to the arbitration algorithm described in this section.

The arbiter is completely transparent to the user. It recognises when the PCI bus is being accessed and accepts requests to read from or write to the bus from any of the bus master devices. The information in this section is provided to allow system performance to be optimised when making PCI bus accesses.

The arbiter will grant PCI bus access when a request is made, once the current access is completed. However, the arbitration algorithm dictates an order of preference for granting access permission if access to the PCI bus is requested by more than one device.

Access is granted to the PCI devices on a round-robin basis. The order of preference for the PCI devices forms a chain from the Universe, PCI9060, PMC Site 1, PMC Site 2 and back to the Universe again.

Figure 4.6 and Table 4.1 illustrates the example described below:

- The Universe has use of the PCI bus.
- The PCI9060 makes a request for the PCI bus.
- PMC Site 1 makes a request for the Interconnect bus.
- When the Universe completes its access it releases the PCI bus.
- The PCI9060 gains control of the PCI bus.
- When the PCI9060 completes its PCI bus access, access is granted to PMC Site 1.

Any number of request signals can be made at any one time, but only one device can be granted the PCI bus.

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Figure 4.6: PCI Bus Arbitration

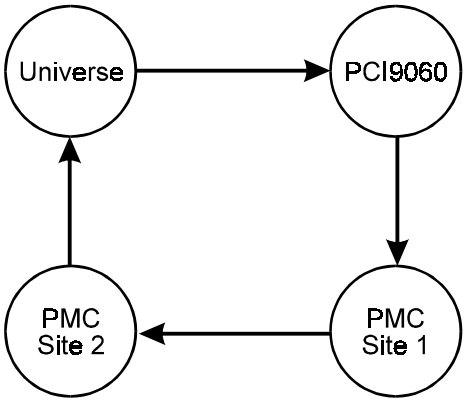


Table 4.1 below illustrates the priority scheme using the example in the text.

Table 4.1: PCI Bus Arbitration Example

Current Master	Priority		
	Highest		Lowest
Universe	PCI9060 (RM)	PMC Site 1 (RM)	PMC Site 2
PCI9060	PMC Site 1 (RM)	PMC Site 2	Universe
PMC Site 1	PMC Site 2	Universe	PCI9060

Note that (RM) indicates that a device is currently requesting to master the PCI bus.

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4.11 Deadlock Resolution

DBV66 provides arbitration to prevent deadlock when a SHARC attempts to access the PCI bus at the same time as a PCI bus device attempts to access the Interconnect bus.

If the SHARC is attempting to access a different PCI device to the one which is attempting to access the Interconnect bus, then the SHARC is given priority.

If the SHARC is trying to access a PCI device which is itself attempting an access to the Interconnect bus then the PCI device is given priority. However, the arbitration mechanism cannot be guaranteed to operate correctly, resulting in erroneous board operation, in either of the following situations:

- The Interconnect bus has been locked by setting the *BUSLK* bit in the SHARC Core *MODE2 Register*.
- The SHARC access is initiated by a DMA controller in the I/O Processor rather than the Core Processor itself.

Note that since the Universe is a PCI device on DBV66, possible deadlock can occur if a SHARC is attempting to access a VME board at the same time as ANY VME board attempts to access the Interconnect bus.

4.12 PMC Module Sites

4.12.1 PMC Facility Summary

DBV66 provides a number of facilities for use by PMC modules fitted to the board as outlined below. Note that in order to take advantage of these facilities, the PMC module must provide the relevant functionality.

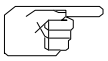
- PMC modules have a full master/slave access capability to the PCI memory, I/O and configuration spaces, see Section 4.4.
- PMC modules can generate interrupts to PCI interrupt lines INTA# to INTD#, see Chapter 9.
- The presence of PMC modules can be detected in software as described in Section 4.12.2.
- A PMC module in Site 1 has access to a number of user-defined pins on the VME P2 connector, see Section 4.12.3.

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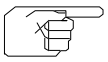
4.12.2 PMC Detection in Software

Application software can test for the presence of PMC modules using the DBV66 Peripheral Status and Control Registers by following the steps given below. Note that a particular PMC module may not support this functionality, refer to the module's documentation for more details.

- Write the value '110' or '111' to bits 7-5 (PMC_TEST) of the Peripheral Control Register to initiate the PMC module test. This register is located at *0E00 0000h* in the SHARC memory map and at S0_BASE+0E00 0000h in PCI space.
- Read bit 0 (PMC1) and/or bit 1 (PMC2) of the Peripheral Status Register. This register is located at *0E00 0001h* in the SHARC memory map and at S0_BASE+0E00 0004h in PCI space. If bit 0 reads '1' then there is a PMC in Site 1, if bit 1 reads '1' then there is a PMC in Site 2.



If a double width PMC module or a DRAM66 module is fitted to DBV66 then the PMC2 bit will indicate that Site 2 is empty.



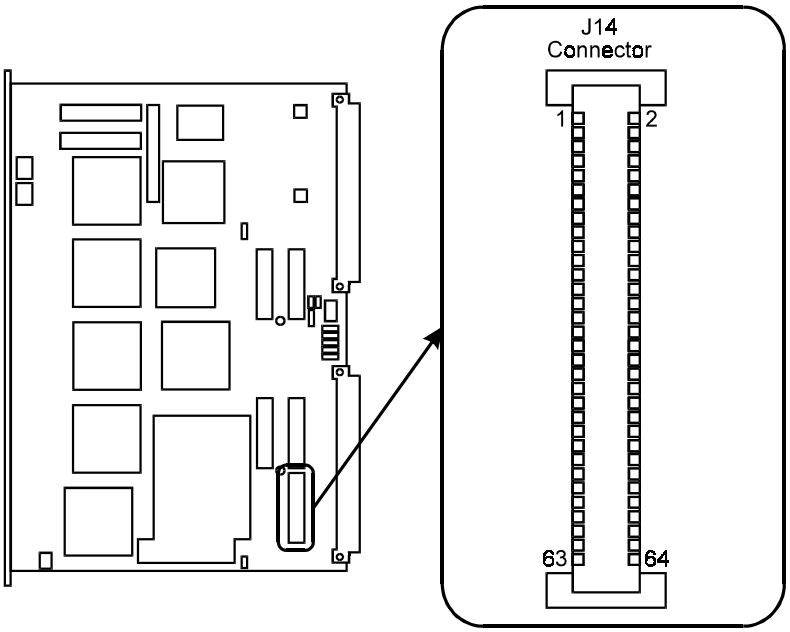
In addition to being used to test for PMC modules, bits 7-5 of the Peripheral Control Register can be used to enable/disable access to a PMC module via the PCI bus. If the bits are set to '000' (default setting) then the module cannot be accessed, or make accesses across the PCI bus. To enable PCI access for a PMC module, bits 7-5 must be set to '110'

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4.12.3 PMC Access to Pins on the VME P2 Connector

A PMC module in Site 1 on DBV66 has access to a number of user-defined pins on the VME P2 connector. The optional PMC J14 connector is provided for this purpose. Table 4.2 indicates which J14 pins are connected to which P2 pins. Figure 4.7 illustrates the pin numbering scheme of the J14 and connector.

Figure 4.7: Pin Numbers on J14 Connector



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Table 4.2: PMC Pins on P2 Connector

PMC Site 1 (J14)	VME P2 Pin	PMC Site 1 (J14)	VME P2 Pin
1	c1	33	c17
2	a1	34	a17
3	c2	35	c18
4	a2	36	a18
5	c3	37	c19
6	a3	38	a19
7	c4	39	c20
8	a4	40	a20
9	c5	41	c21
10	a5	42	a21
11	c6	43	c22
12	a6	44	a22
13	c7	45	c23
14	a7	46	a23
15	c8	47	c24
16	a8	48	a24
17	c9	49	c25
18	a9	50	a25
19	c10	51	c26
20	a10	52	a26
21	c11	53	c27
22	a11	54	a27
23	c12	55	c28
24	a12	56	a28
25	c13	57	c29
26	a13	58	a29
27	c14	59	c30
28	a14	60	a30
29	c15	61	c31
30	a15	62	a31
31	c16	63	c32
32	a16	64	a32

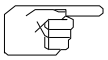
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5 VME Slave Interface

5.1 Introduction

DBV66 provides a software programmable slave interface to the VMEbus that complies with the VME64 Specification. This interface provides access to all resources on the Interconnect bus and on any PMC modules fitted to the board.



LSI's DBV66 support software programs the Universe to provide a VME slave memory map for DBV66, this map is provided in the relevant software User Guides. It also provides functions to allow access to most of the Interconnect bus resources from the VME host. If the support software is used and it provides all of the required functionality then there is no need to program or access the VME slave interface directly.

The VME interface on DBV66 is implemented using a Tundra Universe PCI-VME bridge. The VME slave functionality provided by the Universe is summarised below:

- Allows slave access to the PCI configuration, memory or I/O spaces from any VME address space except A64 space.
- Maps VME interrupts to PCI interrupts allowing VME masters to interrupt the SHARCs via VME interrupt lines /IRQ1 to /IRQ7.
- Provides a software interrupt facility allowing VME masters to interrupt the PMC modules or SHARCs without using the VME interrupt lines.
- Can function as an Auto-ID slave.

DBV66 supports D8, D16, D32, D32 block transfers (BLTs) and D64 multiplexed block transfers (MBLTs) VME slave accesses. However, due to fundamental differences in the way in which the VME and PCI buses handle individual bytes of data, care must be taken to ensure that data is interpreted correctly once it has been transferred.

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When making the following transfers, data will always be interpreted correctly by both the SHARCs on DBV66 and the processors on the target board:

- Any transfer between DBV66 and another DBV66 board.
- 32 bit data types transferred using D32 accesses between DBV66 and any another VME board.
- D8 accesses between DBV66 and any another VME board.

If another access type is required then consideration must be made of how bytes of data are transferred between DBV66 and the VMEbus. Refer to Appendix C for more details.

Section 5.2 below describes how access is provided to the Universe registers from the VMEbus at power-up/system reset. Section 5.3 then outlines how the Universe can be configured to provide DBV66 with a full VME slave memory map.

Full details on the Universe device are provided in the Universe User's Manual. This manual is supplied in an online format which can be installed, viewed and printed as described in Section 2.4.

5.2 Universe Access at Power-Up/System Reset

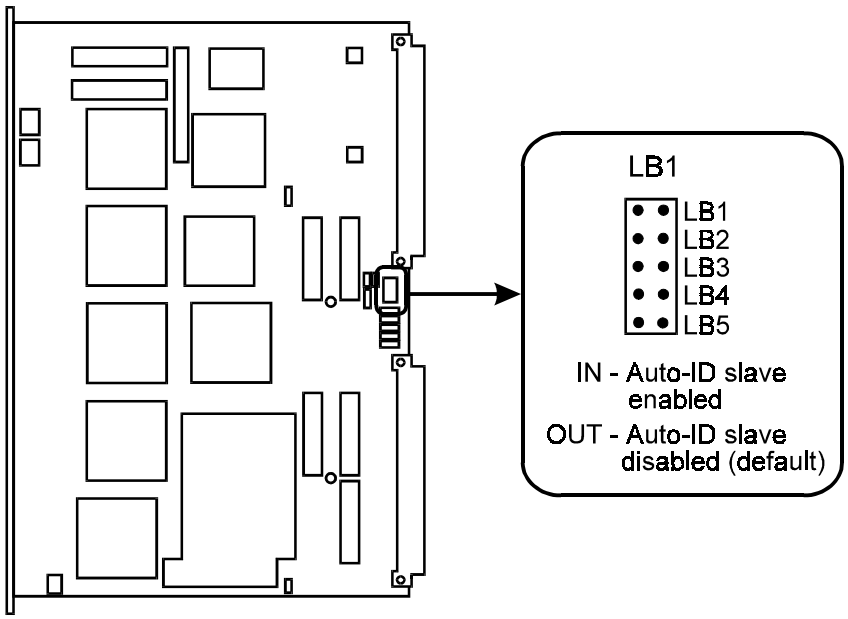
At power-up/system reset, the Universe Registers can be accessed from either the VMEbus or the PCI bus. The options available via these two methods are discussed separately in the subsections below.

5.2.1 Universe Access Via the VMEbus

If the Universe takes part in a VME64 Auto-ID cycle then the Universe registers can be accessed via VME64 CR/CSR space. Hardware link LB1 on DBV66 is used to enable/disable this functionality as illustrated in Figure 5.1 below. For further details refer to Section 2.2.5 of the Universe User Manual.

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Figure 5.1: Universe Auto-ID Enable - LB1



If Auto-ID is not implemented then the Universe VMEbus Register Access Image can be used to access the Universe registers. On DBV66 this image can be located in A24 space. Hardware links LB2 and LB3-LB10 are used to enable and configure the base address of this image respectively, see Section 2.3.4.

After power-up/system reset, the VMEbus Register Access Image can be controlled using the Universe VRAI_CTL and VRAI_BS Registers.

5.2.2 Universe Access Via the PCI bus

The SHARCs and any PMC module with a PCI master access capability can access the Universe PCI Configuration Registers at power-up/system reset via the PCI configuration space. The Universe is presented as Device 1 in the PCI configuration space on DBV66 as illustrated in Figure 4.2.

The other Universe registers (the Device Specific Registers and VMEbus Configuration and Status Registers) cannot be accessed via configuration space. However, the PCI Configuration Registers can be configured to provide access to all of the Universe registers. This is achieved by using one of the Universe VME slave images. Refer to Section below and Section 2.4.1 of the Universe User's Manual for more details.

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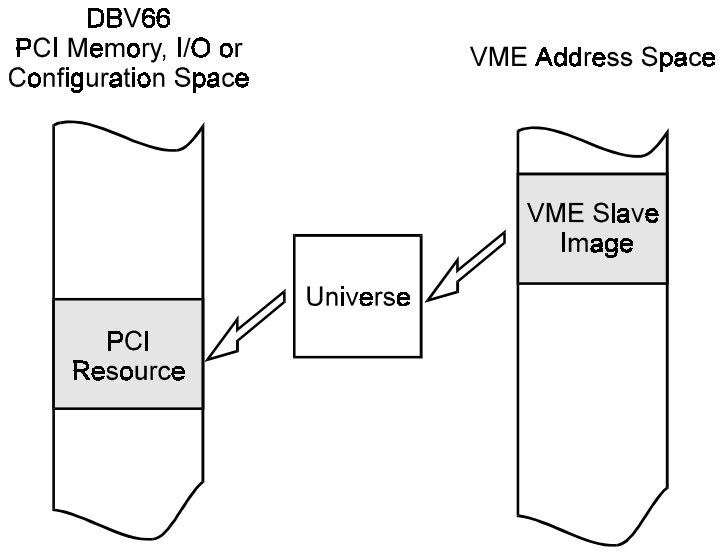
5.3 DBV66 VME Slave Configuration

In addition to the VMEbus Register Access Image outlined in Section 5.2.1, the Universe provides four VME slave images which can be individually mapped to regions in the PCI memory, I/O or configuration spaces. The mapping and enabling of each image is fully programmable using the Universe VSIx_CTL, VSIx_BS, VSIx_BD and VSIx_TO Registers (where x is 0 for Image 0 etc.).

Each image can be mapped from VME address space A16, A24, A32, User 1 or User 2 to either PCI memory, I/O or configuration space.

Once a VME slave image has been configured and enabled, accesses to the image are translated to the PCI bus as illustrated in Figure 5.2 below. Note that the location of the PMC module and Interconnect bus resources in the PCI memory and I/O spaces is configured in software. Therefore, in order to make a VME slave access to these resources, the PCI memory or I/O space must first be configured as outlined in Section 4.5.

Figure 5.2: VME Slave Access to DBV66



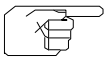
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5.4 Supported Transfers

DBV66 supports D32 transfers and slave block transfers. The transfer modes which are supported are listed and described below.

- **VME Read-Modify-Write Cycles**

  A VME RMW cycle to a Universe VME slave image can be maintained as an indivisible access on the PCI bus. This is achieved by setting the LLRMW bit in the Universe VSIx_CTL Register to '1'.

  Note that if a VME slave image is set to allow RMW cycles then this may introduce overhead to general read accesses.

- **Block/Burst Transfers**

  PCI transfers in which a single address is followed by multiple data cycles are referred to as burst transfers. The equivalent VME transfers are referred to as block transfers. If a VME slave image is configured to map to PCI I/O or configuration space then a block transfer to the image will be split into single cycle accesses on the PCI bus. However, block transfers can be maintained if the image is mapped to PCI memory space and pre-fetching is enabled using the PREN bit in the Universe VSIx_CTL Register.

- **VME64 Locked Cycles**

  The Universe automatically translates VME64 locked transfers to PCI locked transfers.

Note that if you require large blocks of data to be read from DBV66, it is recommended that you use the Universe DMA controller. The VME board requesting the data can program the DMA controller to act as the VME master. The DMA controller then reads data from the PCI bus resource via PCI memory space and writes the data to the target board. This will improve the data transfer rate from DBV66. LSI's software support packages make use of the Universe DMA controller in this way. The use of the DMA controller is described in detail in the Universe User Manual.

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5.5 VME Interrupts to DBV66

The Universe can be configured to respond to interrupts on any or all of VME interrupt lines /IRQ1 to /IRQ7. This is achieved as described in the tutorial steps in Section 9.9.2. Upon detection of an interrupt on one of these lines, a corresponding IACK cycle is automatically generated. The Status/ID vector returned by the interrupter is then stored in the associated Universe VIRQx Status/ID Register. The Universe LINT_STAT Register can be read to determine which VME interrupt level the interrupt was received on.

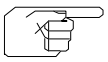
VME interrupts on /IRQ1 to /IRQ7 are all routed to PCI interrupt line INTA#. This line is routed to the SHARC /IRQ0 interrupt line along with a number of other interrupt sources. In order to determine whether a SHARC /IRQ0 interrupt is due to a VME interrupt, read bit 0 of the DBV66 Interrupt Status Register. This bit reads ‘1’ if a VME interrupt is currently generating an INTA# interrupt and ‘0’ otherwise.

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6 VME Master Interface

6.1 Introduction

DBV66 provides a master interface to the VMEbus that complies with the VME64 Specification. This interface provides the Interconnect bus and PMC modules with access to resources on the VMEbus.



LSI's DBV66 support software programs the Universe to provide a VME master memory map for DBV66, this map is provided in the relevant software User Guides. It also provides functions to allow the SHARCs to make VME accesses. If the support software is used and provides all required functionality then there is no need to program or access the VME master interface directly.

The VME interface on DBV66 is implemented using a Tundra Universe PCI-VME bridge. The VME master functionality provided by the Universe is summarised below:

- Allows master access to the VMEbus from either the PCI memory or I/O spaces.
- Allows PCI interrupts to be mapped to VME interrupts allowing the SHARCs on the Interconnect bus to generate VME interrupts on lines /IRQ1 to /IRQ7.
- Provides a software interrupt facility allowing the SHARCs on the Interconnect bus and PMC modules to generate VME interrupts on lines /IRQ1 to /IRQ7.
- Can function as System Controller when located in Slot 1.
- Can function as an Auto-ID monarch.

DBV66 supports D8, D16, D32, D32 block transfers (BLTs) and D64 multiplexed block transfers (MBLTs) VME slave accesses. However, due to fundamental differences in the way in which the VME and PCI buses handle individual bytes of data, care must be taken to ensure that data is interpreted correctly once it has been transferred.

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When making the following transfers, data will always be interpreted correctly by both the SHARCs on DBV66 and the processors on the target board:

- Any transfer between DBV66 and another DBV66 board.
- 32 bit data types transferred using D32 accesses between DBV66 and any another VME board.
- D8 accesses between DBV66 and any another VME board.

If another access type is required then consideration must be made of how bytes of data are transferred between DBV66 and the VMEbus. Refer to Appendix C for more details.

Full details on the Universe device are provided in the Universe User's Manual. This manual is supplied in an online format which can be installed, viewed and printed as described in Section 2.4.

6.2 VME Master Accesses

The SHARCs and PMC modules with a PCI master capability can perform VME master accesses via the Universe. There are two ways in which the master access can be initiated. The first of these involves configuring the Universe to provide PCI slave images in the PCI memory, I/O or configuration spaces which are then mapped onto the VMEbus. The second method is to employ the Universe DMA controller.

Section 6.2.1 and Section 6.2.2 describe the PCI slave images provided by DBV66 and their implementation. These images are documented in detail in Section 2.4.2 of the Universe User's Manual.

Section 6.2.3 outlines the Universe DMA controller. This DMA controller is documented in detail in Section 2.8 of the Universe User's Manual.

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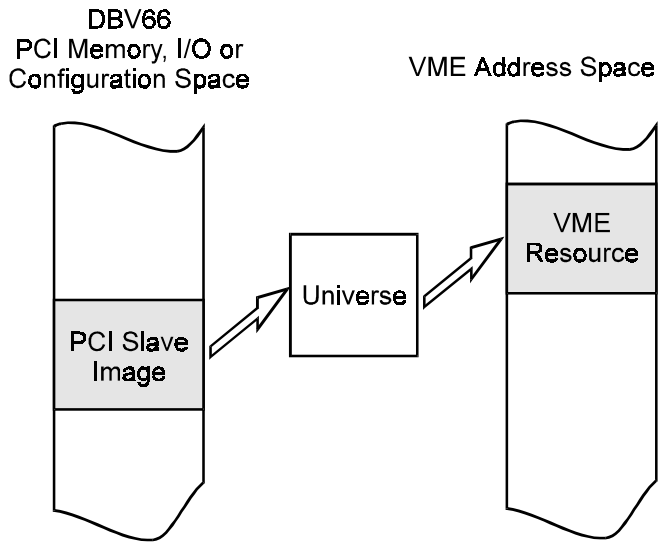
6.2.1 General Purpose PCI Slave Images

The Universe provides four general purpose PCI slave images which can be individually mapped from PCI space to regions in VME address space. The mapping and enabling of each image is fully programmable using the Universe LSIx_CTL, LSIx_BS, LSIx_BD and LSIx_TO Registers (where x is 0 for Image 0 etc.).

Each image can be mapped from PCI memory, I/O or configuration space to either VME A16, A24 or A32 space.

Once a PCI slave image has been configured and enabled, accesses to the image are translated to the VMEbus as illustrated in Figure 6.1 below.

Figure 6.1: VME Slave Access to DBV66



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6.2.2 Special PCI Slave Image

In addition to the general purpose PCI slave images described in Section 6.2.1, the Universe provides a special PCI slave image. This image differs from the general purpose images as follows:

- Its size is fixed at 64 Mbytes and it must be located on a 64 M bytes boundary.
- It provides access to both A16 and A24 spaces without reconfiguration where a general purpose image only provides access to a single address space.
- It is split into four regions, each providing access to both A16 and A24 space. The Program/Data and Supervisor/User address modifier codes for each region can be individually configured.

The Universe SLSI Register is used to configure and enable the special PCI slave image.

6.2.3 Universe DMA Transfers

The Universe incorporates a single channel DMA controller which can be used to transfer data between the PCI memory space and the VMEbus. Note that the DMA controller does not require the Universe PCI slave images to be configured.

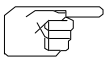
The configuration and use of the DMA controller is described in Section 2.8 of the Universe User Manual.

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6.3 Interrupts to the VMEbus

Interrupts to the VMEbus on interrupt lines /IRQ1 to /IRQ7 can be generated via the Universe from the following sources:

- PCI interrupt lines INTA# to INTD# (interrupts are generated on these lines by the PCI9060 device and PMC modules).
- The UART device used to provide the RS-232 serial interface.
- The ICEPAC which can be used to control the DBV66 JTAG circuitry.
- A Bus Error generated when a VME access is made to an invalid Interconnect bus location.
- Internal sources including a software interrupt.



The SHARCs can generate VME interrupts via the Universe device by generating an INTA# interrupt using the PCI9060 or by employing the Universe internal software interrupt source.

If a software interrupt and another interrupt source simultaneously request an interrupt then the software interrupt is given priority. This section only discusses the software interrupt. For further details on the other interrupt sources, refer to Chapter 9.

A software interrupt to the VMEbus can be generated by changing the status of the SW_INT bit in the Universe VINT_EN Register from ‘0’ to ‘1’. This bit should then be set to '0' before another VME interrupt can be generated. Note that setting this bit to '0' clears the VME interrupt. The VME interrupt level on which the interrupt is generated is configured via the SW_INT field (bits 18-16) in the Universe VINT_MAP1 register. The Universe provides support for a single 8 bit Status/ID vector for all interrupt levels. Bits 7-1 of this vector can be set by writing to the STATID field (bits 31-25) in the Universe STATID Register. Bit 0 of the vector is automatically set to ‘0’ when a software interrupt is being generated.

The relevant Universe register bits used for generating software interrupts to the VMEbus are described in Table 6.1 below.

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Table 6.1: Universe VME Software Interrupt Registers

Register	Bits	Description
VINT_MAP1	18-16 (SW_INT)	Used to set the VMEbus interrupt level. **Bit 18 Bit 17 Bit 16 Interrupt Level** 0 0 0 No Interrupt 0 0 1 /IRQ1 0 1 0 /IRQ2 0 1 1 /IRQ3 1 0 0 /IRQ4 1 0 1 /IRQ5 1 1 0 /IRQ6 1 1 1 /IRQ7
VINT_EN	12 (SW_INT)	Used to initiate the VME interrupt. Changing the status of this bit from '0' to '1' generates a VME interrupt.
STATID	31-24	These bits are used to provide the Status/ID vector. Bit 24 is automatically set to '0' for software interrupts.

To generate an interrupt to the VMEbus follow the instructions below.

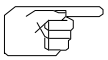
- ❑ Load the Status/ID vector into the STATID Register
- ❑ Set bits 18 to 16 (SW_INT) of the VINT_MAP1 Register to the VME interrupt level required.
- ❑ Change the status of bit 12 (SW_INT) in the VINT_EN register from '0' to '1'.

When the Universe detects a VME IACK cycle, the 8 bit Status/ID vector is placed on the VMEbus. The software interrupt is automatically cleared on completion of the VME interrupt cycle.

Since the software interrupt is only generated when the SW_INT bit in the VINT_EN Register is set from '0' to '1', this bit must be set to '0' before a further VME software interrupt can be generated.

6.4 System Controller Facilities

DBV66 can act as the system controller for your VME system. This is achieved by installing DBV66 in Slot 1 of your VME rack. The Universe automatically detects Slot 1 installation and enables its system controller functions.



Your system must provide one (and only one) system controller.

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7 SHARC Link Ports

7.1 Introduction

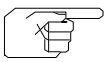
The DBV66 board's parallel processor system can support optimum performance by distributing tasks between two or more SHARCs. High performance multi-processing requires rapid transfer of data between processors. This can be achieved on DBV66 without employing the Interconnect bus by utilising the high speed parallel link ports available to each SHARC to provide rapid processor-to-processor communication.

The key features of each SHARC link port include:

- Maximum rate of 40M bytes/s bidirectional data transfer operations with 40 MHz SHARCs.
- Link port data can be directly accessed by the SHARC Core Processor or the SHARC DMA controller.
- Access is also provided to link port data for external host processors. On DBV66 link port data can be directly accessed from the VMEbus.
- Automatic arbitration and handshaking to ensure communication synchronisation.
- Support for a wide variety of multi-processor architectures.

Each SHARC on DBV66 has six link ports numbered 0 to 5. The SHARC also provides six link buffers for use with the ports. Each buffer can be independently assigned to a link port, more than one buffer can be assigned to a port if required.

The routing of the link ports on DBV66 has been designed to allow optimum access between SHARCs on DBV66 and peripheral boards, see Section 7.2 below.



Unlike similar link ports on other DSPs such as Texas Instruments' TMS320C4x, the SHARC link ports cannot be damaged by contention. In other words, configuring two connected ports as outputs will not result in damage to the SHARCs. However, this type of configuration should be avoided.

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7.2 Link Port Routing

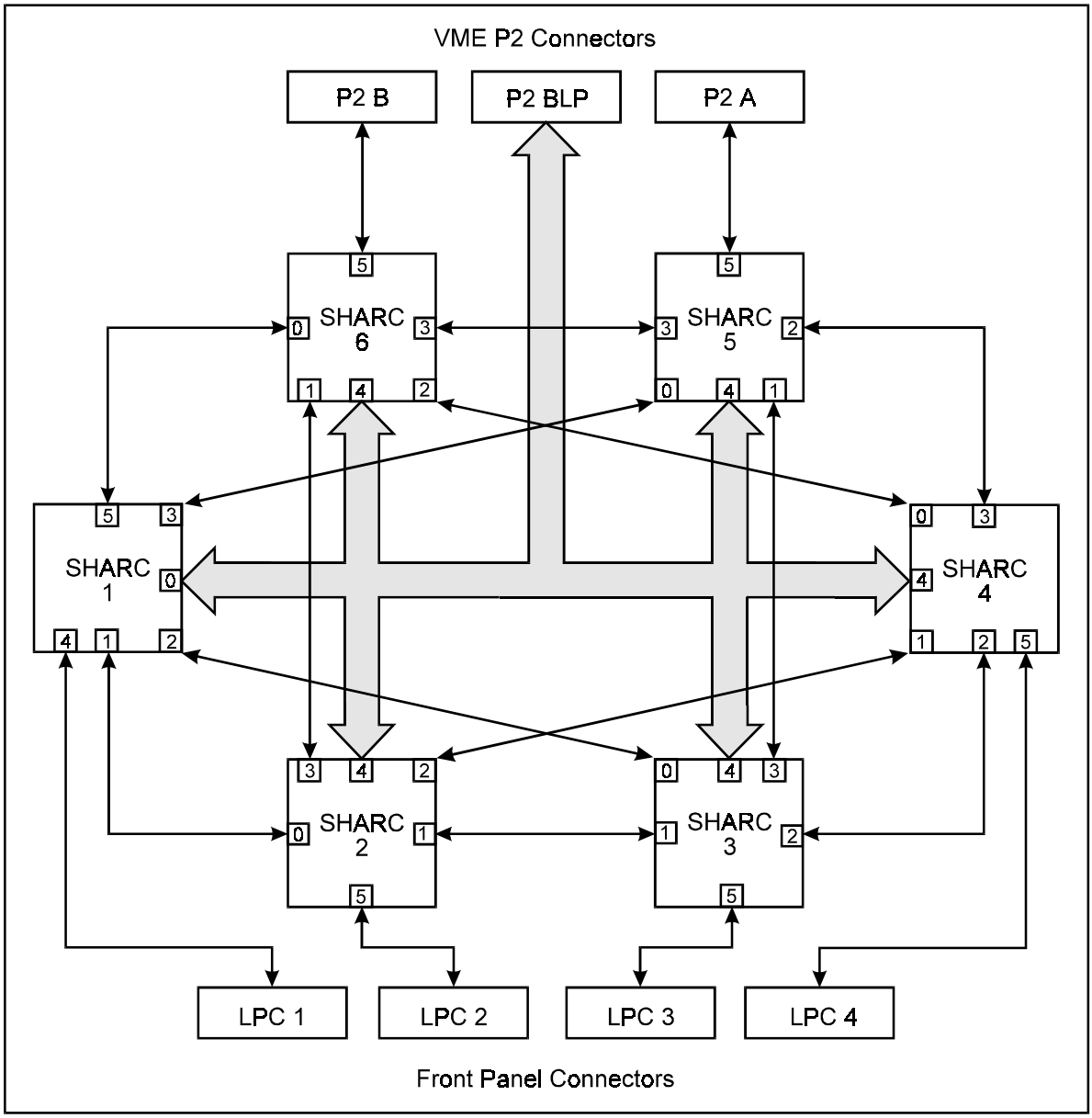
The routing of the SHARC link ports is dependent on the number of SHARCs located on the Interconnect bus. However, each configuration provides a number of common features:

- Each SHARC is connected to the other SHARC(s) on DBV66.
- Two link ports are available over the VME P2 connector.
- Up to four link ports are individually routed to link port connectors for access off-board.
- One port from each processor is connected together to form a Broadcast Link Port (BLP). The BLP provides each SHARC with the ability to broadcast data to all other SHARCs on DBV66. The BLP is described in more detail in Section 7.3 below.

Figure 7.1 to 7.3 below illustrate the link port routing on six, four and two SHARC variants of DBV66 respectively.

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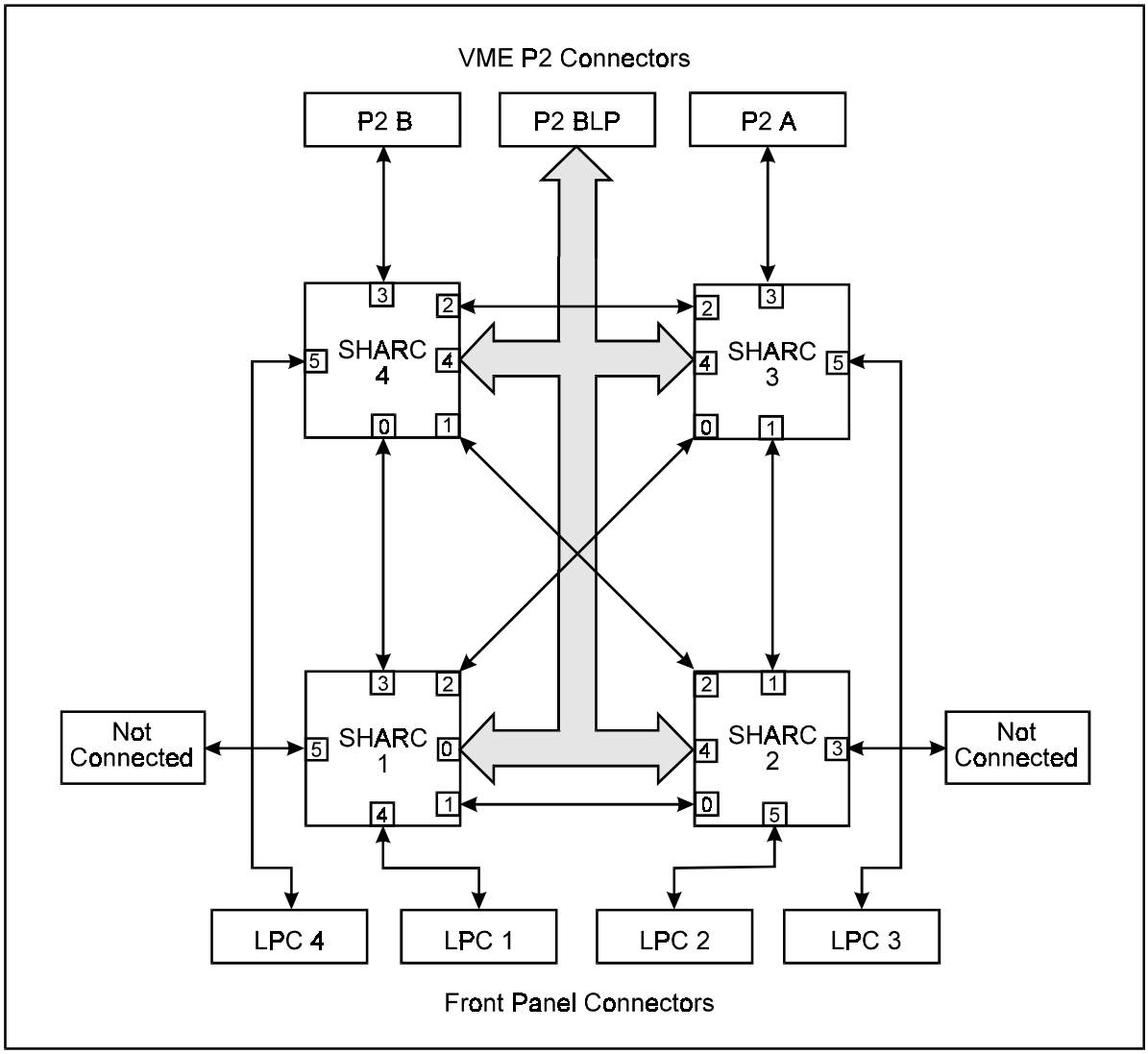
Figure 7.1: Link Port Routing - Six SHARC Variants



Key		
BLP	P2	LPC
Broadcast Link Port	VME P2 Connector	Link Port Connector

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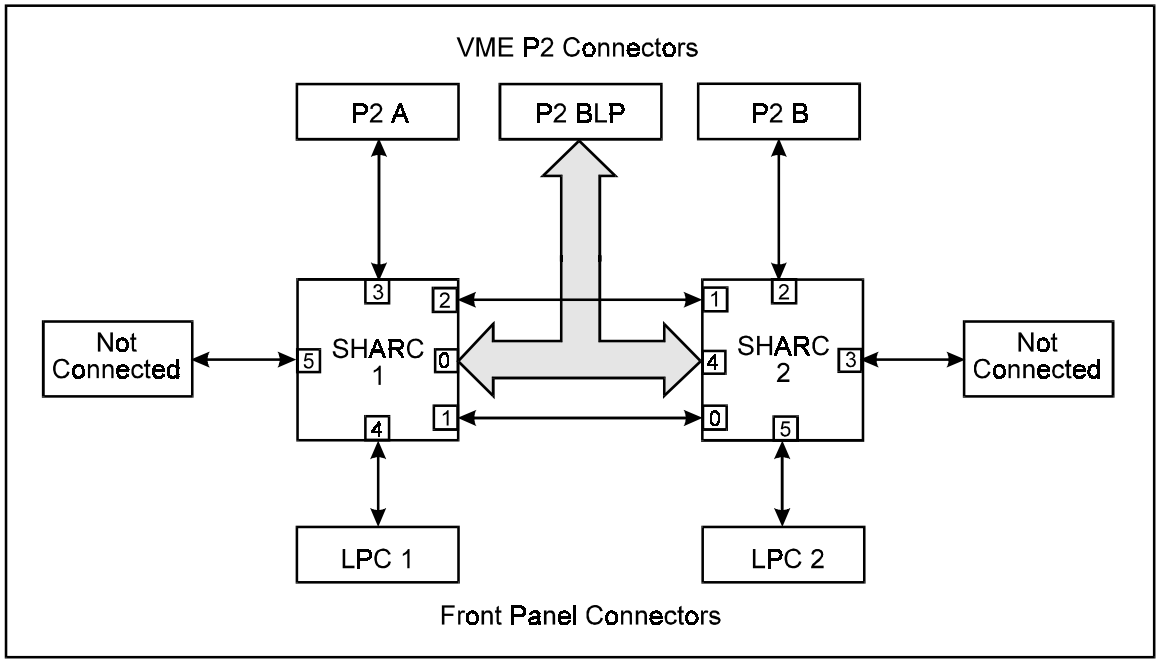
Figure 7.2: Link Port Routing - Four SHARC Variants



Key		
BLP	P2	LPC
Broadcast Link Port	VME P2 Connector	Link Port Connector

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Figure 7.3: Link Port Routing - Two SHARC Variants



Key		
BLP	P2	LPC
Broadcast Link Port	VME P2 Connector	Link Port Connector

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7.3 Broadcast Link Port

DBV66 provides a Broadcast Link Port (BLP), formed by connecting link port 0 from SHARC 1 to link port 4 of the other SHARCs.

The BLP provides the SHARCs with the following broadcast capabilities which are independent of the Interconnect bus:

- Each SHARC can broadcast data to all other SHARCs on the Interconnect bus by simply accessing the BLP as though it were a single port-port connection.
- By individually enabling and disabling the relevant link buffers the broadcast capability can be limited to selected SHARCs.
- The BLP is routed to user-defined pins on the VME P2 connector via bidirectional buffers. This allows the broadcast capability to be extended system wide.

When using the BLP, the DBV66 Peripheral Control Register must be correctly configured. This register is located at *0E00 0000h* in the SHARC memory map. The individual bit functions are described in Table 7.1 below. The use of the BLP is described in more detail in Section 7.3.1.

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Table 7.1: Peripheral Control Register

D31-D8	D7-D5	D4-D2	D1	D0
Not Used	**PMC_TEST**	**BLP_TRANS**	**BLP_DIR**	**BLP_OB**

Bit	Name	Function
0	BLP_OB	Broadcast Link Port off-board routing. '0' - BLP routed on-board only. '1' - BLP routed on-board and off-board via VME P2 connector.
1	BLP_DIR	Broadcast Link Port off-board direction. '0' - BLP input from another board. '1' - BLP output to another board. If the BLP is not routed off-board then the setting of this bit has no effect.
4-2	BLP_TRANS	Must be set to indicate which SHARC will be transmitting on the Broadcast Link Port. Only one SHARC can transmit on the BLP at any one time. The individual bit settings are given below. **Bit 4 Bit 3 Bit 2** 0 0 0 BLP input from another board. 0 0 1 SHARC 1 transmitting. 0 1 0 SHARC 2 transmitting. 0 1 1 SHARC 3 transmitting. 1 0 0 SHARC 4 transmitting. 1 0 1 SHARC 5 transmitting. 1 1 0 SHARC 6 transmitting. 1 1 1 Reserved. If less than six SHARCs are fitted to the board then the relevant bit settings are reserved.
7-5	PMC_TEST	Used to initiate a test for PMC modules in Sites 1 and 2. If these bits are set to '110' then bits 0 and 1 in the Peripheral Status Register (PMC1 and PMC2) can be read to determine if a PMC is present in Sites 1 and 2 respectively. This bit setting also enables access to the PMC modules from the PCI bus. If these bits are set to '111' then a PMC test is initiated as described above but access to the PMC modules is disabled. If these bits are set to '000' (default) then the PMC modules are disabled. They will not be accessible from the PCI bus unless the value '110' is later written to the same bits. All other bit settings are reserved.

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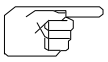
7.3.1 Using the Broadcast Link Port

The following step by step instructions illustrate how to use the DBV66 BLP.

Step 1 Configure Link Buffers

Configure the SHARC link buffers as described in Chapter 9 of the SHARC User's Manual. This process will involve the following in order:

- Ensuring the buffers are disabled.
- Assigning link buffers to the link ports connected to the BLP.
- Setting the direction of the link buffers to receive or transmit



Remember that link port 0 from SHARC 1 and link port 4 from the other SHARCs are connected to the BLP.

Section 7.5 outlines the SHARC registers which must be configured to achieve this.

Step 2 Configure the Peripheral Control Register

Bits 4 to 2 (BLP_TRANS) of the Peripheral Control Register must be configured to reflect which SHARC will be transmitting data. Note the following when configuring this register:

- Only a single SHARC can transmit data on the BLP at any one time.
- If the BLP is to be routed off-board then bits 0 and 1 (BLP_OB and BLP_DIR) must be set up.
- If the BLP is to be received from another board then bits 4 to 0 of the Peripheral Control Register must be set to '00001'.

Step 3 Enable Link Buffers and Transmit Data

The link buffers can now be enabled as appropriate and the transmitting SHARC can begin to transmit data. The configuration required to achieve this is described in the SHARC User's Manual.

Step 4 Changing Transmitter

If the transmitting SHARC needs to change then Steps 1 to 3 must be repeated.

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7.4 Front Panel Link Port Connectors

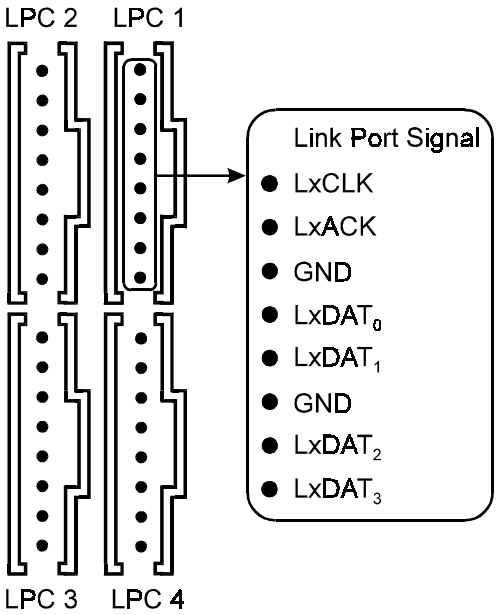
DBV66 provides up to four link port connectors (LPCs) on the front panel for six and four SHARC DBV66 variants and two connectors on two SHARC variants. These are routed as described below. Note that LPC 3 and LPC 4 are not connected on two SHARC DBV66 variants.

- LPC 1 is from SHARC 1, link port 4.
- LPC 2 is from SHARC 2, link port 5.
- LPC 3 is from SHARC 3, link port 5.
- LPC 4 is from SHARC 4, link port 5.

The pinout and orientation of the link port connectors on the front panel is illustrated in Figure 7.4 below.

To ensure reliable link port operation, the ribbon cable length must not exceed 30 cm. Suitable cables are available from LSI.

Figure 7.4: Link Port Connector Pinout and Orientation



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7.5 VME P2 Connector

On DBV66, two link ports are individually routed to user-defined pins on the VME P2 connector, depending on the number of SHARCs on the board. In addition to this, the BLP is available via P2. The pins to which the relevant signals are routed are provided in Table 7.2 below. Note that the SHARC link port indicated by P2 A and P2 B is dependent on the number of SHARCs fitted to DBV66 as described below:

- **Six SHARC DBV66**

  P2 A is from SHARC 5, link port 5.

  P2 B is from SHARC 6, link port 5.

- **Four SHARC DBV66**

  P2 A is from SHARC 3, link port 3.

  P2 B is from SHARC 4, link port 3.

- **Two SHARC DBV66**

  P2 A is from SHARC 1, link port 3.

  P2 B is from SHARC 2, link port 2.

Table 7.2: Link Port Pins on VME P2 Connector

SHARC Link Port	Link Port Signal	P2 Pin
P2 A	$LxDAT_0$	d4
	$LxDAT_1$	d5
	$LxDAT_2$	d6
	$LxDAT_3$	d7
	LxCLK	d1
	LxACK	d2
P2 B	$LxDAT_0$	d12
	$LxDAT_1$	d13
	$LxDAT_2$	d14
	$LxDAT_3$	d15
	LxCLK	d9
	LxACK	d10
P2 BLP	$LxDAT_0$	d19
	$LxDAT_1$	d20
	$LxDAT_2$	d21
	$LxDAT_3$	d22
	LxCLK	d16
	LxACK	d17

Note that pins d3, d8, d11, d18, d23 and d24 are grounded.

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7.6 Port to Port Communication

Data transfers over the SHARC link ports can be controlled from the following sources:

- The Core Processor of the SHARC.
- The DMA controller in the SHARC I/O Processor.
- Any host processor with access to the SHARC IOP registers.

All of these sources implement the link ports via registers in the SHARC I/O Processor. The following registers are associated with the link ports:

- The *Link Buffer Registers* (*LBUF0* to *LBUF5*). These registers provide access to the SHARC link buffers which can be individually assigned to the link ports. Data is written to/read from these registers to transmit/receive data over the link ports.
- The *Link Buffer Assignment Register* (*LAR*). This register is used to assign the link port buffers to the link ports.
- The *Link Buffer Control Register* (*LCTL*). This is the main control register for the link port buffers and includes bits to enable the buffer, configure its direction etc.
- The *Link Buffer Common Control Register* (*LCOM*). This register provides additional control/status for the link buffers. Bits in this register can be used to indicate the full/empty status of each buffer, clock the buffer at twice the SHARC frequency (to transmit 8 bits per cycle) etc.

All three methods of controlling data transfer over the link ports use at least the above three registers. Chapter 9 of the SHARC User's Manual provides additional details on these registers.

The following subsections outline the methods of controlling data transfer over the link ports.

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7.6.1 Core Processor Transfers

Consider two SHARCs, X and Y, where, for example, Port 0 of X is connected to Port 3 of Y. If SHARC X wishes to write to SHARC Y, X writes the block of memory to be transferred to Port X0's assigned link buffer in the SHARC memory map. This is transferred to Port Y3's input link buffer in the memory map. The block is then read by SHARC Y.

Bits in the SHARC *LCOM Register* can polled to determine the full/empty status of the link buffers. Alternatively, interrupts can be set up to indicate when the buffers are full/empty, see Section 9.6 of the SHARC User's Manual.

This process can function in the opposite direction allowing transfers to and from both SHARCs. One drawback with this method of block transfer is that the processor's operation is disrupted because the Core Processor has to read and store the memory blocks.

7.6.2 DMA Transfers

This system of memory block transfer is similar to Core Processor controlled transfer except that neither SHARC is disrupted because the reading and storing of memory is handled by a DMA controller in the I/O Processor rather than the Core Processor. This method is more complex to set up because of the number of registers that need to be configured. See Chapter 9 of the SHARC User's Manual for more information. Each SHARC has ten DMA channels, six of which are available for use by the link ports for transferring data. Therefore, if three ports on the one processor are connected to those on another, three times the data transfer speed of one port can be achieved, providing extremely fast inter-processor communication.

7.6.3 Host Processor Transfers

A host processor can access the registers associated with the link ports (outlined in Section 7.6) via the Interconnect bus. When accessing the link buffers in this way, the host can poll bits in the SHARC *LCOM Register* to determine the full/empty status of the link buffers.

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8 SHARC Serial Ports

8.1 Introduction

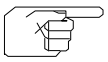
Each SHARC provides two independent synchronous serial ports, SPORT0 and SPORT1, for connection to a wide variety of peripherals. The main features of these ports are listed below.

- Compatible with big and little endian data formats.
- Data size selectable from 3 to 32 bits.
- Double buffering, both receive and transmit functions have an associated data buffer register.
- Serial clock and frame synchronisation signals can be generated internally or externally.
- Optional companding for CODEC applications.
- DMA controlled transfer or interrupt driven single word transfers.

For a full description of the SHARC serial ports, refer to Chapter 10 of the SHARC User's Manual.

8.2 SPORT Implementation on DBV66

On DBV66 both sets of serial ports (SPORT0 and SPORT1 from each SHARC) are tied together to form two individual Time Division Multiplexed (TDM) ports, TDM0 and TDM1. Each TDM port offers up to 32 channels and each SHARC can be configured to respond to individual channels.



Note that the SPORT Transmit Frame Sync (TFS) signal for the TDM port is not connected on DBV66. The Receive Frame Sync (RFS) signal is used for both receiving and transmitting.

Section 10.7 of the SHARC User's Manual provides general details on using the TDM ports. Section 8.3 of this TRM describes some example code provided to demonstrate the use of the TDM ports on DBV66.

The TDM ports are routed off-board via P2. The pins to which the relevant signals are routed are provided in Table 8.1 below.

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Table 8.1: SPORT TDM Pins on VME P2 Connector

Source	Signal	P2 pin
TDM0	DT0	z1
	TCLK0	z3
	DR0	z5
	RCLK0	z7
	RFS0	z9
TDM1	DT1	z23
	TCLK1	z25
	DR1	z27
	RCLK1	z29
	RFS1	z31
Source	Signal	P2 pin
TDM0	DT0	z1
	TCLK0	z3
	DR0	z5
	RCLK0	z7
	RFS0	z9
TDM1	DT1	z23
	TCLK1	z25

Note that all even numbered pins on row z are grounded.

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8.3 DBV66 TDM Port Example Code

Example code is provided with DBV66 to demonstrate the use of the TDM ports. This code is provided on the CD-ROM in the **dbv66trm** subdirectory under **hardware** as the file **serial.asm**. This assembler code transfers a block of sixteen 32 bit words from SPORT1 on one SHARC to SPORT0 of the same SHARC. It assumes that the following signals are connected on the DBV66 VME P2 connector:

- DT1 connected to DR0.
- DR1 connected to DT0.
- RFS1 connected to RFS0.
- TCKL1, TCLK0, RCKL1 and RCLK0 all interconnected.

Table 8.1 provides the actual VME P2 pins to which these signals are routed.

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9 Interrupts

9.1 Introduction

DBV66 provides a number of on-board interrupt sources. These are listed and outlined below:

- **Universe**

  The Universe incorporates an on-chip interrupt generator which can be employed by a number of internal sources to generate PCI bus and VMEbus interrupts. The Universe also routes interrupts between the PCI bus and the VMEbus. It additionally allows interrupt sources on DBV66 to be directly connected to it, independent of the PCI bus, which it then translates to VME interrupts.

- **PCI9060**

  The PCI9060 provides an on-chip interrupt generator which can be used by a number of internal sources to generate SHARC and PCI bus interrupts.

- **PMC Modules**

  A PMC module fitted to DBV66 can generate interrupts to the PCI bus.

- **ICEPAC**

  An ICEPAC module on DBV66 can generate an interrupt to the VMEbus. This interrupt can be implemented to control the DBV66 JTAG circuitry.

- **RS-232**

  The RS-232 serial port can generate interrupts to both the SHARCs and the VMEbus.

Note that the internal interrupt sources in the Universe and PCI9060 devices each include a software source. This software source is available to any device with access to the internal registers of the Universe or PCI9060. The Universe software source can be used to interrupt both the PCI bus and the VMEbus and the PCI9060 source can be used to interrupt the SHARCs and PCI bus.

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Figure 9.1 illustrates the DBV66 interrupt sources and the way in which interrupts are routed across the board. This diagram illustrates the three buses associated with DBV66 interrupts, the Interconnect bus, the PCI bus and the VMEbus. The interrupt lines provided by the three buses are outlined below:

- **Interconnect bus**

  The /IRQ0 maskable interrupt pin from each SHARC are interconnected to form an interrupt line on the Interconnect bus. The /IRQ1 interrupt pins are similarly connected to form another interrupt line. Any interrupt generated on one of these lines is routed to all SHARCs on the Interconnect bus.

- **PCI Bus**

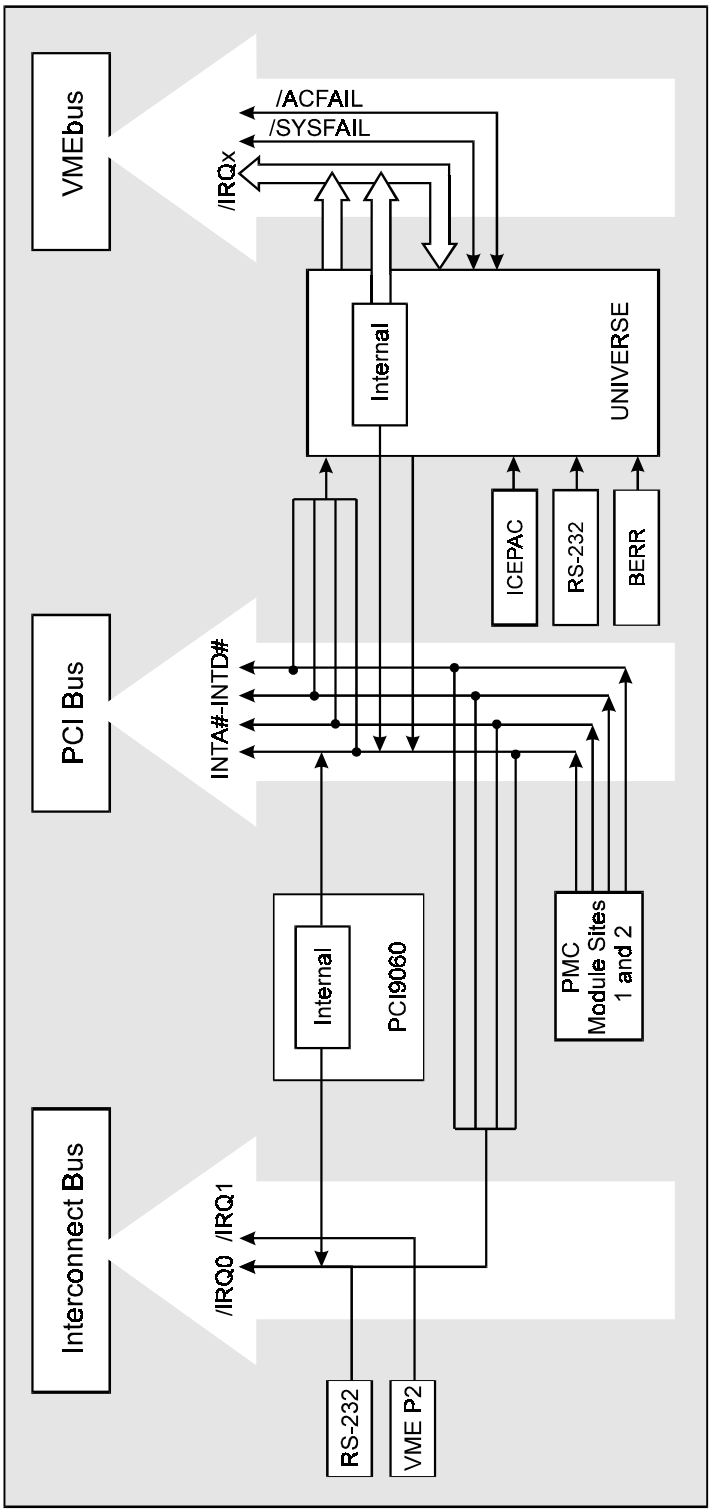
  The DBV66 PCI bus provides all four PCI interrupt lines INTA# to INTD#. Note that the PMC modules cannot receive interrupts from these lines.

- **VMEbus**

  The VMEbus provides seven priority interrupt lines, /IRQ1 to /IRQ7. It also provides two failure indication lines, /SYSFAIL and /ACFAIL.

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Figure 9.1: DBV66 Interrupt Lines



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9.2 Universe Interrupts Overview

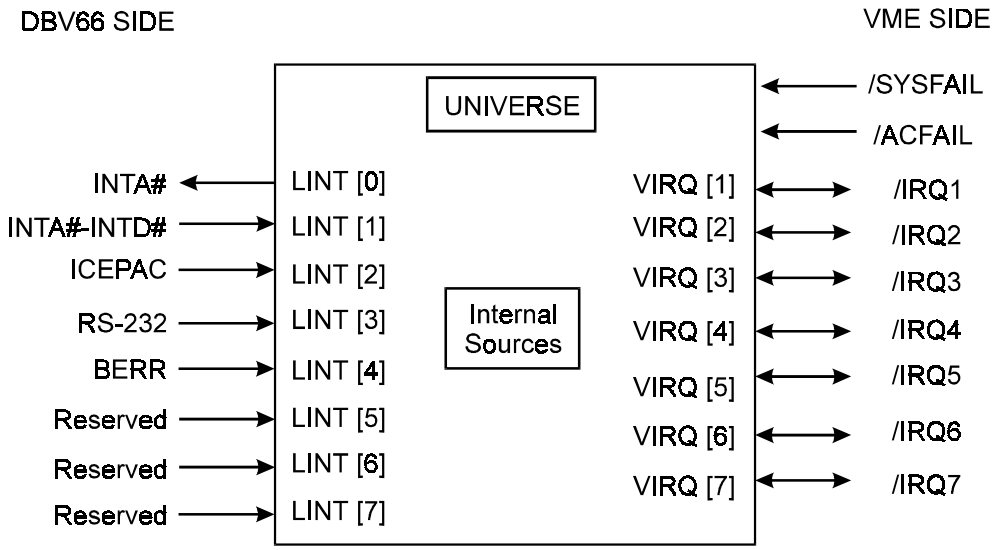
This section provides an overview of how the Universe maps interrupts between DBV66 and the VME interrupt lines. It also outlines how interrupts are routed from the internal interrupt generator to the PCI and VME interrupt lines.

The Universe provides a number of pins for generating and receiving interrupts. These pins can be grouped into two sets. The first set of pins is connected to the VMEbus and the second set is connected to interrupt lines on DBV66. The pins connected to the VMEbus are referred to as being on the 'VME side', those connected to DBV66 are referred to as the 'DBV66 side', see Figure 9.2 below.

On the VME side of the Universe, there are seven pins, named VIRQ [1] to VIRQ [7], which are directly connected to VME interrupt lines /IRQ1 to /IRQ7. These pins can be individually used as either inputs or outputs. There are two further pins for receiving the VME SYSFAIL and ACFAIL signals.

On the DBV66 side there are eight pins, named LINT [0] to LINT [7], which are connected to various interrupt lines on DBV66.

Figure 9.2: Universe Interrupt Sources



An interrupt input on any of the VIRQ [1] to [7] pins can be individually enabled/disabled and mapped in software to any or all the LINT [0] to LINT [1] pins and vice versa.

Also, the internal interrupt sources can be individually enabled and mapped to any of VIRQ [1] to [7] or LINT [0] to LINT [1], although some internal interrupts can only be mapped to either the VME or DBV66 side.

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Section 9.3 and 9.4 of this TRM provide DBV66-specific details on Universe interrupts to the VMEbus and PCI bus respectively. Refer to Section 2.7 of the Universe User's Manual for full details on Universe interrupt handling.

Care must be taken when enabling and mapping interrupts between the VIRQ and LINT pins. DBV66 may be damaged if any LINT pin other than LINT [0] is made an output.

9.3 Universe Interrupts to the VMEbus

Interrupts can be generated to the VMEbus via the Universe LINT pins or via the on-chip interrupt generator.

Each interrupt source can be individually enabled/disabled, monitored and routed to any or all of the VME interrupt lines. This configuration is performed in software using the Universe VINT_EN, VINT_STAT, VINT_MAP0, and VINT_MAP1 Registers. Refer to Section 2.3.6 of the Universe User Manual for further details.

9.3.1 LINT Interrupts

The Universe LINT [1] to LINT [4] pins are implemented as inputs on DBV66 and are connected as listed below. Note that LINT [0] is implemented as an output as described in Section 9.4 and LINT [5] to LINT [7] are reserved.

- LINT [1] is connected to PCI interrupt lines INTA# to INTD#. Interrupts can be generated on INTA# by the SHARCs via the PCI9060 device as described in Section 9.5.2. PMC modules may also be provided with the facility to generate PCI interrupts, refer to the PMC module documentation to determine this.
- LINT [2] is connected to the ICEPAC interrupt source. This interrupt can be used to control the DBV66 JTAG circuitry.
- LINT [3] is connected to the UART INTRN interrupt pin and is used to route interrupts between the RS-232 port and the VMEbus. Interrupts on this pin can be generated by the UART on a number of conditions. For further details on the UART device, refer to the UART Product Specification.
- LINT [4] is connected to decode circuitry on DBV66 which generates an interrupt whenever a VME access to invalid Interconnect bus memory is made. This interrupt is referred to as the BERR interrupt.

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9.3.2 Internal Interrupts

Internal Universe interrupts can be generated to the VMEbus from the on-chip DMA controller or on a PCI or VME error condition. These internal interrupt sources are discussed in the Universe User Manual. In addition to the internal interrupt sources outlined above, the Universe includes a VME software interrupt facility. The use of this facility is described below.

A software interrupt to the VMEbus can be generated by changing the status of the SW_INT bit in the Universe VINT_EN Register from ‘0’ to ‘1’. This bit should then be set to '0' before another VME interrupt can be generated. Note that setting this bit to '0' clears the VME interrupt.

The VME interrupt level on which the interrupt is generated is configured via the SW_INT field (bits 18-16) in the Universe VINT_MAP1 register. The Universe provides support for a single 8 bit Status/ID vector for all interrupt levels. Bits 7-1 of this vector can be set by writing to the STATID field (bits 31-25) in the Universe STATID Register. Bit 0 of the vector is automatically set to ‘0’ when a software interrupt is being generated.

The relevant Universe register bits used for generating software interrupts to the VMEbus are described in Table 9.1 below.

Table 9.1: Universe VME Software Interrupt Registers

Register	Bits	Description
VINT_MAP1	18-16 (SW_INT)	Used to set the VMEbus interrupt level. **Bit 18 / Bit 17 / Bit 16 / Interrupt Level** 0 / 0 / 0 / No Interrupt 0 / 0 / 1 / /IRQ1 0 / 1 / 0 / /IRQ2 0 / 1 / 1 / /IRQ3 1 / 0 / 0 / /IRQ4 1 / 0 / 1 / /IRQ5 1 / 1 / 0 / /IRQ6 1 / 1 / 1 / /IRQ7
VINT_EN	12 (SW_INT)	Used to initiate the VME interrupt. Changing the status of this bit from ‘0’ to ‘1’ generates a VME interrupt.
STATID	31-24	These bits are used to provide the Status/ID vector. Bit 24 is automatically set to ‘0’ for software interrupts, see Section 9.3.3.

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9.3.3 Output Status/ID Vector

When DBV66 generates a VME interrupt the appropriate interrupt handler on the VMEbus generates a corresponding VME IACK cycle. Upon receipt of this IACK cycle, the Universe provides an 8 bit Status/ID vector on VME lines VDATA7 to VDATA0.

The most significant 7 bits of this Status/ID vector are user-defined and must be written to bits 32-25 of the Universe STATID Register before the interrupt is generated. The least significant bit of the Status/ID vector (bit 24 of STATID) is automatically set by the Universe when the interrupt is generated. If the interrupt source is the internal software interrupt then the bit is set to ‘0’. The bit is set to ‘1’ otherwise.

9.3.4 Clearing VME Interrupts

The Universe internal software interrupt is automatically cleared upon receipt of a corresponding IACK cycle. However, all other interrupts to the VMEbus must be cleared by writing a ‘1’ to the relevant bit in the Universe VINT_STAT Register once the VME IACK cycle has been received. The Universe internal interrupt generator can be configured to generate an interrupt to the PCI bus when the IACK cycle is received, see Section 2.7.3.1 of the Universe User's Manual.

Writing a '1' to the relevant bit in VINT_STAT clears the bit to ‘0’. Table 9.2 below indicates which bit in VINT_STAT corresponds to each interrupt source.

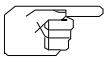
Table 9.2: VINT_STAT Bits

VINT_STAT Bit	Interrupt Source
7-0	LINT [7] - LINT [0]
8	DMA
9	LERR
10	VERR
11	Reserved
12	Software
31-12	Reserved

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9.4 Universe Interrupts to the PCI Bus

The Universe can be configured to monitor any or all of the VME interrupt lines. Interrupts received on these lines can be routed to the PCI bus along with a number of Universe internal interrupts.



All interrupts targeted at the PCI bus must be mapped to the Universe LINT [0] pin which is connected to the PCI INTA# interrupt line.

Each interrupt source can be individually enabled/disabled and monitored. This configuration is performed in software using the Universe LINT_EN and LINT_STAT Registers. The LINT_MAP0 and LINT_MAP1 Registers must be configured to map the appropriate interrupt source to the LINT [0] pin. Refer to Section 2.3.6 of the Universe User Manual for further details.

9.4.1 VME Interrupts

The Universe can be configured to monitor the VME interrupt lines by simply enabling interrupts on the appropriate VIRQ pin. These interrupts can be mapped to PCI interrupt line INTA# which is connected to LINT [0]. INTA# interrupts are routed to the /IRQ0 interrupt line on the Interconnect bus.

Upon receipt of a VME interrupt the Universe automatically generates an IACK cycle on the appropriate level. The 8 bit Status/ID vector returned is written to bits 7-0 of appropriate Universe VIRQ Status/ID Register (V1_STATID to V7_STATID for interrupts on /IRQ1 to /IRQ7 respectively).

All VME interrupts must be routed to the same PCI interrupt line, INTA#. If the Universe is configured to monitor more than one interrupt line then the level on which the interrupt was received can be determined by reading the Universe LINT_STAT Register. If any of bits 7-1 of this register read ‘1’ then a VME interrupt has been received on the corresponding level and the Status/ID vector written to the appropriate Vx_STATID Register.

Note that the Universe will not generate further IACK cycles on a level on which an interrupt has been received until the appropriate bit in LINT_STAT has been set to ‘0’ by writing a '1' to the bit.

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9.4.2 Internal Interrupts

Internal Universe interrupts can be generated to the PCI bus from the on-chip DMA controller, on a PCI or VME error condition, on receipt of VME ownership or when an IACK cycle is serviced on the VMEbus. These internal interrupt sources are discussed in the Universe User Manual.

In addition to the internal interrupt sources listed above, the Universe includes a PCI software interrupt facility. The use of this facility is described below.

A software interrupt to the PCI bus can be generated by changing the status of the SW_INT bit in the Universe LINT_EN Register from '0' to '1'. The SW_INT field in the Universe LINT_MAP1 register must be set to '001' to map the software interrupt to the LINT [0] pin.

The relevant Universe register bits used for generating software interrupts to the PCI bus are described in Table 9.3 below.

Table 9.3: Universe PCI Software Interrupt Registers

Register	Bits	Description
LINT_MAP1	22-20 (SW_INT)	Used to map the software interrupt to the PCI bus. These bits must be set to '000' on DBV66 to map the software interrupt to LINT [0].
LINT_EN	13 (SW_INT)	Used to initiate the PCI interrupt. Changing the status of this bit from '0' to '1' generates a PCI interrupt.

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9.5 PCI9060 Interrupts

The PCI9060 device incorporates an on-chip interrupt generator. This can be used by a number of internal sources to interrupt the SHARCs or the PCI bus. The internal interrupt sources available are described in the following subsections.

9.5.1 PCI9060 to SHARC Interrupts

A number of internal PCI9060 interrupts are routed to the SHARC /IRQ0 line as outlined below. For full details on these interrupt sources, refer to Section 3.10 of the PCI9060 data sheet.

- **PCI to SHARC doorbell**

  Interrupts are generated to the SHARCs by writing a ‘1’ to any bit in the PCI9060 PCI to Local Doorbell Register from the PCI bus. This interrupt can be subsequently cleared by writing a ‘0’ to the same bit from the SHARCs.

- **DMA completion**

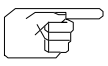
  The PCI9060 incorporates a two channel DMA controller. These can be configured to generate SHARC interrupts on completion of a transfer.

- **Built In Self Test (BIST) request**

  The Interconnect bus supports the PCI BIST functionality. If a ‘1’ is written to bit 6 of the PCI9060 BIST Register to request a BIST then an interrupt is generated to the SHARCs. Note that the BIST request interrupt is used to indicate to the SHARCs that they should perform some user-defined test. If this test is passed then the SHARCs should set bit 6 of the PCI9060 BIST Register to '0'.

- **PCI serious error**

  If the PCI SERR# line becomes active then an interrupt is generated to the SHARCs via the PCI9060.



The DBV66 Interrupt Status Register can be read to determine the source of an interrupt to the SHARCs on /IRQ0. Refer to Section 9.7 for further details.

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9.5.2 PCI9060 to PCI Bus Interrupts

Two internal PCI9060 interrupts are routed to the PCI INTA# line as outlined below. For full details on these interrupt sources, refer to Section 3.10 of the PCI9060 data sheet.

- **SHARC to PCI doorbell**

  Interrupts are generated to the PCI bus on INTA# (which can then be routed to the VMEbus via the Universe) by writing a '1' to any bit in the PCI9060 Local to PCI Doorbell Register from the SHARCs. This interrupt can be subsequently cleared by writing a '0' to the same bit from the PCI bus.

- **Master/Target Abort**

  The PCI9060 can be configured to generate a PCI interrupt on INTA# (which can then be routed to the VMEbus via the Universe) upon receipt of a master/target abort condition.

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9.6 Additional SHARC Interrupts

The following interrupts to the SHARCs are available in addition to the PCI9060 interrupts described in Section 9.5.1.

- **SHARC-SHARC interrupts**

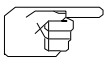
  The SHARCs can interrupt each other using the SHARC IOP *VIRPT Register*. By writing the address of the required interrupt service routine to this register a high priority interrupt is generated, see Section 8.7 of the SHARC User's Manual.

- **Direct PCI to SHARC interrupts**

  The PCI interrupt lines, INTA# to INTD#, are combined together and connected to the SHARC /IRQ0 line. An interrupt on any of these lines will therefore generate a SHARC interrupt independent of the PCI9060 device. The DBV66 Interrupt Status Register and the SHARC FLAG3 line can be used to determine the source of an interrupt to the SHARCs on /IRQ0. Refer to Section 9.7 and Section 9.8 for further details.

- **RS-232 to SHARC interrupts**

  An interrupt generated by the UART device, used to implement the RS-232 serial port will generate a SHARC interrupt on /IRQ0. The DBV66 Interrupt Status Register and the SHARC FLAG3 line can be used to determine the source of an interrupt to the SHARCs on /IRQ0. Refer to Section 9.7 and 9.8 for further details.

  RS-232 interrupts are routed to both the SHARC /IRQ0 line and the Universe LINT [4] pin. Only one device must handle the interrupts at any one time.

- **VME P2 to SHARC interrupts**

  The SHARCs can be interrupted on /IRQ1 from a peripheral device via the VME P2 connector. Pin z21 of the P2 connector is used for this purpose. The SHARC can be configured to respond to either level or edge-triggered interrupts using the SHARC Core *MODE2 Register*.

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9.7 DBV66 Interrupt Status Register

The DBV66 Interrupt Status Register is located at *0E00 0002h* in the SHARC memory map and can be read to determine the source of an /IRQ0 interrupt. The individual bit functions are described in Table 9.4 below.

Interrupts can be generated on the SHARC /IRQ0 interrupt line from the PCI INTA# to INTD# interrupt lines, the RS-232 port and the PCI9060 device. Upon receipt of an /IRQ0 interrupt this register can be read to determine which of these is the interrupt source.

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Table 9.4: DBV66 Interrupt Status Register

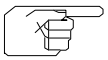
D31-D8	D7	D6	D5	D4	D3	D2	D1	D0
Not Used	**DRAM66**	**LINTo#**	**RS232**	**LSERR#**	**INTD#**	**INTC#**	**INTB#**	**INTA#**

Bit	Name	Function
0	INTA#	Indicates the status of the PCI INTA# interrupt line. ‘1’ - INTA# active. ‘0’ - INTA# not active.
1	INTB#	Indicates the status of the PCI INTB# interrupt line. ‘1’ - INTB# active. ‘0’ - INTB# not active.
2	INTC#	Indicates the status of the PCI INTC# interrupt line. ‘1’ - INTC# active. ‘0’ - INTC# not active.
3	INTD#	Indicates the status of the PCI INTD# interrupt line. ‘1’ - INTD# active. ‘0’ - INTD# not active.
4	LSERR#	Indicates the status of the PCI9060 LSERR# interrupt. ‘1’ - LSERR# interrupt active. ‘0’ - LSERR# interrupt not active. Note that the PCI9060 generates an LSERR# interrupt on a master/target abort or if a PCI parity error occurs. Refer to the PCI9060 data sheet for further details.
5	RS232	Indicates the status of the RS-232 interrupt from the UART device. ‘1’ - RS-232 interrupt active. ‘0’ - RS-232 interrupt not active.
6	LINTo#	Indicates the status of the PCI9060 LINTo# interrupt. ‘1’ - PCI9060 LINTo# interrupt active. ‘0’ - PCI9060 LINTo# interrupt not active. Note that a number of internal PCI9060 sources generate LINTo# interrupts, including the internal PCI to Local Doorbell Register. Refer to the PCI9060 data sheet for further details.
7	DRAM66	Used to indicate the presence of a DRAM66 module. '0' - No DRAM66 module fitted to DBV66. '1' - DRAM66 module fitted to DBV66.

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9.8 SHARC /IRQ0 Interrupt Source Determination

Interrupts to the SHARC /IRQ0 line can be generated via the PCI interrupt lines and the UART device. The PCI interrupt sources are the PMC modules, Universe or PCI9060. In order reduce the time required to determine the source of /IRQ0 interrupts to the SHARCs, the following mechanism is implemented.



This section assumes that Universe interrupts to INTA# are enabled and any PMC modules fitted to DBV66 are capable of generating PCI interrupts. If either of these assumptions are not true then the relevant device can be ignored when determining the /IRQ0 interrupt source.

The FLAG3 line of the SHARCs can be used to determine if an interrupt has been generated by either the UART device, PCI9060 or a different source.

- When configured as an input, the FLAG3 line of each SHARC is set to ‘0’ when either the PMC or Universe generate a PCI interrupt.
- The FLAG3 line is set to ‘1’ when a PCI9060 or RS-232 interrupt is generated to the SHARCs.

If the FLAG3 line is set to ‘0’, then the interrupt source can be determined as follows.

- The Universe LINT_STAT Register can be read to determine if a PCI interrupt has been generated by the Universe.
- If the Universe has not generated an INTA# interrupt then the PMC modules can be interrogated in turn to determine which has generated the PCI interrupt. The documentation accompanying the PMC module should describe how interrupts are implemented.

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9.9 Interrupt Tutorials

This section provides step by step tutorials to demonstrate how to configure and generate interrupts between the SHARCs and the VMEbus.

9.9.1 SHARC to VME Interrupt Tutorial

This tutorial demonstrates how the SHARCs can generate VME interrupts via the internal software source of the Universe. This tutorial assumes that VME /IRQ1 and a Status/ID vector of DCh are used.

Step 1 Map Universe VME software source to VME line

Set bits 18-16 (SW_INT) of the Universe VINT_MAP1 Register to '001'. This maps the Universe internal software interrupt to the VIRQ [1] pin.

Step 2 Configure Universe Status/ID vector

Set bits 31-25 of the Universe STATID Register to '1101110'. Since the Universe automatically sets bit 24 to '0' for software interrupts, this configures the Status/ID vector to DCh.

Step 3 Generate interrupt

In order to generate a VME interrupt, change the status of bit 12 (SW_INT) of the Universe VINT_EN Register from ‘0’ to ‘1’.

Step 4 IACK

The Universe can be configured to generate an interrupt to PCI interrupt line INTA# when it detects a VME IACK cycle corresponding to /IRQ1. The following steps must be followed to achieve this:

- ❑ Set bit 12 (SW_IACK) of the LINT_EN Register to '1' to enable IACK interrupts.
- ❑ Set bits 18-16 (SW_IACK) of the LINT_MAP1 Register to '000'. This maps IACK interrupts on the Universe LINT [0] pin, which is in turn attached to the PCI INTA# interrupt line.

Alternatively, bit 12 (SW_IACK) of the LINT_STAT Register can be polled. If this bit reads '1' then an IACK interrupt condition has occurred.

Once the IACK has been detected, bit 12 (SW_INT) of the Universe VINT_EN Register can be set to ‘0’ to clear the VME interrupt.

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9.9.2 VME to SHARC Interrupt Tutorial

This tutorial demonstrates how to use DBV66 to monitor VME interrupts and to route these interrupts to the SHARCs. VME interrupt level /IRQ2 is used as an example.

Step 1 Enable /IRQ0 on selected SHARCs

VME interrupts are routed to the SHARC /IRQ0 interrupt line of all processors on the Interconnect bus, along with interrupts from a number of other sources. Bit 8 (IRQ0I) of the Core *IMASK Register* of each SHARC to be interrupted should be set to '1' to enable interrupts on /IRQ0.

Step 2 Map VME line to LINT [0]

The Universe VIRQx [2] pin must be mapped to the LINT [0] pin by setting bits 10-8 (VIRQ2) of the Universe LINT_MAP0 Register to '000'.

Step 3 Enable VME line

Once the VME line has been mapped to LINT [0], bit 2 (VIRQ2) of the Universe LINT_EN Register must be set to '1' to enable the VIRQ [2] pin. Once the VIRQ [2] pin has been enabled, any VME interrupts received on /IRQ2 are routed to the PCI INTA# interrupt line. Interrupts on INTA# then generate interrupts on the SHARC /IRQ0 interrupt line.

Upon receipt of a VME interrupt, the Universe automatically generates an IACK cycle of the corresponding level. Upon receipt of this cycle the interrupting device places an 8 bit Status/ID on VME lines VDATA7 to VDATA1. The Universe automatically places this Status/ID vector for /IRQ2 interrupts in bits 7-0 of the V2STATID Register. Bit 2 (VIRQ2) in the Universe LINT_STAT Register is then set to ‘1’. This indicates that a VME interrupt has been received on the VME /IRQ2 line and a Status/ID vector is available.

Step 4 Determine interrupt source

Upon receipt of an interrupt on /IRQ0, the SHARC can read the Interrupt Status Register to determine the interrupt source. If bit 0 (INTA#) of this register reads ‘1’ then a PCI interrupt on INTA# has been received.

INTA# interrupts on DBV66 can be generated from a number of sources. In order to determine whether or not a VME interrupt has been received, read the Universe LINT_STAT Register. If bit 2 (VIRQ2) reads ‘1’ then a VME interrupt has been received on the VME /IRQ2 line.

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Step 5 Read Status/ID vector

Upon receipt of an /IRQ2 VME interrupt, the user-defined SHARC /IRQ0 interrupt service routine must read the relevant Universe V2STATID Register to determine the interrupt condition and must then service the interrupt.

Step 6 Re-enable interrupts

Once the V2_STATID Register has been read, bit 2 (LINT2) of the VINT_STAT Register must be cleared to '0' to re-enable VME interrupts on /IRQ2.

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10 JTAG Emulation System

10.1 Introduction

The IEEE 1149.1 JTAG test access port of the SHARC provides a method of non-intrusive debug. DBV66 provides a JTAG scan chain which is routed to all SHARCs on the Interconnect bus. The chain can be extended to individually include the PMC sites using hardware links on DBV66.

DBV66 provides connectors for Analog Devices' EZ-ICE and ICEPAC systems which can be used as JTAG controllers. The EZ-ICE system consists of an ISA bus board which is located in a PC and connected to DBV66 via ribbon cabling. The emulation software then runs on the PC host.

The ICEPAC system provides the same functionality as the EZ-ICE. However, the ICEPAC hardware consists of a small module which is located on DBV66. The emulation software then runs on the VME host.

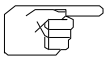
The EZ-ICE and ICEPAC systems are available from LSI. Please contact your local distributor for more details.

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10.2 ICEPAC/EZ-ICE Connectors

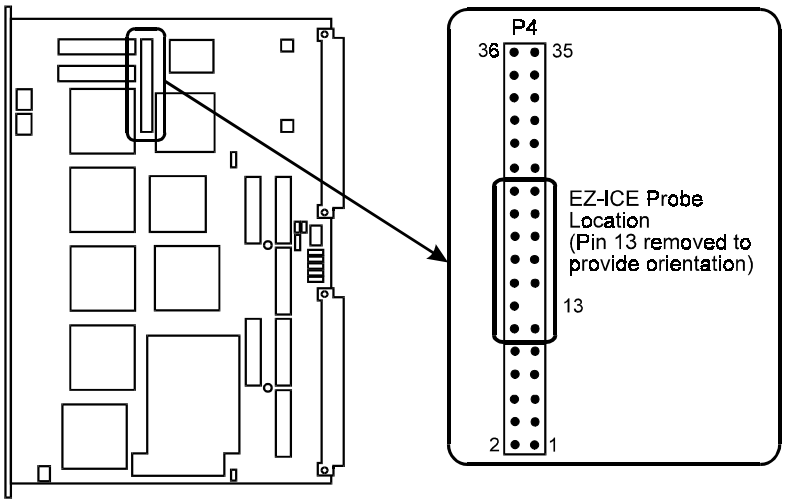
The ICEPAC module site consists of three connectors. There are two 4 pin connectors, labelled P5 and P6 on the board, and one 36 pin connector, labelled P4. The location of these connectors is indicated in Figure 2.1. If an EZ-ICE system is used instead of an ICEPAC then a subset of the pins on the 36 pin connector are used to accept the EZ-ICE probe.

Figure 10.1 below indicates which pins on the 36 pin connector accept the EZ-ICE probe. Note that there is no need to insert any jumpers across P4 whether or not an EZ-ICE system is in use.



When using an EZ-ICE system with DBV66, the system's target probe must be Revision 2.1 or later. Earlier revisions of the probe will cause an error at emulator initialisation of type 'No JTAG devices detected'. Please contact Analog Devices for information on probe upgrades.

Figure 10.1: EZ-ICE Probe Pins



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10.3 JTAG Routing

The JTAG scan chain is routed through all SHARCs (SHARC1 first then in order through the remaining SHARCs) and optionally to the PMC modules. The routing of the scan chain to the PMC modules is configured using hardware link LK12 for Site 1 and LK13 for Site 2, see Figure 10.2 below.

Figure 10.3 indicates the routing of the JTAG Test Data Input (TDI) and Test Data Output (TDO) signals. Note that although TDI is first routed to SHARC 1, JTAG views it as the last processor on the JTAG chain.

Figure 10.2: JTAG PMC Bypass Links - LK12 and LK13

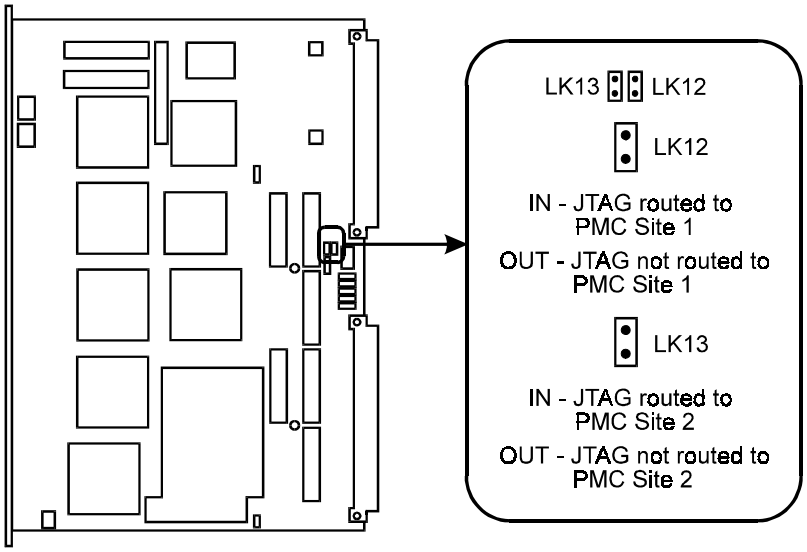
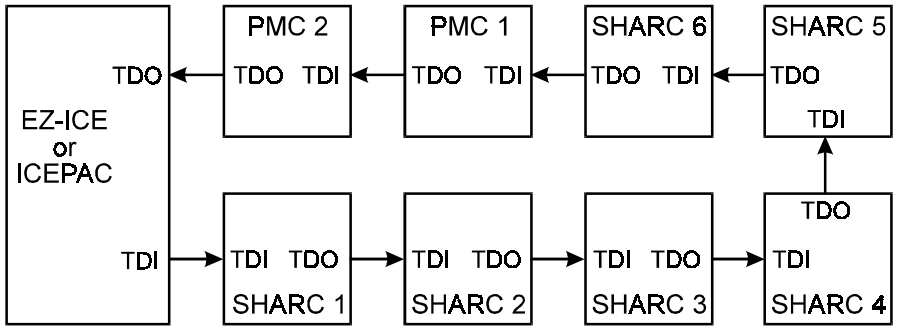


Figure 10.3: JTAG TDI/TDO Routing



If less than six SHARCs are fitted to DBV66 then the corresponding processors are bypassed. The routing of the JTAG chain to the PMC sites is configured via hardware link, see Figure 10.2 above.

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11 Reset Sources

There are a number of possible reset sources for DBV66:

- VMEbus system reset pin, /SYSRESET.
- Front panel reset switch.
- Software reset bits in the PCI9060.
- Software reset bits in the Universe.
- Software reset bits in the SHARCs.

Each of these reset sources is discussed in the sections below.

11.1 /SYSRESET

Whenever the host system is powered up, the VMEbus /SYSRESET pin is asserted. This resets the whole host system. This includes resetting all SHARCs, clearing all the DBV66 registers to their default state and resetting all the PCI9060 and Universe internal registers on all DBV66 boards in the system. If any PMC modules are located on the board then they will also be reset.

11.2 Reset Switch

The reset switch on the front panel is a useful debug feature. Toggling this switch will reset and release the DBV66 board, without having to reboot the whole host system. This resets all the SHARCs and clears the DBV66 registers to their default state. The reset switch also resets all Universe and PCI9060 internal registers.

Note that if DBV66 is configured as the Slot 1 system controller (see Section 6.4), the reset switch will assert the VME /SYSRESET line.

11.3 Universe Software Reset Sources

There are two software reset sources available in the Universe. The SW_SRST bit in the MISC_CTL Register can be used to reset the entire VME system via /SYSRESET. The SW_LRST bit in the MISC_CTL Register can be used to reset all devices on the PCI bus with the exception of the Universe. Note that the SW_SRST bit should not be used by VME masters and the SW_LRST bit should not be used by PCI masters. Refer to Section 2.10 of the Universe User Manual for further details.

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11.4 PCI9060 Software Reset Source

The entire Interconnect bus can be reset in software using a register in the PCI9060 device. Bit 30 of the EEPROM Control, PCI Command Codes, User I/O Control, Init Control Register is used for this purpose. Toggling this bit from ‘0’ to ‘1’ to ‘0’ from the PCI bus resets all SHARCs, the DBV66 control/status registers, the ICEPAC registers and the PCI9060 Shared Runtime and Local DMA Registers.

Refer to the PCI9060 data sheet for further details.

11.5 Individual SHARC Reset

Each SHARC processor on the Interconnect bus can be individually reset by setting bit 0 (*SRST*) in the SHARC IOP *SYSCON Register* to ‘1’ and then clearing it to ‘0’. Since the *SYSCON Register* is one of the SHARC I/O Processor registers, it can be accessed by any device with access to the Interconnect bus. All six SHARCs can be simultaneously reset by writing to the *SYSCON Register* at *0038 0000h* in the broadcast write space.

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12 Additional Debug Features

This chapter describes each of the features provided on DBV66, in addition to the JTAG circuitry, which are provided for software debug purposes.

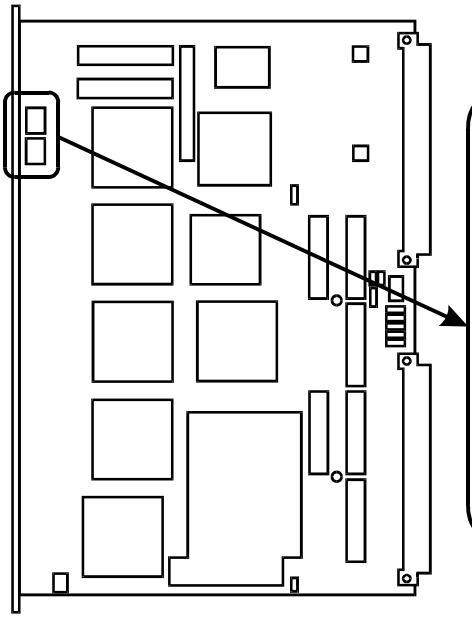
12.1 FLAG1 and FLAG2 Headers

There are two 9-pin headers on DBV66 which provide access to the FLAG1 and FLAG2 pins of each SHARC. The function of these pins is user-defined. Each pin can be individually configured as an input or an output using the SHARC Core *MODE2 Register*. The SHARC Core *ASTAT Register* can be used to monitor the status of an input pin and control the status of an output pin.

The FLAG1 and FLAG2 connectors are routed directly to the SHARCs without any protection circuitry. Care should therefore be taken when using these connectors.

Figure 12.1 below indicates the location and pinout of the FLAG1 and FLAG2 connectors.

Figure 12.1: FLAG1 and FLAG2 Location and Pinout



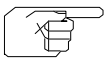
Pin	Signal
1	SHARC 1 FLAG 1/2
2	SHARC 2 FLAG 1/2
3	GND
4	GND
5	SHARC 3 FLAG 1/2
6	SHARC 4 FLAG 1/2
7	GND
8	Removed
9	SHARC 5 FLAG 1/2
10	SHARC 6 FLAG 1/2

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12.2 PCI Bus Error Status

DBV66 provides two methods of monitoring PCI bus errors. Two bits the DBV66 Peripheral Status Register at *0E00 0001h* in the SHARC memory map are used to reflect when a PCI error has occurred. Bit 6 reads '1' if a PCI serious error has occurred and bit 7 reads '1' if a PCI parity error has occurred. These bits are cleared to '0' when the Peripheral Status Register is read.

In order to provide a visual indication of the PCI error conditions, a red LED is provided on the front panel, labelled PCI_ERR in Figure 2.1. This LED lights whenever a PCI parity or serious error has occurred. The LED is switched off when the Peripheral Status Register is read.

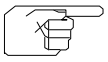


Note that the PCI9060 can be configured to generate an interrupt to the SHARCs on /IRQ0 when a PCI serious error occurs.

12.3 VMEbus Error Status

DBV66 provides two methods of monitoring VMEbus errors which while DBV66 is acting as VME master. Bit 5 (VME_ERR) in the DBV66 Peripheral Status Register at *0E00 0001h* in the SHARC memory map is used to reflect when a VME error has occurred. This bit reads '1' if a VME error has occurred and '0' otherwise. The bit is cleared to '0' when the Peripheral Status Register is read.

In order to provide a visual indication of the VME error condition, a red LED is provided, on the front panel, labelled VME_ERR in Figure 2.1. This LED lights whenever a VME error has occurred. The LED is switched off when the Peripheral Status Register is read.



Note that the Universe can be configured to generate an interrupt to the PCI bus on INTA# when a VME error occurs.

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Appendix A

Internal SRAM Organisation

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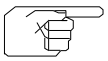
A Internal SRAM Organisation

Each SHARC provides two blocks of internal SRAM, block 0 and block 1. The SHARC can address 16, 32, 40 and 48 bit words in these blocks. When using Analog Devices' code generation tools for the SHARC, the internal memory must be allocated to these word sizes using an architecture description file. For example, a section of internal memory can be logically reserved for 48 bit instructions and another for 32 bit data.

The process of allocating areas of internal memory to different word sizes is not a trivial task. Chapter 5 of the SHARC User's Manual provides detailed information on the subject. This appendix provides a further description of the rules governing the process and gives an example scenario to demonstrate their implementation.

A.1 Overview

The SHARC memory map provides two spaces for accessing SHARC internal SRAM. The first space, from *0002 0000h* to *0003 FFFFh*, is termed the 'normal word addressing' space and provides access to 48, 40 and 32 bit words. The second space, from *0004 0000h* to *0007 FFFFh*, is termed the 'short word addressing' space and provides access to 16 bit words.

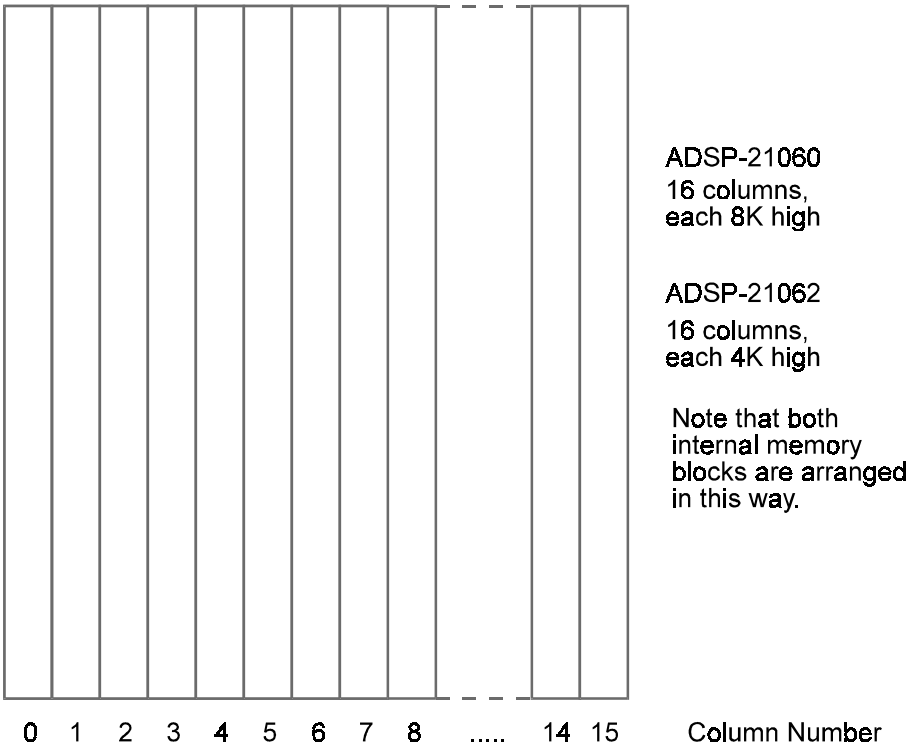


Both spaces in the SHARC memory map provide access to the same physical memory locations.

Each SRAM block is physically subdivided into sixteen 16 bit wide columns, numbered 0 to 15. In the ADSP-21060, each column is 8K bits high. In the ADSP-21062, each column is 4K bits high. The subdivision of an internal block into these columns is illustrated in Figure A.1 below.

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Figure A.1: Internal Memory Columns



As each column is 16 bits wide, 48 bit SHARC instructions each require three adjacent columns, as do 40 bit data words. Two adjacent columns are required for a 32 bit data word and a single column is needed for a 16 bit data word. The following rules determine where instructions and data can be placed in the columns:

- Any section allocated to 48 or 40 bit words in an SRAM block must be located at the start of the block.
- Of the two columns occupied by a 32 bit word, the lowest of the two column numbers must be even. For example, a 32 bit word could be stored in columns 12 and 13 but not 13 and 14.

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A.2 Example Scenario

This section employs an example scenario to describe how the internal SRAM columns are allocated to different word sizes. Memory maps for the scenario are provided to clarify the description.

The example scenario provides information on allocating regions of block 0 in an ADSP-21060. However, the concepts discussed apply equally well to block 1 and the memory blocks in an ADSP-21062.

Section A.2.1 below describes the general organisation within the memory block along with information on accessing 48, 40 and 32 bit words.

Section A.2.2 provides information on addressing 16 bit data with reference to the scenario described in Section A.2.1.

A.2.1 48, 40 and 32 Bit Words

Consider the scenario illustrated in Figure A.2. Here, the application requires 10922 (2AAAh) 48 bit instructions to be stored in an internal SRAM block. Each of these instructions requires 3 of the 16 bit wide columns.

The first instruction is located at *0002 0000h*, the next at *0002 0001h* etc. until the top of the block of three columns is reached at *0002 1FFFh*. A new set of three columns is then used from *0002 2000h* to *0002 2AAAh*. This provides all of the 48 bit locations required to store the instructions. The remaining memory can be allocated to 32 bit words.

The 32 bit data fills columns 4 and 5, 6 and 8 etc. Note that a section of column 3 is inaccessible since the most significant 16 bits of a 32 bit word must be located in an even column. Since this memory is inaccessible, the addresses allocated to it are reserved. These addresses are from *0002 2AAAh* to *0002 3FFFh*. Also, the addresses in column 4 from *0002 4000h* to *0002 4AAAh* are reserved since this section of memory is allocated to 48 bit words. Therefore, the first address for the 32 bit data is *0002 4AABh*.

The memory map for this example scenario is as illustrated in Figure A.3.

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Figure A.2: Example Scenario Column Allocation

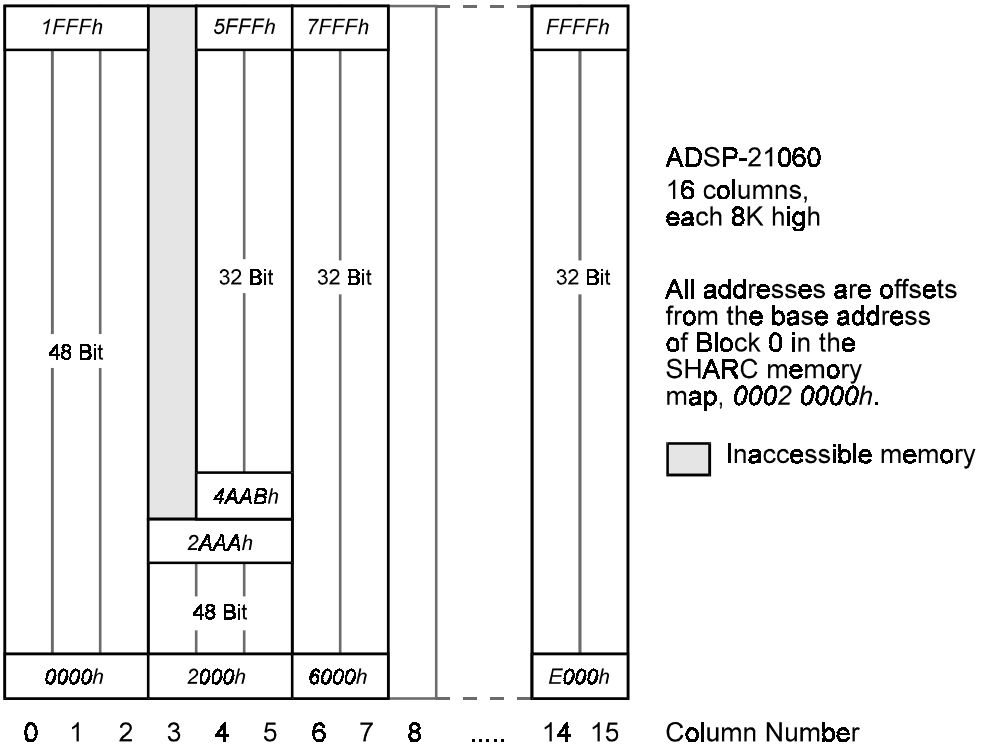
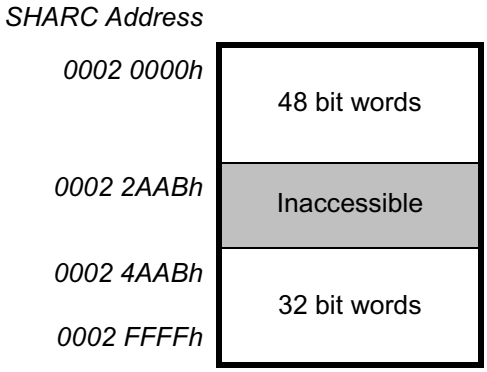


Figure A.3: Example Block 0 Longword Memory Map



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A.2.2 16 Bit Words

This section describes how 16 bit words are addressed in SRAM using the scenario described in Section A.2.1.

Alternate columns are used when addressing 16 bit data. Therefore, if two 16 bit words are written to the start of Block 0 then the first word is written to the bottom of column 1 and second word is written to the bottom of column 0. Therefore, if 16 bit accesses are used to write 32 bit data to internal SRAM, the first access writes the data to the least significant 16 bits of the 32 bit word and the second accesses the most significant bits of the word.

Therefore, taking the last two columns of Block 0 as an example, if 16 bit accesses are used to transfer 32 bit words to the SRAM, then the SHARC memory map for this region is given in Figure A.4.

Figure A.4: Example Block 0 Shortword Memory Map

SHARC Address	32 bit word		*SHARC Address*
	Most significant 16 bits	Least significant 16 bits	
0005 C001h	Word 1	Word 1	*0005 C000h*
0005 C003h	Word 2	Word 2	*0005 C002h*
0005 0005h	Word 3	Word 3	*0005 C004h*
0005 FFFDh	Word 8191	Word 8191	*0005 FFFCh*
0005 FFFFh	Word 8192	Word 8192	*0005 FFFEh*

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Appendix B

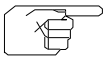
Default PCI9060 Configuration

Register Settings

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B Default PCI9060 Configuration Register Settings

This appendix provides the EEPROM default values assigned to the PCI9060 device on DBV66 at power-up/reset.



The register values provided in this appendix are for advanced users only, who wish to access the PCI9060 device directly. Refer to the PCI9060 data sheet for detailed register descriptions.

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B.1 PCI Configuration Registers

Register Name	PCI Configuration Space Address	SHARC Address	EEPROM value
Vendor ID	00h	1800 0000h (D47-D32)	1171h
Device ID	02h	1800 0000h (D31-D15)	D660h
Command	04h	1800 0001h (D47-D32)	-
Status	06h	1800 0001h (D31-D15)	-
Revision ID	08h	1800 0002h (D47-D24)	0001h
Class Code	09h	1800 0002h (D23-D15)	0680h
Cache Line Size	0Ch	1800 0003h (D47-D40)	-
Latency Timer	0Dh	1800 0003h (D39-D32)	-
Header Type	0Eh	1800 0003h (D31-D24)	-
BIST	0Fh	1800 0003h (D23-D15)	-
PCI Base Address for Memory Mapped Runtime Registers	10h	1800 0004h (D47-D15)	-
PCI Base Address for I/O Mapped Runtime Registers	14h	1800 0005h (D47-D15)	-
PCI Base Address for Local Address Space 0	18h	1800 0006h (D47-D15)	-
PCI Base Address for Local Expansion ROM	30h	1800 000Ch (D47-D15)	-
Interrupt Line	3Ch	1800 000Fh (D47-D40)	00h
Interrupt Pin	3Dh	1800 000Fh (D39-D32)	01h
Min_Gnt	3Eh	1800 000Fh (D31-D24)	FFh
Max_lat	3Fh	1800 000Fh (D23-D15)	01h

- Indicates that this register/register field is not EEPROM initialised - PCI9060 default used.

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B.2 Local Configuration Registers

Register Name	PCI Byte Address *	SHARC Address	EEPROM value
Range for PCI to Local Address Space 0	00h	1800 0020h	F000 0000h
Local Base Address (Re-map) for PCI to Local Address Space 0	04h	1800 0021h	8000 0001h
Range for PCI to Local Expansion ROM	10h	1800 0022h	FFFF F800h
Local Base Address (Re-map) for PCI to Local Expansion ROM and $BREQ_0$ control	14h	1800 0025h	6000 0000h
Bus Region Descriptors for PCI to Local Accesses	18h	1800 0026h	F80B 0343h
Range for Direct Master to PCI	1Ch	1800 0027h	C000 0000h
Local Base Address for Direct Master to PCI Memory	20h	1800 0028h	8000 0000h
Local Base Address for Direct Master to PCI IO/CFG	24h	1800 0029h	C000 0000h
Local Base Address (Re-map) for Direct Master to PCI	28h	1800 002Ah	0000 0003h
PCI Configuration Address Register for Direct Master to PCI IO/CFG	2Ch	1800 002Bh	0000 0000h

* This register set can be mapped into the PCI memory and I/O maps. The addresses given are offsets from the base address contained in the PCI9060 registers named 'PCI Base Address for Memory Mapped Runtime Registers' and/or 'PCI Base Address for I/O Mapped Runtime Registers'. For more details, refer to Section B.1.

B.3 Shared Runtime Registers

Register Name	PCI Byte Address *	SHARC Address	EEPROM value
Mailbox Register 0	40h	1800 0030h	0000 0000h
Mailbox Register 1	44h	1800 0031h	0000 0000h

* This register set can be mapped into the PCI memory and I/O maps. The addresses given are offsets from the base address contained in the PCI9060 registers named 'PCI Base Address for Memory Mapped Runtime Registers' and/or 'PC I Base Address for I/O Mapped Runtime Registers'. For more details, refer to Section B.1.

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Appendix C

D8, D16, D32 and D64 Data Transfers

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C D8, D16, D32 and D64 Data Transfers

DBV66 supports D8, D16, D32, D32 block transfers (BLTs) and D64 multiplexed block transfers (MBLTs) VME master and slave accesses. However, due to fundamental differences in the way in which the VME and PCI buses handle individual bytes of data, care must be taken to ensure that data is interpreted correctly once it has been transferred.

When making the following transfers, data will always be interpreted correctly by both the SHARCs on DBV66 and the processors on the target board:

- Any transfer between DBV66 and another DBV66 board.
- 32 bit data types transferred using D32 accesses between DBV66 and any another VME board.
- D8 accesses between DBV66 and any another VME board.

If another access type is required then consideration must be made of how bytes of data are transferred between DBV66 and the VMEbus. This appendix provides the information necessary to do this. Note that LSI's DBV66 support software employs D32 accesses only and therefore does not need to perform any byte swapping.

This appendix describes how DBV66 is configured to transfer data between memory on the DBV66 Interconnect bus and memory on another VME board, such as a host SPARCstation.

When transferring data to/from DBV66 over the VMEbus, the data is moved in a number of steps. For example, for a data transfer from DBV66:

- From memory on DBV66 to the PCI bus.
- From the PCI bus to the VMEbus.
- From the VMEbus to memory on the target VME board.

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During this transfer sequence, consideration must be given to the way in which the individual bytes of data are moved from one bus to another. In addition to this, the way in which different processors interpret data in memory must be considered.

Section C.1 describes the way in which data is moved between memories on the VME and PCI buses.

Section C.2 details how data is transferred from the PCI bus to the VMEbus on DBV66.

Section C.3 describes how the two types of processor interpret data in memory.

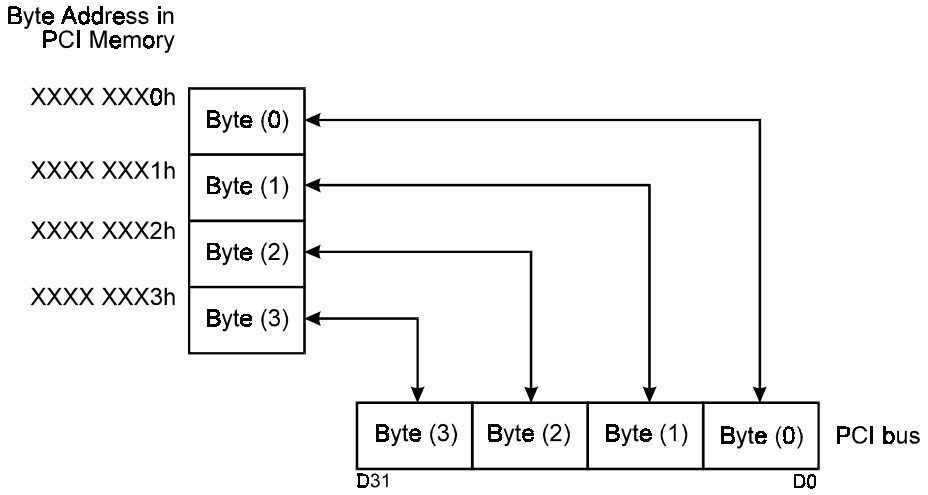
Section C.4 provides example scenarios to illustrate how bytes of data are transferred using D8, D16, D32 and D64 transfers.

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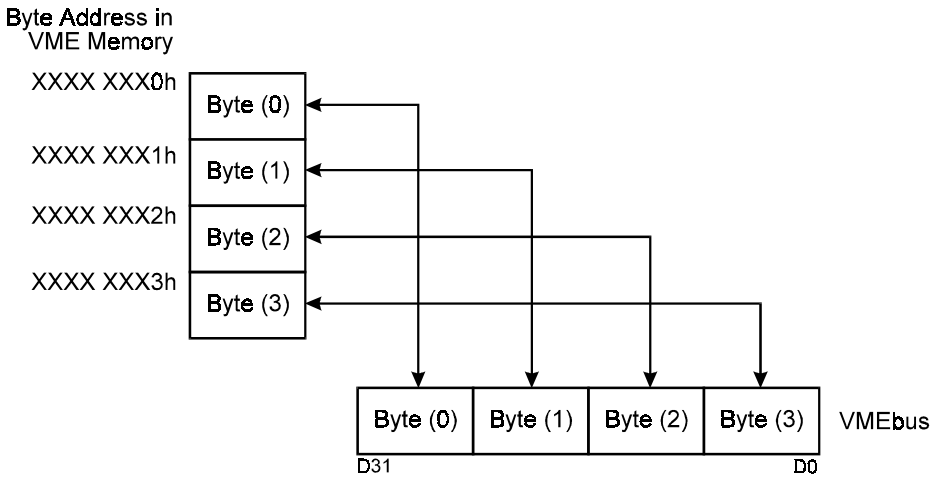
C.1 PCI Bus and VMEbus Endianness

The VME and PCI buses operate using different endian schemes. The PCI bus uses the little endian scheme and the VMEbus uses the big endian scheme. These schemes are outlined below.

The little endian scheme transfers the lowest byte of a data structure from memory to the least significant data lines on the bus. Therefore, for example, four consecutive bytes are transferred from memory to the PCI bus as follows:



The big endian scheme transfers the lowest byte of a data structure from memory to the most significant data lines on the bus. Therefore, for example, four consecutive bytes are transferred from memory to the VMEbus as follows:

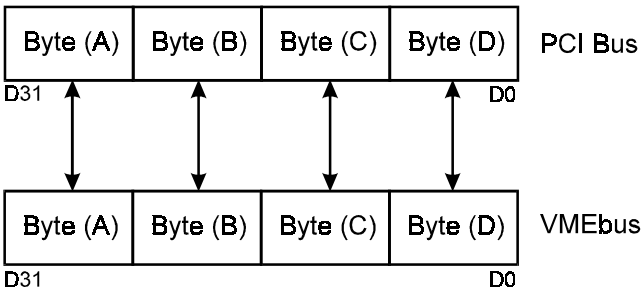


Note that the ordering of bits within individual bytes is always maintained.

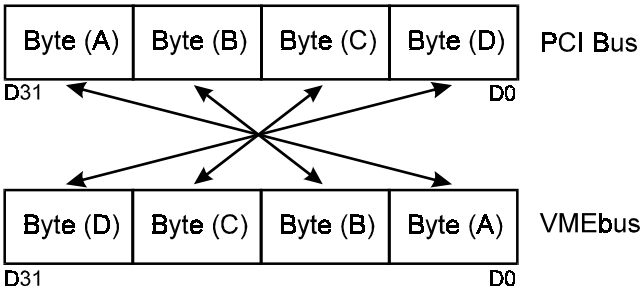
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C.2 DBV66 PCI Bus - VMEbus Byte Lane Mapping

DBV66 is configured in hardware so that there is a one-to-one mapping of byte lanes between the VME and PCI buses when D32 transfers are made, as illustrated below:



When D8, D16 or D64 transfers are made, the bytes lanes are translated as illustrated below:



C.3 Processor Endianness

There is a subtle difference between the endianness of a bus and the endianness of a processor. The endianness of a bus determines how data is transferred between memory and the bus. The endianness of a processor determines how data in memory is interpreted by the processor.

A little endian processor, such as a SHARC, expects the lowest address of a data structure to contain the least significant byte. A big endian processor, such as a SPARC, expects the lowest address to contain the most significant byte.

Therefore, for example, if a section of memory on a VME board contains four bytes of data, 12h (at lowest address), 34h, 56h and 78h (at highest address), then a little endian processor will read the value as 7856 3412h and a big endian processor will read the value as 1234 5678h.

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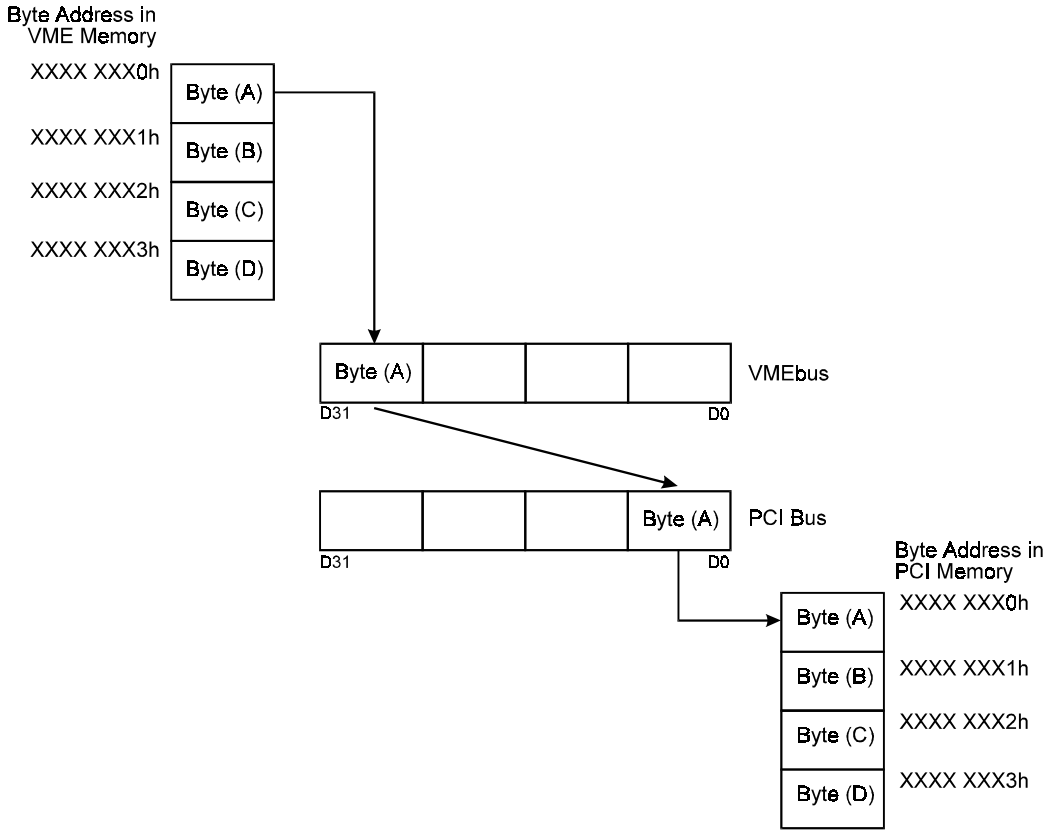
C.4 Example Scenarios

The following subsections illustrate some example scenarios using D8, D16, D32 and D64 transfers.

C.4.1 D8 Transfers

Consider the case where four byte values are stored in consecutive locations and are transferred from VME memory to Interconnect bus memory using four D8 accesses. The diagram below illustrates the first D8 access which transfers Byte A.

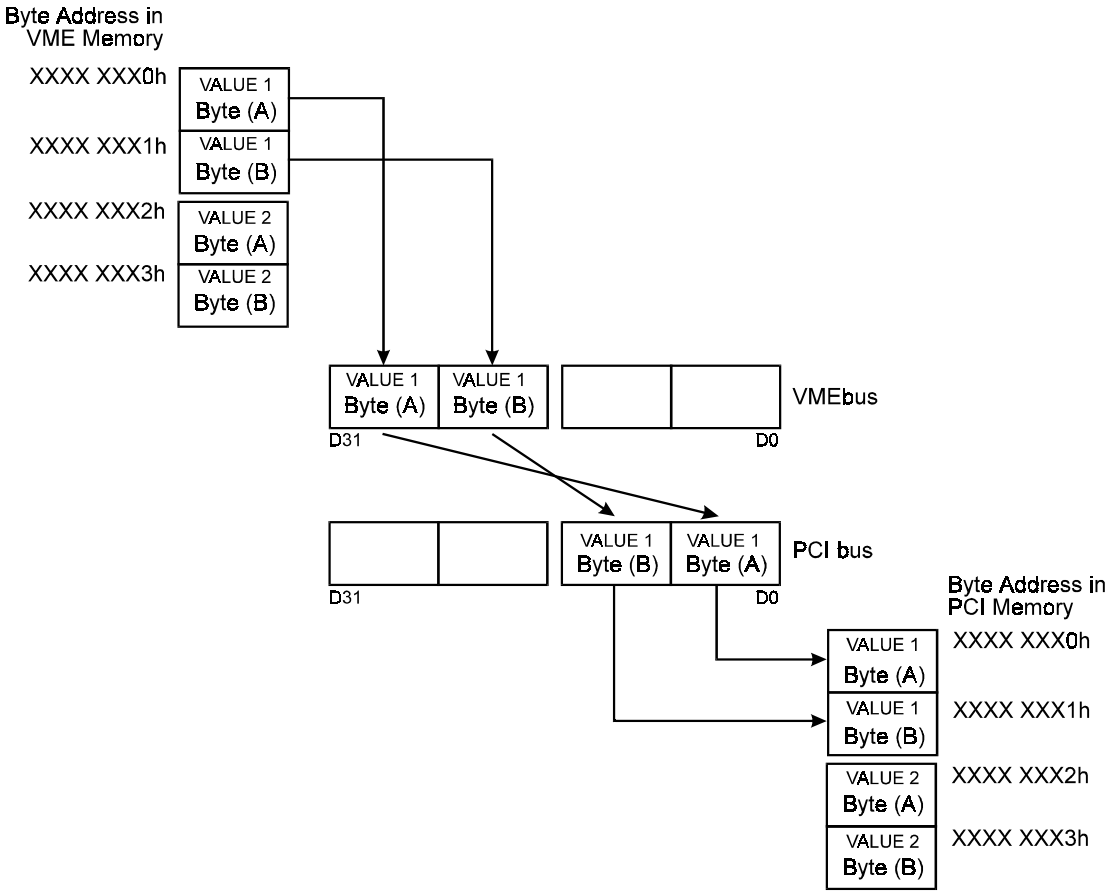
As shown, the bytes are transferred to the same addresses in each memory. Since the individual data structures are only made up of single bytes, both the big endian VME processors and the little endian SHARCs interpret the data correctly.



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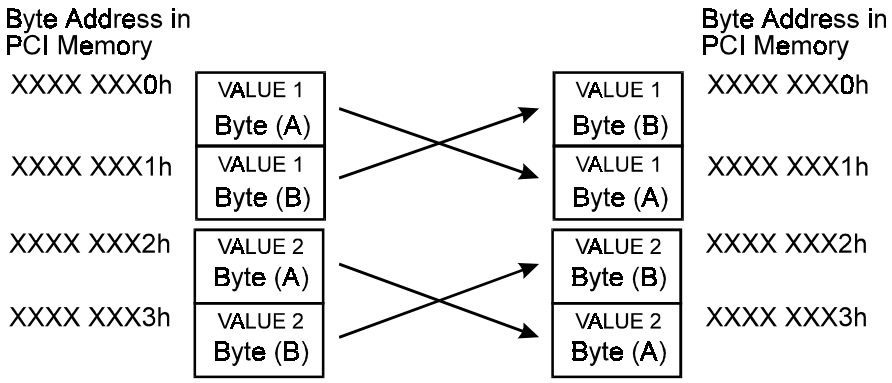
C.4.2 D16 Transfers

Consider the case where two 16 bit values are stored in consecutive locations and are transferred from VME memory to Interconnect bus memory using two D16 accesses. The diagram below illustrates the first D16 access which transfers Value 1.



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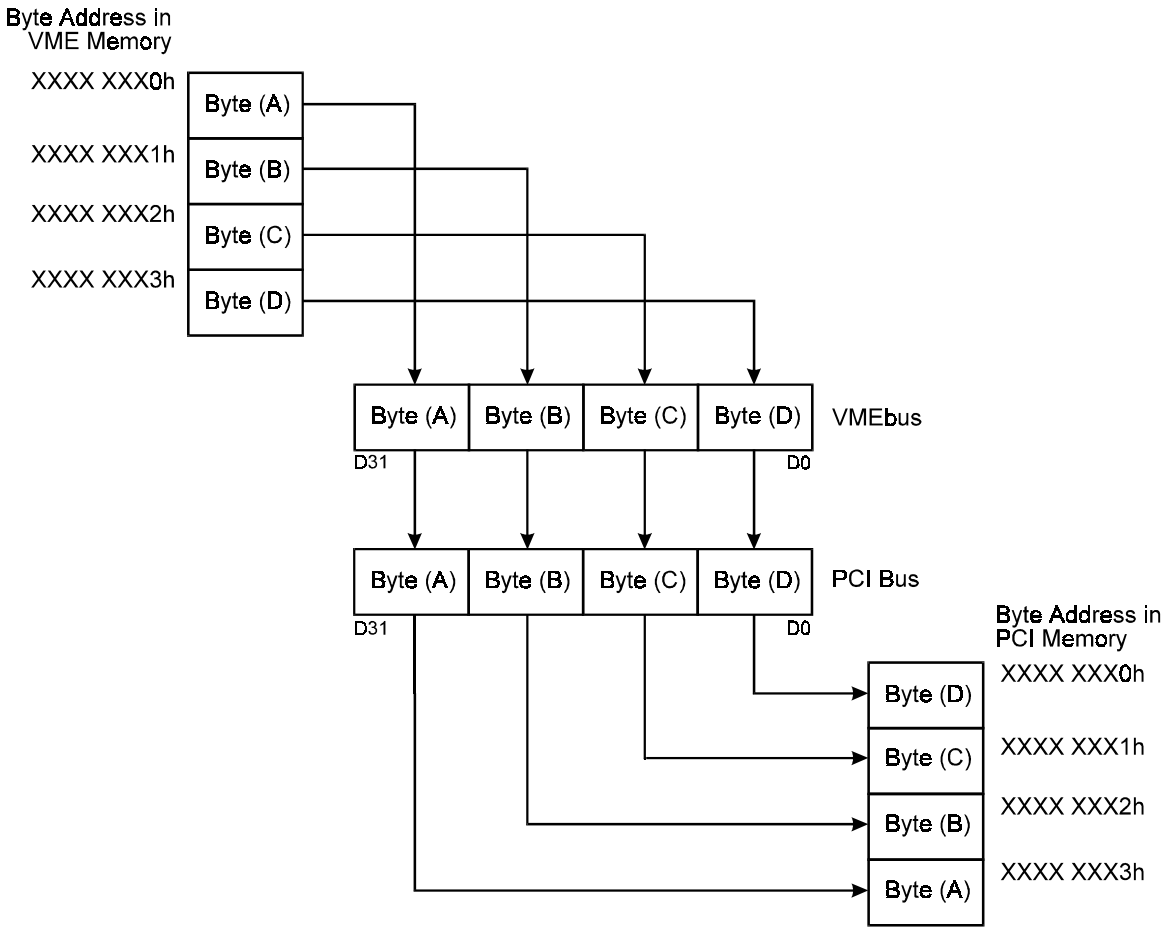
As shown, the address ordering of the two values is maintained as well as the ordering of bytes within the values. Now, since big and little endian processors expect the bytes in a data structure to be ordered in the opposite sense, the following translation must be performed in software to allow the data to be correctly interpreted:



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C.4.3 D32 Transfers

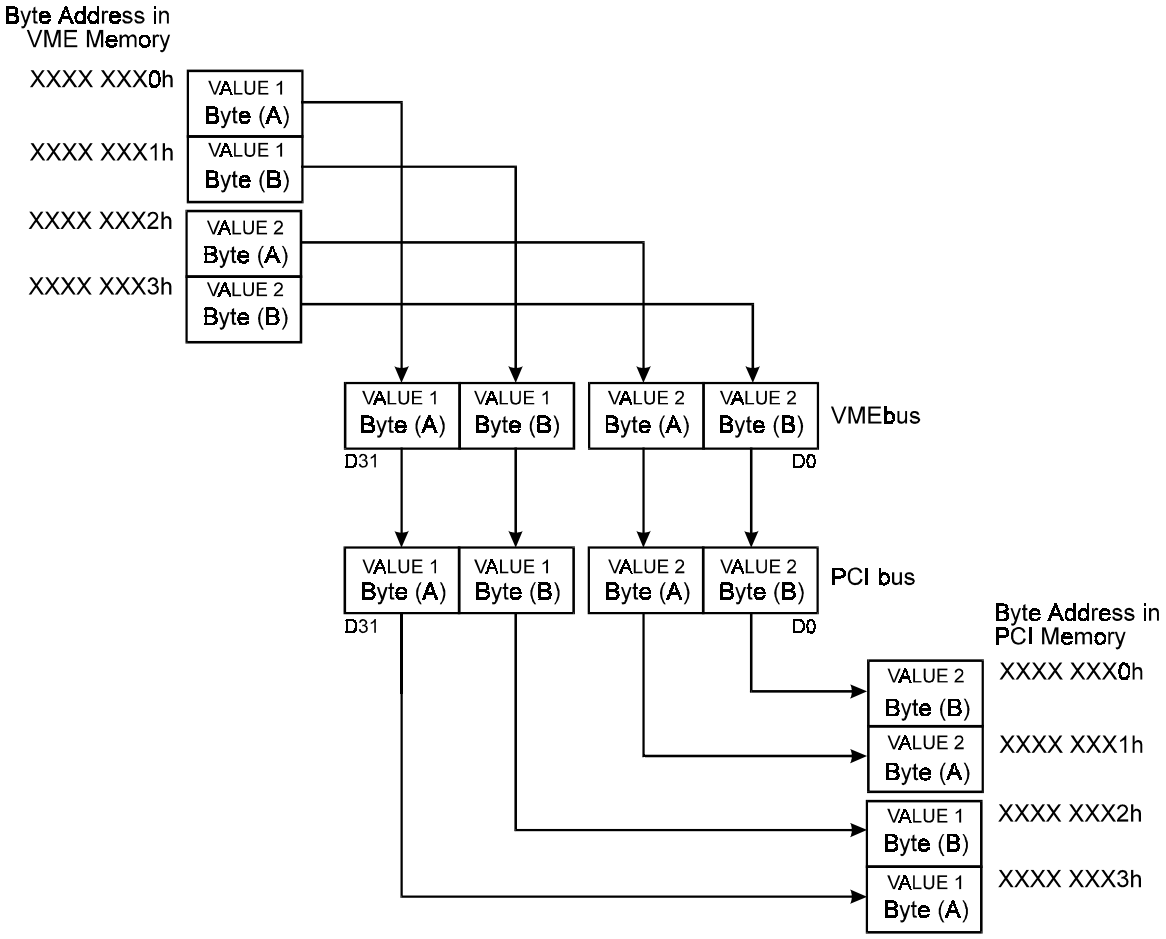
Consider the case where four byte values are stored in consecutive locations and are transferred from VME memory to Interconnect bus memory using a single D32 access. The diagram below illustrates the transfer.



It can be seen that the order of bytes in the two memories has been reversed. The purpose of this reversal is to allow D32 data to be correctly interpreted by both the SHARCs, which expect little endian storage, and big endian processors on the VMEbus such as a SPARC. For example, if the value 1234 5678h is transferred from the Interconnect bus to a host SPARCstation, both the SHARC and the SPARC processors interpret the data as 1234 5678h.

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Now, consider the case of where the four bytes contain two consecutive 16 bit values. The resulting translation of bytes between memories on the two buses, when using a single D32 access to transfer them, is illustrated below.



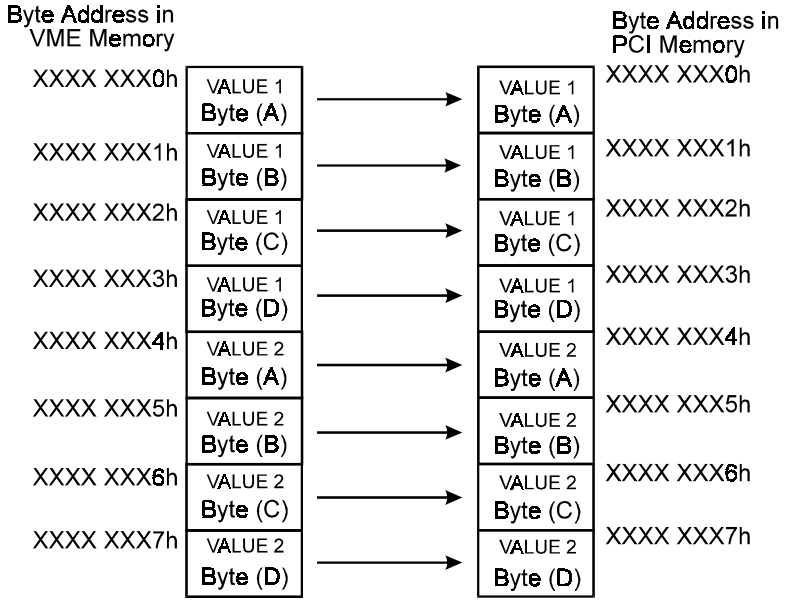
In this case, the ordering of bytes within the 16 bit words is maintained but the ordering of the two words is swapped. For example, the values 1234h and 5678h in VMEbus memory will be swapped to 5678h and 1234h in Interconnect bus memory.

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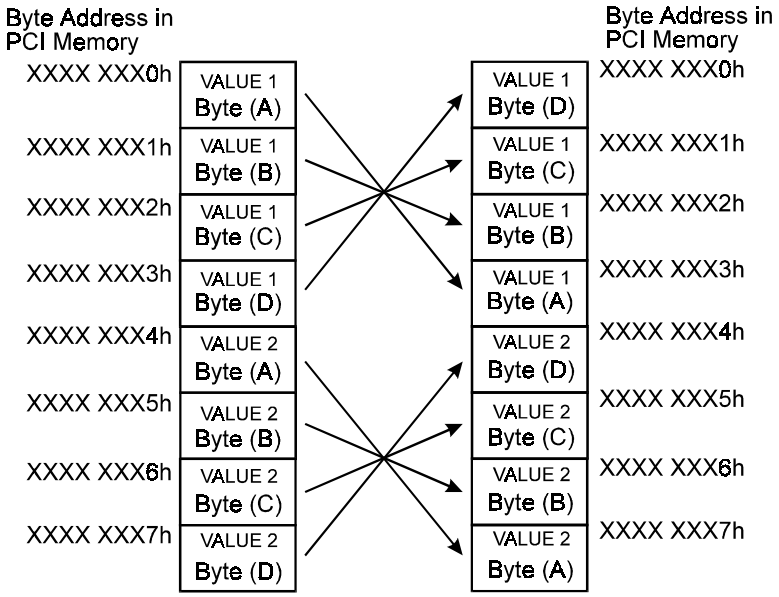
C.4.4 D64 Transfers

Consider the case where two 32 bit values are stored in consecutive locations and are transferred from VME memory to Interconnect bus memory using a single D64 access.

The transfer results in a direct mapping of bytes in the two memories as illustrated below:



Therefore, in order for the data to be correctly interpreted by the SHARCs, the following byte swapping must be performed in software:



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Appendix D

P2 Breakout Board

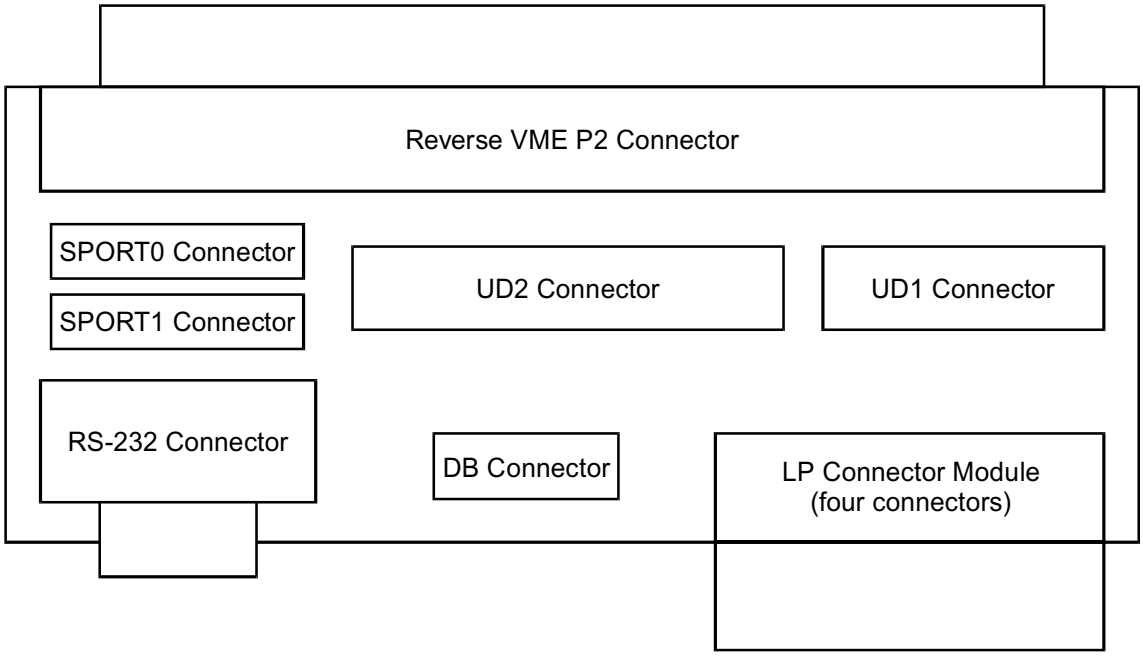
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D P2 Breakout Board

This appendix describes the LSI breakout board which can be connected to the VME P2 connector on the reverse side of the VME back-plane. This board features ten connectors which permit the easy routing of signals to/ from the DBV66 board via the z, a, c and d pins of the P2 connector.

A board layout diagram which indicates the names and positions of the breakout board's connectors is given in Figure D.1. These connectors are detailed in Section D.1. Installation of the breakout board is described in Section D.2.

Figure D.1: P2 Breakout Board Layout Diagram



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D.1 Connectors

In addition to the P2 connector, there are ten connectors on the P2 breakout board. These connectors and the signals that they carry are outlined below.

- **LP**

  The LP connector module consists of four connectors which provide routings to/from the SHARC processor link ports for two of the processors on DBV66. The module also provides routings for the Broadcast Link Port on DBV66. Refer to Chapter 7 for details of the SHARC link ports.

- **SPORT0**

  Provides routings for the SHARC processors' SPORT0 synchronous serial ports on DBV66. Refer to Chapter 8 for details of the SHARC serial ports.

- **SPORT1**

  Provides routings for the SHARC processors' SPORT1 synchronous serial ports on DBV66. Refer to Chapter 8 for details of the SHARC serial ports.

- **RS-232**

  Provides routings for RS-232 serial port signals to/from the Philips SCC2691 UART device on DBV66. Refer to Section 3.6 for details of the RS-232 serial port.

- **DB**

  Provides routings for debug signals to/from DBV66 (refer to Section D.1.5).

- **UD1**

  Provides routings for user-defined signals to/from PMC Site 1 on the DBV66 board (refer to Section 4.12.3 and Section D.1.6).

- **UD2**

  Provides routings for user-defined signals to/from PMC Site 1 on the DBV66 board (refer to Section 4.12.3 and Section D.1.7).

The above connectors are described in more detail in the subsections below which provide the connector pinouts.

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D.1.1 LP Connector Module

This module comprises four 8-pin connectors which can be used to route link port signals to/from the SHARC processors on the DBV66 board. The module routes three sets of link port signals, as follows:

- **Link Port A (LP A) Connector**

  Routes link port signals to/from one of the SHARC processors on the DBV66. The identity of SHARC processor depends on the number of processors on the board, as detailed in Table D.1 below.

- **Link Port B (LP B) Connector**

  Routes link port signals to/from one of the SHARC processors on the DBV66. The identity of SHARC processor depends on the number of processors on the board, as detailed in Table D.1 below.

- **Broadcast Link Port (BLP) Connectors:**

  The two Broadcast Link Port connectors support duplicate sets of signals. Each connector routes SHARC link port 0 signals from any of the processors on DBV66 or conversely to all or selected processors on DBV66. Refer to Section 7.3 for details of the Broadcast Link Port.

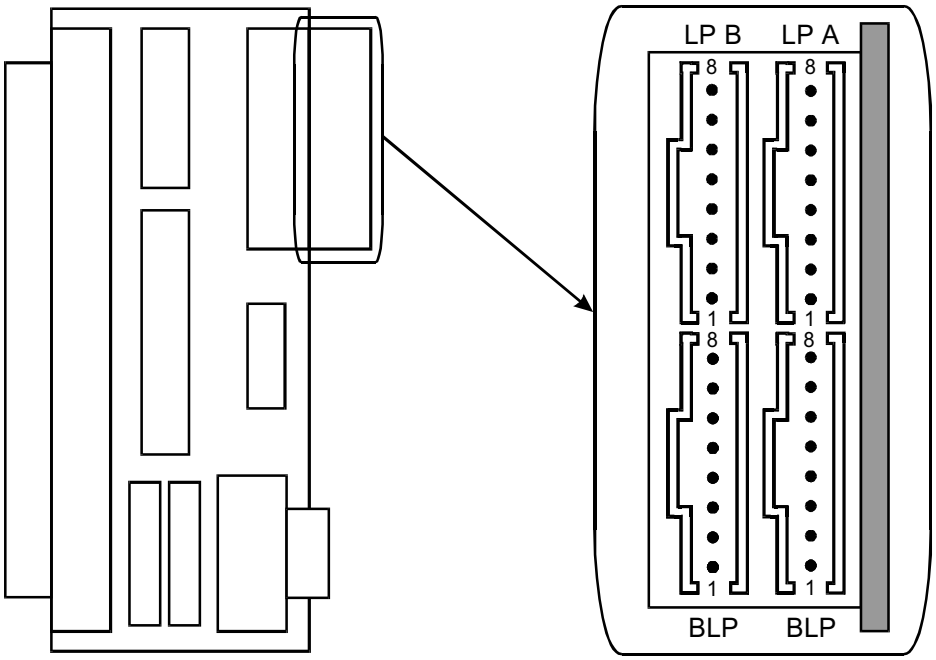
Table D.1: SHARC Processors for Link Port Connectors

Number of Processors on DBV66	LP Connector	SHARC Processor	SHARC Link Port
6	LP A	6	5
	LP B	6	5
4	LP A	3	3
	LP B	4	3
2	LP A	1	3
	LP B	2	2

The LP connector module is illustrated in Figure D.2 below and the connector pinouts are given in Table D.2.

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Figure D.2: LP Connector Module



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Table D.2: LP Connector Module Pinout

LP Connector	LP Pin	P2 Pin	Signal
LP A	1	d1	LxCLK
	2	d2	LxACK
	3	-	GND
	4	d4	$LxDAT_0$
	5	d5	$LxDAT_1$
	6	-	GND
	7	d6	$LxDAT_2$
	8	d7	$LxDAT_3$
LP B	1	d9	LxCLK
	2	d10	LxACK
	3	-	GND
	4	d12	$LxDAT_0$
	5	d13	$LxDAT_1$
	6	-	GND
	7	d14	$LxDAT_2$
	8	d15	$LxDAT_3$
BLP	1	d16	LxCLK
	2	d17	LxACK
	3	-	GND
	4	d19	$LxDAT_0$
	5	d20	$LxDAT_1$
	6	-	GND
	7	d21	$LxDAT_2$
	8	d22	$LxDAT_3$

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D.1.2 SPORT0 Connector

This 8-pin 0.1 inch header can be used to route signals to/from the SPORT0 synchronous serial ports on DBV66 (refer to Chapter 8 for details of these ports). The SPORT0 connector is illustrated in Figure D.3 below and its pinout is given in Table D.3.

Figure D.3: SPORT0 Connector

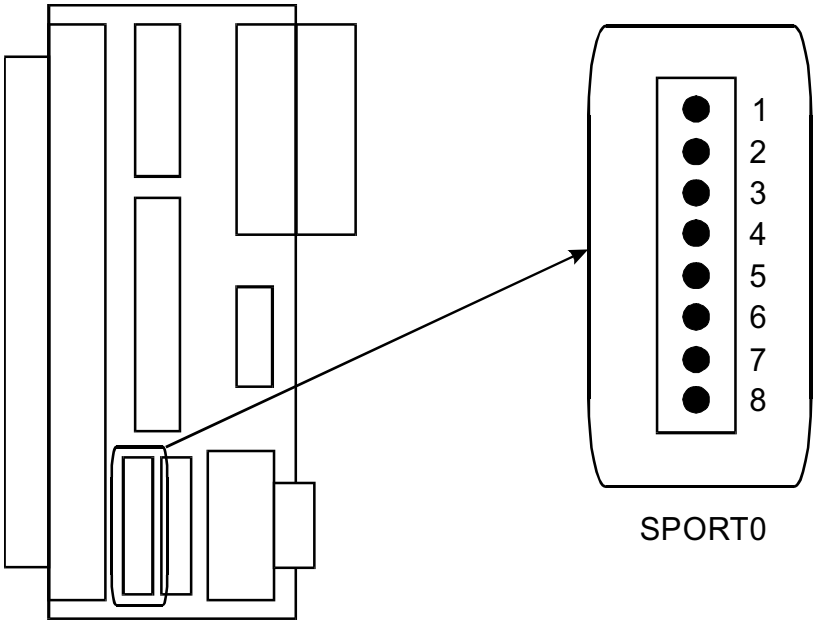


Table D.3: SPORT0 Connector Pinout

SPORT0 Pin	P2 Pin	Signal	Source
1	z9	RFS0	*TDM0
2	-	GND	
3	z1	DT0	
4	z3	TCLK0	
5	-	GND	
6	z7	RCLK0	
7	z5	DR0	
8	-	GND	

* TDM0 refers to Time Division Multiplexed port 0, see Section 8.2.

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D.1.3 SPORT1 Connector

This 8-pin 0.1 inch header can be used to route signals to/from the SPORT1 synchronous serial ports on DBV66 (refer to Chapter 8 for details of these ports). The SPORT1 connector is illustrated in Figure D.4 below and its pinout is given in Table D.4.

Figure D.4: SPORT1 Connector

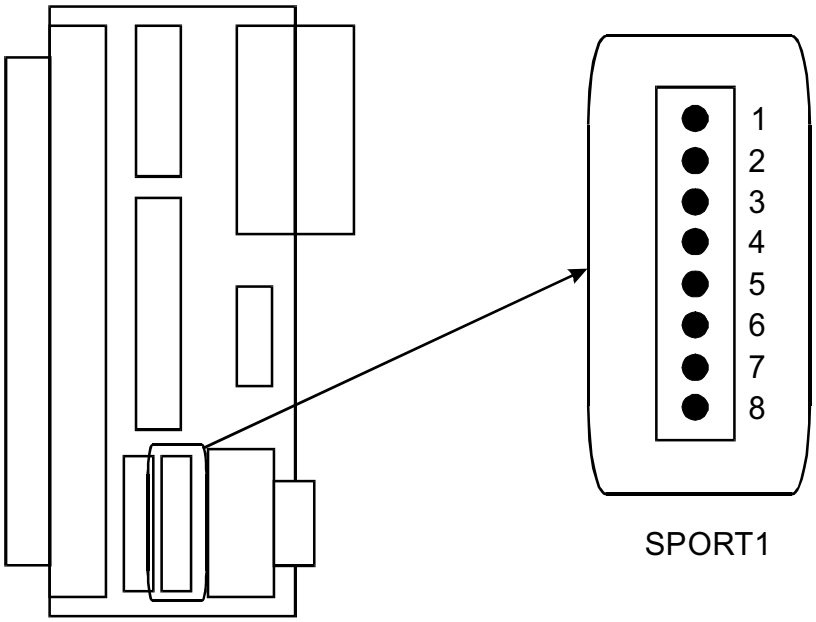


Table D.4: SPORT1 Connector Pinout

SPORT1 Pin	P2 Pin	Signal	Source
1	z31	RFS1	*TDM1
2	-	GND	
3	z23	DT1	
4	z25	TCLK1	
5	-	GND	
6	z29	RCLK1	
7	z27	DR1	
8	-	GND	

* TDM1 refers to Time Division Multiplexed port 1, see Section 8.2.

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D.1.4 RS-232 Connector

This 9-pin right-angled D-type connector can be used to route RS-232 serial port signals to/from the Philips SCC2691 UART device on DBV66 (refer to Section 3.6 for details of this port). The RS-232 connector is illustrated in Figure D.5 below and its pinout is given in Table D.5.

Figure D.5: RS-232 Connector

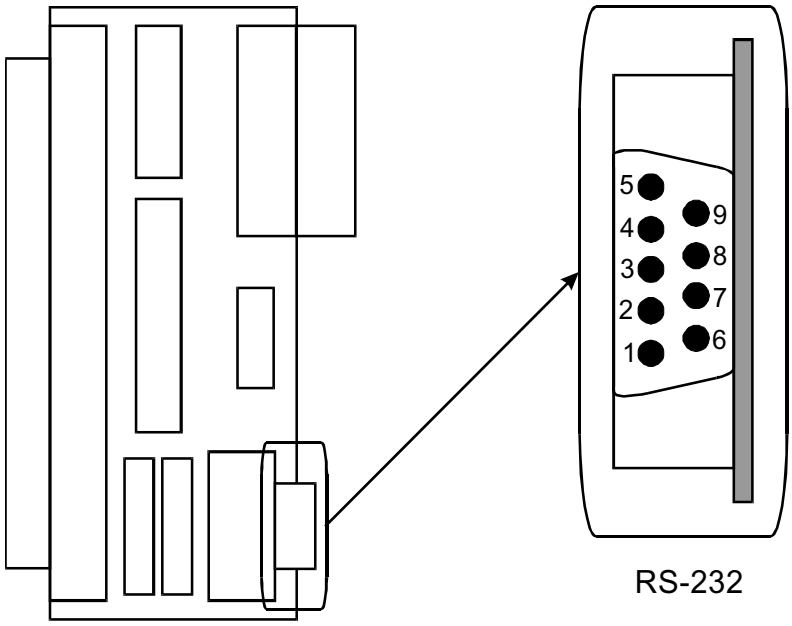


Table D.5: RS-232 Connector Pinout

RS-232 Pin	P2 Pin	Signal
1	N/C	-
2	z15	RXD
3	z11	TXD
4	-	+5V
5	-	GND
6	N/C	-
7	z17	RTS
8	z19	CTS
9	N/C	-

N/C = Not Connected

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D.1.5 DB Connector

This 10-pin 0.1 inch header can be used to route debug signals to/from DBV66. The DB connector is illustrated in Figure D.6 below and its pinout is given in Table D.6.

Figure D.6: DB Connector

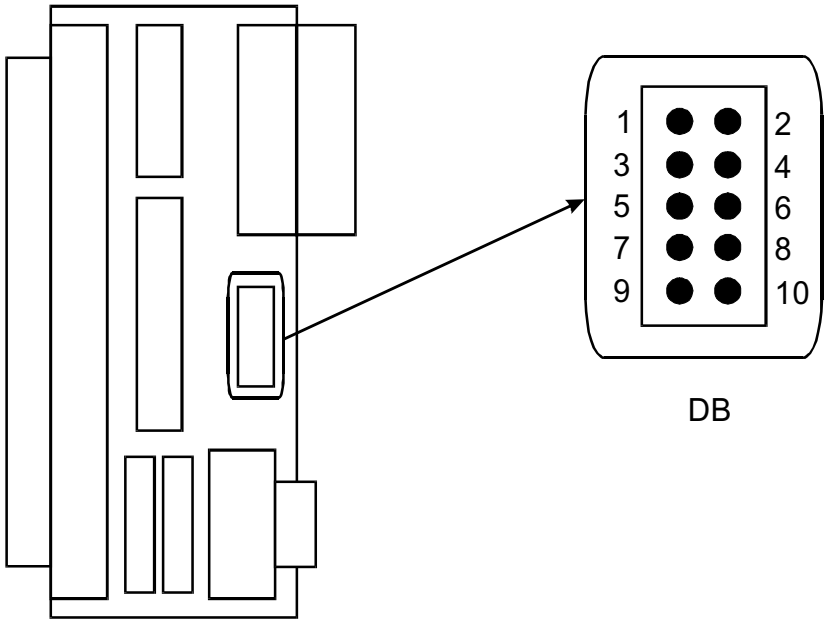


Table D.6: DB Connector Pinout

DB Pin	P2 Pin	Signal	DB Pin	P2 Pin	Signal
1	-	GND	2	z21	GIRQ
3	-	GND	4	d24	IN0
5	d25	IN1	6	d27	OUT0
7	d28	OUT1	8	d29	OUT2
9	d30	OUT3	10	-	+5V

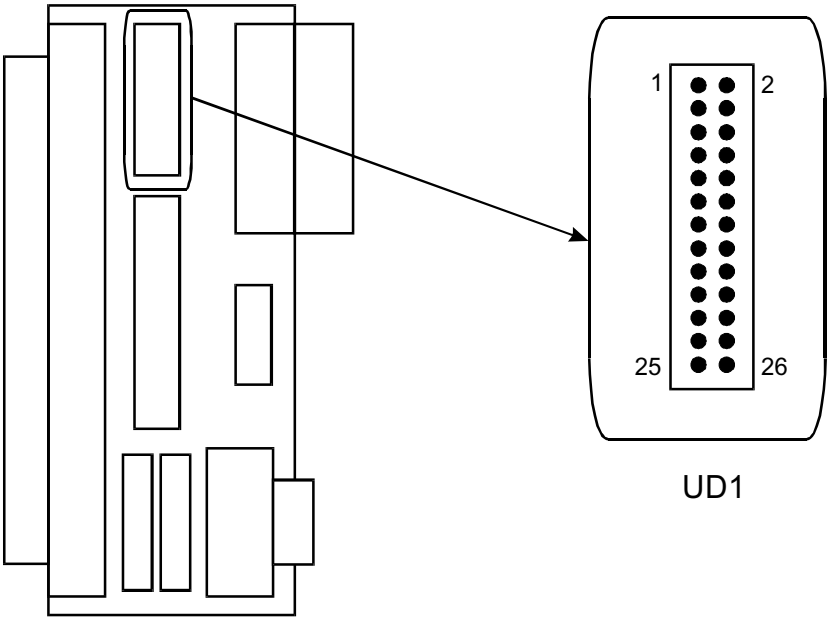
The signals OUT0-3 and IN0-1 are described in Section 3.3.4.

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D.1.6 UD1 Connector

This 26-pin 0.05 inch header can be used to route user-defined signals to/from PMC Site 1 on the DBV66 board. The UD1 connector is illustrated in Figure D.7 below and its pinout is given in Table D.7.

Figure D.7: UD1 Connector



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Table D.7: UD1 Connector Pinout

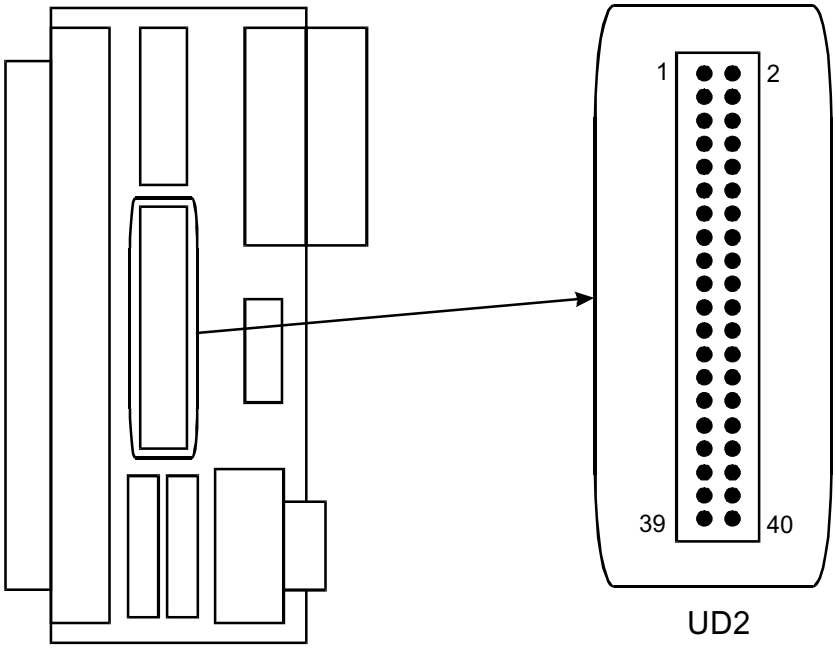
UD1 Pin	P2 Pin	PMC Site 1 J14 Pin	UD1 Pin	P2 Pin	PMC Site 1 J14 Pin
1	c1	1	2	a1	2
3	c2	3	4	a2	4
5	c3	5	6	a3	6
7	c4	7	8	a4	8
9	c5	9	10	a5	10
11	c6	11	12	a6	12
13	c7	13	14	a7	14
15	c8	15	16	a8	16
17	c9	17	18	a9	18
19	c10	19	20	a10	20
21	c11	21	22	a11	22
23	c12	23	24	a12	24
25	c13	25	26	a13	26

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D.1.7 UD2 Connector

This 40-pin 0.05 inch header can be used to route user-defined signals to/from PMC Site 1 on the DBV66 board. The UD2 connector is illustrated in Figure D.8 below and its pinout is given in Table D.8.

Figure D.8: UD2 Connector



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Table D.8: UD2 Connector Pinout

UD2 Pin	P2 Pin	PMC Site 1 J14 Pin	UD2 Pin	P2 Pin	PMC Site 1 J14 Pin
1	c14	27	2	a14	28
3	c15	29	4	a15	30
5	c16	31	6	a16	32
7	c17	33	8	a17	34
9	c18	35	10	a18	36
11	c19	37	12	a19	38
13	c20	39	14	a20	40
15	c21	41	16	a21	42
17	c22	43	18	a22	44
19	c23	45	20	a23	46
21	c24	47	22	a24	48
23	c25	49	24	a25	50
25	c26	51	26	a26	52
27	c27	53	28	a27	54
29	c28	55	30	a28	56
31	c29	57	32	a29	58
33	c30	59	34	a30	60
35	c31	61	36	a31	62
37	c32	63	38	a32	64
39	N/C	-	40	N/C	-

N/C = Not Connected

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D.2 Breakout Board Installation

All LSI hardware must be protected against static discharge. Appropriate anti-static precautions, such as using the wrist strap supplied with DBV66, must be taken during installation of the breakout board.

The P2 breakout board is installed by simply push-fitting the board into the VME P2 connector (corresponding to your DBV66 board) on the reverse side of the VME back-plane. When installing the breakout board, the side containing the connector sockets must be on your left. Push the board into place firmly but gently.

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