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MVME130XT
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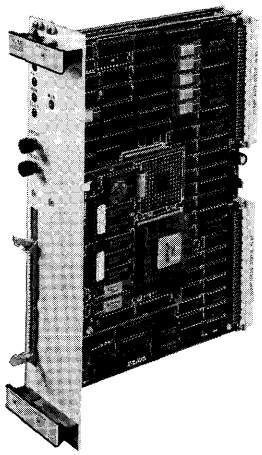
VMEmodule™ 32-Bit Microcomputer with Cache Accelerator

- MC68020 Microprocessor with 32-bit Address and Data Bus
- MC68881 Floating Point Coprocessor
- Demand Paged Virtual Memory Management Capability (MVME131XT only)
- VSB* Interface for High-Speed Data Path to and from Memory
- 16Kb Cache Memory for Concurrent Data Storage with Accelerated Data Access, and Zero Wait-state Operation
- Onboard Interrupt, Interrupt Handler and Arbiter
- Programmable Timer
- Dual Multiprotocol Serial I/O Ports

The MVME130XT is a two-board VME-based microcomputer assembly utilizing state-of-the-art components to achieve the highest level of performance currently available. It consists of an MVME130 Monoboard Microcomputer Module, factory coupled to an MVMEXTCAC Cache Accelerator Module . . . a combination which provides up to 100% improvement in system speed[1] compared with the MVME130 Monoboard Microcomputer alone.

The two-board system plugs into a standard VMEbus backplane and is fully compatible with the wide selection of VME peripheral modules.

Utilizing the MC68020 Microprocessor, the MVME130XT has onboard provisions for plugging in an MC68881 Floating Point Coprocessor and an MC68851 Paged Memory Management Unit when the latter becomes available. In the meantime, a second version of the system, the MVMX131XT, employs an optional auxiliary Memory Management Board which conforms to a subset of the MC68851 and plugs into an onboard socket of the assembly to provide interim memory management functions.



GENERAL DESCRIPTION

The MVME130XT Microcomputer Assembly combines the processing power of the 32-bit MC68020 Microprocessor with the speed-enhancement properties of a 16Kb Cache Memory Accelerator. The Cache Accelerator, a small, fast memory system, compensates for the typical speed mismatch between a very fast CPU and its relatively slow associated dynamic RAM main-memory system. It does so by concurrently storing the data most recently stored in main-memory locations. This data can subsequently be obtained by fast accesses of "cached" locations rather than by much slower accesses of main memory.

To accommodate for the fact that the cache memory normally has much less capacity than the main memory system, little-used accesses stored in the cache memory are routinely replaced with more active ones, based on the bus traffic between the MVME130 Microprocessor Module and the VMEbus and VSB memory interfaces. This assures maximum utilization of the cache.

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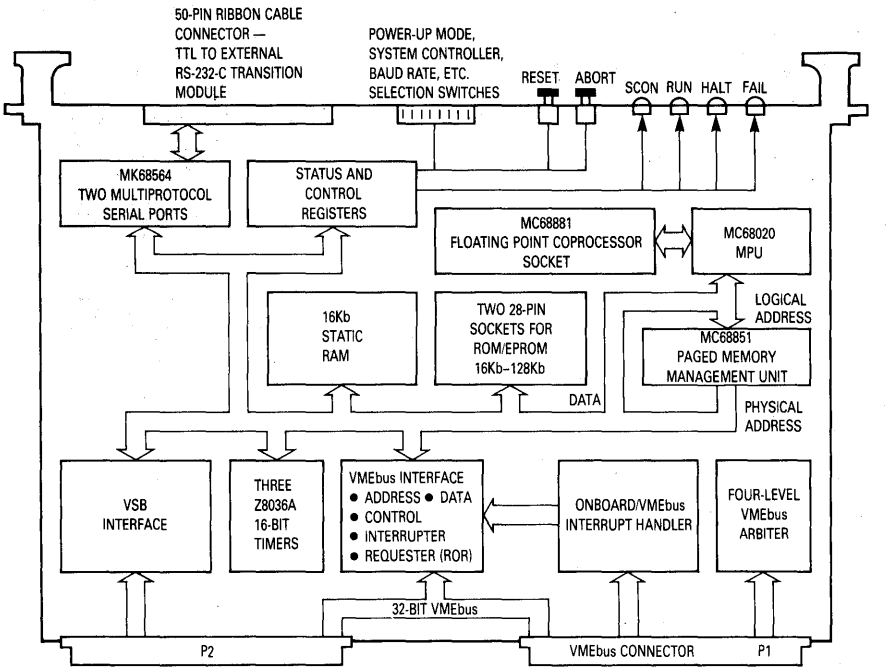


Figure 1. MVME131 Functional Block Diagram

THE MICROCOMPUTER BOARD — MVME130/MVME131

MICROPROCESSORS

A block diagram of the MVME131 Microcomputer Board is shown in Figure 1. The heart of the system is the MC68020 Microprocessor operating at a fixed frequency of 16.67 MHz. This latest member of the Motorola M68000 Family offers full 32-bit operation with 32-bit external address and data paths. With its high clock rate, enhanced addressing modes, and on-chip instruction cache, this advanced MPU provides leading-edge performance while maintaining software compatibility with its widely accepted predecessors.

On the MVME130XT Module the MC68020 Microprocessor is supported by an onboard socket that is prewired to accept the MC68881 Floating Point Coprocessor. This optional accessory chip greatly improves computing speed of the system and is recommended for applications involving a high level of arithmetic operations.

OPTIONAL MEMORY EXPANSION

In support of the microprocessor(s), the microcomputer board has two prewired 28-pin sockets for up to 16Kb of Static RAM. If the intended application does not require onboard RAM, however, these JEDEC sockets can be reconfigured to accept EPROMs up to 512K in size.

With one or more MVME204-1 or -2 DRAM with VSB Modules which provide 1Mb and 2Mb, respectively, the MVME130 can avail itself of virtually unlimited memory capacity while maintaining a performance level similar to that of a Monoboard VMEmodule Microcomputer with onboard memory. Also available for high performance memory expansion is the MVME214 Static RAM/ROM with VSB. This module has provisions for battery backup and has 16 sockets which accept many standard JEDEC 24-pin and 28-pin RAM, ROM and EPROM devices. It can provide up to 1Mb of storage capacity.

Memory modules for expanding VME system memory include the MVME202, MVME222-1 and MVME222-2 DRAM modules which have a 8-/16-bit data bus width and offer 512K, 1Mb and 2Mb of capacity, respectively, the MVME225 DRAM, a full 32-bit module offering 2Mb of capacity, the MVME215-1, -2, and -3 CMOS RAM modules with onboard power monitor and battery for power down backup and which offer 256Kb, 512Kb and 1Mb of capacity, respectively, and the MVME211 Static RAM/ROM module with 16 sockets for JEDEC 24-pin and 28-pin devices and which can provide up to 1Mb of storage capacity.

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MEMORY MANAGEMENT UNIT

The MVME130XT anticipates the eventual utilization of the MC68851 Demand Paged Virtual Memory Management Unit with an onboard socket prewired for this device. In the interim, until the MC68851 MMU becomes available, Motorola furnishes the MVME131XT System which includes a Daughter Board plugged in the socket that is allocated for the MMU Chip. This auxiliary board contains circuitry that conforms to a subset of the MC68851, and provides the hardware logical-to-physical address translation and access protection necessary for operating system support.

VMEbus INTERFACE

The VMEbus interface permits:

- VMEbus arbitration
- Buffering of data, address and control signals
- Word data manipulation
- Interrupt handling

The VMEbus arbiter arbitrates up to four levels of bus mastership on a priority basis, and incorporates the Release on Request option described in the VMEbus specification.

MVMX32bus INTERFACE

This interface occupies 64 I/O pins which provide access to the system's high-speed memory channel. The signals utilize multiplexing of address and data to accommodate full 32-bit functionality, along with appropriate control signals, within the 64-pin allotment. On the MVME130 Module, this interface is limited to serving one master. It can be turned off via a control bit to force all accesses to go to the VMEbus, and speed up VMEbus accesses.

PROGRAMMABLE TIMER

The onboard programmable timer provides three independent cascadable 16-bit counters with interrupt capability.

SERIAL I/O

The Module is equipped with two multiprotocol serial I/O ports accessible via a 50-pin flat ribbon cable connector at the top of the board. Signal levels at this connector correspond to TTL specifications, but can be transformed to RS-232-C levels by means of a separately available distribution board and cable assembly (MVME707). The ports have full- and half-duplex compatibility with programmable baud rates. They are suitable for synchronous or asynchronous operation, with 5 to 8 bits per character, plus parity.

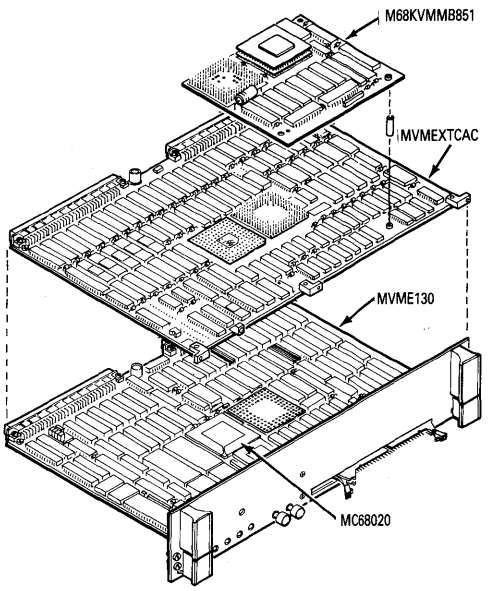


Figure 2. Exploded View Showing MVME131XT Assembly Details

MEMORY MAP

Table 1 indicates the 32-bit memory address map for various devices addressed by the MVME130 Module. A 24-bit address map is determined by eliminating the two most significant hex digits from the 32-bit addresses. A control bit on the control register permits a switch between 16- and 32-bit data paths, and between 32-/24-bit modifier codes.

Table 1. Address Map

Device	Physical Address	Comments
VMEbus/VSB	00000000-FFEFFFFF	32/16-bit port size; R/W.
ROM	FFF00000-FFF8FFFF	16-bit port size; read only.
Local Static RAM	FFF20000-FFF2FFFF	16-bit port size; R/W.
Spare	FFF40000-FFF6FFFF	32-bit port size; R/W provided for cache expansion ability.
Timer	FFFBxx00-FFFBxx2F	8-bit port size; R/W.
Status & Control	FFFBxx30-FFFBxx3F	32-bit port size; Status is read only; Control is R/W.
Serial I/O Port	FFFBxx40-FFFBxx5F	8-bit port size; most are R/W.
Reserved	FFFBxx60-FFFBxx6F	Unimplemented.
Spare	FFFBxx70-FFFEFFFF	Unimplemented; Access will cause LBTO (BERR source) cycle termination.
VMEbus Short I/O	FFFF0000-FFFFFFFF	16-bit; R/W; VMEbus Short I/O Address Modifier will be generated.

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INTERRUPT HANDLER

The MVME130 allows interrupts to the onboard CPU from up to 20 sources. The interrupt handler preprocesses interrupt sources into three groups of seven interrupts corresponding to the seven possible MC68020 interrupt levels. The groups are labeled Group 1, Group 2, and Group 3. The interrupt service priority is determined by the interrupt level and the group number. Interrupts with different interrupt levels are processed according to the standard interrupt processing discipline. Interrupts within an interrupt level are processed according to the group number.

Group 1 is reserved for VMEbus interrupts. The interrupt handler processes Group 2 and 3 interrupts differently from Group 1 interrupts. If the interrupt being acknowledged is a Group 2 or 3 interrupt, the interrupt handler fetches the appropriate exception vector number from PROM and sends it to the CPU via the local bus. If the interrupt being acknowledged is a Group 1 interrupt, the exception vector number is fetched from the VMEbus where it was placed by the interrupting device.

The Interrupt assignments are described in Table 2.

VMEbus INTERRUPTER

The VMEbus Interrupter can generate any level of VMEbus interrupt under software control. When the VMEbus interrupt is acknowledged, the Interrupter places the appropriate vector from a hardware register on the VMEbus.

STATUS/CONTROL REGISTERS

The MVME130 Status and Control Registers provide local and system-wide status information from which the onboard MPU can determine VMEbus information, interrupt status, the source of a particular BERR, and which self-test to perform. The MVME130 Status/Control Register bits control the module's hardware by providing configuration and control information to the VMEbus Interrupter, the Interrupt Handler, the VMEbus Arbiter and VSB.

The Control Register bits are software alterable. The Status/Control registers are privileged resources and in special cases can be made accessible by the user. The Status and Control Register formats are described in Tables 3 and 4, respectively.

Table 2. Interrupt Handler Priority Assignments

IRQ Level	Priority Within a Particular IRQ Level Determines the Service Order		
	(Highest)	(Middle)	(Lowest)
	Group 3	Group 2	Group 1 (VMEbus)
7	ABORT	ACFAIL Interrupt ACFIRQ	IRQ7
6	TMRIRQ	SYSFIRQ	IRQ6
5	SIOIRQ	VBISIRQ	IRQ5
4	Unassigned	VXIRQ	IRQ4
3	Unassigned	Unassigned	IRQ3
2	Unassigned	Unassigned	IRQ2
1	N/A	Unassigned	IRQ1

Within a Group x, interrupt priority decreases from top to bottom in the table.
Within a particular IRQ level, interrupt priority decreases from left to right.

Group 3 Interrupts

ABORT	<Abort Pushbutton IRQ>
TMRIRQ	<Timer IRQ>
SIOIRQ	<Dual Channel Serial Port IRQ>

Group 2 Interrupts

ACFIRQ	<VMEbus AC Power Fail Interrupt>
SYSFIRQ	<VMEbus System Fail Interrupt>
VBISIRQ	<VMEbus IRQ Request Acknowledge Interrupt>
VXIRQ	<VSB Interrupt>

Group 1 Interrupts

IRQ7-1	<VMEbus Interrupts>

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Table 3. Status Register Format

<STAT0>

31	Front Panel Switch Selectable						24
MODE	AMSEL	SO	GPC	GPB	GPA	GP9	GP8

<STAT1>

23	Front Panel Switch Selectable						16
GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0
← Provides VME130 Networking Base Address →							
← and useful as general purpose status →							

<STAT2>

15	Power Up Reset Condition: "1"						08
**	**	ABORT	SYSFAIL	VBERR	VXBERR	MMUBERR	LBTO
				BERR Source Status Register			

(**denotes: unimplemented — always read as "1").

MODE, AMSEL	<Power Up VMEbus Mode>	VBERR	<VMEbus BERR Flag>
SC	<VMEbus System Controller>	VXBERR	<VSB BERR Flag>
GPC-GP0	<General Purpose User Status Bits>	MMUBERR	<MMU BERR Flag>
ABORT	<Abort Pushbutton Status>	LBTO	<Local Bus Timeout BERR Flag>
SYSFAIL	<VMEbus System Failure Flag>		

Table 4. Control Register Format

<CNT0>

31	Power Up Reset Condition: "1"						24
VBV7	VBV6	VBV5	VBV4	VBV3	VBV2	VBV1	VBV0
← VMEbus IRQ Vector →							
← Port A on the Z8036 Timer →							

<CNT1>

31	Power Up Reset Condition: "1"						24
MPIRQ	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
← Port B on the Z8036 Timer →							

<CNT2>

31	Power Up Reset Condition: "1"						24
VBIMSK7	VBIMSK6	VBIMSK5	VBIMSK4	VBIMSK3	VBIMSK2	VBIMSK1	VBISMSK
← which VMEbus IRQ's this Interrupt Handler responds to →							

<CNT3>

23	Power Up Reset Condition: "0"						16
Reserved	ALLIEN	SYSFIEN	Reserved	IL2	IL1	IL0	Reserved
← Interrupt Enables →				← VME IRQ Request Level, Status →			

<CNT4>

15	Power Up Reset Condition: "1"						08
Reserved	Reserved	Reserved	32/24	Reserved	Reserved	Reserved	Reserved

<CNT5>

07	Power Up Reset Condition: "1"						00
PMEN	VXDIS	VXRR	VXDEN	UXIRQ	32/24	32/16	BDFAIL

VBV7-VBV0	<VMEbus IRQ Vector Number Register>	VXDIS	<VSB Disable>
MPIRQ	<Multi-Processor Interrupt Request>	VXRR	<VSB Read Only Mode>
VBIMSK7-1	<VMEbus Interrupt Masks>	VXDEN	<VSB Decode Enable>
VBISMSK	<VMEbus Interrupt Status IRQ Mask>	VXIRQ	<VSB Interrupt Request>
ALLIEN	<All IRQ Enable>	32/24	<VMEbus Address Size>
SYSFIEN	<SYSFAIL IRQ Enable>	32/16	<VMEbus Data Bus Width>
IL2–IL0	<VMEbus IRQ Request Level>	BDFAIL	<Board of System Failure>

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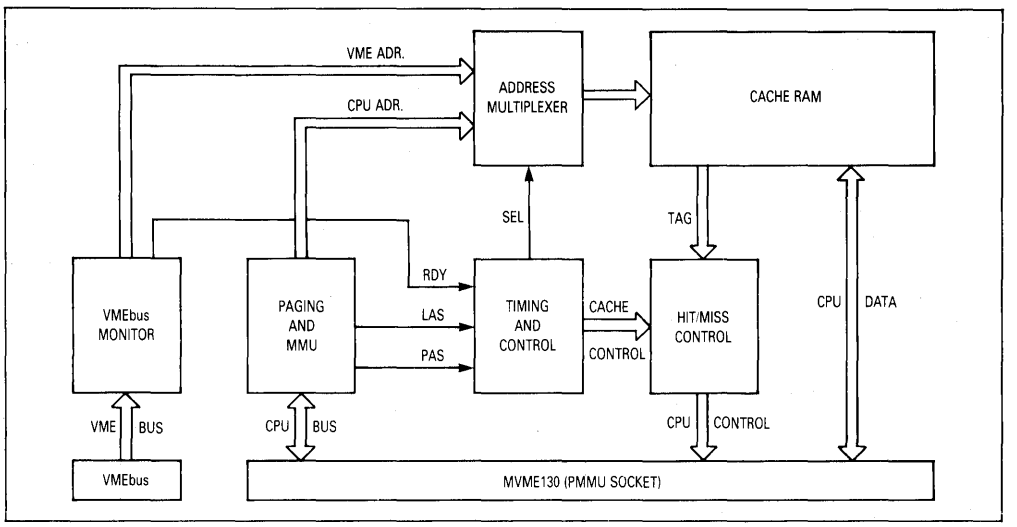


Figure 3. MVMEXTCAC Functional Block Diagram

THE CACHE ACCELERATOR MODULE

The Cache Accelerator Module (MVMEXTCAC), normally an independent product of the Motorola VME-module Family, is plugged into the MMU socket of the MVME130 Microcomputer Module and becomes an intregral part of the Assembly. Its function is to accelerate the performance of MC68020-based systems without modification of existing programs. The degree to which this objective is being achieved is indicated by the results of the two benchmark programs tabulated in Table 5. The first of these utilized EDN benchmarks[2] which perform commonly used character and data manipulations; the second utilized user-supplied routines performing data intensive array operations. The tests, run for four combinations of cache memory utilization, indicate the degree of improvement attributable to the use of the Cache Accelerator.

Table 5. Performance Test Results

Test	No Cache	MC68020 Cache	MVMEXTCAC Cache	MC68020 and MVMEXTCAC Cache
EDN-E (Char. String Search)	285	141	131	99 μs
EDN-F (Set/Reset/Test Bit)	60	36	33	30 μs
EDN-H (Link List Insertion)	121	194	70	70 μs
EDN-I (Quicksort)	22,320	11,792	11,072	9001 μs
EDN-K (Bit Matrix Translation)	243	173	159	136 μs
CUSTOMER BENCHMARK	125	104	73	68 sec.

2. EDN — September 16, 1981

The Accelerator is a single-set, direct-mapped cache comprising 16Kb of high-speed static memory, organized as 4K, 32-bit data entries. Each entry replicates a 32-bit word located in memory across the VMEbus or VSB memory space, and is updated concurrently with a processor write-access or initial read-access. Any combination of bytes from an access can be cached at a time, and a data-fill function implemented for VSB enables the caching of the entire 32-bit entry for byte- and word-read operations. The Accelerator caches both program and data transactions throughout, and it can be configured, by function code, to cache any combination of supervisor program, supervisor data, user program and user data mode accesses.

An onboard Monitor automatically cleanses the cache of stale data and enables the Cache Accelerator to operate in both single and multiprocessor environments without software intervention.

The Cache Accelerator Module supports any speed MC68020 microprocessor, and is jumper selectable to support either the MC68851 Memory Management Unit or M68KVMMB851 Memory Management Board, or an MMU bypass board if the MMU function is not required. With an MMU installed, the page detection circuitry on the cache enables its RAMs to operate in parallel with the MMU address translation RAMs to maximize system performance. A cache page is defined by the physical address bits PA08–PA13, and if they remain the same on a following cycle, then the address access time of the cache RAMs is buried in the MMU address translation period. With a bypass board installed, the cache receives the address signals directly from the MC68020 microprocessor and zero wait-state operation is obtainable. Zero wait-state operation is achieved at a processor frequency of

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12.5 MHz[3], and it may be achieved at 16.67 MHz when faster static RAMs become available.

The Cache Accelerator provides direct access to the cache RAMs for diagnostic and inquiry purposes, and provides a test mode of operation to establish general system confidence.

MEMORY ORGANIZATION

The complete memory section of the Cache Accelerator is organized as 4K entries of 55 bits per entry (see Table 6). It consists of a "Tag Section" and a "Data Section," where the tag section stores the physical addresses of the off-board memory locations, and the data section stores the data residing at those locations. The lower address bits (PA02–PA13) form an "index" that directly addresses the cache RAMs to select the particular entry to be used, and the remaining address bits (PA14–PA31) are stored and read from the tag RAMs as data. An Address Valid bit (AV) is generated internally for each entry to indicate that the address stored in the Tag is valid information. It may not be valid either because the tag entry has not been written to since power-up or since the cache was last cleared, or because the VMEbus Monitor has set the entry invalid. The data RAMs contain the corresponding bytes that were cached from the bus, and the four Byte-Valid bits (BV0–BV3) are generated internally to qualify those bytes. BV0 is associated with byte address 0 of the long-word entry, and operates on the most significant byte of the data bus, D31–D24. The other Byte-Valid bits operate in sequence.

BASIC CACHE OPERATION

When the processor drives an address for a read operation, the index section PA02–13 addresses the tag and data RAMs to select one entry from the cache. The remaining address bits from the processor are then compared to the corresponding address bits read from the tag section of that entry. If they match, and the Address-Valid bit is set, and if the Byte-Valid bits for the bytes the processor is requesting also match, then the cycle "hits" and the cache supplies the requested data to the processor and terminates the cycle. If any event does not match, then the cycle "misses" and a VME or VSB bus access is initiated, the cache entry is updated with the new address and data information, and the Valid bits are set appropriately. Note that a write cycle will always cause a miss since the processor, and not the cache, is supplying the data. Several other factors determine the hit qualification and cacheability of a processor cycle. These include the control bits, the type of processor cycle, the MMU cache enable signal and the onboard address decoder.

VMEbus MONITOR

The VMEbus Monitor is a separate machine on the Cache Accelerator that operates asynchronously with the processor to prevent "stale" data from remaining in the cache. It operates automatically so that the host user benefits from the performance advantages offered by the cache without even being aware that the Cache Accelerator has been installed in the system.

Stale data could occur in the cache when other VMEbus masters modify data in main memory which was previously cached. To prevent this, the Bus Monitor has a two-level FIFO register stack which captures the addresses of write operations initiated by bus masters other than the host, and presents the addresses to the cache for processing. The cache services the monitor by comparing the captured address with the corresponding entry in its tag memory. If the tag is Valid and compares, a "monitor hit" occurs and the cache invalidates the entry by resetting its Address Valid bit. If the processor then accesses that physical address, the cache will miss because of the reset Address Valid bit, and the cycle will be routed out to main memory for the new data to update the invalid entry.

USER INTERFACE

The user interface in Table 7 shows the devices on the Cache Accelerator used to control and diagnose its operation. These are Cache Control and Mask Registers, and two hard-decoded address spaces used to directly access the cache RAMs for diagnostic and inquiry purposes. The cache powers-up in a cleared and disabled state, and can be enabled for software transparent operation by storing an "F1" to the Cache Control Register. In addition, the cache can be tested or configured for a specific user application through the various control bits shown. Since the entire user interface address space can safely be accessed with or without the Cache Accelerator installed, a cache utility can be implemented without prior knowledge of its presence in the system.

MEMORY MANAGEMENT BOARD

The M68KVMMB851 Memory Management Board, Figure 4, is an interim solution for implementing demand-paged virtual memory operations prior to the availability of the MC68851 single-chip Paged Memory Management Unit. It provides the required logical to physical address translation by performing chip-controlled searching of translation tables in main memory.

The 4.5" x 3.5" mezzanine board plugs into a socket of the 131XT board which is reserved for the MC68851 chip. It contains an MC68461 Memory Management Controller and an external Address Translation Cache. The Controller contains address translation circuitry and a state machine which, together, execute the table walking algorithm of the MC68851. The Address Translation Cache, a 512-entry set associative cache, is a fast memory that translates logical addresses and function codes to corresponding physical addresses and protection bits. It speeds address translation by avoiding the overhead of searching translation tables for each bus access.

The functional differences between the MC68851 PMMU and the MMB are detailed in Table 8. The MMB requires an addition to the supervisor's bus error handler to allow the use of indivisible memory cycles (i.e. the TAS instruction). The MMB must use the bus error signal to inform the MC68020 microprocessor that the address of this indivisible cycle is not resident in the address translation cache. When the MC68020 takes the bus error signal, the MMB is allowed to request the bus and to perform

3. With MMU bypass card installed and dependent on MC68020 clock to address strobe timing.

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the necessary address translation table walk. The MC68020 then proceeds to the bus error routine where software must perform an instruction retry to the indivisible cycle.

Functionally, the MMB is compatible with the MC68851 PMMU to the extent that algorithms and programs developed for a system using the MMB can be moved to one using the MC68851 after a few minor changes.

Table 6. MVMEXTCAC — Memory Organization

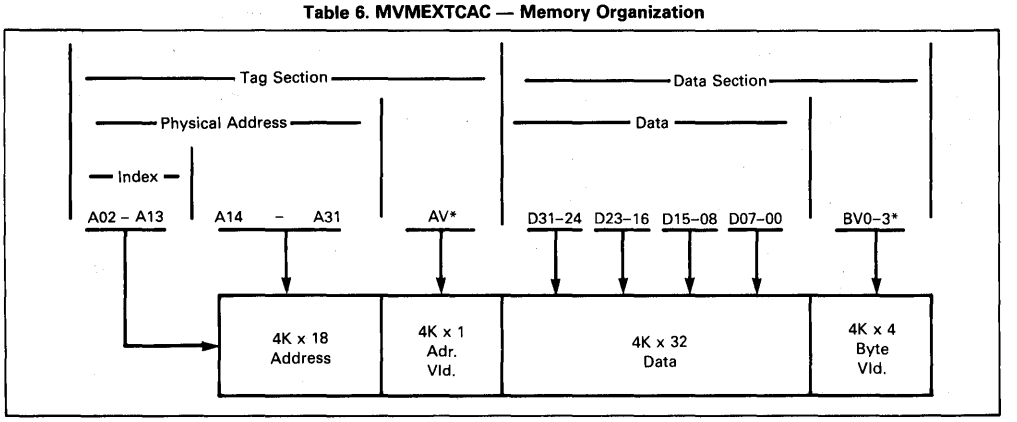


Table 7. MVMEXTCAC — User Interface

Cache Control Register — Address FFFC0000

D31 (Reset State = FF)							D24
VBCEN	MONEN	MLBK	MBLC	CCLR	CWEN	CREN	CTST

Mask Register — Address FFFC0001

D23 (Reset State = xF)							D16
X	X	X	X	MSD	MSP	MUD	MUP

Data Access Space — Address FFFD000–FFFD3FFC
Data Entries, 000–FFF

D31			D00
BYTE0 D31–D24	BYTE1 D23–D16	BYTE2 D15–D08	BYTE3 D07–D00
.	.	.	.
.	.	.	.
.	.	.	.

Tag Access Space (read-only)
Addresses — FFFE0000–FFFE3FFC
Tag Entries, 000–FFF

D31	D14	D07	D03–D00
PAD31–PAD14	NA	AV	BV0–BV3
.	.	.	.
.	.	.	.
.	.	.	.

DEFINITIONS

VBCEN	—	VMEbus Cache Enable
MONEN	—	VMEbus Monitor Enable
MLBK	—	Monitor Loopback (for diagnostic use)
MBLC	—	Monitor Block (for diagnostic use)
CCLR	—	Cache Clear
CWEN	—	Cache Write Enable
CREN	—	Cache Read Enable
CTST	—	Cache Test (for diagnostic use)
MSD	—	Mask Supervisor Data
MSP	—	Mask Supervisor Program
MUD	—	Mask User Data
MUP	—	Mask User Program
AV	—	Address Valid Status
BV0	—	Byte Valid Status for D31–D24 (byte address 0)
BV1	—	Byte Valid State for D23–D16 (byte address 1)
BV2	—	Byte Valid Status for D15–D08 (byte address 2)
BV3	—	Byte Valid Status for D07–D00 (byte address 3)

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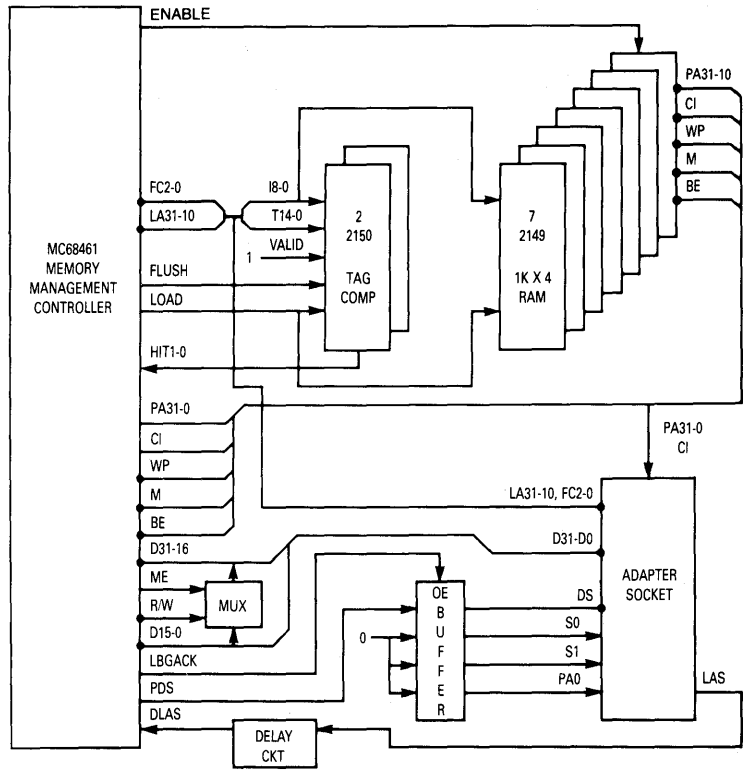


Figure 4. M68KVMMB851 Memory Management Board

Table 8. Functional Differences Between Chip and Board

Feature	MC68851 PMMU	MC68KVMMB851 Boards
Address Translation Cache	Internal, Fully Associative	External, Set Associative
Page Size	256, 512, 1K, 2K, 4K, 8K, 16K & 32Kb	1Kb
Logical Address Support	From 17 to 32 Bits	24- or 32-Bit
Supports Multiple Logical Bus Masters	Yes	No
Logical and Physical Bus Arbitration Support	Yes	Yes, But Not Identical to the MC68851
Access Level Support	Yes	Does Not Support Supervisor Root Pointer, Root Pointer Cache or DMA Root Pointer
Coprocessor Interface Support	Yes	No, Operations are Performed by Accessing Memory Mapped Locations
Translation Table Configuration	Supports Several	Expects One Given Table Walking Algorithm
Translates CPU Space Accesses	Yes	No, Acts as Peripheral Only
Pin-out	—	Compatible with MC68851

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MECHANICAL AND ENVIRONMENTAL SPECIFICATIONS

Characteristic	Specification
Cache Implementation	Single-set, direct mapped, physical
Memory Organization	4K, 32-bit data entries
Replacement Algorithm	Single entry, write-through
Hit Timing, LAS to DSACKx	No MMU — 60 nanoseconds With MMU — 70 nanoseconds (Page Hit) — 130 nanoseconds (Page Miss)
Power Requirements MVME130XT MVME131XT	 +5 Vdc, 9.3 A typ, 12.4 A max +5 Vdc, 10.3 A typ, 13.4 A max +12 Vdc, 250 mA max −12 Vdc, 250 mA max
Clock Signal	16.67 MHz clock frequency
Addressing Total System Size ROM/EPROM/RAM	 4 Gigabytes (32-bit addressing) Four 28-pin sockets for 16/32/64Kb devices using +5 Vdc only.
Operating Temperature	0° to 50°C
Storage Temperature	−40° to 85°C
Relative Humidity	5% to 95% (non-condensing)
Physical Characteristics Height Width Thickness (MVME130XT) (MVME131XT)	 6.30 in (16.00 cm) 9.19 in (23.34 cm) 1.438 in (3.652 cm) 2.238 in (5.684 cm)
Component Projections Component Side Solder Side	 0.50 in (1.27 cm) max 0.067 in (0.17 cm) max (except for interconnect header)

ORDERING INFORMATION

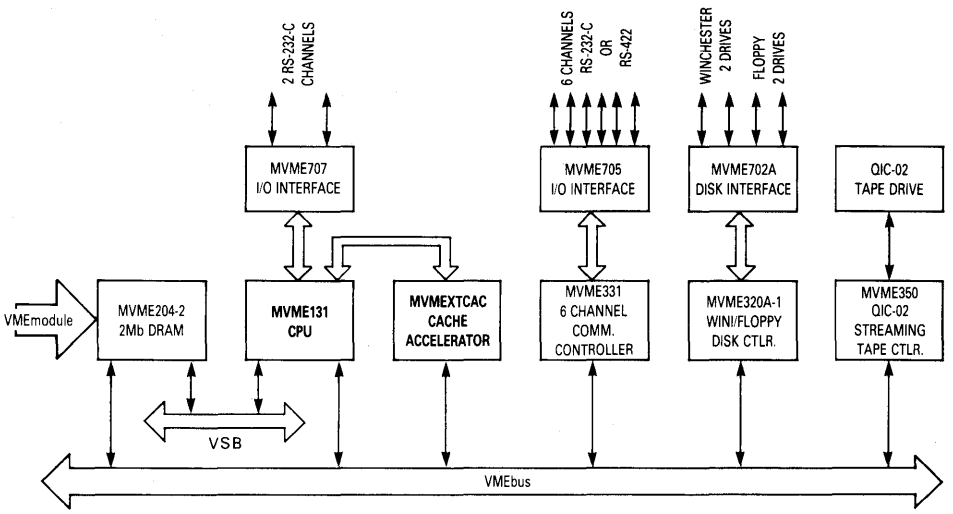
Part Number	Description
MVME130XT	VMEmodule 32-Bit Monoboard Microcomputer with 16.67 MHz MC68020 CPU and MC68881 Floating Point Coprocessor, MVMEXTCAC-1 Cache Accelerator Module and MVME130bug Debug/Diagnostic Monitor. Includes set of User's Manuals.
MVME131XT	VMEmodule 32-Bit Monoboard Microcomputer with 16.67 MHz MC68020 CPU, MC68881 Floating Point Coprocessor, MVMEXTCAC-2 Cache Accelerator Module with Memory Management Unit and MVME130bug Debug/Diagnostic Monitor. Includes set of User's Manuals.
MVME130XT/D	User's Manual Set for MVME130XT.
MVME131XT/D	User's Manual Set for MVME131XT.
MVME130BUG/D	130bug Debug/Diagnostic Monitor User's Manual.

RELATED DOCUMENTATION

Part Number	Description
MVME204-1	VMEmodule 1024Kb Dynamic RAM with Byte Parity and VSB. Includes User's Manual.
MVME204-2	VMEmodule 2048Kb Dynamic RAM with Byte Parity and VSB. Includes User's Manual.
MVME214	VMEmodule Static RAM/ROM with VSB and up to 1Mb RAM capacity. Includes User's Manual.
MVME707	Dual RS-232-C Serial I/O Cable Assembly. Includes User's Manual.

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The VMEsystem



A Typical High-Speed MVME130/131XT Microcomputer VMEsystem

The MVME131XT 32-Bit Microcomputer with Cache Accelerator Module conforms to the VMEbus interconnect system which has emerged as a world-wide Standard for 8-/6-/32-bit microcomputers. It is part of the VMEmodule product family whose M68000-based processing power, Eurocard mechanical format, powerful VERSAdos real-time software support and international multiple sourcing have made it one of the most popular product lines in the industry.

The VMEsystem architecture, and a board-level component complement that relate to the Cache Accelerator, are illustrated in the above block diagram. Of particular significance are:

- The well-established functional versatility of the VMEbus whose non-proprietary technical specification is widely used for system implementation
- An auxiliary VSB for high-speed memory expansion
- An MC68020-based, 32-bit CPU board (MVME131) utilizing the latest advances in microprocessor design
- A large repertoire of peripheral (controller) modules and memory boards

The unrivalled acceptance of the VMEsystem philosophy has yielded a selection of compatible board-level products from well over a hundred vendors, to offer systems manufacturers the basic tools with which to implement their designs quickly, efficiently, reliably and cost effectively.

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