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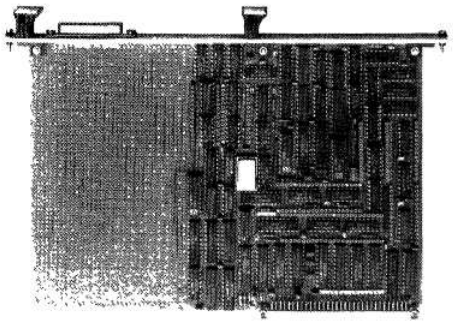
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MVME310

VMEmodule Intelligent Controller for Custom Interfacing



- Based on MC68121 Intelligent Peripheral Controller
- Standalone debugger supporting:
  - — Four Channel DMA Controller
  - — Interrupt Controller
  - — Serial download from host
  - — Checksum self test
- Large Wirewrap Area (3.5" x 6.3") for Prototype Construction
- Local Bus Interface Signals Available at Header Locations
- Serial Port Connector
- Two Sockets Expandable to Four for up to 32K Bytes Dual Ported RAM Buffer, 4K Bytes Static RAM Supplied
- Two sockets for up to 16K Bytes Program ROM/PROM. One Socket Static RAM Configurable
- Double Eurocard Form Factor
- VMEbus Compatible
- 0°C–70°C Operating Temperature Range

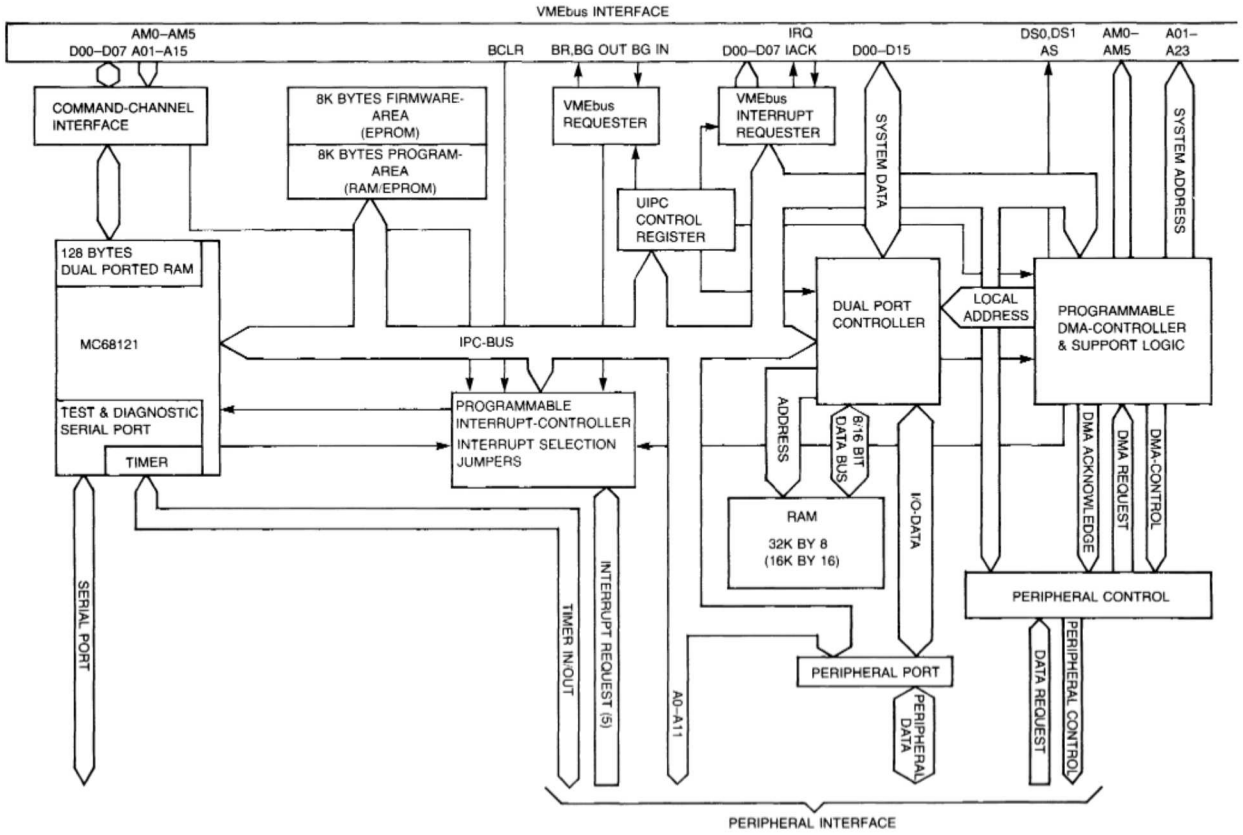
The MVME310 is a double high Eurocard module which is used for developing the prototype for a custom interface to a VMEbus peripheral. It provides a large wirewrap area, has interrupt and DMA controller devices and, to facilitate development of executive firmware, is based on the MC68121 Intelligent Peripheral Controller.

MVME310 provides two sockets for 16K of byte wide, dual ported static RAM buffer (4K bytes are supplied and two additional sockets in the user area can be used for buffer expansion) and two sockets for up to 32K bytes of user program in ROM/PROM. One of these sockets is configurable for 8K bytes of static RAM. One PROM socket contains the 4K byte standalone debugger — IPCbug. A serial port connector is also provided. Figure 1 is a block diagram of MVME310.

One example of the kinds of interfaces that can be implemented using as a basis MVME310 with IPCbug is found in the MVME315 Intelligent Floppy Controller/SASI Interface This module expanded the basic MC68121 functions into a universal intelligent peripheral controller (UIPC) function which provided a means of implementing an interface using a standard protocol for host/MVME315 communications and for development of control firmware. The control programs for the UIPC, the floppy disk controller, and the SASI interface are contained in two 8K PROMS on MVME315.

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FIGURE 1 — MVME310 Functional Block Diagram



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PERIPHERAL INTERFACE SUPPORT

The MVME310 offers the user the basic hardware facilities for implementing one or more peripheral interfaces and for developing the required control firmware. Access to the local bus is provided by a dual 28-pin row of plated through holes for mounting two headers. Bus signals available at the header locations are listed in Table 1A and Table 1B.

To accomodate the timing requirements of the various available interface chips, the MVME310 has a programmable logic array which, with additional user-supplied hardware, can be used to adjust the timing of the accesses from the on-board IPC.

TABLE 1A — Header Position K4 Hole Assignments and Signal Names

Pin Number	Signal Name	Pin Number	Signal Name
1	LATCH*	15	DREQ3*
2	NOT USED	16	DACK1
3	(2XE)	17	DACK3
4	NOT USED	18	IA1
5	TOUT	19	IA3
6	IPCRW	20	IA5
7	NOT USED	21	IA7
8	PRD*	22	IA9
9	AIOEN*	23	IA11
10	IIRQ4*	24	I/O1
11	IIRQ6*	25	I/O3
12	(TXC)	26	I/O5
13	DREQ0*	27	I/O7
14	DREQ2*	28	+5.0 Vdc

TABLE 1B — Header Position K5 Hole Assignments and Signal Names

Pin Number	Signal Name	Pin Number	Signal Name
1	DACK0*	15	−12 Vdc
2	DACK2*	16	I/ODMA
3	IA0	17	NOT USED
4	IA2	18	NOT USED
5	IA4	19	TIN
6	IA6	20	E
7	IA8	21	SRESET*
8	IA10	22	PWR*
9	I/O0	23	IDEN*
10	I/O2	24	IIRQ1*
11	I/O4	25	IIRQ5*
12	I/O6	26	IIRQ7*
13	GND	27	PREADY
14	+12 Vdc	28	DREQ1*

DMA SUPPORT

For DMA capability, MVME310 has an AMD Multimode DMA Controller-AM9517-5. This device has four independent DMA channels each with separate registers. To facilitate the development of control firmware, IPCbug offers three commands: DMA Controller Status Display (DS); DMA Control Register Modify (DM); and Initiate and Execute DMA transfer (DX). Provided RAM and available sockets are sufficient for a buffer to accomodate differences in VMEbus and peripheral data transfer rates.

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BUS REQUEST LEVEL SELECTION

The MVME310 has three headers for jumper selection of one of the four VMEbus request levels.

INTERRUPTER LEVEL SELECTION

The MVME310 has two headers for jumper selection of one of the seven VMEbus interrupt priority levels.

ENABLING THE SYSTEM FAIL FUNCTION

The MVME310 has a header for jumper connection of the board fail timer circuit to the VMEbus SYSFAIL* line.

DATA AND PROGRAM MEMORY DEVICE SIZE AND TYPE SELECTION

The MVME310 has five headers by means of which four data and program memory sockets are jumper configured for the supported memory device sizes and types. Two headers provide for jumper configuration of the two dual ported local RAM sockets for 2K x 8 or 8K x 8 devices. This also configures the two data memory socket locations in the user wirewrap area. Three headers allow jumper configuration of the program memory sockets. Two of these are used for jumper configuration of the low program memory block for 2K, 4K or 8K ROM devices. The other header is used for configuring the high program memory block for a 2K, 4K or 8K RAM/ROM device.

Interrupt Source Selection

Five signals are brought directly to the on-board interrupt controller from the peripheral interface. The MVME310 also has a header for jumper connection to the on-board interrupt controller of two additional interrupt sources. These can be selected from the VMEbus signals BCLR*, IRQ6* and IRQ7* and the local signal IPCWR*.

Base Address Selection

For command channel accesses, the MVME310 has a header for jumper selection of a base address. This can be set on any 512 byte boundary throughout the 65,536 byte VMEbus short I/O address space.

Serial Communications

The MVME310 has a 25-pin sub-D female connector for implementing a serial data function in order to connect a terminal. Firmware support for a serial function is provided by the LO command of IPCbug which provides download from a host of a user program in Motorola S-Record format.

Users can provide their own serial communications firmware using the support offered by the on-board MC68121 microcomputer for full duplex, asynchronous communications. These are:

- The rate and mode control register
- The transmit/receive control and status register
- The transmit data register
- The receive data register

The basic data rate can be obtained from an external source or the 16-bit internal timer. Subsequently, operation at one of four baud rates is program selectable. Data format can be NRZ or bi-phase.

Usage

The MVME310 will operate as a slave in VMEbus systems having any of the listed bus masters:

MVME101 VMEmodule Monoboard Microcomputer
MCME110-1 VMEmodule Monoboard Microcomputer
MVME115 VMEmodule Monoboard Microcomputer

MVME310 SPECIFICATIONS

The specifications for the MVME310 are listed in Table 2.

TABLE 2 — MVME310 Specifications

Characteristic	Specification
Power Requirements	+5.0 Vdc ± 5% at 2.5 A (typical) +12 Vdc ± 5% −12 Vdc ± 5% at 2.5 A (typical)
Environmental Requirements Operating Temperature Storage Temperature Humidity Range	 0° to 70°C −55°C to +85°C 0% to 95% (non-condensing)
Mechanical Specifications Height x Depth (board) Height x Width (front panel)	 9.2" (234 mm) x 6.3" (160 mm) 10.3" (262 mm) x 0.79" (20 mm)
Connectors VMEbus Serial Connector	 D1N41612 C96 25-pin D-Subminiature

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Software Driver

For users desiring to write their own device driver, a manual, Guide to Writing Device Drivers for VERSAdos, M68DRVGD/D1, detailing how to write a driver that runs under the M68000 Real-time Multitasking kernel or under VERSAdos is available.

VMEbus Interface

The MVME310 has a VMEbus interface which decodes all address and address modifier lines and provides bus requester and bus interrupter functions.

VMEbus Connector P1

The electrical and mechanical characteristics of VMEbus connector P1 are fully described in the VMEbus Specification Manual MVMEBS/D1.

Serial Connector

The serial connector is a Sub-D female, TMC-5-3-25, or equivalent.

Ordering Information

Part Number	Description
MVME310	VMEmodule Intelligent Controller For Custom Interfacing. Includes User's Manual.
MVME310/D1	VMEmodule Intelligent Controller for Custom Interfacing User's Manual

Related Documentation

Part Number	Description
MVMEBS/D1	VMEbus Specification Manual
M68DRVGD/D1	Guide to Writing Device Drivers for VERSAdos
M68IPCS/D2	M68000/IPC Command Channel Software Interface Reference Manual

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