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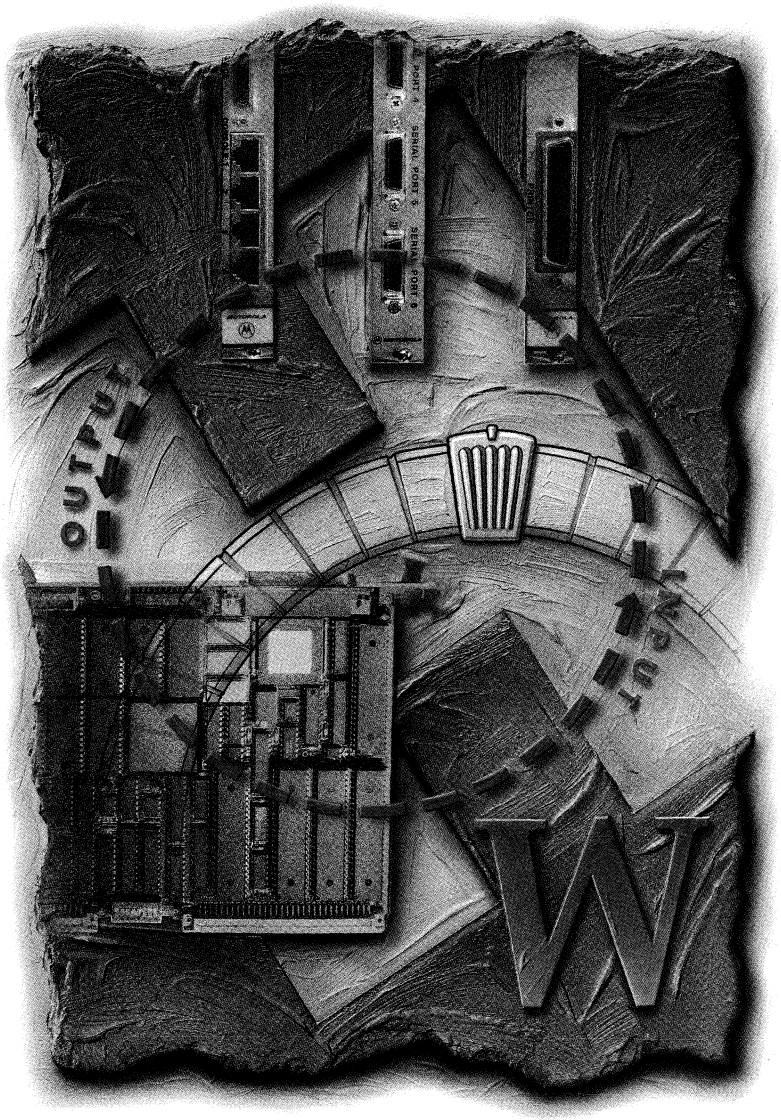
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MOTOROLA

MVME320B
VMEbus Disk Controller Module User's Manual

HARDWARE

MOTOROLA

MVME320B/D1

JANUARY 1988

MVME320B

VMEbus DISK CONTROLLER MODULE

USER'S MANUAL

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First Edition

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SAFETY SUMMARY
SAFETY DEPENDS ON YOU

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Motorola Inc. assumes no liability for the customer's failure to comply with these requirements. The safety precautions listed below represent warnings of certain dangers of which we are aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

GROUND THE INSTRUMENT.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. The equipment is supplied with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter, with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified maintenance personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

USE CAUTION WHEN EXPOSING OR HANDLING THE CRT.

Breakage of the Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the equipment. Handling of the CRT should be done only by qualified maintenance personnel using approved safety mask and gloves.

DO NOT SUBSTITUTE PARTS OR MODIFY EQUIPMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the equipment. Contact Motorola Field Service Division for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

WARNING

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

PREFACE

Unless otherwise specified, all address references are in hexadecimal throughout this manual.

An asterisk (*) following the signal name for signals which are level significant denotes that the signal is true or valid when the signal is low.

An asterisk (*) following the signal name for signals which are edge significant denotes that the actions initiated by that signal occur on a high to low transition.

Signal names in parentheses denote internal module (onboard) signals.

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CHAPTER 1 - GENERAL INFORMATION

1.1 INTRODUCTION

This manual describes the Motorola MVME320B Disk Controller Module (hereafter referred to as MVME320B), which interfaces with industry-standard 5-1/4 inch hard disk drives and floppy disk drives (5-1/4 inch and 8-inch). The manual includes a general description, hardware preparation and installation instructions, a functional description, operations information, and support information for the MVME320B.

1.2 MVME320 FAMILY DIFFERENCES

The original MVME320 and MVME320-1 Disk Controller modules were upgraded to the MVME320A and MVME320A-1. These have been upgraded to the MVME320B and MVME320B-1. The MVME320/320A/320B have front mount drive connectors for J1, J2, and J3. The MVME320-1/320A-1/320B-1 have side mount drive connectors, intended for cables to be routed to the rear of the module.

The MVME320 and MVME320-1 were intended for use with the MVME702 and MVME702A Transition boards when connecting to 5-1/4 inch floppy drives. The MVME320A/320A-1/320B/320B-1 have an additional 34-pin drive connector (J4) for direct connection to 5-1/4 inch floppy drives. These disk controller modules are compatible with the MVME702 and MVME702A, but, because of the new J4 connector, do not require an MVME702 or MVME702A Transition board in most applications.

The MVME320A and MVME320A-1 modules, compared to the MVME320/320-1, have revised firmware with additional features, including support for large capacity hard disk drives using up to 16 heads, and speed-enhanced firmware, with interleave factors up to 2:1. The board layout was also revised and provides an onboard clock as a substitute for SYSCLK.

The MVME320A/320A-1 may be substituted for the MVME320/320-1.

Additionally, the MVME320B/320B-1 modules, compared to the MVME320A/320A-1, have revised board layout and VMEbus interface. The firmware has been revised with software selection of speed/density, when using 5-1/4 inch dual density/speed drives connected to J4. These new drives, when operated in the high density/speed mode, operate with 8-inch floppy data rates and formats, but interface with the controller module as a standard 5-1/4 inch floppy disk drive. For these drives, provision has been made to connect the READY line via optional jumpers. Another jumper connects the speed/density control line.

The MVME320B/320B-1 may be substituted for the MVME320A/320A-1 or for the MVME320/320-1. Do not attempt to replace newer boards with the older versions.

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1.3 FEATURES

The features of the MVME320B include:

- Combined control for hard and floppy disk drives
- Supports MFM and FM recording
- Cylinder number: 8- or 16-bit
- Standard IBM formats
- Multiple-sector read/write
- Implied seek
- Error correction up to 11 bits
- 32-bit ECC code
- Serial data rate of 5 megabits/sec hard disk
- Serial data rates of 125/250/500 kilobits/sec floppy disk
- 8-bit register transfer, 16-bit DMA data transfer
- 24-bit host address and 6-bit address modifier
- VMEbus-compatible
- Supports drives with up to 16 heads
- Software selectable speed/density for 5-1/4 inch floppy disk drives

1.4 SPECIFICATIONS

The MVME320B is a VMEbus-compatible module. The specifications are given in Table 1-1.

TABLE 1-1. MVME320B Specifications

CHARACTERISTIC	SPECIFICATIONS
Physical characteristics	
Height	160 mm (6.299 inches)
Width	233.35 mm (9.187 inches)
Thickness	12.7 mm (0.5 inches)
Power requirements (at 25 degrees C and no drives connected)	3.9 A typical at +5 Vdc 60 mA typical at +12 Vdc <20 mA typical at -12 Vdc
Operating temperature	0 degrees C to 55 degrees C at point of entry of forced air (approximately 150 LFM)
Storage temperature	-40 degrees C to 85 degrees C max.
Relative humidity	0% to 90% (noncondensing)

TABLE 1-1. MVME320B Specifications (cont'd)

CHARACTERISTIC	SPECIFICATIONS
Serial data rate	5 megabits/second (hard disk) 125 kilobits/second (floppy disk) 250 kilobits/second (floppy disk) 500 kilobits/second (floppy disk)
Configuration	
DTB master	A24, D16
DTB slave	A16, D8
Requester	Release when done

1.4.1 Cooling Requirements

The Motorola MVME320B VMEmodule is specified, designed, and tested to operate reliably with an incoming air temperature range 0 degrees C to 55 degrees C (32 degrees to 131 degrees F) with forced air cooling at a velocity typically achievable by using a 71 CFM axial fan. Temperature qualification is performed in a standard Motorola VMEsystem 1000 chassis. Twenty-five watt load boards are inserted in two card slots, one on each side, adjacent to the board under test, to simulate a high power density system configuration. An assembly of three axial fans, rated at 71 CFM per fan, is placed directly under the VME card cage. The incoming air temperature is measured between the fan assembly and the card cage, where the incoming airstream first encounters the module under test. Test software is executed as the module is subjected to ambient temperature variations. Case temperatures of critical, high power density integrated circuits are monitored to ensure component vendors' specifications are not exceeded.

While the exact amount of airflow required for cooling depends on the ambient air temperature and the type, number, and location of boards and other heat sources, adequate cooling can usually be achieved with 10 CFM and 150 LFM flowing over the module. Less airflow is required to cool the module in environments having lower maximum ambients. Under more favorable thermal conditions, it may be possible to operate the module reliably at higher than 55 degrees C with increased airflow. It is important to note that there are several factors, in addition to the rated CFM of the air mover, which determine the actual volume and speed of air flowing over a module.

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1.4.2 FCC Compliance

This VMEmodule was tested in an FCC-compliant chassis, and meets the requirements for Class A equipment. FCC compliance was achieved under the following conditions:

a. Shielded cables on all external I/O ports.

b. Cable shields connected to earth ground via metal shell connectors bonded to a conductive module front panel.

c. Conductive chassis rails connected to earth ground. This provides the path for connecting shields to earth ground.

d. Front panel screws properly tightened.

e. Drives and cables to the MVME320B were internal to the chassis.

For minimum RF emissions, it is essential that the conditions above be implemented; failure to do so could compromise the FCC compliance of the equipment containing the module.

1.5 GENERAL DESCRIPTION

The MVME320B is a dual-height module that provides the traditional and advanced features required to control Winchester-type hard disk drives and floppy disk drives. It can control up to four disk drives (up to two hard disk drives or up to four floppy disk drives) in many combinations. The MVME711 Transition board (or equivalent) enables the use of four hard disk drives with the MVME320B.

The MVME320B supports single- and double-density (FM and MFM) recordings on floppy disk drives, and double-density (MFM) recording on hard disk drives.

- IBM 3740 single-density format (FM)
- IBM System 34 double-density format (MFM)
- Hard disk format

The controller is programmable using high-level commands over the VMEbus. The Direct Memory Access (DMA) data transfer on the host bus is 16-bit in parallel at one megabyte/second. The MVME320B is capable of handling serial data rates up to five megabits/second over the disk drive interface.

The disk interface consists of two sections:

- Input and output ports that sense and generate "slow changing" or static control signals.

- Serial data Input/Output (I/O) and high-speed disk control.

Because both sections are controlled by a fast internal microprocessor (8X305), the MVME320B is able to control a variety of different disk types and media formats.

The host system communicates with the MVME320B through Event Control Areas (ECAs) which reside in system memory. An ECA parameter block is set up for each disk drive (up to four) to be controlled. These areas contain information required by the MVME320B to execute disk commands. This information includes data about the requested command and the disk drive. DMA operations are defined by the ECA description of the command.

The MVME320B contains seven internal 8-bit registers. The host system requests an operation using these registers. Registers 1, 3, 5, and 7 are loaded with the 24-bit address (divided by 2) of the pointer to the ECA parameter block to be acted upon. Register 1 is the Least Significant Byte (LSB). After a command is accepted for execution, no further interaction between the host processor and the MVME320B need occur until the command is completed. For the register formats, see Figure 4-1.

The MVME320B microprogram uses the data contained in the ECA block to generate disk interface signals and perform the requested drive I/O. Data transfers to and from floppy disks are executed in real-time (with 2-byte buffering). Data transfers to and from Winchester drives are buffered on a sector basis.

The host is informed of completion of a command by an interrupt request signal from the MVME320B. The MVME320B writes the return status information to the appropriate ECA block memory. On interrupt service, the host reads the interrupt vector number from the internal vector number register on the data bus.

1.6 DRIVE COMPATIBILITY AND CAUTIONS

a. All ST506 and SA400 drives are not the same. Although designed to meet the ST506 and SA400 standard, all such drives are not identical, and the MVME320B may be sensitive to some of these differences. The user will need to independently qualify the drives to be used in an MVME320B system. When using 1.6Mb (unformatted) 5-1/4 inch drives in the high density mode, the user will also have to qualify the media. High density media is not usable in the low density mode.

b. The user should take care to comply with vendor environmental specifications for drives and media, and must be careful to lock out those sectors corresponding to media defects as identified by the drive vendor and the user's incoming inspection procedures.

c. The MVME320B supports interleave factors of up to 2:1. It is important to select the interleave factor that matches your system performance. It is suggested that you try several interleave factors to decide which one will give you the best performance from your system.

d. The MVME320B supports drives with up to four head selects.

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e. Disk drives which have power supplies separate from the MVME320B must not be powered up when the MVME320B is not powered up; power up these drives after the MVME320B is on, and remove the drive power before turning off the MVME320B.

f. Do not open or close the floppy disk drive door when the drive is selected, or about to be selected.

g. Do not power down the drive when the drive is selected, or about to be selected.

h. Remove the "READY" jumper, J15, when using drives which are not truly ready when this signal is asserted.

i. Floppy disk reads are not buffered; therefore, a heavily loaded VMEbus can cause floppy I/O not to complete. One suggested solution is to raise the priority of the MVME320B.

1.7 DUAL DENSITY PERFORMANCE CONSIDERATIONS

Each time that the drive speed is changed, the drive requires that a "speed change" time delay occur. At present, this delay is 1.25 seconds. Whenever the 320B firmware generates a change in floppy speed, such as when selecting another floppy to be run at a density different from the last floppy selected, or when changing density on a single floppy, the "speed change" time delay will be invoked. For multiple accesses to a floppy at the same density, no time delay is necessary, except for floppy drives which do not sense the pin 2 signal when not selected. THESE DRIVES ARE NOT SUPPORTED IN THE DUAL DENSITY MODE.

When copying from one density to the other, for best performance, the "speed change" time delay may be avoided by copying in large blocks, and not copying directly from floppy to floppy. Reading all the desired records into a buffer (memory or to hard disk) and then out to the floppy would invoke the "speed change" time delay only once. Repeated read/write operations between high and low speed floppies would invoke the time delay for each access to a floppy.

1.8 PROGRAMMING CAUTIONS

Users writing their own drivers should be aware of some functions that need to be handled in software:

NOTE

These functions have been implemented in Motorola's software drivers.

a. All hard disk media have defective areas which increase with the size of the drive. The user is responsible for determining, with the assistance of the disk drive vendor, the location of defective areas of the hard disk media, and through software, locking out these areas.

b. It is possible for the MVME320B to incorrectly return a Main Status Code of zero (no error). To be assured of a true "No Error" condition:

   . test Main Status for 00

   . test Extended Status for 00 00

   . for READ/WRITE operations, also verify that the return value of the bytes transferred equals bytes requested.

   . for READ operations, also verify ECC remainder equal to 00 00 (if using ECC).

c. Command Codes should be verified. The MVME320B ignores invalid codes; therefore, a driver waiting for an interrupt after an invalid code would wait indefinitely.

d. Verify the Buffer Address. A transfer to an address where no memory is installed may return with an incorrect "No Error" message.

e. Verify that the Cylinder Number is "in range." An invalid cylinder number causes the current command and the following command to fail.

f. Verify the Drive Type. An invalid drive type may cause the floppy to be erroneously selected.

g. Set the Main Status to "Busy" (Code = 07) when issuing commands, and then verify (or wait until) non-busy after the MVME320B returns an interrupt. The MVME320B sometimes interrupts before it updates the ECA.

   Busy code = 07 is not used by all drivers. Other codes such as 08 or FF, which will not be confused with an error condition, may be used. Code 07 is used by VERSAdos and is shown in "Main Status Codes," Table 5-1.

h. Re-try the Recalibrate command at least once if it returns an error (Main Status = 01; Extended Status = 2080). On large drives, it is possible for the Recalibrate to time-out before the head is "home."

i. Following a successful re-try, the Main Status is cleared, but the Extended Status still reflects the condition that forced the re-try.

j. Do not attempt to execute concurrent operations; this can generate problems.

k. Do three to five re-tries in the driver. Many command errors returned by the MVME320B are "soft" errors, meaning that the command may work correctly if tried again. Firmware re-tries, requested through the ECA table entry, only occur for Cycle Redundancy Check/Error Correction Code (CRC/ECC) errors and, occasionally, DMA over/underrun errors. The driver should initiate three to five re-tries for the following error codes:

1

Main/Extended Status	Description
01-0002 (NOTE)	CRC Error
01-0008 (NOTE)	Identifier not found
01-0080 (NOTE)	Positioning Error
01-0102	CRC/ECC Error
01-2080	Positioning Error/Data Point Time-out
09-8000	Throughput error on DMA operation

NOTE: Any combination of these error codes is possible; all other codes appear as shown.

l. Do not use the "Sector Out of Range" status bit in the Extended Status Word; it is not implemented. Only those status conditions listed in item "k" above and those listed below are implemented:

02-0010	Drive Not Ready (do not re-try)
06-0040	Write Protect Violation (do not re-try)
08-1800	Drive Not Available (do not re-try)
10-0800	Command Aborted by Driver

1.9 RELATED DOCUMENTATION

The following publications may provide additional helpful information. If not shipped with this product, they may be purchased from Motorola's Literature Distribution Center, 616 West 24th Street, Tempe, AZ 85282; telephone (602) 994-6561.

DOCUMENT TITLE	MOTOROLA PUBLICATION NUMBER
VMEbus Specification Manual	HB212/D
MVME702/MVME702A Disk Interface Module User's Manual	MVME702
MVME711 Transition Module User's Manual	MVME711

CHAPTER 2 - HARDWARE PREPARATION AND INSTALLATION INSTRUCTIONS

2.1 INTRODUCTION

This chapter provides unpacking instructions, hardware preparation, and installation instructions for the MVME320B.

2.2 UNPACKING INSTRUCTIONS

NOTE

If the shipping carton is damaged upon receipt,request carrier's agent be present during unpacking and inspection of equipment.

Unpack equipment from shipping carton. Refer to packing list and verify that all items are present. Save packing material for storing and reshipping of equipment.

2.3 HARDWARE PREPARATION

CAUTION

AVOID TOUCHING AREAS OF INTEGRATED CIRCUITRY; STATIC DISCHARGE CAN DAMAGE CIRCUITS.

The MVME320B contains the following jumper-selectable configuration options. The as-shipped factory jumper configurations are listed in Table 2-1. Header locations are shown in Figure 2-1.

TABLE 2-1. As-Shipped Jumper Configurations

HEADER	INITIAL FACTORY JUMPER PLACEMENT
J5	1-3, 2-4, 5-6, 7-8, 11-12
J6	1-2
J7	9-10
J8	2-3
J9	3-4, 9-10, 11-12
J10	2-3
J11	1-2, 3-4
J12	1-2
J13	2-3
J14	1-2
J15	1-2
J16	Not jumpered
J17	Not jumpered
J18	1-2

NOTE: J1, J2, J3, and J4 are cable connectors.

2

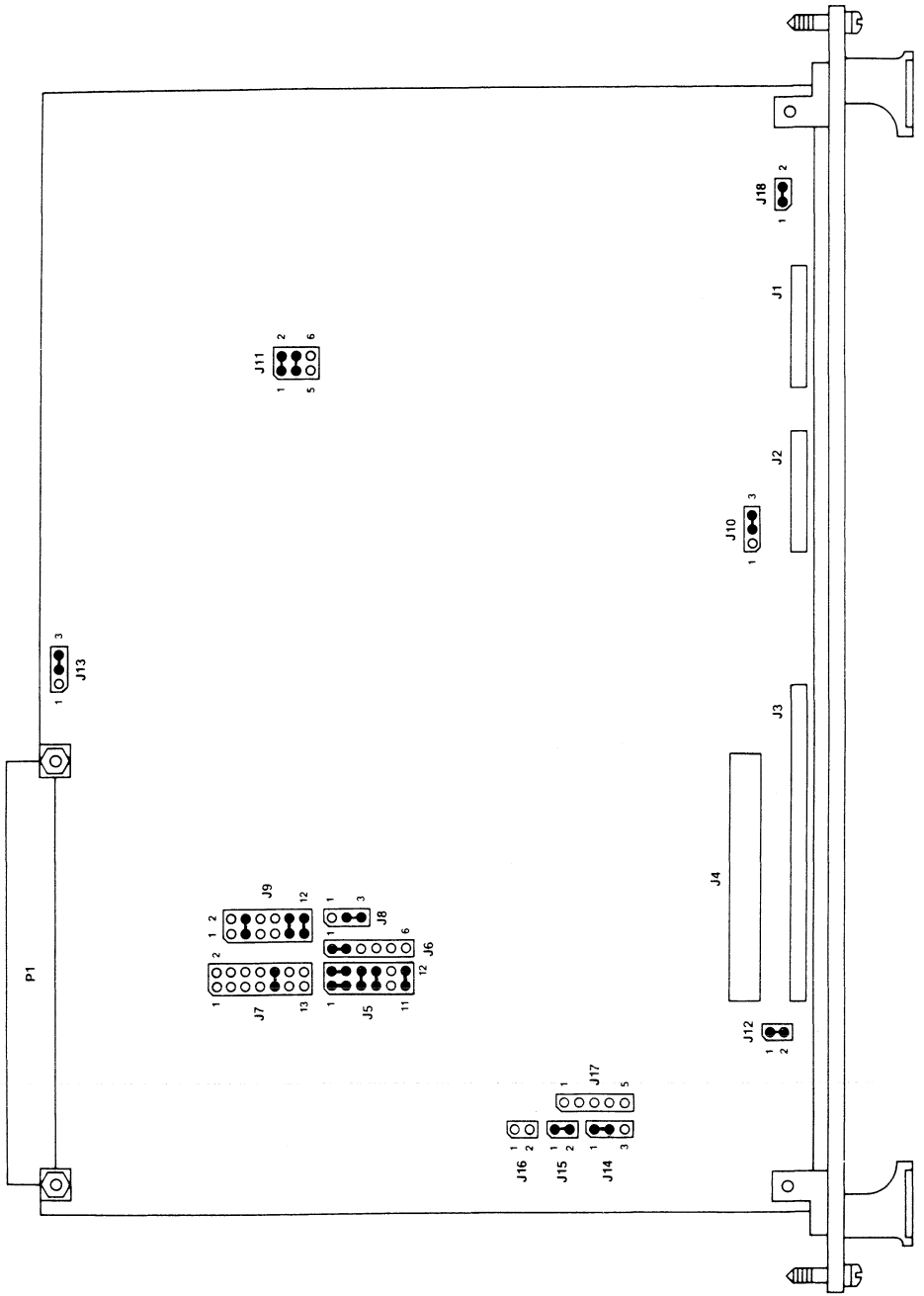
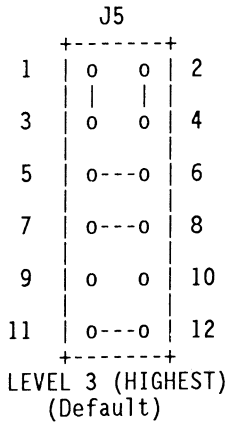
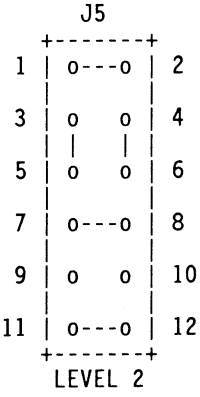


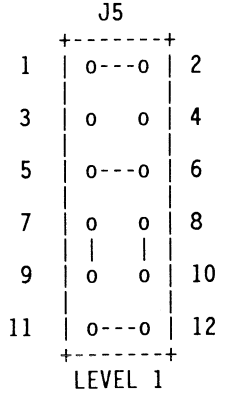
FIGURE 2-1. MVME320B Connector and Header Locations

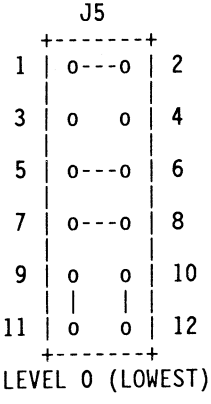
2.3.1 Bus Arbitration Level (J5 and J6)

Bus arbitration priority level is selected at headers J5 (BUS GRANT) and J6 (BUS REQUEST).

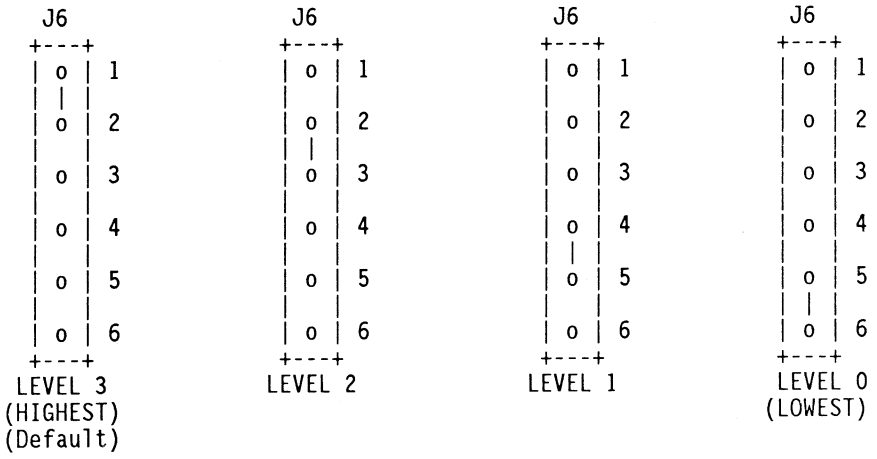








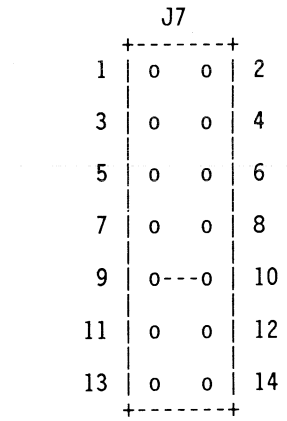
2



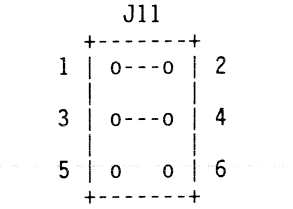
2.3.2 Interrupt Level (J7 and J11)

Interrupt level selection is accomplished at headers J7 (IRQ) and J11 (IACK). Please note that both IRQ and IACK must be set at the same interrupt level.

Interrupt Level		J7 (IRQ)	J11 (IACK)
(highest)	6	3-4	3-4, 5-6
	5	5-6	1-2, 5-6
	4	7-8	5-6
(default)	3	9-10	1-2, 3-4
	2	11-12	3-4
(lowest)	1	13-14	1-2



DEFAULT = IRQ LEVEL 3

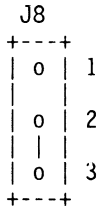


DEFAULT = IACK LEVEL 3

2.3.3 Address Modifier (J8)

The address modifier is selected at header J8.

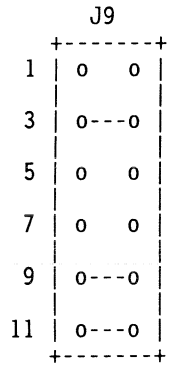
To Select Address Modifier	Indicating	Jumper Pins
29 or $2D	Short Non-privileged or Supervisor access	2-3 (DEFAULT)
only $2D	Short Supervisory access only	1-2



2.3.4 Address Decode (J9)

Address decoding is done at header J9, where jumper inserted = 0, no jumper = 1.

Address Bit	Pins
A10	11-12
A11	9-10
A12	7-8
A13	5-6
A14	3-4
A15	1-2



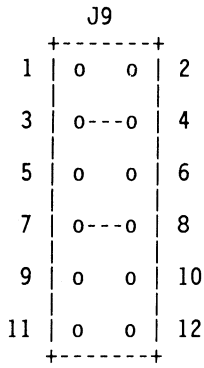
DEFAULT = 320 #1

Short I/O = $B000
A24 = $FFB000
A32 = $FFFFB000

2

Address Bit	Pins
A10	11-12
A11	9-10
A12	7-8
A13	5-6
A14	3-4
A15	1-2

J9

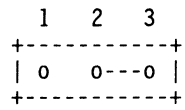


320 #2

Short I/O = $AC00
A24 = $FFAC00
A32 = $FFFFAC00

2.3.5 Reserved (J10)

J10

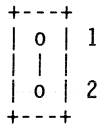


(Default)

2.3.6 PROM Enable (J12)

Pins 1-2 are jumpered with a removable jumper. This header can be used to disable the PROMs for factory test. (The PROMs are disabled if no jumper is installed.)

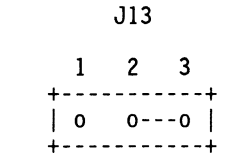
J12



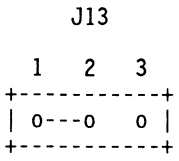
DEFAULT = ENABLED (1-2 JUMPERED)

2.3.7 Clock Select (J13)

This header is used to select onboard clock or the system clock (SYSCLK).



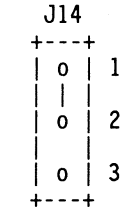
USES ONBOARD 16 MHz OSCILLATOR (Default)



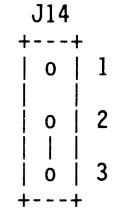
USES SYSCLK

2.3.8 PROM Size (J14)

PROM size is selected by J14. The user should not change the configuration.

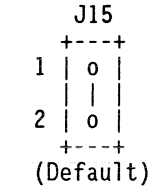


4K PROM (Default)



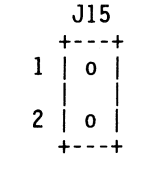
8K PROM

2.3.9 READY Line (J15)



(Default)

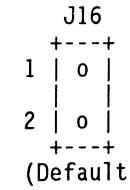
J4-34 is connected to J3-22 (READY line). (Used for floppy disk drives which are ready for access at READY true.)



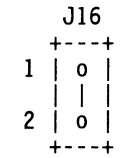
J4-34 is not connected. (Used for floppy disk drives which are not guaranteed to be ready for access at READY true, or for drives which have no READY line.)

2

2.3.10 J4-4 Option (IN USE/HEAD LOAD) (J16)

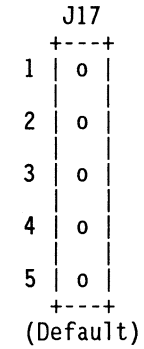


J4-4 defined as logic high by 1k ohm pullup resistor to +5 Vdc.

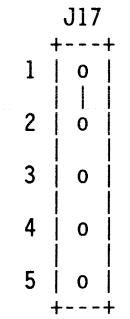


J4-4 defined as logic low by grounding at J16.

2.3.11 J4-2 Option (SPARE/DENSITY) (J17)

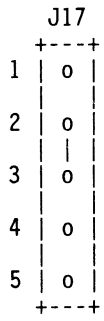


J4-2 is SPARE (n.c.)



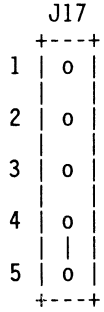
DENSITY

J4-2 is defined as logic high by 1k ohm pull-up resistor.



DENSITY

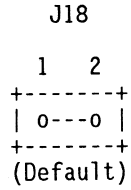
J4-2 is defined as logic low by grounding at J17.



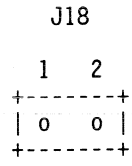
DENSITY

J4-2 is driven by firmware control register. Logic high for 8-inch ECA table; logic low for 5-1/4 inch ECA table, unless J18 jumper is removed.

2.3.12 Density Mode (J18)



J4-2 is high for 8-inch ECA table;
J4-2 is low for 5-1/4 inch ECA table.



J4-2 is low for 8-inch ECA table;
J4-2 is high for 5-1/4 inch ECA table.

2.4 MVME320B SOFTWARE SPEED CONTROL

To use 5-1/4 inch dual density floppy drives in the high density (1.6Mb, unformatted) and low density modes with the MVME320B and MVME320B-1, under software speed control, do the following:

a. On the MVME320B module, install a jumper on J17, pins 4 and 5, to connect DENSITY signal to J4, pin 2.

b. On the MVME320B module, install a jumper on J15, pins 1 and 2, to connect the READY line. Please note that if you are using a drive which asserts READY before the drive is at speed, DO NOT CONNECT JUMPER J15. The MVME320B will then ignore the READY, and assume READY after 1.25 seconds.

c. The drive must be appropriately jumpered for pin 2 control of DENSITY (speed): 300 R.P.M. = low density, 360 R.P.M = high density. The MVME320B, as shipped, uses pin 2 "high" for high density, and pin 2 "low" for low density. To reverse this, remove the jumper on J18 on the MVME320B.

d. The ECA table selects the density mode. Refer to Chapter 5 for more information on the ECA table.

   DRIVE TYPE, offset address $2E in the ECA table, defines the density.
   Drive types 0 and 1 are 8-inch floppy disks.
   Drive types 4 and 5 are 5-1/4 inch floppy disks.
   To select high density, set up an 8-inch floppy ECA table.
   To select low density, set up a 5-1/4 inch floppy ECA table.

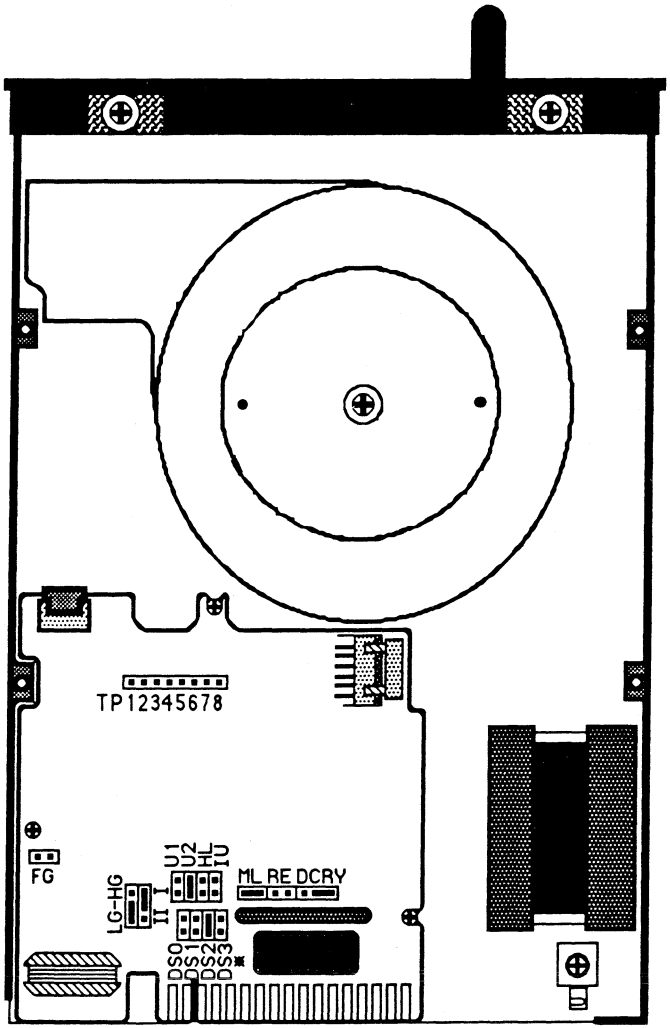
e. The high density mode requires media specially certified for this purpose. Normal media will not suffice. Note that high density media typically will not work in low density mode.

f. The 5-1/4 inch MOTOR ON (pin 16) is supported in both low and high density mode. Jumper the drive to enable the motor by the MOTOR ON signal (pin 16).

g. Since the MVME320B controls the MOTOR ON function, the drive need not have the HEAD LOAD function.

h. If the drive has a HEAD LOAD function, jumper it for HEAD LOAD at MOTOR ON. This avoids excessive "tap-tap" head loading wear on both media and heads.

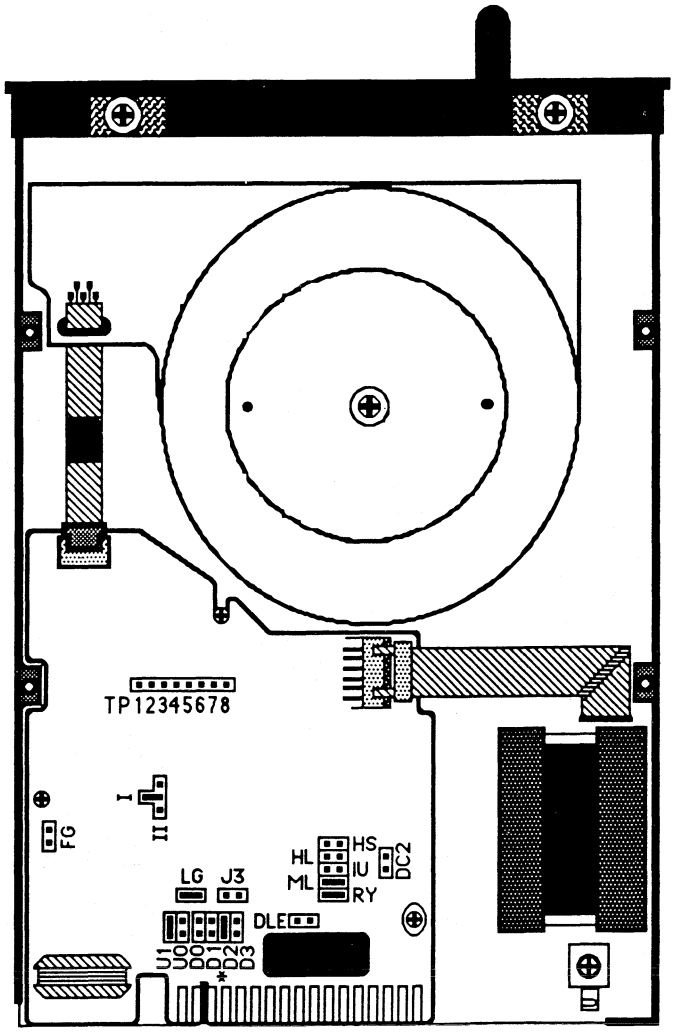
The following examples of disk drive configuration assume that the jumper on J18 on the MVME320B has been removed. TEAC drive FD-55GFV-17-V (Motorola part number 01-W0316B01) is configured as shown in Figure 2-2. TEAC drive FD-55GFR-606-U (Motorola part number 01-W0316B02) is configured as shown in Figure 2-3.



For software selection of speed/density, two jumper changes must be made on the MVME320B: the removal of the jumper on J18 and the installation of a jumper on pins 4-5 of J17 (refer to sections 2.3.11, 2.3.12, and 2.4.c).

FIGURE 2-2. TEAC Drive FD-55GFV-17-V (Motorola Number 01-W0316B01)

2



For software selection of speed/density, two jumper changes must be made on the MVME320B: the removal of the jumper on J18 and the installation of a jumper on pins 4-5 of J17 (refer to sections 2.3.11, 2.3.12, and 2.4.c).

FIGURE 2-3. TEAC Drive FD-55GFR-606-U (Motorola Number 01-W0316B02)

2.5 INSTALLATION CONSIDERATIONS

This section should be read and understood prior to installing the MVME320B.

WARNING

WHEN HANDLING OR TRANSPORTING THE MVME320B, CARE MUST BE TAKEN TO AVOID STATIC DISCHARGE DAMAGE TO THE INTEGRATED CIRCUITS ON THE MODULE. CONDUCTIVE MATERIALS SUCH AS ALUMINUM FOIL OR SPECIALLY TREATED FOAM IN CONTACT WITH THE SOLDER-SIDE SURFACE OF THE MODULE WILL BE ADEQUATE PROTECTION AGAINST SUCH POTENTIAL DAMAGE.

a. If you are using the MVME320B in a system which has one or more of the MVME204-series memory modules, please note the following:

   . model MVME204-1 must be at revision level F or later. (NOTE)
   . model MVME204-2 must be at revision level E or later. (NOTE)
   . model MVME204-2F must be at revision level C or later. (NOTE)
   . model MVME204 should not be used.

   NOTE: The revision level refers to the matrix revision, not the PCB revision. The matrix revision level is located to the right of the 01-W*xxxx*B*xx* number on the module.

b. Be sure that socketed IC's are fully seated in their sockets.

c. Make sure that adequate cooling is provided so that an ambient temperature of 55 degrees C will not be exceeded.

d. Ensure that the specifications outlined in paragraph 1.3 of this manual can be handled by the user's system.

e. Provide adequate grounding. It is important that the chassis ground is interconnected (e.g., drives, enclosure), and wired to the signal ground in one place only, typically at the power supply.

f. Plug in the MVME320B making sure that it is fully seated in its connector.

CAUTION

THE MVME320B SHOULD NEVER BE REMOVED OR INSERTED WHILE POWER IS ON OR DAMAGE TO THIS UNIT MAY RESULT.

2.6 CABLING

System configurations, floppy disk cabling, and examples of termination are presented in the following sections.

2

2.6.1 System Configurations

A maximum of four drives can be attached to the MVME320B at one time; they may be a mixture of hard and floppy drives, with certain restrictions.

All drives connected to the MVME320B must be soft-sectored.

The MVME320B supports 5-1/4 inch hard disks and single- and double-sided, single- and double-density floppy disks.

Up to two 5-1/4 inch hard disks may be attached to the MVME320B, unless the MVME711 is used, which allows up to four 5-1/4 inch hard disk to be used.

Connector J3 is the 50-pin header-type that connects drives in a daisy-chain configuration, as shown in Figure 2-2. This connector carries control and data information for the floppy disk drives and control information only for the hard disk drives. Maximum cable length should not exceed 10 feet (3 m). If using the MVME320B with the MVME702 or MVME711, refer to the appropriate user's manual for cable interface.

If using double-sided floppy drives on J3, isolate the "two-sided" status bit from the cable. Refer to the data reference sheet covering the drive.

Connector J4 is equivalent to J3 or J10 on an MVME702 and is used to connect to 5-1/4 inch floppy drives. Thus, in most user applications the MVME702 module is no longer required.

Connectors J1 and J2 are 20-pin header-type connectors used to radially connect data lines from the hard disks to the controller. Maximum cable length should not exceed 10 feet (3 m). Cables for connectors J1, J2, and J3 should be kept as short as possible.

Connecting two 5-1/4 inch hard disk drives and two 5-1/4 inch floppy disk drives to the MVME320B is illustrated in Figure 2-4.

Connecting four 5-1/4 inch floppy drives to the MVME320B is illustrated in Figure 2-5.

Connecting two 5-1/4 inch hard disk drives, one 8-inch floppy drive, and one 5-1/4 inch floppy drive to the MVME320B is shown in Figure 2-6.

Connecting two 5-1/4 inch hard disk drives and two 8-inch hard disk drives to the MVME320B is shown in Figure 2-7.

Connecting 5-1/4 inch floppy disk drives, not using connector J4 on the MVME320B, is shown in Figure 2-8.

2.6.1.1 Examples of Termination of 5-1/4 Inch Hard Disk

When using a 5-1/4 inch hard disk drive in configurations including 8-inch floppy disks, disconnect terminators on the following signals:

DIRECTION HEAD 20 HEAD 21

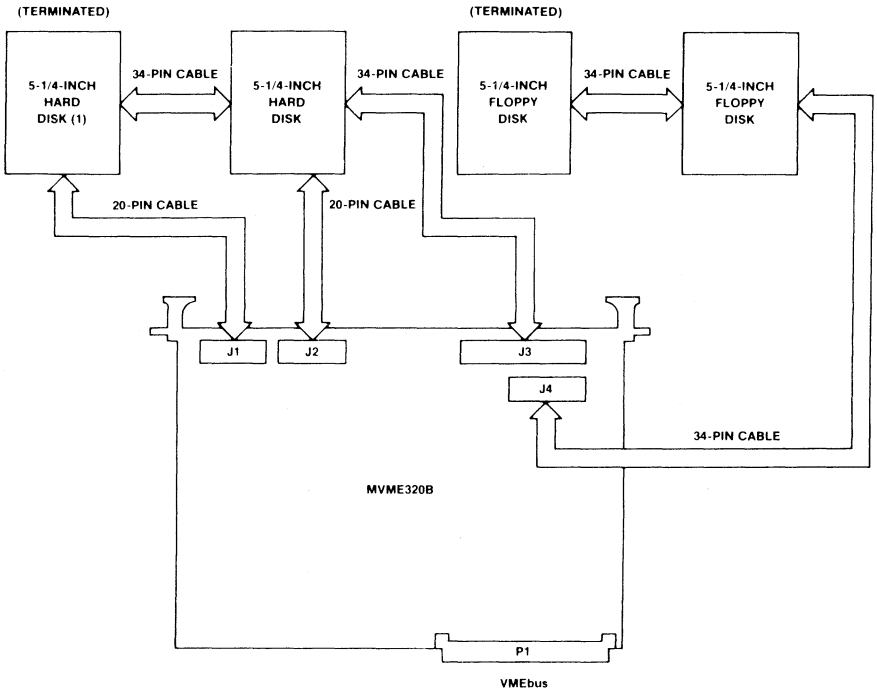
by lifting pins on the terminator resistor network IC on the hard disk drive.

	Delete Pins
IMI 50xx	9, 10, 12
ST4xx	2, 3, 11
ST506	8, 9, 11
MINISCRIBE II (Mod#2006)	1, 11, 12

Always consult the disk drive reference sheet, and compare signal positions on connector J1 of the drive. Each signal should be terminated only once at the physical end of the line.

If a good description or schematic is not available, use a signal-continuity meter to find the corresponding terminator pin for each connector J1 signal pin.

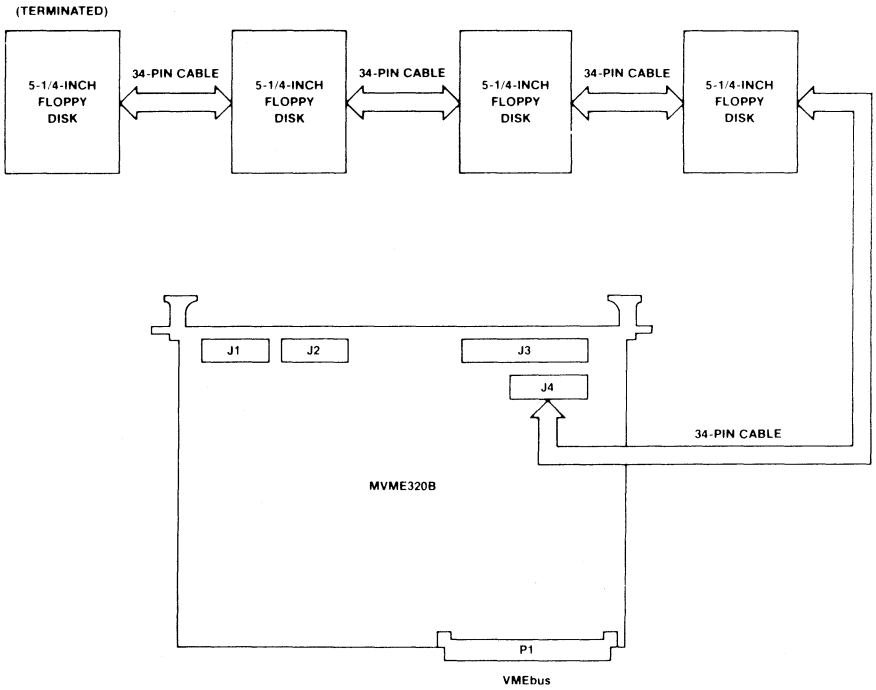
2



NOTES: (1) Only the end of each signal line (typically on the last drive) requires termination.

2. The 5-1/4 inch hard disk uses the first 34 lines (1-34) of J3.

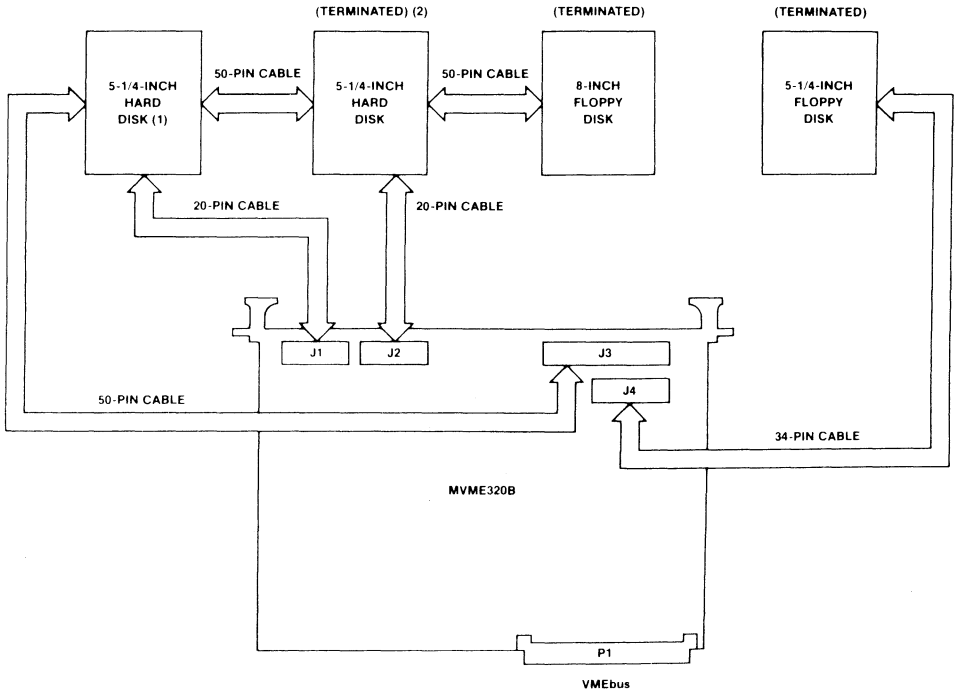
FIGURE 2-4. Two 5-1/4 Inch Hard and Two 5-1/4 Inch Floppy Drives



NOTE: 1. Only the end of each signal line (typically on the last drive) requires termination.

FIGURE 2-5. Four 5-1/4 Inch Floppy Drives

2



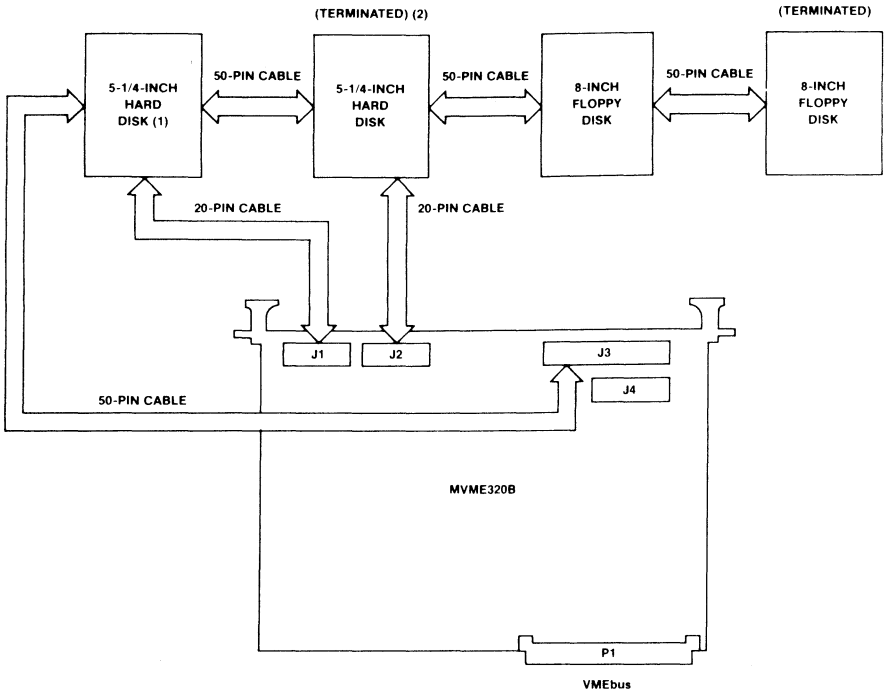
NOTES: (1) Only the end of each signal line requires termination. For systems mixing 5-1/4 inch and 8-inch drives, this can be accomplished by using an 8-inch drive as the last drive installed and terminating all signal lines on that drive.

(2) Refer to examples of termination at the beginning of this section.

3. For 5-1/4 inch hard drives (pins 1-34), the cable will have a 34-pin connector spliced into the lower side of the 50-pin cable.

4. See Figure 2-9.

FIGURE 2-6. Two 5-1/4 Inch Hard, One 8-Inch and One 5-1/4 Inch Floppy Drives



NOTES: (1) Only the end of each signal line requires termination. For systems mixing 5-1/4 inch and 8-inch drives, this can be accomplished by using an 8-inch drive as the last drive installed and terminating all signal lines on that drive.

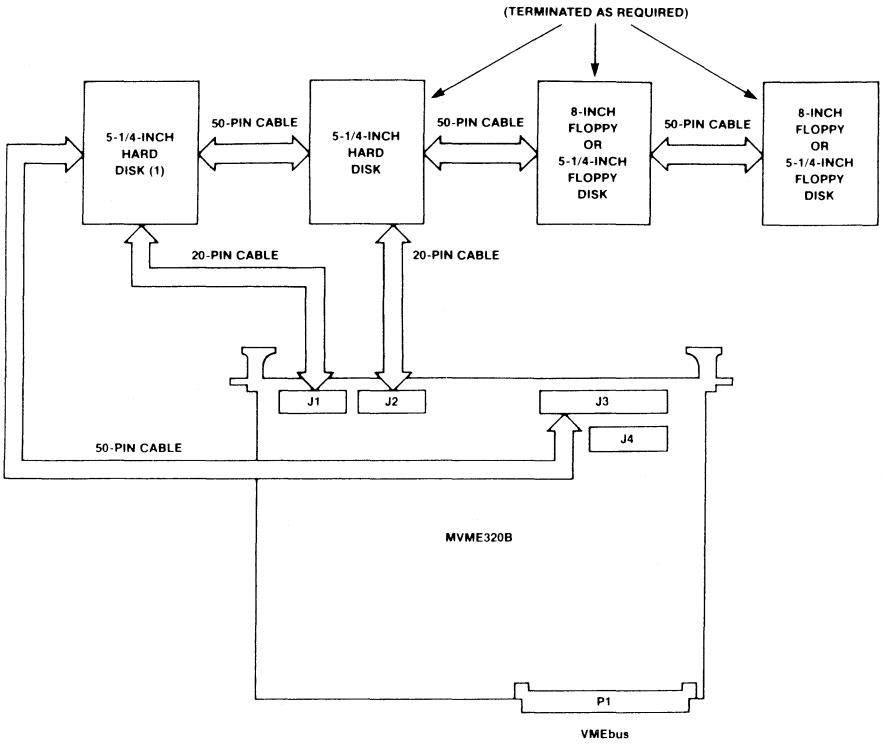
(2) Refer to examples of termination at the beginning of this section.

3. For 5-1/4 inch hard drives (pins 1-34), the cable will have a 34-pin connector spliced into the lower side of the 50-pin cable.

4. See Figure 2-9.

FIGURE 2-7. Two 5-1/4 Inch Hard and Two 8-Inch Floppy Drives

2



NOTES: (1) Only the end of each signal line requires termination. For systems mixing 5-1/4 inch and 8-inch drives, this can be accomplished by using an 8-inch drive as the last drive installed and terminating all signal lines on that drive.

2. In the above illustrations, one or two floppies and one or two hard disks may be attached (daisy-chained), e.g., two ST506 and two SA400 disk drives. The 5-1/4 inch hard disk uses the first 34 lines (1-34) of the 50-pin cable, while the 5-1/4 inch floppy disk uses the last 34 lines (17-50).

3. See Figure 2-9.

4. This figure is shown only for compatibility with older systems not using J4 on the MVME320B module.

FIGURE 2-8. 5-1/4 Inch Floppy Drives Not Using J4

2.6.2 Floppy Disk Cabling

NOTE

This section applies only to the use of floppy drives on J3.

To avoid delays caused by head-settling times or motor-on delay periods, the MVME320B uses the signal line 50 to turn the motor-on for all 5-1/4 inch floppy disk drives every time an access is made on any of the floppy drives. This increases throughput substantially during copying between floppy drives.

Therefore, it is necessary to modify either the radial cable (J3) or the drives as shown in Figure 2-9.

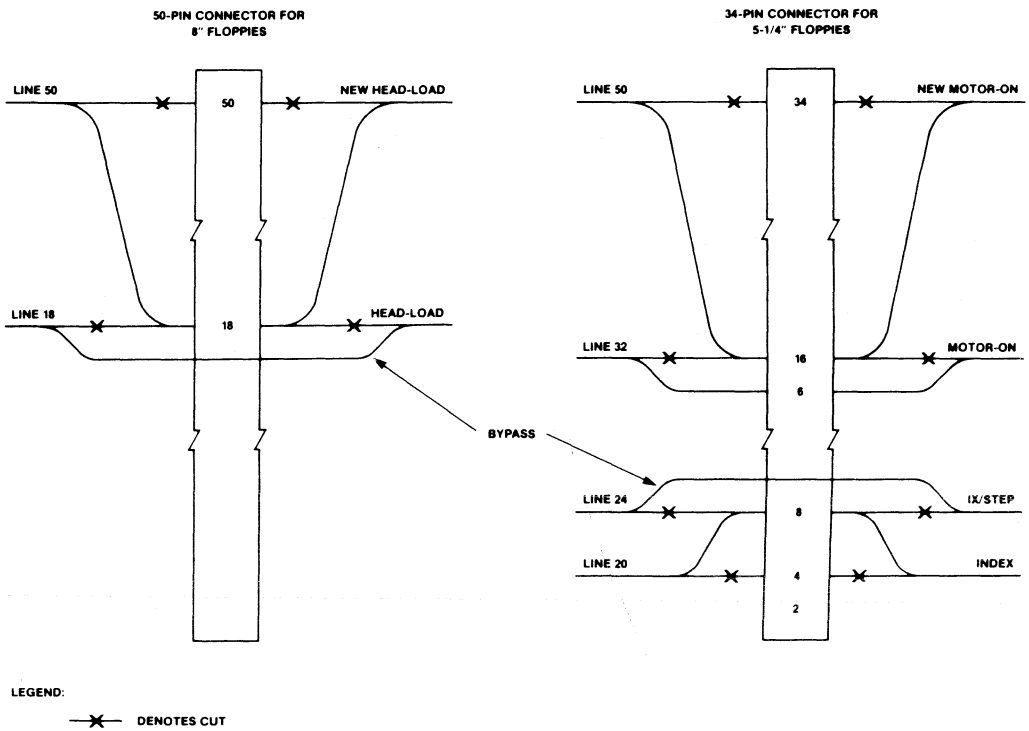


FIGURE 2-9. Floppy Disk Cabling

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CHAPTER 3 - FUNCTIONAL DESCRIPTION

3.1 INTRODUCTION

This chapter presents more detailed information about the MVME320B logic operation. A simplified functional block diagram of the MVME320B is shown in Figure 3-1.

3.2 LOGIC OPERATION

The MVME320B logic is functionally divided as follows:

a. 8X305 MICROCONTROLLER -- executes the microprogram (in the 4K x 24 ROM) at 250-nsec instruction time. The MVME320B uses main SYSCLOCK 16 MHz divided by 2. The 8X305 processes commands and data from the host via the VMEbus, and controls the disk that will perform the user-selected operation. It also returns the result and status bytes to the host in the Event Control Area (ECA) table after the operation is complete.

b. MICROPROGRAM MEMORY -- The 4K x 24 ROM which stores the control microprogram that is executed by the 8X305 microcontroller.

c. DISK I/O PORTS -- Controls slow disk operations (e.g., stepping) as directed by the 8X305.

d. VMEbus I/O PORTS -- Interfaces with the host system using VMEbus I/O operation. This block has an I/O address comparator, control signal receivers, 8-bit data receivers/drivers and control logic.

e. DMA CHANNEL -- Data to/from global VMEbus memory.

f. BUFFER MEMORY (1K x 8 RAM) -- Used both as a disk sector buffer and as scratchpad memory for MVME320B internal operations.

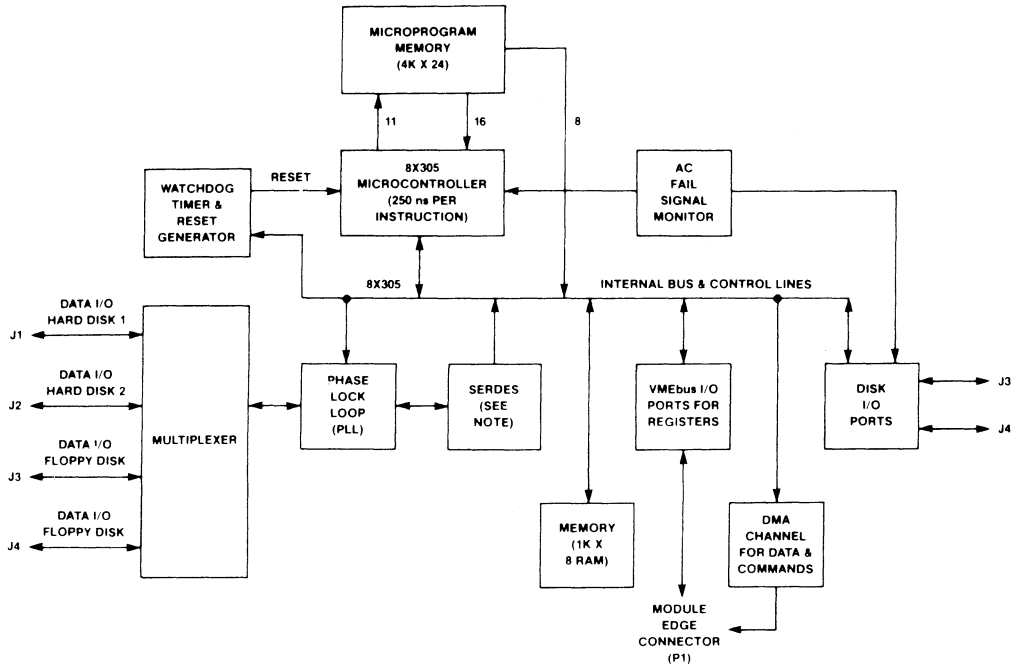
g. SERDES (i.e., SERIALIZER/DESERIALIZER) -- Disk data transfers are performed serially. The SERDES serializes data to be written to the disks and deserializes data received from the disks. The SERDES generates and checks ECC/CRC code.

h. PHASE LOCK LOOP (PLL) -- The PLL circuit is a multifrequency data separator. The use of PLL assures reliable data recovery from the disk.

i. MULTIPLEXER -- This circuit multiplexes I/O data to the PLL circuit from the disk units attached to the MVME320B.

j. AC FAIL SIGNAL MONITOR -- The microprogram monitors this signal using a sampling period 200 usec. Upon power-fail detection, all active disk drives are immediately deselected to protect drives, disk medium, and data.

k. WATCHDOG TIMER/RESET GENERATOR -- This circuit is used as a time-out for disk operations. It contains an error recovery or "watchdog" circuit that monitors for timely completion of various disk operations performed by the MVME320B. If the specified disk operation was unsuccessful within the expected time, the MVME320B repeats the same operation up to the specified re-try number.



NOTE: Serializer/Deserializer, with CRC/ECC circuits.

FIGURE 3-1. MVME320B Block Diagram

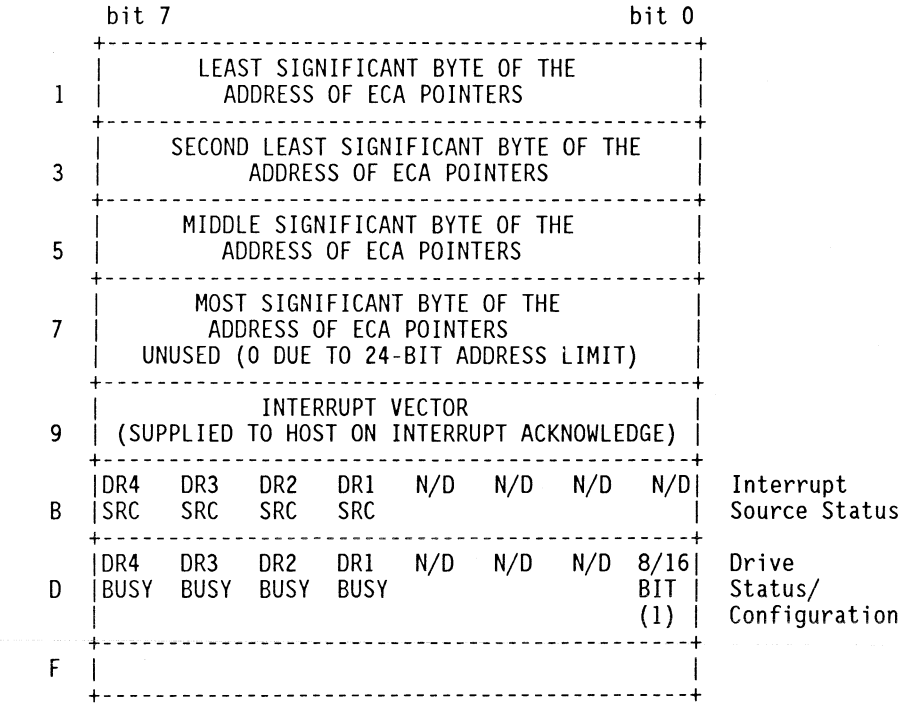
3

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CHAPTER 4 - REGISTERS

4.1 INTRODUCTION

The MVME320B is a Direct Memory Access (DMA) transfer oriented device; only minimal control information needs to be transferred between the I/O and the seven internal registers. The format of the internal registers is shown in Figure 4-1. The addresses for the internal registers are shown in Figure 4-2. The registers reside on the low-order data bus (D0-D7); therefore, their effective address is always an odd value ranging from 1 to D (hex). Each register is referred to by its address (e.g., register D). The contents of the internal registers control the command execution. The following paragraphs describe the contents and format of each register.



NOTE: (1) Ignored.

FIGURE 4-1. Internal Registers

Register	A3	A2	A1	DS1*	DS0*
1	0	0	0	1	0
3	0	0	1	1	0
5	0	1	0	1	0
7	0	1	1	1	0
9	1	0	0	1	0
B	1	0	1	1	0
D	1	1	0	1	0

FIGURE 4-2. Internal Register Address

NOTE

Because the registers on the MVME320B are "virtual" registers, the 8X305 controller performs the protocol. Polling a register during a command execution causes decreased performance. Also, if the command is uninterruptible, the VMEbus time-out may occur before the MVME320B returns the DATA ACKNOWLEDGE signal.

Write "busy" (7), in the main status byte of the ECA table before starting a command. After initiating the command, the main status will be polled until "BUSY" is replaced. Thus, the MVME320B is free to run without servicing the register interface.

4.2 EVENT CONTROL AREA REGISTERS (REGISTERS 1-7)

These registers are read/write registers containing the 24-bit address of the Event Control Area (ECA) pointers. The least significant bit and the most significant byte of the address are not used by the MVME320B. These registers are cleared by RESET to 00. The host subsequently initializes these registers by writing a pointer value to them before issuing a command. This indicates to the MVME320B the location of the ECA pointer table in the system memory. The ECA pointer table consists of four long-word addresses that indicate the location of the four ECA control blocks. The addresses are arranged in ascending order by drive number. Register 7 contains the most significant byte of the address and register 1 the least significant byte.

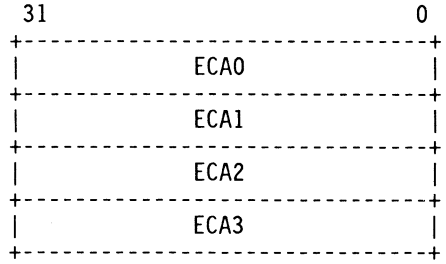
NOTE

Since the least significant address bit is not used, the effective address for the pointer table in registers 1-7 has to be the actual address divided by 2 (shifted 1 bit to the right).

Example: pointer table address: 00C1234
address divided by 2: 006091A
data in register 1: 1A
data in register 3: 09
data in register 5: 60
data in register 7: 00

The host system must not modify ECA information after the command is issued and before the corresponding interrupt is received.

The ECA pointer table can be represented as:



where ECA0 is the address of the ECA table for drive 0.

4.3 INTERRUPT VECTOR REGISTER (REGISTER 9)

The contents of this register is presented to the host system during the interrupt-acknowledge cycle. The register is initialized to the value 0FH by a reset of the MVME320B. This register contains the global interrupt vector assigned by the host system.

4.4 INTERRUPT SOURCE REGISTER (REGISTER B)

The four most significant bits of this register, one for each drive (Dr1-4), are used to indicate which drive is the source of an interrupt.

The reset signal initializes all four bits to 0, indicating that all four drives are inactive and none of them has initiated an interrupt.

When the MVME320B interrupts the host, it indicates which drive has caused the interrupt by setting the interrupt source bit in this register. When the host services the interrupt, it resets the interrupt bit by resetting the corresponding busy bit(s) in register D.

NOTE

When an interrupt occurs, there is a delay before a bit in the interrupt source register is set. Since polling the interrupt source register causes reduced performance by the MVME320B, it is suggested that the status byte in the ECA table be set to "busy" before the operation begins. After an interrupt occurs, the status byte is polled until the "busy" is written over. At this time, the interrupt source register is updated.

4.5 DRIVE STATUS AND CONFIGURATION REGISTER (REGISTER D)

The host can activate a drive by setting the corresponding "busy" bit in register D. The MVME320B responds by accessing the corresponding ECA and performing the requested action. At any time the host can abort the current drive operation by resetting the bit before the operation is completed. This initiates the normal MVME320B interrupt sequence. The MVME320B returns a status in the ECA to indicate that the command has been aborted.

The reset signal initializes all bits to 0, indicating that all four drives are inactive.

CHAPTER 5 - EVENT CONTROL AREA

5.1 INTRODUCTION

The Event Control Area (ECA) is a dedicated block of data stored in the system memory. It consists of a fixed-length mailbox area for controlling the exchange of information between the MVME320B and the host system. The MVME320B requires one ECA for each drive connected. The entire ECA pointer table should be set to 0 (zero) before it is initialized. The ECA block format is illustrated in Figure 5-1. Appendix C provides sample ECA block tables.

	15 EVEN	ODD 0	
$00	COMMAND CODE	MAIN STATUS	
$02	EXTENDED STATUS		
$04	MAXIMUM NUMBER OF RE-TRIES	ACTUAL NUMBER OF RE-TRIES	
$06	DMA TYPE	COMMAND OPTIONS	
$08	BUFFER ADDRESS MOST SIGNIFICANT WORD		
$0A	BUFFER ADDRESS LEAST SIGNIFICANT WORD		
$0C	BUFFER LENGTH REQUESTED		
$0E	ACTUAL NUMBER OF BYTES TRANSFERRED		
$10	CYLINDER NUMBER		(NOTE 1)
$12	HEAD OR SURFACE NUMBER	SECTOR NUMBER	(NOTE 1)
$14	CURRENT CYLINDER POSITION		
$16-$1F	RESERVED (10 BYTES)		
$20	N0 -- PRE-INDEX GAP	N1 -- POST-INDEX GAP	(NOTE 2)
$22	N2 -- SYNC BYTE COUNT	N3 -- POST-ID GAP	(NOTE 2)
$24	N4 -- POST-DATA GAP	N5 -- ADDRESS MARK COUNT	(NOTE 2)
$26	SECTOR LENGTH CODE	FILL BYTE	(NOTE 2)

FIGURE 5-1. ECA Block Format

	15 EVEN 8	7 ODD 0	
$28-$2D	RESERVED (6 BYTES)		
$2E	DRIVE TYPE	NUMBER OF SURFACES	
30	NUMBER OF SECTORS/TRACK	STEPPING RATE	
$32	HEAD SETTLING TIME	HEAD LOAD TIME	
$34	SEEK TYPE	PHASE COUNT (MUST BE SET TO 0)	
$36	LOW WRITE CURRENT BOUNDARY CYLINDER		
$38	PRECOMPENSATION BOUNDARY CYLINDER		
$3A-$3F	ECC REMAINDER (6 BYTES)		(NOTE 3)
$40-$45	APPENDED ECC REMAINDER FROM DISK (6 BYTES)		(NOTE 3)
$46-$49	RESERVED (4 BYTES)		
$4A-$55	MVME320B WORKING AREA (12 BYTES)		
$56	RESERVED FOR THE CONTROLLER		

NOTES: (1) Physical starting sector number.

(2) Track format fields (refer to Chapter 8).

(3) Last word (don't care).

FIGURE 5-1. ECA Block Format (cont'd)

5.2 ECA FIELDS

ECA fields are listed and described in the following paragraphs.

5.2.1 Command Code (1 byte; offset = $00)

The command code indicates the command to be executed (refer to Chapter 6, Commands).

5.2.2 Main Status (1 byte; offset = $01)

The main status field contains general value-oriented status information about the command execution. The status codes and definitions are listed in Table 5-1.

5.2.3 Extended Status (2 bytes; offset = $02)

The extended status field contains specific bit-oriented status information about the command execution. If errors result during execution, the corresponding bit will be ORed into extended status and kept there. This OR function is used by the host system for error logging. The extended status will automatically be reset to zero by the MVME320B at the beginning of command execution. The status codes and definitions are listed in Table 5-1. Examples of error codes are provided in Table 5-2.

TABLE 5-1. Status Codes

Main Status Codes	
$0	Correct execution without error
1	Non-recoverable error which cannot be completed (auto re-tries were attempted)
2	Drive not ready
3	Reserved
4	Sector address out of range
5	Throughput error (floppy data overrun)
6	Command rejected (illegal command)
7	Controller busy (refer to Paragraph 1.8, g)
8	Drive not available (head out of range)
9	DMA operation cannot be completed (VMEbus not available)
A	Command abort (busy bit in register D has been reset prior to completion of operation)
$B-FF	Not used

Extended Status Codes	
$0001	Write fault
0002	CRC error on data or ID
0004	Data overrun
0008	No identifier found
0010	Not ready
0020	Deleted data address mark
0040	Write on write-protected diskette
0080	Positioning error
0100	Data port time-out
0200	Disk format error
0400	Uncorrectable data error (ECC)
0800	Command stop or drive not available
1000	Drive type rejected
2000	Positioning time-out
4000	Wrong ID-DATA-ID sequence during track read command
8000	Bus error fault

TABLE 5-2. Examples of Error Codes

Ms-Es: (1)	Description	Firmware Re-tries	Comments
00-0000	Successful completion	No	The command has completed without errors.
01-0002 (2)	CRC error	No	Soft error, driver should re-try.
01-0008 (2)	Identifier not found	No	Soft error, driver should re-try.
01-0080 (2)	Positioning error	No	Soft error, driver should re-try.
01-0102	CRC/ECC error	Yes	Soft error, driver should re-try.
01-2080	Positioning error/ Data port time-out	No	Soft error, driver should re-try.
02-0010	Drive not ready (door may be open)	No	Hard error, driver should not re-try. Install media and/or close door
06-0040	Write protect violation	No	Hard error, driver should not re-try.
08-1800	Drive not available	No	Hard error, driver should not re-try. This error will occur for: Invalid drive type Invalid seek type
09-8000	Throughput error on DMA operation.	Yes (Sometimes)	Soft error, driver should re-try.
10-0800	Command aborted	No	The driver aborted the command.

NOTES: (1) MS = Main status
ES = Extended status

(2) Any combination of these error codes are possible. All other error codes will appear as shown.

3. The recommended number of re-tries for the firmware, as given in the ECA table is 5 to 10. The recommended number of driver re-tries is 3 to 5.

5.2.4 Maximum Number of Re-tries (1 byte; offset = $04)

This parameter specifies the maximum number of re-tries per command (not per sector) that the MVME320B should attempt after a disk operation error. The value of zero indicates that no re-tries will be attempted.

NOTE

Firmware re-tries, requested through the ECA table entry, occur only for CRC/ECC errors and, occasionally, DMA over/underrun errors. All other re-tries should be initiated by the driver.

The MVME320B re-try logic does re-tries on a per command basis. For example, five re-tries are selected, and a command is given to read 20 sectors. If five sectors read bad the first time, but good the second time, the sixth bad sector will cause the command to fail. Therefore, it is recommended that commands be kept as short as possible.

5.2.5 Actual Number of Re-tries (1 byte; offset = $05)

This byte is set by the MVME320B to the actual number of re-tries executed per command. All re-tries are accumulated by the MVME320B on a sector-by-sector basis.

5.2.6 DMA Type (1 byte; offset = $06)

This 1 byte field should be set to a zero value. This value specifies the Direct Memory Access (DMA) transfer mode of releasing the bus between word transfers. No other options are implemented at this time.

5.2.7 Command Options (1 byte; offset = $07)

This byte contains options that apply to the current command. These options are listed in Table 5-3.

TABLE 5-3. Command Option Byte

BIT	OPTION NAME	LOGIC LEVEL (OPTION)	DESCRIPTION/ACTION
0	Handling of deleted data address mark	0	The sectors with deleted data address mark will be skipped, as if it did not exist. A successful CRC/ECC check is not required.
		1	The data of the sector(s) with deleted data address mark will be transferred to the host system regardless of the CRC/ECC check result, and the operation will be terminated.
1	"Reserved"	Should always be 0	(Reserved for future use, if necessary)
2	Automatic error correction (NOTE)	0	Automatic error correction disabled.
		1	Automatic error correction enabled. This option enables the correction of data in the MVME320B internal memory. It uses the ECA remainder field of the ECA. Besides the correct data, the MVME320B writes the error correction vector and its relative position from the end of the data buffer into the ECA working area.
3-7	"Not used"	---	---

NOTE: After all re-tries failed.

5.2.8 Buffer Address (4 bytes; offset = $08)

This is a 32-bit starting byte buffer address for the DMA transfers. The buffer can start on an odd address. The least significant byte of the address field defines the even or odd byte address of the 16-bit words when in 16-bit mode. The eight most significant bits should be set to zero.

5.2.9 Buffer Length Requested (2 bytes; offset = $0C)

This field contains the requested number of bytes to be transferred. This field implicitly defines the number of multiple-sector transfers to be performed. If a zero length is specified, then only a seek will occur.

5.2.10 Actual Number of Bytes Transferred (2 bytes; offset = $0E)

This field indicates how many bytes have actually been read or written during a command execution. The value can be used, for example, for a location of a problem sector with a nonrecoverable error. The value of this field can be changed by the MVME320B during execution of a command and used as an intermediate field.

5.2.11 Physical Starting Disk Address (4 bytes; offset = $10)

This field contains the physical disk location at which the command is to begin execution. The format of the field is:

$10	Cylinder (High)	Cylinder (Low)
$12	Head/Surface Number	Sector Number

5.2.12 Current Cylinder Position (2 bytes; offset = $14)

These two bytes will be updated by the MVME320B after each positioning. During the first positioning after reset, the MVME320B will execute an automatic recalibration. If the current cylinder = 0, prior to the execution of the next command, the MVME320B will check the track 0 signals. If neither of the two track signals is active, the MVME320B will execute a recalibration procedure and then start command execution.

5.2.13 Reserved (10 bytes; offset = $16)

This field is not used by the MVME320B.

5.2.14 Disk Track Format Fields (8 bytes; offset = $20)

The disk track format fields are described in Chapter 8, Disk Track Format.

5.2.15 Reserved (6 bytes; offset = $28)

This field is not used by the MVME320B.

5.2.16 Disk Control Fields (40 bytes; offset = $2E)

These fields describe the drive interface to the MVME320B.

a. Drive Type (1 byte; offset = $2E) - The most significant bit of this byte designates hard or soft sectoring (a set bit indicates hard sectoring). The seven least significant bits of this byte specify the disk type.

Value	Indicates
0	IBM single-density format, 8-inch floppy disk
1	IBM double-density format, 8-inch floppy disk
2	Hard-disk format with ECC
3	Hard-disk format with CRC
4	Single-density, 5-1/4 inch floppy drive
5	Double-density, 5-1/4 inch floppy drive

b. Number of Surfaces (1 byte; offset = $2F) - The number of heads (surfaces) is used by the MVME320B for calculating the increment sector address.

c. Number of Sectors Per Track (1 byte; offset = $30) - This value is used for calculating the sector address.

NOTE

The first sector on a drive is labeled sector one (not zero).

d. Stepping Rate (1 byte; offset = $31) - This field contains the head stepping rate in 500-usec units, if applicable.

NOTE

The step rate decreases from 1 (fastest step rate), through FF, and then wraps around to 0 (slowest step rate).

e. Head Settling Time (1 byte; offset = $32) - This field contains the head settling time in 500-usec units. If a nonzero head settling time is specified, the MVME320B assumes that a seek-complete is not available from the drive. The head settling time is used on a recalibrate command, even with implied seeks enabled.

f. Head Load Time (1 byte; offset = $33) - This field contains the head load time in 500-usec units. For drives with a seek-complete signal such as hard disks, this value must always be set to zero by the host system.

g. Seek Type (1 byte; offset = $34) - This field defines the type of seek positioning to be performed.

Value	Indicates
0	Normal single-step seek
1	Accelerated seek (for ST506)
2	Buffered seek (for ST412)

NOTE

During a recalibrate, single-step seeks are always used.

h. Phase Count (1 byte; offset = $35) - This field contains the phase counter, which is a status of the command execution set by the MVME320B. For all commands, this field must be initialized to zero by the host system prior to a new command to the MVME320B.

i. Low Write Current Boundary Cylinder (2 bytes; offset = $36) - This field defines to the MVME320B the starting track at which low current write current is to be used. (Must not exceed 8 heads, otherwise line is redefined as "Head Select".)

j. Precompensation Boundary Cylinder (2 bytes; offset = $38) - This field defines to the MVME320B the starting track at which precompensation is to be used.

k. ECC Remainder (6 bytes; offset = $3A) - This field contains the calculated ECC remainder generated by the MVME320B (should be 0). Since ECC is 32-bits long, the last two bytes are "don't care".

l. Appended ECC Remainder from Disk (6 bytes; offset = $40) - This field contains the actual ECC remainder attached to the data on the disk when written.

m. Reserved (4 bytes; offset = $46) - This field is not used by the MVME320B. (It is reserved for future expansion.)

n. MVME320B Work Area (12 bytes; offset = $4A) - These six words are reserved for the MVME320B microprogram. The meaning of certain bytes of this area will be determined by the command being executed.

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CHAPTER 6 - COMMANDS

6.1 INTRODUCTION

The MVME320B command set is as follows:

Command	Function
0	Recalibrate to track zero
1	Write deleted data
2	Verify (read without data transfer)
3	Transparent sector read
4	Read Identifier
5	Read multiple sector with overlapped seek
6	Write multiple sector with overlapped seek
7	Format a track

A new command is requested by the host by writing into the Drive Status and Configuration Register (register D). The user sets a bit corresponding to the drive to be serviced. This causes the MVME320B to start execution of the command on the requested drive (only one drive at a time).

After a command is started, it is executed without further communication with the host system. All drive/memory data transfers are handled automatically by the Direct Memory Access (DMA) controller of the MVME320B. The MVME320B signifies through an interrupt signal that the command is completed.

The following is a generalized description of the sequence performed by the MVME320B when executing a command:

a. The MOTOR ON line is driven active, if not already active.

b. The head will be selected or, for a floppy disk, loaded. The MVME320B will wait for four byte times to ensure that head selection has occurred.

c. The MVME320B verifies that the drive is available. If it is not, the MVME320B generates an error status and a completion interrupt.

d. The MVME320B executes a track seek if necessary. For drives which have a seek-complete signal (as indicated by a zero value in the head settling time field of the Event Control Area (ECA)), a command termination can be caused by the time-out of the Seek Complete signal drive. For drives for which the head settling time is nonzero, the MVME320B waits the specified time after issuing the stepping pulses (i.e., there is no time-out on the seeks).

e. The MVME320B reads the sector identifier to locate the requested sector. If the MVME320B is unable to read the sector identifier, the command is terminated (step g) and the status "no identifier found" is returned. In this case, do a recalibrate and re-try -- treat as a soft error.

f. After the requested sector has been located, the MVME320B performs the sector disk I/O (read or write) and DMA operations. If the operation cannot be completed, re-try processing is attempted. A failure in this portion of the command is indicated by the return status "data port time out", which distinguishes it from the read identifier failure of step d. The MVME320B reads the data from the disk into an internal register first and then through the DMA to the VMEbus memory. The floppy disk read and DMA transfer are executed simultaneously.

g. If multiple sectors have been specified in the command, the MVME320B assumes contiguous physical sectors; steps b, c, d, and e are repeated for each sector. The MVME320B automatically performs any track seek required if the next physical sector is located on the next cylinder.

h. Upon command completion, all relevant ECA fields are updated and the appropriate bits of the "Interrupt Source Status" and "Drive Status and Configuration" registers ($B and $D) are set, and an interrupt signal is generated by the MVME320B. Upon interrupt acknowledge, the MVME320B presents the interrupt vector from the Interrupt Vector Register on the data bus.

6.2 COMMAND DESCRIPTION

In the command descriptions, the term "FIFO" refers to the MVME320B internal memory when it is used as a FIFO buffer. Command descriptions are as follows.

6.2.1 Recalibrate to Track Zero (0)

The function of this command is to retract the heads to track 0. The MVME320B issues one step "IN" and then steps "OUT", a maximum of 1536 times, until signal track 0 becomes active. The check on seek completed time-out will be made for the hard disk.

NOTE

It is possible to get a positioning error and a positioning time-out while recalibrating large drives (40 megabytes, or larger). This error should be considered a soft error, and re-tries should be attempted.

6.2.2 Write with Deleted Data (1)

This command differs from the normal write only by writing the Deleted Data address mark (F8).

6.2.3 Verify (2)

Verify with implied seek functionally is the same as the read command, but the data is not transferred to the host system.

6.2.4 Transparent Sector Read (3)

This command reads a single sector and transfers the data to the host system buffer regardless of a CRC/ECC check. Only the extended status will be updated with all the error conditions encountered.

This command can be used for diagnostic purposes and for recovery of damaged data with some manual intervention.

If an incorrect CRC/ECC remainder occurs, the MVME320B places the remainder into the ECA table, reserved for this purpose.

6.2.5 Read Identifier (4)

This command reads the first identifier found, using the head and cylinder last accessed by the previous command. The cylinder and head entered in the current ECA table are ignored during this command.

This command will read the first identifier found on the disk and fill the buffer with one record consisting of :

- Flag byte
- ID data
- CRC
- Remainder generated by the MVME320B

A CRC error does not terminate execution of the command. This command is generally used for diagnostic purposes.

6.2.6 Read Multiple Sector with Implied Seek (5)

After a successful seek to the desired sector, the MVME320B will start to read the data of the sector into the FIFO buffer and check the CRC or ECC code. Sector data is then transferred through the DMA interface to the host system memory. This procedure is repeated until the number of sectors, implied by the buffer length field of the ECA, have been read.

For sectors with deleted data address mark, the MVME320B will process them according to the command option field of the ECA.

6.2.7 Write Multiple Sector with Implied Seek (6)

After the desired sector is located, the MVME320B will write the complete data part: preamble, data address mark, flag, data, CRC or ECC, and postamble. The precise format is given by the drive type. The FIFO will be continuously filled with new data (or zeros if all buffer data from the buffer has been transferred). The number of data bytes written in one sector is determined by the MVME320B using information from the ECA fields. This operation is repeated until the number of sectors, implied by the buffer length field of the ECA, have been written.

NOTE

The first sector on a disk is labeled sector one (not zero).

6.2.8 Format a Track with Implied Seek (7)

CAUTION

WHILE FORMATTING FLOPPY MEDIA, CARE SHOULD BE TAKEN NOT TO OPEN THE DRIVE DOOR. THE MVME320B WILL WAIT FOR THE DOOR TO BE CLOSED AND WILL NOT TIME-OUT.

The MVME320B supports three different media formats (refer to Chapter 8, Disk Track Format, for detailed information). This allows the user to write the format information specified in the ECA track format fields to the recording media. The buffer address fields of the ECA table point to a memory space that contains sector information for each sector in the track to be formatted. The format for each section of the buffer information is as follows:

FOR FLOPPY DISKS:

BYTE 0	BYTE 1	BYTE 2	BYTE 3

where:
BYTE 0 = CYLINDER NUMBER
BYTE 1 = HEAD NUMBER
BYTE 2 = SECTOR NUMBER
BYTE 3 = SECTOR SIZE CODE, 00 = 128 bytes, 01 = 256 bytes, 02 = 512 bytes

FOR HARD DISKS:

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4

where:
BYTE 0 = CYLINDER NUMBER (MSB)
BYTE 1 = CYLINDER NUMBER (LSB)
BYTE 2 = HEAD NUMBER
BYTE 3 = SECTOR NUMBER
BYTE 4 = SECTOR SIZE CODE, 00 = 128 bytes, 01 = 256 bytes, 02 = 512 bytes

CHAPTER 7 - ERROR CORRECTION

7.1 INTRODUCTION

This chapter describes how the MVME320B supports error correction.

7.2 GENERAL DESCRIPTION

The hard-disk format provides the space for a four-byte error correction code in the data part of the sector. The MVME320B has a bit-serial CRC/ECC generator.

The MVME320B supports error correction in the following ways:

- Generates the remainder during the sector-write operation.
- Checks the remainder during the sector-read operation.
- Delivers all four bytes of remainder for diagnostic purposes.
- Corrects the data either directly in the memory or provides the remainder in the ECC appended area of the ECA.

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CHAPTER 8 - DISK TRACK FORMAT

8.1 INTRODUCTION

The MVME320B supports the following track formats:

- IBM 3740 single-density floppy disk
- IBM System 34 double-density floppy disk
- Hard disk format

In each of the formats, data on the physical media is separated into sectors. The format serves several purposes in this arrangement -- it defines the structure of the sector, the location of the actual data, and provides overhead bytes that allow an interval for any switching required by the drive hardware. These intervals, in turn, allow the MVME320B to compensate for any variations in either the recording media and/or the drive hardware. Although each of these formats is well defined, variations in parameter values within a given format require that the MVME320B provide the user with the capability to adjust (program) them. The purpose of this chapter is to describe the formats that are supported and how to program them with the MVME320B.

Because no single standard defines track format parameters, a description of parameters and other pertinent definitions are included later in this chapter. For the definition of any format parameter, refer to paragraph 8.4. A summary of the formats and the programmable values is provided in Table 8-1.

The hard disk format is a MFM format which is nearly identical to the IBM System 34 double-density format. The differences are summarized below:

IBM FLOPPY DISK	HARD DISK
Uses index address marks	No index address marks
Sector ID part has one byte of cylinder data	Uses two bytes
Sector ID part has three address marks	Uses one address mark
Sector data part has three address marks	Uses one address mark
Data field check consists of 2-byte CRC only	Uses either 2-byte CRC or 32-bit ECC

The Format Track command allows the user to write formatting information to the recording media. Specification of format parameters is accomplished by changing appropriate Event Control Area (ECA) fields. This structure gives the user the flexibility to accommodate, through changes in the ECA, variations that occur within a given format.

NOTE

The first sector on a disk is labeled sector one (not zero).

TABLE 8-1. Summary of Format Parameters

		IBM-COMPATIBLE FLOPPY DRIVES			HARD DISKS		
DESCRIPTION	MODULE USES	HEX DATA VALUE	FM CNT	HEX DATA VALUE	MFM CNT	HEX DATA VALUE	PGM CNT
Pre-Index Gap	N0	FF	40	4E	80	-	-
Sync Field	N2	00	6	00	12	-	-
Index Mark		FC/D7 (1)	1	C2 (2)	3	-	-
Index Flag		-	-	FC	1	-	-
Index Gap	N1	FF	26	4E	50	4E	20
Sync Field		00	6	00	12	00	12
ID Address Mark		FE/C7 (1)	1	A1 (3)	3	A1 (3)	1
ID Address Flag		-	-	FE	1	FE	1
Cylinder	DMA		1		1		1or2
Side/Head	DMA		1		1		1
Sector	DMA		1		1		1
Record Length	DMA	01 (4)	1	01 (4)	1		
CRC-CCITT			2		2		2
Post-ID Gap	N3	FF	11	4E	22	00	3
Sync Field	N2	00	6	00	12	00	12
Data Address Mark		FB/C7 (1)	1	A1 (3)	3	A1 (3)	1
Data Address Flag		-	-	FB	1	FB	1
Data (4)		Fill Byte	256	Fill Byte	256	Fill Byte	256
CRC-CCITT			2		2	(5)	2or4
Post-Data Gap	N4	FF	27	4E	54	00/4E	15
Inter-record Gap (4)		FF	170	4E	589	4E	346

NOTES: (1) Shows data pattern and clock pattern (clock pattern normally is FF).
(2) Shows data pattern; clock pattern should suppress clock bit between data bit 3 & 4.
(3) Shows data pattern; clock pattern should suppress clock bit between data bit 4 & 5.
(4) This example is for a 256-byte sector; others will have different values.
(5) This can be either a CRC-CITT or a 32-bit ECC field.

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The MVME320B writes the sector identifier and fills the data part with "fill byte" starting with the leading edge of the first index pulse and ending with the leading edge of the next pulse.

The "buffer length" field of the ECA designates the end of the formatting operation.

Sector interleaving can be done by filling the buffer.

8.2 BAD SECTOR HANDLING

Sometimes defective media sectors are encountered. The cost of perfect media is impractical. Since defective media areas cannot be used for recording data, the occurrence of bad sectors must be taken into account. It is suggested that a software implementation similar to bad sector lockout (as used on Motorola's VERSAdos) or bad sector replacement (as used on Motorola's SYSTEM V/68) be implemented in the driver.

Sector lockout may be accomplished by keeping a table of known bad sectors on the disk. The sectors on this list are then avoided. This table need only be checked when accessing sectors of unknown quality (e.g., writing a new sector).

A sector replacement algorithm involves keeping a list of known bad sectors and their replacement sector on the disk. This list is checked every time a disk access is made. A copy of this list should be kept in RAM for quicker disk accesses.

8.3 ECA TRACK FORMAT FIELDS

For the three formats supported by the MVME320B, eight parameters are required to specify the format of the recording media to the MVME320B. The format parameters are programmed by changing the values of the appropriate ECA fields. A detailed description of each of these parameters follows. The layout of the track format portion of the ECA is:

15 8	7 4	3 0
N0 -- Pre-Index Gap	N1 -- Post-Index Gap	
N2 -- Sync Byte Count	N3 -- Post-ID Gap	
N4 -- Post-Data Gap	N5 -- Address Mark Count	
Sector Length Code	Fill Byte	

where: Sector Length Code = zero, for 128 byte sectors
one, for 256 byte sectors
two, for 512 byte sectors

N0, N1, N2, N3, and N5 are fields reserved for future use; the MVME320B uses constants, which are listed in Table 8-1.

N4 must be initialized in the ECA table using the values listed in Table 8-1.

8.4 DESCRIPTION OF FORMAT PARAMETERS

Although exhibiting some differences, the parameters that constitute each of the three formats supported by the MVME320B are basically similar. In each format, the data on the diskette or disk is separated into a logical data block or sector. The sector becomes the smallest block of information that can be addressed directly by the MVME320B.

The hard disk and both IBM formats organize the physical disk into a circular path or track that is separated into several sectors. In this scheme, tracks on the media are referenced with respect to a physical index mark. An index mark pulse is generated by the media to indicate the beginning of a track. By specification of a track and sector, the location of a sector on the media is uniquely addressed (for at least one side of the media). The programmable hard-sectored format also uses this track and sector structure; however, it differs from the other formats in that in addition to the index pulse, each sector is preceded by a sector pulse.

In each of the formats a sector can be further separated into two parts or subfields -- an ID and a data subfield. The ID subfield contains a unique identifier (or address) and description of the sector. The data subfield contains the actual data of the sector. Both subfields contain three types of information:

a. address mark(s)
b. data (either actual or about the sector)
c. error report.

The following definitions apply to the information contained in these subfields:

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Address Mark -- A unique character which precedes the data in the subfield. For MFM formats, (non-IBM single-density) it is followed by a single character, the address mark flag, which further describes the subsequent data.

Error Report -- A pattern generated by the MVME320B that is used to verify the data transmitted.

Both fields contain character sequences called "gaps" and "syncs". These sequences are used to differentiate the sector subfields and to provide an interval that allows any hardware switching to be performed. This, in turn, compensates for any timing problems caused by variations in either the recording media or the disk drive.

For the programmable hard-sectored and IBM formats (which use the index pulse), a third subfield is used: the index subfield. This subfield appears prior to the first physical sector of a track on the recording media and has subfields which contain gap and sync sequences. Unlike the other two fields, it occurs only once per track and contains only the address mark information.

Definitions and abbreviations applicable to the track format specifications are provided in Table 8-2.

TABLE 8-2. Track Format Definitions and Abbreviations

NAME	SUBFIELD	FORMATS	DESCRIPTION
N0	Index	IBM	Pre-Index Gap. This gap represents the only number of bytes that appear prior to the index pulse.
N1	Index	All except hard sector	Post-Index Gap. This gap represents the number of bytes that appear after the index pulse and prior to the ID subfield.
N2	ID, Data, Index	All	Preamble Count or Sync. This is the number of sync bytes that precede the address mark.
N3	ID	All	Post-ID Gap. This count is the number of bytes that separate the ID subfield from the data subfield.
N4	Data	All	Post-Data Gap. This count is the number of bytes that separate the data subfield to the beginning of the ID subfield of the next sector.
N5	ID, Data, Index	IBM	Address Mark Count. This contains the number of address marks contained by the subfields. For single-density formats the count is one; for double-density formats the count is three, except hard disk where it is also one.

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CHAPTER 9 - SYSTEM OPERATION

9.1 INTRODUCTION

This chapter provides information concerning MVME320B initialization, status on reset, host initialization, and ECA field types.

9.2 MVME320B INITIALIZATION

Before the MVME320B can process command requests from the host, it must go through an initialization sequence that places it into a known condition in preparation for commands. This initialization occurs in two distinct stages. The first is started by the activation of the Reset line, and the second is performed by the host system. The MVME320B status to be considered consists of the following components:

- Content of the MVME320B control registers
- State of the control and signal lines
- Status of the MVME320B microprogram

9.3 STATUS ON RESET

On activation of the Reset line, the MVME320B performs the following:

- Resets all control registers
- Three-states all bus interface and control lines
- Clears all internal registers and counters
- Places the MVME320B microprogram into an idle loop

9.4 HOST INITIALIZATION

The second stage of initialization occurs after the reset. The host must initialize the MVME320B before it can process any command requests. The initialization information must be passed from the host to the MVME320B control registers. The information consists of the following:

- Load an interrupt vector number into the Interrupt Vector Register.
- Load the Event Control Area (ECA) registers with the start location of the ECA pointer table in system memory.

The host prepares for MVME320B operation by loading the ECA pointer table in system memory with the address of each of the ECA blocks. The disk drive to ECA block assignment is determined by the relative position of the pointer in the table. The first table entry corresponds to drive one, the second entry to drive two, etc.

9.5 ECA FIELD TYPES

ECA formats, drive control parameters, command execution parameters, and command status are described in the following paragraphs.

9.5.1 ECA Formats

The ECA parameter blocks are the main means of communication between the host system and the MVME320B. The information contained in its fields serves essentially two purposes. First, it provides the information required by the MVME320B to generate the disk drive interface signals. Second, the ECA is used by the MVME320B to pass to the host information required to execute system-level disk operations. To emphasize this second purpose, consider a system operation such as "open a read file". Such an operation implies that the host system issues several commands to the MVME320B to read the disk. Implementing such a system-level command requires that, at the completion of a command, the MVME320B pass to the host current information about the drive and the command (such as the current position of the read/write head). The host uses this information to prepare the next sequence of MVME320B commands.

As an MVME320B command proceeds through its execution, it references and alters various fields of the ECA. To gain a better understanding of the interaction between the MVME320B and the various ECA fields, the ECA data can be separated into three catagories:

- Drive control parameters
- Command execution parameters
- Command status

These categories differentiate the ECA fields with respect to content, access, and alterability. The following paragraphs describe the characteristics of each category.

9.5.2 Drive Control Parameters

These fields contain information that defines the disk interface to the MVME320B. This information is provided by the host system and is not altered by the MVME320B. The MVME320B microprogram that controls the disk drive I/O issued will continually reference this information during execution of a command.

To protect against positioning errors when switching from one ECA field to another, the field "current cylinder number" cannot be initialized by the host (since the MVME320B only writes into it and does not read from it).

9.5.3 Command Execution Parameters

These parameters consist of those ECA data fields required by the MVME320B to execute a command. These fields can be further separated into two groups: static and dynamic. The static fields are valid for the duration of a command; the MVME320B does not alter any information in these fields while the command is being processed. The dynamic fields provide the "logical storage" needed to execute multiple-sector commands. The MVME320B uses the dynamic fields of the ECA to maintain the current execution status of the online disk drives.

Both the static and dynamic fields are loaded prior to initiation of a new command request by the host. The MVME320B provides only rudimentary checks of these fields to ensure integrity of the information. The host must provide the level of safeguards desired.

9.5.4 Command Status

These fields report to the host the results of a command operation and are continually updated after each transfer. They are cleared by the MVME320B when a new request is accepted. Busy should be set to ensure the MVME320B has updated the ECA table (an interrupt may occur before table is updated -- test "Busy" to check for the table update.)

9.6 SUMMARY

Communications between the MVME320B and the host are established through the ECA. After a command has been accepted by the MVME320B, the host must not alter the ECA.

The host can monitor progress by polling the main status byte. The MVME320B can modify other values for internal operations.

Implicit to the execution of any disk operation is the reading of the ECA data by the MVME320B to allow loading of drive control parameters. At the conclusion of a disk operation, the MVME320B performs a write operation to the corresponding ECA parameters to store the results of the command. Both reading and writing of the ECA fields by the MVME320B use the Host/Direct Memory Access (DMA) interface to arbitrate for the system bus and to perform required handshaking.

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CHAPTER 10 - SCHEDULER CONCEPTS

10.1 INTRODUCTION

The primary purpose of the MVME320B in a system is to reduce the overhead processing of a host involved with controlling several disk drives. Off-loading from the host performs those tasks directly associated with disk control and permits the host processor to concentrate on its main application(s).

10.2 RESOURCES

The MVME320B resources available to the disk drives and the host processor consist of:

- Host/DMA interface
- Internal memory
- Control registers
- High-speed disk controls and serial I/O interface
- Low-speed disk controls

The following is the set of basic activities in which the MVME320B can interact with the drives and/or host:

a. Read control register
b. Write control register
c. Slow disk drive read
d. Slow disk drive write
e. Read FIFO (DMA)
f. Write FIFO (DMA)
g. Read ECA data field (DMA)
h. Write ECA data field (DMA)
i. Disk drive serial read (high-speed disk control)
j. Disk drive serial write (high-speed disk control)

Because performance of items a. to h. involves the common MVME320B data bus, (D00-D15) interface, the items are executed one at a time; that is, the MVME320B cannot perform them in parallel. The MVME320B is structured such that the host/DMA and the high-speed disk control interfaces operate asynchronously with the MVME320B processor as well as with each other. This suggests that items i. and j. can be performed concurrently with any of the other 8 activities. Concurrent operation or command queueing is not supported.

10.3 LOGICAL OPERATIONS

Theoretically, a new activity could be scheduled after any one of the basic operations has been performed. In practice, this is not an efficient use of the MVME320B. Also, certain of these combinations are not logically useful. For example, during serial disk I/O it would not make sense to allow the ECA pointer register to be altered. For these reasons, the MVME320B does not execute a command in terms of these basic activities; instead, it joins them into the following logical groups:

- Load and initiate a new command request
- Perform disk positioning I/O
- Perform disk read/write I/O
- Disk write I/O for format commands
- Abort a command

These operations are the most fundamental level of MVME320B activity. The MVME320B commands are implemented essentially as combinations of these operations. For example, the MVME320B read multiple sector command consists of "disk positioning I/O" and several "disk read I/O" operations. For the remainder of this document this set of MVME320B operations will be referred to as "logical operations".

With several disk drives online, the scheduler should do more than sequence through the execution of a command; it must decide what drives are to be serviced and when certain operations are to be performed. The algorithm that the host incorporates must not only service the online drives, but it must do this in an equitable manner. No drive should be allowed to monopolize the MVME320B resources; for example, the unserviced drives in this situation would appear to "wait" while one drive completes a command. The host system should not be required to "idle", waiting to submit a new command request. This situation would degrade the performance of the entire system. Another responsibility of the host is to provide some safeguards against a command destroying information of another current command.

Although the host program will be responsible for making the decisions described above, the operational characteristics of the MVME320B dictate when new commands are allowed and when certain operations can be scheduled. The following describes each of the logical MVME320B operations and their interaction with an external host; this information constitutes the limitations and requirements the MVME320B imposes on this host scheduler.

10.4 COMMAND INITIATION

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Although requesting the MVME320B to perform a command involves simply setting the start bit for the desired drive in the configuration and semaphore register, execution of the command is dictated by the status of the MVME320B when the request is received. Because the MVME320B is operating asynchronously with an external processor or processes, submitting a new command is not always as straight-forward as altering the content of a few MVME320B control registers. The following describes the MVME320B behavior when the scheduler makes a new command request.

For the remainder of this section the internal memory of the MVME320B will be referred to as the FIFO.

10.4.1 New Command Requests

The host must wait for completion of the previous command before issuing a new command. If this is not done, the MVME320B may not function properly.

The host can then signal the MVME320B that it has a new command by setting the bit assigned to the desired drive in the drive status and configuration register. This can be performed as long as the bus is available.

10.4.2 Validity Checks for New Commands

The MVME320B can only perform limited checks on the Event Control Area (ECA) data. The host should perform these checks whenever a disk command request is made; this is especially important when the command request is a continuation of a "system-level" disk drive command. Three ECA fields are continually updated and are required for continuation of such commands. These fields are:

- Physical sector start
- Current cylinder
- Buffer start address

Validity check errors detected by the MVME320B will result in termination of the command request and initiation of the interrupt sequence. These checks are limited to the following:

- Valid options
- Valid number of re-tries requested

After a command has been accepted, the MVME320B will not interact with the host again until the command has been completed or terminated.

NOTE

The MVME320B does not verify the following fields within the ECA:

- Drive type
- Command code
- Buffer address
- Cylinder number
- Sector number

If any of these fields are invalid, the MVME320B will not function properly.

10.5 MVME320B DISK DRIVE CONTROLS

One of the most powerful features of the MVME320B is its ability to control a variety of different disk drive interfaces. This ability is achieved by providing it with facilities to easily "program" the desired disk drive interface. The MVME320B disk drive interface signals are generated by an onboard processor which is controlled by a "table-driven" microprogram. The host system defines the table parameters to the MVME320B microprogram through the device control parameter fields of the ECA. The processor uses this information to generate the appropriate signals for the interface.

Disk drive I/O can be separated into two groups -- positioning and read/write operations. The MVME320B drive interface, as described previously, consists of two sections:

- Slow disk control and status signals
- High-speed control and serial data read/write signals

Generally, the former controls the positioning, and the latter controls the read/write operation.

10.5.1 Positioning Operations

During positioning operations, the read/write mechanism of the disk drive is moved to the selected track and the drive is prepared for the read/write operation. The positioning procedure performed by the MVME320B consists basically of the following seven steps:

a. Read the device control parameters from the ECA.

b. Read the slow drive status.

c. Issue drive signals to the drive to move the heads to the desired track (cylinder). The mechanical motion associated with this movement is referred to as "seek".

d. Test the "seek-complete" flag for the drive until the operation is complete.

e. Wait for the "head settling time" as specified by the corresponding ECA field to ensure the heads have settled.

The MVME320B performs a seek to the desired track by issuing one seek pulse for each track the heads are to be moved. Because the actual "seeking" is a mechanical operation, it is a relatively slow activity; a minimum of 3 msec is required in drives without a buffered seek feature.

The "type of seek" field of the ECA defines which course of action is performed by the MVME320B. Three types of seek operations are commonly available on most disk drives. The "normal" seek allows the MVME320B to issue a single seek pulse and after a sufficient stabilization period becomes available for other processing. The "buffered" and "accelerated" seeks require a dedicated processor to produce a continuous stream of pulses. Drives interfaced in this manner contain internal counters that store the "seek" count before initiating the actual seek operation. For such interfaces, the number of steps must be sent as a continuous stream of pulses to the disk drive. The MVME320B must issue all the required seek pulses before it can attempt other processing.

For buffered and accelerated seek devices, the maximum time the MVME320B uses doing head positioning can be easily derived. The MVME320B firmware generates head step pulses at a rate of 26 usecs per pulse. (The ST506 interface specification specifies a minimum of 6 usecs per pulse in buffered mode.) Therefore, the time for the MVME320B to generate the required number of seeks is the product of the number of seeks and the pulse period per seek. For example, a 512-track seek would require 13.3 msecs on a hard disk (512 x 26 usecs/pulse = 13.3 msecs).

10.5.2 Read/Write Operations

After the read/write head(s) have been positioned to the correct track, the MVME320B is ready to generate the high-speed disk control and serial data transfer signals needed for disk read/write. For the MVME320B, this operation is closely integrated with the activities of the DMA controller. The disk drive and DMA interfaces operate in parallel and independent of each other and of the MVME320B control processor.

The MVME320B FIFO buffer is the primary data transmission facility between system memory and the disk drive. The DMA controller of the host/DMA interface is responsible for performing the actual transfer. For disk read, the serial data from the drive is placed into the FIFO after it is read from the drive. For disk write, data is loaded by the DMA into the FIFO from system memory before it is sent serially to the disk drive.

The "basic read and write" disk operations consist of the following sequence. The read/write operation for the format command is essentially executed as described in the following sequence. However, implementation of these commands involves additional processing, which is described in separate subsections.

The disk write operation consists of the following sequence:

a. Read the ECA for drive control parameters.

b. Transfer write data from system memory to MVME320B FIFO. Perform disk read operation to locate the data part of the requested sector (i.e., process the ID part of the sector).

c. Transfer one operand from the FIFO to serial drive output.

d. Perform disk write I/O on the drive interface.

e. Continue steps c. and d. asynchronously until a sector has been written.

f. After a sector has been written, write the status and dynamic command execution information about the transfer into the ECA.

g. Repeat steps b. through f. until the requested number of sectors has been written.

The disk read operation consists of the following activities:

a. Read the ECA for drive control parameters.

b. Perform disk read operation to locate the data part of the requested sector (i.e., process the ID part of the sector).

c. Perform disk read I/O on the drive interface. Move the character read into the FIFO buffer.

d. DMA transfer the operand from the FIFO to the system memory.

e. Continue steps c. and d. asynchronously until a sector has been read.

f. After a sector has been read, write the status and dynamic command execution information about the transfer into the ECA.

g. Repeat steps b. through f. until the requested number of sectors has been read.

Notes on Basic Read/Write Operations

The previous description for the MVME320B read/write I/O operations has been greatly simplified and some important points should not be overlooked. First, the actual DMA transfer involves three tasks:

a. Request mastership of the system bus.

b. After becoming bus master, generate the handshake signals required to send/receive data through the system bus.

c. Terminate the transmission and return the bus for arbitration.

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Second, in step b. for both the read or write, the MVME320B processes the format information from the media. For a description of this activity, refer to Chapter 8, Disk Track Format.

10.5.3 DMA Transfers

The serial read/write I/O portion of the drive interface is a dedicated slave of the MVME320B disk drive interface; that is, a serial string is sent or received by the interface without interruption. The DMA interface, however, must surrender the bus for arbitration after the requested number of operands have been transferred. If the number of transfers does not provide the MVME320B with sufficient bus access time, the DMA could fail to keep track with the disk I/O operation.

For floppy disks, contiguous sectors can be transferred directly from the floppy disks via DMA. The floppy disk is slow enough to allow new arbitration for each word transfer without significant system restrictions on other components. The fastest floppy disk drive (double-density, 8-inch) allows 30 usec bus latency; 62 usec for double-density, 5-1/4 inch; 125 usec for single-density, 5-1/4 inch.

For hard disks, however, the bus latency time needed for arbitration could cause throughput errors if data were transferred directly from hard disk to host memory. Therefore, the MVME320B reads the disk data into an internal one-sector buffer and then transfers from buffer to host memory. DMA buffering occurs only for hard disks.

10.6 DISK WRITE I/O FOR FORMAT COMMANDS

The format command write operation is performed by the MVME320B as integral operations on a per-track basis. This command would be most efficient if allowed to monopolize the MVME320B resource. However, this would prevent any other drive from being serviced until the command had been completed. Normally this command is a background task with the other disk operations having a higher priority. For this reason, allowing the MVME320B to concentrate completely on either command is not a good system practice.

To allow other drives to be serviced without severely slowing down the execution of these commands, the MVME320B performs the I/O associated with them on a per-track basis.

The MVME320B becomes available for other processing after a full track has been processed. For the worst-case situation for the format command, the time the MVME320B will not be able to process the other drives will not exceed two disk revolutions. This would occur if the index pulse were just "missed" and a complete revolution were required to find the pulse.

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CHAPTER 11 - THEORY OF OPERATION

11.1 INTRODUCTION

This chapter provides a brief theory of operation for the MVME320B Disk Controller Module.

11.2 THEORY OF OPERATION

The first step in requesting a new command of the MVME320B is to build the ECA table. All entries in the ECA table should initially be set to 0, then the proper fields should be set up (refer to Chapter 5 for a complete definition of the ECA fields). The ECA registers are now initialized. These registers tell the MVME320B where to find the ECA table and what interrupt vector to give the drive status and configuration register (register D) is written to. Once the command is started, no other communication with the host is necessary. All drive/memory data transfers are handled automatically by the DMA controller on the MVME320B. Command completion is signaled with an interrupt generated by the MVME320B.

The MVME320B verifies whether or not the drive is available. If the drive is not available, an error status and completion interrupt are generated. If the drive is available, a track seek command is executed, if necessary. For drives which have a seek complete signal (indicated by a zero value in the head settling time field of the ECA), a termination command can be caused by a time-out of the seek complete signal. For drives without this feature, the MVME320B waits a specified amount of time after issuing the stepping pulses. The head is then selected, or loaded for a floppy disk, and the MVME320B waits four byte times to ensure proper head selection. The sector identifier is then looked for, and if not found the status "no identifier found" is returned and the command is completed.

After the requested sector has been located, the MVME320B performs the disk I/O (read/write) and the DMA operations. If these operations cannot be completed, re-try processing is attempted. If an error occurs at this time, it is reported as a "data port time-out", and the command is terminated. The MVME320B reads the data from the disk into an internal register, and then the DMA controller moves it to global memory on the VMEbus. Floppy disk read, and DMA transfer are executed simultaneously. If multiple sectors have been specified, the MVME320B automatically searches for the next sector identifier and the process is repeated.

Upon command completion, all relevant ECA fields are updated and the appropriate bits in the interrupt source status register (register B) and the drive status and configuration register (register D) are set. The MVME320B then generates an interrupt to the host system, and when the interrupt acknowledge is received, the contents of the interrupt vector register (register 9) are placed on the VMEbus.

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CHAPTER 12 - MAINTENANCE

12.1 INTRODUCTION

This chapter contains preventive and corrective maintenance instructions as well as Voltage Control Oscillator (VCO) test procedures for the MVME320B.

12.2 PREVENTIVE MAINTENANCE

Periodically, the user should perform the normal maintenance procedure for his system. Dirt should be cleaned from the MVME320B module and all filters. Verify the installation procedure for the MVME320B module (refer to installation instructions in Chapter 2).

CAUTION

WHEN USING THE MVME320B WITH A DISK DRIVE ENCLOSURE CONTAINING A SEPARATE POWER SUPPLY, TURN OFF POWER TO THE DRIVE ENCLOSURE BEFORE TURNING OFF POWER TO THE MVME320B TO PREVENT POSSIBLE DAMAGE TO THE SYSTEM. ALSO, WHEN POWERING UP THE SYSTEM, TURN ON THE POWER TO THE MVME320B BEFORE POWERING UP THE DISK DRIVE.

12.3 CORRECTIVE MAINTENANCE

In most cases, if the MVME320B fails, the module should be returned to the factory. However, the following items should be verified first as they could be causing the failure:

CAUTION

IF THE MVME320B MUST BE REMOVED WHEN PERFORMING ANY OF THE FOLLOWING CHECKS, TURN POWER OFF BEFORE REMOVING OR RE-INSERTING THE MODULE.

a. Perform the procedures in the installation section, verifying that the 50-pin connector, the 34-pin connector, and 20-pin connectors are properly plugged into both the MVME320B and the first disk drive.

b. Verify the connections between drives (e.g., the daisy-chain connections).

c. Verify that the last drive in the chain is terminated.

d. Be sure that all ICs on the MVME320B are fully seated in their sockets.

e. Be sure that the module edge connector is free of dirt and grease. If necessary, clean the edge connector. Be sure that the connector is fully inserted into the backplane in the VMEbus system.

12.4 VCO TEST PROCEDURE

Power up the MVME320B disk controller module on an extender board. Drives need not be connected.

Connect a 15 MHz or better frequency counter to ground and U83, pin 6. This measures VCO frequency.

Momentarily ground AR1, pin 6, and note the VCO frequency. It must be at or below 6.80 MHz.

Momentarily connect AR1, pin 6, to VCC (+5V) and note the VCO frequency. It must be at or above 11.50 MHz.

If the VCO fails at both the 6.80 MHz and 11.50 MHz test, replace the VCO chip U83, MC4024, 51NW9615A28.

If the VCO fails by not being low enough in frequency to meet the 6.80 MHz test, replace C56, 33 pF, 21NW9629A11, with 36 pF, 21NW9629A12, or with 39 pF, 21NW9629A13, etc., as necessary.

If the VCO fails by not being high enough in frequency to meet the 11.50 MHz test, replace C56, 21NW9629A11, with 30 pF, 21NW9629A10, or with 27 pF, 21NW9629A09, etc., as necessary.

CHAPTER 13 - SUPPORT INFORMATION

13.1 INTRODUCTION

This chapter contains connector pin signal descriptions and a parts list for the MVME320B.

13.2 CONNECTOR PIN SIGNALS

The VMEbus signals on connector P1, giving the signal mnemonic, connector and pin number, and signal description are listed in Table 13-1. Connector P2 is not used. The signals for disk interface connectors J1 and J2 are listed in Table 13-2. The signals for disk interface connector J3 are listed in Table 13-3. The signals for disk interface connector J4 are listed in Table 13-4.

13.3 PARTS LIST

The components of the MVME320B are listed in Table 13-5. The parts location diagram is shown in Figure 13-1. The parts list reflects the latest issue of hardware at the time of printing.

TABLE 13-1. Connector P1 Signals

SIGNAL MNEMONIC	CONNECTOR AND PIN NUMBER	SIGNAL NAME AND DESCRIPTION
ACFAIL*	1B: 3	AC FAILURE - Open-collector driven signal which indicates that the AC input to the power supply is no longer being provided or that the required input voltage levels are not being met.
IACKIN*	1A: 21	INTERRUPT ACKNOWLEDGE IN - Totem-pole driven signal. IACKIN* and IACKOUT* signals form a daisy-chained acknowledge. The IACKIN* signal indicates to the VME module that an acknowledge cycle is in progress.
IACKOUT*	1A: 22	INTERRUPT ACKNOWLEDGE OUT - Totem-pole driven signal. IACKIN* and IACKOUT* signals form a daisy-chained acknowledge. The IACKOUT* signal indicates to the next module that an acknowledge cycle is in progress.

TABLE 13-1. Connector P1 Signals (cont'd)

SIGNAL MNEMONIC	CONNECTOR AND PIN NUMBER	SIGNAL NAME AND DESCRIPTION
AM0-AM5	1A: 23 1B: 16,17 18,19 1C: 14	ADDRESS MODIFIER (bits 0-5) - Three-state driven lines that provide additional information about the address bus, such as size, cycle type, and/or DTB master identification
AS*	1A: 18	ADDRESS STROBE - Three-state driven signal that indicates a valid address is on the address bus.
A01-A23	1A: 24-30 1C: 15-30	ADDRESS bus (bits 1-23) - Three-state driven address lines that specify a memory address.
BBSY*	1B: 1	BUS BUSY - Open-collector driven signal generated by the current DTB master to indicate that it is using the bus.
BCLR*	1B: 2	BUS CLEAR - Totem-pole driven signal generated by the bus arbitrator to request release by the current DTB master in the event that a higher level is requesting the bus.
BERR*	1C: 11	BUS ERROR - Open-collector driven signal generated by a slave. This signal indicates that an unrecoverable error has occurred and the bus cycle must be aborted.
BG0IN*- BG3IN*	1B: 4,6 8,10	BUS GRANT (0-3) IN - Totem-pole driven signals generated by the Arbiter or Requesters. Bus grant in and out signals form a daisy-chained bus grant. The bus grant in signal indicates to this module that it may become the next bus master.
BG0OUT*- BG3OUT*	1B: 5,7 9,11	BUS GRANT (0-3) OUT - Totem-pole driven signals generated by Requesters. Bus grant in and out signals form a daisy-chained bus grant. The bus grant out signal indicates to the next board that it may become the next bus master.

TABLE 13-1. Connector P1 Signals (cont'd)

SIGNAL MNEMONIC	CONNECTOR AND PIN NUMBER	SIGNAL NAME AND DESCRIPTION
BR0*-BR3*	1B: 12-15	BUS REQUEST (0-3) - Open-collector driven signals generated by Requesters. These signals indicate that a DTB master in the daisy-chain requires access to the bus.
DS0*	1A: 13	DATA STROBE 0 - Three-state driven signal that indicates during byte and word transfers that a data transfer will occur on data bus lines (D00-D07).
DS1*	1A: 12	DATA STROBE 1 - Three-state driven signal that indicates during byte and word transfers that a data transfer will occur on data bus lines (D08-D15).
DTACK*	1A: 16	DATA TRANSFER ACKNOWLEDGE - Open-collector driven signal generated by a DTB slave. The falling edge of this signal indicates that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle.
D00-D15	1A: 1-8 1C: 1-8	DATA BUS (bits 0-15) - Three-state driven bidirectional data lines that provide a data path between the DTB master and slave.
GND*	1A: 9,11, 15,17,19 1B: 20,23 1C: 9	GROUND
IRQ1*-IRQ7*	1B: 24-30	INTERRUPT REQUEST (1-7) - Open-collector driven signals, generated by an interrupter, which carry prioritized interrupt requests. Level seven is the highest priority.
LWORD*	1C: 13	LONGWORD - Three-state driven signal to indicate that the current transfer is a 32-bit transfer.

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TABLE 13-1. Connector P1 Signals (cont'd)

SIGNAL MNEMONIC	CONNECTOR AND PIN NUMBER	SIGNAL NAME AND DESCRIPTION
SYSCLK	1A: 10	SYSTEM CLOCK - A constant 16 MHz clock signal that is independent of processor speed or timing. This signal is used for general system timing use.
SYSFAIL*	1C: 10	SYSTEM FAIL - Open-collector driven signal that indicates that a failure has occurred in the system. This signal may be generated by any module on the VMEbus.
SYSRESET*	1C: 12	SYSTEM RESET - Open-collector driven signal which, when low, will cause the system to be reset.
WRITE*	1A: 14	WRITE - Three-state driven signal that specifies the data transfer cycle in progress to be either read or write. A high level indicates a read operation; a low level indicates a write operation.
+5V STDBY	1B: 31	+5 Vdc STANDBY - This line supplies +5 Vdc to devices requiring battery backup.
+5V	1A: 32 1B: 32 1C: 32	+5 Vdc Power - Used by system logic circuits.
+12V	1C: 31	+12 Vdc Power - Used by system logic circuits.
-12V	1A: 31	-12 Vdc Power - Used by system logic circuits.

TABLE 13-2. Connectors J1 and J2 Pin Assignments

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1	DRSEL1	DRIVE SELECT 1 - This signal connects the drive 1 I/O interface to the control lines.
2	GND	GROUND.
3		No connection.
4	GND	GROUND.
5		No connection.
6	GND	GROUND.
7		No connection.
8	GND	GROUND.
9	SA1000TMGI	TIMING+ - This signal plus the TIMING- signal form a differential pair of clock signals.
10	SIGJ1-10	TIMING- - This signal plus the TIMING+ signal form a differential pair of clock signals.
11,12	GND	GROUND
13	WRDATAHD1	MFM WRITE DATA+ - This signal plus the MFM WRITE DATA- signal form a differential pair of high-speed write data signals.
14	SIGJ1-14	MFM WRITE DATA- - This signal plus the MFM WRITE DATE+ signal form a differential pair of high-speed write data signals.
15,16	GND	GROUND
17	DATA1	MFM READ DATA+ - This signal plus the READ DATA- signal form a differential pair of high speed read data signals.
18	HD1	MFM READ DATA- - This signal plus the READ DATA+ signal form a differential pair of high speed read data signals.
19,20	GND	GROUND

TABLE 13-3. Connector J3 Pin Assignments

	5-1/4" FLOPPY SA450	8" FLOPPY SA800	8" FLOPPY (DS) SA850	5-1/4" HARD ST506
1 2		RWC	RWC	RWC/Head Sel 2^3
3 4				HEAD SEL 2^2
5 6				WR. GATE
7 8				SK. COMPLETE
9 10		(NOTE)	TWO SIDED	TRACK 00
11 12				WR. FAULT
13 14			SIDE SEL	HEAD SEL 2^0
15 16				reserved
17 18	---	HEAD LOAD	HEAD LOAD	HEAD SEL 2^1
19 20		INDEX	INDEX	INDEX
21 22	---	READY	READY	READY
23 24	IX (INDEX)			STEP
25 26	DR. SEL 1	DR. SEL 1	DR. SEL 1	DR. SEL 1
27 28	DR. SEL 2	DR. SEL 2	DR. SEL 2	DR. SEL 2
29 30	DR. SEL 3	DR. SEL 3	DR. SEL 3	DR. SEL 3
31 32	MOTOR ON	DR. SEL 4	DR. SEL 4	DR. SEL 4
33 34	DIRECTION	DIRECTION	DIRECTION	DIRECTION
35 36	STEP	STEP	STEP	
37 38	WRITE DATA	WR. DATA	WR. DATA	
39 40	WRITE GATE	WR. GATE	WR. GATE	
41 42	TRACK 00	TRACK 00	TRACK 00	N/A
43 44	WR. PROTECT	WR. PROTECT	WR. PROTECT	
45 46	READ DATA	READ DATA	READ DATA	
47 48	SIDE SELECT			
49 50	"Special signal" Motor-on/Head-load for floppies			

NOTE: Always disable two-sided status from drive.

TABLE 13-4. Connector J4 Pin Assignments

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1-33 (Odd)	GND	GROUND
2	SPARE/DENSITY	SPARE/DENSITY allows optional control of motor speed/density on dual speed/density drives.
4	INUSE*/HEADLOAD*	IN USE/HEAD LOAD - This optional input to the disk drive is jumperable to a low state.
6	DRSEL4*	DRIVE SELECT 4 - This signal, when low, connects the drive 4 I/O interface to the control lines.
8	INDEX*	INDEX - This signal is driven by the drive once each revolution to indicate the beginning of a track. This line is valid on the high to low transition.
10	DRSEL1*	DRIVE SELECT 1 - This signal, when low, connects the drive 1 I/O interface to the control lines.
12	DRSEL2*	DRIVE SELECT 2 - This signal, when low, connects the drive 2 I/O interface to the control lines.
14	DRSEL3*	DRIVE SELECT 3 - This signal, when low, connects the drive 3 I/O interface to the control lines.
16	MTRON*	MOTOR ON - When this signal is low, the motor(s) in the 5-1/4 inch FDD(s) will be energized and start accelerating to operating speed.
18	DIR	DIRECTION - This signal defines the direction of motion of the read/write heads when the STEP line (pin 20) is pulsed. A high level when the STEP line is pulsed causes the read/write heads to move out away from the center of the disk. A low level when the STEP line is pulsed causes the read/write heads to move in towards the center of the disk.

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TABLE 13-4. Connector J4 Pin Assignments (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
20	STEP*	HEAD STEP - This signal causes the read/write heads to move in the direction defined by the DIR signal (pin 18).
22	WTDATA	FLOPPY WRITE DATA - This line carries the encoded write data to be recorded on the diskette.
24	WTGATE*	WRITE GATE - This signal controls the read/write mode of the selected drive. The write circuitry is enabled when WRGATE is low, provided the diskette is not write-protected.
26	TRK000*	TRACK ZERO - This signal indicates the read/write heads are positioned at cylinder zero (the outermost data track).
28	WTFLTPT*	WRITE PROTECT - This signal indicates the diskette in the drive is write-protected.
30	RDDATA	FLOPPY READ DATA - This line carries composite serial data from the selected diskette to the controller.
32	SIDESEL*	SIDE SELECT - This signal indicates when read/write head is used on the selected drive. When this signal is high, head 0 is selected. When this signal is low, head 1 is selected.
34	SPARE/READY*	SPARE/READY - This is an optional connection to the READY line of 5-1/4 inch floppy.

TABLE 13-5. MVME320B Parts List

LOCATION/REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
--	84-W8483B01	PWB for MVME320B
--	64-W5470B01	Front panel, MVME320B
--	67NW9415A17	Kit, ejector handle, 6U
--	33-W5089B59	Nameplate, Scanbe, MVME320B
--	33-W5089B01	Nameplate, Scanbe, logo
AR1	51NW9615P12	IC, NE530N, 8 pin
AR1	51NW9615T29	IC, NE538N, 8 pin
C1,C34,C41	23NW9618A79	Capacitor, electrolytic, 100 uF at 25 Vdc, 20%
C2-C5,C7-C26,C28, C29,C31,C33,C35-C39,C42-C46,C54, C58-C61,C64,C69, C72,C85-C87	21NW9632A03	Capacitor, ceramic, .1 uF at 50 Vdc, 20%
C6	21NW9629A06	Capacitor, mica, 20 pF at 500 Vdc, 5%
C27,C84	23NW9618A71	Capacitor, electrolytic, 47 uF at 10 Vdc, 20%
C30, C55	21NW9629A30	Capacitor, mica, 180 pF at 500 Vdc, 5%
C40,C56	21NW9629A11	Capacitor, mica, 33 pF at 500 Vdc, 5% (C56 value subject to change at test)
C47,C48	21NW9604A78	Capacitor, ceramic, 2.2K pF, 5%
C49,C53,C62	21NW9604A76	Capacitor, ceramic, 18K pF at 50 Vdc, 5%
C50	21NW9629A47	Capacitor, mica, .001 uF at 100 Vdc, 5%
C51,C52	23NW9618A82	Capacitor, electrolytic, 22 uF at 25 Vdc

TABLE 13-5. MVME320B Parts List (cont'd)

LOCATION/REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
C57	21NW9629A16	Capacitor, mica, 50 pF at 500 Vdc, 5%
C63	21NW9629A22	Capacitor, mica, 82 pF at 500 Vdc, 5%
C66	21NW9629A02	Capacitor, mica, 10 pF at 500 Vdc, 5%
C68	23NW9704B01	Capacitor, 4.7 uF at 10 Vdc, 20%
C73-C80	21SW992C008	Capacitor, ceramic, 150 pF at 50 Vdc
CR1,CR2,CR3	48NW9616A03	Diode, 1N4148/1N914
DL1	01NW9804B83	Delay module, digital, 50 ns
DL2	01-W4328B01	Delay module, triple, 20 ns
DS1	48NW9612A49	LED, red
J1,J2	28NW9802F98	Header, double row, right angle, 20-pin
J3	28NW9802F99	Header, double row, right angle, 50-pin
J4-J17	28NW9805C07	Pin, .025", square, autoinsert J4(1-34), J5(1-12), J6(1-6), J7(1-14), J8(1-3), J9(1-12), J10(1-3), J11(1-6), J12(1-2), J13(1-3), J14(1-3), J15(1-2), J16(1-2), J17(1-2)
L1	24NW9708A03	Inductor, 100 mH
P1	28NW9802E51	Connector, 96-pin
Q1	48NW9610A34	Transistor, NPN, 2N5320
Q2	48NW9610A13	Transistor, NPN, 2N2222
Q3	51NW9615N82	I.C. SD5000N
R1	06SW-124A41	Resistor, film, 470 ohms, 1/4 W, 5%
R2,R49	51NW9626A47	Resistor network, 8-pin, 7 per package, 4.7k ohms

TABLE 13-5. MVME320B Parts List (cont'd)

LOCATION/REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
R5,R6	06SW-124A35	Resistor, film, 270 ohms, 1/4 W, 5%
R7,R15,R21	51NW9626A41	Resistor network, 10-pin, 9 per package, 4.7k ohms
R9,R10	06SW-124A73	Resistor, film, 10k ohms, 1/4 W, 5%
R11	51NW9626A60	Resistor network, 8-pin, 6 per package, 220/330 ohms
R12	51NW9626A67	Resistor network, 10-pin, 8 per package, 220/330 ohms
R13,R22, R26,R27	06SW-124A49	Resistor, film, 1.0k ohms, 1/4 W, 5%
R16,R18,R19	51NW9626A53	Resistor network, 8-pin, 4 per package, 47 ohms
R17	51NW9626B02	Resistor network, 8-pin, 7 per package, 47 ohms
R20	06SW-961C68	Resistor, film, 4.99k ohms, 1/4 W, 1%
R23	06SW-124A81	Resistor, film, 22k ohms, 1/4 W, 5%
R24	06SW-124A45	Resistor, film, 680 ohms, 1/4 W, 5%
R25	06SW-124A39	Resistor, film, 390 ohms, 1/4 W, 5%
R27,R31,R37,R40	06SW-960D47	Resistor, film, 30.1k ohms, 1/8 W, 1%
R28	06SW-960D05	Resistor, film, fixed, 11.0k ohms, 1/8 W, 1%
R29,R31, R37,R40	06SW-960D47	Resistor, film, 30.1k ohms, 1/8 W, 1%
R30,R36	06SW-960B43	Resistor, film, 274 ohms, 1/8 W, 1%
R32,R33,R42	06SW-124A65	Resistor, film, 4.7k ohms, 1/4 W, 5%
R38	06SW-960B09	Resistor, film, 121 ohms, 1/8 W, 1%
R39	06SW-960B18	Resistor, film, 150 ohms, 1/8 W, 1%
R41	06SW-960E01	Resistor, film, 100k ohms, 1/8 W, 1%

TABLE 13-5. MVME320B Parts List (cont'd)

LOCATION/REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
R43	06SW-960C50	Resistor, film, fixed, 3.2k ohms, 1/8 W, 1%
R44	06SW-960B93	Resistor, film, 909 ohms, 1/8 W, 1%
R47	51NW9626A22	Resistor, network, 6-pin, 5 per package, 10k ohms
R48	51NW9626A46	Resistor, network, 6-pin, 5 per package, 4.7k ohms
U1	NOTE	Programmed I.C.
U3	NOTE	Programmed I.C.
U5,U7	51NW9615P41	I.C., AM2953DC
U6,U8	51NW9615H89	I.C., SN74LS645-1N
U9	(NOTE)	Programmed I.C.
U11,U59,U63, U87-U90	51NW9615F52	I.C., SN74LS273N
U12	51NW9615S11	I.C., AM29824PC
U13	51NW9615N81	I.C., SN74LS642-1N
U14	51NW9615F79	I.C., SN74S240N
U15	51NW9615N06	I.C., N8X305N
U16,U20,U24, U67,U70	51NW9615J39	I.C., 74F74PC
U17	51NW9615K70	I.C., 74F08PC
U18,U22	51NW9615P17	I.C., 74F112PC
U19	51NW9615T31	I.C., 74F1240N
U21,U55,U56	51NW9615K66	I.C., 74F32PC
U23	51NW9615K16	I.C., 74F521PC
U25	51NW9615E98	I.C., SN74LS373N

TABLE 13-5. MVME320B Parts List (cont'd)

LOCATION/REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
U26,U27,U31,U32, U36,U37	51NW9615F23	I.C., SN74LS163AN
U28,U33,U38	51NW9615T32	I.C., 74F1244N
U29,U30	51NW9615N51	I.C., UPD2149D
U34	51NW9615K70	I.C., 74F08PC
U35	51NW9615F65	I.C., SN74S241N
U39	51NW9615K68	I.C., 74F11PC
U40	51NW9615E95	I.C., SN74LS240N
U41,U45	51NW9615C69	I.C., SN74LS138N
U42	51NW9615C34	I.C., SN74S138N
U43	(NOTE)	Programmed I.C.
U44,U49	51NW9615N83	I.C., AM29825PC
U46	51NW9615C29	I.C., SN74LS174N
U47	(NOTE)	Programmed I.C.
U48,U53	51NW9615F02	I.C, SN74LS244N
U50	(NOTE)	Programmed I.C.
U51	(NOTE)	Programmed I.C.
U52	(NOTE)	Programmed I.C.
U54	51NW9615P24	I.C., N8X371N
U57	51NW9615P20	I.C., DM74LS952N
U58	51NW9615L69	I.C., SN74LS377N3
U60,U72	51NW9615E93	I.C., SN74LS14N
U61,U91	51NW9615K71	I.C., 74F04PC
U62	(NOTE)	Programmed I.C.

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TABLE 13-5. MVME320B Parts List (cont'd)

LOCATION/REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
U64	(NOTE)	Programmed I.C.
U65	51NW9615E91	I.C., SN74LS00N
U68,U79	51NW9615C26	I.C., SN74LS123N
U69	(NOTE)	Programmed I.C.
U71	51NW9615L98	I.C., AM26LS31PC
U73,U76,U77	51NW9615F38	I.C., SN74LS393N
U74	51NW9615C24	I.C., SN74LS32N
U75	51NW9615F60	I.C., MC3486P
U78	51NW9615T14	I.C., MC74F10N
U80,U92	51NW9615E84	I.C., SN74LS153N
U81	51NW9615K62	I.C., 74F153PC
U82	51NW9615T15	I.C., MC74F74N
U83	51NW9615A28	I.C., MC4024P
U84	51NW9615K72	I.C., 74F02PC
U85,U86	51NW9615F01	I.C., SN74LS86N
VR1	51NW9615E11	I.C., MC7805CT
Y1	48AW1015B07	Crystal oscillator, 16 MHz
Y2	48AW1014B11	Crystal oscillator, 10 MHz
--	14NW9416A01	Pad, mounting, nylon (use at Q1)
--	09-4659B12	Socket, I.C., SIL, 12-pin (use at U1, U3, and U9)
--	09NW9811A78	Socket, I.C., DIL, 20-pin (use at U43, U50, U52, U64, and U69)

TABLE 13-5. MVME320B Parts List (cont'd)

LOCATION/REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
--	09NW9811A86	Socket, I.C,. DIL, 16-pin (use at Q3, and U62)
--	09-W4659B25	Socket, I.C., SIL, 25-pin (use at 15)
--	09NW9811B01	Socket, I.C., DIL, 24-pin (use at U47)
--	09NW9811A78	Socket, I.C., DIL, 20-pin (use at U51)
--	29NW9805B17	Jumper, shorting, insulated

NOTE: When ordering, use number labeled on part.

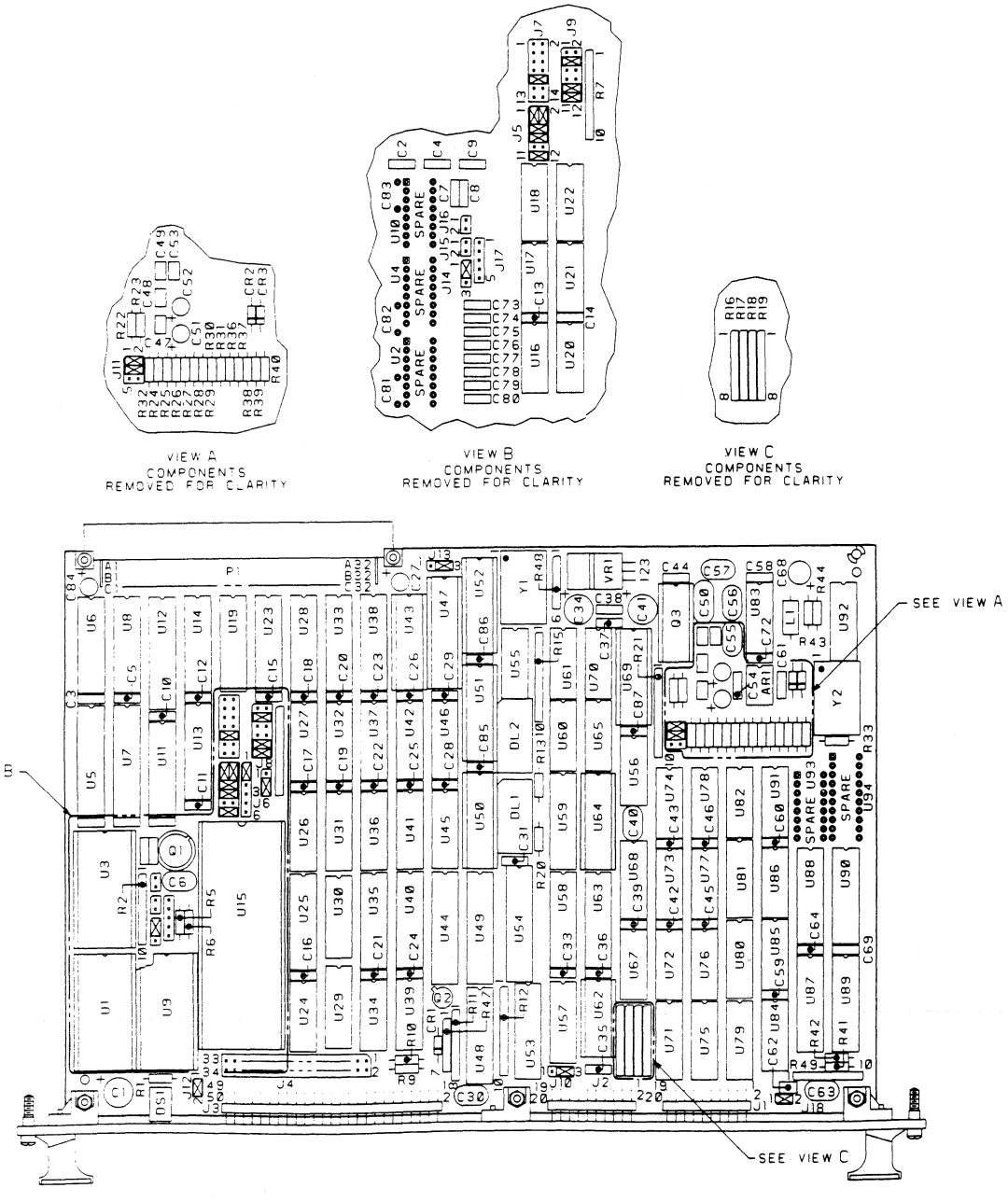


FIGURE 13-1. MVME320B Parts Location Diagram (Sheet 1 of 2)

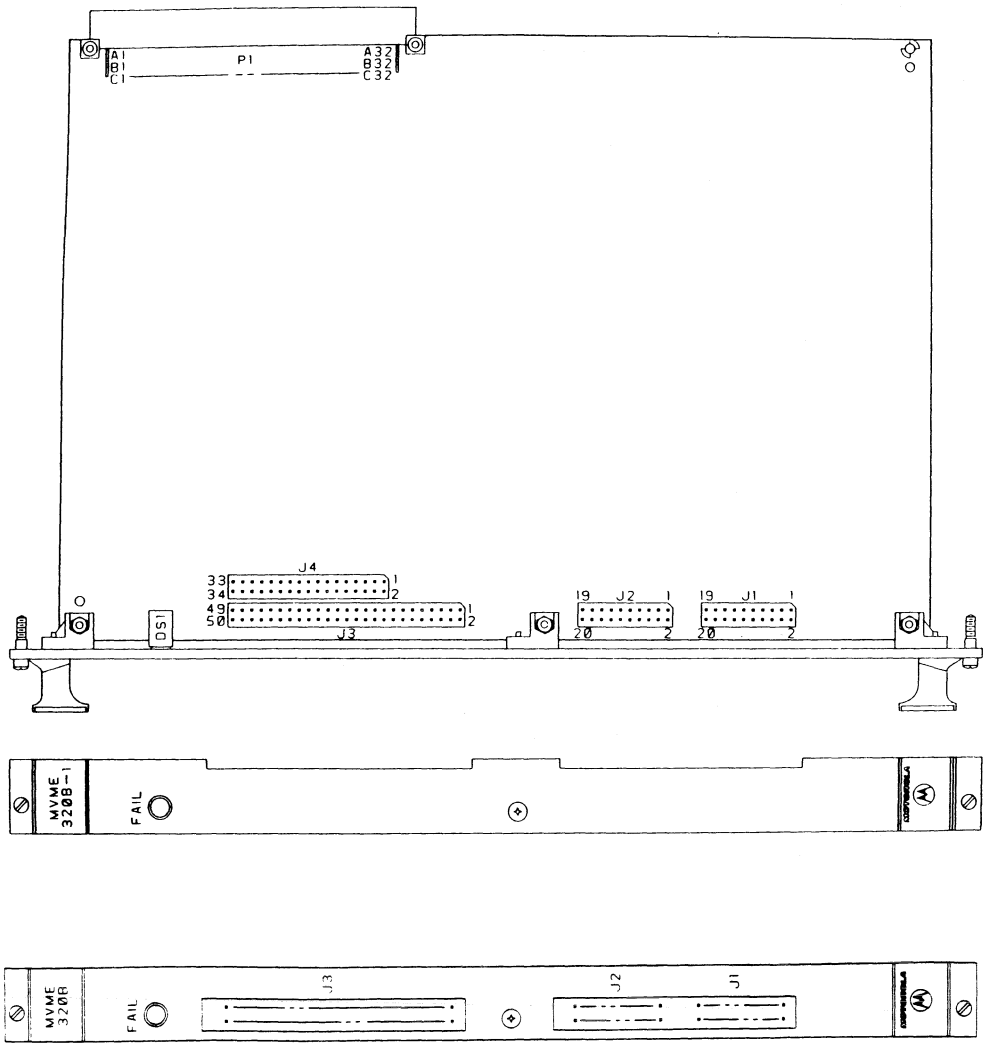


FIGURE 13-1. MVME320B Parts Location Diagram (Sheet 2 of 2)

13

13.4 SCHEMATIC DIAGRAMS

A detailed schematic diagram for the MVME320B is provided in Figure 13-2. This schematic diagram represents the latest design. Occasionally, minor component changes are made at the factory. Therefore, when replacing a component, always use the same value as the defective component, even though the schematic diagram may indicate a different value or type.

NOTES:

1. FOR REFERENCE DRAWINGS REFER TO BILL(S) OF MATERIAL 01-W3483B01, B02
2. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, ±5PCT, 1/4 WATT.
   ALL CAPACITORS ARE IN UF.
   ALL VOLTAGES ARE DC.
3. INTERRUPTED LINES CODED WITH THE SAME LETTER OR LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.
4. DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH THE MANUFACTURER.
5. SPECIAL SYMBOL USAGE:
   * DENOTES - ACTIVE LOW SIGNAL.
   [] DENOTES - ON BOARD SIGNAL.
6. INTERPRET DIAGRAM IN ACCORDANCE WITH AMERICAN NATIONAL STANDARDS INSTITUTE SPECIFICATIONS, CURRENT REVISION.
7. PART TYPES ARE ABBREVIATED IN THE FIELD OF THE DRAWING, FOR FULL PART TYPE, REFER TO TABLE 1.
8. CODE FOR SHEET TO SHEET REFERENCES IS AS FOLLOWS: SHEET 6 A6 ZONE
9. PART NOT INSTALLED - USER OPTION.

Y2	
VR1	
U94	U66
R49	R3,4,8,14,34,35
Q3	
P1	
L1	
J18	
DL2	
DS1	
CR3	
C87	C32,65,66, 67,70,71
AR1	
HIGHEST NUMBER USED	NOT USED

REFERENCE DESIGNATIONS

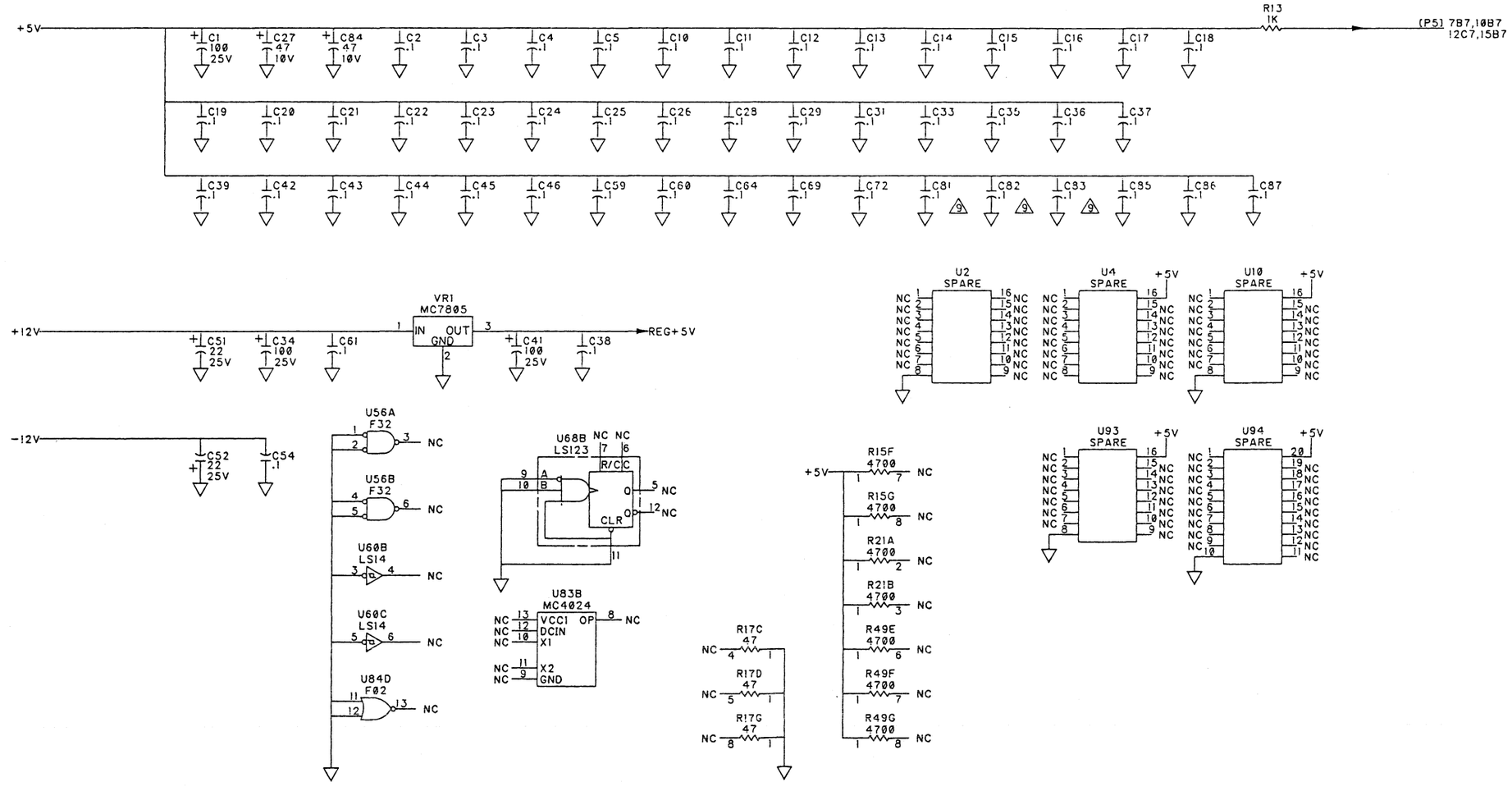
7 TABLE 1

REF DES	TYPE 4	GND	+5V	+12V	-12V	SH
AR1	NE530			7	4	11
DL1	50NS	7	14			14
DL2	20NS	7	14			8
U1	HM76321	12	24			10
U2	SPARE					2
U3	HM76321	12	24			10
U4	SPARE					2
U5	AM2953	12	24			5
U6	74LS645	10	20			5
U7	AM2953	12	24			5
U8	74LS645	10	20			5
U9	HM76321	12	24			10
U10	SPARE					2
U11	74LS273	10	20			7
U12	AM29824	12	24			5
U13	74LS642	10	20			14
U14	74S240	10	20			15,16
U15	8X305	12	37			10
U16	74F74	7	14			16
U17	74F08	7	14			10,15
U18	74F112	8	16			10
U19	74F1240	10	20			15
U20	74F74	7	14			16
U21	74F32	7	14			7,9
U22	74F112	8	16			10,12
U23	74F521	10	20			8
U24	74F74	7	14			16
U25	74LS373	10	20			9
U26	74LS163A	8	16			6
U27	74LS163A	8	16			6
U28	74F1244	10	20			6
U29	UPD2149-2	9	18			9
U30	UPD2149-2	9	18			9
U31	74LS163A	8	16			6
U32	74LS163A	8	16			6
U33	74F1244	10	20			6
U34	74F08	7	14			9,11
U35	74S241	10	20			7
U36	74LS163A	8	16			6
U37	74LS163A	8	16			6
U38	74F1244	10	20			6
U39	74F11	7	14			8,9
U40	74LS240	10	20			7
U41	74LS138	8	16			7
U42	74S138	8	16			7
U43	PAL16L8B	10	20			8
U44	AM29825	12	24			13
U45	74LS138	8	16			7
U46	74LS174	8	16			7
U47	PAL20R4B	12	24			15
U48	74LS244	10	20			13
U49	AM29825	12	24			13
U50	PAL16R6B	10	20			14
U51	PAL16L8B	10	20			8
U52	PAL16L8B	10	20			16
U53	74LS244	10	20			13
U54	8X371	12	24			9
U55	74F32	7	14			5,13,16
U56	74F32	7	14			2,7
U57	74LS952	9	18			13

7 TABLE 1 CONT

REF DES	TYPE 4	GND	+5V	REG +5V	SH
U58	74LS377	10	20		13
U59	74LS273	10	20		13
U60	74LS14	7	14		2,8,11,14,16
U61	74F04	7	14		7,8,9,15,16
U62	82S129	8	16		13
U63	74LS273	10	20		13
U64	82S147A	10	20		13
U65	74LS00	7	14		10,12,13,14
U67	74F74	7	14		15,16
U68	74LS123	8	16		2,9
U69	PAL16R4B	10	20		8
U70	74F74	7	14		10,12
U71	AM26LS31	8	16		14
U72	74LS14	7	14		11,12,14
U73	74LS393	7	14		12
U74	74LS32	7	14		7,11,12,13
U75	MC3486	8	16		14
U76	74LS393	7	14		12
U77	74LS393	7	14		12
U78	74F10	7		14	11
U79	74LS123	8	16		10
U80	74LS153	8	16		12
U81	74F153	8	16		12
U82	74F74	7		14	11
U83	MC4024	7	14		2,11
U84	74F02	7	14		2,12,13
U85	74LS86	7	14		12
U86	74LS86	7	14		12,13
U87	74LS273	10	20		12
U88	74LS273	10	20		12
U89	74LS273	10	20		12
U90	74LS273	10	20		12
U91	74F04	7	14		7,8,9,11,15
U92	74LS153	8	16		11
U93	SPARE				2
U94	SPARE				2
Q3	SD5000	2			11
Y1	K1100A	7	14		15
Y2	K1114AM	7	14		12

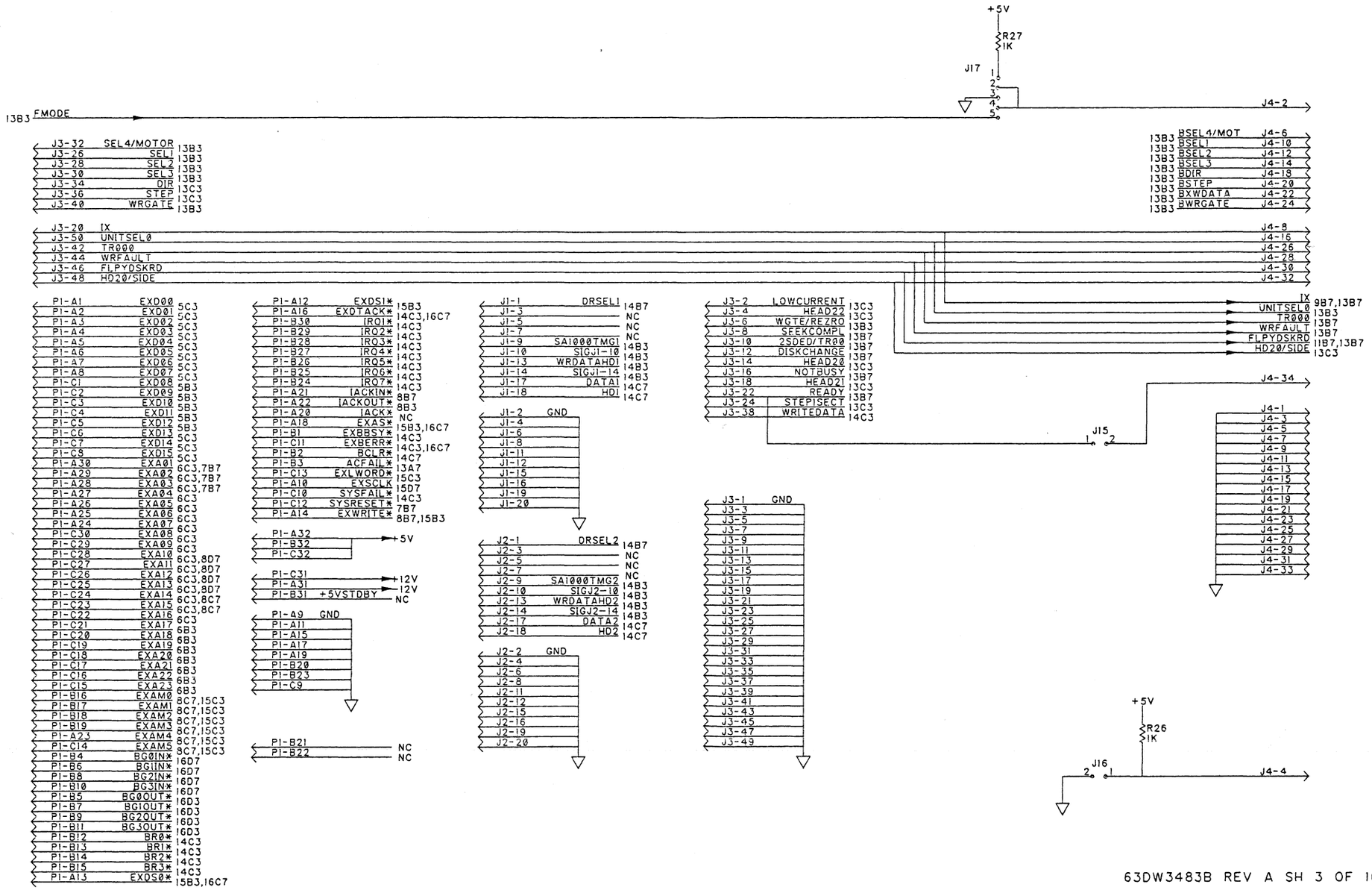
FIGURE 13-2. Schematic Diagram
13-19/20



NOT USED

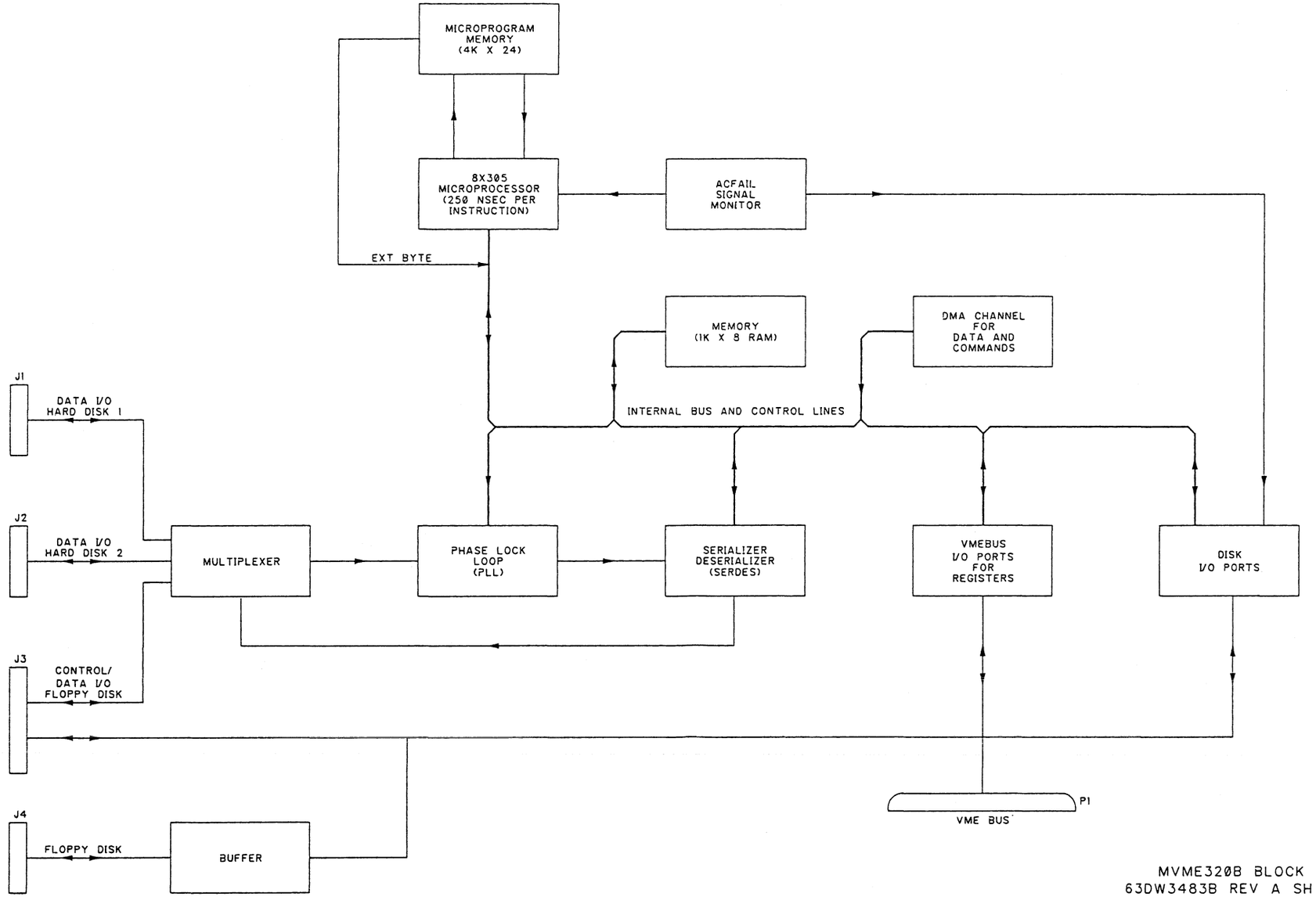
63DW3483B REV A SH 2 OF 16

FIGURE 13-2. Schematic Diagram
13-21/22



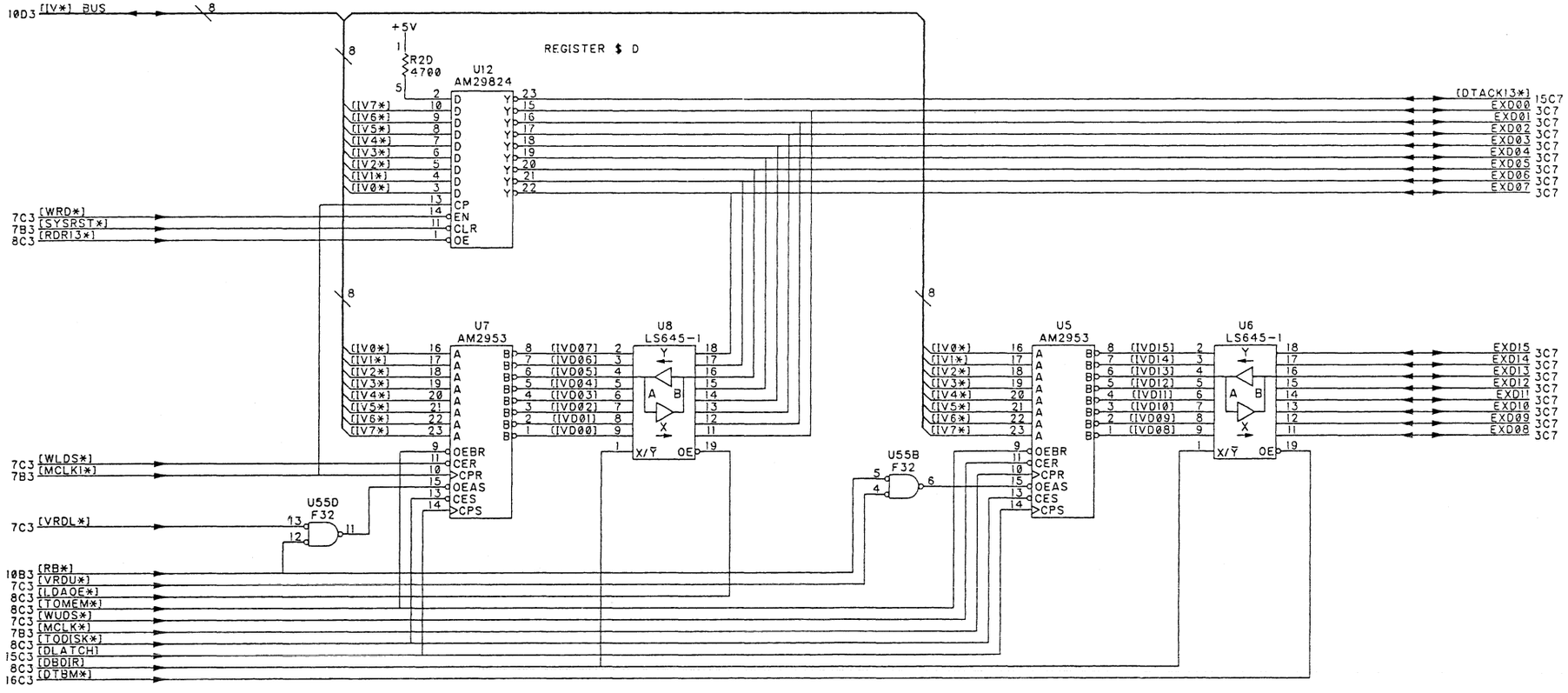
63DW3483B REV A SH 3 OF 16

FIGURE 13-2. Schematic Diagram
13-23/24



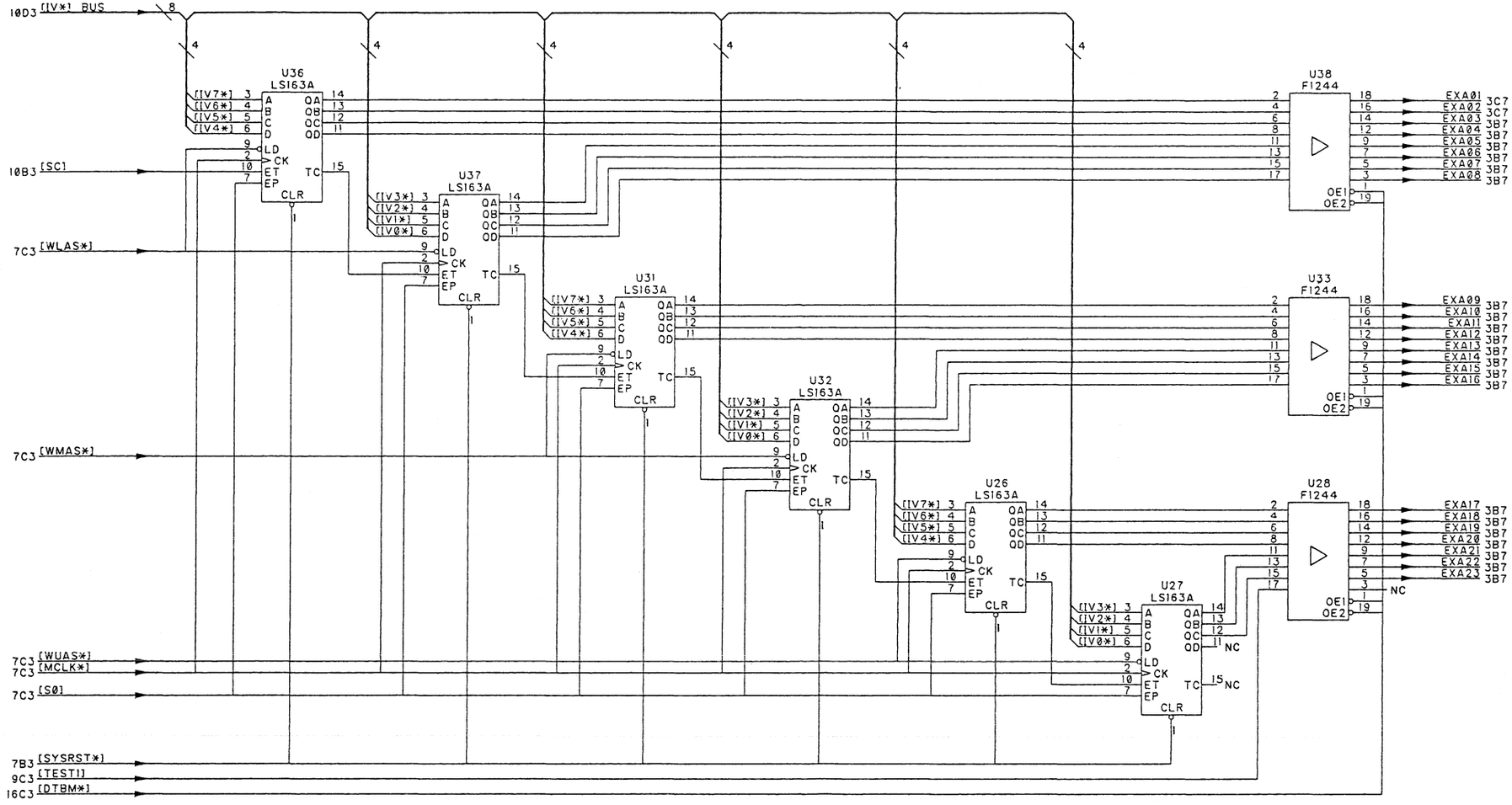
MVME320B BLOCK DIAGRAM
63DW3483B REV A SH 4 OF 16

FIGURE 13-2. Schematic Diagram
13-25/26



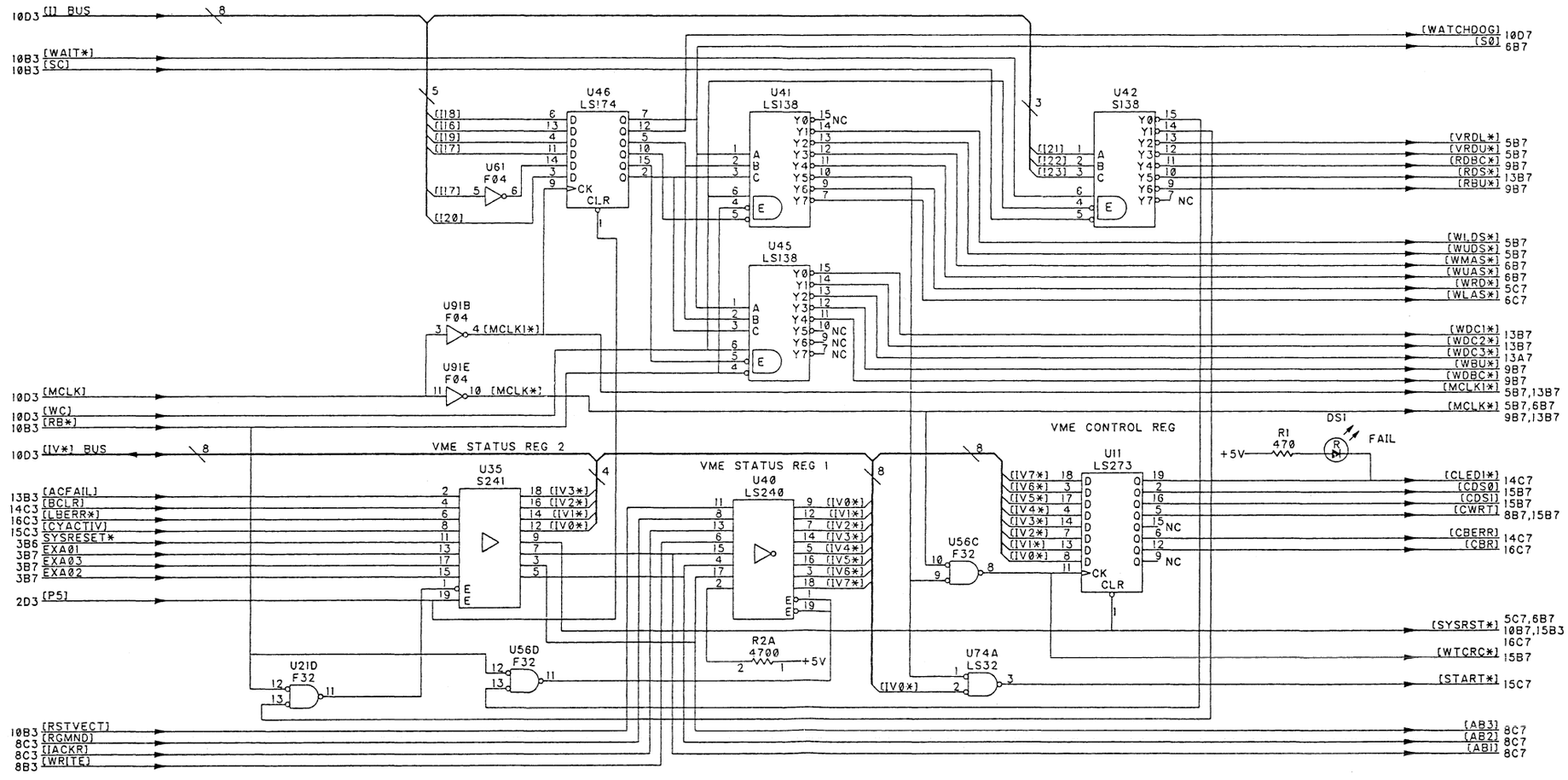
VME DATA BUS INTERFACE
63DW3483B REV A SH 5 OF 16

FIGURE 13-2. Schematic Diagram
13-27/28



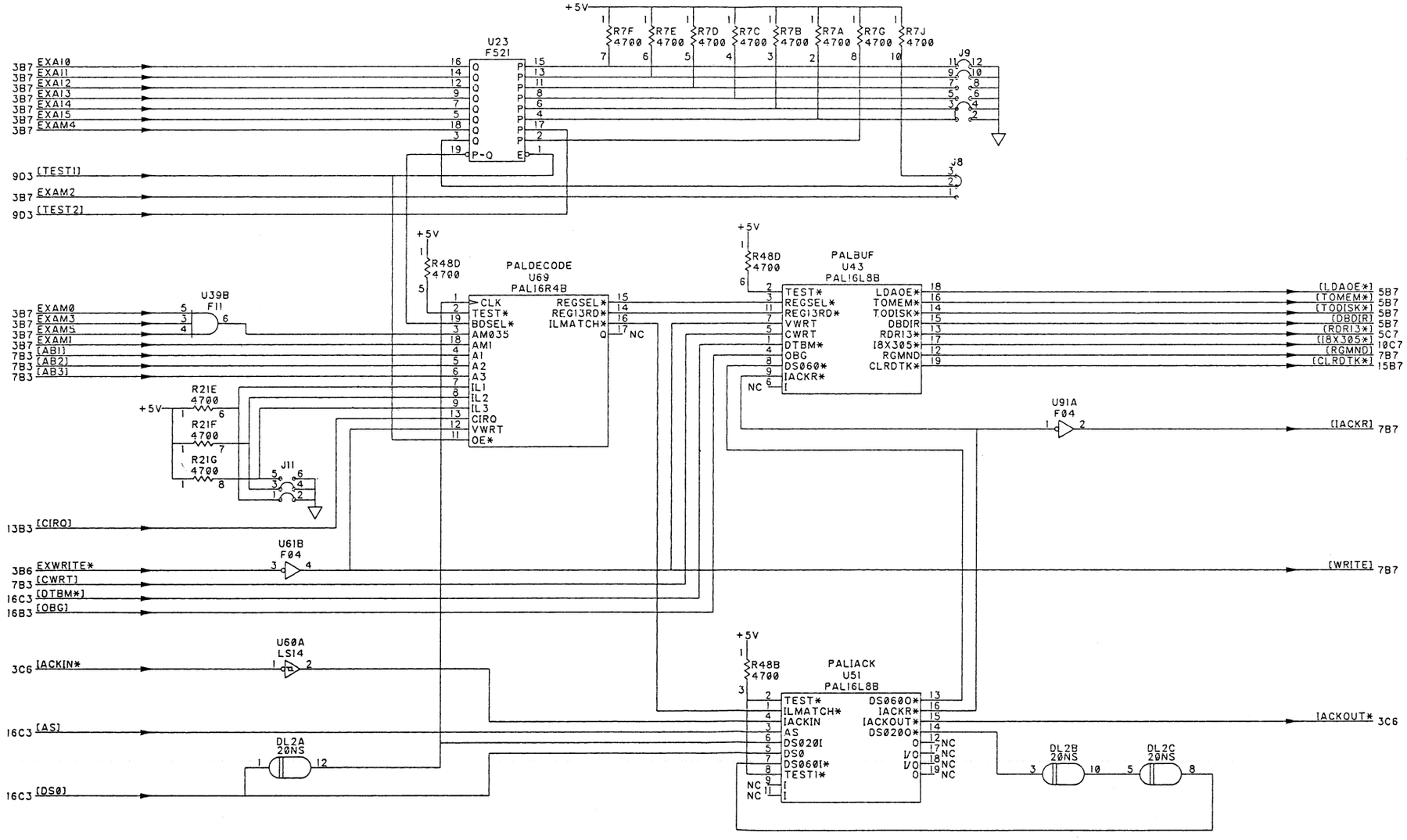
ADDRESS BUS INTERFACE
63DW3483B REV A SH 6 OF 16

FIGURE 13-2. Schematic Diagram
13-29/30



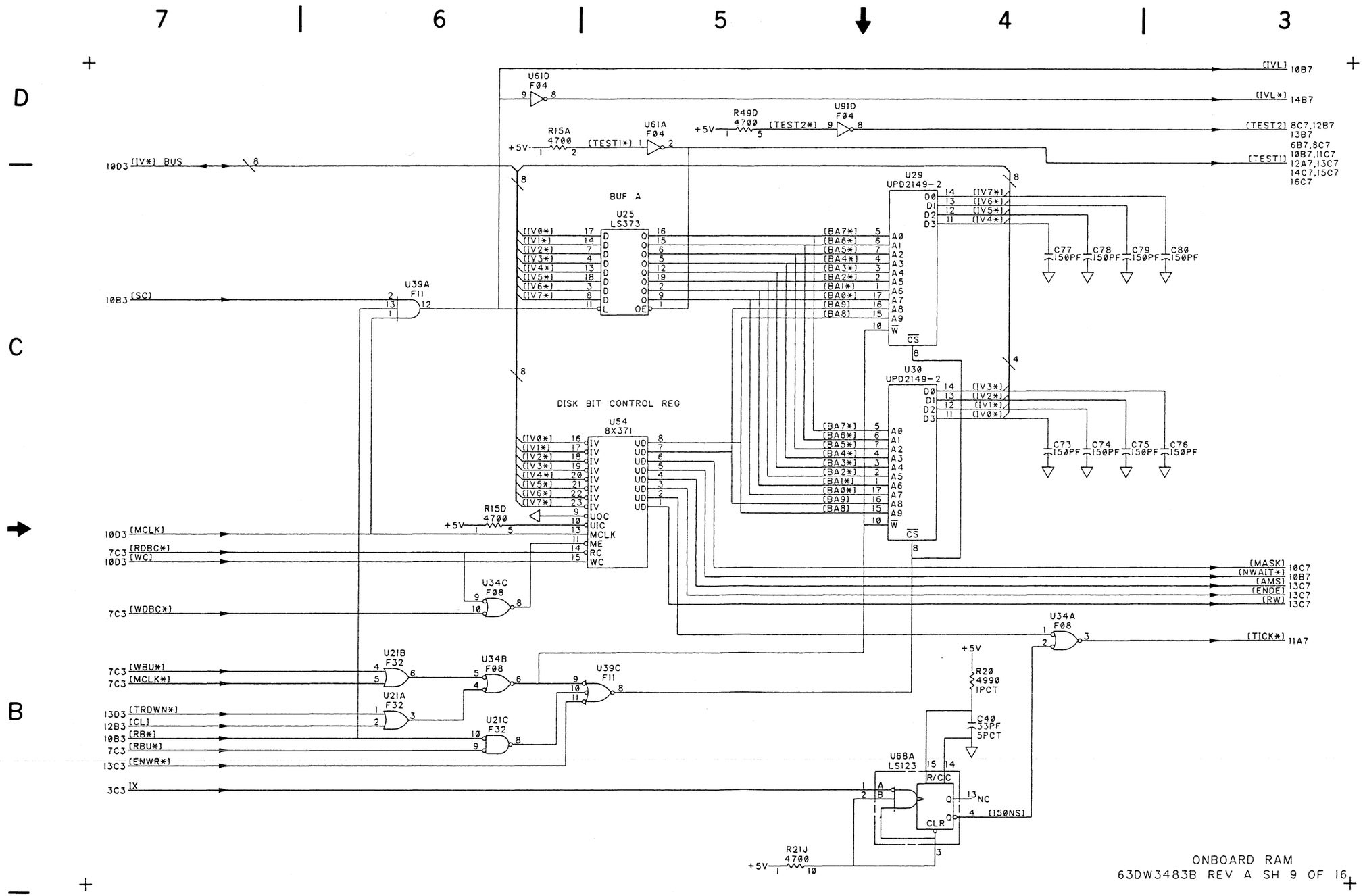
REGISTER DECODING
63DW3483B REV A SH 7 OF 16

FIGURE 13-2. Schematic Diagram
13-31/32



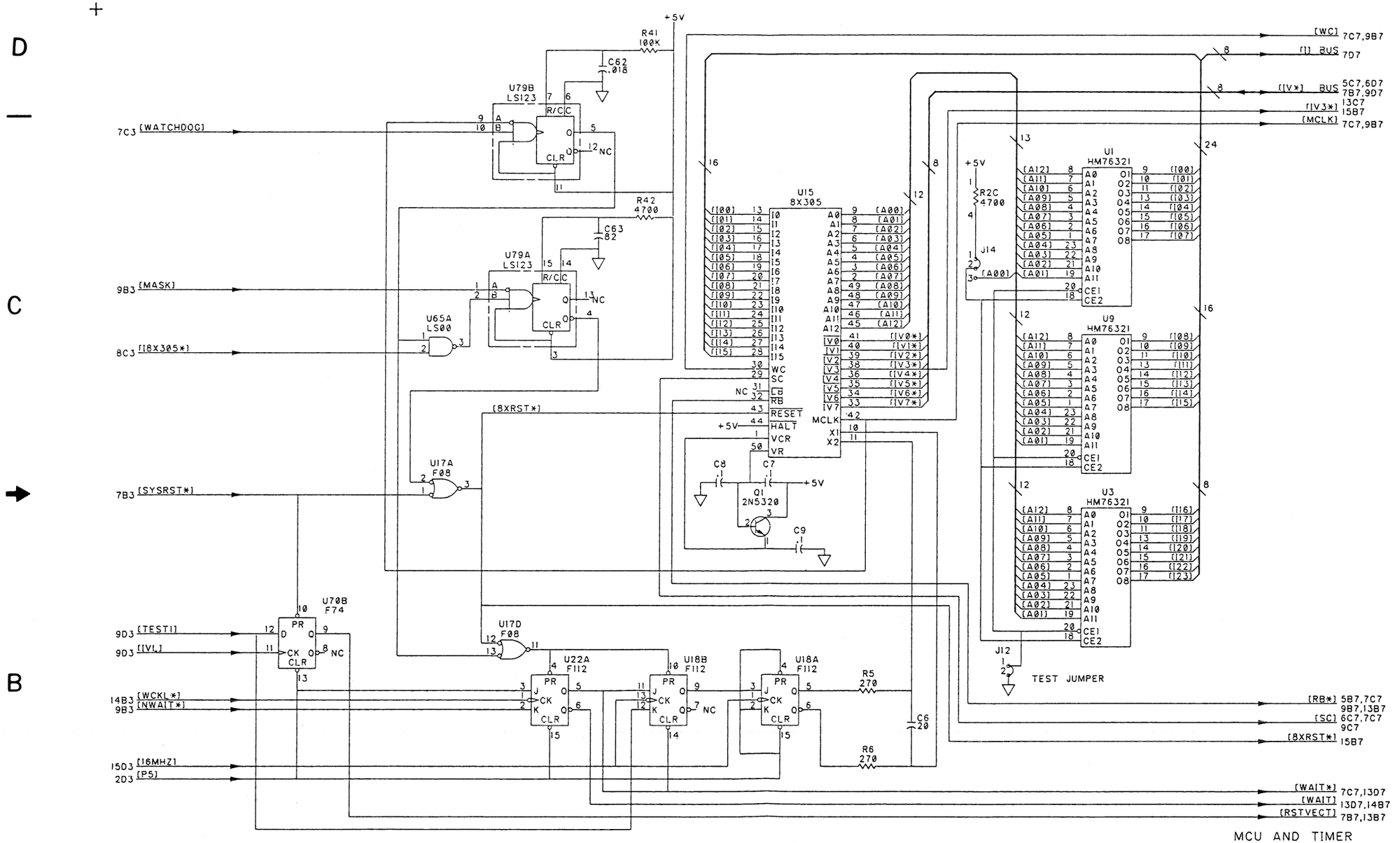
VMEBUS CONTROL LOGIC
63DW3483B REV B SH 8 OF 16

FIGURE 13-2. Schematic Diagram
13-33/34



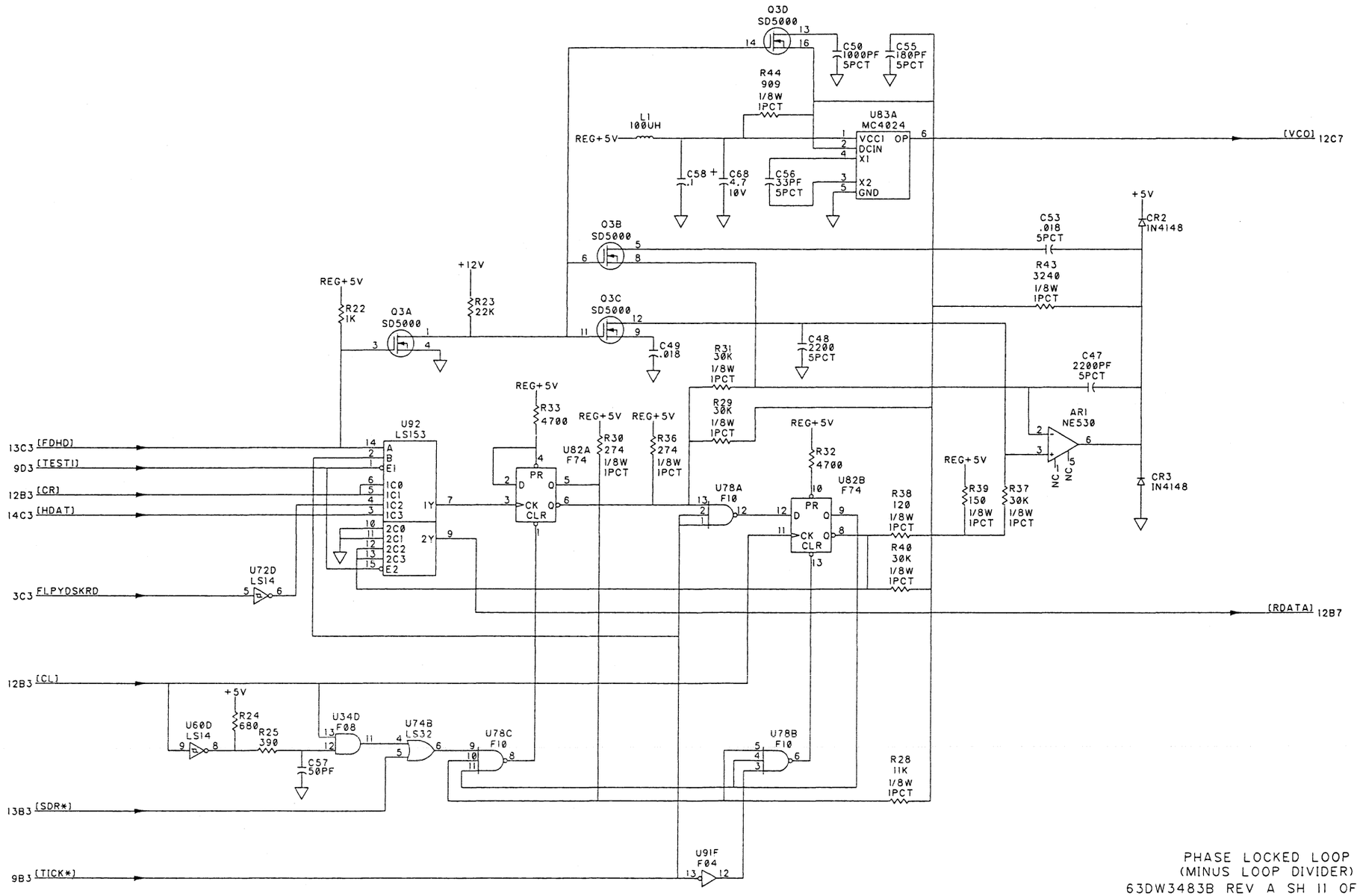
ONBOARD RAM
63DW3483B REV A SH 9 OF 16

FIGURE 13-2. Schematic Diagram
13-35/36



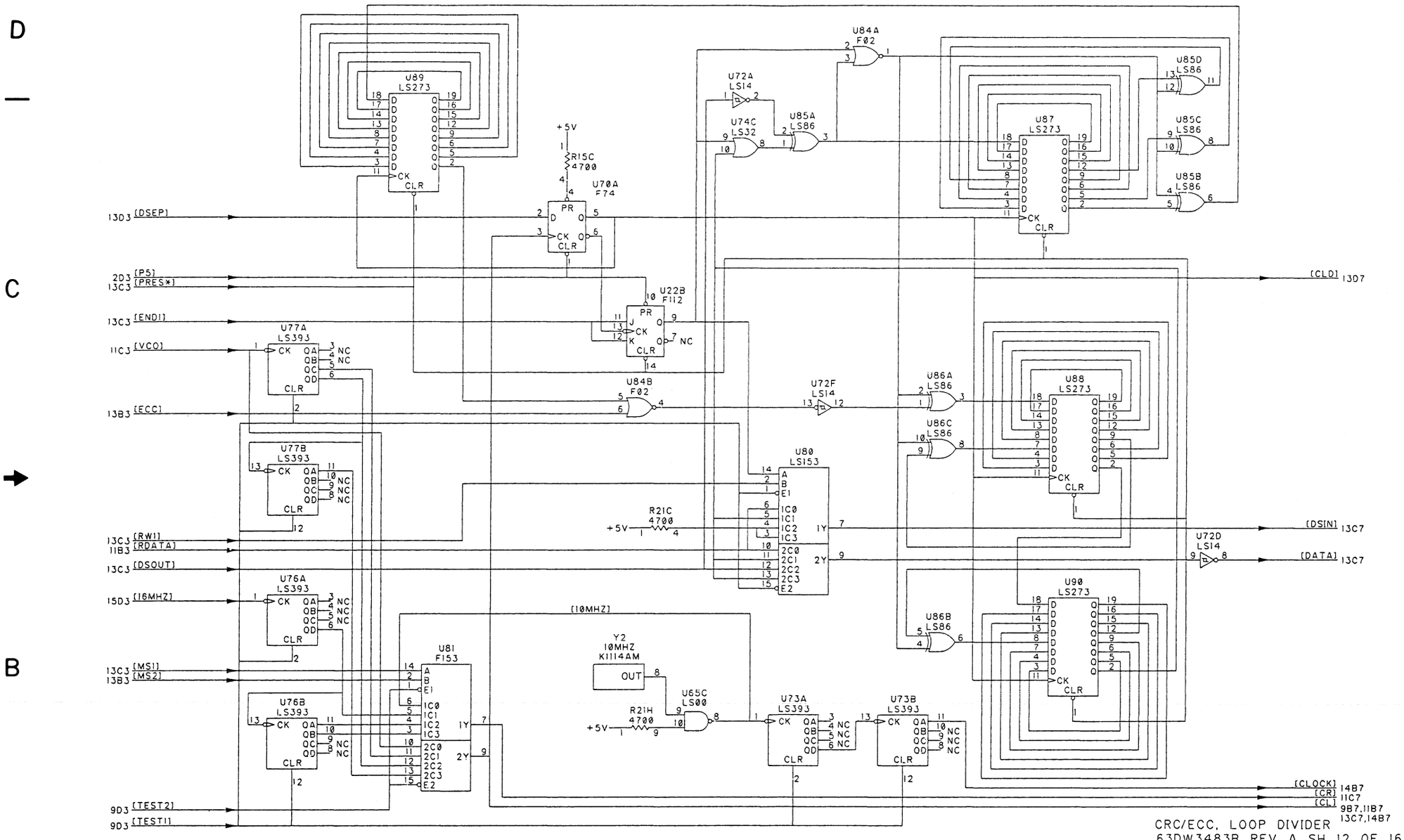
MCU AND TIMER
63DW3483B REV B SH 10 OF 16

FIGURE 13-2. Schematic Diagram
13-37/38



PHASE LOCKED LOOP
(MINUS LOOP DIVIDER)
63DW3483B REV A SH 11 OF 16

FIGURE 13-2. Schematic Diagram
13-39/40



CRC/ECC, LOOP DIVIDER
63DW3483B REV A SH 12 OF 16

FIGURE 13-2. Schematic Diagram
13-41/42

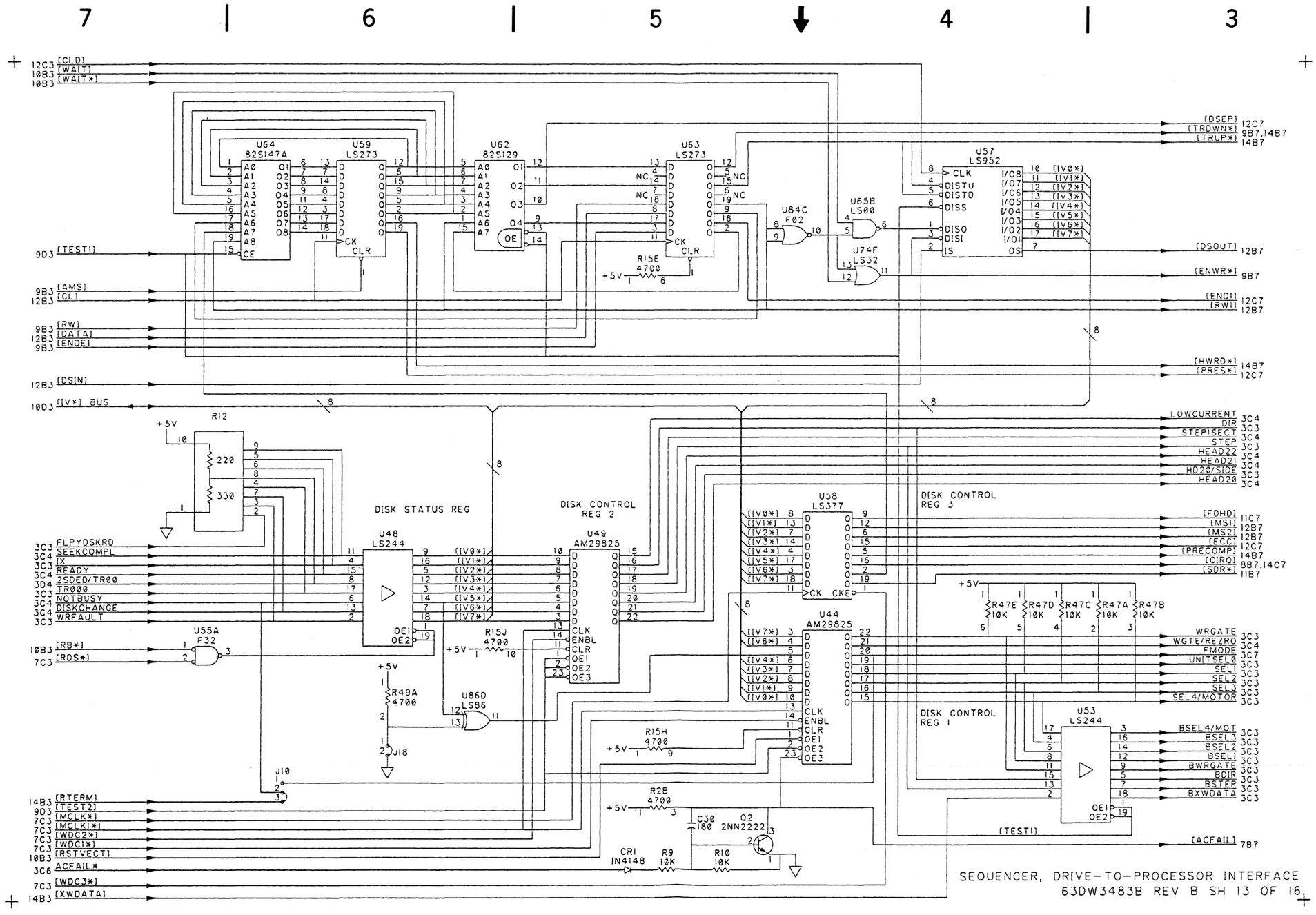
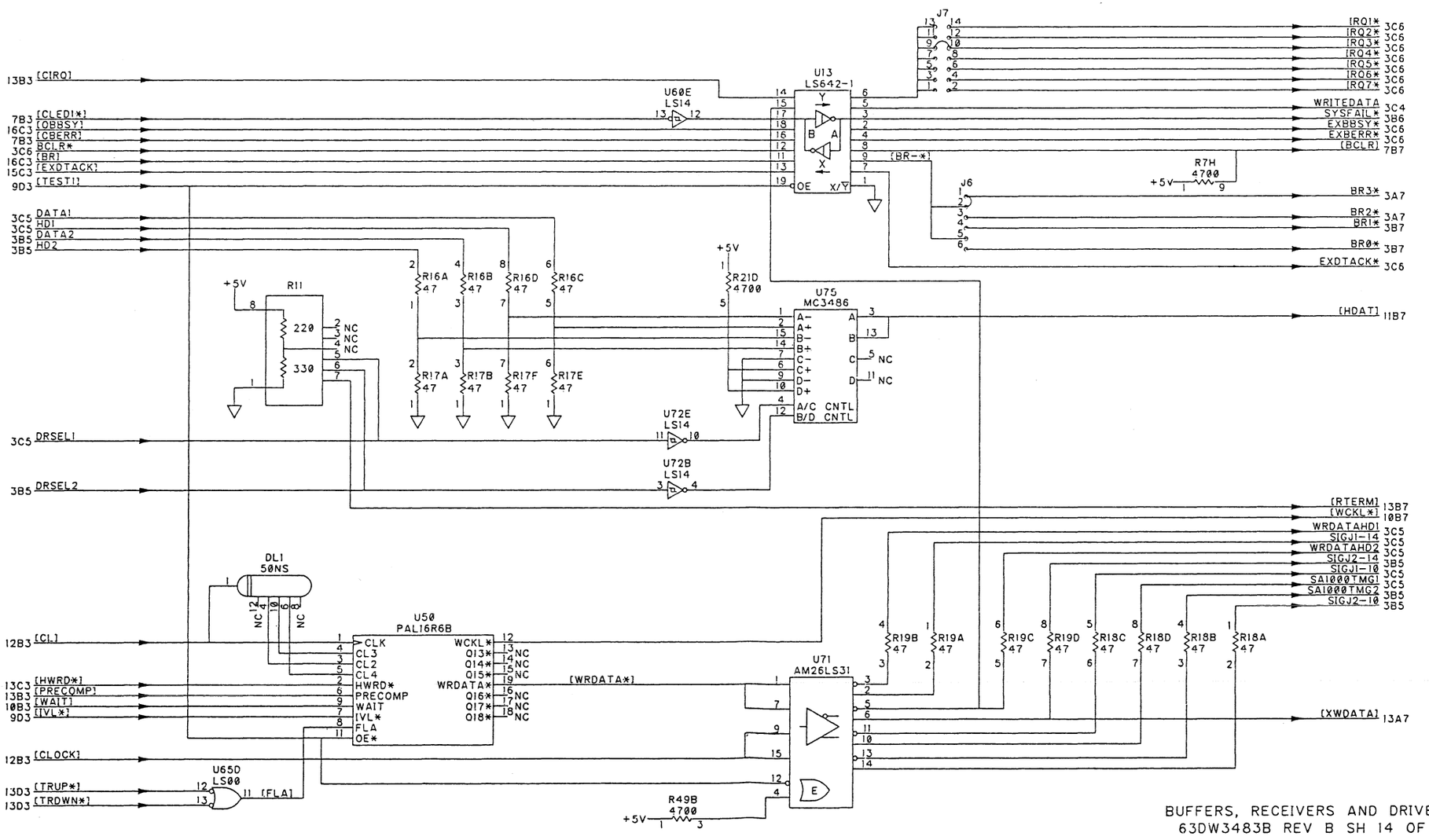
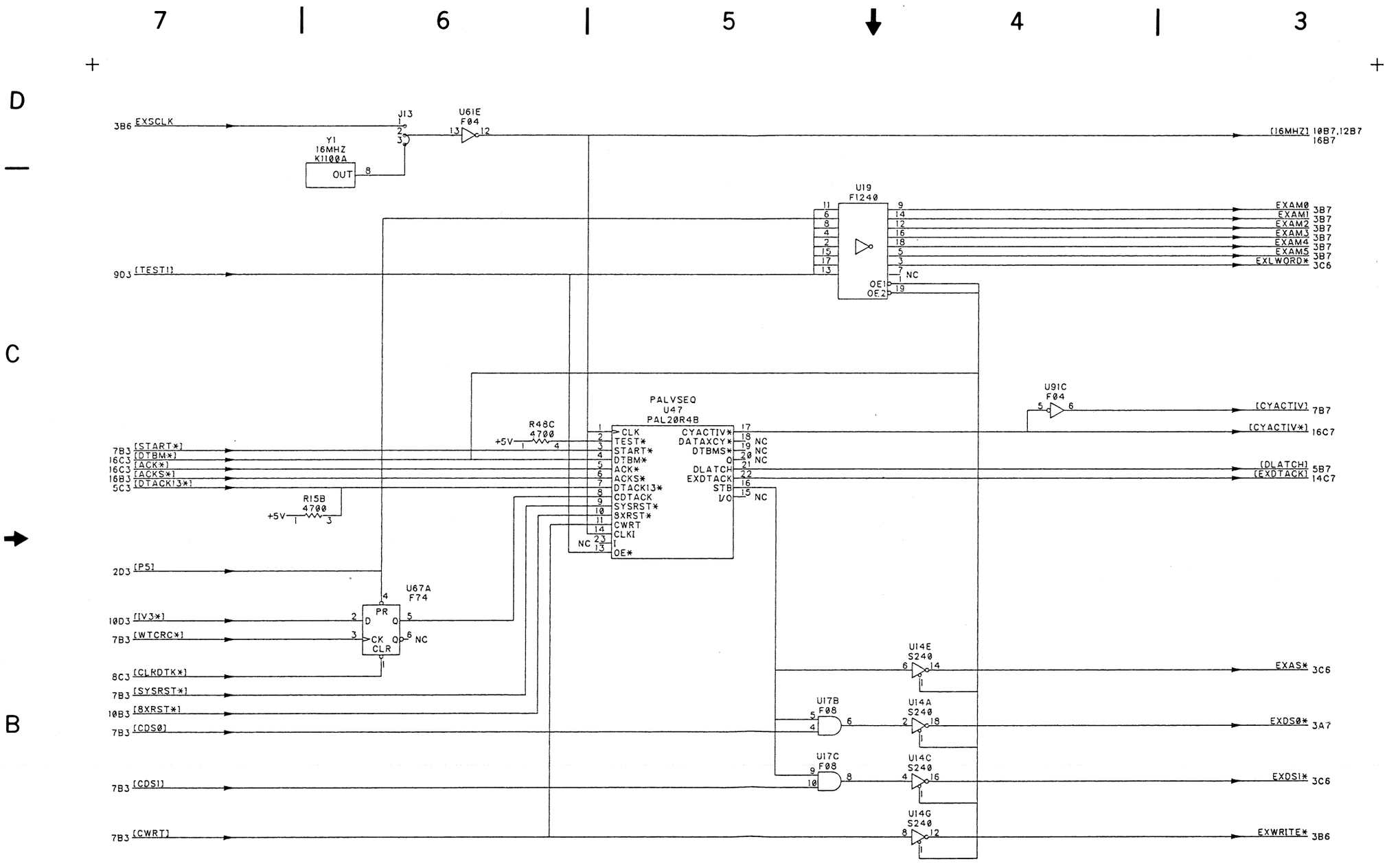


FIGURE 13-2. Schematic Diagram
13-43/44



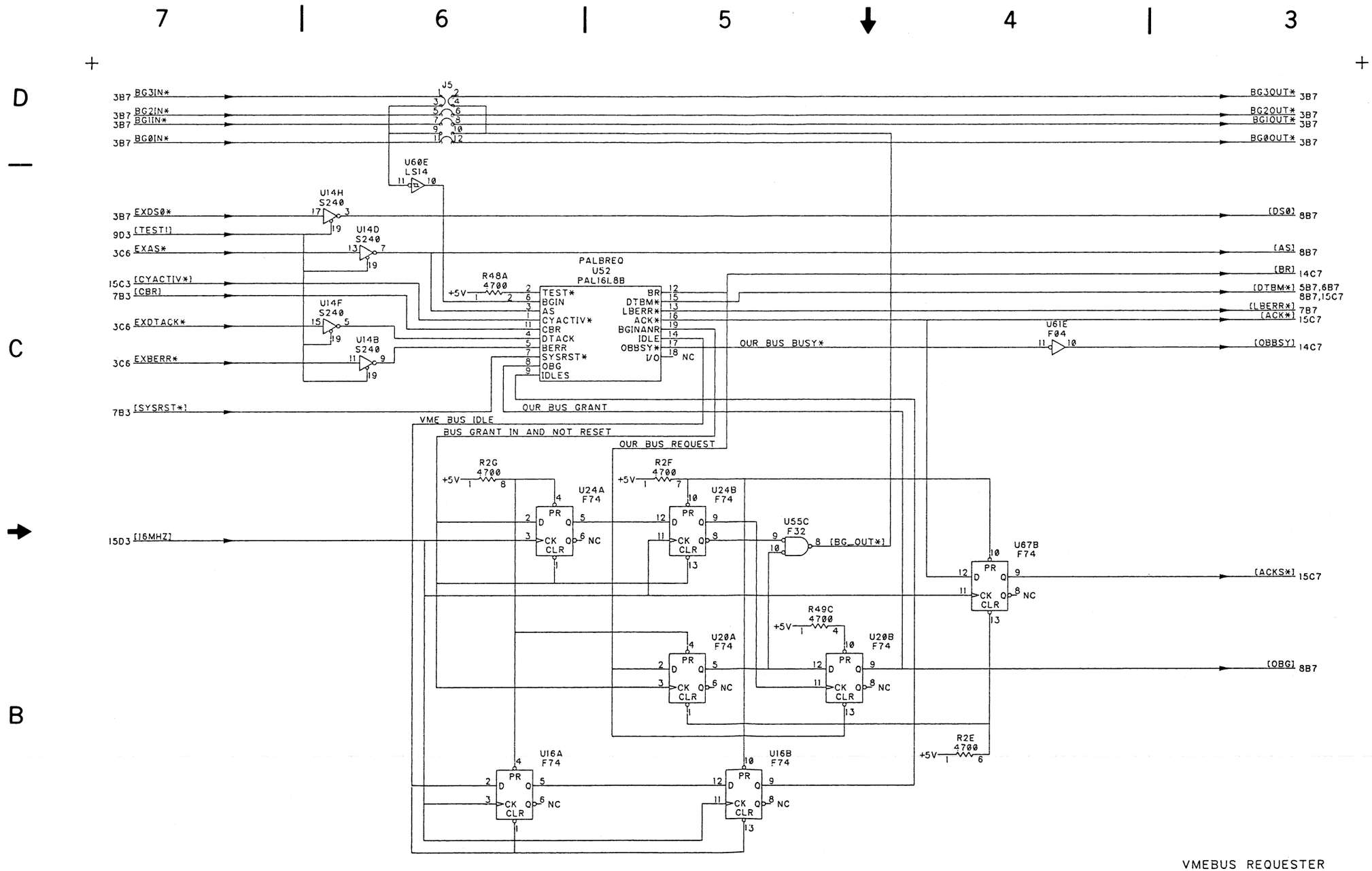
BUFFERS, RECEIVERS AND DRIVERS
63DW3483B REV B SH 14 OF 16

FIGURE 13-2. Schematic Diagram
13-45/46



VMEBUS MASTER INTERFACE
63DW3483B REV B SH 15 OF 16

FIGURE 13-2. Schematic Diagram
13-47/48



VMEBUS REQUESTER
63DW3483B REV B SH 16 OF 16

FIGURE 13-2. Schematic Diagram
13-49/50

APPENDIX A - DISK FORMATS

A.1 INTRODUCTION

This appendix describes 8-inch and 5-1/4 inch hard disk and diskette formats.

A.2 5-1/4 INCH HARD DISK FORMATS

The industry standard format for 5-1/4 inch hard disks is 32 sectors/track, 256 bytes/sector; however, the MVME320B supports:

- Sector lengths of 128, 256, and 512 bytes per sector
- Up to 8 heads per drive, and
- Up to 64K cylinders per drive.

Each sector on the track consists of two fields separated by gaps to allow updating and recovery. The first field in the sector is the sector identifier (ID). The ID field contains four data type bytes for unique identification of the sector. These four bytes are:

- Cylinder number
- Head number
- Sector number
- Length code

The second field in the sector is the data field containing user data. The track format used for 5-1/4 inch hard disk drives is shown in Figure A-1.

The recording method used is MFM on all tracks. MFM is encoded using the following rules:

a. Write data bits at the center of the cell.

b. Write clock bits at the beginning of the cell if:

No data was written in the previous cells
No data will be written in the present cell.

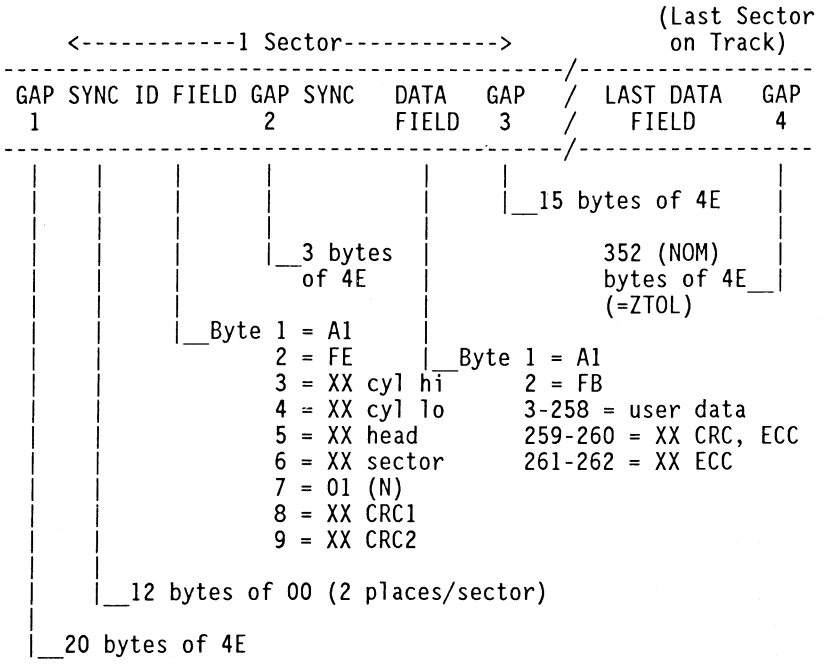


FIGURE A-1. Recommended Hard Disk Track Format (256 Bytes/Sector)

A

A.3 8-INCH AND 5-1/4 INCH DISKETTE FORMATS

The track formats supported on the diskette drives are listed in Table A-1.

TABLE A-1. Diskette Formats

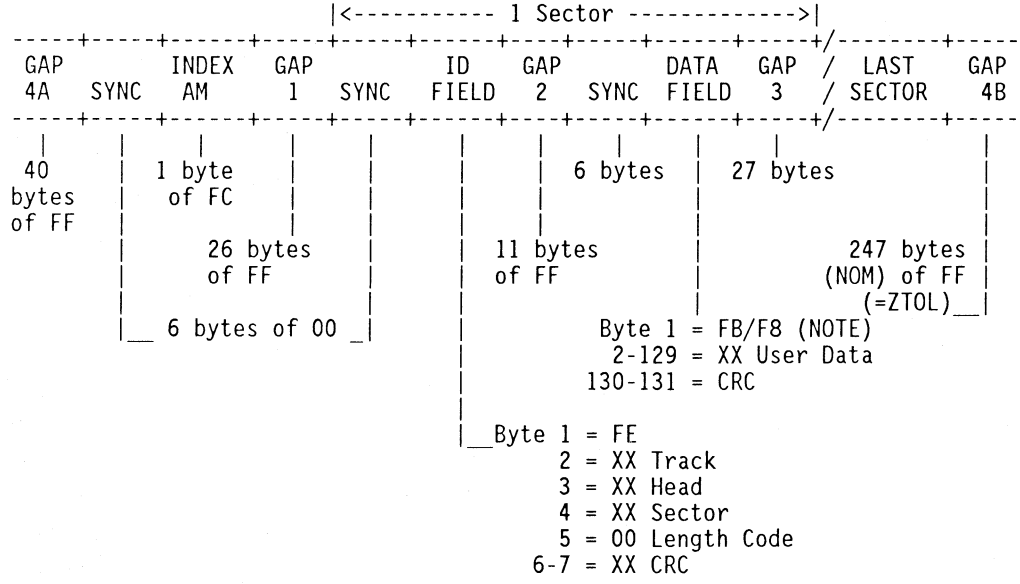
	8-INCH SINGLE-SIDED	8-INCH DOUBLE-SIDED	5-1/4 INCH SINGLE-SIDED	5-1/4 INCH DOUBLE-SIDED	5-1/4 INCH DOUBLE-SIDED 96TPI	5-1/4 INCH DUAL SPEED Vdos	5-1/4 INCH DUAL SPEED PC/AT
	IBM	IBM	Formatted the same as 8-inch			IBM	
TRACKS/DISK	77	154	40	80	160	160	
DATA RATE (BITS/SEC)	250K/500K		125/250K			250K/500K	500K
RECORDING METHOD	FM/MFM					FM/MFM	MFM
ERROR DETECT CORRECT METHOD	16-bit CRC						
BASIC FORMAT: (BYTES/SECTOR)							
UNBUFFERED	128 to 8192					128/256	512
TYPICAL SECTORS/TRACK	26	26	16	16		26	
TRACKS/CYLINDER	1	2	1	2		2	
USER DATA BYTES/DISKETTE	246.272K (SS) 480K (DD)	985.088K (DS, DD)	250.25K (SS)	480K (DS)		1061K (DS, DD, HS)	1228K (DS, DD, HS)

NOTE: SS = single-sided, DS = double-sided, DD = double-density, HS = high speed

The recording formats for floppy disks are similar to those for hard disks. The MVME320B supports both FM and MFM formats for single-density and double-density floppies, respectively.

A.3.1 3740 IBM Format

This format uses FM single-density encoding on all tracks. The track format is illustrated in Figure A-2.



NOTE: Deleted data address mark byte:

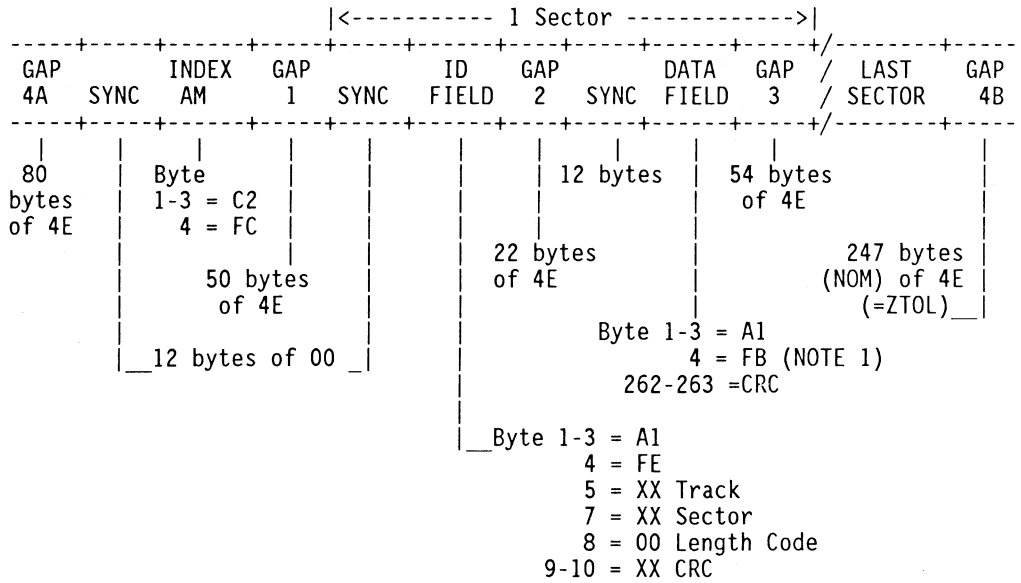
FB = data field contains normal data
F8 = data field contains deleted data

FIGURE A-2. IBM FM Track Format (128 Bytes/Sector)

A.3.2 System 34 IBM Format

This format uses MFM double-density encoding on all tracks except track 0, head 0, which uses the 3740 format described above. The track format is illustrated in Figure A-3.

The MVME320B can support both FM and MFM on track 0.



NOTES: (1) Deleted data address mark:

FB = data field contains normal data
F8 = data field contains deleted data

2. TRACK 0, HEAD 0 uses the format shown in Figure A-2.

FIGURE A-3. IBM MFM Track Format (256 Bytes/Sector)

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APPENDIX B - ECA BLOCK TABLES

Figures B-1 through B-6 are sample ECA block formats for various hard and floppy disks.

	15 EVEN	ODD 0	
$00	COMMAND CODE	MAIN STATUS	
$02	EXTENDED STATUS	0000	
$04	MAXIMUM # OF RE-TRIES 0A	00 ACTUAL # OF RE-TRIES	
$06	DMA TYPE 00	00 COMMAND OPTIONS	
$08	BUFFER ADDRESS MOST SIGNIFICANT WORD	000C	
$0A	BUFFER ADDRESS LEAST SIGNIFICANT WORD	2000	
$0C	BUFFER LENGTH REQUESTED		
$0E	ACTUAL NUMBER OF BYTES TRANSFERRED	0000	
$10	CYLINDER NUMBER		(NOTE 1)
$12	HEAD OR SURFACE NUMBER 00	01 SECTOR NUMBER	(NOTE 1)
$14	CURRENT CYLINDER POSITION	0000	
$16-$1F	RESERVED (10 BYTES)	0000	
$20	N0 -- PRE-INDEX GAP 00	00 N1 -- POST-INDEX GAP	(NOTE 2)
$22	N2 -- SYNC BYTE COUNT 00	00 N3 -- POST-ID GAP	(NOTE 2)
$24	N4 -- POST-DATA GAP 1B	01 N5 -- ADDR MARK CNT	(NOTE 2)
$26	SECTOR LENGTH CODE 00	E5 FILL BYTE	(NOTE 2)

FIGURE B-1. Sample ECA Block Format -- Shugart 450
5-1/4 Inch Single-Density Floppy Disk
IBM 3740 Format, 128 Bytes/Sector

	15 EVEN		ODD 0	
$28-$2D	RESERVED (6 BYTES)		0000	
$2E	DRIVE TYPE	04 | 02	NUMBER OF SURFACES	
$30	# OF SECTORS/TRACK	10 | 0C	STEPPING RATE	
$32	HEAD SETTLING TIME	46 | 46	HEAD LOAD TIME	
$34	SEEK TYPE	00 | 00	RESERVED FOR CONTROLLER	
$36	LOW WRITE CURRENT BOUNDARY CYLINDER		0028	
$38	PRECOMPENSATION BOUNDARY CYLINDER		0028	
$3A-$3F	ECC REMAINDER (6 BYTES)		0000	(NOTE 3)
$40-$45	APPENDED ECC REMAINDER FROM DISK (6 BYTES)		0000	(NOTE 3)
$46-$49	RESERVED (4 BYTES)		0000	
$4A-$55	MVME320B WORKING AREA (12 BYTES)		0000	
$56	RESERVED FOR THE CONTROLLER			

NOTES: (1) Physical starting sector number.

(2) Track format fields (refer to Chapter 8).

(3) Last word (don't care).

4. This is an example, assuming the system memory address has been selected as 000C0000...000FFFFF for a 256K memory module.

5. All numbers are hexadecimal initial ECA values.

FIGURE B-1. Sample ECA Block Format -- Shugart 450
5-1/4 Inch Single-Density Floppy Disk
IBM 3740 Format, 128 Bytes/Sector (cont'd)

	15 EVEN	ODD 0	
$00	COMMAND CODE	MAIN STATUS	
$02	EXTENDED STATUS	0000	
$04	MAXIMUM # OF RE-TRIES 0A	00 ACTUAL # OF RE-TRIES	
$06	DMA TYPE 00	00 COMMAND OPTIONS	
$08	BUFFER ADDRESS MOST SIGNIFICANT WORD	000C	
$0A	BUFFER ADDRESS LEAST SIGNIFICANT WORD	2000	
$0C	BUFFER LENGTH REQUESTED		
$0E	ACTUAL NUMBER OF BYTES TRANSFERRED	0000	
$10	CYLINDER NUMBER		(NOTE 1)
$12	HEAD OR SURFACE NUMBER 00	01 SECTOR NUMBER	(NOTE 1)
$14	CURRENT CYLINDER POSITION	0000	
$16-$1F	RESERVED (10 BYTES)	0000	
$20	N0 -- PRE-INDEX GAP 00	00 N1 -- POST-INDEX GAP	(NOTE 2)
$22	N2 -- SYNC BYTE COUNT 00	00 N3 -- POST-ID GAP	(NOTE 2)
$24	N4 -- POST-DATA GAP 36	03 N5 -- ADDR MARK CNT	(NOTE 2)
$26	SECTOR LENGTH CODE 01	E5 FILL BYTE	(NOTE 2)

FIGURE B-2. Sample ECA Block Format -- Shugart 450
5-1/4 Inch Double-Density Floppy Disk
IBM 34 Format, 256 Bytes/Sector

	15 EVEN		ODD 0		
$28-2D	RESERVED (6 BYTES)			0000	
$2E	DRIVE TYPE	05	02	NUMBER OF SURFACES	
$30	# OF SECTORS/TRACK	10	0C	STEPPING RATE	
$32	HEAD SETTLING TIME	46	46	HEAD LOAD TIME	
$34	SEEK TYPE	00	00	RESERVED FOR CONTROLLER	
$36	LOW WRITE CURRENT BOUNDARY CYLINDER			0028	
$38	PRECOMPENSATION BOUNDARY CYLINDER			0028	
$3A-$3F	ECC REMAINDER (6 BYTES)			0000	(NOTE 3)
$40-$46	APPENDED ECC REMAINDER FROM DISK (6 BYTES)			0000	(NOTE 3)
$46-$49	RESERVED (4 BYTES)			0000	
$4A-$55	MVME320B WORKING AREA (12 BYTES)			0000	
$56	RESERVED FOR THE CONTROLLER				

NOTES: (1) Physical starting sector number.

(2) Track format fields (refer to Chapter 8).

(3) Last word (don't care).

4. This is an example, assuming the system memory address has been selected as 000C0000...000FFFFF for a 256K memory module.

5. All numbers are hexadecimal initial ECA values.

FIGURE B-2. Sample ECA Block Format -- Shugart 450
5-1/4 Inch Double-Density Floppy Disk
IBM 34 Format, 256 Bytes/Sector (cont'd)

	15 EVEN		ODD 0	
$00	COMMAND CODE		MAIN STATUS	
$02	EXTENDED STATUS			0000
$04	MAXIMUM # OF RE-TRIES	0A	00 ACTUAL # OF RE-TRIES	
$06	DMA TYPE	00	00 COMMAND OPTIONS	
$08	BUFFER ADDRESS MOST SIGNIFICANT WORD			000C
$0A	BUFFER ADDRESS LEAST SIGNIFICANT WORD			2000
$0C	BUFFER LENGTH REQUESTED			
$0E	ACTUAL NUMBER OF BYTES TRANSFERRED			0000
$10	CYLINDER NUMBER			(NOTE 1)
$12	HEAD OR SURFACE NUMBER	00	01 SECTOR NUMBER	(NOTE 1)
$14	CURRENT CYLINDER POSITION			0000
$16-$1F	RESERVED (10 BYTES)			0000
$20	N0 -- PRE-INDEX GAP	00	00 N1 -- POST-INDEX GAP	(NOTE 2)
$22	N2 -- SYNC BYTE COUNT	00	00 N3 -- POST-ID GAP	(NOTE 2)
$24	N4 -- POST-DATA GAP	1B	01 N5 -- ADDR MARK CNT	(NOTE 2)
$26	SECTOR LENGTH CODE	00	E5 FILL BYTE	(NOTE 2)

FIGURE B-3. Sample ECA Block Format -- Shugart 860
8-Inch Single-Density Floppy Disk
IBM 3740 Format, 128 Bytes/Sector

B

	15 EVEN		ODD 0		
$28-$2D	RESERVED (6 BYTES)			0000	
$2E	DRIVE TYPE	00	02	NUMBER OF SURFACES	
$30	# OF SECTORS/TRACK	1A	06	STEPPING RATE	
$32	HEAD SETTLING TIME	46	46	HEAD LOAD TIME	
$34	SEEK TYPE	00	00	RESERVED FOR CONTROLLER	
$36	LOW WRITE CURRENT BOUNDARY CYLINDER			0028	
$38	PRECOMPENSATION BOUNDARY CYLINDER			0028	
$3A-$3F	ECC REMAINDER (6 BYTES)			0000	(NOTE 3)
$40-$45	APPENDED ECC REMAINDER FROM DISK (6 BYTES)			0000	(NOTE 3)
$46-$49	RESERVED (4 BYTES)			0000	
$4A-$55	MVME320B WORKING AREA (12 BYTES)			0000	
$56	RESERVED FOR THE CONTROLLER				

NOTES: (1) Physical starting sector number.

(2) Track format fields (refer to Chapter 8).

(3) Last word (don't care).

4. This is an example, assuming the system memory address has been selected as 000C0000...000FFFFF for a 256K memory module.

5. All numbers are hexadecimal initial ECA values.

FIGURE B-3. Sample ECA Block Format -- Shugart 860
8-Inch Single-Density Floppy Disk
IBM 3740 Format, 128 Bytes/Sector (cont'd)

	15 EVEN		ODD 0	
$00	COMMAND CODE		MAIN STATUS	
$02	EXTENDED STATUS			0000
$04	MAXIMUM # OF RE-TRIES	0A	00 ACTUAL # OF RE-TRIES	
$06	DMA TYPE	00	CO COMMAND OPTIONS	
$08	BUFFER ADDRESS MOST SIGNIFICANT WORD			000C
$0A	BUFFER ADDRESS LEAST SIGNIFICANT WORD			2000
$0C	BUFFER LENGTH REQUESTED			
$0E	ACTUAL NUMBER OF BYTES TRANSFERRED			0000
$10	CYLINDER NUMBER			(NOTE 1)
$12	HEAD OR SURFACE NUMBER	00	01 SECTOR NUMBER	(NOTE 1)
$14	CURRENT CYLINDER POSITION			0000
$16-$1F	RESERVED (10 BYTES)			0000
$20	N0 -- PRE-INDEX GAP	00	00 N1 -- POST-INDEX GAP	(NOTE 2)
$22	N2 -- SYNC BYTE COUNT	00	00 N3 -- POST-ID GAP	(NOTE 2)
$24	N4 -- POST-DATA GAP	36	03 N5 -- ADDR MARK CNT	(NOTE 2)
$26	SECTOR LENGTH CODE	01	E5 FILL BYTE	(NOTE 2)

FIGURE B-4. Sample ECA Block Format -- Shugart 860
8-Inch Double-Density Floppy Disk
IBM 34 Format, 256 Bytes/Sector

B

	15 EVEN		ODD 0		
$28-$2D	RESERVED (6 BYTES)			0000	
$2E	DRIVE TYPE	01	02	NUMBER OF SURFACES	
$30	# OF SECTORS/TRACK	1A	06	STEPPING RATE	
$32	HEAD SETTLING TIME	46	46	HEAD LOAD TIME	
$34	SEEK TYPE	00	00	RESERVED FOR CONTROLLER	
$36	LOW WRITE CURRENT BOUNDARY CYLINDER			0028	
$38	PRECOMPENSATION BOUNDARY CYLINDER			0028	
$3A-$3F	ECC REMAINDER (6 BYTES)			0000	(NOTE 3)
$40-$45	APPENDED ECC REMAINDER FROM DISK (6 BYTES)			0000	(NOTE 3)
$46-$49	RESERVED (4 BYTES)			0000	
$4A-$55	MVME320B WORKING AREA (12 BYTES)			0000	
$56	RESERVED FOR THE CONTROLLER				

NOTES: (1) Physical starting sector number.

(2) Track format fields (refer to Chapter 8).

(3) Last word (don't care).

4. This is an example, assuming the system memory address has been selected as 000C0000...000FFFFF for a 256K memory module.

5. All numbers are hexadecimal initial ECA values.

FIGURE B-4. Sample ECA Block Format -- Shugart 860
8-Inch Double-Density Floppy Disk
IBM 34 Format, 256 Bytes/Sector (cont'd)

	15 EVEN	ODD 0	
$00	COMMAND CODE	MAIN STATUS	
$02	EXTENDED STATUS 0000		
$04	MAXIMUM # OF RE-TRIES 0A	00 ACTUAL # OF RE-TRIES	
$06	DMA TYPE 00	00 COMMAND OPTIONS	
$08	BUFFER ADDRESS MOST SIGNIFICANT WORD 000C		
$0A	BUFFER ADDRESS LEAST SIGNIFICANT WORD 2000		
$0C	BUFFER LENGTH REQUESTED		
$0E	ACTUAL NUMBER OF BYTES TRANSFERRED 0000		
$10	CYLINDER NUMBER		(NOTE 1)
$12	HEAD OR SURFACE NUMBER 00	01 SECTOR NUMBER	(NOTE 1)
$14	CURRENT CYLINDER POSITION 0000		
$16-$1F	RESERVED (10 BYTES) 0000		
$20	N0 -- PRE-INDEX GAP 00	00 N1 -- POST-INDEX GAP	(NOTE 2)
$22	N2 -- SYNC BYTE COUNT 00	00 N3 -- POST-ID GAP	(NOTE 2)
$24	N4 -- POST-DATA GAP 0F	01 N5 -- ADDR MARK CNT	(NOTE 2)
$26	SECTOR LENGTH CODE 01	E5 FILL BYTE	(NOTE 2)

FIGURE B-5. Sample ECA Block Format -- ST412
5-1/4 Inch Hard Disk (10 MHz, 15Mb)

	15 EVEN		ODD 0	
$28-$2D	RESERVED (6 BYTES)		0000	
$2E	DRIVE TYPE	03 | 06	NUMBER OF SURFACES	
$30	# OF SECTORS/TRACK	20 | 00	STEPPING RATE	
$32	HEAD SETTLING TIME	00 | 00	HEAD LOAD TIME	
$34	SEEK TYPE	02 | 00	RESERVED FOR CONTROLLER	
$36	LOW WRITE CURRENT BOUNDARY CYLINDER		0050	
$38	PRECOMPENSATION BOUNDARY CYLINDER		0050	
$3A-$3F	ECC REMAINDER (6 BYTES)		0000	(NOTE 3)
$40-$45	APPENDED ECC REMAINDER FROM DISK (6 BYTES)		0000	(NOTE 3)
$46-$49	RESERVED (4 BYTES)		0000	
$4A-$55	MVME320B WORKING AREA (12 BYTES)		0000	
$56	RESERVED FOR THE CONTROLLER			

NOTES: (1) Physical starting sector number.

(2) Track format fields (refer to Chapter 8).

(3) Last word (don't care).

4. This is an example, assuming the system memory address has been selected as 000C0000...000FFFFF for a 256K memory module.

5. All numbers are hexadecimal initial ECA values.

FIGURE B-5. Sample ECA Block Format -- ST412 5-1/4 Inch Hard Disk (10 MHz, 15Mb) (cont'd)

APPENDIX C - PROGRAMMING CONCEPTS AND SEQUENCE

C.1 INTRODUCTION

Appendix C provides programming concepts and sequence and a command execution procedure for the MVME320B.

C.2 PROGRAMMING CONCEPTS

In the VMEbus I/O space, the MVME320B is assigned a base address of the form:

ZZZR

where:

ZZZ = address bits A4 - A9 (don't care)
and A10 - A15 (from J6)

R = any register number (odd numbers from 1 - D)

For example:

3C01 = register 1 at address 3C01

```
  15   12  11     8  7     4   3     0
 ---------------------------------------
  0 0 1 1   1 X X X  X X X X   R R R R
 ---------------------------------------

 \_from J6_/
```

where:

X = don't care
R = register number (binary expression of R above)
J6 = jumper network J6 (at location H1)

C.3 PROGRAMMING SEQUENCE

Any time after system power-up or system reset, and before executing a command for the first time, the host must:

- Initialize the ECA
- Set the ECA pointer (Registers 1, 3, 5, 7)
- Set the interrupt acknowledge status/ID byte (Register 9)
- Set the interrupt acknowledge address in the trap area (if appropriate to the host, as described below)

a. Initialize the ECA - To create the ECA in main memory, the host must initialize the following portions of the ECA. See Figure 5-1.

- Command code
- Maximum number of re-tries
- Command options
- DMA type
- Buffer address most significant word
- Buffer length requested
- Cylinder number
- Sector number
- Head or surface number
- Post-data gap
- Fill byte
- Sector length
- Number of surfaces
- Drive type
- Stepping rate
- Number of sectors per track
- Head load time
- Head settling time
- Seek type
- Low write current boundary track
- Precompensation boundary track

The following portions of the ECA may be changed by the MVME320B.

- Main status - the MVME320B sets main status to busy in its own memory. The host doesn't need to initialize main status. However, if the host wants main status to be meaningful during command execution, the host must set main status to busy before starting to execute a command.
- Extended status
- Actual number of bytes transferred
- Current cylinder position
- ECC remainder
- Append ECC remainder from disk
- All reserved areas

b. Set the ECA Pointer (Registers 1, 3, 5, and 7) - This tells the MVME320B where the ECA was created in main memory.

c. Set the Interrupt Acknowledge Status/ID Bit (Register 9) - When the MVME320B wants to interrupt, it activates the interrupt line. The host acknowledges the interrupt request, and the MVME320B returns the status/ID byte from register 9.

d. Set the Interrupt Acknowledge Address in the Trap Area - If the host system is an MC68000-based system and if the system is interpreting the interrupt acknowledge status/ID bits as an interrupt vector number, the interrupt acknowledge address in the trap area must be initialized.

C.4 COMMAND EXECUTION

The following sequence is required each time a command is executed.

a. Check the busy bit in register D. Wait for 0.

b. Set main status in ECA to busy.

c. Fill in and set up ECA.

d. Set busy bit in register D.

e. Wait for main status in ECA to change (polling mode)
or
Wait for interrupt and wait for main status in ECA to change. Check register B for interrupting unit (interrupt mode).

f. If main status ≠ 0, then handle errors.

If extended status ≠ 0, then handle errors.

If read or write command, and the number of bytes transferred does not equal number of bytes requested, then handle errors.

If read command, and ECC remainder ≠ 0, then handle errors.

g. Clear busy bit in register D.

C

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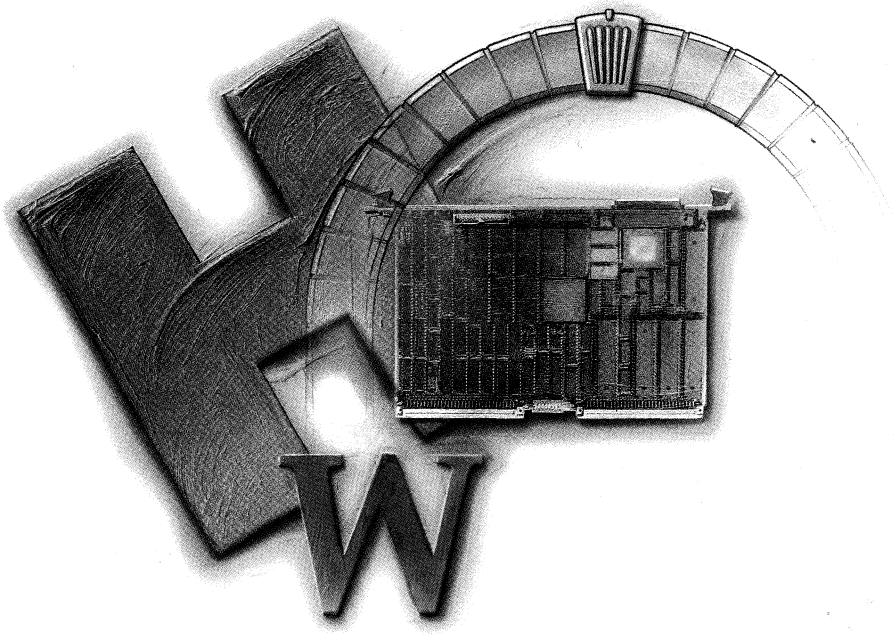
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