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MVME340/D1

MVME340
Parallel Interface/Timer Module
User's Manual

M V M E 3 4 0

P A R A L L E L I N T E R F A C E / T I M E R M O D U L E

U S E R ' S M A N U A L

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TABLE OF CONTENTS

		Page
Chapter 1	GENERAL INFORMATION	
1.1	INTRODUCTION	1-2
1.2	SPECIFICATIONS	1-2
1.3	REFERENCE MANUALS	1-2
1.4	MANUAL TERMINOLOGY	1-4
1.4.1	Address and Data Formats	1-4
1.4.2	Electrical Signal Levels	1-4
1.4.3	Logic Signal States	1-4
Chapter 2	FUNCTIONAL DESCRIPTION	
2.1	INTRODUCTION	2-1
2.2	HARDWARE OVERVIEW	2-1
2.3	VMEBUS INTERFACE	2-3
2.3.1	VMEbus Signals	2-3
2.3.2	Timing Specifications	2-8
2.4	ADDRESS DECODER	2-12
2.5	PERIPHERAL INTERFACE AND TIMER CIRCUITS	2-13
2.6	PERIPHERAL SIGNALS	2-15
2.7	INTERRUPTERS	2-19
2.8	MODULE CONTROL REGISTER	2-21
2.9	MODULE RESET	2-21
2.10	MODULE CLOCK	2-21
Chapter 3	INSTALLATION INSTRUCTIONS	
3.1	INTRODUCTION	3-1
3.2	UNPACKING INSTRUCTIONS	3-1
3.3	INSPECTION	3-1
3.4	MODULE PREPARATION	3-1
3.4.1	Base Address Selection	3-3
3.4.2	Address Modifier Decoder	3-4
3.4.3	Local Clock Option	3-6
3.4.4	Handshake Line Configuration	3-7
3.4.5	Peripheral Line Termination	3-8
3.4.6	Peripheral Line Connection	3-9
3.5	MODULE INSTALLATION	3-11
Chapter 4	OPERATING INSTRUCTIONS	
4.1	INTRODUCTION	4-1
4.2	ADDRESS MAP	4-1
4.3	PARALLEL INTERFACE CONFIGURATION	4-3
4.3.1	Single Bit Input/Output	4-4
4.3.2	8-Bit Input/Output	4-5
4.3.3	Port-Concatenated 16-Bit Input/Output	4-6
4.3.4	Device-Parallel 16-Bit Input/Output	4-7
4.3.5	32-Bit Input/Output	4-8
4.4	TIMER AND PORT C CONFIGURATION	4-9

TABLE OF CONTENTS

		Page
4.5	REGISTER DESCRIPTIONS	4-9
4.5.1	Port General Control Registers (PGCR)	4-10
4.5.2	Port Service Request Registers (PSRR)	4-11
4.5.3	Port A Data Direction Registers (PADDR)	4-12
4.5.4	Port B Data Direction Registers (PBDDR)	4-13
4.5.5	Port C Data Direction Registers (PCDDR)	4-14
4.5.6	Port Interrupt Status/ID Byte Registers (PISBR)	4-15
4.5.7	Port A Control Registers (PACR)	4-16
4.5.8	Port B Control Registers (PBCR)	4-20
4.5.9	Port A Data Registers (PADR)	4-24
4.5.10	Port B Data Registers (PBDR)	4-24
4.5.11	Port A Alternate Registers (PAAR)	4-25
4.5.12	Port B Alternate Registers (PBAR)	4-25
4.5.13	Port C Data Registers (PCDR)	4-26
4.5.14	Port Status Registers (PSR)	4-27
4.5.15	Timer Control Register (TCR)	4-28
4.5.16	Timer Interrupt Status/ID Byte Registers (TISBR)	4-30
4.5.17	Counter Preload Registers High, Mid, Low (CPRH-CPRL)	4-31
4.5.18	Count Registers High, Mid, Low (CNTRH-CNTRL)	4-32
4.5.19	Timer Status Registers (TSR)	4-33
4.5.20	Interrupt Level Registers (ILR)	4-34
4.5.21	Module Control Register (MCR)	4-35
4.5.22	PI/T 1/2 Peripheral Line Direction Register (PLDR12)	4-36
4.5.23	PI/T 3 Peripheral Line Direction Register (PLDR3)	4-37
4.5.24	Driver Characteristic Control Register (DCCR)	4-38
4.6	PROGRAMMING CONSIDERATIONS	4-39
4.6.1	Initialization Procedure	4-39
4.6.2	Issue Command Procedure	4-39
4.6.3	Interrupt Service Routine	4-40
4.6.4	Termination Procedure	4-40

Chapter 5 MAINTENANCE INFORMATION

5.1	INTRODUCTION	5-1
5.2	PARTS LIST	5-1
5.3	ASSEMBLY DRAWING, SCHEMATIC DIAGRAMS	5-2

APPENDICES

APPENDIX A:	MC68230 Parallel Interface/Timer Data Sheet	A-1
APPENDIX B:	MC3448A Transceiver Data Sheet	B-1
APPENDIX C:	MVME340 Register Equate File	C-1

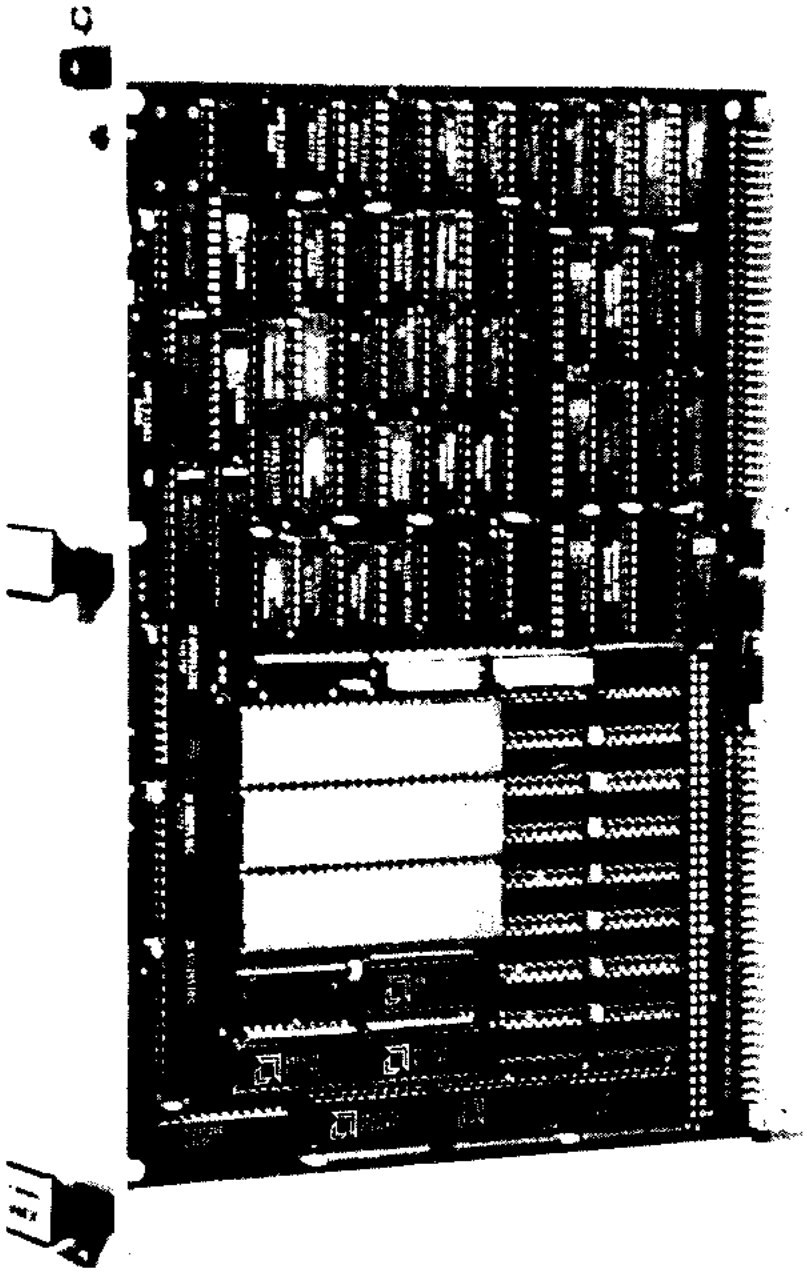
LIST OF TABLES

		Page
Table 1.1:	MVME340 Specifications	1-3
Table 2.1:	VMEbus Signal Description	2-4
Table 2.2:	Connector P1 VMEbus Signal Locations	2-6
Table 2.3:	Connector P2 VMEbus Signal Locations	2-7
Table 2.4:	Read Cycle Timing PI/T Registers	2-9
Table 2.5:	Read Cycle Timing Module Registers	2-9
Table 2.6:	Write Cycle Timing PI/T Registers	2-10
Table 2.7:	Write Cycle Timing Module Registers	2-10
Table 2.8:	Interrupt Acknowledge Cycle Timing	2-11
Table 2.9:	Address Decoder Options	2-12
Table 2.10:	Peripheral Signal Description	2-15
Table 2.11:	Connector P2 Peripheral Signal Locations	2-18
Table 3.1:	Base Address Configuration K1, K2, K3 and K4	3-3
Table 3.2:	Address Modifier Decoder PROM Specification	3-5
Table 3.3:	Handshake Line Configuration K5	3-7
Table 3.4:	Resistor Network/Port Signal Locations	3-8
Table 3.5:	Interface Connector Signal Locations	3-10
Table 4.1:	MVME340 Address Map	4-2
Table 5.1:	MVME340 Parts List	5-1

LIST OF FIGURES

Figure 1.1:	The MVME340 Parallel Interface/Timer Module	1-1
Figure 2.1:	MVME340 Block Diagram	2-2
Figure 2.2:	Read Cycle	2-9
Figure 2.3:	Write Cycle	2-10
Figure 2.4:	Interrupt Acknowledge Cycle	2-11
Figure 2.5:	Peripheral Interface Block Diagram	2-14
Figure 2.6:	Interrupter Block Diagram	2-20
Figure 3.1:	MVME340 Jumper Area Locations	3-2
Figure 3.2:	Jumper Area K1	3-3
Figure 3.3:	Jumper Areas K2, K3 and K4	3-3
Figure 3.4:	Address Modifier Decoder PROM	3-4
Figure 3.5:	Jumper Area K6 and IC socket Y1	3-6
Figure 3.6:	Jumper Area K5	3-7
Figure 3.7:	Termination Resistor Networks RP1-RP8	3-8
Figure 3.8:	Peripheral Connection Through Connector Assembly	3-9
Figure 5.1:	MVME340 Assembly Drawing	5-3
Figure 5.2:	MVME340 Schematic Diagram Sheet 1/11	5-4
Figure 5.3:	MVME340 Schematic Diagram Sheet 2/11	5-5
Figure 5.4:	MVME340 Schematic Diagram Sheet 3/11	5-6
Figure 5.5:	MVME340 Schematic Diagram Sheet 4/11	5-7
Figure 5.6:	MVME340 Schematic Diagram Sheet 5/11	5-8
Figure 5.7:	MVME340 Schematic Diagram Sheet 6/11	5-9
Figure 5.8:	MVME340 Schematic Diagram Sheet 7/11	5-10
Figure 5.9:	MVME340 Schematic Diagram Sheet 8/11	5-11
Figure 5.10:	MVME340 Schematic Diagram Sheet 9/11	5-12
Figure 5.11:	MVME340 Schematic Diagram Sheet 10/11	5-13
Figure 5.12:	MVME340 Schematic Diagram Sheet 11/11	5-14

Figure 1.1: The MVME340 Parallel Interface/Timer Module



CHAPTER 1

GENERAL INFORMATION

1.1 INTRODUCTION

The MVME340 Parallel Interface/Timer Module is a general purpose input/output interface module for interfacing a controlling VME system to peripheral hardware, e.g. industrial control or data acquisition equipment. The MVME340 module provides 64 peripheral lines which can be programmed for input, output, handshake and timer functions. The peripheral lines comply with the electrical requirements specified in the IEEE 488-1975 document.

This manual provides general information, functional description, installation instructions, operating instructions and maintenance information for the MVME340 Parallel Interface/Timer Module.

Figure 1.1 shows the MVME340 module.

1.2 SPECIFICATIONS

The specifications of the MVME340 Parallel Interface/Timer module are given in Table 1.1.

1.3 REFERENCE MANUALS

The following manuals may be used for further information concerning the VMEbus and the MC68230 Parallel Interface/Timer.

- MVMEBS VMEbus Specification Manual
- MC68230 Parallel Interface/Timer Data Sheet

Table 1.1: MVME340 Specifications

CHARACTERISTIC	SPECIFICATION
Interface Devices	The MVME340 module contains three MC68230 Parallel Interface/Timer devices.
VMEbus Interface	The VMEbus slave interface is selected by jumpers as any one option of A16:D16, A24:D16 or A32:D16. The address modifier codes are factory-programmed or user-selectable. The interrupt request levels and the status/ID bytes of the three interrupters are software programmable.
Peripheral Interface	The peripheral interface consists of 50 parallel I/O lines, 8 handshake lines and 6 timer I/O lines. The electrical characteristics of the I/O lines comply with the IEEE 488-1975 specification. Locations are provided on the module for user supplied termination resistor networks. All peripheral outputs can be programmed for active pull-up or open-collector characteristics.
Parallel I/O Functions	The parallel interfaces can be configured to operate in unidirectional or bidirectional modes either 8, 16 or 32 bit wide. In the unidirectional modes, port data direction registers determine whether the port lines are inputs or outputs. In the bidirectional modes the data direction is determined dynamically by the peripheral system. The programmable handshake lines are used for controlling and timing the data transfer between the MVME340 and the connected peripheral devices.
Timer Functions	The module contains three programmable 24-bit timers with 5-bit prescalers which may be clocked either by the internal module clock or by an external device. The timers can be used for peripheral timing and counting functions, time measurements, or for generating single or periodic system interrupts.
Indicators	Programmable STATUS LED on the front panel
Mechan. Dimensions	Double height VME board with front panel Board size: 233 mm * 160 mm Front panel size: 262 mm * 20 mm
Power Requirements	+ 5 V DC (+/- 5%), 3.2 A (typ), 4.0 A (max) (supply current without peripheral line load)
Environmental Conditions	Operating temperature: 0 to 55 C Storage temperature: -40 to 100 C Operating humidity: 0 to 90 % non condensing

1.4 MANUAL TERMINOLOGY

1.4.1 Address and Data Formats

Throughout this manual, unless otherwise noted, all address and data values are given in hexadecimal format.

1.4.2 Electrical Signal Levels

A signal line is always assumed to be in one of two levels, or in transition between those levels. Whenever the term "high" is used, it refers to a high TTL voltage level (> +2.0 V). The term "low" refers to a low TTL voltage level (< +0.8 V).

There are two possible transitions which can appear on a signal line, and they will be referred to as "edges". A "rising edge" is defined as the time period during which a signal line makes its transition from a low level to a high level. The "falling edge" is defined as the time period during which a signal line makes its transition from a high level to a low level.

A signal is defined as "active low" if the function associated with the signal line is valid or initiated by either a low level or a falling edge on the signal line. The mnemonics of active low signals are marked with the suffix "*".

A signal is defined as "active high" if the function associated with the signal line is valid or initiated by either a high level or a rising edge on the signal line.

1.4.3 Logic Signal States

The terms "assert" and "negate" describe the logic state of a signal without indicating the associated voltage level. An active low signal is asserted when its voltage level is low, it is negated when its voltage level is high. An active high signal is asserted when its voltage level is high, it is negated when its voltage level is low.

For signals which are driven by three-state or open-collector outputs, the term "release" describes the high impedance state of the corresponding driver. Typically these signal lines are driven to a high voltage level by pull-up resistors when all drivers on the line are turned off.

CHAPTER 2

FUNCTIONAL DESCRIPTION

2.1 INTRODUCTION

For the purposes of the following description, the MVME340 module is regarded as consisting of functional blocks as shown in Figure 2.1.

For details of the hardware, schematic diagrams and an assembly drawing are included in Chapter 5.

2.2 HARWARE OVERVIEW

The MVME340 Parallel Interface/Timer Module consists of: address decoder, VMEbus slave interface, VMEbus interrupters and interrupter control, module control register, three parallel interface/timer devices, peripheral line transceivers and transceiver control, and user supplied optional termination networks for the peripheral lines.

The address decoder supports either the extended, standard, or short addressing range. The appropriate address mode is jumper selectable, and configures the module to respond to the corresponding address modifier codes, and to decode the corresponding number of address lines.

Three MC68230 parallel interface/timer devices are located on the module. Through the VMEbus interface each of the three parallel I/O devices is accessed by byte wide data transfers. Two of the parallel I/O devices may be configured for word wide data transfers. The module control and status registers are accessed byte wide only.

Three VMEbus interrupters are located on the MVME340. The interrupt request levels and status/ID bytes are software programmable. Interrupts may be requested by any of the three timers and by any of the peripheral handshake inputs.

The module control register drives the STATUS LED, and masks the timer interrupt request signals.

The peripheral signals of the parallel interface/timer devices are connected to P2 via the peripheral line transceivers. The parallel interface operates in unidirectional or bidirectional modes. Each timer can be clocked either by the system clock or an external clock. For a more detailed description of the device refer to the MC68230 Parallel Interface/Timer data sheet in Appendix A.

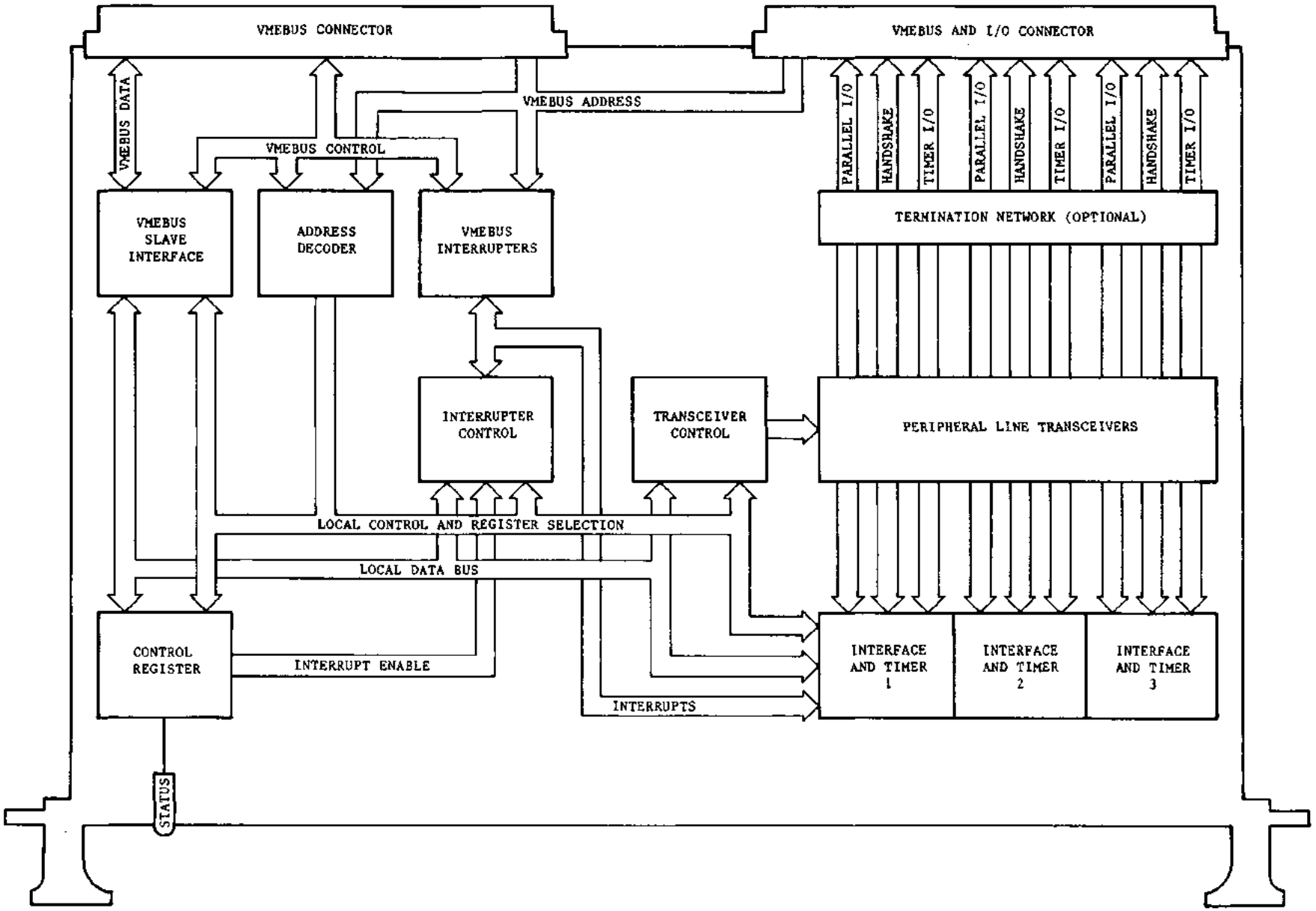


Figure 2.1: MVME340 Block Diagram

The peripheral line transceivers meet the electrical I/O characteristics of the IEEE 488-1975 standard digital interface for programmable instrumentation for driver, receiver, and composite device loads. The transceiver control contains two sets of registers, comprising peripheral line direction registers and a driver characteristic control register. The peripheral line direction registers are accessed directly or parallel to the PI/T port direction registers.

The peripheral line transceiver driver outputs are controlled by the driver characteristic control register and can be defined as active pull-up or open-collector.

All peripheral lines may be terminated by optional termination networks which are application specific and supplied by the user.

2.3 VMEBUS INTERFACE

The VMEbus interface provides the data path between the MVME340 module and the VMEbus backplane. The interface complies with all requirements for the signal driver/receiver characteristics and bus operation protocols, as specified in the VMEbus Specification Rev.B.

The following paragraphs supply detailed specifications of all VMEbus signals and operations supported by the MVME340 module.

2.3.1 VMEbus Signals

Table 2.1 identifies all VMEbus signals by mnemonics and functional descriptions. The locations of the VMEbus signals at the connector P1 and P2 are shown in Table 2.2 and Table 2.3 respectively.

Table 2.1: VMEbus Signal Description

SIGNAL	SIGNAL DESCRIPTION
A01..A31	ADDRESS BUS 31 address input lines that specify a register location.
AM0..AM5	ADDRESS MODIFIERS Six address modifier input signals that provide additional address information.
D00..D15	DATA BUS 16 bidirectional three-state data lines for byte and word transfers.
WRITE*	WRITE An active low input signal that specifies the direction of a data transfer: A high level indicates a read operation, a low level indicates a write operation.
AS*	ADDRESS STROBE An active low input signal that indicates a valid address on the bus.
DS0*	DATA STROBE 0 An active low input signal that indicates a data transfer on the data lines D00..D07.
DS1*	DATA STROBE 1 An active low input signal that indicates a data transfer on the data lines D08...D15.
LWORD*	LONG WORD An active low input signal that indicates a 32-bit data transfer.
DTACK*	DATA TRANSFER ACKNOWLEDGE An active low open-collector output signal that indicates the completion of a data transfer.
IRQ1*..IRQ7*	INTERRUPT REQUEST LEVEL 1-7 7 active low open-collector output signals that generate prioritized interrupt requests.

Table 2.1: VMEbus Signal Description (continued)

SIGNAL	SIGNAL DESCRIPTION
IACK*	INTERRUPT ACKNOWLEDGE An active low input signal that indicates an interrupt status/ID byte fetch on the bus.
IACKIN* IACKOUT*	INTERRUPT ACKNOWLEDGE INPUT INTERRUPT ACKNOWLEDGE OUTPUT These active low signals form an interrupt acknowledge daisy chain through all interrupters in the system. IACKIN* is an input which indicates that the acknowledgement has been propagated from the previous interrupter. IACKOUT* is a totem-pole output that propagates the acknowledgement to the next interrupter.
SYSRESET*	SYSTEM RESET An active low input signal that causes a complete reset of the module.
SYSCLK	SYSTEM CLOCK A 16 MHz input signal that supplies the clock for the module.
GND	GROUND
+5V	+ 5 VOLTS POWER
BERR* BR0*..BR3* BG0IN*...BG3IN* BG0OUT*..BG3OUT* BBSY* BCLR* ACFAIL* SYSFAIL* SERCLK SERDAT +5VSTB +12V -12V	BUS ERROR BUS REQUEST LEVEL 0-3 BUS GRANT INPUTS LEVEL 0-3 BUS GRANT OUTPUTS LEVEL 0-3 BUS BUSY BUS CLEAR AC POWER FAILURE SYSTEM FAILURE VMSBUS CLOCK VMSBUS DATA + 5 VOLTS STAND BY POWER + 12 VOLTS POWER - 12 VOLTS POWER These signals are not connected with the module.

Table 2.2: Connector P1 VMEbus Signal Locations

PIN NO.	ROW A SIGNALS	ROW B SIGNALS	ROW C SIGNALS	PIN NO.
1	D00	(BBSY*)	D08	1
2	D01	(BCLR*)	D09	2
3	D02	(ACFAIL*)	D10	3
4	D03	(BG0IN*)	D11	4
5	D04	(BG0OUT*)	D12	5
6	D05	(BG1IN*)	D13	6
7	D06	(BG1OUT*)	D14	7
8	D07	(BG2IN*)	D15	8
9	GND	(BG2OUT*)	GND	9
10	SYSCLK	(BG3IN*)	(SYSFAIL*)	10
11	GND	(BG3OUT*)	(BERR*)	11
12	DS1*	(BR0*)	SYSRESET*	12
13	DS0*	(BR1*)	LWORD*	13
14	WRITE*	(BR2*)	AM5	14
15	GND	(BR3*)	A23	15
16	DTACK*	AM0	A22	16
17	GND	AM1	A21	17
18	AS*	AM2	A20	18
19	GND	AM3	A19	19
20	IACK*	GND	A18	20
21	IACKIN*	(SERCLK)	A17	21
22	IACKOUT*	(SERDAT)	A16	22
23	AM4	GND	A15	23
24	A07	IRQ7*	A14	24
25	A06	IRQ6*	A13	25
26	A05	IRQ5*	A12	26
27	A04	IRQ4*	A11	27
28	A03	IRQ3*	A10	28
29	A02	IRQ2*	A09	29
30	A01	IRQ1*	A08	30
31	(-12V)	(5V STBY)	(+12V)	31
32	+5V	+5V	+5V	32

Note: Signals in parentheses are not used by the MVME340

Table 2.3: Connector P2 VMEbus Signal Locations

PIN NO.	ROW A SIGNALS	ROW B SIGNALS	ROW C SIGNALS	PIN NO.
1	I/O	+5V	I/O	1
2	I/O	GND	I/O	2
3	I/O	(RESERVE)	I/O	3
4	I/O	A24	I/O	4
5	I/O	A25	I/O	5
6	I/O	A26	I/O	6
7	I/O	A27	I/O	7
8	I/O	A28	I/O	8
9	I/O	A29	I/O	9
10	I/O	A30	I/O	10
11	I/O	A31	I/O	11
12	I/O	GND	I/O	12
13	I/O	+5V	I/O	13
14	I/O	(D16)	I/O	14
15	I/O	(D17)	I/O	15
16	I/O	(D18)	I/O	16
17	I/O	(D19)	I/O	17
18	I/O	(D20)	I/O	18
19	I/O	(D21)	I/O	19
20	I/O	(D22)	I/O	20
21	I/O	(D23)	I/O	21
22	I/O	GND	I/O	22
23	I/O	(D24)	I/O	23
24	I/O	(D25)	I/O	24
25	I/O	(D26)	I/O	25
26	I/O	(D27)	I/O	26
27	I/O	(D28)	I/O	27
28	I/O	(D29)	I/O	28
29	I/O	(D30)	I/O	29
30	I/O	(D31)	I/O	30
31	I/O	GND	I/O	31
32	I/O	+5V	I/O	32

Note: Signals in parentheses are not used by the MVME340

2.3.2 Timing Specifications

This paragraph provides detailed VMEbus timing specifications of the MVME340 Parallel Interface/Timer modules for read, write, and interrupt acknowledge operations.

The tables specify the timings supplied by the MVME340 modules interacting with other modules on the VMEbus. No timing requirements for these modules are given as it is assumed that they comply with the requirements of the VMEbus Specification Rev.B.

If a user supplied module clock oscillator is used the timings will differ. The VMEbus timings will however, remain within the valid range of the VMEbus specifications.

Separate tables are given for the PI/T internal registers, and the module registers external to the PI/Ts. The timings given are valid if the VMEbus SYSCLK line is used as the module clock signal. The tabulated maximum and minimum times are guaranteed over the recommended operating conditions, as specified in Table 1.1.

Figure 2.2: Read Cycle

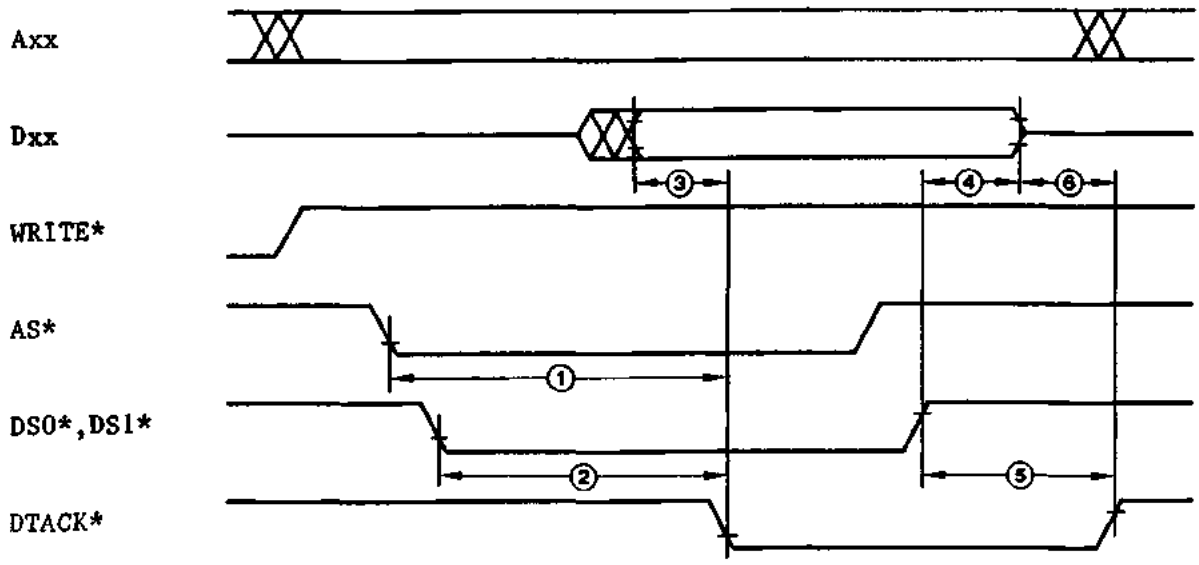


Table 2.4: Read Cycle Timing PI/T Registers

NO.	PARAMETER	NOTES	MIN	MAX	UNIT
1	AS* low to DTACK* low	1		500	ns
2	DS0*/DS1* low to DTACK* low	2		460	ns
3	Data valid to DTACK* low		10		ns
4	DS0*/DS1* high to Data invalid		30		ns
5	DS0*/DS1* high to DTACK* high			190	ns
6	Data high imp. to DTACK* high		60		ns

Note 1: Provided that the VMEbus master drives DS0*/DS1* low less than 40 ns after driving AS* low.

Note 2: Provided that the VMEbus master drives DS0*/DS1* low more than 40 ns after driving AS* low.

Table 2.5: Read Cycle Timing Module Registers

NO.	PARAMETER	NOTES	MIN	MAX	UNIT
1	AS* low to DTACK* low	1		240	ns
2	DS0* low to DTACK* low	2		175	ns
3	Data valid to DTACK* low		10		ns
4	DS0* high to Data invalid		30		ns
5	DS0* high to DTACK* high			175	ns
6	Data high imp. to DTACK* high		75		ns

Note 1: Provided that the VMEbus master drives DS0* low less than 65 ns after driving AS* low.

Note 2: Provided that the VMEbus master drives DS0* low more than 65 ns after driving AS* low.

Figure 2.3: Write Cycle

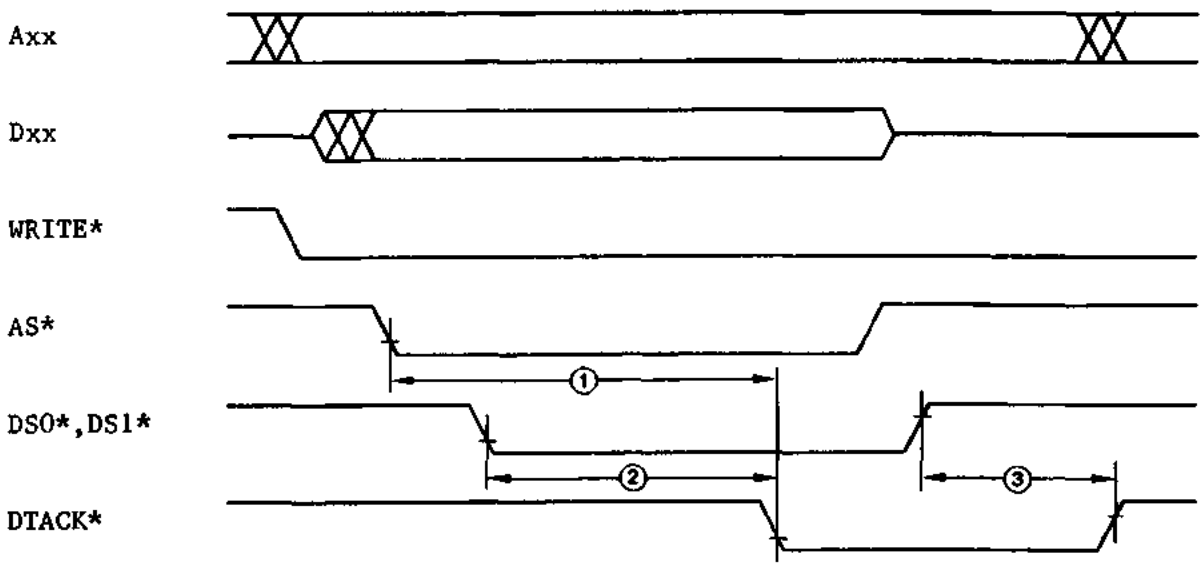


Table 2.6: Write Cycle Timing PI/T Registers

NO.	PARAMETER	NOTES	MIN	MAX	UNIT
1	AS* low to DTACK* low	1		500	ns
2	DS0*/DS1* low to DTACK* low	2		460	ns
3	DS0*/DS1* high to DTACK* high			190	ns

Note 1: Provided that the VMEbus master drives DS0*/DS1* low less than 40 ns after driving AS* low.

Note 2: Provided that the VMEbus master drives DS0*/DS1* low more than 40 ns after driving AS* low.

Table 2.7: Write Cycle Timing Module Registers

NO.	PARAMETER	NOTES	MIN	MAX	UNIT
1	AS* low to DTACK* low	1		240	ns
2	DS0* low to DTACK* low	2		175	ns
3	DS0* high to DTACK* high			175	ns

Note 1: Provided that the VMEbus master drives DS0* low less than 65 ns after driving AS* low.

Note 2: Provided that the VMEbus master drives DS0* low more than 65 ns after driving AS* low.

Figure 2.4: Interrupt Acknowledge Cycle

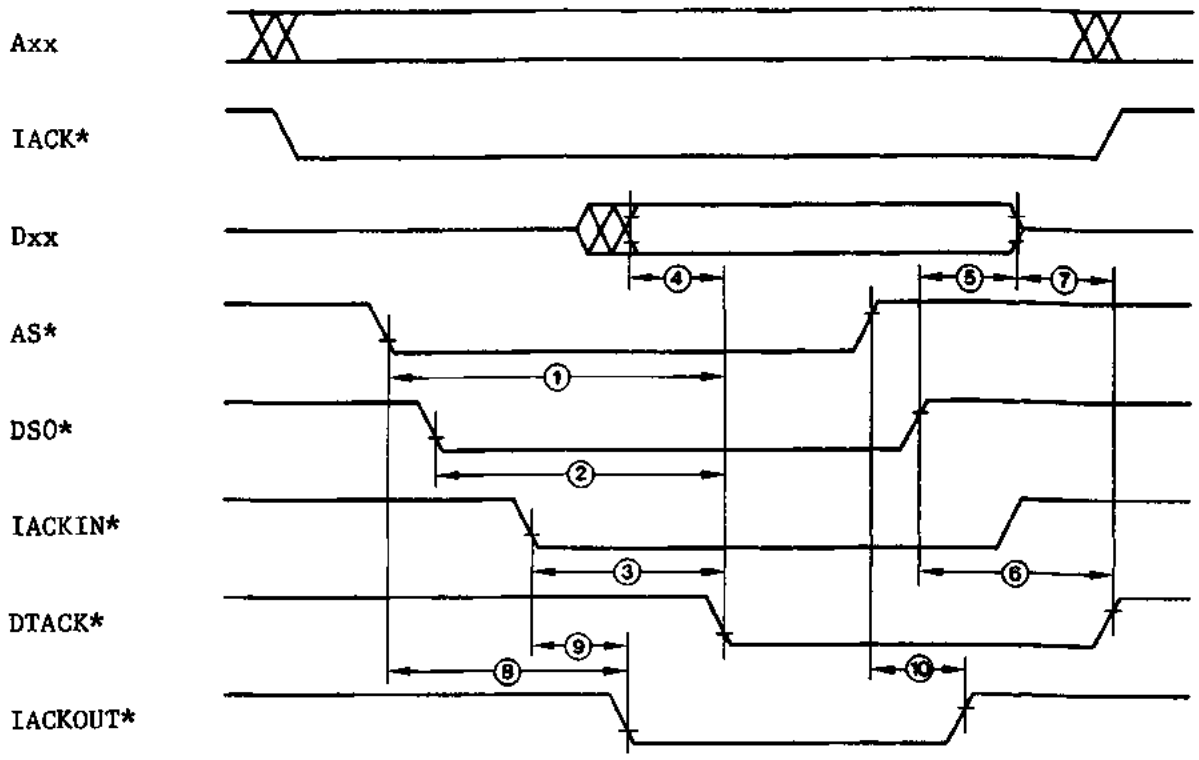


Table 2.8: Interrupt Acknowledge Cycle Timing

NO.	PARAMETER	NOTES	MIN	MAX	UNIT
1	AS* low to DTACK* low	1		365	ns
2	DS0* low to DTACK* low	1		365	ns
3	IACKIN* low to DTACK* low	1		365	ns
4	Data valid to DTACK* low			85	ns
5	DS0* high to Data invalid		20		ns
6	DS0* high to DTACK* high			130	ns
7	Data high imp. to DTACK* high		5		ns
8	AS* low to IACKOUT* low	2		225	ns
9	IACKIN* low to IACKOUT* low	3		40	ns
10	AS* high to IACKOUT* high			25	ns

Note 1: The delay time for DTACK* low is determined by the last signal AS*, DS0*, and IACKIN* to be received.

Note 2: Provided that IACKIN* is received less than 185 ns after receiving AS0* low.

Note 3: Provided that IACKIN* is received more than 185 ns after receiving AS0* low.

2.4 ADDRESS DECODER

The address decoding logic supports either the 64 kbyte (A16) short addressing, or the 16 Mbyte (A24) standard addressing, or the 4 Gbyte (A32) extended addressing range. The module's base address is jumper selectable in 256 byte steps.

The address modifier lines are decoded by a PROM which may be easily customized for specific requirements. As configured by Motorola the module will respond to address modifier codes $29 and $2D, or $39 and $3D, or $09 and $0D.

Jumpers select the required address range and define the address modifier codes which the module will respond to. The address options are defined as follows:

Table 2.9: Address Decoder Options

ADDRESS OPTION	AM CODES	AM CODE FUNCTION	ADDRESS LINES
A16	$29 $2D	Short Non-Privileged I/O Access Short Supervisory I/O Access	A01-A15
A24	$39 $3D	Standard Non-Privileged Data Access Standard Supervisory Data Access	A01-A23
A32	$09 $0D	Extended Non-Priviledged Data Access Extended Supervisory Data Access	A01-A31

Depending on jumper positioning, the module will only respond to the corresponding AM code and decode the relevant address lines. A detailed description of how to configure address option, base address and address modifier codes is given in Chapter 3. An address map is shown in Chapter 4.

2.5 PARALLEL INTERFACE AND TIMER CIRCUITS

Three MC68230 Parallel Interface/Timer devices are located on the module. Each device consists of logically independent parallel interface and timer circuits.

The parallel interfaces operate in unidirectional or bidirectional modes, 1-bit, 8-bit, or 16-bit wide. In the unidirectional modes, data direction registers determine the direction of the I/O lines. In the bidirectional modes the transfer direction is dynamically controlled by peripheral handshake lines.

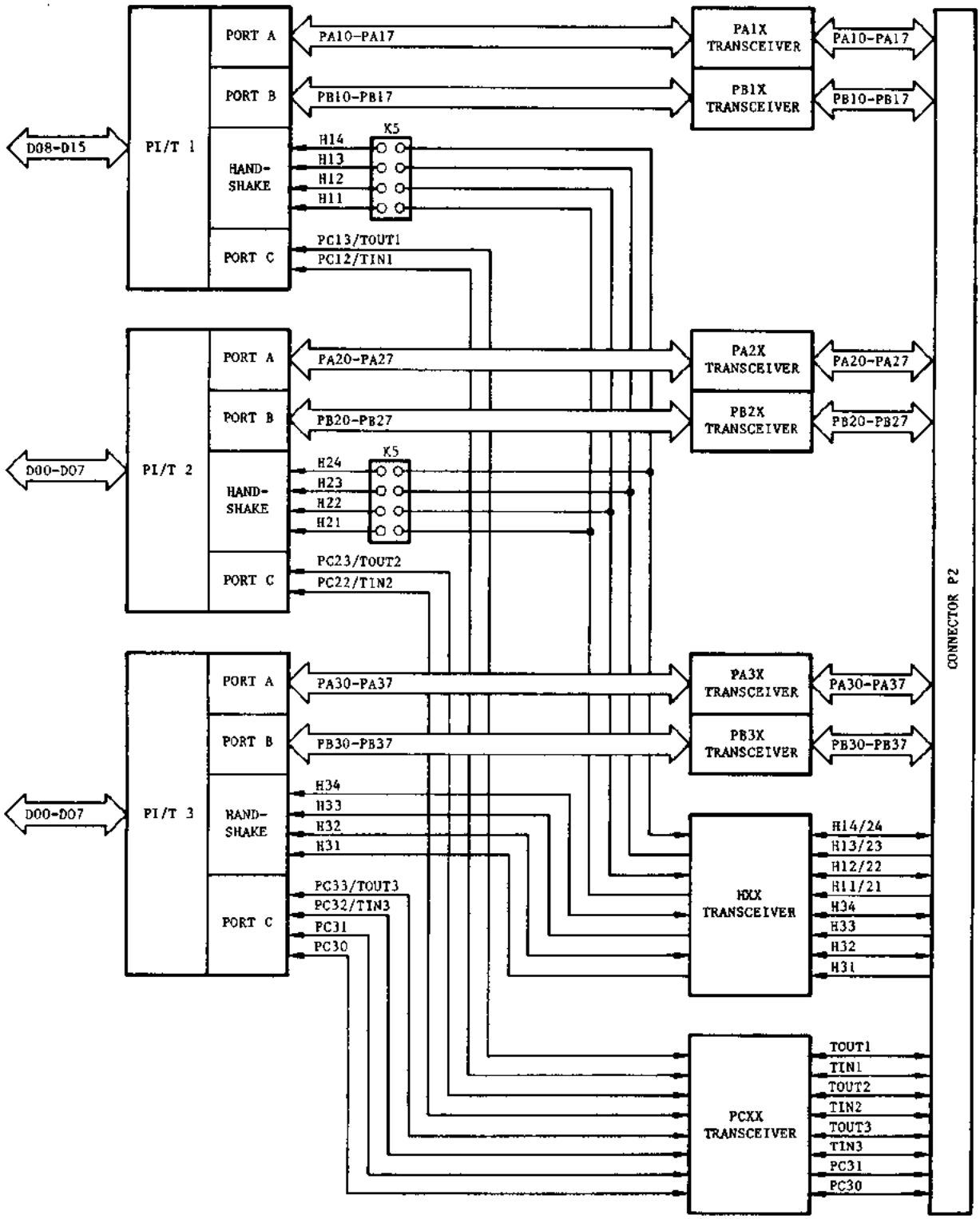
The unidirectional modes are defined as the (8-bit and 16-bit) modes 0 and 1. In mode 0, ports A and B are independent 8-bit I/O ports. In mode 1, ports A and B are concatenated to form a single 16-bit I/O port. Data transfer direction changes are performed by a programable data direction register.

The bidirectional modes are defined as the (8-bit and 16-bit) modes 2 and 3. In mode 2, ports A and B are independent 8-bit I/O ports. In mode 3, ports A and B are concatenated to to form a single 16-bit I/O port. The data transfer direction is dynamically controlled by peripheral handshake lines independent of the data direction register contents.

Each timer consists of a 24-bit counter and a 5-bit prescaler. The timers may be clocked either by the system clock or by an external clock, and can be used for peripheral functions (such as square wave generation, pulse width measurement, or event counting) or for system internal functions (such as single or periodic interrupts, elapsed time measurement, or device watchdog functions).

For a more detailed description of the MC68230 Parallel Interface/Timer devices see the data sheet in Appendix A.

Figure 2.5: Peripheral Interface Block Diagram



2.6 PERIPHERAL SIGNALS

The peripheral input/output interface consists of 64 signals routed to rows A and C of connector P2, and can be grouped into parallel I/O signals, handshake signals and timer I/O signals. A peripheral interface block diagram is shown in Figure 2.5.

All peripheral lines of the parallel interface/timer devices are connected to P2 via bidirectional GPIB transceivers (IEEE 488-1978 standard). The output characteristics of the peripheral line drivers are programmable either as active pull-up or as open-collector. For a more detailed description of the peripheral line transceivers refer to the MC3448A data sheet in Appendix B.

In modes 0 and 1 the data direction of the peripheral line transceivers for the parallel port A and B signals is controlled by registers which are accessed in parallel to the PI/T device internal data direction registers. In modes 2 and 3 the line transceiver direction is directly controlled by the handshake signals.

The data direction of the peripheral line transceivers for the handshake and port C signals is controlled by direction registers which are to be programmed separately according to the desired line operation.

A functional description of the peripheral signals is given in Table 2.10. The peripheral signal locations at P2 are shown in Table 2.11.

Table 2.10: Peripheral Signal Description

SIGNAL	SIGNAL DESCRIPTION
PA10..PA17	PI/T 1 PORT A The 8-bit parallel input/output Port A of PI/T 1.
PB10..PB17	PI/T 1 PORT B The 8-bit parallel input/output Port B of PI/T 1.
PA20..PA27	PI/T 2 PORT A The 8-bit parallel input/output Port A of PI/T 2.
PB20..PB27	PI/T 2 PORT B The 8-bit parallel input/output Port B of PI/T 2.
PA30..PA37	PI/T 3 PORT A The 8-bit parallel input/output Port A of PI/T 3.
PB30..PB37	PI/T 3 PORT B The 8-bit parallel input/output Port B of PI/T 3.

Table 2.10: Peripheral Signal Description (continued)

SIGNAL	SIGNAL DESCRIPTION
H11/21	PI/T 1 AND/OR PI/T 2 HANDSHAKE LINE H1 An interrupt input, status input, or handshake input line. H11/21 may be connected with any of the H1 pins of PI/T 1 and/or PI/T 2 by jumpers.
H12/22	PI/T 1 AND/OR PI/T 2 HANDSHAKE LINE H2 An interrupt input, status input, handshake output, or general purpose output line. H12/22 may be connected with any of the H2 pins of PI/T 1 and/or PI/T 2 by jumpers.
H13/23	PI/T 1 AND/OR PI/T 2 HANDSHAKE LINE H3 An interrupt input, status input or handshake input line. H13/23 may be connected with any of the H3 pins of PI/T 1 and/or PI/T 2 by jumpers.
H14/24	PI/T 1 AND/OR PI/T 2 HANDSHAKE LINE H4 An interrupt input, status input, handshake output, or general purpose output line. H14/24 may be connected with any of the H4 pins of PI/T 1 and/or PI/T 2 by jumpers.
H31	PI/T 3 HANDSHAKE LINE H1 The interrupt input, status input, or handshake input line H1 of PI/T 3.
H32	PI/T 3 HANDSHAKE LINE H2 The interrupt input, status input, handshake output, or general purpose output line H2 of PI/T 3.
H33	PI/T 3 HANDSHAKE LINE H3 The interrupt input, status input, or handshake input line H3 of PI/T 3.
H34	PI/T 3 HANDSHAKE LINE H4 The interrupt input, status input, handshake output, or general purpose output line H4 of PI/T 3.
PC30, PC31	PI/T 3 PORT C LINES 0 AND 1 The general purpose input/outpout lines PC0 and PC1 of PI/T 3.

Table 2.10: Peripheral Signal Description (continued)

SIGNAL	SIGNAL DESCRIPTION
TIN1	PI/T 1 TIMER INPUT The dual-function line PC2/TIN of PI/T 1 which can be used either as a general purpose input/output line or as a clock or run/halt control input to the timer.
TOUT1	PI/T 1 TIMER OUTPUT The dual-function line PC3/TOUT of PI/T 1 which can be used either as a general purpose input/output line or as a square wave output of the timer.
TIN2	PI/T 2 TIMER INPUT The dual-function line PC2/TIN of PI/T 2 which can be used either as a general purpose input/output line or as a clock or run/halt control input to the timer.
TOUT2	PI/T 2 TIMER OUTPUT The dual-function line PC3/TOUT of PI/T 2 which can be used either as a general purpose input/output line or as a square wave output of the timer.
TIN3	PI/T 3 TIMER INPUT The dual-function line PC2/TIN of PI/T 3 which can be used either as a general purpose input/output line or as a clock or run/halt control input to the timer.
TOUT3	PI/T 3 TIMER OUTPUT The dual-function line PC3/TOUT of PI/T 3 which can be used either as a general purpose input/output line or as a square wave output of the timer.

Table 2.11: Connector P2 Peripheral Signal Locations

PIN NO.	ROW A SIGNALS	ROW B SIGNALS	ROW C SIGNALS	PIN NO.
1	PA17	VMEBUS	PB17	1
2	PA16	VMEBUS	PB16	2
3	PA15	VMEBUS	PB15	3
4	PA14	VMEBUS	PB14	4
5	PA13	VMEBUS	PB13	5
6	PA12	VMEBUS	PB12	6
7	PA11	VMEBUS	PB11	7
8	PA10	VMEBUS	PB10	8
9	PA27	VMEBUS	PB27	9
10	PA26	VMEBUS	PB26	10
11	PA25	VMEBUS	PB25	11
12	PA24	VMEBUS	PB24	12
13	PA23	VMEBUS	PB23	13
14	PA22	VMEBUS	PB22	14
15	PA21	VMEBUS	PB21	15
16	PA20	VMEBUS	PB20	16
17	PA37	VMEBUS	PB37	17
18	PA36	VMEBUS	PB36	18
19	PA35	VMEBUS	PB35	19
20	PA34	VMEBUS	PB34	20
21	PA33	VMEBUS	PB33	21
22	PA32	VMEBUS	PB32	22
23	PA31	VMEBUS	PB31	23
24	PA30	VMEBUS	PB30	24
25	H12/22	VMEBUS	H14/24	25
26	H11/21	VMEBUS	H13/23	26
27	H32	VMEBUS	H34	27
28	H31	VMEBUS	H33	28
29	TIN1	VMEBUS	TOUT1	29
30	TIN2	VMEBUS	TOUT2	30
31	TIN3	VMEBUS	TOUT3	31
32	PC30	VMEBUS	PC31	32

2.7 INTERRUPTERS

Three interrupters are located on the MVME340 module, one associated with each Peripheral Interface/Timer device. Figure 2.6 is a block diagram of the complete interrupt circuitry.

An Interrupt Level Register is associated with each interrupter which enables or disables VMEbus interrupt requests and defines their priority level. As the three interrupters operate totally independent from each other, each of the Interrupt Level Registers is to be loaded with a seperate priority level to avoid VMEbus conflicts during the interrupt acknowledge cycle.

For each of the three interrupters, two interrupt sources are available; either an interrupt request generated by one of the port handshake lines, or an interrupt request generated by the timer output. The timer outputs of the PI/T devices (TOUT) are fed to the timer interrupt request inputs of the interrupters (TIRQ) through mask circuits which are gated by the Module Control Register. This prevents timer interrupts being generated unintentionally when a timer output is used for peripheral functions.

The PI/T devices contain two registers for storing seperate status/ID bytes for port interrupts and timer interrupts.

When anyone of the timer or port interrupt requests is asserted to an interrupter, and when the interrupter is enabled, it will assert a VMEbus interrupt request on the priority level specified in its associated Interrupt Level Register.

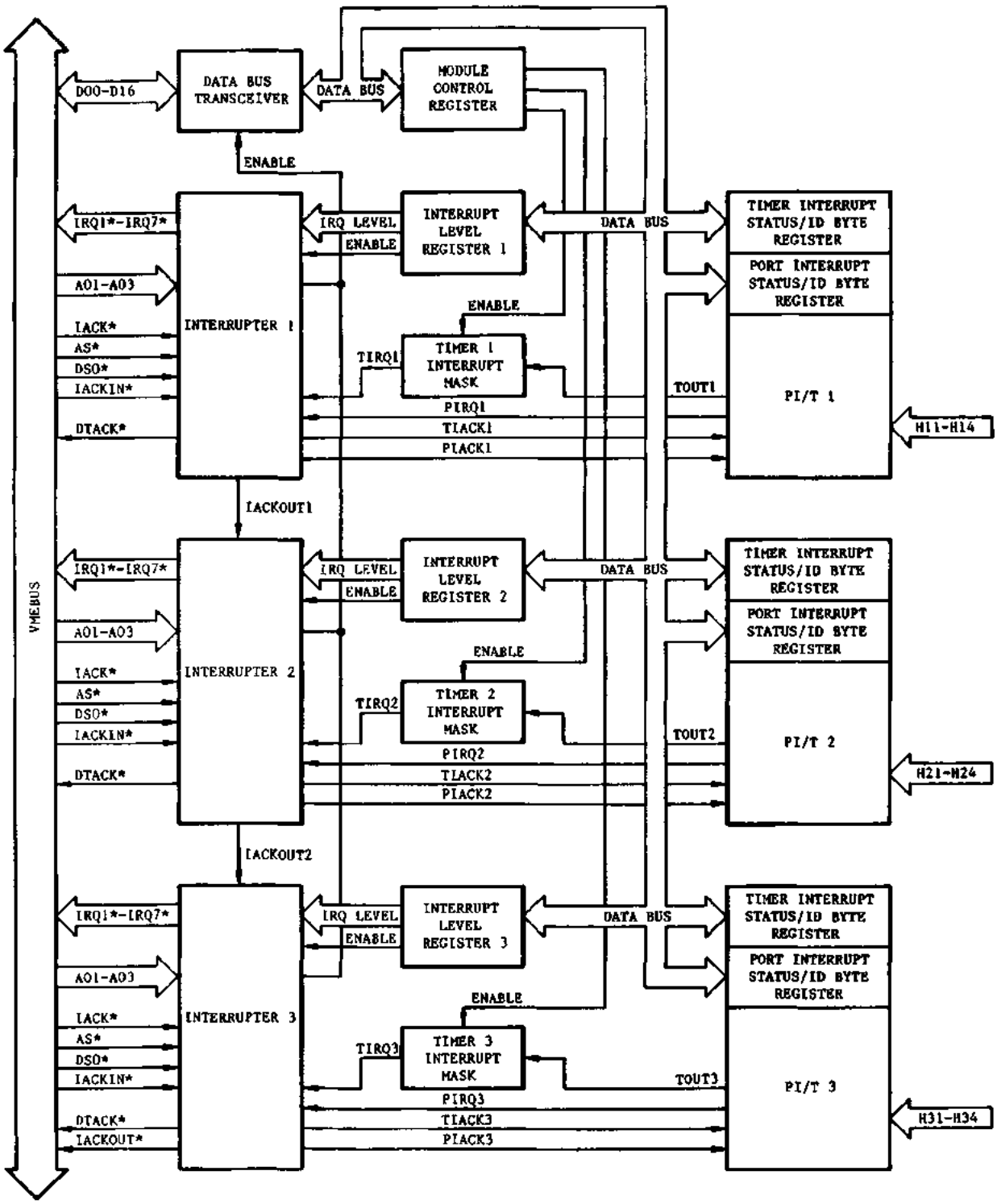
When the interrupter detects an interrupt acknowledge cycle on the VMEbus, the interrupter checks if it has an interrupt request pending, and if its own priority level matches the priority level encoded in the address lines A01-A03. If both are true, the interrupter waits for the assertion of IACKIN*, and then transmits either a timer interrupt acknowledge (TIACK) or a port interrupt acknowledge (PIACK) to the PI/T, depending on which interrupt request is pending.

The interrupter prioritizes the timer interrupts with a higher priority than the port interrupts; i. e. when both are pending, the timer interrupt request will be acknowledged first.

Upon receiving TIACK or PIACK, the PI/T places the corresponding interrupt status/ID byte on the VMEbus and asserts DTACK*.

If during a VMEbus interrupt acknowledge cycle none of the three interrupters has a request pending which matches the level encoded on the bus, the IACKIN* signal will be propagated to IACKOUT*.

Figure 2.6: Interrupter Block Diagram



2.8 MODULE CONTROL REGISTER

The Module Control Register (MCR) drives the Status LED, and masks the timer interrupt requests TIRQ1, TIRQ2 and TIRQ3.

If any of the timer outputs TOUT1, TOUT2, or TOUT3 are used for peripheral functions, the corresponding TIRQ must be masked in the MCR to prevent unintended timer interrupts. When a TIRQ is enabled, a VMEbus interrupt request will be asserted each time the corresponding timer output goes low. For further details of the MCR refer to Paragraph 4.5.

2.9 MODULE RESET

On assertion of the VMEbus SYSRESET* signal during power-up or reset the registers external to the MC68230 are cleared and the MC68230 Parallel Interface/Timer circuits are reset.

The following list summarizes the RESET conditions:

Status LED:	switched OFF
VMEbus Interrupters:	disabled
Peripheral line direction:	input (all signal lines)
Peripheral line driver characteristics:	active pull-up
Parallel Interface/Timer devices	reset

For further datails of the MC68230 reset state, refer to the data sheet in Appendix A.

2.10 MODULE CLOCK

The MVME340 module can be clocked either by the VMEbus system clock (SYSCLK) or an on-board clock oscillator supplied by the user.

The module provides an unpopulated socket at location Y1 for an on-board clock oscillator supplied by the user. The valid frequency range of the on-board oscillator is 4 to 16 MHz. The on-board clock oscillator signal is divided by two for clocking the PI/Ts.

When using an on-board clock oscillator, there will be an impact on VMEbus and peripheral timings.

Refer to Chapter 3 for hardware configuration if an on-board clock oscillator is used.

CHAPTER 3

INSTALLATION INSTRUCTIONS

3.1 INTRODUCTION

This chapter provides the user of the MVME340 Parallel Interface/Timer Module with the unpacking, inspection, module preparation and installation procedures.

3.2 UNPACKING INSTRUCTIONS

IF THE SHIPPING CARTON IS DAMAGED UPON RECEIPT, REQUEST THAT CARRIER'S AGENT BE PRESENT DURING UNPACKING AND INSPECTION OF THE MODULE.

Unpack the MVME340 Parallel Interface/Timer Module from its shipping carton. Refer to the packing list and verify that all items are present. Save the packing material for storing or reshipping the module.

AVOID TOUCHING AREAS OF MOS CIRCUITRY. STATIC DISCHARGE CAN DAMAGE INTEGRATED CIRCUITS.

3.3 INSPECTION

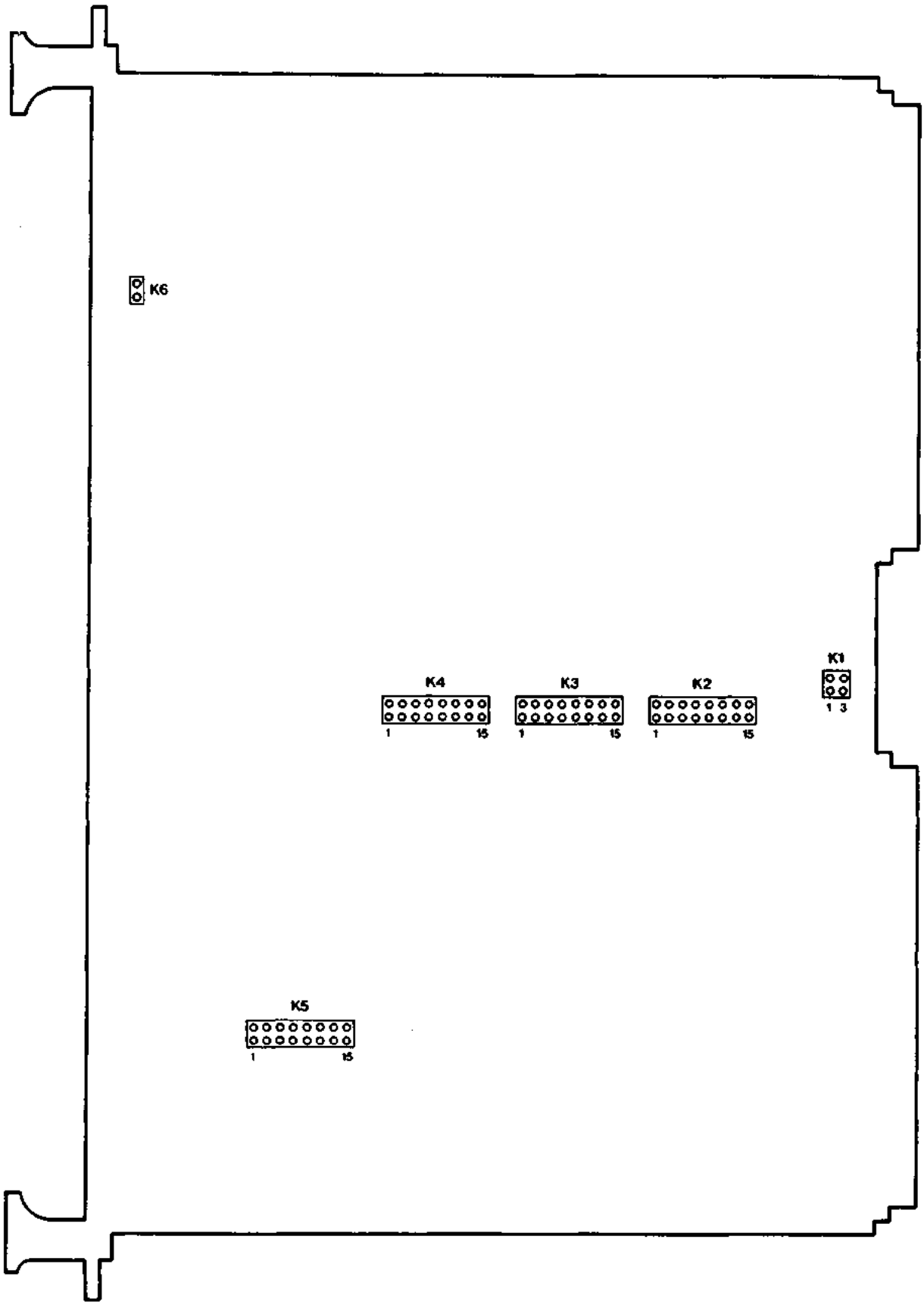
The module should be inspected upon receipt for broken, damaged or missing parts and for physical damage to the printed circuit board.

3.4 MODULE PREPARATION

This section describes the hardware preparation of the MVME340 module prior to system installation. The module is shipped with factory-installed jumpers ready for use in a VME system. However, the jumper areas must be configured according to the actual system requirements. Also, if the module shall respond to address modifier codes other than the factory-programmed codes listed in Table 2.9, the user has to program a new address modifier PROM.

Figure 3.1 illustrates the locations of the jumper areas and the address modifier PROM on the MVME340 module. Jumper area K1 determines the module address range, jumper areas K2, K3 and K4 specify the module's base address, jumper area K5 configures the peripheral handshake lines, and jumper K6 determines the clock source.

Figure 3.1: MVME340 Jumper Area Locations



3.4.1 Base Address Selection

The jumper area K1 selects the address comparator circuits and the corresponding AM codes in the address modifier decoder PROM. The module may be configured for either; A16, short I/O addressing, or A24, standard addressing, or A32, extended addressing range.

Jumper areas K2, K3 and K4 determine the base address of the module in the VMEbus address map. The base address is selectable in 256-byte steps.

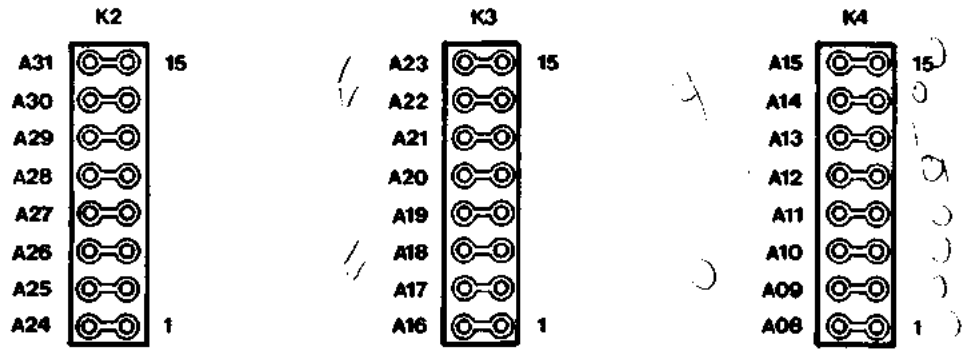
Depending on the address range determined by jumper K1, only K4 (A08-A15), or K4 and K3 (A08-A23), or K4, K3 and K2 (A08-A31) are used to decode the base address. If a jumper is set the module will respond when the corresponding address line is low. If removed the module will respond when the line is high.

Table 3.1. defines the dependency between the configuration of K1, K2, K3 and K4, the selected AM codes, the address ranges, and the numbers of decoded address lines.

Figure 3.2: Jumper Area K1



Figure 3.3: Jumper Areas K2, K3 and K4



Note: Axx = 0, if jumper is set,
Axx = 1, if jumper is removed.

Table 3.1: Base Address Configuration K1, K2, K3 and K4

K1 JUMPERS	AM CODES	ADDRESS RANGE	DECODED ADDRESS LINES	RELEVANT BASE ADDRESS JUMPERS
1-2, 3-4	$29, $2D	Short I/O	A08-A15	K4
3-4	$39, $3D	Standard	A08-A23	K4 + K3
none	$09, $0D	Extended	A08-A31	K4 + K3 + K2

3.4.2 Address Modifier Decoder

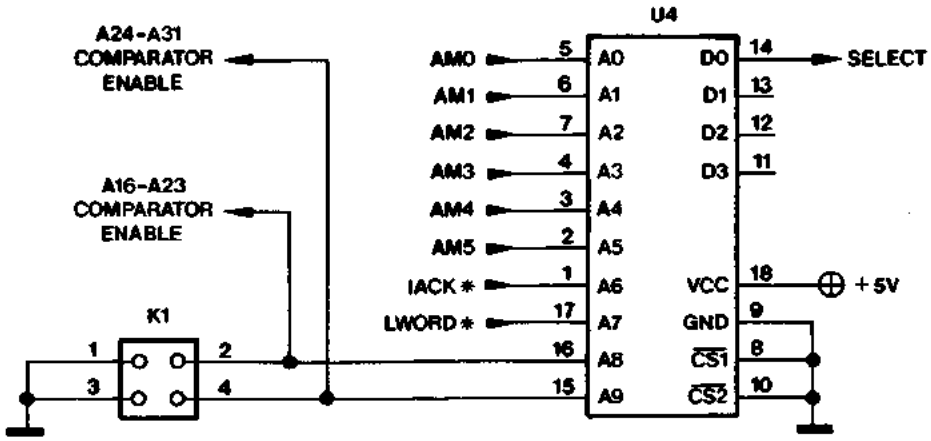
The address modifier decoder is a bipolar PROM at designation U4 on the MVME340 module. This PROM is programmed in the factory to respond to the address modifier codes for supervisory and non-privileged short I/O ($29, $2D), or standard I/O ($39, $3D), or extended I/O ($09, $0D) data access, depending on the location of jumper K1.

The user may however, select any other subset of valid address modifier codes and program the decoder PROM accordingly. Valid address modifier codes for the MVME340 modules are the codes 10-1F, 09, 0D, 29, 2D, 39, and 3D.

In addition to decoding the address modifiers, the PROM is used for disabling a board selection during interrupt acknowledge and longword transfer cycles.

Figure 3.4 illustrates the connections of the address modifier decoder PROM. The signals AM0-AM5 are fed to the PROM address inputs A0-A5, IACK* and LWORD* are fed to A6 and A7 respectively. The inputs A8 and A9 are connected to jumper area K1. The PROM data output D0 is used for the board selection.

Figure 3.4: Address Modifier Decoder PROM



The PROM may be an Advanced Micro Devices Am27S33A or any electrically and physically compatible bipolar PROM, organized in 1024 x 4 bits, with a maximum address access time of 35 ns.

Table 3.2 may be used for specifying the PROM contents. Each combination of address modifier code (00-3F) and jumper K1 configuration is represented by a corresponding PROM address. All PROM locations belonging to address modifier codes and K1 configurations to which the module shall respond must be programmed with the data "0". All other PROM locations must be programmed with the data "F". For unused and invalid locations "F" is already entered in the table.

Table 3.2: Address Modifier Decoder PROM Specification

K1 JUMPER	AM CODE	FUNCTION	ADDRESS	DATA
none	20-3F	Not Applicable	3E0-3FF	F
"	10-1F	User Defined Extended Access	3D0-3DF	.
"	0E-0F	Not Applicable	3CE-3CF	F
"	0D	Extended Supervisory Data Access	3CD	.
"	0A-0C	Not Applicable	3CA-3CC	F
"	09	Extended Non-Privileged Data Access	3C9	.
"	00-08	Not Applicable	3C0-3C8	F
"	xx	Not Applicable	300-3BF	F
(1-2)	xx	N.A. - Invalid Jumper Configuration	200-2FF	F
3-4	3E-3F	Not Applicable	1FE-1FF	F
"	3D	Standard Supervisory Data Access	1FD	.
"	3A-3C	Not Applicable	1FA-1FC	F
"	39	Standard Non-Privileged Data Access	1F9	.
"	20-38	Not Applicable	1E0-1F8	F
"	10-1F	User Defined Standard Access	1D0-1DF	.
"	00-0F	Not Applicable	1C0-1CF	F
"	xx	Not Applicable	100-1BF	F
1-2,3-4	2E-3F	Not Applicable	0EE-0FF	F
"	2D	Short Supervisory I/O Access	0ED	.
"	2A-2C	Not Applicable	0EA-0EC	F
"	29	Short Non-Privileged I/O Access	0E9	.
"	20-28	Not Applicable	0E0-0E8	F
"	10-1F	User Defined Short I/O Access	0D0-0DF	.
"	00-0F	Not Applicable	0C0-0CF	F
"	xx	Not Applicable	000-0BF	F

Note: The contents of addresses marked with "." in the data column may be defined by the user. Data "F" disables, data "0" enables the MVME340 module for the corresponding address modifier code and K1 configuration.

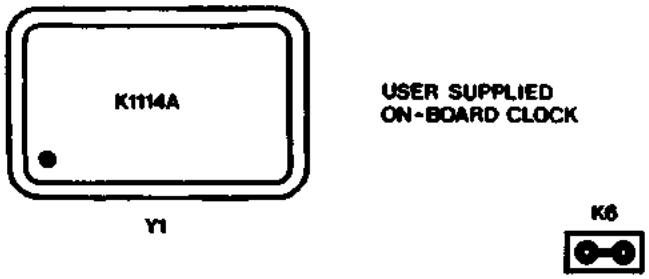
3.4.3 Local Clock Option

The jumper K6 determines whether the module will be clocked by an on-board clock oscillator supplied by the user, or by the VMEbus SYSCLK line.

If an on-board clock oscillator is used it is to be fitted in the unpopulated socket at location Y1, and the jumper is to be located. With the jumper removed the module is clocked by the SYSCLK line.

The recommended part is Motorola K1114A Crystal Clock Oscillator. The valid frequency range is 4 to 16 MHz.

Figure 3.5: Jumper Area K6 and IC socket Y1



3.4.4 Handshake Line Configuration

The jumper area K5 determines which of the handshake lines of PI/T 1 and PI/T 2 are connected to connector P2. The handshake pins at P2 can be so configured that they are connected to either PI/T 1 or PI/T 2, or to both. The actual configuration depends on the intended mode of operation.

Figure 3.6: Jumper Area K5

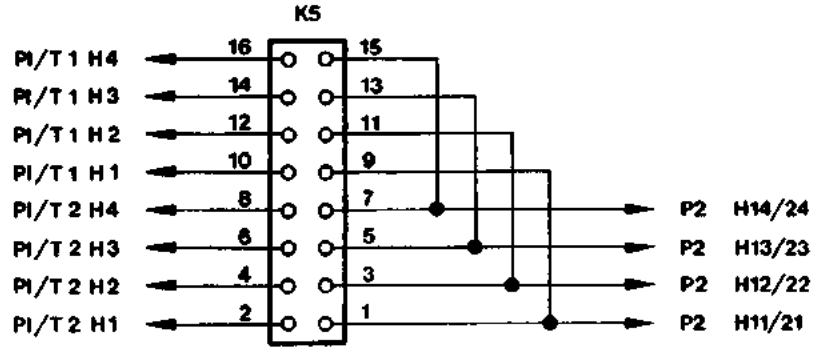


Table 3.3: Handshake Line Configuration K5

K5 JUMPER	DESCRIPTION
1-2	Handshake line H11/21 connected to PI/T 2 H1
3-4	Handshake line H12/22 connected to PI/T 2 H2
5-6	Handshake line H13/23 connected to PI/T 2 H3
7-8	Handshake line H14/24 connected to PI/T 2 H4
9-10	Handshake line H11/21 connected to PI/T 1 H1
11-12	Handshake line H12/22 connected to PI/T 1 H2
13-14	Handshake line H13/23 connected to PI/T 1 H3
15-16	Handshake line H14/24 connected to PI/T 1 H4

3.4.5 Peripheral Line Termination

The MVME340 module provides areas for the location of user supplied termination resistor networks. The termination resistor networks may be 9-pin or 10-pin SIL packages soldered in the locations RP1 to RP8.

Resistor networks may be optionally used as: pull-up, pull-down, or voltage dividers. Figure 3.7 illustrates the resistor network location for each option. Table 3.4 shows which P2 lines are connected to which network.

Figure 3.7: Termination Resistor Networks RP1-RP8

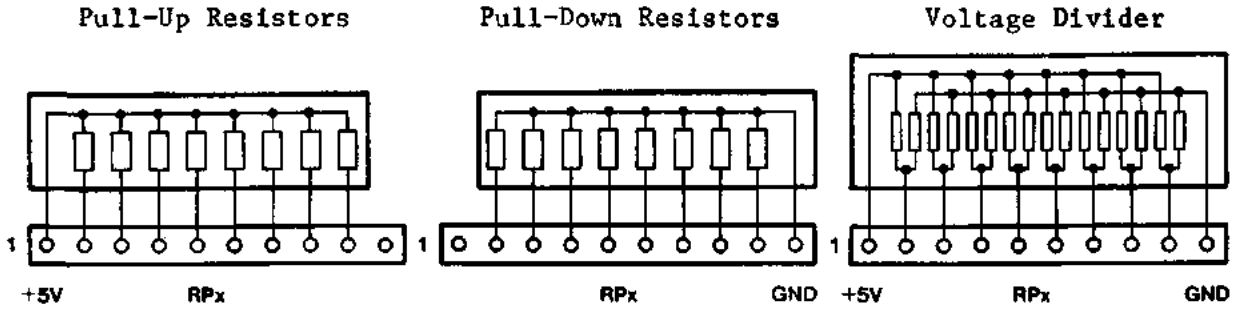


Table 3.4: Resistor Network/Port Signal Locations

RP#	PORT SIGNALS
RP1	PA10..PA17
RP2	PB10..PB17
RP3	PA20..PA27
RP4	PB20..PB27
RP5	PA30..PA37
RP6	PB30..PB37
RP7	H11/21, H12/22, H13/23, H14/24, H31, H32, H33, H34
RP8	PC30, PC31, TIN1, TIN2, TIN3, TOUT1, TOUT2, TOUT3

3.4.6 Peripheral Line Connection

The MVMW340 product package contains an interface connector assembly for connecting two 64-pin flat-ribbon cables to connector P2.

The connector assembly can easily be mounted in any double height VME card cage and distributes the 64 I/O lines of P2 and additional ground lines to the DIN 41651 connectors Pa and Pc. The signals are so arranged that each signal line is separated by a ground line when 64-pin flat-ribbon cables are used for the peripheral connection.

Figure 3.8 shows the connection of the MVME340 module and two 64-pin cables to the interface connector assembly. Table 3.5 shows the interface connector signal location.

The maximum line length and load of the peripheral signal lines is to conform with the IEEE 488-1975 electrical specifications.

Note that this connector assembly cannot be used in conjunction with extended addressing.

Figure 3.8: Peripheral Connection Through Connector Assembly

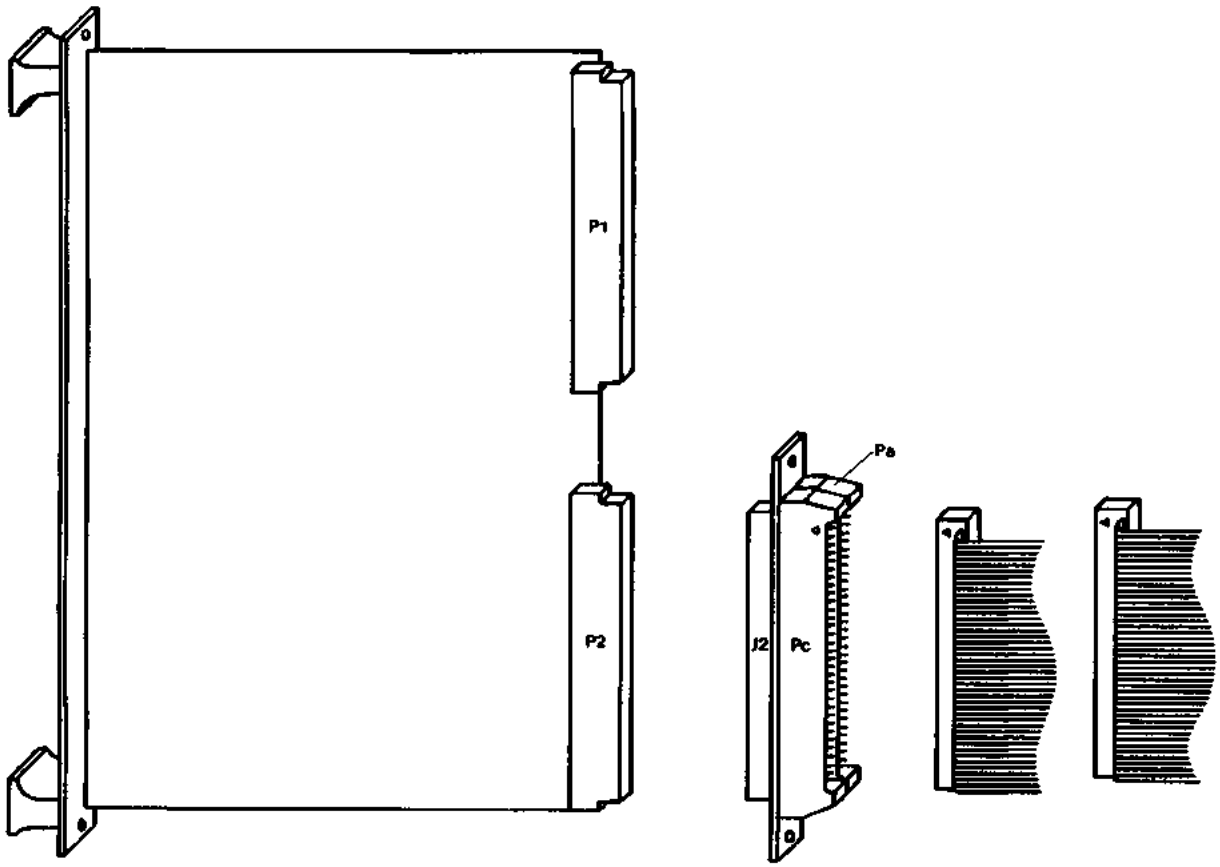


Table 3.5: Interface Connector Signal Locations

Pc

PIN	SIGNAL	SIGNAL	PIN
1	GND	PB17	2
3	GND	PB16	4
5	GND	PB15	6
7	GND	PB14	8
9	GND	PB13	10
11	GND	PB12	12
13	GND	PB11	14
15	GND	PB10	16
17	GND	PB27	18
19	GND	PB26	20
21	GND	PB25	22
23	GND	PB24	24
25	GND	PB23	26
27	GND	PB22	28
29	GND	PB21	30
31	GND	PB20	32
33	GND	PB37	34
35	GND	PB36	36
37	GND	PB35	38
39	GND	PB34	40
41	GND	PB33	42
43	GND	PB32	44
45	GND	PB31	46
47	GND	PB30	48
49	GND	H14/24	50
51	GND	H13/23	52
53	GND	H34	54
55	GND	H33	56
57	GND	TOUT1	58
59	GND	TOUT2	60
61	GND	TOUT3	62
63	GND	PC31	64

Pa

PIN	SIGNAL	SIGNAL	PIN
1	PA17	GND	2
3	PA16	GND	4
5	PA15	GND	6
7	PA14	GND	8
9	PA13	GND	10
11	PA12	GND	12
13	PA11	GND	14
15	PA10	GND	16
17	PA27	GND	18
19	PA26	GND	20
21	PA25	GND	22
23	PA24	GND	24
25	PA23	GND	26
27	PA22	GND	28
29	PA21	GND	30
31	PA20	GND	32
33	PA37	GND	34
35	PA36	GND	36
37	PA35	GND	38
39	PA34	GND	40
41	PA33	GND	42
43	PA32	GND	44
45	PA31	GND	46
47	PA30	GND	48
49	H12/22	GND	50
51	H11/21	GND	52
53	H32	GND	54
55	H31	GND	56
57	TIN1	GND	58
59	TIN2	GND	60
61	TIN3	GND	62
63	PC30	GND	64

3.5 MODULE INSTALLATION

When the MVME340 Parallel Interface/Timer module has been configured as desired by the user, it is ready to be installed in a VME chassis as follows:

a. Turn all equipment power off.

b. Insert the MVME340 module in any VMEbus card slot other than A1.

c. Secure the module in place with two screws on the front panel.

d. Turn the equipment power on.

PRIOR TO INSERTING OR REMOVING MODULES FROM THE VME CHASSIS, ENSURE THAT POWER IS TURNED OFF TO AVOID DAMAGE TO THE COMPONENTS.

CHAPTER 4

OPERATING INSTRUCTIONS

4.1 INTRODUCTION

This Chapter provides the user of the MVME340 Parallel Interface/Timer module with an address map description, configuration instructions and programming considerations for the parallel interfaces, timers and interrupters.

4.2 ADDRESS MAP

The MVME340 module contains an address area of 128 consecutive words for the transfer of data between the operating system and the registers. The module is accessed from the VMEbus through an option A16:D16, or A23:D16, or A32:D16 slave interface, and is selected with the address modifier codes $29 and $2D (short I/O), or $39 and $3D (standard), or $09 and $0D (extended). The base address is selectable in 256-byte boundaries.

Table 4.1 gives a detailed description of the register address map as seen from the VMEbus. Note that the addresses are given relative to the module base address.

Table 4.1: MVME340 Address Map

ADDR	EVEN BYTES	ODD BYTES	ADDR
FE	not used	not used	FF
:			:
:			8F
:		Driver Characteristic Control Register	8D
:		PI/T 3 Peripheral Line Direction Reg.	8B
:		PI/T 1/2 Peripheral Line Direction Reg.	89
:		Module Control Register	87
:		PI/T 3 Interrupt Level Register	85
:		PI/T 2 Interrupt Level Register	83
:		PI/T 1 Interrupt Level Register	81
:		not used	7F
:			:
:			77
:		PI/T 3 Timer Status Register	75
:		PI/T 3 Count Register (low)	73
:		PI/T 3 Count Register (mid)	71
:		PI/T 3 Count Register (high)	6F
:		not used	6D
:		PI/T 3 Counter Preload Register (low)	6B
:		PI/T 3 Counter Preload Register (mid)	69
:		PI/T 3 Counter Preload Register (high)	67
:	not used	not used	65
:		PI/T 3 Timer Interrupt Status/ID Byte	63
:		PI/T 3 Timer Control Register	61
:		not used	5F
:			5D
:		PI/T 3 Port Status Register	5B
:		PI/T 3 Port C Data Register	59
:		PI/T 3 Port B Alternate Register	57
:		PI/T 3 Port A Alternate Register	55
:		PI/T 3 Port B Data Register	53
:		PI/T 3 Port A Data Register	51
:		PI/T 3 Port B Control Register	4F
:		PI/T 3 Port A Control Register	4D
:		PI/T 3 Port Interrupt Status/ID Byte	4B
:		PI/T 3 Port C Data Direction Register	49
:		PI/T 3 Port B Data Direction Register	47
:		PI/T 3 Port A Data Direction Register	45
:		PI/T 3 Port Service Request Register	43
:		PI/T 3 Port General Control Register	41
:		not used	3F
:			:
36			37
34	PI/T 1 Timer Status Register	PI/T 2 Timer Status Register	35
32	PI/T 1 Count Register (low)	PI/T 2 Count Register (low)	33
30	PI/T 1 Count Register (mid)	PI/T 2 Count Register (mid)	31
2E	PI/T 1 Count Register (high)	PI/T 2 Count Register (high)	2F
2C	not used	not used	2D
2A	PI/T 1 Counter Preload Register (low)	PI/T 2 Counter Preload Register (low)	2B
28	PI/T 1 Counter Preload Register (mid)	PI/T 2 Counter Preload Register (mid)	29
26	PI/T 1 Counter Preload Register (high)	PI/T 2 Counter Preload Register (high)	27
24	not used	not used	25
22	PI/T 1 Timer Interrupt Status/ID Byte	PI/T 2 Timer Interrupt Status/ID Byte	23
20	PI/T 1 Timer Control Register	PI/T 2 Timer Control Register	21
1E	not used	not used	1F
1C			1D
1A	PI/T 1 Port Status Register	PI/T 2 Port Status Register	18
18	PI/T 1 Port C Data Register	PI/T 2 Port C Data Register	19
16	PI/T 1 Port B Alternate Register	PI/T 2 Port B Alternate Register	17
14	PI/T 1 Port A Alternate Register	PI/T 2 Port A Alternate Register	15
12	PI/T 1 Port B Data Register	PI/T 2 Port B Data Register	13
10	PI/T 1 Port A Data Register	PI/T 2 Port A Data Register	11
0E	PI/T 1 Port B Control Register	PI/T 2 Port B Control Register	0F
0C	PI/T 1 Port A Control Register	PI/T 2 Port A Control Register	0D
0A	PI/T 1 Port Interrupt Status/ID Byte	PI/T 2 Port Interrupt Status/ID Byte	0B
08	PI/T 1 Port C Data Direction Register	PI/T 2 Port C Data Direction Register	09
06	PI/T 1 Port B Data Direction Register	PI/T 2 Port B Data Direction Register	07
04	PI/T 1 Port A Data Direction Register	PI/T 2 Port A Data Direction Register	05
02	PI/T 1 Port Service Request Register	PI/T 2 Port Service Request Register	03
00	PI/T 1 Port General Control Register	PI/T 2 Port General Control Register	01

4.3 PARALLEL INTERFACE CONFIGURATION

The transfer of data between peripheral devices and the VMEbus may be performed in several ways.

Data transfers between the VMEbus and the PI/T devices may be either:

- byte wide data to and from each PI/T device independently, or
- word wide data to and from PI/T 1 and PI/T 2 operating in parallel.

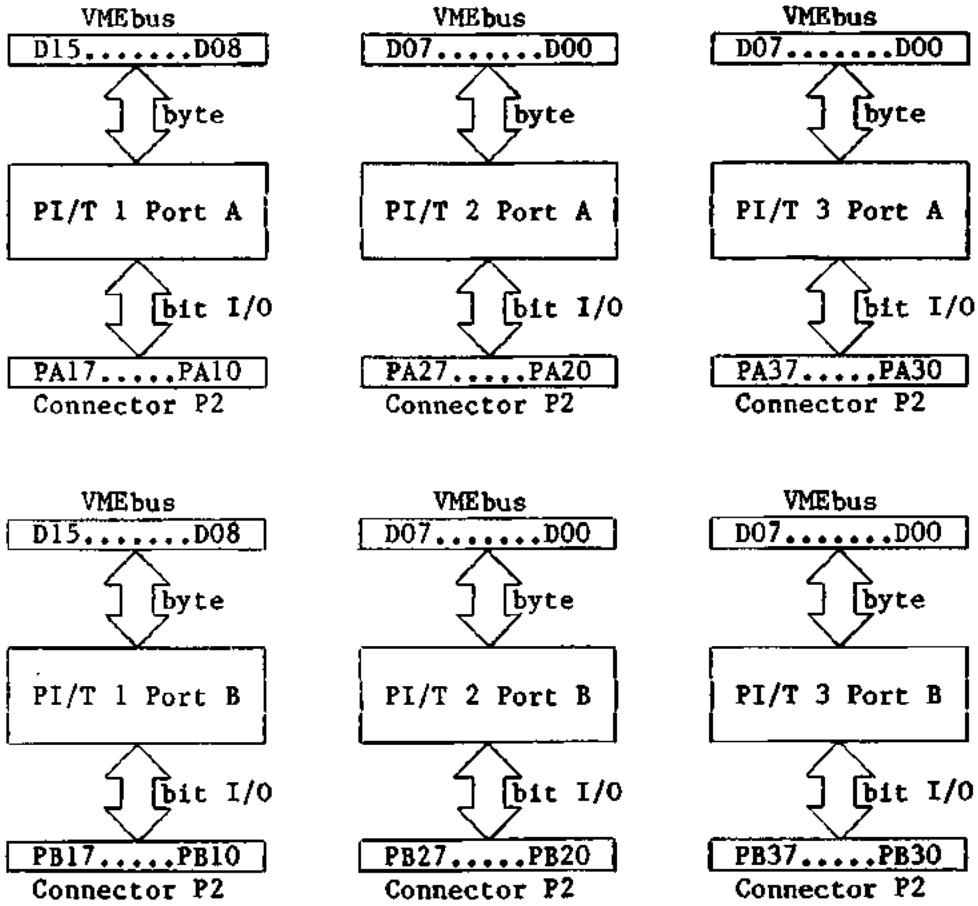
Data transfers between the PI/T devices and peripherals may be either:

- single bit input/output to and from any port of any PI/T device, or
- 8-bit input/output to and from any port of any PI/T device, or
- 16-bit input/output to and from any PI/T device when port A and port B are concatenated, or
- 16-bit input/output to and from both ports A or both ports B of PI/T 1 and PI/T 2 operating in parallel, or
- 32-bit input/output to and from PI/T 1 and PI/T 2 operating in parallel with port A and port B of both PI/T devices concatenated.

In the following paragraphs each of these options and the corresponding port configurations will be described. For detailed information about the various port modes and submodes refer to the MC68230 Parallel Interface/ Timer Data Sheet in Appendix A.

4.3.1 Single Bit Input/Output

Single bit input/output can be performed through any port of any PI/T device. The figure below illustrates the correlations between the VMEbus data lines, the PI/T ports, and the peripheral lines for single bit I/O.



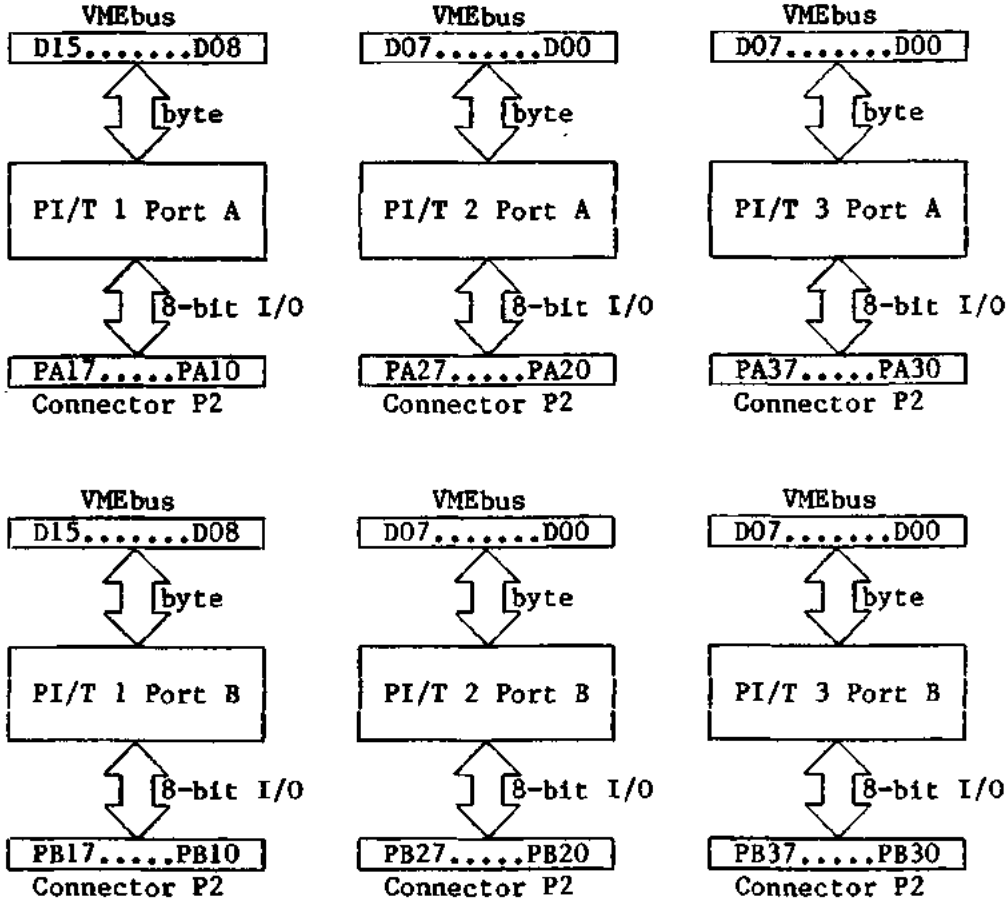
Ports A or B used for single bit I/O are to be programmed for Mode 0 Submode 1X. Ports A can also be used for single bit I/O in Mode 2.

The handshake lines associated with those ports may be used as status inputs or interrupt inputs or general purpose outputs. Note that handshake lines of independant PI/T 1 and PI/T 2 ports must not be shortened by jumpers on K5.

Data transfers to and from the VMEbus are performed by independent byte accesses to each PI/T port.

4.3.2 8-Bit Input/Output

8-bit input/output can be performed through any port of any PI/T device. The figure below illustrates the correlations between the VMEbus data lines, the PI/T ports, and the peripheral lines for 8-bit I/O.



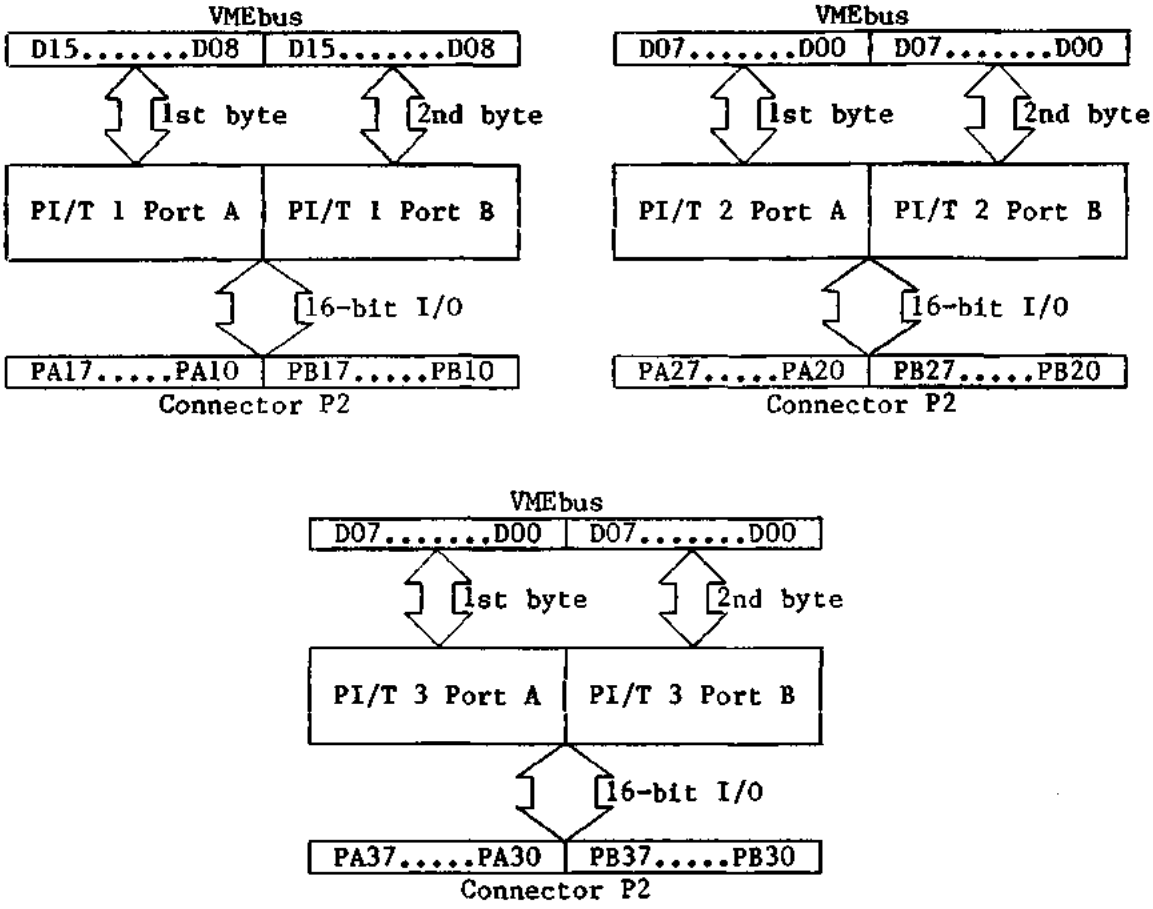
Ports A or B used for unidirectional 8-bit input are to be programmed for Mode 0 Submode 00. Ports A or B used for unidirectional 8-bit output are to be programmed for Mode 0 Submode 01. Ports B used for bidirectional 8-bit input/output are to be programmed for Mode 2.

Handshake lines associated with unidirectional ports may be used as status inputs, interrupt inputs, general purpose outputs, or input/output control signals. Handshake lines associated with bidirectional ports are used for input/output control only. Note that handshake lines of independant PI/T 1 and PI/T 2 ports must not be shortened by jumpers on K5.

Data transfers to and from the VMEbus are performed by independent byte accesses to each PI/T port.

4.3.3 Port-Concatenated 16-Bit Input/Output

16-bit input/output can be performed through any PI/T device when port A and port B of the device are concatenated. The figure below illustrates the correlations between the VMEbus data lines, the PI/T ports, and the peripheral lines for port-concatenated 16-bit I/O.



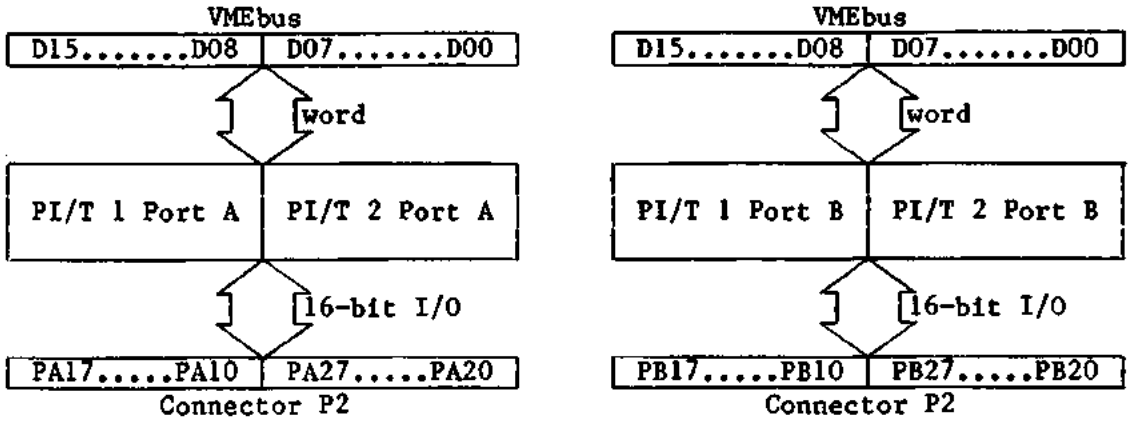
PI/T devices used for unidirectional port-concatenated 16-bit input are to be programmed for Mode 1 Port A Submode XX Port B Submode X0. PI/T devices used for unidirectional port-concatenated 16-bit output are to be programmed for Mode 1 Port A Submode XX Port B Submode X1. PI/T devices used for bidirectional port-concatenated 16-bit input/output are to be programmed for Mode 3.

Handshake lines associated with unidirectional ports may be used as status inputs, interrupt inputs, general purpose outputs, or input/output control signals. Handshake lines associated with bidirectional ports are used for input/output control only. Note that handshake lines of independant PI/T 1 and PI/T 2 ports must not be shortened by jumpers on K5.

Data transfers to and from the VMEbus are performed by two consecutive byte accesses, first to port A, second to port B.

4.3.4 Device-Parallel 16-Bit Input/Output

16-bit input/output can be performed through both ports A or both ports B of PI/T 1 and PI/T 2 when the devices operate in parallel. The figure below illustrates the correlations between the VMEbus data lines, the PI/T ports, and the peripheral lines for device-parallel 16-bit I/O.



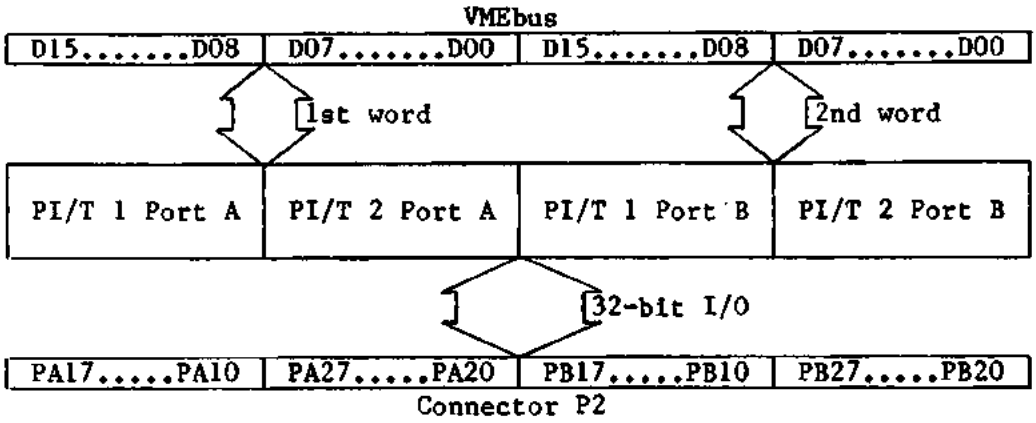
Both ports A or B used for unidirectional device-parallel 16-bit input are to be programmed for Mode 0 Submode 00. Both ports A or B used for unidirectional device-parallel 16-bit output are to be programmed for Mode 0 Submode 01. Both ports B used for bidirectional device-parallel 16-bit input/output are to be programmed for Mode 2.

Handshake lines associated with unidirectional ports may be used as status inputs, interrupt inputs, general purpose outputs, or input/output control signals. Handshake lines associated with bidirectional ports are used for input/output control only. Note that handshake lines used for input/output control in the device-parallel configuration are to be connected to both PI/T devices 1 and 2 by jumpers on K5. This guarantees proper parallel operation of the ports.

Data transfers to and from the VMEbus are performed by word accesses to both ports A or ports B of PI/T 1 and PI/T 2.

4.3.5 32-Bit Input/Output

32-bit input/output can be performed through the four ports A and ports B of PI/T 1 and PI/T 2 when both ports of each PI/T device are concatenated and both devices operate in parallel. The figure below illustrates the correlations between the VMEbus data lines, the PI/T ports, and the peripheral lines for 32-bit I/O.



For unidirectional 32-bit input both PI/T devices are to be programmed for Mode 1 Port A Submode XX Port B Submode X0. For unidirectional 32-bit output both PI/T devices are to be programmed for Mode 1 Port A Submode XX Port B Submode X1. For bidirectional 32-bit input/output both PI/T devices are to be programmed for Mode 3.

In the unidirectional modes the handshake lines may be used as status inputs, interrupt inputs, general purpose outputs, or input/output control signals. In the bidirectional mode the handshake lines are used for input/output control only. Note that handshake lines used for input/output control in the 32-bit configuration are to be connected to both PI/T devices 1 and 2 by jumpers on K5. This guarantees proper parallel operation of the ports.

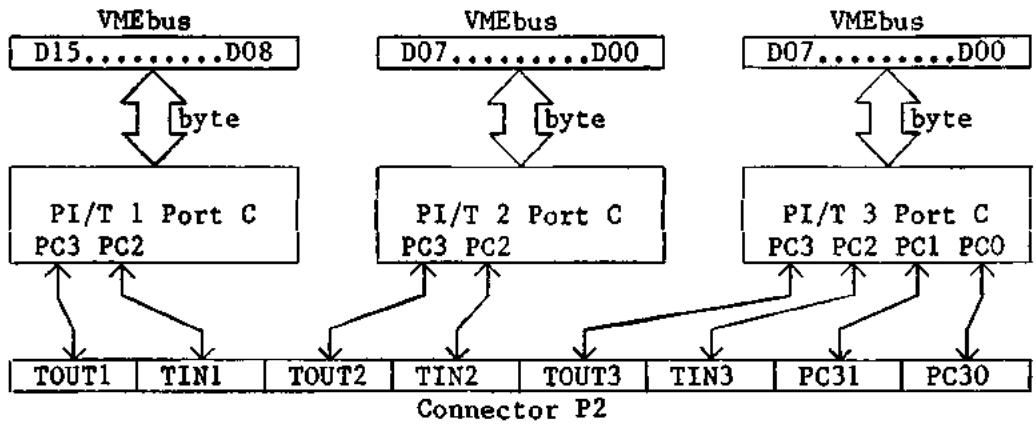
Data transfers to and from the VMEbus are performed by two consecutive word accesses, first to both ports A, second to both ports B of PI/T 1 and PI/T 2.

4.4 TIMER AND PORT C CONFIGURATION

The timers in the PI/T devices can be used either for peripheral functions (such as square wave generation, pulse width measurement, or event counting) or for system internal functions (such as single or periodic interrupts, elapsed time measurement, or device watchdog functions).

The timer input and output lines are part of the PI/T port C dual-function lines. Those lines which are not employed for timer input/output functions in the actual application may be used for general purpose single bit input/output functions. Also available for single bit input/output are two general purpose lines of PI/T 3 port C.

The figure below illustrates the correlations between the VMEbus data lines, the PI/T ports C, and the peripheral lines at connector P2.



The TIN1, TIN2 and TIN3 lines may either be used as single bit I/O lines (port C function) or as clock or run/halt control inputs to the timers (alternate function). The TOUT1, TOUT2 and TOUT3 lines may either be used as single bit I/O lines (port C function) or as square wave outputs from the timers (alternate function). The PC30 and PC31 lines are single function lines and can only be used for general purpose single bit I/O.

Data transfers to and from the VMEbus are performed by independent byte accesses to each PI/T device.

4.5 REGISTER DESCRIPTIONS

The following section describes all registers on the MVME340 module and their functions, and specifies the contents written or read after reset, for initialization and during operation.

The contents of this section differ to that of the MC68230 PI/T data sheet to the extent that the information given here relates only to the configurations that the MVME340 module supports, not what the MC68230 device generally can do.

For a more detailed description of the MC68230 Parallel Interface/Timer functions and operations refer to the data sheet in Appendix A.

4.5.1 Port General Control Registers (PGCR)

7	6	5	4	3	2	1	0
Port Mode Control		H34 Enable	H12 Enable	H4 Sense	H3 Sense	H2 Sense	H1 Sense

The Port General Control Registers control the operational modes of ports A and B, enable and disable the handshake lines, and define the handshake line sense.

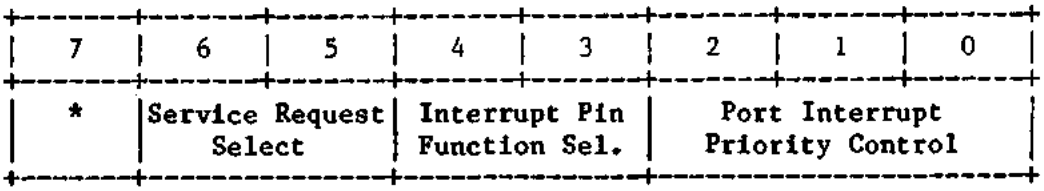
The Port Mode Control field should be altered only when the H12 Enable and H34 Enable bits are 0.

The direction control logic for the peripheral line transceivers on the MVME340 assumes that the handshake line H1 is active high in modes 2 and 3. Therefore the H1 sense bit must always be set to 1 when using modes 2 or 3.

The PGCRs are read/write registers and are cleared to 0 on reset.

BIT	DESCRIPTION
7-6	Port Mode Control 0 0 = Mode 0 (unidirectional 8-bit mode) 0 1 = Mode 1 (unidirectional 16-bit mode) 1 0 = Mode 2 (bidirectional 8-bit mode) 1 1 = Mode 3 (bidirectional 16-bit mode)
5	H34 Enable 0 = disabled 1 = enabled
4	H12 Enable 0 = disabled 1 = enabled
3	H4 Sense 0 = active low 1 = active high
2	H3 Sense 0 = active low 1 = active high
1	H2 Sense 0 = active low 1 = active high
0	H1 Sense 0 = active low (invalid for modes 2 and 3) 1 = active high

4.5.2 Port Service Request Registers (PSRR)



The Port Service Request Registers determine the function of the PC4/DMAREQ, PC5/PIRQ and PC6/PIACK dual function lines, and define the priority among all port interrupt sources.

As the MVME340 does not support DMA, the Service Request Select field should always be set to 0.

To avoid malfunctions of the interrupt control logic on the MVME340, both bits of the Interrupt Pin Function Select field should always be set to 1, even if interrupts are not used.

As the interrupt control logic on the MVME340 cannot handle more than one port interrupt source per PI/T device at any one time, the Port Interrupt Priority Control field will not affect interrupt operation and may be set to any value. However, it is recommended that bits 0, 1 and 2 be changed only when all port interrupts are disabled, or known to remain inactive.

The PSRRs are read/write registers and are cleared to 0 on reset.

BIT	DESCRIPTION
7	Not used (always read as 0)
6-5	Service Request Select 0 x = DMA request disabled 1 x = invalid
4-3	Interrupt Pin Function Select 0 x = invalid x 0 = invalid 1 1 = port interrupt request/acknowledge pins enabled
2-0	Port Interrupt Priority Control x x x = irrelevant

4.5.3 Port A Data Direction Registers (PADDR)

7	6	5	4	3	2	1	0
PA7 Direct. Control	PA6 Direct. Control	PA5 Direct. Control	PA4 Direct. Control	PA3 Direct. Control	PA2 Direct. Control	PA1 Direct. Control	PA0 Direct. Control

The Port A Data Direction Registers determine the direction and buffering characteristics of each of the Port A lines when the port is operating in mode 0, 1 or 2. One bit in the registers is assigned to each line. Whereby a 0 determines that the line is used as an input, and a 1 determines it is used as an output.

When writing to the PI/T Port Data Direction Registers, the corresponding registers in the transceiver control logic are accessed in parallel to set the direction of the peripheral line transceivers accordingly.

In Mode 3 the PADDR is ignored and the direction of the peripheral lines is controlled by the handshake signals. Therefore, when changing from Mode 3 to any of the Modes 0, 1 or 2, the PADDR must be re-programmed to assure that the PI/T port data direction and the peripheral line transceiver direction do coincide.

The PADDRs are read/write registers and are cleared to 0 on reset.

BIT	DESCRIPTION
7-0	PA7..PA0 Direction Control 0 = input 1 = output

4.5.4 Port B Data Direction Registers (PBDDR)

7	6	5	4	3	2	1	0
PB7 Direct. Control	PB6 Direct. Control	PB5 Direct. Control	PB4 Direct. Control	PB3 Direct. Control	PB2 Direct. Control	PB1 Direct. Control	PB0 Direct. Control

The Port B Data Direction Registers determine the direction and buffering characteristics of each of the Port B lines when the port is operating in mode 0 or 1. One bit in the registers is assigned to each line. Whereby a 0 determines that the line is used as an input, and a 1 determines it is used as an output.

When writing to the PI/T Port Data Direction Registers, the corresponding registers in the transceiver control logic are accessed in parallel to set the direction of the peripheral line transceivers accordingly.

In Modes 2 and 3 the PBDDR is ignored and the direction of the peripheral lines is controlled by the handshake signals. Therefore, when changing from Mode 2 or 3 to any of the Modes 0 or 1, the PBDDR must be re-programmed to assure that the PI/T port data direction and the peripheral line transceiver direction do coincide.

The PBDDRs are read/write registers and are cleared to 0 on reset.

BIT	DESCRIPTION
7-0	PB7..PB0 Direction Control 0 = input 1 = output

4.5.5 Port C Data Direction Registers (PCDDR)

7	6	5	4	3	2	1	0
PC7 Direct. Control	PC6 Direct. Control	PC5 Direct. Control	PC4 Direct. Control	PC3 Direct. Control	PC2 Direct. Control	PC1 Direct. Control	PC0 Direct. Control

The Port C Data Direction Registers specify the direction of each dual-function line that is chosen for Port C operation. One bit in the registers is assigned to each line. Whereby a 0 determines that the line is used as an input, and a 1 determines it is used as an output. The PCDDRs, along with bits that define the respective line's function, also specify the exact hardware to be accessed at the Port C Data Register addresses. (See the Port C Data Register description for more details.)

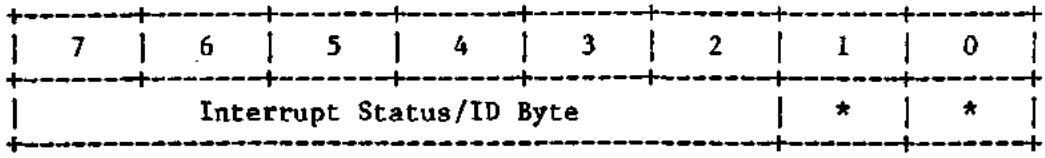
Note that on the MVME340 only the timer outputs (PC3) and inputs (PC2) of any PI/T and the single-function lines (PC1 and PC0) of PI/T 3 are available for Port C operation. All other dual-function lines must be programmed for the alternate functions and their corresponding bits in the PCDDRs will have no operational effect.

The direction of the peripheral line transceivers must be programmed to coincide with the direction of the Port C signals for the desired operation. (See the Peripheral Line Direction Register description for more details.)

The PCDDRs are read/write registers and are cleared to 0 on reset.

BIT	DESCRIPTION
7-4	PC7..PC4 Direction Control for Port C Function x = not used (should be 0)
3-0	PC3..PC0 Direction Control for Port C Function 0 = input 1 = output

4.5.6 Port Interrupt Status/ID Byte Registers (PISBR)



The Port Interrupt Status/ID Byte Registers contain the six most significant bits of the four port interrupt status/ID bytes. This byte is placed on the VMEbus during the interrupt acknowledge cycle with the two least significant bits reflecting the source of the interrupt.

The PISBRs are read/write registers and the value $0F is loaded on reset.

BIT	DESCRIPTION
7-2	Interrupt Status/ID Byte (six most significant bits)
1-0	Interrupt Source 0 0 = H1 source 0 1 = H2 source 1 0 = H3 source 1 1 = H4 source

4.5.7 Port A Control Registers (PACR)

7	6	5	4	3	2	1	0
Port A Submode		H2 Control			H2 Int. Enable	H1 Int. Enable	H1 Status Control

The Port A Control Registers, in conjunction with the programmed modes and Port B submodes, control the operation of the Ports A and handshake lines H1 and H2.

When the Port A Submode field is relevant in a mode/submode definition, the field must not be altered unless the H12 Enable bit in the Port General Control Register is 0.

As the interrupt control logic on the MVME340 cannot handle more than one port interrupt source per PI/T device at any one time, only one of the handshake line interrupt enable bits in both (Port A and Port B) Control Registers of each PI/T may be set.

Note that the direction of the peripheral line transceivers must be programmed to coincide with the direction of the handshake signals for the desired operation. (See the Peripheral Line Direction Register description for more details.)

The PACRs are read/write registers and are cleared to 0 on reset.

The following description is so organized that for each mode/submode all programmable options of each bit are given.

BIT DESCRIPTION — Mode 0 Port A Submode 00

7-6 Port A Submode
0 0 = pin-definable double-buffered input or single-buffered output

5-3 H2 Control
0 x x = input - status only
1 0 0 = output - always negated
1 0 1 = output - always asserted
1 1 0 = output - interlocked input handshake protocol
1 1 1 = output - pulsed input handshake protocol

2 H2 Interrupt Enable
0 = disabled
1 = enabled

1 H1 Interrupt Enable
0 = disabled
1 = enabled

0 H1 Status Control
x = not used

BIT	DESCRIPTION	Mode 0 Port A Submode 01

7-6 Port A Submode
0 1 = pin-definable double-buffered output or non-latched input

5-3 H2 Control
0 x x = input - status only
1 0 0 = output - always negated
1 0 1 = output - always asserted
1 1 0 = output - interlocked output handshake protocol
1 1 1 = output - pulsed output handshake protocol

2 H2 Interrupt Enable
0 = disabled
1 = enabled

1 H1 Interrupt Enable
0 = disabled
1 = enabled

0 H1 Status Control
0 = The H1S status bit is 1 when either the Port A initial or final output latch can accept new data. It is 0 when both latches are full and cannot accept new data.
1 = The H1S status bit is 1 when both of the Port A output latches are empty. It is 0 when at least one latch is full.

BIT	DESCRIPTION	Mode 0 Port A Submode 1X

7-6 Port A Submode
1 x = pin-definable single-buffered output or non-latched input

5-3 H2 Control
0 x x = input - status only
1 x 0 = output - always negated
1 x 1 = output - always asserted

2 H2 Interrupt Enable
0 = disabled
1 = enabled

1 H1 Interrupt Enable
0 = disabled
1 = enabled

0 H1 Status Control
x = not used

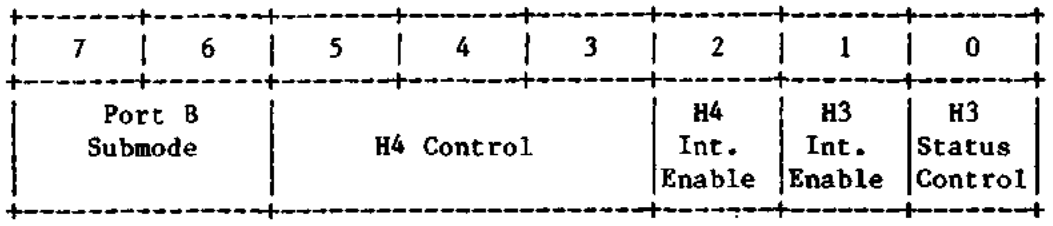
BIT	DESCRIPTION	Mode 1 Port A Submode XX Port B Submode X0
7-6	Port A Submode x x = not used (Submode configured by PBCR)	
5-3	H2 Control 0 x x = input - status only 1 x 0 = output - always negated 1 x 1 = output - always asserted	
2	H2 Interrupt Enable 0 = disabled 1 = enabled	
1	H1 Interrupt Enable 0 = disabled 1 = enabled	
0	H1 Status Control x = not used	

BIT	DESCRIPTION	Mode 1 Port A Submode XX Port B Submode X1
7-6	Port A Submode x x = not used (Submode configured by PBCR)	
5-3	H2 Control 0 x x = input - status only 1 x 0 = output - always negated 1 x 1 = output - always asserted	
2	H2 Interrupt Enable 0 = disabled 1 = enabled	
1	H1 Interrupt Enable 0 = disabled 1 = enabled	
0	H1 Status Control x = not used	

BIT	DESCRIPTION	Mode 2
7-6	Port A Submode x x = not used	
5-3	H2 Control x x 0 = output - interlocked output handshake protocol x x 1 = output - pulsed output handshake protocol	
2	H2 Interrupt Enable 0 = disabled 1 = enabled	
1	H1 Interrupt Enable 0 = disabled 1 = enabled	
0	H1 Status Control 0 = The H1S status bit is 1 when either the Port B initial or final output latch can accept new data. It is 0 when both latches are full and cannot accept new data. 1 = The H1S status bit is 1 when both of the Port B output latches are empty. It is 0 when at least one latch is full.	

BIT	DESCRIPTION	Mode 3
7-6	Port A Submode x x = not used	
5-3	H2 Control x x 0 = output - interlocked output handshake protocol x x 1 = output - pulsed output handshake protocol	
2	H2 Interrupt Enable 0 = disabled 1 = enabled	
1	H1 Interrupt Enable 0 = disabled 1 = enabled	
0	H1 Status Control 0 = The H1S status bit is 1 when either the initial or final output latch of Port A and B can accept new data. It is 0 when both latches are full and cannot accept new data. 1 = The H1S status bit is 1 when both the initial and final output latches of Ports A and B are empty. It is 0 when either the initial or final latch of Ports A and B is full.	

4.5.8 Port B Control Registers (PBCR)



The Port B Control Registers, in conjunction with the programmed modes, control the operation of the Ports B and handshake lines H3 and H4.

When the Port B Submode field is relevant in a mode/submode definition, the field must not be altered unless the H34 Enable bit in the Port General Control Register is 0.

As the interrupt control logic on the MVME340 cannot handle more than one port interrupt source per PI/T device at any one time, only one of the handshake line interrupt enable bits in both (Port A and Port B) Control Registers of each PI/T may be set.

Note that the direction of the peripheral line transceivers must be programmed to coincide with the direction of the handshake signals for the desired operation. (See the Peripheral Line Direction Register description for more details.)

The PBCRs are read/write registers and are cleared to 0 on reset.

The following description is so organized that for each mode/submode all programmable options of each bit are given.

BIT	DESCRIPTION	Mode 0 Port B Submode 00
7-6	Port B Submode 0 0 = pin-definable double-buffered input or single-buffered output	
5-3	H4 Control 0 x x = input - status only 1 0 0 = output - always negated 1 0 1 = output - always asserted 1 1 0 = output - interlocked input handshake protocol 1 1 1 = output - pulsed input handshake protocol	
2	H4 Interrupt Enable 0 = disabled 1 = enabled	
1	H3 Interrupt Enable 0 = disabled 1 = enabled	
0	H3 Status Control x = not used	

BIT	DESCRIPTION	Mode 0 Port B Submode 01

7-6 Port B Submode
0 1 = pin-definable double-buffered output or non-latched input

5-3 H4 Control
0 x x = input - status only
1 0 0 = output - always negated
1 0 1 = output - always asserted
1 1 0 = output - interlocked output handshake protocol
1 1 1 = output - pulsed output handshake protocol

2 H4 Interrupt Enable
0 = disabled
1 = enabled

1 H3 Interrupt Enable
0 = disabled
1 = enabled

0 H3 Status Control
0 = The H3S status bit is 1 when either the Port B initial or final output latch can accept new data. It is 0 when both latches are full and cannot accept new data.
1 = The H3S status bit is 1 when both of the Port B output latches are empty. It is 0 when at least one latch is full.

BIT	DESCRIPTION	Mode 0 Port B Submode 1X

7-6 Port B Submode
1 x = pin-definable single-buffered output or non-latched input

5-3 H4 Control
0 x x = input - status only
1 x 0 = output - always negated
1 x 1 = output - always asserted

2 H4 Interrupt Enable
0 = disabled
1 = enabled

1 H3 Interrupt Enable
0 = disabled
1 = enabled

0 H3 Status Control
x = not used

BIT	DESCRIPTION	Mode 1 Port B Submode X0

7-6 Port B Submode
x 0 = pin-definable double-buffered input or single-buffered output

5-3 H4 Control
0 x x = input - status only
1 0 0 = output - always negated
1 0 1 = output - always asserted
1 1 0 = output - interlocked input handshake protocol
1 1 1 = output - pulsed input handshake protocol

2 H4 Interrupt Enable
0 = disabled
1 = enabled

1 H3 Interrupt Enable
0 = disabled
1 = enabled

0 H3 Status Control
x = not used

BIT	DESCRIPTION	Mode 1 Port B Submode X1

7-6 Port B Submode
x 1 = pin-definable double buffered output or non-latched input

5-3 H4 Control
0 x x = input - status only
1 0 0 = output - always negated
1 0 1 = output - always asserted
1 1 0 = output - interlocked output handshake protocol
1 1 1 = output - pulsed output handshake protocol

2 H4 Interrupt Enable
0 = disabled
1 = enabled

1 H3 Interrupt Enable
0 = disabled
1 = enabled

0 H3 Status Control
0 = The H3S status bit is 1 when either the initial or final output latch of Port A and B can accept new data. It is 0 when both latches are full and cannot accept new data.
1 = The H3S status bit is 1 when both the initial and final output latches of Ports A and B are empty. It is 0 when either the initial or final latch of Ports A and B is full.

BIT	DESCRIPTION	Mode 2
7-6	Port B Submode x x = not used	
5-3	H4 Control x x 0 = output - interlocked input handshake protocol x x 1 = output - pulsed input handshake protocol	
2	H4 Interrupt Enable 0 = disabled 1 = enabled	
1	H3 Interrupt Enable 0 = disabled 1 = enabled	
0	H3 Status Control x = not used	

BIT	DESCRIPTION	Mode 3
7-6	Port B Submode x x = not used	
5-3	H4 Control x x 0 = output - interlocked input handshake protocol x x 1 = output - pulsed input handshake protocol	
2	H4 Interrupt Enable 0 = disabled 1 = enabled	
1	H3 Interrupt Enable 0 = disabled 1 = enabled	
0	H3 Status Control x = not used	

4.5.9 Port A Data Registers (PADR)

7	6	5	4	3	2	1	0
PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0

The Port A Data Registers are addresses for moving data to and from the Port A lines. Each bit in the register corresponds to one I/O line. The actual data directions and paths are determined by the Port A Data Direction Registers and the chosen modes and submodes.

The PADRs read/write registers and are not affected by reset.

BIT	DESCRIPTION
7-0	Peripheral Signals PA7..PA0 0 = PAx low 1 = PAx high

4.5.10 Port B Data Registers (PBDR)

7	6	5	4	3	2	1	0
PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0

The Port B Data Registers are addresses for moving data to and from the Port B lines. Each bit in the register corresponds to one I/O line. The actual data directions and paths are determined by the Port B Data Direction Registers and the chosen modes and submodes.

The PBDRs read/write registers and are not affected by reset.

BIT	DESCRIPTION
7-0	Peripheral Signals PB7..PB0 0 = PBx low 1 = PBx high

4.5.11 Port A Alternate Registers (PAAR)

7	6	5	4	3	2	1	0
PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0

The Port A Alternate Registers are alternate addresses for reading the Port A lines. Each bit in the register corresponds to one I/O line. In all modes the instantaneous line level is read and no input latching is performed.

The PAARs read-only registers.

BIT	DESCRIPTION
7-0	Peripheral Lines PA7..PA0 0 = PAx low 1 = PAx high

4.5.12 Port B Alternate Registers (PBAR)

7	6	5	4	3	2	1	0
PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0

The Port B Alternate Registers are alternate addresses for reading the Port B lines. Each bit in the register corresponds to one I/O line. In all modes the instantaneous line level is read and no input latching is performed.

The PBARs read-only registers.

BIT	DESCRIPTION
7-0	Peripheral Lines PB7..PB0 0 = PBx low 1 = PBx high

4.5.13 Port C Data Registers (PCDR)

7	6	5	4	3	2	1	0
PC7/ TIACK*	PC6/ PIACK*	PC5/ PIRQ*	PC4/ DMAREQ*	PC3/ TOUT	PC2/ TIN	PC1	PC0

The Port C Data Registers are addresses for moving data to and from the Port C dual function lines. Each bit in the registers corresponds to one I/O line. The PCDRs are single buffered for output lines, and not buffered for input lines.

The hardware access is determined by the type of bus cycle and the individual conditions affecting each line. These conditions are:

1) Whether the line is used for the port C or alternate function.
2) Whether the PCDDR indicates the input or output direction.

The table below illustrates the hardware access for the different conditions.

Read Port C Data Register			
Port C function PCDDR = 0	Port C function PCDDR = 1	Altern.function PCDDR = 0	Altern.function PCDDR = 1
line	Port C output register buffer enabled	line	Port C output register buffer disabled

Write Port C Data Register			
Port C function PCDDR = 0	Port C function PCDDR = 1	Altern.function PCDDR = 0	Altern.function PCDDR = 1
Port C output register buffer disabled	Port C output register buffer enabled	Port C output register buffer disabled	Port C output register buffer disabled

Note that on the MVME340 only the timer outputs (PC3) and inputs (PC2) of any PI/T and the single function lines (PC1 and PC0) of PI/T 3 are available for Port C operation. All other dual-function lines must be programmed for the alternate functions.

The PCDRs are read/write registers and are not affected by reset.

BIT	DESCRIPTION
7-0	Peripheral Lines PC7..PC0 0 = PCx low 1 = PCx high

4.5.14 Port Status Registers (PSR)

7	6	5	4	3	2	1	0
H4	H3	H2	H1	H4S	H3S	H2S	H1S

The Port Status Registers contain information regarding handshake pin activity.

Bits 7-4 reflect the instantaneous level of the handshake lines, and are independent of the handshake line sense bits in the Port General Control Registers.

Bits 3-0 are the respective handshake status bits, and their operation depends on the mode and submode of the respective PI/T. The status bits are flip-flops that are set to 1 by the occurrence of the asserted edge of the corresponding handshake input line. To clear a status bit that is resettable by a direct clear operation, a 1 must be written into the bit position of the PSR corresponding to the desired status bit. For status bits that are not resettable by the direct method, the data written to the PSR has no effect.

The PSRs are read/write registers. The handshake status bits are cleared on reset. A write to the PSRs may perform a special status resetting operation.

BIT	DESCRIPTION
7-4	Handshake Lines H4..H1 read 0 = Hx low read 1 = Hx high write x = no effect
3-0	Handshake Status H4S..H1S read 0 = negated, inactive read 1 = asserted, active write 0 = no effect write 1 = clear status bit, if resettable. Otherwise no effect.

4.5.15 Timer Control Register (TCR)

7	6	5	4	3	2	1	0
TOUT/TIACK Control			Zero D. Control	*	Clock Control		Timer Enable

The Timer Control Registers determine all operations of the timers.

The TOUT/TIACK Control field selects either the Port C function, or the timer output function, or the interrupt request function for the PC3/TOUT line. Note that the corresponding TIRQ Enable bit in the Module Control Register must be set when a timer is used for interrupts; otherwise the bit must be cleared. (See the Module Control Register description for more details.)

The Zero Detect Control bit specifies whether the counter receives data from the Counter Preload Register or continues counting when zero is detected.

The Clock Control field selects either the Port C function, or the run/halt control function, or the clock input function for the PC2/TIN line. This field also determines the use of the prescaler and whether the module clock or the TIN line is used as the clock source for the timer.

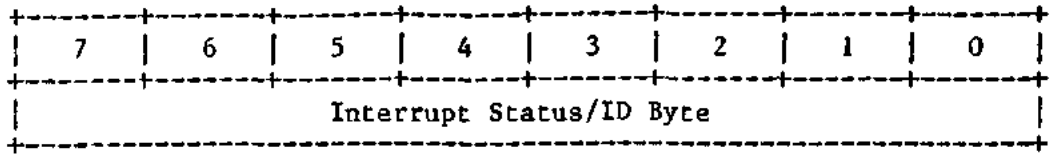
The Timer Enable bit determines whether the timer is in the run or halt state.

Note that the direction of the peripheral line transceivers must be programmed to coincide with the direction of the Port C signals for the desired operation. (See the Peripheral Line Direction Register description for more details.)

The TCRs are read/write registers and are cleared to 0 on reset.

BIT	DESCRIPTION
7-5	TOUT/TIACK Control 0 0 x = The PC3/TOUT line carries the Port C function. 0 1 x = The PC3/TOUT line carries the timer output function. In the run state it is used as a square wave output and is toggled on zero detect. In the halt state it is always high. 1 0 0 = The PC3/TOUT line carries the interrupt request function. However, the timer interrupt is disabled; thus, the TOUT line is always high and no interrupt request is asserted on the VMEbus. 1 0 1 = The PC3/TOUT line carries the interrupt request function. The timer interrupt is enabled; thus, the TOUT line is low when the ZDS status bit is 1, and an interrupt request is asserted on the VMEbus. 1 1 x = invalid
4	Zero Detect Control 0 = The counter is loaded from the Counter Preload Register on the first clock to the 24-bit counter after zero detect, and resumes counting. 1 = The counter rolls over on zero detect, then continues counting.
3	Not used (always read as 0)
2-1	Clock Control 0 0 = The PC2/TIN line carries the Port C function. The module clock is used for clocking the prescaler. The 24-bit counter is decremented or loaded from the Counter Preload Registers when the prescaler rolls over from $00 to $1F. 0 1 = The PC2/TIN line carries the run/halt control function. The module clock is used for clocking the prescaler. The 24-bit counter is decremented or loaded from the Counter Preload Registers when the prescaler rolls over from $00 to $1F. The timer is in the run state when the TIN line is high and the Timer Enable bit is set. Otherwise the timer is in the halt state. 1 0 = The PC2/TIN line carries the clock input function. The prescaler is decremented following the rising edge of TIN after synchronization with the module clock. The 24-bit counter is decremented or loaded from the Counter Preload Registers when the prescaler rolls over from $00 to $1F. 1 1 = The PC2/TIN line carries the clock input function. The prescaler is not used. The 24-bit counter is decremented or loaded from the Counter Preload Registers following the rising edge of TIN after synchronization with the module clock.
0	Timer Enable 0 = timer in halt state 1 = timer in run state

4.5.16 Timer Interrupt Status/ID Byte Registers (TISBR)



The Timer Interrupt Status/ID Byte Registers contain the interrupt status/ID bytes of the timers which are placed on the VMEbus during the interrupt acknowledge cycle.

The TISBRs are read/write registers and the value $0F is loaded on reset.

BIT	DESCRIPTION
7-0	Interrupt Status/ID Byte

4.5.17 Counter Preload Registers High, Mid, Low (CPRH-CPRL)

7	6	5	4	3	2	1	0	
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	CPRH
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	CPRM
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	CPRL

The Counter Preload Registers (High, Mid, Low) are groups of three 8-bit registers which contain the data to be transferred to the counters.

To insure proper timer operation, a value of $000000 must not be stored in the Counter Preload Registers.

The CPRHs, CPRMs and CPRLs are read/write registers and are not affected by reset.

REGISTER	BIT	DESCRIPTION
CPRH	7-0	Counter Preload Value (High Byte)
CPRM	7-0	Counter Preload Value (Mid Byte)
CPRL	7-0	Counter Preload Value (Low Byte)

4.5.18 Count Registers High, Mid, Low (CNTRH-CNTRL)

7	6	5	4	3	2	1	0	
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	CNTRH
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	CNTRM
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	CNTRL

The Count Registers (High, Mid, Low) are groups of three 8-bit addresses at which the instantaneous value of the counters can be read.

The contents of the counters are not latched during a read cycle; therefore the data read at these addresses is not guaranteed if the timer is in the run state.

The CNTRHs, CNTRMs and CNTRLs are read-only registers. The counters are not affected by reset.

REGISTER	BIT	DESCRIPTION
CNTRH	7-0	Counter Instantaneous Value (High Byte)
CNTRM	7-0	Counter Instantaneous Value (Mid Byte)
CNTRL	7-0	Counter Instantaneous Value (Low Byte)

4.5.19 Timer Status Registers (TSR)

7	6	5	4	3	2	1	0
*	*	*	*	*	*	*	ZDS

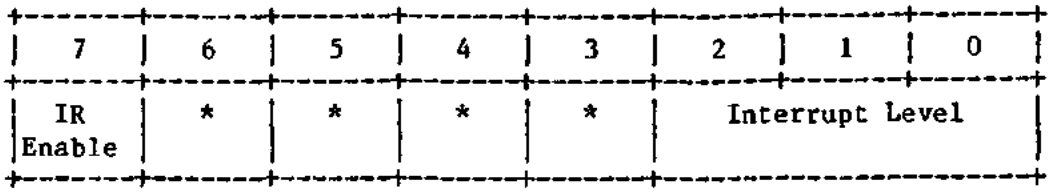
The Timer Status Registers contain one bit from which the zero detect status can be determined.

The Zero Detect Status bit is a flip-flop that is set to 1 when the 24-bit counter decrements from $000001 to $000000. The ZDS bit is reset to 0 when the timer is halted, or by writing a 1 into bit 0 of the TSR (direct clear operation).

The TSRs are read/write registers. The ZDS bit is cleared to 0 on reset. A write to the TSRs may perform a special status resetting operation.

BIT	DESCRIPTION
7-1	Not used (always read as 0)
0	Zero Detect Status read 0 = no zero count detected since last reset operation read 1 = zero count detected write 0 = no effect write 1 = reset ZDS bit

4.5.20 Interrupt Level Registers (ILR)



The Interrupt Level Registers enable/disable the VMEbus interrupters and define their priority level.

To ensure proper interrupt operation, each of the three ILRs is to be loaded with a separate interrupt priority level. The Interrupt Level Register contents are not to be changed while the corresponding interrupter has an interrupt request pending on the VMEbus.

The ILRs are read/write registers and are cleared to 0 on reset.

BIT	DESCRIPTION
7	Interrupter Enable 0 = disabled 1 = enabled
6-3	Not used (read as random values)
2-0	Interrupt Request Level 1 1 1 = level 7 1 1 0 = level 6 1 0 1 = level 5 1 0 0 = level 4 0 1 1 = level 3 0 1 0 = level 2 0 0 1 = level 1 0 0 0 = no interrupt

4.5.21 Module Control Register (MCR)

7	6	5	4	3	2	1	0
STATUS LED On	*	*	*	*	TIRQ3 Enable	TIRQ2 Enable	TIRQ1 Enable

The Module Control Register drives the STATUS LED, and masks the timer interrupt requests TIRQ1, TIRQ2 and TIRQ3.

If any of the timer outputs TOUT1, TOUT2, TOUT3 are used for peripheral functions, the corresponding Timer Interrupt Request Enable bit in the MCR must be cleared to avoid unintended timer interrupts. When a Timer Interrupt Request Enable bit is set, a VMEbus interrupt request will be asserted each time the corresponding timer output goes low.

The MCR is a read/write register and is cleared to 0 on reset.

BIT	DESCRIPTION
7	STATUS LED 0 = off 1 = on
6-3	Not used (read as written before)
2	Timer 3 Interrupt Request Enable 0 = disabled 1 = enabled
1	Timer 2 Interrupt Request Enable 0 = disabled 1 = enabled
0	Timer 1 Interrupt Request Enable 0 = disabled 1 = enabled

4.5.22 PI/T 1/2 Peripheral Line Direction Register (PLDR12)

7	6	5	4	3	2	1	0
TOUT1 Direct. Control	TIN1 Direct. Control	TOUT2 Direct. Control	TIN2 Direct. Control	H14/24 Direct. Control	H13/23 Direct. Control	H12/22 Direct. Control	H11/21 Direct. Control

The PI/T 1/2 Peripheral Line Direction Register controls the the peripheral line transceiver direction for the PI/T 1 and PI/T 2 handshake and timer I/O lines. Each bit in the register corresponds to one I/O line. Whereby a 0 determines that the line is used as an input, and a 1 determines it is used as an output.

As opposed to the Port Data Direction Registers, the PLDR1/2 is not accessed in parallel to a PI/T device internal register. Therefore it has to be programmed separately according to the desired operation of the peripheral handshake and timer signals.

The PLDR1/2 is a read/write register and is cleared to 0 on reset.

BIT	DESCRIPTION
7	TOUT1 Direction Control 0 = input 1 = output
6	TIN1 Direction Control 0 = input 1 = output
5	TOUT2 Direction Control 0 = input 1 = output
4	TIN2 Direction Control 0 = input 1 = output
3	H14/24 Direction Control 0 = input 1 = output
2	H13/23 Direction Control 0 = input 1 = output
1	H12/22 Direction Control 0 = input 1 = output
0	H11/21 Direction Control 0 = input 1 = output

4.5.23 PI/T 3 Peripheral Line Direction Register (PLDR3)

7	6	5	4	3	2	1	0
TOUT3 Direct. Control	TIN3 Direct. Control	PC31 Direct. Control	PC30 Direct. Control	H34 Direct. Control	H33 Direct. Control	H32 Direct. Control	H31 Direct. Control

The PI/T 3 Peripheral Line Direction Register controls the peripheral line transceiver direction for the PI/T 3 handshake, timer, and Port C I/O lines. Each bit in the register corresponds to one I/O line. Whereby a 0 determines that the line is used as an input, and a 1 determines it is used as an output.

As opposed to the Port Data Direction Registers, the PLDR3 is not accessed in parallel to a PI/T device internal register. Therefore it has to be programmed separately according to the desired operation of the peripheral handshake, timer and Port C signals.

The PLDR3 is a read/write register and is cleared to 0 on reset.

BIT	DESCRIPTION
7	TOUT3 Direction Control 0 = input 1 = output
6	TIN3 Direction Control 0 = input 1 = output
5	PC31 Direction Control 0 = input 1 = output
4	PC30 Direction Control 0 = input 1 = output
3	H34 Direction Control 0 = input 1 = output
2	H33 Direction Control 0 = input 1 = output
1	H32 Direction Control 0 = input 1 = output
0	H31 Direction Control 0 = input 1 = output

4.5.24 Driver Characteristic Control Register (DCCR)

7	6	5	4	3	2	1	0
PCxx Driver Control	Hxx Driver Control	PB3x Driver Control	PA3x Driver Control	PB2x Driver Control	PA2x Driver Control	PB1x Driver Control	PA1x Driver Control

The Driver Characteristic Control Register defines the electrical output characteristics of the peripheral line transceivers. Each bit in the register controls one group of eight peripheral line drivers and selects either an active pull-up (if the bit is 0) or an open-collector (if the bit is 1) characteristic for each line in the group which is operating as an output. The register does not affect the peripheral line receivers.

For more detailed information about the peripheral line transceivers refer to the MC3448A Data Sheet in Appendix B.

The DCCR is a read/write register and is cleared to 0 on reset.

BIT	DESCRIPTION
7	PC30, PC31, TIN1, TOUT1, TIN2, TOUT2, TIN3, TOUT3 Driver Control 0 = active pull-up 1 = open-collector
6	H11/21, H12/22, H13/23, H14/24, H31, H32, H33, H34 Driver Control 0 = active pull-up 1 = open-collector
5	PB30..PB37 Driver Control 0 = active pull-up 1 = open-collector
4	PA30..PA37 Driver Control 0 = active pull-up 1 = open-collector
3	PB20..PB27 Driver Control 0 = active pull-up 1 = open-collector
2	PA20..PA27 Driver Control 0 = active pull-up 1 = open-collector
1	PB10..PB17 Driver Control 0 = active pull-up 1 = open-collector
0	PA10..PA17 Driver Control 0 = active pull-up 1 = open-collector

4.6 PROGRAMMING CONSIDERATIONS

This section provides the user with information on programming considerations. The following programs are not "ready-to-use" routines. They might however, assist the user in writing his own driver software.

The general structure of an interrupt driven device driver might consist of the following routines:

- initialization procedure
- issue command procedure
- interrupt service routine
- termination procedure

4.6.1 Initialization Procedure

The initialization procedure has to be called before any I/O operation is issued. Normally this procedure is executed after power up or during execution of an "attach" command.

For the MVME340 a basic initialization procedure could look like the following example:

```
procedure INIT_MVME340
  reserve memory for variables and data
    initialize variables which are used later
      set data direction
        load interrupt vectors
      load interrupt levels
    set handshake lines data direction
  enable interrupts
end
```

4.6.2 Issue Command Procedure

The issue command procedure performs the actual I/O and status passing to or from the MVME340. Typical commands are write data, read data, get status, and put status.

The basic structure of a WRITE_DATA procedure is given in the following example. A READ_DATA procedure has a similar format except the data direction is set to the opposite.

```
procedure WRITE_DATA
  while not end of data
    begin
      put next data into output registers
       wait until data has been accepted
      process status information returned
    end
end
```

4.6.3 Interrupt Service Routine

The interrupt service routine can be seen as part of a WRITE_DATA or READ_DATA command procedure.

In the above example the statement "wait until data has been accepted" means that the current data output is suspended and another part of the program is being executed at the present time. An interrupt request generated by a handshake line causes that execution of the WRITE_DATA routine is resumed. The interrupt service routine might look like the following:

```
WRITE_DATA interrupt service routine
  read status
    pass status to operating system
  return from interrupt
end
```

4.6.4 Termination Procedure

The termination procedure is normally called during execution of a "detach" command or during a power down sequence. The I/O lines data direction is changed to input so that they cannot disturb the actual I/O hardware. The termination procedure might look like the following:

```
procedure TERM_MVME340
  if any I/O activities
    then wait
      disable interrupts
    set data direction to input
  return memory to operating system
end
```

CHAPTER 5

MAINTENANCE INFORMATION

5.1. INTRODUCTION

This chapter provides parts list, assembly drawing and schematic diagrams for the MVME340 Parallel Interface/Timer Module.

5.2. PARTS LIST

Table 5.1 reflects the latest issue of hardware for the MVME340 module at the time of printing. All parts are identified by quantity, designation on the board, Motorola part number, and a short part description. The part locations are shown in Figure 5.1.

Table 5.1: MVME340 Parts List

QU	DESIGNATION	PART NUMBER	DESCRIPTION
32	C2-C33	21NW9702A09	0.1 uF, 50 V Ceramic Capacitor
1	C1	23NW9618A74	47uF, 10 V Electrolytic Capacitor
2	DL1,DL2	01NG9804A05	3*30 ns Triple Delay Line
1	K6	28NW9802D01	Header Single Row 1*2 Pins
1	K1	28NW9802C29	Header Double Row 2*2 Pins
4	K2-K5	28NW9802B34	Header Double Row 2*8 Pins
1	LD1	48NW9612A34	Light Emitting Diode Red
2	P1,P2	28-G9802M03	DIN 41612 C 96 Male Connector
1	R1	29NW9805B98	0 ohm Dummy Resistor
1	RP20	51NW9626A47	7*4.7 kohm, 5 % SIL Resistor Network
8	RP10,RP12, RP14-RP19	51NW9626B41	9*1.2 kohm, 5% SIL Resistor Network
3	RP9,RP11, RP13	51NW9626A41	9*4.7 kohm, 5% SIL Resistor Network
1	U4	51-G5021M03	AM27S33APC 1024*4 PROM (programmed)
6	U17,U34,U50, U51,U60,U71	51NW9615G01	AM2920PC 8-Bit Register
3	U80,U84,U86	51NG9615A14	AM2952PC Bidirectional 8-Bit Register
1	U85	51NG9615A15	AM2953PC Bidirectional 8-Bit Register
16	U9-U16, U26-U33	51NG9615A16	MC3448AP Quad IEEE 488 Transceiver
3	U57,U58,U59	51NG9615A11	MC68230L8 Parallel Interface/Timer
3	U23-U25	51-G5022M01	PAL16L8CN PAL (programmed)
1	U77	51-G5022M02	PAL16L8CN PAL (programmed)
1	U78	51-G5022M03	PAL16L8CN PAL (programmed)
1	U79	51-G5023M01	PAL20L10CN PAL (programmed)
1	U82	51-G5023M02	PAL20L10CN PAL (programmed)
1	U83	51-G5023M03	PAL20L10CN PAL (programmed)
2	U61,U76	51NG9615A05	SN74AS74N Dual D-Flip-Flop

Table 5.1: MVME340 Parts List (continued)

QU	DESIGNATION	PART NUMBER	DESCRIPTION
2	U64,U72	51NW9615E91	SN74LS00N Quad 2-Input NAND Gate
2	U55,U68	51NW9615C21	SN74LS04N Hex Inverter
2	U69,U75	51NW9615C22	SN74LS08N Quad 2-Input AND Gate
1	U62	51NW9615F05	SN74LS20N Dual 4-Input NAND Gate
2	U53,U66	51NW9615C25	SN74LS74AN Dual D-Flip-Flop
5	U37,U44,U49, U63,U74	51NW9615N09	SN74LS113AN Dual J-K-Flip-Flop
1	U56	51NW9615F10	SN74LS125AN Quad Line Driver
3	U36,U38,U39	51NW9615C69	SN74LS138N 3-Bit Decoder
3	U35,U40,U45	51NW9615D33	SN74LS173AN 4-Bit D-Register
3	U42,U47,U54	51NW9615F09	SN74LS266N Quad EXOR-Gate
2	U41,U52	51NW9615J50	SN74LS367AN Hex Line Driver
2	U67,U70	51NW9615G12	SN74LS375N Dual 2-Bit D-Latch
2	U46,U73	51NG9615A19	SN74LS396N 8-Bit Register
4	U2,U3,U18, U22	51NG9615A20	SN74LS541N Octal Bus Driver
3	U19-U21	51NW9615H83	SN74LS641-1N Octal Bus Driver OC
2	U1,U5	51NW9615H89	SN74LS645-1N Octal Bus Driver TS
3	U6-U8	51NW9615N77	SN74LS688N 8-Bit Comparator
1	U81	51NW9615C96	SN74S04N Hex Inverter
1	U43	51NW9615C56	SN74S08N Quad 2-Input AND Gate
1	U65	51NW9615D93	SN74S30N 8-Input NAND Gate
1	U48	51NW9615E67	SN74S260N Dual 5-Input NOR Gate
1	at Y1	09NW9811A46	4-Pin Oscillator Socket
1	at U4	09NW9811A09	18-Pin DIL IC Socket
5	at U23-U25, U77,U78	09NW9811A27	20-Pin DIL IC Socket
3	at U79,U82, U83	09NG9811A03	24-Pin DIL IC Socket
3	at U57-U59	09NG9811A04	48-Pin DIL IC Socket
7	at P1,P2, Front Panel	03SW993D210	DIN 84 M 2.5*10 Flat Head Screw
7	at P1,P2, Front Panel	02SW990D001	DIN 934 M 2.5 Hexagonal Nut
35		29NW9805B17	Jumper Shorting Insulated
1		84-G8026M01	MVME340 Printed Circuit Board
1		64-G4166M01	MVME340 Front Panel
1		07-G4169M01	Interface Connector Assembly

5.3 ASSEMBLY DRAWING, SCHEMATIC DIAGRAMS

Figure 5.1 is the assembly drawing, Figures 5.2 to 5.12 are the schematic diagrams of the MVME340 Parallel Interface/Timer Module.

Figure 5.1: MVME340 Assembly Drawing

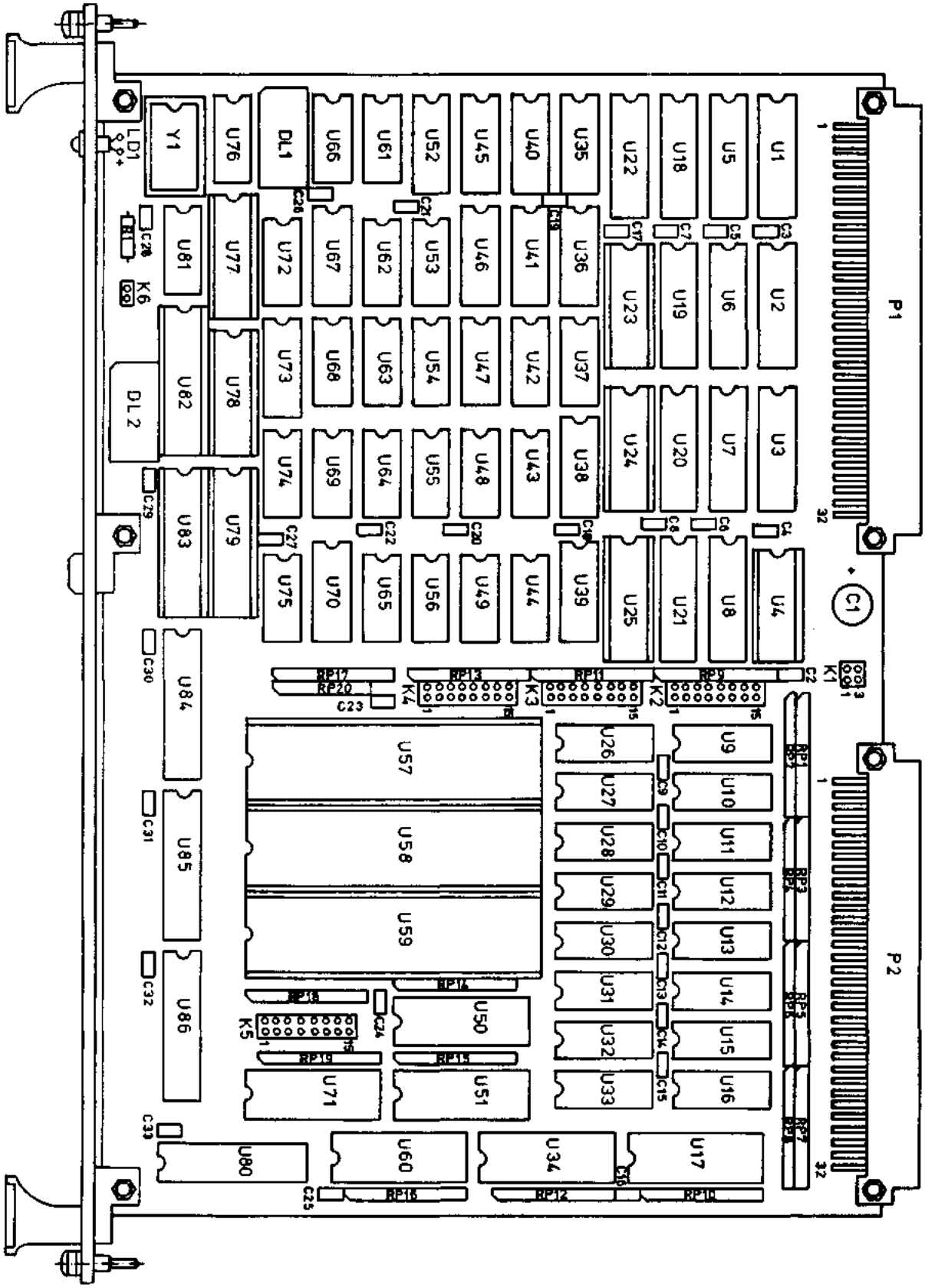
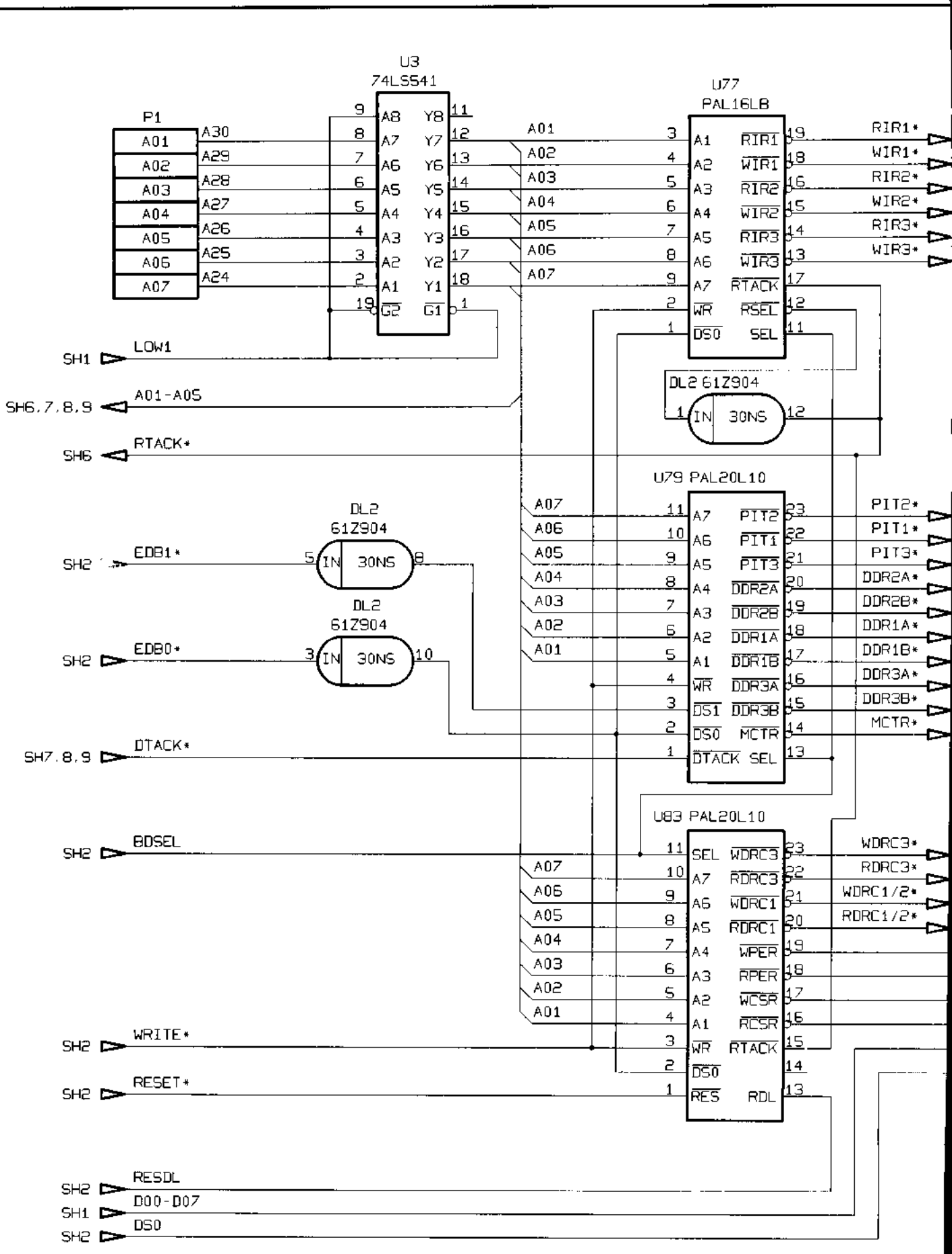
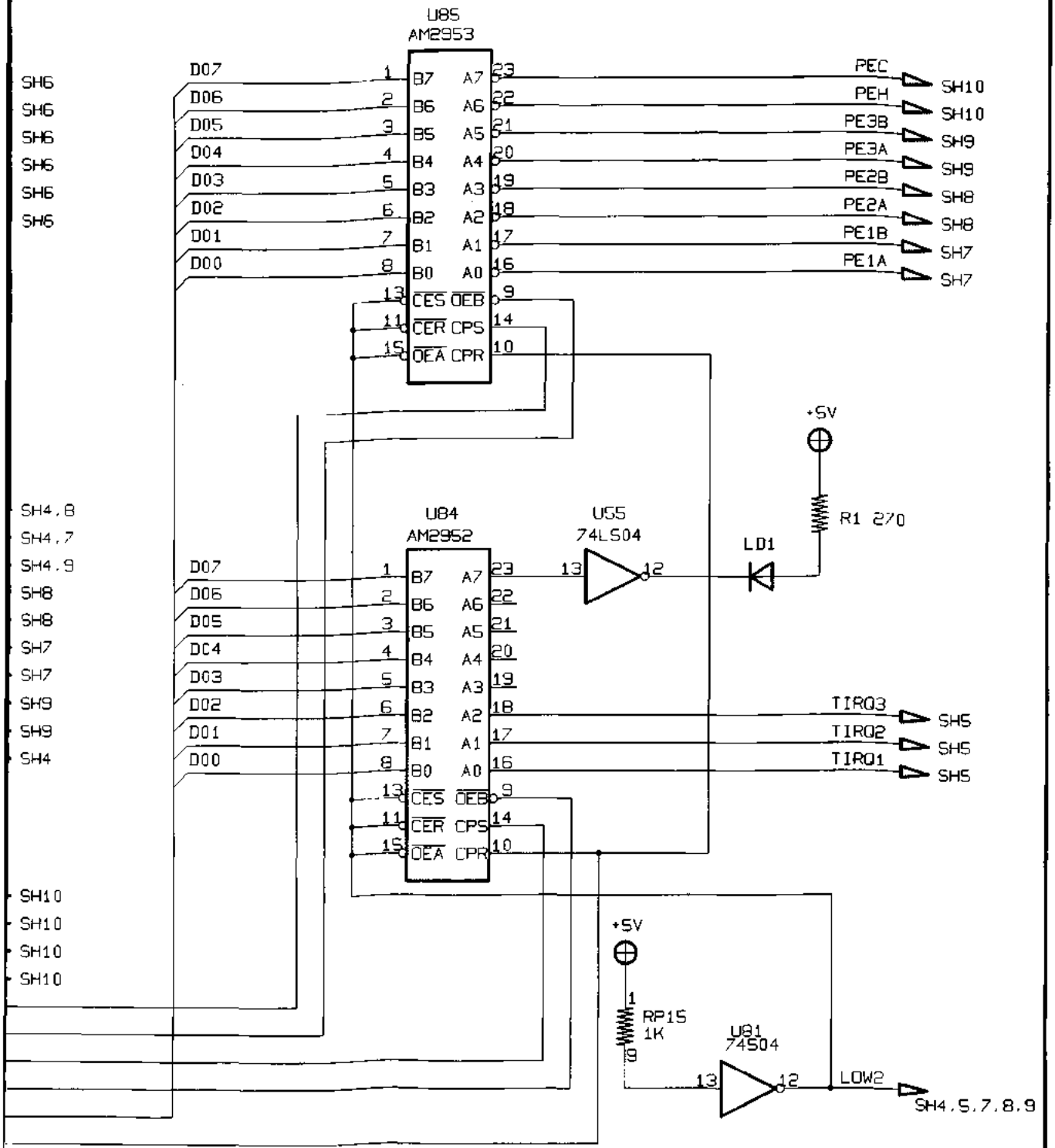


Figure 5.4: MVME340 Schematic Diagram Sheet 3/11





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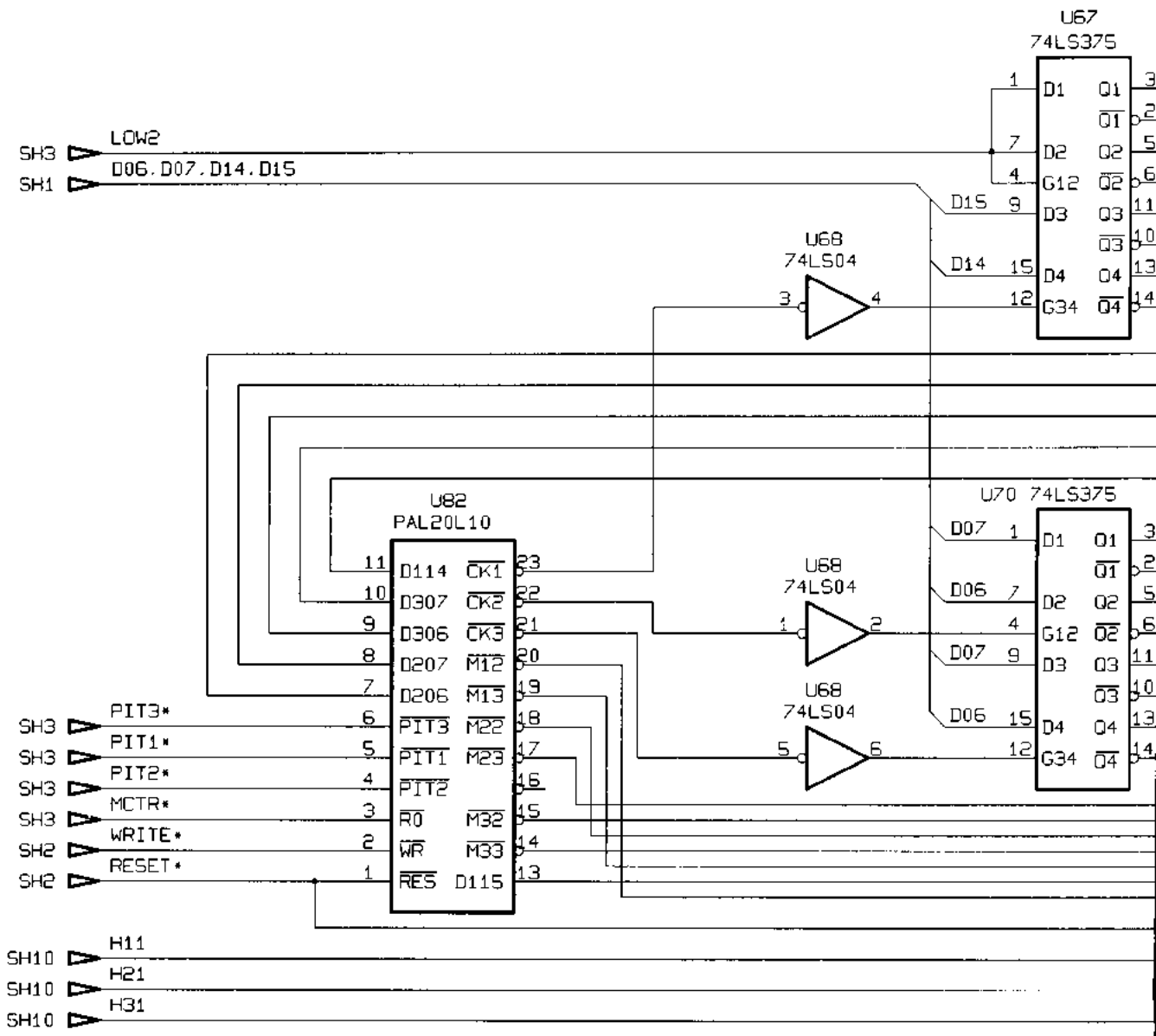
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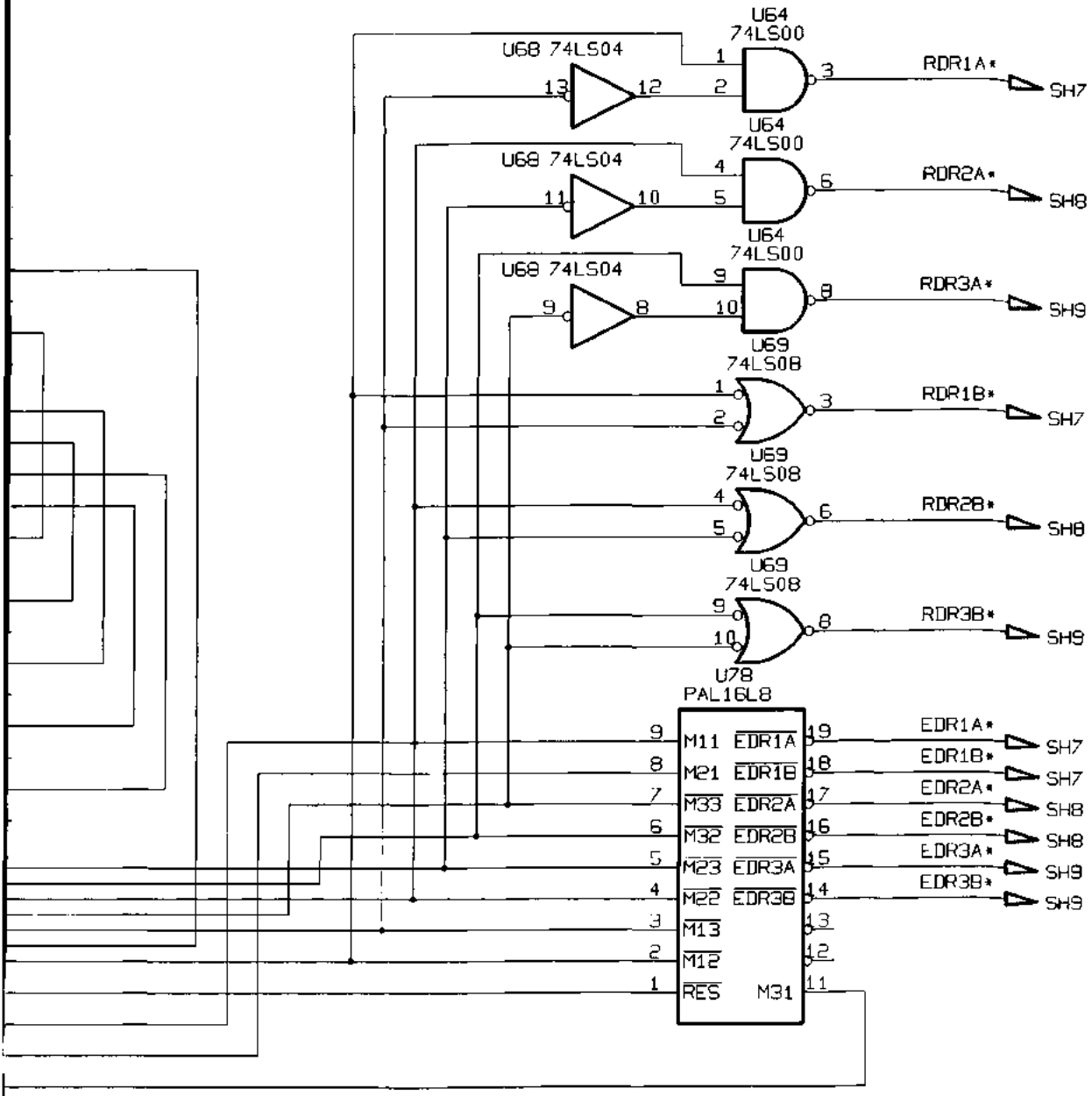
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Figure 5.5: MVME340 Schematic Diagram Sheet 4/11





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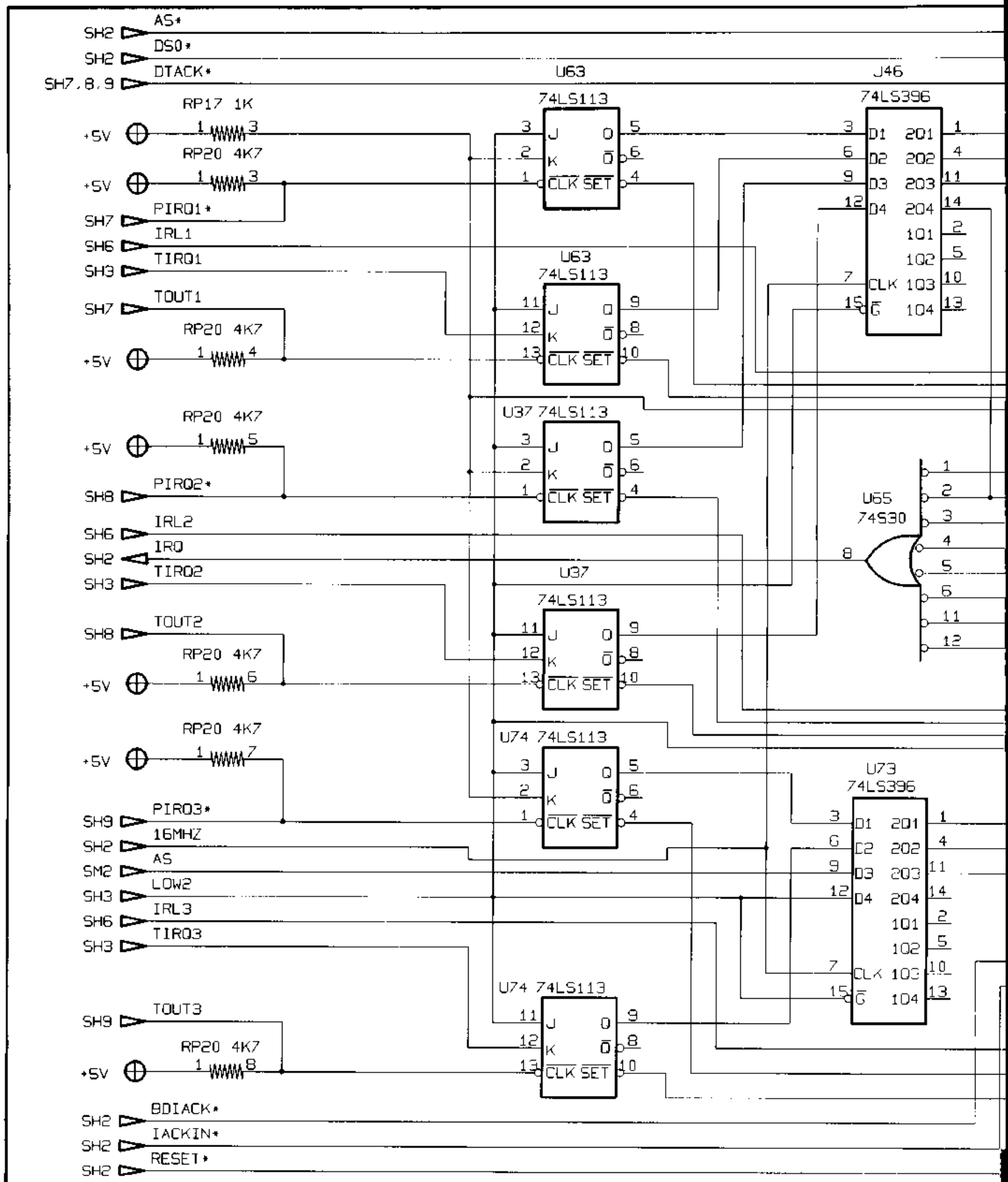
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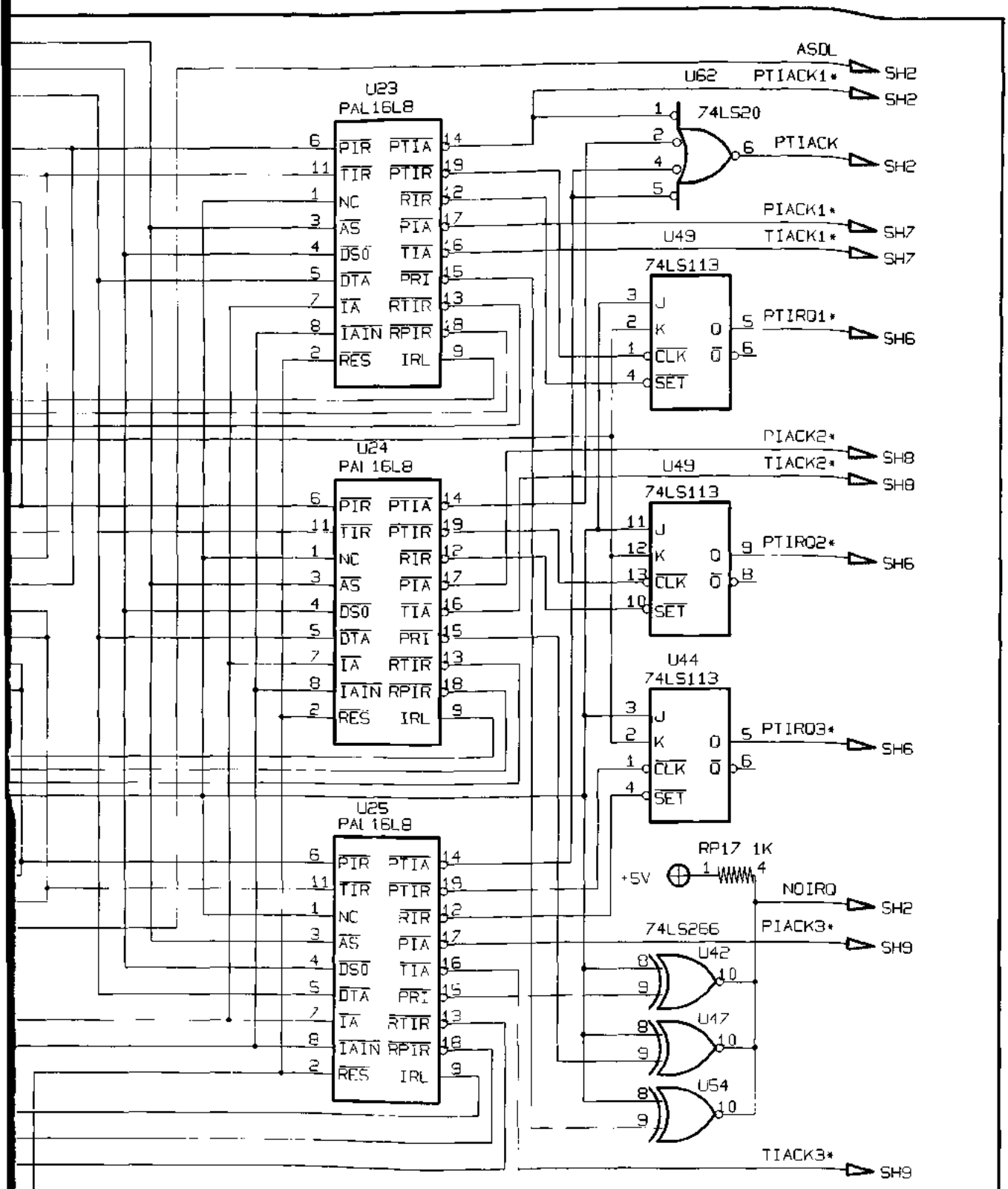
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Figure 5.6: MVME340 Schematic Diagram Sheet 5/11





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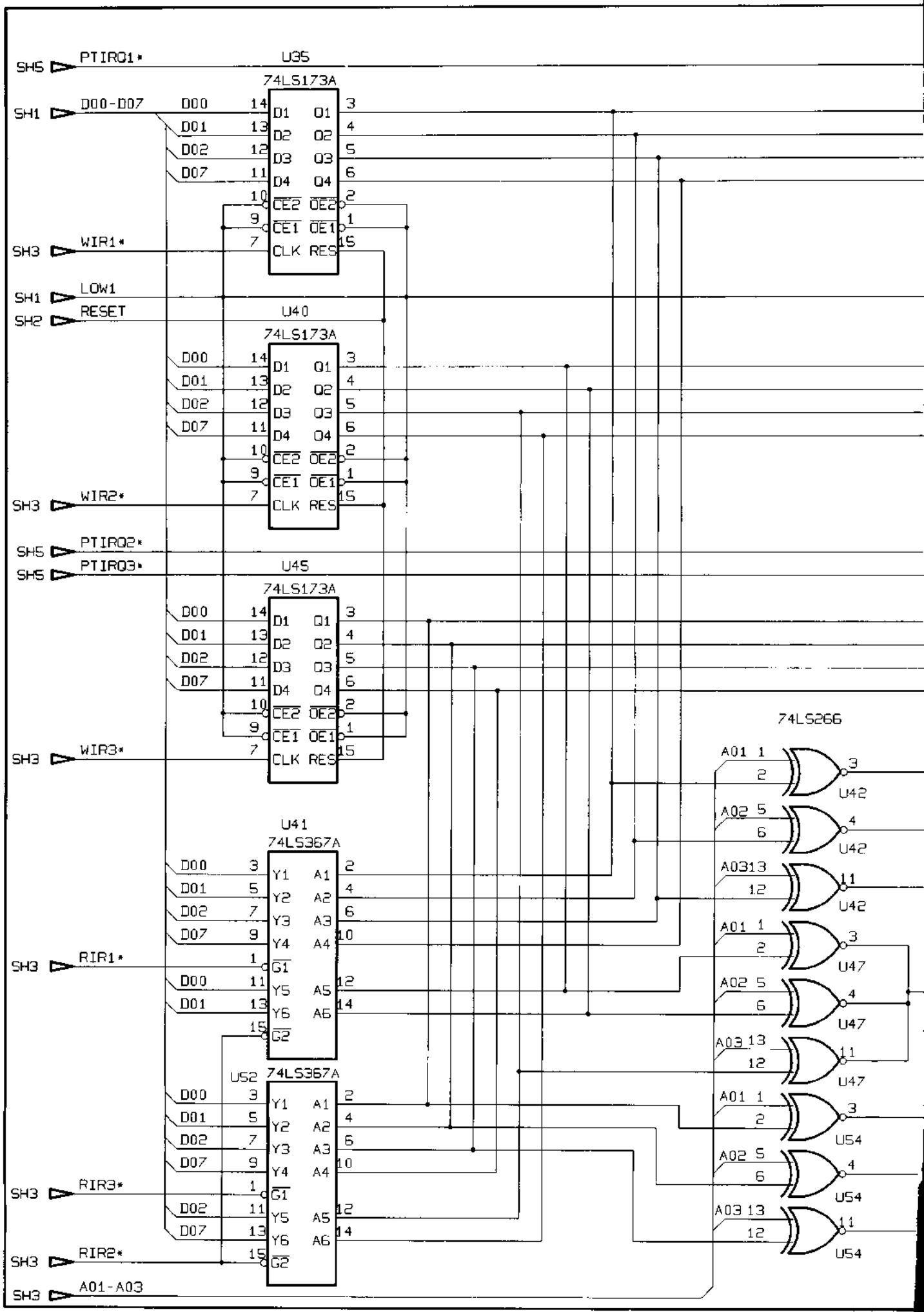
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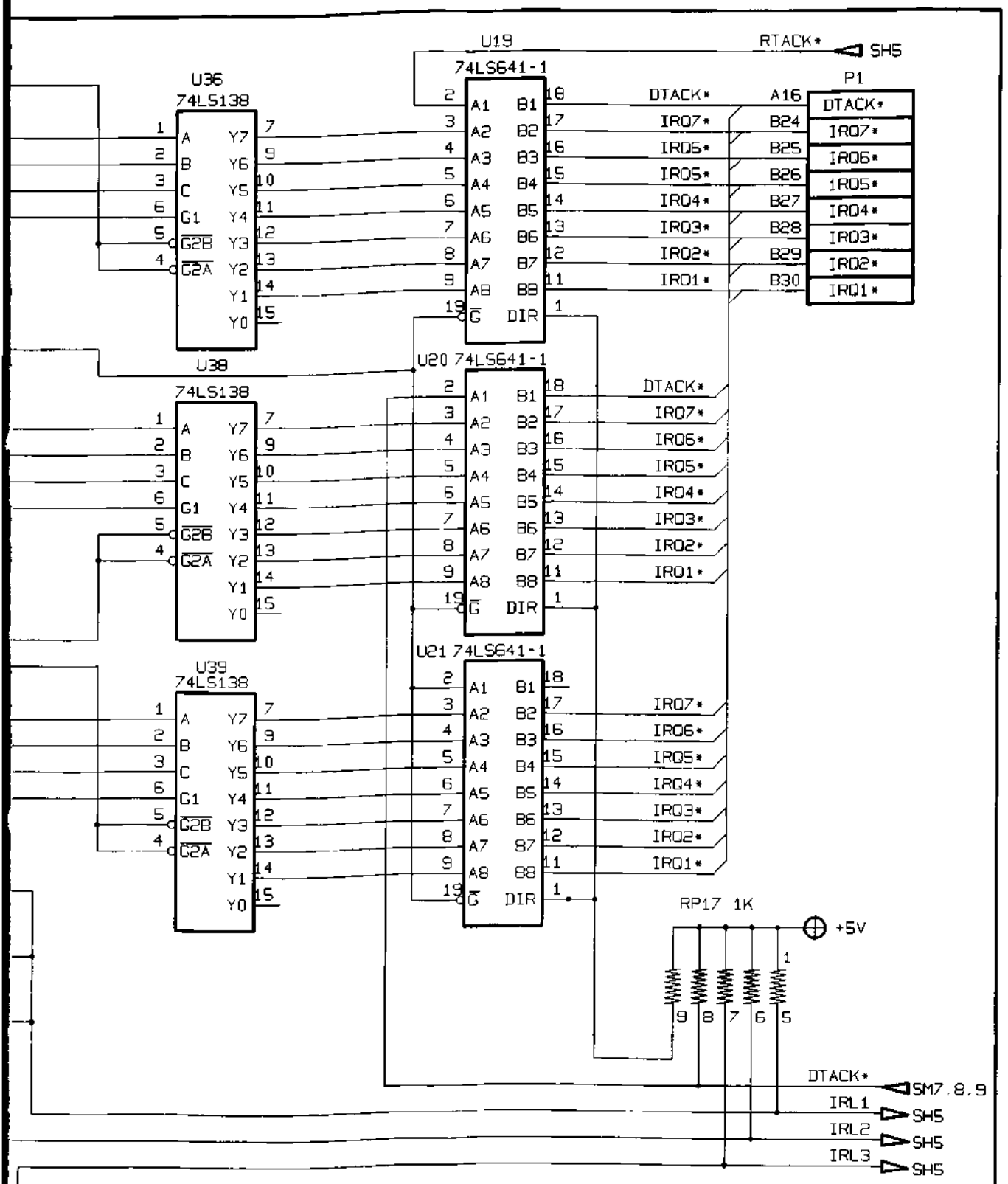
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Figure 5.7: MVME340 Schematic Diagram Sheet 6/11





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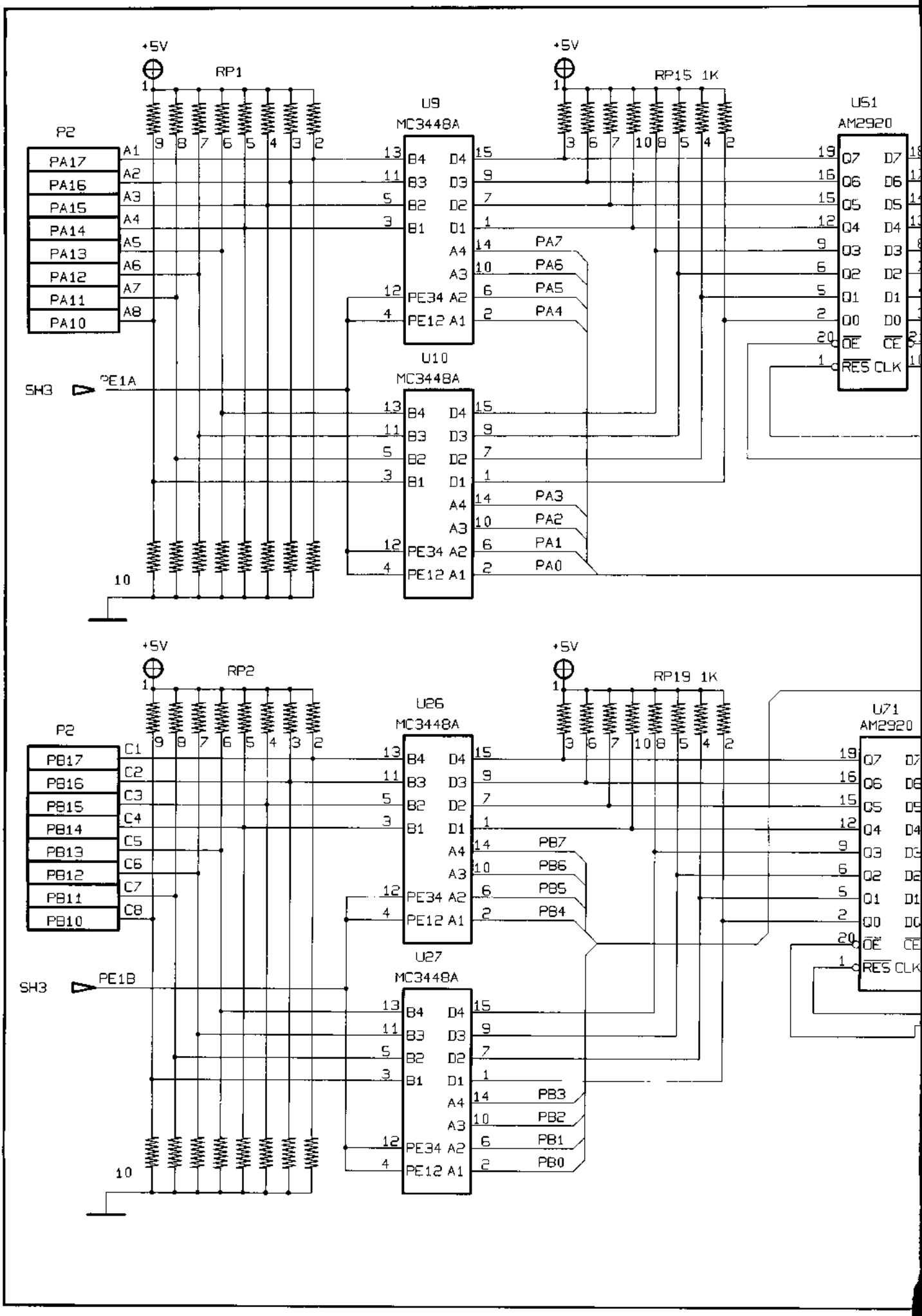
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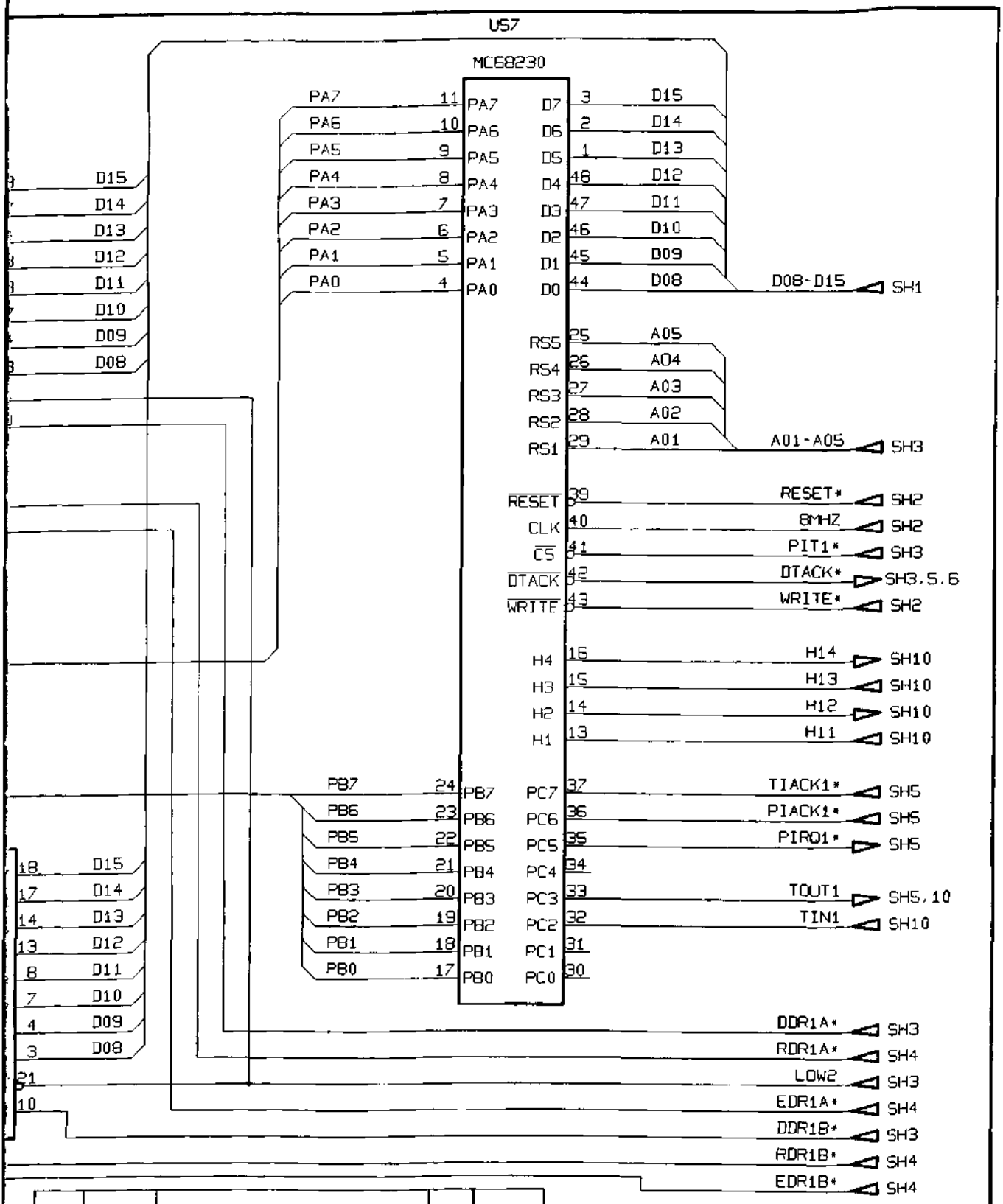
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Figure 5.8: MVME340 Schematic Diagram Sheet 7/11





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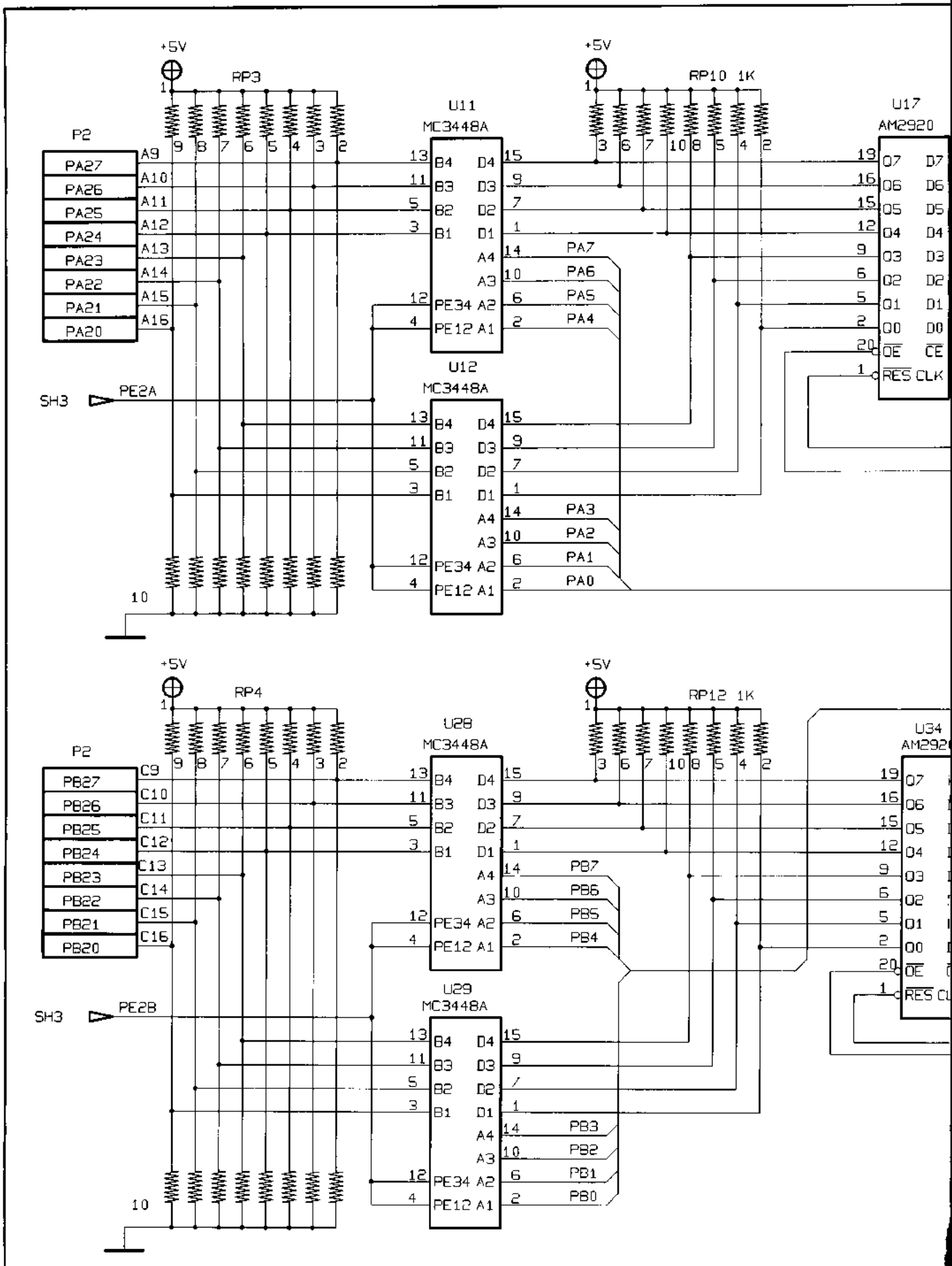
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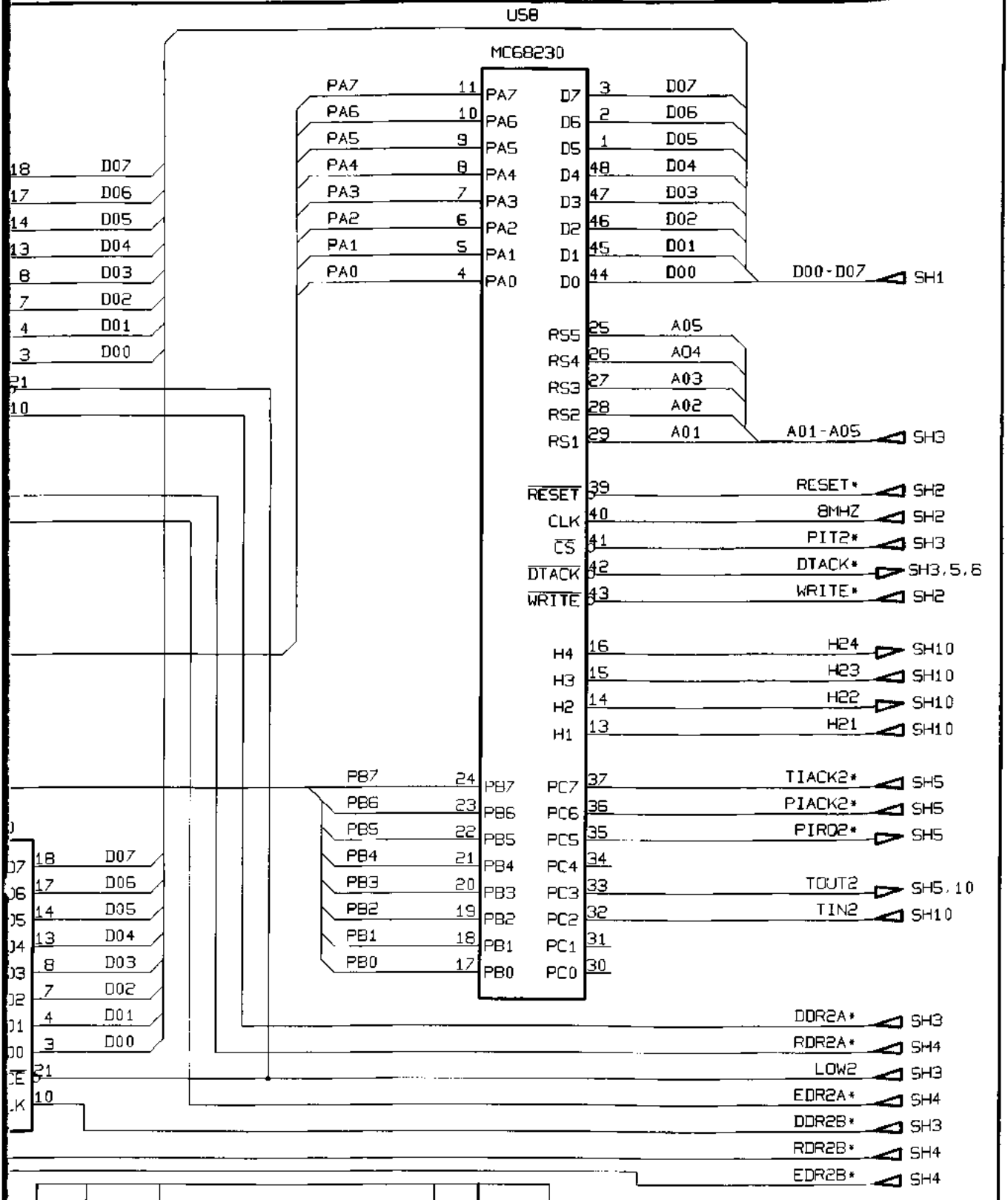
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Figure 5.9: MVME340 Schematic Diagram Sheet 8/11





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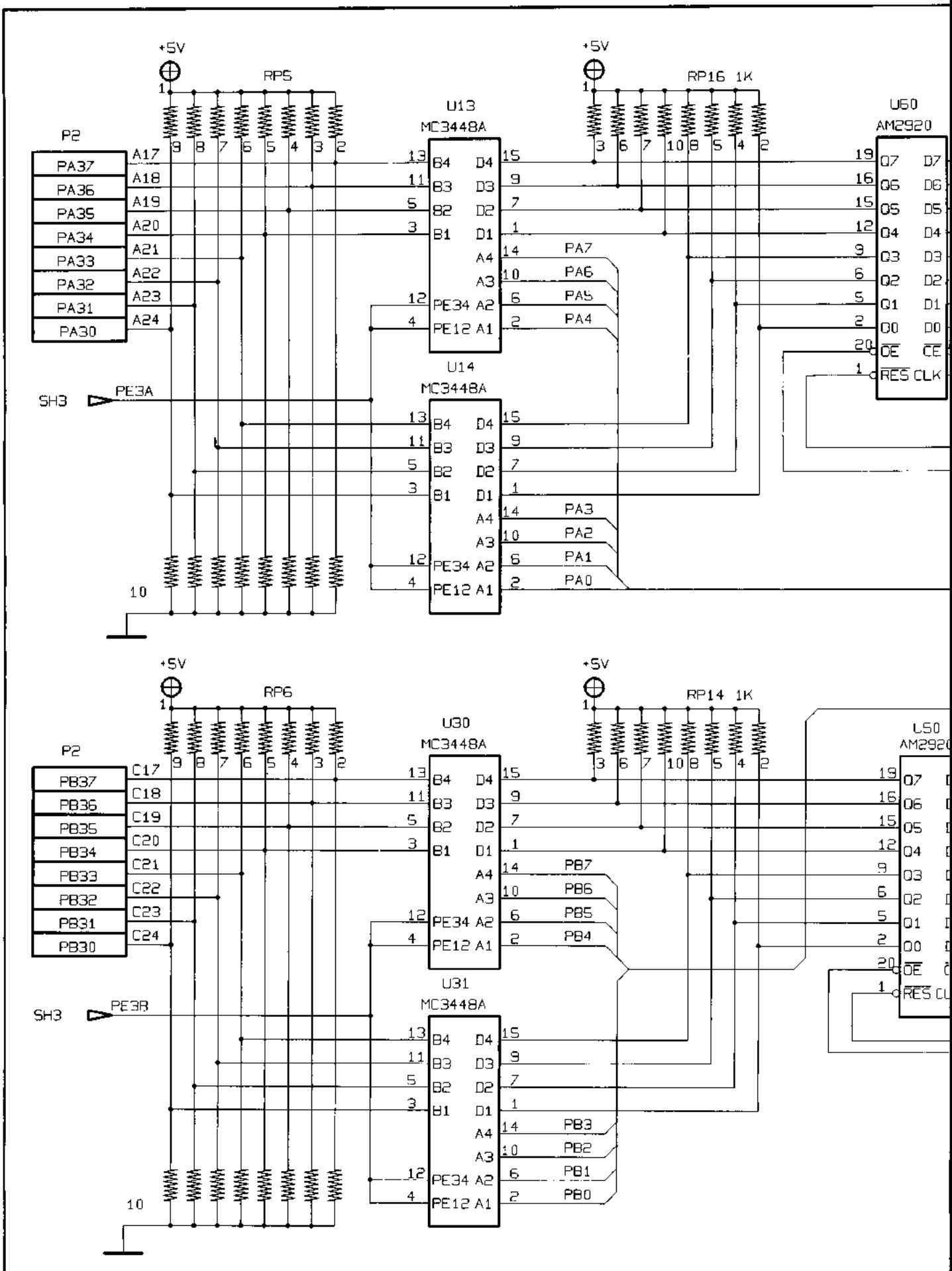
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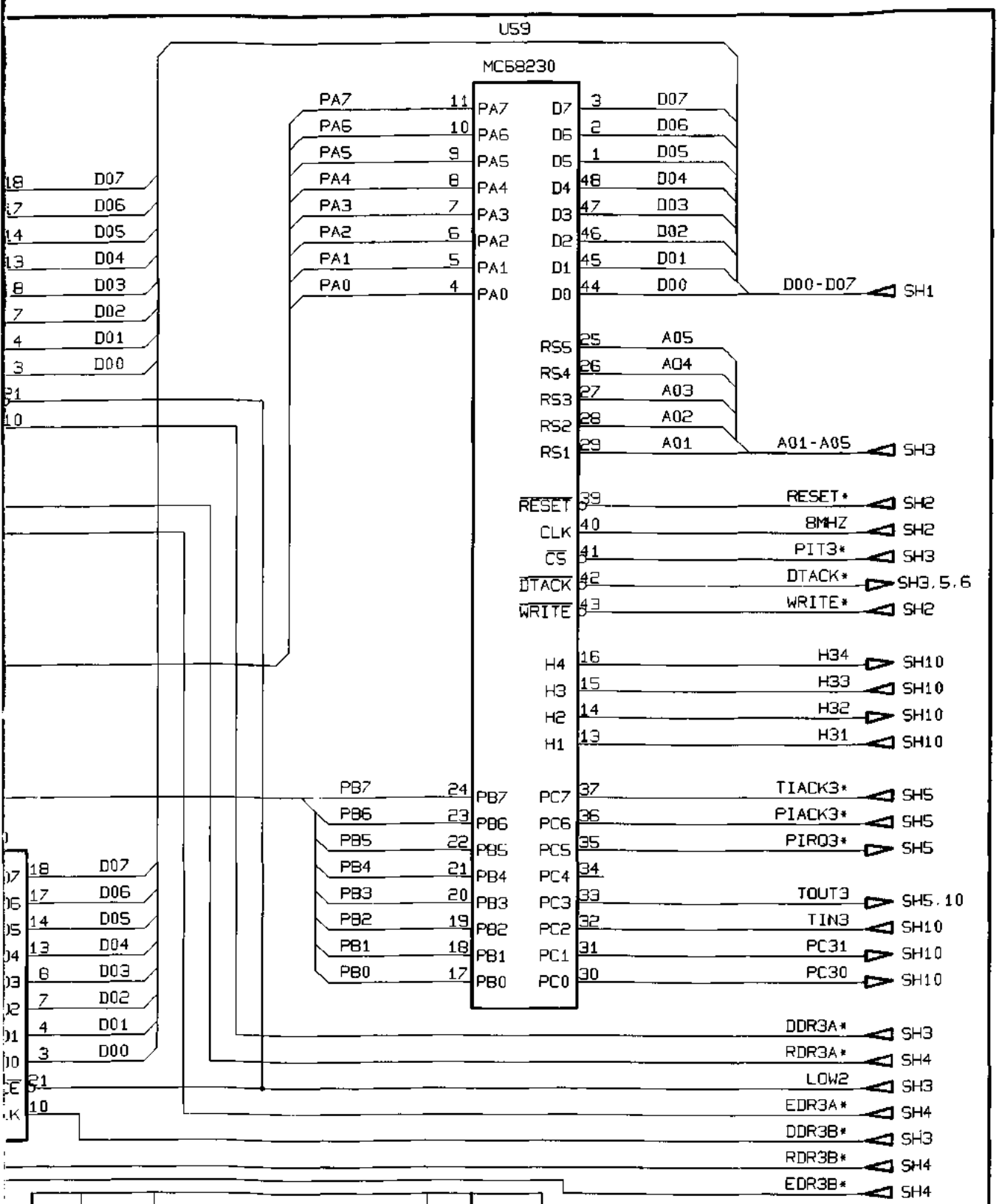
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Figure 5.10: MVME340 Schematic Diagram Sheet 9/11





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DRAWING NO:
63BG3026M01

SHEET: 9
OF: 11

APPENDIX A

MC68230 Parallel Interface/Timer Data Sheet

TABLE OF CONTENTS

Paragraph Number	Title	Page Number
	Section 1 Introduction	
1.1	Port Mode Description	1-2
1.2	Signal Description	1-5
1.2.1	Bidirectional Data Bus (D0-D7)	1-5
1.2.2	Register Selects (RS1-RS5)	1-5
1.2.3	Read/Write (R/$\overline{W}$)	1-6
1.2.4	Chip Select ($\overline{CS}$)	1-6
1.2.5	Data Transfer Acknowledge ($\overline{DTACK}$)	1-7
1.2.6	Reset ($\overline{RESET}$)	1-7
1.2.7	Clock (CLK)	1-7
1.2.8	Port A and Port B (PA0-PA7 and PB0-PB7)	1-7
1.2.9	Handshake Pins (H1-H4)	1-7
1.2.10	Port C (PC0-PC7/Alternate Function)	1-7
1.3	Register Model	1-8
1.4	Bus Interface Operation	1-10
1.4.1	Read Cycles	1-10
1.4.2	Interrupt Acknowledge Cycles	1-11
1.4.3	Write Cycles	1-11
	Section 2 Port General Information and Conventions	
2.1	Unidirectional vs Bidirectional	2-1
2.1.1	Control of Double-Buffered Data Paths	2-1
2.1.2	Double-Buffered Input Transfers	2-2
2.1.3	Double-Buffered Output Transfers	2-2
2.2	Requesting Bus Master Service	2-4
2.2.1	Vectored, Prioritized Port Interrupts	2-5
2.2.2	Autovectored Port Interrupts	2-5
2.2.3	DMA Request Operation	2-6
2.3	Direct Method of Resetting Status	2-6
2.4	Handshake Pin Sense Control	2-7
2.5	Enabling Ports A and B	2-7
2.6	Port A and B Alternate Registers	2-7

TABLE OF CONTENTS
(Continued)

Paragraph Number	Title	Page Number
	Section 3 **Port Modes**	
3.1	Port A Control Register	3-1
3.2	Port B Control Register	3-1
3.3	Mode 0 — Unidirectional 8-Bit Mode	3-2
3.3.1	Submode 00 — Pin-Definable Double-Buffered Input or Single-Buffered Output	3-2
3.3.2	Submode 01 — Pin-Definable Double-Buffered Output or Non-Latched Input	3-4
3.3.3	Submode 1X — Bit I/O (Pin-Definable Single-Buffered Output or Non-Latched Input)	3-6
3.4	Mode 1 — Unidirectional 16-Bit Mode	3-8
3.4.1	Port A Control Register	3-9
3.4.2	Port B Control Register	3-9
3.4.3	Submode X0 — Pin-Definable Double-Buffered Input or Single-Buffered Output	3-9
3.4.4	Submode X1 — Pin-Definable Double-Buffered Output or Non-Latched Input	3-12
3.5	Mode 2 — Bidirectional 8-Bit Mode	3-14
3.5.1	Port A Bit I/O (Pin-Definable Single-Buffered Output or Non-Latched Input)	3-14
3.5.2	Port B Double-Buffered I/O	3-14
3.5.2.1	Double-Buffered Input Transfers	3-15
3.5.2.2	Double-Buffered Output Transfers	3-15
3.6	Mode 3 — Bidirectional 16-Bit Mode	3-17
3.6.1	Double-Buffered Input Transfers	3-17
3.6.2	Double-Buffered Output Transfers	3-18
	Section 4 **Programmer's Model**	
4.1	Port General Control Register (PGCR)	4-2
4.2	Port Service Request Register (PSRR)	4-3
4.3	Port Data Direction Registers	4-4
4.3.1	Port A Data Direction Register (PADDR)	4-4
4.3.2	Port B Data Direction Register (PBDDR)	4-4
4.3.3	Port C Data Direction Register (PCDDR)	4-4
4.4	Port Interrupt Vector Register (PIVR)	4-4
4.5	Port Control Registers (PACR, PBCR)	4-4
4.6	Port Data Registers	4-5
4.6.1	Port A Data Register (PADR)	4-5
4.6.2	Port B Data Register (PBDR)	4-5
4.6.3	Port C Data Register (PCDR)	4-5

TABLE OF CONTENTS
(Concluded)

Paragraph Number	Title	Page Number
4.7	Port Alternate Registers	4-6
4.7.1	Port A Alternate Register (PAAR)	4-6
4.7.2	Port B Alternate Register (PBAR)	4-6
4.8	Port State Register (PSR)	4-6
4.9	Timer Control Register (TCR)	4-6
4.10	Timer Interrupt Vector Register (TIVR)	4-8
4.11	Counter Preload Register H, M, L (CPRH-L)	4-8
4.12	Count Register H, M, L (CNTRH-L)	4-8
4.13	Timer Status Register (TSR)	4-8
4.14	Register Value After Reset	4-9
	Section 5	
	Timer Operation and Applications Summary	
5.1	Timer Operation	5-1
5.1.1	Run/Halt Definition	5-1
5.1.2	Timer Rules	5-2
5.1.3	Timer Interrupt Acknowledge Cycles	5-2
5.2	Timer Applications Summary	5-2
5.2.1	Periodic Interrupt Generator Example	5-3
5.2.2	Square Wave Generator	5-3
5.2.3	Interrupt After Timeout	5-4
5.2.4	Elapsed Time Measurement Examples	5-5
5.2.4.1	System Clock Example	5-5
5.2.4.2	External Clock	5-6
5.2.5	Device Watchdog	5-6
	Section 6	
	Electrical Specifications	
6.1	Maximum Ratings	6-1
6.2	Thermal Characteristics	6-1
6.3	Power Considerations	6-1
6.4	DC Electrical Characteristics	6-2
6.5	AC Electrical Specifications — Clock Timing	6-3
6.6	AC Electrical Specifications	6-4
	Section 7	
	Mechanical Data and Ordering Information	
7.1	Pin Assignment	7-1
7.2	Ordering Information	7-2
7.3	Package Dimensions	7-2

LIST OF ILLUSTRATIONS

Figure Number	Title	Page Number
1-1	Block Diagram	1-2
1-2	Port Mode Layout	1-4
1-3	Logical Pin Assignment	1-6
2-1	Double-Buffered Input Transfers Timing Diagram	2-3
2-2	Double-Buffered Output Transfers Timing Diagram	2-4
2-3	$\overline{\text{DMAREQ}}$ Associated with Output Transfers	2-6
2-4	$\overline{\text{DMAREQ}}$ Associated with Input Transfers	2-6
5-1	Periodic Interrupt Generator Example	5-3
5-2	Square Wave Generator Example	5-4
5-3	Single Interrupt After Timeout Example	5-5
5-4	Elapsed Time Measurement Example	5-6
5-5	Device Watchdog Example	5-7
6-1	Clock Input Timing Diagram	6-3
6-2	Read Cycle Timing Diagram	Foldout 3
6-3	Write Cycle Timing Diagram	Foldout 3
6-4	IACK Timing Diagram	Foldout 4
6-5	Peripheral Input Timing Diagram	Foldouts 5 and 6
6-6	Peripheral Output Timing Diagram	Foldouts 5 and 6

LIST OF TABLES

Table Number	Title	Page Number
1-1	Port Mode Control Summary	1-3
1-2	Signal Summary	1-6
1-3	Register Model	1-8
2-1	Response to Port Interrupt Acknowledge	2-5
3-1	Mode 0 Port Data Paths	3-2
3-2	Mode 1 Port Data Paths	3-8
3-3	Mode 2 Port A Data Paths	3-14
3-4	Mode 2 Port B Data Paths	3-16
3-5	Mode 3 Port A and B Data Paths	3-18
4-1	PI/T Register Addressing Assignments	4-1
4-2	PSRR Port Interrupt Priority Control	4-3
4-3	PCDR Hardware Accesses	4-5
5-1	Response to Timer Interrupt Acknowledge	5-2

SECTION 1
INTRODUCTION

The MC68230 parallel interface/timer (PI/T) provides versatile double buffered parallel interfaces and a system oriented timer for M68000 systems. The parallel interfaces operate in unidirectional or bidirectional modes, either 8 or 16 bits wide. In the unidirectional modes, an associated data direction register determines whether each port pin is an input or output. In the bidirectional modes the data direction registers are ignored and the direction is determined dynamically by the state of four handshake pins. These programmable handshake pins provide an interface flexible enough for connection to a wide variety of low, medium, or high speed peripherals or other computer systems. The PI/T ports allow use of vectored or autovectored interrupts, and also provide a DMA request pin for connection to the MC68450 direct memory access controller (DMAC) or a similar circuit. The PI/T timer contains a 24-bit wide counter and a 5-bit prescaler. The timer may be clocked by the system clock (PI/T CLK pin) or by an external clock (TIN pin), and a 5-bit prescaler can be used. It can generate periodic interrupts, a square wave, or a single interrupt after a programmed time period. It can also be used for elapsed time measurement or as a device watchdog.

Features of the PI/T include:

- M68000 Bus Compatible
- Port Modes Include:
  - Bit I/O
  - Unidirectional 8 Bit and 16 Bit
  - Bidirectional 8 Bit and 16 Bit
- Programmable Handshaking Options
- 24-Bit Programmable Timer Modes
- Five Separate Interrupt Vectors
- Separate Port and Timer Interrupt Service Requests
- Registers are Read/Write and Directly Addressable
- Registers are Addressed for MOVEP (Move Peripheral) and DMAC Compatibility

The PI/T consists of two logically independent sections: the ports and the timer. The port section consists of port A (PA0-PA7), port B (PB0-PB7), four handshake pins (H1, H2, H3, and H4), two general input/output (I/O) pins, and six dual-function pins. The dual-function pins can individually operate as a third port (port C) or an alternate function related to either port A, port B, or the timer. The four programmable handshake pins, depending on the mode, can control data transfer to and from the ports, or can be used as interrupt generating inputs or I/O pins. Refer to Figure 1-1.

The timer consists of a 24-bit counter, optionally clocked by a 5-bit prescaler. Three pins provide complete timer I/O: PC2/TIN, PC3/TOUT, and PC7/$\overline{\text{TIACK}}$. Only the ones needed for the given configuration perform the timer function, while the others remain port C I/O.

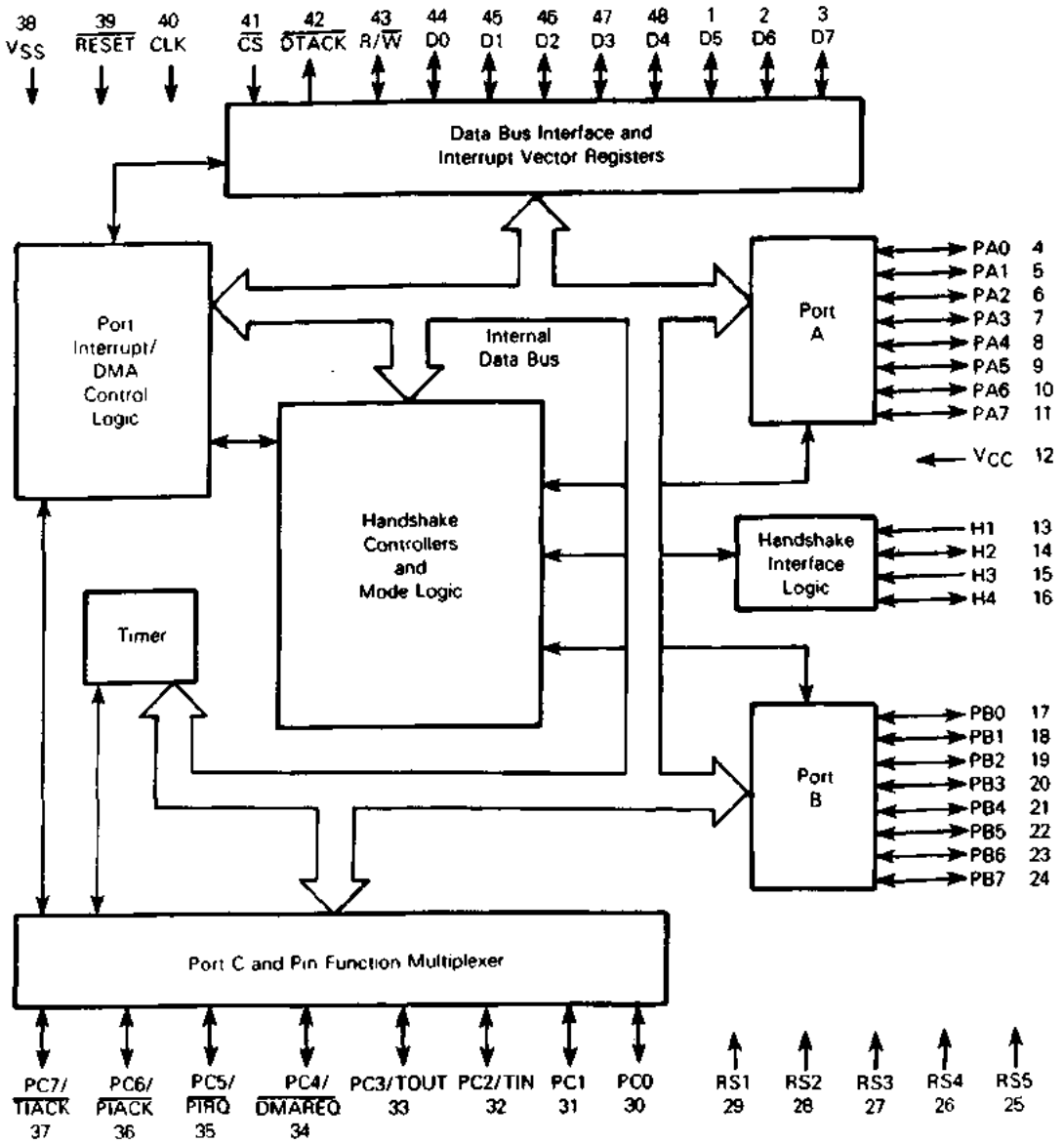


Figure 1-1. Block Diagram

The system bus interface provides for asynchronous transfer of data from the PI/T to a bus master over the data bus (D0-D7). Data transfer acknowledge ($\overline{DTACK}$), register selects (RS1-RS5), timer interrupt acknowledge ($\overline{TIACK}$), read/write line (R/$\overline{W}$), chip select ($\overline{CS}$), or port interrupt acknowledge ($\overline{PIACK}$) control data transfer between the PI/T and an M68000.

1.1 PORT MODE DESCRIPTION

The primary focus of most applications will be on port A, port B, the handshake pins, the port interrupt pins, and the DMA request pin. They are controlled in the following way: the port general control register contains a 2-bit field that specifies one of four operation modes. These govern the

overall operation of the ports and determine their interrelationships. Some modes require additional information from each port's control register to further define its operation. In each port control register, there is a 2-bit submode field that serves this purpose. Each port mode/submode combination specifies a set of programmable characteristics that fully define the behavior of that port and two of the handshake pins. This structure is summarized in Table 1-1 and Figure 1-2.

Table 1-1. Port Mode Control Summary

Mode 0 (Unidirectional 8-Bit Mode)
- Port A
  - Submode 00 – Pin-Definable Double-Buffered Input or Single-Buffered Output
    - H1 – Latches input data
    - H2 – Status/interrupt generating input, general-purpose output, or operation with H1 in the interlocked or pulsed handshake protocols
  - Submode 01 – Pin-Definable Double-Buffered Output or Non-Latched Input
    - H1 – Indicates data received by peripheral
    - H2 – Status/interrupt generating input, general-purpose output, or operation with H1 in the interlocked or pulsed handshake protocols
  - Submode 1X – Pin-Definable Single-Buffered Output or Non-Latched Input
    - H1 – Status/interrupt generating input
    - H2 – Status/interrupt generating input or general-purpose output
- Port B
  - H3 and H4 – Identical to port A, H1 and H2

Mode 1 (Unidirectional 16-Bit Mode)
- Port A – Most-Significant Data Byte or Non-Latched Input or Single-Buffered Output
  - Submode XX – (not used)
    - H1 – Status/interrupt generating input
    - H2 – Status/interrupt generating input or general-purpose output
- Port B – Least-Significant Data Byte
  - Submode X0 – Pin-Definable Double-Buffered Input or Single-Buffered Output
    - H3 – Latches input data
    - H4 – Status/interrupt generating input, general-purpose output, or operation with H3 in the interlocked or pulsed handshake protocols
  - Submode X1 – Pin-Definable Double-Buffered Output or Non-Latched Input
    - H3 – Indicates data received by peripheral
    - H4 – Status/interrupt generating input, general-purpose output, or operation with H3 in the interlocked or pulsed handshake protocols

Mode 2 (Bidirectional 8-Bit Mode)
- Port A – Bit I/O
  - Submode XX – (not used)
- Port B – Double-Buffered Bidirectional Data
  - Submode XX – (not used)
    - H1 – Indicates output data received by the peripheral and controls output drivers
    - H2 – Operation with H1 in the interlocked or pulsed output handshake protocols
    - H3 – Latches input data
    - H4 – Operation with H3 in the interlocked or pulsed input handshake protocols

Mode 3 (Bidirectional 16-Bit Mode)
- Port A – Double-Buffered Bidirectional Data (Most-Significant Data Byte)
  - Submode XX – (not used)
- Port B – Double-Buffered Bidirectional Data (Least-Significant Data Byte)
  - Submode XX – (not used)
    - H1 – Indicates output data received by peripheral and controls output drivers
    - H2 – Operation with H1 in the interlocked or pulsed output handshake protocols
    - H3 – Latches input data
    - H4 – Operation with H3 in the interlocked or pulsed input handshake protocols

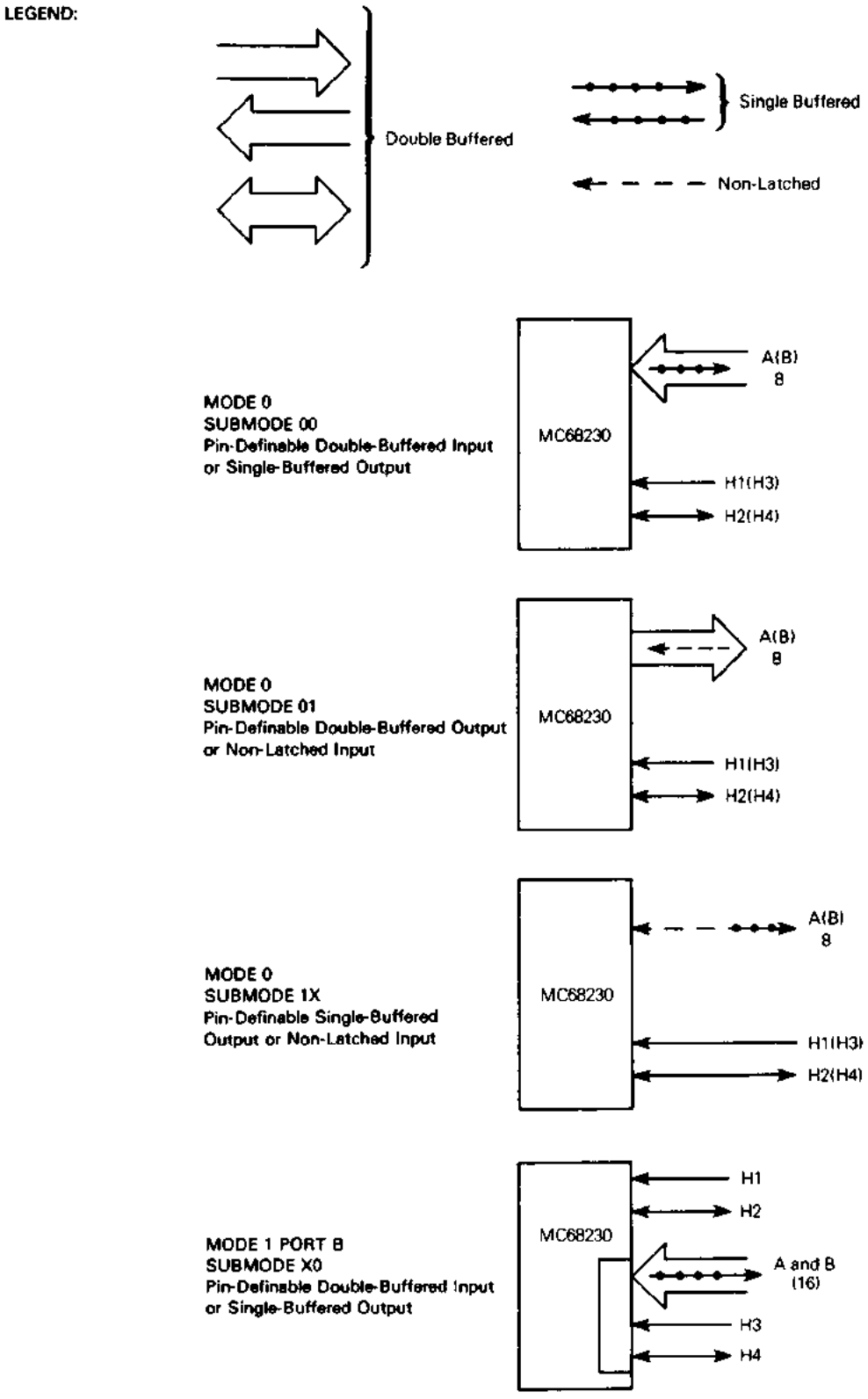


Figure 1-2. Port Mode Layout (Sheet 1 of 2)

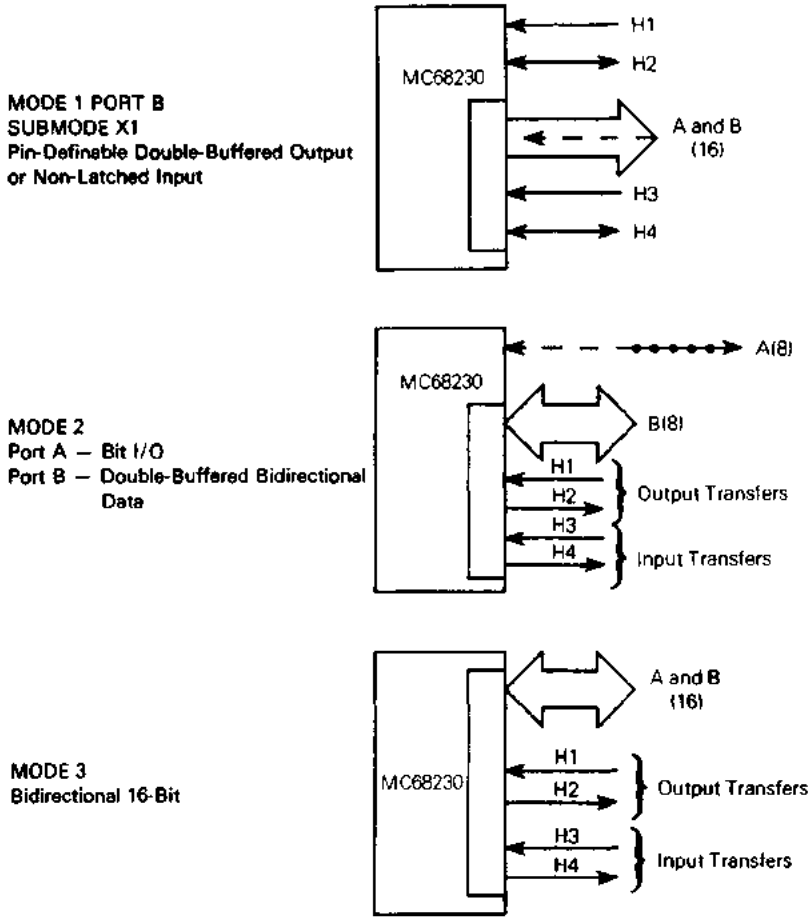


Figure 1-2. Port Mode Layout (Sheet 2 of 2)

1.2 SIGNAL DESCRIPTION

Throughout this data sheet, signals are presented using the terms active and inactive or asserted and negated independent or whether the signal is active in the high-voltage state or low-voltage state. (The active state of each logic pin is given below.) Active low signals are denoted by a superscript bar. R/$\overline{W}$ indicates a write is active low and a read active high. Table 1-2 further describes each pin and the logical pin assignments are given in Figure 1-3.

1.2.1 Bidirectional Data Bus (D0-D7)

The data bus pins, D0-D7, form an 8-bit bidirectional data bus to/from an M68000 bus master. These pins are active high.

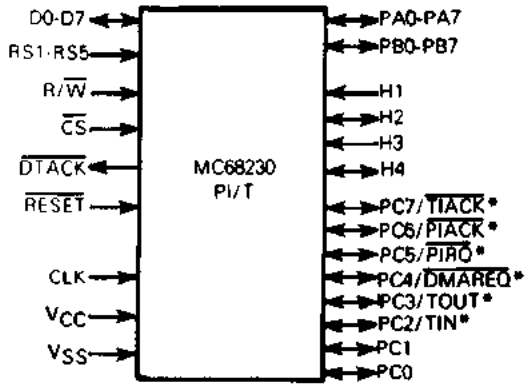
1.2.2 Register Selects (RS1-RS5)

The register select pins, RS1-RS5, are active high high-impedance inputs that determine which of the 23 internal registers is being selected. They are provided by the M68000 bus master or other bus master.

Table 1-2. Signal Summary

Signal Name	Input/Output	Active State	Edge/Level Sensitive	Output States
CLK	Input		Falling and Rising Edge	
$\overline{CS}$	Input	Low	Level	
D0-D7	Input/Output	High = 1, Low = 0	Level	High, Low, High Impedance
$\overline{DMAREQ}$	Output	Low		High, Low
$\overline{DTACK}$	Output	Low		High, Low, High Impedance*
H1(H3)***	Input	Low or High	Asserted Edge	
H2(H4)**	Input or Output	Low or High	Asserted Edge	High, Low, High Impedance
PA0-PA7**, PB0-PB7**, PC0-PC7	Input/Output, Input or Output	High = 1, Low = 0	Level	High, Low, High Impedance
$\overline{PIACK}$	Input	Low	Level	
$\overline{PIRQ}$	Output	Low		Low, High Impedance*
RS1-RS5	Input	High = 1, Low = 0	Level	
R/$\overline{W}$	Input	High Read, Low Write	Level	
$\overline{RESET}$	Input	Low	Level	
$\overline{TIACK}$	Input	Low	Level	
TIN (External Clock)	Input		Rising Edge	
TIN (Run/Halt)	Input	High	Level	
TOUT (Square Wave)	Output	Low		High, Low
TOUT ($\overline{TIRQ}$)	Output	Low		Low, High Impedance*

*Pullup resistors required.
**Note these pins have internal pullup resistors.
***H1 is level sensitive for output buffer control in modes 2 and 3.



*Individually Programmable Dual-Function Pin

Figure 1-3. Logical Pin Assignment

1.2.3 Read/Write (R/$\overline{W}$)

R/$\overline{W}$ is a high-impedance read/write input signal from the M68000 bus master, indicating whether the current bus cycle is a read (high) or write (low) cycle.

1.2.4 Chip Select ($\overline{CS}$)

$\overline{CS}$ is a high-impedance input that selects the PI/T registers for the current bus cycle. Address strobe and the data strobe (upper or lower) of the bus master, along with the appropriate address bits, must be included in the chip-select equation. A low level corresponds to an asserted chip select.

1.2.5 Data Transfer Acknowledge ($\overline{DTACK}$)

$\overline{DTACK}$ is an active low output that signals the completion of the bus cycle. During read or interrupt acknowledge cycles, $\overline{DTACK}$ is asserted after data has been provided on the data bus; during write cycles it is asserted after data has been accepted at the data bus. Data transfer acknowledge is compatible with the MC68000 and with other M68000 bus masters such as the MC68450 direct memory access controller (DMAC). A pullup resistor is required to maintain $\overline{DTACK}$ high between bus cycles.

1.2.6 Reset ($\overline{RESET}$)

$\overline{RESET}$ is a high-impedance input used to initialize all PI/T functions. All control and data direction registers are cleared and most internal operations are disabled by the assertion of $\overline{RESET}$ (low).

1.2.7 Clock (CLK)

The clock pin is a high-impedance TTL-compatible signal with the same specifications as the MC68000. The PI/T contains dynamic logic throughout, and hence this clock must not be gated off at any time. It is not necessary that this clock maintain any particular phase relationship with the M68000 system clock. It may be connected to an independent frequency source (faster or slower) as long as all bus specifications are met.

1.2.8 Port A and Port B (PA0-PA7 and PB0-PB7)

Ports A and B are 8-bit ports that may be concatenated to form a 16-bit port in certain modes. The ports may be controlled in conjunction with the handshake pins H1-H4. For stabilization during system power up, ports A and B have internal pullup resistors to V_{CC}. All port pins are active high.

1.2.9 Handshake Pins (H1-H4)

Handshake pins H1-H4 are multi-purpose pins that (depending on the operational mode) may provide an interlocked handshake, a pulsed handshake, an interrupt input (independent of data transfers), or simple I/O pins. For stabilization during system power up, H2 and H4 have internal pullup resistors to V_{CC}. The sense of H1-H4 (active high or low) may be programmed in the port general control register bits 3-0. Independent of the mode, the instantaneous level of the handshake pins can be read from the port status register.

1.2.10 Port C (PC0-PC7/Alternate Function)

This port can be used as eight general purpose I/O pins (PC0-PC7) or any combination of six special function pins and two general purpose I/O pins (PC0-PC1). Each dual-function pin can be a standard I/O or a special function independent of the other port C pins. When used as a port C pin, these pins are active high. They may be individually programmed as inputs or outputs by the port C data direction register. The dual-function pins are defined in the following paragraphs.

The alternate functions TIN, TOUT, and $\overline{TIACK}$ are timer I/O pins. TIN may be used as a rising-edge triggered external clock input or an external run/halt control pin (the timer is in the run state if run/halt is high and in the halt state if run/halt is low). TOUT may provide an active low timer interrupt request output or a general-purpose square-wave output, initially high. $\overline{TIACK}$ is an active low high-impedance input used for timer interrupt acknowledge.

Port A and B functions have an independent pair of active low interrupt request ($\overline{PIRQ}$) and interrupt acknowledge ($\overline{PIACK}$) pins.

The $\overline{DMAREQ}$ (direct memory access request) pin provides an active low direct memory access controller request pulse for three clock cycles, completely compatible with the MC68450 DMAC.

1.3 REGISTER MODEL

A register model that includes the corresponding register selects is shown in Table 1-3.

Table 1-3. Register Model (Sheet 1 of 2)

Register Select Bits 5	4	3	2	1	7	6	5	4	3	2	1	0	Register Value After $\overline{RESET}$ (Hex Value)	
0	0	0	0	0	Port Mode Control		H34 Enable	H12 Enable	H4 Sense	H3 Sense	H2 Sense	H1 Sense	0 0	Port General Contol Register
0	0	0	0	1	*	SVCRQ Select		IPF Select		Port Interrupt Priority Control			0 0	Port Service Request Register
0	0	0	1	0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	0 0	Port A Data Direction Register
0	0	0	1	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	0 0	Port B Data Direction Register
0	0	1	0	0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	0 0	Port C Data Direction Register
0	0	1	0	1	Interrupt Vector Number						*	*	0 F	Port Interrupt Vector Register
0	0	1	1	0	Port A Submode		H2 Control			H2 Int Enable	H1 SVCRQ Enable	H1 Stat Ctrl	0 0	Port A Control Register
0	0	1	1	1	Port B Submode		H4 Control			H4 Int Enable	H3 SVCRQ Enable	H3 Stat Ctrl	0 0	Port B Control Register
0	1	0	0	0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	**	Port A Data Register
0	1	0	0	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	**	Port B Data Register
0	1	0	1	0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	***	Port A Alternate Register
0	1	0	1	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	***	Port B Alternate Register
0	1	1	0	0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	****	Port C Data Register
0	1	1	0	1	H4 Level	H3 Level	H2 Level	H1 Level	H4S	H3S	H2S	H1S	****	Port Status Register
0	1	1	1	0	*	*	*	*	*	*	*	*	0 0	(Null)
0	1	1	1	1	*	*	*	*	*	*	*	*	0 0	(Null)

* Unused, read as zero
** Value before $\overline{RESET}$
*** Current value on pins
**** Undetermined value

Table 1-3. Register Model (Sheet 2 of 2)

Register Select Bits												Register Value After $\overline{\text{RESET}}$ (Hex Value)	
5	4	3	2	1	7	6	5	4	3	2	1	0	
1	0	0	0	0	TOUT/$\overline{\text{TIACK}}$ Control			Z D Ctrl	*	Clock Control		Timer Enable	0 0	Timer Control Register
1	0	0	0	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	0 F	Timer Interrupt Vector Register
1	0	0	1	0	*	*	*	*	*	*	*	*	0 0	(Null)
1	0	0	1	1	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	* *	Counter Preload Register (High)
1	0	1	0	0	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	* *	Counter Preload Register (Mid)
1	0	1	0	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	* *	Counter Preload Register (Low)
1	0	1	1	0	*	*	*	*	*	*	*	*	0 0	(Null)
1	0	1	1	1	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	* *	Count Register (High)
1	1	0	0	0	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	* *	Count Register (Mid)
1	1	0	0	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	* *	Count Register (Low)
1	1	0	1	0	*	*	*	*	*	*	*	ZDS	0 0	Timer Status Register
1	1	0	1	1	*	*	*	*	*	*	*	*	0 0	(Null)
1	1	1	0	0	*	*	*	*	*	*	*	*	0 0	(Null)
1	1	1	0	1	*	*	*	*	*	*	*	*	0 0	(Null)
1	1	1	1	0	*	*	*	*	*	*	*	*	0 0	(Null)
1	1	1	1	1	*	*	*	*	*	*	*	*	0 0	(Null)

*Unused, read as zero
**Value before $\overline{\text{RESET}}$

1.4 BUS INTERFACE OPERATION

The PI/T has an asynchronous bus interface, primarily designed for use with an M68000 microprocessor. With care, however, it can be connected to synchronous microprocessor buses. This section completely describes the PI/T's bus interface, and is intended for the asynchronous bus designer unless otherwise mentioned.

In an asynchronous system the PI/T clock may operate at a significantly different frequency, either higher or lower, than the bus master and other system components, as long as all bus specifications are met. The MC68230 CLK pin has the same specifications as the MC68000 CLK pin, and must not be gated off at any time.

The following signals generate normal read and write cycles to the PI/T: $\overline{CS}$ (chip select), R/$\overline{W}$ (read/write), RS1-RS5 (five register select bits), D0-D7 (the 8-bit bidirectional data bus), and $\overline{DTACK}$ (data transfer acknowledge). To generate interrupt acknowledge cycles, PC6/$\overline{PIACK}$ or PC7/$\overline{TIACK}$ is used instead of $\overline{CS}$, and the register select pins are ignored. No combination of the following pin functions may be asserted simultaneously: $\overline{CS}$, $\overline{PIACK}$, or $\overline{TIACK}$.

1.4.1 Read Cycles

This category includes all register reads, except port or timer interrupt acknowledge cycles. When $\overline{CS}$ is asserted, the register select and R/$\overline{W}$ inputs are latched internally. They must meet small setup and hold time requirements with respect to the asserted edge of $\overline{CS}$. (Refer to **6.6 AC ELECTRICAL SPECIFICATIONS** for further information.) The PI/T is not protected against aborted (shortened) bus cycles generated by an address error or bus error exception in which it is addressed.

Certain operations triggered by normal read (or write) bus cycles are not complete within the time allotted to the bus cycle. One example is transfers to/from the double-buffered latches that occur as a result of the bus cycle. If the bus master's clock is significantly faster than the PI/T's the possibility exists that, following the bus cycle, $\overline{CS}$ can be negated then re-asserted before completion of these internal operations. In this situation the PI/T does not recognize the re-assertion of $\overline{CS}$ until these operations are complete. Only at that time does it begin the internal sequencing necessary to react to the asserted $\overline{CS}$. Since $\overline{CS}$ also controls the $\overline{DTACK}$ response, this "bus cycle recovery time" can be related to the clock edge on which $\overline{DTACK}$ is asserted for that cycle. The PI/T will recognize the subsequent assertion of $\overline{CS}$ three clock periods after the clock edge on which $\overline{DTACK}$ was previously asserted.

The register select and R/$\overline{W}$ inputs pass through an internal latch that is transparent when the PI/T can recognize a new $\overline{CS}$ pulse (see above paragraph). Since the internal data bus of the PI/T is continuously engaged for read transfers, the read access time (to the data bus buffers) begins when the register selects are stabilized internally. Also, when the PI/T is ready to begin a new bus cycle, the assertion of $\overline{CS}$ enables the data bus buffers within a short propagation delay. This does not contribute to the overall read access time unless $\overline{CS}$ is asserted significantly after the register select and R/$\overline{W}$ inputs are stabilized (as may occur with synchronous bus microprocessors).

In addition to the chip select's previously mentioned duties, it controls the assertion of $\overline{DTACK}$ and latching of read data at the data bus interface. Except for controlling input latches and enabling the data bus buffers, all of these functions occur only after $\overline{CS}$ has been recognized internally and synchronized with the internal clock. Chip select is recognized on the falling edge of the clock if the setup time is met; $\overline{DTACK}$ is asserted (low) on the next falling edge of the clock. Read data is

latched at the PI/T's data bus interface at the same time $\overline{DTACK}$ is asserted. It is stable as long as chip select remains asserted independent of other external conditions.

From the above discussion it is clear that if the chip select setup time prior to the falling edge of the clock is met, the PI/T can consistently respond to a new read or write bus cycle every four clock cycles. This fact is especially useful in designing the PI/T's clock in synchronous bus systems not using $\overline{DTACK}$. (An extra clock period is required in interrupt acknowledge cycles, see **1.4.2 Interrupt Acknowledge Cycles.**)

In asynchronous bus systems in which the PI/T's clock differs from that of the bus master, generally there is no way to guarantee that the chip select setup time with respect to the PI/T clock is met. Thus, the only way to determine that the PI/T recognized the assertion of $\overline{CS}$ is to wait for the assertion of $\overline{DTACK}$. In this situation, all latched bus inputs to the PI/T must be held stable until $\overline{DTACK}$ is asserted. These include register select, R/$\overline{W}$, and write data inputs (see below).

System specifications impose a maximum delay from the trailing (negated) edge of $\overline{CS}$ to the negated edge of $\overline{DTACK}$. As system speeds increase this becomes more difficult to meet with a simple pullup resistor tied to the $\overline{DTACK}$ line. Therefore, the PI/T provides an internal active pullup device to reduce the rise time, and a level-sensitive circuit that later turns this device off. $\overline{DTACK}$ is negated asynchronously as fast as possible following the rising edge of chip select, then three-stated to avoid interference with the next bus cycle.

The system designer must take care that $\overline{DTACK}$ is negated and three-stated quickly enough after each bus cycle to avoid interference with the next one. With an M68000 this necessitates a relatively fast external path from the data strobe negation to $\overline{CS}$ bus master negation.

1.4.2 Interrupt Acknowledge Cycles

Special internal operations take place on PI/T interrupt acknowledge cycles. The port interrupt vector register or the timer vector register are implicitly addressed by the assertion of PC6/$\overline{PIACK}$ or PC7/$\overline{TIACK}$, respectively. The signals are first synchronized with the falling edge of the clock. One clock period after they are recognized, the data bus buffers are enabled and the vector is driven onto the bus. $\overline{DTACK}$ is asserted after another clock period to allow the vector some setup time prior to $\overline{DTACK}$. $\overline{DTACK}$ is negated, then three-stated, as with normal read or write cycles, when $\overline{PIACK}$ or $\overline{TIACK}$ is negated.

1.4.3 Write Cycles

In many ways, write cycles are similar to normal read cycles. On write cycles, data at the D0-D7 pins must meet the same setup specifications as the register select and R/$\overline{W}$ lines. Like these signals, write data is latched on the asserted edge of $\overline{CS}$, and must meet small setup and hold time requirements with respect to that edge. The same bus cycle recovery conditions exist as for normal read cycles. No other differences exist.

NOTE

For mask sets GG7 and KD1 if the RS lines are selecting the port interrupt vector register (PIVR) or timer interrupt vector register (TIVR) during an interrupt acknowledge bus cycle then those registers may be changed. Four cases exist for this situation, they are:

1. Case: RS lines are addressing PIVR during a port interrupt acknowledge cycle (PIACK asserted).
   Results: Incorrect IACK vector on data lines, bits 0 and 1 are zero, PIVR and TIVR remain the same and are not changed.
2. Case: RS lines are addressing TIVR during a port interrupt acknowledge cycle (PIACK asserted).
   Results: Incorrect IACK vector on data lines, PIVR and TIVR are changed.
3. Case: RS lines are addressing PIVR during a timer interrupt acknowledge cycle (TIACK asserted).
   Results: Incorrect IACK vector on data lines, PIVR and TIVR are changed.
4. Case: RS lines are addressing TIVR during a timer interrupt acknowledge cycle (TIACK asserted).
   Results: Correct IACK vector on data lines, PIVR and TIVR remain the same and are not changed.

For MC68000 and MC68010 systems that use A1-A5 for RS lines RS1-RS5 the above cases will never occur. A5 and A4 will remain high during interrupt acknowledge cycles and thus PIVR and TIVR will not be selected as shown below.

	RS5	RS4	RS3	RS2	RS1
MC68000 IACK Cycle	1	1	— Encoded Level —		
MC68230 PIVR Address	0	0	1	0	1
MC68230 TIVR Address	1	0	0	0	1

SECTION 2
PORT GENERAL INFORMATION AND CONVENTIONS

This section introduces concepts that are generally applicable to the PI/T ports independent of the chosen mode and submode. For this reason, no particular port or handshake pins are mentioned; the notation H1(H3) indicates that, depending on the chosen mode and submode, the statement given may be true for either the H1 or H3 handshake pin.

2.1 UNIDIRECTIONAL VS BIDIRECTIONAL

Figure 1-2 shows the configuration of ports A and B and each of the handshake pins in each port mode and submode. In modes 0 and 1, a data direction register is associated with each of the ports. These registers contain one bit for each port pin to determine whether that pin is an input or an output. Modes 0 and 1 are, thus, called unidirectional modes because each pin assumes a constant direction, changeable only by a reset condition or a programming change. These modes allow double-buffered data transfers in one direction. This direction, determined by the mode and submode definition, is known as the primary direction. Data transfers in the primary direction are controlled by the handshake pins. Data transfers not in the primary direction are generally unrelated, and single or unbuffered data paths exist.

In modes 2 and 3 there is no concept of primary direction as in modes 0 and 1. Except for port A in mode 2 (bit I/O), the data direction registers have no effect. These modes are bidirectional, in that the direction of each transfer (always 8 or 16 bits, double buffered) is determined dynamically by the state of the handshake pins. Thus, for example, data may be transferred out of the ports, followed very shortly by a transfer into the same port pins. Transfers to and from the ports are independent and may occur in any sequence. Since the instantaneous direction is always determined by the external system, a small amount of arbitration logic may be required.

2.1.1 Control of Double-Buffered Data Ports

Generally speaking, the PI/T is a double-buffered device. In the primary direction, double buffering allows orderly transfers by using the handshake pins in any of several programmable protocols. (When bit I/O is used, double buffering is not available and the handshake pins are used as outputs or status/interrupt inputs.)

Use of double buffering is most beneficial in situations where a peripheral device and the computer system are capable of transferring data at roughly the same speed. Double buffering allows the fetch operation of the data transmitter to be overlapped with the store operation of the data receiver. Thus, throughput measured in bytes or words-per-second may be greatly enhanced. If there is a large mismatch in transfer capability between the computer and the peripheral, little or no benefit is obtained. In these cases there is no penalty in using double buffering.

2.1.2 Double-Buffered Input Transfers

In all modes, the PI/T supports double-buffered input transfers. Data that meets the port setup and hold times is latched on the asserted edge of H1(H3). H1(H3) is edge sensitive, and may assume any duty cycle as long as both high and low minimum times are observed. The PI/T contains a port status register whose H1S(H3S) status bit is set anytime any input data that has not been read by the bus master is present in the double-buffered latches. The action of H2(H4) is programmable; it may indicate whether there is room for more data in the PI/T latches or it may serve other purposes. The following options are available, depending on the mode.

1. H2(H4) may be an edge-sensitive input that is independent of H1(H3) and the transfer of port data. On the asserted edge of H2(H4), the H2S(H4S) status bit is set. It is cleared by the direct method (refer to **2.3 DIRECT METHOD OF RESETTING STATUS**), the $\overline{\text{RESET}}$ pin being asserted, or when the H12 enable (H34 enable) bit of the port general control register is zero.
2. H2(H4) may be a general purpose output pin that is always negated. The H2S(H4S) status bit is always zero.
3. H2(H4) may be a general purpose output pin that is always asserted. The H2S(H4S) status bit is always zero.
4. H2(H4) may be an output pin in the interlocked input handshake protocol. It is asserted when the port input latches are ready to accept new data. It is negated asynchronously following the asserted edge of the H1(H3) input. As soon as the input latches become ready, H2(H4) is again asserted. When both double-buffered latches are full, H2(H4) remains negated until data is removed by a read of port A (port B) data register. Thus, anytime the H2(H4) output is asserted, new input data may be entered by asserting H1(H3). At other times transitions of H1(H3) are ignored. The H2S(H4S) status bit is always zero. When H12 enable (H34 enable) is zero, H2(H4) is held negated.

5. H2(H4) may be an output pin in the pulsed input handshake protocol. It is asserted exactly as in the interlocked input protocol, but never remains asserted longer than four clock cycles. Typically, a four clock cycle pulse is generated. But in the case that a subsequent H1(H3) asserted edge occurs before termination of the pulse, H2(H4) is negated asynchronously. Thus, anytime after the leading edge of the H2(H4) pulse, new data may be entered in the PI/T double-buffered input latches. The H2S(H4S) status bit is always zero. When H12 enable (H34 enable) is zero, H2(H4) is held negated.

A sample timing diagram is shown in Figure 2-1. The H2(H4) interlocked and pulse input handshake protocols are shown. The $\overline{\text{DMAREQ}}$ pin is also shown assuming it is enabled. All handshake pin sense bits are assumed to be zero (refer to **4.1 PORT GENERAL CONTROL REGISTER (PGCR)**); thus, the pins are in the low state when asserted. Due to the great similarity between modes, this timing diagram is applicable to all double-buffered input transfers.

2.1.3 Double-Buffered Output Transfers

The PI/T supports double-buffered output transfers in all modes. Data, written by the bus master to the PI/T, is stored in the port's output latch. The peripheral accepts the data by asserting H1(H3), which causes the next data to be moved to the port's output latch as soon as it is available. The function of H2(H4) is programmable; it may indicate whether new data has been moved to the output latch or it may serve other purposes. The H1S(H3S) status bit may be programmed for two interpretations. First, the status bit is a one when there is at least one latch in the double-buffered data path that can accept new data. After writing one byte/word of data to the ports, an interrupt

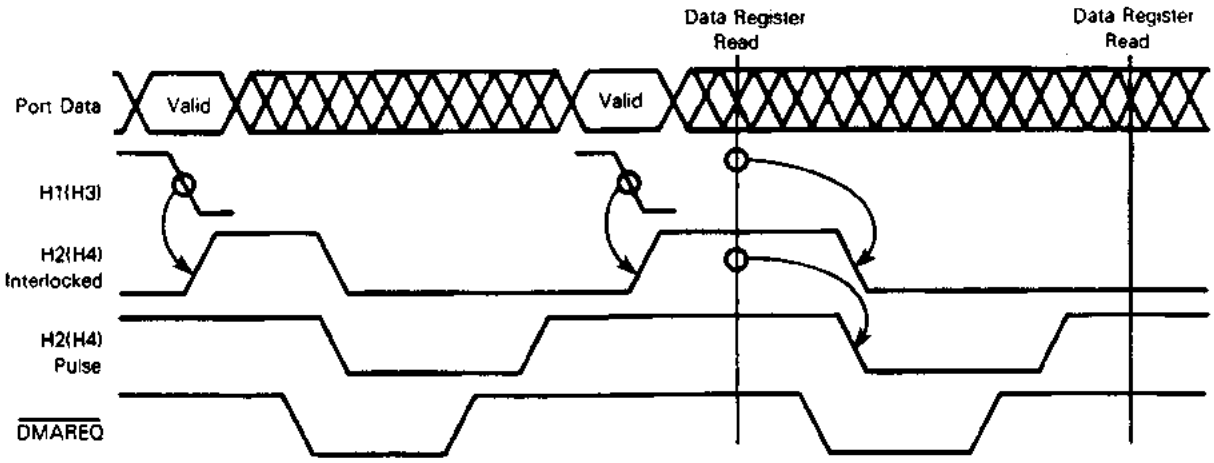


Figure 2-1. Double-Buffered Input Transfers Timing Diagram

service routine could check this bit to determine if it could store another byte/word, thus filling both latches. Second, when the bus master is finished, it is often useful to be able to check whether all of the data has been transferred to the peripheral. The H1S(H3S) status bit is set when both output latches are empty. The programmable options of the H2(H4) pin are given below, depending on the mode.

1. H2(H4) may be an edge-sensitive input pin independent of H1(H3) and the transfer of port data. On the asserted edge of H2(H4), the H2S(H4S) status bit is set. It is cleared by the direct method (refer to **2.3 DIRECT METHOD OF RESETTING STATUS**), the $\overline{\text{RESET}}$ pin being asserted, or when the H12 enable (H34 enable) bit of the port general control register is zero.
2. H2(H4) may be a general-purpose output pin that is always negated. The H2S(H4S) status bit is always zero.
3. H2(H4) may be a general-purpose output pin that is always asserted. The H2S(H4S) status bit is always zero.
4. H2(H4) may be an output pin in the interlocked output handshake protocol. H2(H4) is asserted two clock cycles after data is transferred to the double-buffered output latches. The data remains stable and H2(H4) remains asserted until the next asserted edge of the H1(H3) input. At that time, H2(H4) is asynchronously negated. As soon as the next data is available, it is transferred to the output latches and H2(H4) is asserted. When H2(H4) is negated, asserted transitions on H1(H3) have no effect on the data paths. As is explained later, however, in modes 2 and 3 H1 does control the three-state output buffers of the bidirectional port(s). The H2S(H4S) status bit is always zero. When H12 enable (H34 enable) is zero, H2(H4) is held negated.
5. H2(H4) may be an output pin in the pulsed output handshake protocol. It is asserted exactly as in the interlocked output protocol above, but never remains asserted longer than four clock cycles. Typically, a four clock pulse is generated. But in the case that a subsequent H1(H3) asserted edge occurs before termination of the pulse, H2(H4) is negated asynchronously, thus shortening the pulse. The H2S(H4S) status bit is always zero. When H12 enable (H34 enable) is zero, H2(H4) is held negated.

A sample timing diagram is shown in Figure 2-2. The H2(H4) interlocked and pulsed output handshake protocols are shown. The $\overline{\text{DMAREQ}}$ pin is also shown assuming it is enabled. All handshake pin sense bits are assumed to be zero; thus, the pins are in the low state when asserted. Due to the great similarity between modes, this timing diagram is applicable to all double-buffered output transfers.

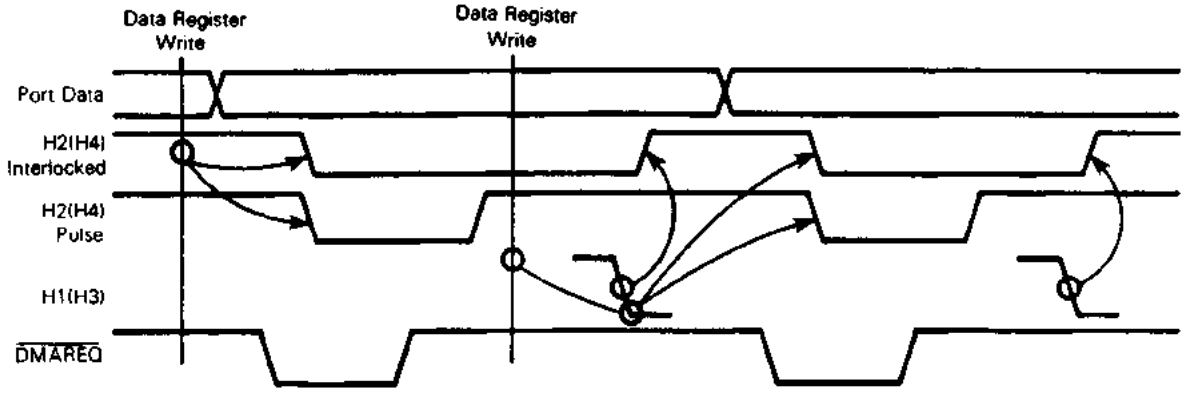


Figure 2-2. Double-Buffered Output Transfers Timing Diagram

2.2 REQUESTING BUS MASTER SERVICE

The PI/T has several means of indicating a need for service by a bus master. First, the processor may poll the port status register. It contains a status bit for each handshake pin, plus a level bit that always reflects the instantaneous state of that handshake pin. A status bit is one when the PI/T needs servicing (i.e., generally when the bus master needs to read or write data to the ports) or when a handshake pin used as a simple status input has been asserted. The interpretation of these bits is dependent on the chosen mode and submode.

Second, the PI/T may be placed in the processor's interrupt structure. As mentioned previously, the PI/T contains port A and B control registers that configure the handshake pins. Other bits in these registers enable an interrupt associated with each handshake pin. This interrupt is made available through the PC5/$\overline{\text{PIRQ}}$ pin, if the $\overline{\text{PIRQ}}$ function is selected. Three additional conditions are required for $\overline{\text{PIRQ}}$ to be asserted: 1) the handshake pin status bit is set, 2) the corresponding interrupt (service request) enable bit is set, and 3) DMA requests are not associated with that data transfer (H1 and H3 only). The conditions from each of the four handshake status bits and corresponding status bits are ORed to determine $\overline{\text{PIRQ}}$. To clear the interrupt, the proper status bit must be cleared (see **2.3 DIRECT METHOD OF RESETTING STATUS**).

The third method of requesting service is via the PC4/$\overline{\text{DMAREQ}}$ pin. This pin can be associated with double-buffered transfers in each mode. If it is used as a DMA controller request, it can initiate requests to keep the PI/T's input/output double-buffering empty/full as much as possible. It will not overrun the DMA controller. The pin is compatible with the MC68450 direct memory access controller (DMAC).

2.2.1 Vectored, Prioritized Port Interrupts

Use of MC68000-compatible vectored interrupts with the PI/T requires the $\overline{\text{PIRQ}}$ and $\overline{\text{PIACK}}$ pins. When $\overline{\text{PIACK}}$ is asserted while $\overline{\text{PIRQ}}$ is asserted, the PI/T places an 8-bit vector on the data pins D0-D7. Under normal conditions, this vector corresponds to the highest priority enabled active port interrupt source with which the $\overline{\text{DMAREQ}}$ pin is not currently associated. The most-significant six bits are provided by the port interrupt vector register (PIVR), with the lower two bits supplied by prioritization logic according to conditions present when $\overline{\text{PIACK}}$ is asserted. It is important to note that the only effect on the PI/T caused by interrupt acknowledge cycles is that the vector is placed on the data bus. Specifically, no registers, data, status, or other internal states of the PI/T are affected by the cycle.

Several conditions may be present when the $\overline{\text{PIACK}}$ input is asserted to the PI/T. These conditions affect the PI/T's response and the termination of the bus cycle. If the PI/T has no interrupt function selected, or is not asserting $\overline{\text{PIRQ}}$, the PI/T will make no response to $\overline{\text{PIACK}}$ ($\overline{\text{DTACK}}$ will not be asserted). If the PI/T is asserting $\overline{\text{PIRQ}}$ when $\overline{\text{PIACK}}$ is received, the PI/T will output the contents of the port interrupt vector register and the prioritization bits. If the PIVR has not been initialized, $0F will be read from this register. These conditions are summarized in Table 2-1.

Table 2-1. Response to Port Interrupt Acknowledge

Conditions	$\overline{\text{PIRQ}}$ negated OR interrupt request function not selected	$\overline{\text{PIRQ}}$ asserted
PIVR has not been initialized since $\overline{\text{RESET}}$	No response from PI/T. No $\overline{\text{DTACK}}$.	PI/T provides $0F, the Uninitialized Vector*
PIVR has been initialized since $\overline{\text{RESET}}$	No response from PI/T. No $\overline{\text{DTACK}}$.	PI/T provides PIVR contents with prioritization bits.

*The uninitialized vector is the value returned from an interrupt vector register before it has been initialized.

The vector table entries for the PI/T appear as a contiguous block of four vector numbers whose common upper six bits are programmed in the PIVR. The following table pairs each interrupt source with the 2-bit value provided by the prioritization logic when interrupt acknowledge is asserted (see **4.2. PORT SERVICE REQUEST REGISTER (PSRR)**).

H1 source — 00	H3 source — 10
H2 source — 01	H4 source — 11

2.2.2 Autovectored Port Interrupts

Autovectored interrupts use only the $\overline{\text{PIRQ}}$ pin. The operation of the PI/T with vectored and autovectored interrupts is identical except that no vectors are supplied and the PC6/$\overline{\text{PIACK}}$ pin can be used as a port C pin.

2.2.3 DMA Request Operation

The direct memory access request ($\overline{\text{DMAREQ}}$) pulse (when enabled) is associated with output or input transfers to keep the initial and final output latches full or initial and final input latches empty, respectively. Figures 2-3 and 2-4 show all the possible paths in generating DMA requests. See **4.2 PORT SERVICE REQUEST REGISTER (PSRR)** for programming the operation of the DMA request bit.

$\overline{\text{DMAREQ}}$ is generated on the bus side of the MC68230 by the synchronized* chip select. If the conditions of Figures 2-3 or 2-4 are met, an assertion of $\overline{\text{CS}}$ will cause $\overline{\text{DMAREQ}}$ to be asserted three PI/T clocks (plus the delay time from the clock edge) after $\overline{\text{CS}}$ is synchronized. $\overline{\text{DMAREQ}}$ remains asserted three clock cycles (plus the delay time from the clock edge) and is then negated.

$\overline{\text{DMAREQ}}$ pulses are associated with peripheral transfers or are generated by the synchronized* H1(H3) input. If the conditions of Figures 2-3 or 2-4 are met, an assertion of the H1(H3) input will cause $\overline{\text{DMAREQ}}$ to be asserted 2.5 PI/T clock cycles (plus the delay time from clock edge) after H1(H3) is synchronized. $\overline{\text{DMAREQ}}$ remains asserted three clock cycles (plus the delay time from the clock edge) and is then negated.

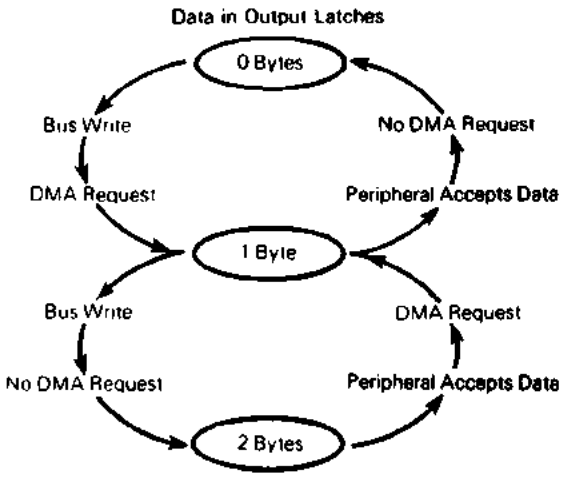


Figure 2-3. $\overline{\text{DMAREQ}}$ Associated with Output Transfers

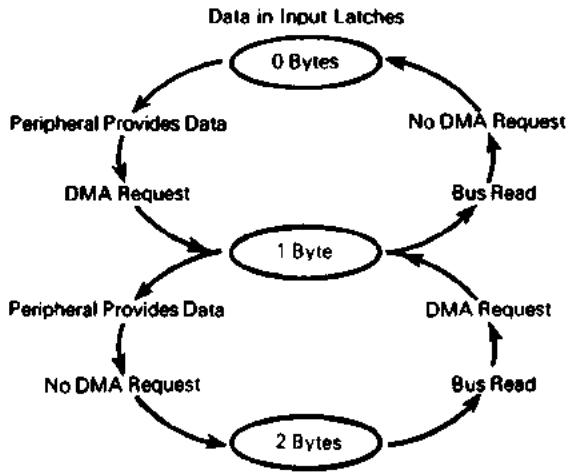


Figure 2-4. $\overline{\text{DMAREQ}}$ Associated with Input Transfers

2.3 DIRECT METHOD OF RESETTING STATUS

In certain modes one or more handshake pins can be used as edge-sensitive inputs for the sole purpose of setting bits in the port status register. These bits consist of simple flip-flops. They are set (to one) by the occurrence of the asserted edge of the handshake pin input. Resetting a handshake status bit can be done by writing an 8-bit mask to the port status register. This is called the direct method of resetting. To reset a status bit that is resettable by the direct method, the mask must

* Synchronized means that the appropriate input signal (H1, H3, or $\overline{\text{CS}}$) has been sampled by the PI/T on the appropriate edge of the clock (rising edge for H1(H3) and falling edge for $\overline{\text{CS}}$). Refer to **1.4 BUS INTERFACE OPERATION** for the exception concerning $\overline{\text{CS}}$. If a bus access (assertion of $\overline{\text{CS}}$) and a port access (assertion of H1(H3)) occur at the same time, $\overline{\text{CS}}$ will be recognized without any delay. H1(H3) will be recognized one clock cycle later.

contain a one in the bit position of the port status register corresponding to the desired status bit. For status bits that are not resettable by the direct method in the chosen mode, the data written to the port status register has no effect. For status bits that are resettable by the direct method in the chosen mode, a zero in the mask has no effect.

2.4 HANDSHAKE PIN SENSE CONTROL

The PI/T contains exclusive-OR gates to control the sense of each of the handshake pins, whether used as inputs or outputs. Four bits in the port general control register may be programmed to determine whether the pins are asserted in the low- or high-voltage state. As with other control registers, these bits are reset to zero when the $\overline{\text{RESET}}$ pin is asserted, defaulting the asserted level to be low.

2.5 ENABLING PORTS A AND B

Certain functions involved with double-buffered data transfers, the handshake pins, and the status bits may be disabled by the external system or by the programmer during initialization. The port general control register contains two bits, H12 enable and H34 enable, which control these functions. These bits are cleared to the zero state when the $\overline{\text{RESET}}$ pin is asserted, and the functions are disabled. The functions are the following:

1. Independent of other actions by the bus master or peripheral (via the handshake pins), the PI/T's disabled handshake controller is held to the "empty" state; i.e., no data is present in the double-buffered data path.
2. When any handshake pin is used to set a simple status flip-flop, unrelated to double-buffered transfers, these flip-flops are held reset to zero (see Table 1-1).
3. When H2(H4) is used in an interlocked or pulsed handshake with H1(H3), H2(H4) is held negated, regardless of the chosen mode, submode, and primary direction. Thus, for double-buffered input transfers, the programmer may signal a peripheral when the PI/T is ready to begin transfers by setting the associated handshake enable bit to one.

2.6 PORT A AND B ALTERNATE REGISTERS

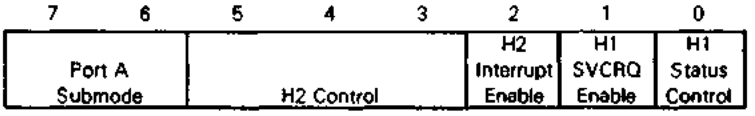
In addition to the port A and B data registers, the PI/T contains port A and B alternate registers. These registers are read only, and simply provide the instantaneous (non-latched) level of each port pin. They have no effect on the operation of the handshake pins, double-buffered transfers, status bits, or any other aspect of the PI/T, and they are mode/submode independent. Refer to **4.7 PORT ALTERNATE REGISTERS** for further information.

SECTION 3
PORT MODES

This section contains information that distinguishes the various port modes and submodes. General characteristics common to all modes are defined in **SECTION 2 PORT GENERAL INFORMATION AND CONVENTIONS.** A description of the port A control register (PACR) and port B control register (PBCR) is given before each mode description. After each submode description, the programmable options are listed for that submode.

3.1 PORT A CONTROL REGISTER

Port A Control Register (PACR)

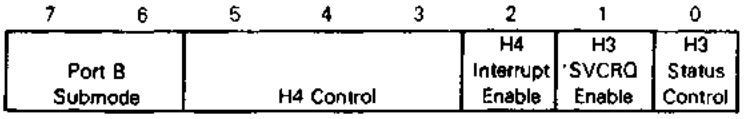


The port A control register, in conjunction with the programmed mode and the port B submode, controls the operation of port A and the handshake pins H1 and H2. The port A control register contains five fields: bits 7 and 6 specify the port A submode; bits 5, 4, and 3 control the operation of the H2 handshake pin and the H2S status bit; bit 2 determines whether an interrupt will be generated when the H2S status bit goes to one; and bit 1 determines whether a service request (interrupt request or DMA request) will occur; bit 0 controls the operation of the H1S status bit. The PACR is always readable and writable.

All bits are cleared to zero when the $\overline{\text{RESET}}$ pin is asserted. When the port A submode field is relevant in a mode/submode definition, it must not be altered unless the H12 enable bit in the port general control register is clear (see Table 1-3 located on foldout pages 1 and 2 at the end of this document). Altering these bits will give unpredictable results.

3.2 PORT B CONTROL REGISTER

Port B Control Register (PBCR)



The port B control register specifies the operation of port B and the handshake pins H3 and H4. The port B control register contains five fields: bits 7 and 6 specify the port B submode; bits 5, 4, and 3 control the operation of the H4 handshake pin and H4S status bit; bit 2 determines whether an interrupt will be generated when the H4S status bit goes to a one; bit 1 determines whether a service request (interrupt request or DMA request) will occur; and bit 0 controls the operation of the H3S status bit. The PBCR is always readable and writable. There is never a consequence to reading the register.

All bits are cleared to zero when the $\overline{\text{RESET}}$ pin is asserted. When the port B submode field is relevant in a mode/submode definition, it must not be altered unless the H34 enable bit in the port general control register is clear (see Table 1-3 located on foldout pages 1 and 2 at the end of this document).

3.3 MODE 0 — UNIDIRECTIONAL 8-BIT MODE

In mode 0, ports A and B operate independently. Each may be configured in any of its three possible submodes:

Submode 00 — Pin-Definable Double-Buffered Input or Single-Buffered Output
Submode 01 — Pin-Definable Double-Buffered Output or Non-Latched Input
Submode 1X — Bit I/O (Pin-Definable Single-Buffered Output or Non-Latched Input)

Handshake pins H1 and H2 are associated with port A and configured by programming the port A control register. (The H12 enable bit of the port general control register enables port A transfers.) Handshake pins H3 and H4 are associated with port B and configured by programming the port B control register. (The H34 enable bit of the port general control register enables port B transfers.) The port A and B data direction registers operate in all three submodes. Along with the submode, they affect the data read and write at the associated data register according to Table 3-1. They also enable the output buffer associated with each port pin. The $\overline{\text{DMAREQ}}$ pin may be associated with either (not both) port A or port B, but does not function if the bit I/O submode (submode 1X) is programmed for the chosen port.

Table 3-1. Mode 0 Port Data Paths

Mode	Read Port A/B Data Register		Write Port A/B Data Register	
	DDR = 0	DDR = 1	DDR = X	
0 Submode 00	FIL, D.B.	FOL Note 3	FOL, S.B.	Note 1
0 Submode 01	Pin	FOL Note 3	IOL/FOL, D.B.	Note 2
0 Submode 1X	Pin	FOL Note 3	FOL, S.B.	Note 1

Abbreviations:
IOL — Initial Output Latch
FOL — Final Output Latch
FIL — Final Input Latch
S.B. — Single Buffered
D.B. — Double Buffered
DDR — Data Direction Register

Note 1: Data is latched in the output data registers (final output latch) and will be single buffered at the pin if the DDR is 1. The output buffers will be turned off if the DDR is 0.
Note 2: Data is latched in the double-buffered output data registers. The data in the final output latch will appear on the port pin if the DDR is a 1.
Note 3: The output drivers that connect the final output latch to the pins are turned on.

3.3.1 Submode 00 — Pin-Definable Double-Buffered Input or Single-Buffered Output

In mode 0, double-buffered input transfers of up to eight bits are available by programming submode 00 in the desired port's control register. Data that meets the port setup and hold times is latched on the asserted edge of H1(H3) and is placed in the initial or final input latch. H1(H3) is edge sensitive and may assume any duty cycle as long as both high and low minimum times are observed. The PI/T contains a port status register whose H1S(H3S) status bit is set anytime any input data that has not been read by the bus master is present in the double-buffered latches. The action of H2(H4) is programmable. The following options are available:

1. H2(H4) may be an edge-sensitive status input that is independent of H1(H3) and the transfer of port data. On the asserted edge of H2(H4), the H2S(H4S) status bit is set. It is cleared by either the $\overline{\text{RESET}}$ pin being asserted, writing a one to the particular status bit in the port status register (PSR), or when the H12 enable (H34 enable) bit of the port general register is clear.
2. H2(H4) may be a general-purpose output pin that is always negated. In this case the H2S(H4S) status bit is always clear.
3. H2(H4) may be a general-purpose output pin that is always asserted. In this case the H2S(H4S) status bit is always clear.
4. H2(H4) may be an output pin in the interlocked input handshake protocol. It is asserted when the port input latches are ready to accept new data. It is negated asynchronously following the asserted edge of the H1(H3) input. As soon as the input latches become ready, H2(H4) is again asserted. When the input double-buffered latches are full, H2(H4) remains negated until data is removed. Thus, anytime the H2(H4) output is asserted, new input data may be entered by asserting H1(H3). At other times, transitions on H1(H3) are ignored. The H2S(H4S) status bit is always clear. When H12 enable (H34 enable) in the port general control register is clear, H2(H4) is held negated.
5. H2(H4) may be an output pin in the pulsed input handshake protocol. It is asserted exactly as in the interlocked input protocol above, but never remains asserted longer than four clock cycles. Typically, a four clock cycle pulse is generated. But in the case of a subsequent H1(H3) asserted edge occurring before termination of the pulse, H2(H4) is negated asynchronously. Thus, anytime after the leading edge of the H2(H4) pulse, new data may be entered in the double-buffered input latches. The H2S(H4S) status bit is always clear. When H12 enable (H34 enable) is clear, H2(H4) is held negated.

For pins used as outputs, the data path consists of a single latch driving the output buffer. Data written to the port's data register does not affect the operation of any handshake pin or status bit. Output pins may be used independently of the input transfers. However, read bus cycles to the data register do remove data from the port. Therefore, care should be taken to avoid processor instructions that perform unwanted read cycles.

Programmable Options Mode 0 — Port A Submode 00 and Port B Submode 00 (Sheet 1 of 2)

PACR 7 6	Port A Submode
0 0	Submode 00

PACR 5 4 3	H2 Control
0 X X	Input pin — edge-sensitive status input, H2S is set on an asserted edge.
1 0 0	Output pin — negated, H2S is always clear.
1 0 1	Output pin — asserted, H2S is always clear.
1 1 0	Output pin — interlocked input handshake protocol, H2S is always clear.
1 1 1	Output pin — pulsed input handshake protocol, H2S is always clear.

PACR 2	H2 Interrupt Enable
0	The H2 interrupt is disabled.
1	The H2 interrupt is enabled.

Programmable Options Mode 0 — Port A Submode 00 and Port B Submode 00 (Sheet 2 of 2)

PACR

1	**H1 SVCR Enable**
0	The H1 interrupt and DMA request are disabled.
1	The H1 interrupt and DMA request are enabled.

PACR

0	**H1 Status Control**
X	The H1S status bit is set anytime input data is present in the double-buffered input path.

PBCR

7 6	**Port B Submode**
0 0	Submode 00

PBCR

5 4 3	**H4 Control**
0 X X	Input pin — edge-sensitive status input, H4S is set on an asserted edge.
1 0 0	Output pin — negated, H4S is always cleared.
1 0 1	Output pin — asserted, H4S is always cleared.
1 1 0	Output pin — interlocked input handshake protocol, H4S is always cleared.
1 1 1	Output pin — pulsed input handshake protocol, H4S is always cleared.

PBCR

2	**H4 Interrupt Enable**
0	The H4 interrupt is disabled.
1	The H4 interrupt is enabled.

PBCR

1	**H3 SVCRQ Enable**
0	The H3 interrupt and DMA request are disabled.
1	The H3 interrupt and DMA request are enabled.

PBCR

0	**H3 Status Control**
X	The H3S status bit is set anytime input data is present in the double-buffered input path.

3.3.2 Submode 01 — Pin-Definable Double-Buffered Output or Non-Latched Input

In mode 0, double-buffered output transfers of up to eight bits are available by programming submode 01 in the desired port's control register. The operation of H2 and H4 may be selected by programming the port A and B control registers, respectively. Data, written by the bus master to the PI/T, is stored in the port's output latches. The peripheral accepts the data by asserting H1(H3), which causes the next data to be moved to the port's output latch as soon as it is available.

The H1S(H3S) status bit may be programmed for two interpretations:

1. The H1S(H3S) status bit is set when either the port initial or final output latch can accept new data. It is cleared when both latches are full and cannot accept new data.
2. The H1S(H3S) status bit is set when both of the port output latches are empty. It is cleared when at least one latch is full.

The programmable options of the H2(H4) pin are:

1. H2(H4) may be an edge-sensitive input pin independent of H1(H3) and the transfer of port data. On the asserted edge of H2(H4), the H2S(H4S) status bit is set. It is cleared by either the

$\overline{\text{RESET}}$ pin being asserted, writing a one to the particular status bit in the port status register (PSR), or when the H1(H2) enable (H3(H4) enable) bit of the port general control register is clear.

2. H2(H4) may be a general-purpose output pin that is always negated. The H2S(H4S) status bit is always clear.
3. H2(H4) may be a general-purpose output pin that is always asserted. The H2S(H4S) status bit is always clear.
4. H2(H4) may be an output pin in the interlocked output handshake protocol. H2(H4) is asserted two clock cycles after data is transferred to the double-buffered output latches. The data remains stable at the port pins and H2(H4) remains asserted until the next asserted edge of the H1(H3) input. At that time, H2(H4) is asynchronously negated. As soon as the next data is available, it is transferred to the output latches. When H2(H4) is negated, asserted transitions of H1(H3) have no affect on data paths. The H2S(H4S) status bit is always clear. When H12 enable (H34 enable) is clear, H2(H4) is held negated.
5. H2(H4) may be an output pin in the pulsed output handshake protocol. It is asserted exactly as in the interlocked protocol above, but never remains asserted longer than four clock cycles. Typically, a four clock pulse is generated. But in the case that a subsequent H1(H3) asserted edge occurs before termination of the pulse, H2(H4) is negated asynchronously shortening the pulse. The H3S(H4S) status bit is always clear. When H12 enable (H34 enable) is clear H2(H4) is held negated.

For pins used as inputs, data written to the associated data register is double-buffered and passed to the initial or final output latch, but, the output buffer is disabled.

Programmable Options Mode 0 — Port A Submode 01 and Port B Submode 01 (Sheet 1 of 2)

PACR 7 6	Port A Submode
0 1	Submode 01

PACR 5 4 3	H2 Control
0 X X	Input pin — edge-sensitive status input, H2S is set on an asserted edge.
1 0 0	Output pin — negated, H2S is always clear.
1 0 1	Output pin — asserted, H2S is always clear.
1 1 0	Output pin — interlocked input handshake protocol, H2S is always clear.
1 1 1	Output pin — pulsed input handshake protocol, H2S is always clear.

PACR 2	H2 Interrupt Enable
0	The H2 interrupt is disabled.
1	The H2 interrupt is enabled.

PACR 1	H1 SVCRQ Enable
0	The H1 interrupt and DMA request are disabled.
1	The H1 interrupt and DMA request are enabled.

Programmable Options Mode 0 — Port A Submode 01 and Port B Submode 01 (Sheet 2 of 2)

PACR

0	H1 Status Control
0	The H1S status bit is set when either the port A initial or final output latch can accept new data. It is clear when both latches are full and cannot accept new data.
1	The H1S status bit is one when both of the port A output latches are empty. It is clear when at least one latch is full.

PBCR

7 6	Port B Submode
0 1	Submode 01

PBCR

5 4 3	H4 Control
0 X X	Input pin — edge-sensitive status input, H4S is set on an asserted edge.
1 0 0	Output pin — negated, H4S is always cleared.
1 0 1	Output pin — asserted, H4S is always cleared.
1 1 0	Output pin — interlocked input handshake protocol, H4S is always cleared.
1 1 1	Output pin — pulsed input handshake protocol, H4S is always cleared.

PBCR

2	H4 Interrupt Enable
0	The H4 interrupt is disabled.
1	The H4 interrupt is enabled.

PBCR

1	H3 SVCRQ Enable
0	The H3 interrupt and DMA request are disabled.
1	The H3 interrupt and DMA request are enabled.

PBCR

0	H3 Status Control
0	The H3S status bit is set when either the port B initial or final output latch can accept new data. It is clear when both latches are full and cannot accept new data.
1	The H3S status bit is one when both of the port B output latches are empty. It is clear when at least one latch is full.

3.3.3 Submode 1X — Bit I/O (Pin-Definable Single-Buffered Output or Non-Latched Input)

In mode 0, simple bit I/O is available by programming submode 1X in the desired port's control register. This submode is intended for applications in which several independent devices must be controlled or monitored. Data written to the associated (input/output) register is single buffered. If the data direction register bit for that pin is a one (output), the output buffer is enabled. If it is a zero (input), data written is still latched, but is not available at the pin. Data read from the data register is the instantaneous value of the pin or what was written to the data register, depending on the contents of the data direction register. H1(H3) is an edge-sensitive status input pin only and it controls no data related function. The H1S(H3S) status bit is set following the asserted edge of the input waveform. It is cleared by either the $\overline{\text{RESET}}$ pin being asserted, writing a one to the associated status bit in the port status register (PSR), or when the H12 enable (H34 enable) bit of the port general control register is clear. H2 may be programmed as:

1. H2(H4) may be an edge-sensitive status input that is independent of H1(H3) and the transfer of port data. On the asserted edge of H2(H4), the H2S(H4S) status bit is set. It is cleared by either the $\overline{\text{RESET}}$ pin being asserted, writing a one to the particular status bit in the port status

register (PSR), or when the H12 enable (H34 enable) bit of the port general control register is clear.

2. H2(H4) may be a general-purpose output pin that is always negated. In this case the H2S(H4S) status bit is always clear.
3. H2(H4) may be a general-purpose output pin that is always asserted. In this case the H2S(H4S) status bit is always clear.

Programmable Option Mode 0 — Port A Submode 1X and Port B Submode 1X (Sheet 1 of 2)

PACR 7 6	Port A Submode
1 X	Submode 1X

PACR 5 4 3	H2 Control
0 X X	Input pin — edge-sensitive status input, H2S is set on an asserted edge.
1 X 0	Output pin — negated, H2S is always cleared.
1 X 1	Output pin — asserted, H2S is always cleared.

PACR 2	H2 Interrupt Enable
0	The H2 interrupt is disabled.
1	The H2 interrupt is enabled.

PACR 1	H1 SVCRQ Enable
0	The H1 interrupt is disabled.
1	The H1 interrupt is enabled.

PACR 0	H1 Status Control
X	H1 is an edge-sensitive status input, H1S is set by an asserted edge of H1.

PBCR 7 6	Port B Submode
1 X	Submode 1X

PBCR 5 4 3	H4 Control
0 X X	Input pin — edge-sensitive status input, H4S is set on an asserted edge.
1 X 0	Output pin — negated, H4S is always cleared.
1 X 1	Output pin — asserted, H4S is always cleared.

PBCR 2	H4 Interrupt Enable
0	The H4 interrupt is disabled.
1	The H4 interrupt is enabled.

PBCR 1	H3 SVCRQ Enable
0	The H3 interrupt is disabled.
1	The H3 interrupt is enabled.

Programmable Options Mode 0 — Port A Submode 1X and Port B Submode 1X (Sheet 2 of 2)

PBCR	
0	**H3 Status Control**
X	H3 is an edge-sensitive status input, H3S is set by an asserted edge of H3.

3.4 MODE 1 — UNIDIRECTIONAL 16-BIT MODE

In mode 1, ports A and B are concatenated to form a single 16-bit port. The port B submode field controls the configuration of both ports. The possible submodes are:

Port B Submode X0 — Pin-Definable Double-Buffered Input or Single-Buffered Output

Port B Submode X1 — Pin-Definable Double-Buffered Output or Non-Latched Input

Handshake pins H3 and H4, configured by programming the port B control register, are associated with the 16-bit double-buffered transfer. These 16-bit transfers are enabled by setting the H34 enable bit in the port general control register (PGCR). Handshake pins H1 and H2 may be used as simple status inputs not related to the 16-bit data transfer or H2 may be an output. Enabling of the H1 and H2 handshake pins is done by setting the H12 enable bit of the port general control register. The port A and B data direction registers operate in each submode. Along with the submode, they affect the data read and written at the data register according to Table 3-2. The data direction register also enables the output buffer associated with each port pin. The $\overline{\text{DMAREQ}}$ pin may be associated only with H3.

Table 3-2. Mode 1 Port Data Paths

Mode	Read Port A/B Register		Write Port A/B Register	
	DDR = 0	DDR = 1	DDR = 0	DDR = 1
1, Port B Submode X0	FIL, D.B.	FOL Note 3	FOL, S.B. Note 2	FOL, S.B. Note 2
1, Port B Submode X1	Pin	FOL Note 3	IOL/FOL, D.B., Note 1	IOL/FOL, D.B., Note 1

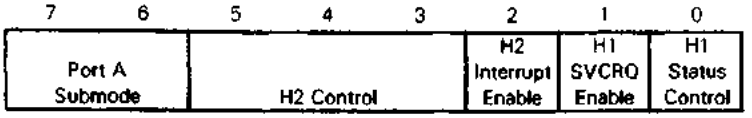
Note 1: Data written to Port A goes to a temporary latch. When the Port B data register is later written, Port A data is transferred to IOL/FOL.
Note 2: Data is latched in the output data registers (final output latch) and will be single buffered at the pin if the DDR is 1. The output buffers will be turned off if the DDR is 0.
Note 3: The output drivers that connect the final output latch to the pins are turned on.

Abbreviations:
IOL — Initial Output Latch
FOL — Final Output Latch
FIL — Final Input Latch
S.B. — Single Buffered
D.B. — Double Buffered
DDR — Data Direction Register

Mode 1 can provide convenient high-speed 16-bit transfers. The port A and port B data registers are addressed for compatibility with the MC68000 move peripheral (MOVEP) instruction and with the MC68450 direct memory access controller (DMAC). To take advantage of this, port A should contain the most-significant byte of data and always be read or written by the bus master first. The interlocked and pulsed handshake protocols, status bits, and $\overline{\text{DMAREQ}}$ are keyed to the access of port B data register in mode 1. Transfers proceed properly with interlocked or pulsed handshakes when the port B data register is accessed last.

3.4.1 Port A Control Register

Port A Control Register (PACR)

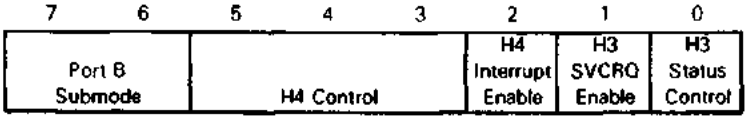


The port A control register, in conjunction with the programmed mode and the port B submode, controls the operation of port A and the handshake pins H1 and H2. The port A control register contains five fields: bits 7 and 6 specify the port A submode; bits 5, 4, and 3 control the operation of the H2 handshake pin and H2S status bit; bit 2 determines whether an interrupt will be generated when the H2S status bit goes to one; bit 1 determines whether a service request (interrupt request or DMA request) will occur; and bit 0 controls the operation of the H1S status bit. The PACR is always readable and writable. There is never a consequence to reading the register.

All bits are cleared to zero when the $\overline{\text{RESET}}$ pin is asserted. When the port A submode field is relevant in a mode/submode definition, it must not be altered unless the H12 enable bit in the port general control register is clear (see Table 1-3 located on foldout pages 1 and 2 at the end of this document). Altering these bits may give unpredictable results if the H12 enable bit in the PGCR is set.

3.4.2 Port B Control Register

Port B Control Register (PBCR)



The port B control register specifies the operation of port B and the handshake pins H3 and H4. The port B control register contains five fields: bits 7 and 6 specify the port B submode; bits 5, 4, and 3 control the operation of the H4 handshake pin and H4S status bit goes to a one; bit 1 determines whether a service request (interrupt request or DMA request) will occur; and bit 0 controls the operation of the H3S status bit. The PBCR is always readable and writable.

All bits are cleared to zero when the $\overline{\text{RESET}}$ pin is asserted. When the port B submode field is relevant in a mode/submode definition, it must not be altered unless the H34 enable bit in the port general control register is clear (see Table 1-3 located on foldout pages 1 and 2 at the end of this document). Altering these bits may give unpredictable results if the H12 enable bit in the PGCR is set.

3.4.3 Submode X0 — Pin-Definable Double-Buffered Input or Single-Buffered Output

In mode 1 submode X0, double-buffered input transfers of up to 16 bits may be obtained. The level of each pin is asynchronously latched with the asserted edge of H3 and placed in the initial input latch or the final input latch. The processor may check the H3S status bit to determine if new data is present. The $\overline{\text{DMAREQ}}$ pin may be used to signal a DMA controller to empty the input buffers. Regardless of the bus master, port A data should be read first and port B data should be read last. The operation of the internal handshake controller, the H3S bit, and the $\overline{\text{DMAREQ}}$ are keyed to the reading of the port B data register. (The MC68450 DMAC can be programmed to perform the exact transfers needed for compatibility with the PI/T.) H4 may be programmed as:

1. H4 may be an edge-sensitive status input that is independent of H3 and the transfer of port data. On the asserted edge of H4, the H4S status bit is set. It is cleared by either the $\overline{\text{RESET}}$ pin being asserted, writing a one to the particular status bit in the port status register (PSR), or when the H34 enable bit of the port general control register is clear.
2. H4 may be a general-purpose output pin that is always negated. In this case the H4S status bit is always clear.
3. H4 may be a general-purpose output pin that is always asserted. In this case the H4S status bit is always clear.
4. H4 may be an output pin in the interlocked input handshake protocol. It is asserted when the port input latches are ready to accept new data. It is negated asynchronously following the asserted edge of the H3 input. As soon as the input latches become ready, H4 is again asserted. When the input double-buffered latches are full, H4 remains negated until data is removed. Thus, anytime the H4 output is asserted, new input data may be entered by asserting H3. At other times transitions on H3 are ignored. The H4S status bit is always clear. When H34 enable in the port general control register is clear, H4 is held negated.
5. H4 may be an output pin in the pulsed input handshake protocol. It is asserted exactly as in the interlocked input protocol above, but never remains asserted longer than four clock cycles. Typically, a four clock cycle pulse is generated. But in the case that a subsequent H3 asserted edge occurs before termination of the pulse, H4 is negated asynchronously. Thus, anytime after the leading edge of the H4 pulse, new data may be entered in the double-buffered input latches. The H4S status bit is always clear. When H34 enable is clear, H4 is held negated.

For pins used as outputs, the data path consists of a single latch driving the output buffer. Data written to the port's data register does not affect the operation of any handshake pin, status bit, or any other aspect of the PI/T. Thus, output pins may be used independently of the input transfer.

The programmable options of the H2 pin are:

1. H2 may be an edge-sensitive input pin independent of H1 and the transfer of port data. On the asserted edge of H2, the H2S status bit is set. It is cleared by either the $\overline{\text{RESET}}$ pin being asserted, writing a one to the particular status bit in the port status register (PSR), or when the H12 enable bit of the port general control register is clear.
2. H2 may be a general-purpose output pin that is always negated. The H2S status bit is always clear.
3. H2 may be a general-purpose output pin that is always asserted. The H2S status bit is always clear.

Programmable Options Mode 1 — Port A Submode XX and Port B Submode X0

PACR

7 6	Port A Submode
0 0	Submode XX

PACR

5 4 3	H2 Control
0 X X	Input pin — edge-sensitive status input, H2S is set on an asserted edge.
1 X 0	Output pin — negated, H2S is always cleared.
1 X 1	Output pin — asserted, H2S is always cleared.

PACR

2	H2 Interrupt Enable
0	The H2 interrupt is disabled.
1	The H2 interrupt is enabled.

PACR

1	H1 SVCRQ Enable
0	The H1 interrupt is disabled.
1	The H1 interrupt is enabled.

PACR

0	H1 Status Control
X	H1 is an edge-sensitive status input. H1S is set by an asserted edge of H1.

PBCR

7 6	Port B Submode
0 0	Submode X0

PBCR

5 4 3	H4 Control
0 X X	Input pin — edge-sensitive status input, H4S is set on an asserted edge.
1 0 0	Output pin — negated, H4S is always cleared.
1 0 1	Output pin — asserted, H4S is always cleared.
1 1 0	Output pin — interlocked input handshake protocol.
1 1 1	Output pin — pulsed input handshake protocol.

PBCR

2	H2 Interrupt Enable
0	The H4 interrupt is disabled.
1	The H4 interrupt is enabled.

PBCR

1	H3 SVCRQ Enable
0	The H3 interrupt and DMA request are disabled.
1	The H3 interrupt and DMA request are enabled.

PBCR

0	H3 Status Control
X	The H3S status bit is set anytime input data is present in the double-buffered input path.

3.4.4 Submode X1 — Pin-Definable Double-Buffered Output or Non-Latched Input

In mode 1 submode X1, double-buffered output transfers of up to 16 bits may be obtained. Data is written by the bus master (processor or DMA controller) in two bytes. The first byte (most significant) is written to the port A data register. It is stored in a temporary latch until the next byte is written to the port B data register. Then all 16 bits are transferred to one of the output latches of ports A and B. The $\overline{\text{DMAREQ}}$ pin may be used to signal a DMA controller to transfer another word to the port output latches. (The MC68450 DMAC can be programmed to perform the exact transfers needed for compatibility with the PI/T.) H4 may be programmed as:

1. H4 may be an edge-sensitive status input that is independent of H3 and the transfer of port data. On the asserted edge of H4, the H4S status bit is set. It is cleared by either the $\overline{\text{RESET}}$ pin being asserted, writing a one to the particular status bit in the port status register (PSR), or when the H34 enable bit of the port general control register is clear.
2. H4 may be a general-purpose output pin that is always negated. In this case the H4S status bit is always clear.
3. H4 may be a general-purpose output pin that is always asserted. In this case the H4S status bit is always clear.
4. H4 may be an output pin in the interlocked output handshake protocol. H4 is asserted two clock cycles after data is transferred to the double-buffered output latches. The data remains stable at the port pins and H4 remains asserted until the next asserted edge of the H3 input. At that time, H4 is asynchronously negated. As soon as the next data is available, it is transferred to the output latches. When H4 is negated, asserted transitions of H3 have no affect on data paths. The H4S status bit is always clear. When H34 enable is clear, H4 is held negated.
5. H4 may be an output pin in the pulsed output handshake protocol. It is asserted exactly as in the interlocked protocol above, but never remains asserted longer than four clock cycles. Typically, a four clock pulse is generated. But in the case that a subsequent H3 asserted edge occurs before termination of the pulse, H4 is negated asynchronously shortening the pulse. The H4S status bit is always cleared. When H34 enable is clear, H4 is held negated.

The H3S status bit may be programmed for two interpretations:

1. The H3S status bit is set when either the port initial or final output latch can accept new data. It is clear when both latches are full and cannot accept new data.
2. The H3S status bit is set when both of the port output latches are empty. It is clear when at least one latch is full.

The programmable options of the H2 pin are:

1. H2 may be an edge-sensitive input pin independent of H1 and the transfer of port data. On the asserted edge of H2, the H2S status bit is set. It is cleared by either the $\overline{\text{RESET}}$ pin being asserted, writing a one to the particular status bit in the port status register (PSR), or when the H12 enable bit of the port general control register is clear.
2. H2 may be a general-purpose output pin that is always negated. The H2S status bit is always clear.
3. H2 may be a general-purpose output pin that is always asserted. The H2S status bit is always clear.

For pins used as inputs, data written to either data register is double buffered and passed to the initial or final output latch, as usual, but the output buffer is disabled (refer to **3.3.2 Submode 01 — Pin-Definable Double-Buffered Output or Non-Latched Input**).

Programmable Options Mode 1 — Port A Submode XX and Port B Submode X1 (Sheet 1 of 2)

PACR 7 6	Port A Submode
0 0	Submode XX

PACR 5 4 3	H2 Control
0 X X	Input pin — edge-sensitive status input, H2S is set on an asserted edge.
1 X 0	Output pin — negated, H2S is always cleared.
1 X 1	Output pin — asserted, H2S is always cleared.

PACR 2	H2 Interrupt Enable
0	The H2 interrupt is disabled.
1	The H2 interrupt is enabled.

PACR 1	H1 SVCRQ Enable
0	The H1 interrupt is disabled.
1	The H1 interrupt is enabled.

PACR 0	H1 Status Control
X	H1 is an edge-sensitive status input. H1S is set by an asserted edge of H1.

PBCR 7 6	Port B Submode
0 0	Submode X1

PBCR 5 4 3	H4 Control
0 X X	Input pin — edge-sensitive status input, H4S is set on an asserted edge.
1 0 0	Output pin — negated, H4S is always cleared.
1 0 1	Output pin — asserted, H4S is always cleared.
1 1 0	Output pin — interlocked input handshake protocol.
1 1 1	Output pin — pulsed input handshake protocol.

PBCR 2	H4 Interrupt Enable
0	The H4 interrupt is disabled.
1	The H4 interrupt is enabled.

Programmable Options Mode 1 — Port A Submode XX and Port B Submode X1 (Sheet 2 of 2)

PBCR
1 **H3 SVCRQ Enable**
0 The H3 interrupt and DMA request are disabled.
1 The H3 interrupt and DMA request are enabled.

PBCR
0 **H3 Status Control**
0 The H3S status bit is set when either the initial or final output latch of ports A and B can accept new data. It is clear when both latches are full and cannot accept new data.
1 The H3S status bit is set when both the initial and final output latches of ports A and B are empty. The H3S status bit is clear when at least one set of output latches is full.

3.5 MODE 2 — BIDIRECTIONAL 8-BIT MODE

In mode 2, port A is used for bit I/O with no associated handshake pins. Port B is used for bidirectional 8-bit double-buffered transfers. H1 and H2, enabled by the H12 enable bit in the port general control register, control output transfers, while H3 and H4, enabled by the port general control register bit H34 enable, control input transfers. The instantaneous direction of the data is determined by the H1 handshake pin. The port B data direction register is not used. The port A and port B submode fields do not affect PI/T operation in mode 2.

3.5.1 Port A Bit I/O (Pin-Definable Single-Buffered Output or Non-Latched Input)

Mode 2, port A performs simple bit I/O with no associated handshake pins. This configuration is intended for applications in which several independent devices must be controlled or monitored. Data written to the port A data register is single buffered. If the port A data direction register bit for that pin is set (output), the output buffer is enabled. If it is zero (input), data written is still latched but not available at the pin. Data read from the data register is either the instantaneous value of the pin (if data is stable from CS asserted to DTACK asserted, data on these pins will be guaranteed valid in the data register) or what was written to the data register, depending on the contents of the port A data direction register. This is summarized in Table 3-3.

Table 3-3. Mode 2 Port A Data Paths

Mode	Read Port A Data Register		Write Port A Data Register	
	DDR = 0	DDR = 1	DDR = 0	DDR = 1
2	Pin	FOL	FOL	FOL, S.B.

Abbreviations:
S.B. – Single Buffered
FOL – Final Output Latch
DDR – Data Direction Register

3.5.2 Port B — Double-Buffered Bidirectional Data

The output buffers of port B are controlled by the level of H1. When H1 is negated, the port B output buffers (all eight) are enabled and the pins drive the bidirectional bus. Generally, H1 is negated by the peripheral in response to an asserted H2, which indicates that new output data is present in the double-buffered latches. Following acceptance of the data, the peripheral asserts H1, disabling the port B output buffers. Other than controlling the output buffers, H1 is edge-sensitive as in other modes.

3.5.2.1 DOUBLE-BUFFERED INPUT TRANSFERS. Port B input data that meets the port setup and hold times is latched on the asserted edge of H3 and placed in the initial input latch or the final input latch. H3 is edge-sensitive, and may assume any duty-cycle as long as both high and low minimum times are observed. The PI/T contains a port status register whose H3S status bit is set anytime any input data that has not been read by the bus master is present in the double-buffered latches. The action of H4 is programmable and can be programmed as:

1. H4 may be an output pin in the interlocked input handshake protocol. It is asserted when the port input latches are ready to accept new data. It is negated asynchronously following the asserted edge of the H3 input. As soon as the input latches become ready, H4 is again asserted. When the input double-buffered latches are full, H4 remains negated until data is removed. Thus, anytime the H4 output is asserted, new input data may be entered by asserting H3. At other times transitions on H3 are ignored. The H4S status bit is always clear. When H34 enable in the port general control register is clear, H4 is held negated.
2. H4 may be an output pin in the pulsed input handshake protocol. It is asserted exactly as in the interlocked input protocol above, but never remains asserted longer than four clock cycles. Typically, a four clock cycle pulse is generated. But in the case that a subsequent H3 asserted edge occurs before termination of the pulse, H4 is negated asynchronously. Thus, anytime after the leading edge of the H4 pulse, new data may be entered in the double-buffered input latches. The H4S status bit is always clear. When H34 enable is clear, H4 is held negated.

3.5.2.2 DOUBLE-BUFFERED OUTPUT TRANSFERS. Data, written by the bus master to the PI/T, is stored in the port's output latch. The peripheral accepts the data by asserting H1, which causes the next data to be moved to the port's output latch as soon as it is available. The H1S status bit, in the port status register, may be programmed for two interpretations. Normally the status bit is a one when there is at least one latch in the double-buffered data path that can accept new data. After writing one byte of data to the ports, an interrupt service routine could check this bit to determine if it could store another byte; thus filling both latches. When the bus master is finished, it is often useful to be able to check whether all of the data has been transferred to the peripheral. The H1S status control bit of the port A control register provides this flexibility. The H1S status bit is set when both output latches are empty. The programmable options for H2 are:

1. H2 may be an output pin in the interlocked output handshake protocol. It is asserted when the port output latches are ready to transfer new data. It is negated asynchronously following the asserted edge of the H1 input. As soon as the output latches become ready, H2 is again asserted. When the output double-buffered latches are full, H2 remains asserted until data is removed. Thus, anytime the H2 output is asserted, new output data may be transferred by asserting H1. At other times transitions on H1 are ignored. The H2S status bit is always clear. When H12 enable in the port general control register is clear, H2 is held negated.
2. H2 may be an output pin in the pulsed output handshake protocol. It is asserted exactly as in the interlocked input protocol above, but never remains asserted longer than four clock cycles. Typically, a four clock cycle pulse is generated. But in the case that a subsequent H1 asserted edge occurs before termination of the pulse, H2 is negated asynchronously. Thus, anytime after the leading edge of the H2 pulse, new data may be transferred to the double-buffered output latches. The H2S status bit is always clear. When H12 enable is clear, H2 is held negated.

The $\overline{\text{DMAREQ}}$ pin may be associated with either input transfers (H3) or output transfers (H1), but not both. Refer to Table 3-4 for a summary of the port B data register responses in mode 2.

Table 3-4. Mode 2 Port B Data Paths

Mode	Read Port B Data Register	Write Port B Data Register
2	FIL, D.B.	IOL/FOL, D.B.

Abbreviations:
IOL – Initial Output Latch
FOL – Final Output Latch
FIL – Final Input Latch
D.B. – Double Buffered

Programmable Options Mode 2 – Port A Submode XX and Port B Submode XX (Sheet 1 of 2)

PACR
7 6 **Port A Submode**
X X Submode XX

PACR
5 4 3 **H2 Control**
X X 0 Output pin – interlocked output handshake protocol, H2S is always cleared.
X X 1 Output pin – pulsed output handshake protocol, H2S is always cleared.

PACR
2 **H2 Interrupt Enable**
0 The H2 interrupt is disabled.
1 The H2 interrupt is enabled.

PACR
1 **H1 SVCRQ Enable**
0 The H1 interrupt and DMA request are disabled.
1 The H1 interrupt and DMA request are enabled.

PACR
0 **H1 Status Control**
0 The H1 status bit is set when either the port B initial or final output latch can accept new data. It is clear when both latches are full and cannot accept new data.
1 The H1S status bit is set when both of the port B output latches are empty. It is clear when at least one latch is full.

PBCR
7 6 **Port B Submode**
X X Submode XX

PBCR
5 4 3 **H4 Control**
X X 0 Output pin – interlocked input handshake protocol, H4S is always cleared.
X X 1 Output pin – pulsed input handshake protocol, H4S is always cleared.

PBCR
2 **H4 Interrupt Enable**
0 The H4 interrupt is disabled.
1 The H4 interrupt is enabled.

Programmable Options Mode 2 — Port A Submode XX
and Port B Submode XX (Sheet 2 of 2)

PBCR	H3 SVCRQ Enable
0	The H3 interrupt and DMA request are disabled.
1	The H3 interrupt and DMA request are enabled.

PBCR	H3 Status Control
X	The H3S status bit is set anytime input data is present in the double-buffered input path.

3.6 MODE 3 — BIDIRECTIONAL 16-BIT MODE

In mode 3, ports A and B are used for bidirectional 16-bit double-buffered transfers. H1 and H2 control output transfers, while H3 and H4 control input transfers. H1 and H2 are enabled by the H12 enable bit while H3 and H4 are enabled by the H34 enable bit of the port general control register. The instantaneous direction of data is determined by the H1 handshake pin, thus, the data direction registers are not used and have no affect. The port A and port B submode fields do not affect PI/T operation in mode 3. Port A and port B output buffers are controlled by the level of H1. When H1 is negated, the output buffers (all 16) are enabled and the pins drive the bidirectional port bus. Generally a peripheral will negate H1 in response to an asserted H2, which indicates that new output data is present in the double-buffered latches. Following acceptance of the data, the peripheral asserts H1, disabling the output buffers. Other than controlling the output buffers, H1 is edge-sensitive as in other modes. The port A and port B data direction registers are not used.

3.6.1 Double-Buffered Input Transfers

Port A and B input data that meets the port setup and hold times is latched on the asserted edge of H3 and placed in the initial input latch or the final input latch. H3 is edge-sensitive, and may assume any duty-cycle as long as both high and low minimum times are observed. The PI/T contains a port status register whose H3S status bit is set anytime any input data is present in the double-buffered latches that has not been read by the bus master. The action of H4 is programmable and can be programmed as:

1. H4 may be an output pin in the interlocked input handshake protocol. It is asserted when the port input latches are ready to accept new data. It is negated asynchronously following the asserted edge of the H3 input. As soon as the input latches become ready, H4 is again asserted. When the input double-buffered latches are full, H4 remains negated until data is removed. Thus, anytime the H4 output is asserted, new input data may be entered by asserting H3. At other times transitions on H3 are ignored. The H4S status bit is always clear. When H34 enable in the port general control register is clear, H4 is held negated.
2. H4 may be an output pin in the pulsed input handshake protocol. It is asserted exactly as in the interlocked input protocol above, but never remains asserted longer than four clock cycles. Typically, a four clock cycle pulse is generated. But in the case that a subsequent H3 asserted edge occurs before termination of the pulse, H4 is negated asynchronously. Thus, anytime after the leading edge of the H4 pulse, new data may be entered in the double-buffered input latches. The H4 status bit is always clear. When H34 enable is clear, H4 is held negated.

3.6.2 Double-Buffered Output Transfers

Data, written by the bus master to the PI/T, is stored in the port's output latch. The peripheral accepts the data by asserting H1, which causes the next data to be moved to the port's output latch as soon as it is available. The H1S status bit, in the port status register, may be programmed for two interpretations. Normally the status bit is a one when there is at least one latch in the double-buffered data path that can accept new data. After writing one byte of data to the ports, an interrupt service routine could check this bit to determine if it could store another byte; thus filling both latches. When the bus master is finished, it is often useful to be able to check whether all of the data has been transferred to the peripheral. The H1S status control bit of the port A control register provides this flexibility. The H1S status bit is set when both output latches are empty. The programmable options for H2 are:

1. H2 may be an output pin in the interlocked output handshake protocol. It is asserted when the port output latches are ready to transfer new data. It is negated asynchronously following the asserted edge of the H1 input. As soon as the output latches become ready, H2 is again asserted. When the output double-buffered latches are full, H2 remains asserted until data is removed. Thus, anytime the H2 output is asserted, new output data may be transferred by asserting H1. At other times transitions on H1 are ignored. The H2S status bit is always clear. When H12 enable in the port general control register is clear, H2 is held negated.
2. H2 may be an output pin in the pulsed output handshake protocol. It is asserted exactly as in the interlocked output protocol above, but never remains asserted longer than four clock cycles. Typically, a four clock pulse is generated. But in the case that a subsequent H1 asserted edge occurs before termination of the pulse, H2 is negated asynchronously shortening the pulse. The H2S status bit is always zero. When H12 enable is zero, H2 is held negated.

Mode 3 can provide convenient high-speed 16-bit transfers. The port A and B data registers are addressed for compatibility with the MC68000's move peripheral (MOVEP) instruction and with the MC68450 DMAC. To take advantage of this, port A should contain the most significant data and always be read or written by the bus master first. The interlocked and pulsed handshake protocols, status bits, and $\overline{\text{DMAREQ}}$ are keyed to the access of port B data register in mode 3. If it is accessed last, the 16-bit double-buffered transfer proceeds smoothly.

The $\overline{\text{DMAREQ}}$ pin may be associated with either input transfers (H3) or output transfers (H1), but not both. Refer to Table 3-5 for a summary of the port A and B data paths in mode 3.

Table 3-5. Mode 3 Port A and B Data Paths

Mode	Read Port A and B Data Register	Write Port A and B Data Register
3	FIL, D.B	IOL/FOL, D.B., Note 1
Note 1: Data written to Port A goes to a temporary latch. When the Port B data register is later written, Port A data is transferred to IOL/FOL.		
Abbreviations: IOL – Initial Output Latch FOL – Final Output Latch FIL – Final Input Latch		S.B – Single Buffered D.B – Double Buffered

Programmable Options Mode 3 — Port A Submode XX and Port B Submode XX

PACR

7 6	Port A Submode
X X	Submode XX

PACR

5 4 3	H2 Control
X X 0	Output pin — interlocked output handshake protocol, H2S status always cleared.
X X 1	Output pin — pulsed output handshake protocol, H2S status always cleared.

PACR

2	H2 Interrupt Enable
0	The H2 interrupt is disabled.
1	The H2 interrupt is enabled.

PACR

1	H1 SVCRQ Enable
0	The H1 interrupt and DMA request are disabled.
1	The H1 interrupt and DMA request are enabled.

PACR

0	H1 Status Control
0	The H1 status bit is set when either the port B initial or final output latch can accept new data. It is clear when both latches are full and cannot accept new data.
1	The H1S status bit is set when both of the port B output latches are empty. It is clear when at least one latch is full.

PBCR

7 6	Port B Submode
X X	Submode XX

PBCR

5 4 3	H4 Control
X X 0	Output pin — interlocked input handshake protocol, H4S is always clear
X X 1	Output pin — pulsed input handshake, H4S is always clear.

PBCR

2	H4 Interrupt Enable
0	The H4 interrupt is disabled.
1	The H4 interrupt is enabled.

PBCR

1	H3 SVCRQ Enable
0	The H3 interrupt and DMA request are disabled.
1	The H3 interrupt and DMA request are enabled.

PBCR

0	H3 Status Control
X	The H3S status bit is set anytime input data is present in the double-buffered input path.

SECTION 4
PROGRAMMER'S MODEL

This section describes the internal accessible register organization as represented in Table 1-3 located on foldout pages 1 and 2 at the end of this document and in Table 4-1. Address space within the address map is reserved for future expansion.

Table 4-1. PI/T Register Addressing Assignments

Register		Register Select Bits					Accessible	Affected by Reset	Affected by Read Cycle
		5	4	3	2	1			
Port General Control Register	(PGCR)	0	0	0	0	0	R W	Yes	No
Port Service Request Register	(PSRR)	0	0	0	0	1	R W	Yes	No
Port A Data Direction Register	(PADDR)	0	0	0	1	0	R W	Yes	No
Port B Data Direction Register	(PBDDR)	0	0	0	1	1	R W	Yes	No
Port C Data Direction Register	(PCDDR)	0	0	1	0	0	R W	Yes	No
Port Interrupt Vector Register	(PIVR)	0	0	1	0	1	R W	Yes	No
Port A Control Register	(PACR)	0	0	1	1	0	R W	Yes	No
Port B Control Register	(PBCR)	0	0	1	1	1	R W	Yes	No
Port A Data Register	(PADR)	0	1	0	0	0	R W	No	**
Port B Data Register	(PBDR)	0	1	0	0	1	R W	No	**
Port A Alternate Register	(PAAR)	0	1	0	1	0	R	No	No
Port B Alternate Register	(PBAR)	0	1	0	1	1	R	No	No
Port C Data Register	(PCDR)	0	1	1	0	0	R W	No	No
Port Status Register	(PSR)	0	1	1	0	1	R W*	Yes	No
Timer Control Register	(TCR)	1	0	0	0	0	R W	Yes	No
Timer Interrupt Vector Register	(TIVR)	1	0	0	0	1	R W	Yes	No
Counter Preload Register High	(CPRH)	1	0	0	1	1	R W	No	No
Counter Preload Register Middle	(CPRM)	1	0	1	0	0	R W	No	No
Counter Preload Register Low	(CPRL)	1	0	1	0	1	R W	No	No
Count Register High	(CNTRH)	1	0	1	1	1	R	No	No
Count Register Middle	(CNTRM)	1	1	0	0	0	R	No	No
Count Register Low	(CNTRL)	1	1	0	0	1	R	No	No
Timer Status Register	(TSR)	1	1	0	1	0	R W*	Yes	No

* A write to this register may perform a special status resetting operation.
** Mode dependent.

R = Read
W = Write

Throughout this section the following conventions are maintained:

1. A read from a reserved location in the map results in a read from the "null register." The null register returns all zeros for data and results in a normal bus cycle. A write to one of these locations results in a normal bus cycle, but written data is ignored.
2. Unused bits of a defined register are denoted by "*" and are read as zeros; written data is ignored.

3. Bits that are unused in the chosen mode/submode but are used in others are denoted by "X", and are readable and writable. Their content, however, is ignored in the chosen mode/submode.
4. All registers are addressable as 8-bit quantities. To facilitate operation with the MOVEP instruction and the DMAC, addresses are ordered such that certain sets of registers may also be accessed as words (two bytes) or long words (four bytes).

4.1 PORT GENERAL CONTROL REGISTER (PGCR)

Port General Control Register (PGCR)

7	6	5	4	3	2	1	0
Port Mode Control		H34 Enable	H12 Enable	H4 Sense	H3 Sense	H2 Sense	H1 Sense

The port general control register controls many of the functions that are common to the overall operation of the ports. The PGCR is composed of three major fields: bits 7 and 6 define the operational mode of ports A and B and affect operation of the handshake pins and status bits; bits 5 and 4 allow a software-controlled disabling of particular hardware associated with the handshake pins of each port; and bits 3-0 define the sense of the handshake pins. The PGCR is always readable and writable.

All bits are reset to zero when the $\overline{\text{RESET}}$ pin is asserted.

The port mode control field should be altered only when the H12 enable and H34 enable bits are zero. Except when mode zero is desired (submode 1X), the port general control register should be written once to establish the mode with the H12 and H34 bits clear. Any other necessary control registers can then be programmed, after which H12 or H34 is set. In order to enable the respective operation(s), the port general control register should be written again.

PGCR
7 6 **Port Mode Control**

0 0 Mode 0 (Unidirectional 8-Bit Mode)
0 1 Mode 1 (Unidirectional 16-Bit Mode)
1 0 Mode 2 (Bidirectional 8-Bit Mode)
1 1 Mode 3 (Bidirectional 16-Bit Mode)

PGCR
5 **H34 Enable**

0 Disabled
1 Enabled

PGCR
4 **H12 Enable**

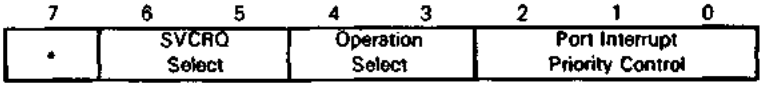
0 Disabled
1 Enabled

PGCR
3-0 **Handshake Pin Sense**

0 The associated pin is at the high-voltage level when negated and at the low-voltage level when asserted.
1 The associated pin is at the low-voltage level when negated and at the high-voltage level when asserted.

4.2 PORT SERVICE REQUEST REGISTER (PSRR)

Port Service Request Register (PSRR)



The port service request register controls other functions that are common to the overall operation to the ports. It is composed of four major fields: bit 7 is unused and is always read as zero; bits 6 and 5 define whether interrupt or DMA requests are generated from activity on the H1 and H3 handshake pins; bits 4 and 3 determine whether two dual-function pins operate as port C or port interrupt request/acknowledge pins; and bits 2, 1, and 0 control the priority among all port interrupt sources. Since bits 2, 1, and 0 affect interrupt operation, it is recommended that they be changed only when the affected interrupt(s) is (are) disabled or known to remain inactive. The PSRR is always readable and writable.

All bits are reset to zero when the $\overline{\text{RESET}}$ pin is asserted.

PSRR
6 5 **SVCRQ Select**

0 X The PC4/$\overline{\text{DMAREQ}}$ pin carries the PC4 function; DMA is not used.

PSRR **SVCRQ Select**

1 0 The PC4/$\overline{\text{DMAREQ}}$ pin carries the $\overline{\text{DMAREQ}}$ function and is associated with double-buffered transfers controlled by H1. H1 is removed from the PI/T's interrupt structure, and thus, does not cause interrupt requests to be generated. To obtain $\overline{\text{DMAREQ}}$ pulses, port A control register bit 1 (H1 SVCRQ enable) must be a one.

1 1 The PC4/$\overline{\text{DMAREQ}}$ pin carries the $\overline{\text{DMAREQ}}$ function and is associated with double-buffered transfers controlled by H3. H3 is removed from the PI/T's interrupt structure, and thus, does not cause interrupt requests to be generated. To obtain $\overline{\text{DMAREQ}}$ pulses, port B control register bit 1 (H3 SVCRQ enable) must be one.

PSRR
4 3 **Interrupt Pin Function Select**

0 0 The PC5/$\overline{\text{PIRQ}}$ pin carries the PC5 function, no interrupt support.
The PC6/$\overline{\text{PIACK}}$ pin carries the PC6 function, no interrupt support.

0 1 The PC5/$\overline{\text{PIRQ}}$ pin carries the $\overline{\text{PIRQ}}$ function, supports autovectored interrupts.
The PC6/$\overline{\text{PIACK}}$ pin carries the PC6 function, supports autovectored interrupts.

1 0 The PC5/$\overline{\text{PIRQ}}$ pin carries the PC5 function.
The PC6/$\overline{\text{PIACK}}$ pin carries the $\overline{\text{PIACK}}$ function.

1 1 The PC5/$\overline{\text{PIRQ}}$ pin carries the $\overline{\text{PIRQ}}$ function, supports vectored interrupts.
The PC6/$\overline{\text{PIACK}}$ pin carries the $\overline{\text{PIACK}}$ function, supports vectored interrupts.

Bits 2, 1, and 0 determine port interrupt priority. The priority as shown in Table 4-2 is in descending order left to right.

Table 4-2. PSRR Port Interrupt Priority Control

2 1 0	Highest			Lowest
0 0 0	H1S	H2S	H3S	H4S
0 0 1	H2S	H1S	H3S	H4S
0 1 0	H1S	H2S	H4S	H3S
0 1 1	H2S	H1S	H4S	H3S

2 1 0	Highest			Lowest
1 0 0	H3S	H4S	H1S	H2S
1 0 1	H3S	H4S	H2S	H1S
1 1 0	H4S	H3S	H1S	H2S
1 1 1	H4S	H3S	H2S	H1S

4.3 PORT DATA DIRECTION REGISTERS

The following paragraphs describe the port data direction registers.

4.3.1 Port A Data Direction Register (PADDR)

The port A data direction register determines the direction and buffering characteristics of each of the port A pins. One bit in the PADDR is assigned to each pin. A zero indicates that the pin is used as a input, while a one indicates it is used as an output. The PADDR is always readable and writable. This register is ignored in mode 3.

All bits are reset to the zero (input) state when the $\overline{\text{RESET}}$ pin is asserted.

4.3.2 Port B Data Direction Register (PBDDR)

The PBDDR is identical to the PADDR for the port B pins and the port B data register, except that this register is ignored in modes 2 and 3.

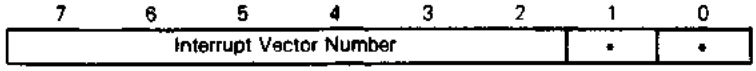
4.3.3 Port C Data Direction Register (PCDDR)

The port C data direction register specifies whether each dual-function pin that is chosen for port C operation is an input (zero) or an output (one) pin. The PCDDR, along with bits that determine the respective pin's function, also specify the exact hardware to be accessed at the port C data register address (see **4.6.3 Port C Data Register (PCDR)** for more details). The PCDDR is an 8-bit register that is readable and writable at all times. Its operation is independent of the chosen PI/T mode.

These bits are cleared to zero when the $\overline{\text{RESET}}$ pin is asserted.

4.4 PORT INTERRUPT VECTOR REGISTER (PIVR)

Port Interrupt Vector Register (PIVR)



The port interrupt vector register contains the upper order six bits of the four port interrupt vectors. The contents of this register may be read two ways: by an ordinary read cycle, or by a port interrupt acknowledge bus cycle. The exact data read depends on how the cycle was initiated and other factors. Behavior during a port interrupt acknowledge cycle is summarized in Table 2-1.

From a normal read cycle, there is never a consequence to reading this register. Following negation of the $\overline{\text{RESET}}$ pin, but prior to writing to the PIVR, a $0F will be read. After writing to the register, the upper six bits may be read and the lower two bits are forced to zero. No prioritization computation is performed.

4.5 PORT CONTROL REGISTERS (PACR, PBCR)

The port A and B control registers (PACR and PBCR) are described in **SECTION 3 PORT MODES.** The description is organized such that for each mode/submode all programmable options of each pin and status bit are given.

4.6 PORT DATA REGISTERS

The following paragraphs describe the port data registers.

4.6.1 Port A Data Register (PADR)

The port A data register is a holding register for moving data to and from the port A pins. The port A data direction register determines whether each pin is an input (zero) or an output (one), and is used in configuring the actual data paths. The data paths are described in **SECTION 3 PORT MODES.**

This register is readable and writable at all times. Depending on the chosen mode/submode, reading or writing may affect the double-buffered handshake mechanism. The port A data register is not affected by the assertion of the $\overline{\text{RESET}}$ pin.

4.6.2 Port B Data Register (PBDR)

The port B data register is a holding register for moving data to and from port B pins. The port B data direction register determines whether each pin is an input (zero) or an output (one), and is used in configuring the actual data paths. The data paths are described in **SECTION 3 PORT MODES.**

This register is readable and writable at all times. Depending on the chosen mode/submode, reading or writing may affect the double-buffered handshake mechanism. The port B data register is not affected by the assertion of the $\overline{\text{RESET}}$ pin.

4.6.3 Port C Data Register (PCDR)

The port C data register is a holding register for moving data to and from each of the eight port C/alternate-function pins. The exact hardware accessed is determined by the type of bus cycle (read or write) and individual conditions affecting each pin. These conditions are: 1) whether the pin is used for the port C or alternate function, and 2) whether the port C data direction register indicates the input or output direction. The port C data register is single buffered for output pins and non-latched for input pins. These conditions are summarized in Table 4-3.

Table 4-3. PCDR Hardware Accesses

Operation	Port C Function		Alternate Function	
	PCDDR = 0	PCDDR = 1	PCDDR = 0	PCDDR = 1
Read Port C Data Register	Pin	Output Register	Pin	Output Register
Write Port C Data Register	Output Register, Buffer Disabled	Output Register, Buffer Enabled	Output Register	Output Register

Note that two additional useful benefits result from this structure. First, it is possible to directly read the state of a dual-function pin while used for the non-port C function. Second, it is possible to generate program controlled transitions on alternate-function pins by switching back to the port C function and writing to the PCDR.

This register is readable and writable at all times and operation is independent of the chosen PI/T mode. The port C data register is not affected by the assertion of the $\overline{\text{RESET}}$ pin.

4.7 PORT ALTERNATE REGISTERS

The following paragraphs describe the port alternate registers.

4.7.1 Port A Alternate Register (PAAR)

The port A alternate register is an alternate register for reading the port A pins. It is a read-only address and no other PI/T condition is affected. In all modes, the instantaneous pin level is read and no input latching is performed except at the data bus interface. Writes to this address are answered with $\overline{DTACK}$, but the data is ignored.

4.7.2 Port B Alternate Register (PBAR)

The port B alternate register is an alternate register for reading the port B pins. It is a read-only address and no other PI/T condition is affected. In all modes, the instantaneous pin level is read and no input latching is performed except at the data bus interface. Writes to this address are answered with $\overline{DTACK}$, but the data is ignored.

4.8 PORT STATUS REGISTER (PSR)

Port Status Register (PSR)

7	6	5	4	3	2	1	0
H4 Level	H3 Level	H2 Level	H1 Level	H4S	H3S	H2S	H1S

The port status register contains information about handshake pin activity. Bits 7-4 show the instantaneous level of the respective handshake pin, and are independent of the handshake pin sense bits in the port general control register. Bits 3-0 are the respective status bits referred to throughout this document. Their interpretation depends on the programmed mode/submode of the PI/T. For bits 3-0 a one is the active or asserted state.

4.9 TIMER CONTROL REGISTER (TCR)

Timer Control Register (TCR)

7	6	5	4	3	2	1	0
TOUT/$\overline{TIACK}$ Control			Z. D. Control	*	Clock Control		Timer Enable

The timer control register (TCR) determines all operations of the timer. Bits 7-5 configure the PC3/TOUT and PC7/$\overline{TIACK}$ pins for port C, square wave, vectored interrupt, or autovectored interrupt operation; bit 4 specifies whether the counter receives data from the counter preload register or continues counting when zero detect is reached; bit 3 is unused and is read as zero; bits 2 and 1 configure the path from the CLK and TIN pins to the counter controller; and bit 0 enables the timer. This register is readable and writable at all times. All bits are cleared to zero when the $\overline{RESET}$ pin is asserted.

TCR 7 6 5	TOUT/TIACK Control
0 0 X	The dual-function pins PC3/TOUT and PC7/$\overline{TIACK}$ carry the port C function.
0 1 X	The dual-function pin PC3/TOUT carries the TOUT function. In the run state it is used as a square-wave output and is toggled on zero detect. The TOUT pin is high while in the halt state. The dual-function pin PC7/$\overline{TIACK}$ carries the PC7 function.

1 0 0 The dual-function pin PC3/TOUT carries the TOUT function. In the run or halt state it is used as a timer interrupt request output. The timer interrupt is disabled; thus, the pin is always three stated. The dual-function pin PC7/$\overline{\text{TIACK}}$ carries the $\overline{\text{TIACK}}$ function; however, since interrupt request is negated, the PI/T produces no response (i.e., no data or DTACK) to an asserted $\overline{\text{TIACK}}$. Refer to **5.1.3 Timer Interrupt Acknowledge Cycles** for details.

1 0 1 The dual-function pin PC3/TOUT carries the TOUT function and is used as a timer interrupt request output. The timer interrupt is enabled; thus, the pin is low when the timer ZDS status bit is one. The dual-function pin PC7/$\overline{\text{TIACK}}$ carries the $\overline{\text{TIACK}}$ function and is used as a timer interrupt acknowledge input. Refer to the **5.1.3 Timer Interrupt Acknowledge Cycles** for details. This combination supports vectored timer interrupts.

1 1 0 The dual-function pin PC3/TOUT carries the TOUT function. In the run or halt state it is used as a timer interrupt request output. The timer interrupt is disabled; thus, the pin is always three-stated. The dual-function pin PC7/$\overline{\text{TIACK}}$ carries the PC7 function.

1 1 1 The dual-function pin PC3/TOUT carries the TOUT function and is used as a timer interrupt request output. The timer interrupt is enabled; thus, the pin is low when the timer ZDS status bit is one. The dual-function pin PC7/$\overline{\text{TIACK}}$ carries the PC7 function and autovectored interrupts are supported.

TCR
4 **Zero Detect Control**

0 The counter is loaded from the counter preload register on the first clock to the 24-bit counter after zero detect, then resumes counting.

1 The counter rolls over on zero detect, then continues counting.

TCR
3 Unused and is always read as zero.

TCR
2 1 **Clock Control**

0 0 The PC2/TIN input pin carries the port C function, and the CLK pin and prescaler are used. The prescaler is decremented on the falling transition of the CLK pin; the 24-bit counter is decremented, rolls over, or is loaded from the counter preload registers when the prescaler rolls over from $00 to $1F. The timer enable bit determines whether the timer is in the run or halt state.

0 1 The PC2/TIN pin serves as a timer input, and the CLK pin and prescaler are used. The prescaler is decremented on the falling transition of the CLK pin; the 24-bit counter is decremented, rolls over, or is loaded from the counter preload registers when the prescaler rolls over from $00 to $1F. The timer is in the run state when the timer enable bit is one and the TIN pin is high; otherwise, the timer is in the halt state.

1 0 The PC2/TIN pin serves as a timer input and the prescaler is used. The prescaler is decremented following the rising transition of the TIN pin after being synchronized with the internal clock. The 24-bit counter is decremented, rolls over, or is loaded from the counter preload registers when the prescaler rolls over from $00 to $1F. The timer enable bit determines whether the timer is in the run or halt state.

1 1 The PC2/TIN pin serves as a timer input and the prescaler is not used. The 24-bit counter is decremented, rolls over, or is loaded from the counter preload registers following the rising edge of the TIN pin after being synchronized with the internal clock. The timer enable bit determines whether the timer is in the run or halt state.

TCR
0 **Timer Enable**

0 Disabled

1 Enabled

4.10 TIMER INTERRUPT VECTOR REGISTER (TIVR)

The timer interrupt vector register contains the 8-bit vector supplied when the timer interrupt acknowledge pin $\overline{\text{TIACK}}$ is asserted. The register is readable and writable at all times, and the same value is always obtained from a normal read cycle or a timer interrupt acknowledge bus cycle ($\overline{\text{TIACK}}$). When the $\overline{\text{RESET}}$ pin is asserted the value of $0F is loaded into the register. Refer to **5.1.3 Timer Interrupt Acknowledge Cycles** for more details.

4.11 COUNTER PRELOAD REGISTER H, M, L (CPRH-L)

Counter Preload Register H, M, L (CPRH-L)

7	6	5	4	3	2	1	0	
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	CPRH
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	CPRM
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	CPRL

The counter preload registers are a group of three 8-bit registers used for storing data to be transferred to the counter. Each of the registers is individually addressable, or the group may be accessed with the MOVEP.L or the MOVEP.W instructions. The address $12 (one less than the address of CPRH) is the null register and is reserved so that zeros are read in the upper eight bits of the destination data register when a MOVEP.L is used. Data written to this address is ignored.

These registers are readable and writable at all times. A read cycle proceeds independently of any transfer to the counter, which may be occurring simultaneously. To insure proper operation of the PI/T timer, a value of $000000 may not be stored in the counter preload registers for use with the counter. The $\overline{\text{RESET}}$ pin does not affect the contents of these registers.

4.12 COUNT REGISTER H, M, L (CNTRH-L)

Count Register H, M, L (CNTRH-L)

7	6	5	4	3	2	1	0	
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	CNTRH
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	CNTRM
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	CNTRL

The count registers are a group of three 8-bit addresses at which the counter can be read. The contents of the counter are not latched during a read bus cycle; thus, the data read at these addresses is not guaranteed if the timer is in the run state. Write operations to these addresses result in a normal bus cycle but the data is ignored.

Each of the registers is individually addressable, or the group may be accessed with the MOVEP.L or the MOVEP.W instructions. The address, one less than the address CNTRH, is the null register and is reserved so that zeros are read in the upper eight bits of the destination data register when a MOVEP.L is used. Data written to this address is ignored.

4.13 TIMER STATUS REGISTER (TSR)

Timer Status Register (TSR)

7	6	5	4	3	2	1	0
•	•	•	•	•	•	•	ZDS

The timer status register contains one bit from which the zero detect status can be determined. The ZDS status bit (bit 0) is an edge-sensitive flip-flop that is set to one when the 24-bit counter decrements from $000001 to $000000. The ZDS status bit is cleared to zero following the direct reset operation or when the timer is halted. Note that when the $\overline{\text{RESET}}$ pin is asserted the timer is disabled, and thus enters the halt state.

This register is always readable without consequence. A write access performs a direct reset operation if bit 0 in the written data is one. Following that, the ZDS bit is zero.

This register is constructed with a reset dominant S-R flip-flop so that all clearing conditions prevail over the possible zero detect condition.

Bits 7-1 are unused and are read as zero.

4.14 REGISTER VALUE AFTER RESET

Table 1-3, located on foldout pages 1 and 2 at the end of this document, shows the values that remain or are changed after a reset. Note that interrupt vector registers are initialized to $0F. For the port interrupt vector register, the only time that bits 0 and 1 are set is after reset.

SECTION 5
TIMER OPERATION AND APPLICATIONS SUMMARY

This section describes the programmable options available, capabilities, and restrictions that apply to the timer. Programming of the timer control register is outlined with several examples given.

5.1 TIMER OPERATION

The MC68230 timer can provide several facilities needed by M68000 operating systems. It can generate periodic interrupts, a square wave, or a single interrupt after a programmed time period. Also, it can be used for elapsed time measurement or as a device watchdog.

The PI/T timer contains a 24-bit synchronous down counter that is loaded from three 8-bit counter preload registers. The 24-bit counter may be clocked by the output of a 5-bit (divide-by-32) prescaler or by an external timer input (TIN). If the prescaler is used, it may be clocked by the system clock (CLK pin) or by the TIN external input. The counter signals the occurrence of an event primarily through zero detection. (A zero is when the counter of the 24-bit timer is equal to zero.) This sets the zero detect status (ZDS) bit in the timer status register. It may be checked by the processor or may be used to generate a timer interrupt. The ZDS bit can be reset by writing a one to the timer status register in that bit position independent of timer operation.

The general operation of the timer is flexible and easily programmable. The timer is fully configured and controlled by programming the 8-bit timer control register (refer to **4.9 TIMER CONTROL REGISTER (TCR)** for additional information). It controls: 1) the choice between the port C operation and the timer operation of three timer pins, 2) whether the counter is loaded from the counter preload register or rolls over when zero detect is reached, 3) the clock input, 4) whether the prescaler is used, and 5) whether the timer is enabled.

5.1.1 Run/Halt Definition

The overall operation of the timer is described in terms of the run or halt states. The control of the current state is determined by programming the timer control register. When in the halt state, all of the following occur:

1. The prior content of the counter is not altered and is reliably readable via the count registers.
2. The prescaler is forced to $1F whether or not it is used.
3. The ZDS status bit is forced to zero, regardless of the possible zero contents of the 24-bit counter.

The run state is characterized by:

1. The counter is clocked by the source programmed in the timer control register.
2. The counter is not reliably readable.
3. The prescaler is allowed to decrement if programmed for use.
4. The ZDS status bit is set when the 24-bit counter transitions from $000001 to $000000.

5.1.2 Timer Rules

The following is a set of rules that allow easy application of the timer.

1. Refer to **5.1.1 Run/Halt Definition**.
2. When the $\overline{\text{RESET}}$ pin is asserted, all bits of the timer control register are cleared, configuring the dual function pins as port C inputs.
3. The contents of the counter preload registers and counter are not affected by the $\overline{\text{RESET}}$ pin.
4. The count registers provide a direct read data path from each portion of the 24-bit counter, but data written to their addresses is ignored. (This results in a normal bus cycle.) These registers are readable at any time, but their contents are never latched. Unreliable data may be read when the timer is in the run state.
5. The counter preload registers are readable and writable at any time and this occurs independently of any timer operation. No protection mechanisms are provided against ill-timed writes.
6. The input frequency to the 24-bit counter from the TIN pin or prescaler output must be between zero and the input frequency at the CLK pin divided by eight, regardless of the configuration chosen.
7. For configurations in which the prescaler is used (with the CLK pin or TIN pin as an input), the contents of the counter preload register (CPR) is transferred to the counter the first time that the prescaler passes from $00 to $1F (rolls over) after entering the run state. Thereafter, the counter decrements, rolls over, or is loaded from the counter preload register each time the prescaler rolls over.
8. For configurations in which the prescaler is not used, the contents of the counter preload registers are transferred to the counter on the first asserted edge of the TIN input after entering the run state. On subsequent asserted edges the counter decrements, rolls over, or is loaded from the counter preload registers.
9. The smallest value allowed in the counter preload register for use with the counter is $000001.

5.1.3 Timer Interrupt Acknowledge Cycles

Several conditions may be present when the timer interrupt acknowledge pin ($\overline{\text{TIACK}}$) is asserted. These conditions affect the PI/T's response and the termination of the bus cycle (see Table 5-1).

Table 5-1. Response to Timer Interrupt Acknowledge

PC3/TOUT Function	Response to Asserted $\overline{\text{TIACK}}$
PC3 – Port C Pin	No Response No $\overline{\text{DTACK}}$
TOUT – Square Wave	No Response No $\overline{\text{DTACK}}$
TOUT – Negated Timer Interrupt Request	No Response No $\overline{\text{DTACK}}$
TOUT – Asserted Timer Interrupt Request	Timer Interrupt Vector Contents $\overline{\text{DTACK}}$ Asserted

5.2 TIMER APPLICATIONS SUMMARY

The following paragraphs outline programming of the timer control register for several typical examples.

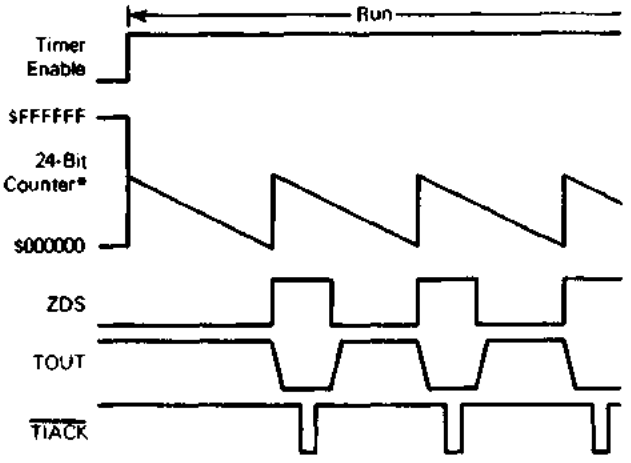
5.2.1 Periodic Interrupt Generator Example

Periodic Interrupt Generator Example

7	6	5	4	3	2	1	0
TOUT/$\overline{\text{TIACK}}$ Control			Z.D. Control	*	Clock Control		Timer Enable
1	X	1	0	0	00 or 1X		Changed

In this configuration the timer generates a periodic interrupt. The TOUT pin is connected to the system's interrupt request circuitry and the $\overline{\text{TIACK}}$ pin may be used as an interrupt acknowledge input to the timer. The TIN pin may be used as a clock input.

The processor loads the counter preload registers (CPR) and timer control register (TCR), and then enables the timer. When the 24-bit counter passes from $000001 to $000000, the ZDS status bit is set and the TOUT (interrupt request) pin is asserted. At the next clock to the 24-bit counter, it is again loaded with the contents of the CPRs and thereafter decrements. In normal operation, the processor must direct clear the status bit to negate the interrupt request (see Figure 5-1).



* Analog representation of counter value.

Figure 5-1. Periodic Interrupt Generator Example

5.2.2 Square Wave Generator

Square Wave Generator

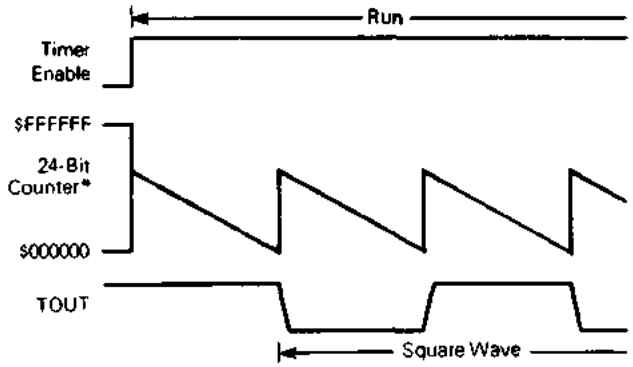
7	6	5	4	3	2	1	0
TOUT/$\overline{\text{TIACK}}$ Control			Z. D. Control	*	Clock Control		Timer Enable
0	1	X	0	0	00 or 1X		Changed

In this configuration the timer produces a square wave at the TOUT pin. The TOUT pin is connected to the user's circuitry and the $\overline{\text{TIACK}}$ pin is not used. The TIN pin may be used as a clock input.

The processor loads the counter preload registers and timer control register, and then enables the timer. When the 24-bit counter passes from $000001 to $000000 the ZDS status bit is set and the

TOUT (square wave output) pin is toggled. At the next clock to the 24-bit counter it is again loaded with the contents of the CPRs, and thereafter decrements. In this application there is no need for the processor to direct clear the ZDS status bit; however, it is possible for the processor to sync itself with the square wave by clearing the ZDS status bit, then polling it. The processor may also read the TOUT level at the port C address.

Note that the PC3/TOUT pin functions as PC3 following the negation of $\overline{\text{RESET}}$. If used in the square wave configuration, a pullup resistor may be required to keep a known level prior to programming. Prior to enabling the timer, TOUT is high (see Figure 5-2).



* Analog representation of counter value.

Figure 5-2. Square Wave Generator Example

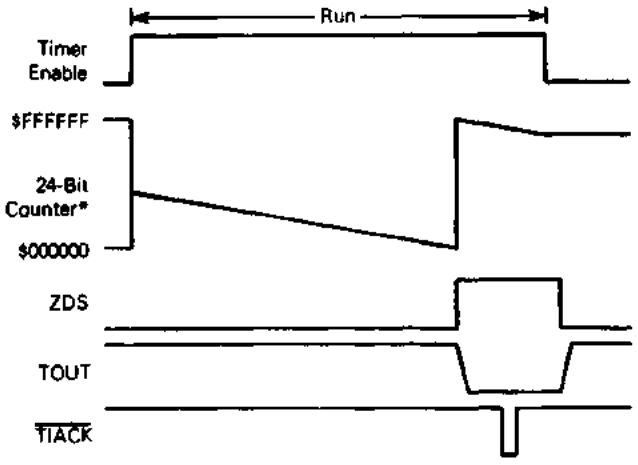
5.2.3 Interrupt After Timeout

Interrupt After Timeout

7	6	5	4	3	2	1	0
TOUT/$\overline{\text{TIACK}}$ Control			Z. D. Control	*	Clock Control		Timer Enable
1	X	1	1	0	00 or 1X		Changed

In this configuration the timer generates an interrupt after a programmed time period has expired. The TOUT pin is connected to the system's interrupt request circuitry and the $\overline{\text{TIACK}}$ pin may be an interrupt acknowledge input to the timer. The TIN pin may be used as a clock input.

This configuration is similar to the periodic interrupt generator except that the zero detect control bit is set. This forces the counter to roll over after zero detect is reached, rather than reloading from the CPRs. When the processor takes the interrupt it can halt the timer, read the counter and calculate the time from the interrupt request to entering the service routine. Accurate knowledge of the interrupt latency may be useful in some applications (see Figure 5-3).



* Analog representation of counter value.

Figure 5-3. Single Interrupt After Timeout Example

5.2.4 Elapsed Time Measurement Examples

Elapsed time measurement takes several forms; two forms are described in the following paragraphs.

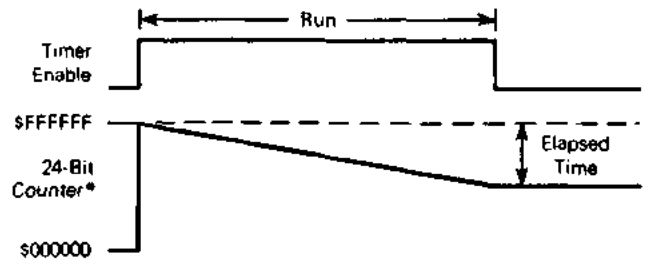
5.2.4.1 SYSTEM CLOCK EXAMPLE. This configuration allows time interval measurement by software. The TIN pin may be used as an external timer enable if desired.

System Clock Example

7	6	5	4	3	2	1	0
TOUT/TIACK Control			Z. D. Control	*	Clock Control		Timer Enable
0	0	X	1	0	0	0	Changed

The processor loads the counter preload registers (generally with all ones), loads the timer control register, and then enables the timer. The counter is allowed to decrement until the ending event takes place. When it is desired to read the time interval, the processor must halt the timer and then read the counter. If TIN is used as an enable, the start and stop counter functions are controlled externally.

For applications in which the interval may exceed the programmed time interval, zero detection can be counted by polling the status register or through interrupts to simulate additional timer bits. Note that the ZDS bit is latched and should be cleared after each detection of zero. At the end, the timer can be halted and read (see Figure 5-4).



* Analog representation of counter value.

Figure 5-4. Elapsed Time Measurement Example

5.2.4.2 EXTERNAL CLOCK. This configuration allows measurement (counting) of the number of input pulses occurring in an interval in which the counter is enabled. The TIN input pin provides the input pulses. Generally the TOUT and $\overline{\text{TIACK}}$ pins are not used.

External Clock

7	6	5	4	3	2	1	0
TOUT/$\overline{\text{TIACK}}$ Control			Z. D. Control	*	Clock Control		Timer Enable
0	0	X	1	0	1	X	Changed

This configuration is similar to the elapsed time measurement/system clock configuration except that the TIN pin is used to provide the input frequency. It can be connected to a simple oscillator and the same methods could be used. Alternately, it could be gated off and on externally and the number of cycles occurring while in the run state can be counted. However, minimum pulse width high and low specifications must be met.

5.2.5 Device Watchdog

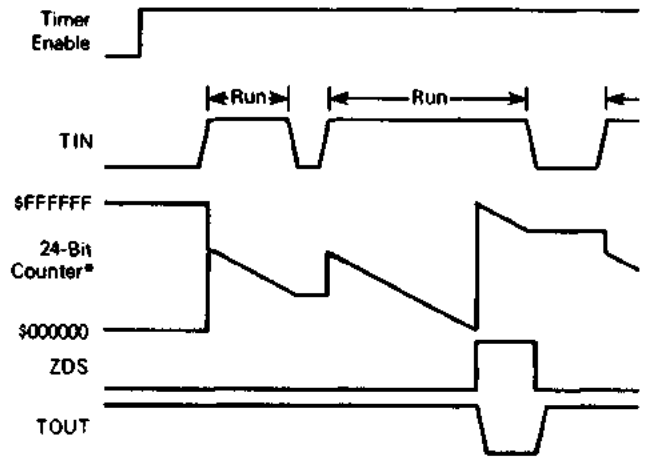
Device Watchdog Example

7	6	5	4	3	2	1	0
TOUT/$\overline{\text{TIACK}}$ Control			Z. D. Control	*	Clock Control		Timer Enable
1	X	1	1	0	0	1	Changed

This configuration provides the watchdog function needed in many systems. The TIN pin is the timer input whose period at the high (one) level is to be checked. Once allowed by the processor, the TIN input pin controls the run/halt mode. The TOUT pin is connected to external circuitry requiring notification when the TIN pin has been asserted longer than the programmed time. The $\overline{\text{TIACK}}$ pin (timer interrupt acknowledge) is only needed if the TOUT pin is connected to the interrupt circuitry.

The processor loads the counter preload register and timer control register, and then enables the timer. When the TIN input is asserted (one, high) the timer transfers the contents of the counter preload register to the counter and begins counting. If the TIN input is negated before zero detect is reached, the TOUT output and the ZDS status bit remain negated. If zero detect is reached while the TIN input is still asserted, the ZDS status bit is set and the TOUT output is asserted. (The counter rolls over and keeps counting.)

In either case, when the TIN input is negated the ZDS status bit is zero, the TOUT output is negated, the counting stops, and the prescaler is forced to all ones (see Figure 5-5).



* Analog representation of counter value.

Figure 5-5. Device Watchdog Example

SECTION 6
ELECTRICAL SPECIFICATIONS

This section contains electrical specifications and associated timing information for the MC68230.

6.1 MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature	T_{stg}	−55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precuations be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

6.2 THERMAL CHARACTERISTICS

Characteristics	Symbol	Value	Rating
Thermal Resistance Ceramic Plastic	θ_{JA}	 50 TBD	°C/W

6.3 POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts − Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins − User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

6.4 DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ±5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristics		Symbol	Min	Max	Unit
Input High Voltage	All Inputs	V_{IH}	V_{SS} + 2.0	V_{CC}	V
Input Low Voltage	All Inputs	V_{IL}	V_{SS} − 0.3	V_{SS} + 0.8	V
Input Leakage Current (V_{in} = 0 to 5.25 V)	H1, H3, R/$\overline{W}$, $\overline{RESET}$, CLK, RS1-RS5, $\overline{CS}$	I_{in}	–	10.0	μA
Hi-Z (Off State) Input Current (V_{in} = 0.4 to 2.4)	$\overline{DTACK}$, PC0-PC7, D0-D7 H2, H4, PA0-PA7, PB0-PB7	I_{TSI}	– −0.1	20 −1.0	μA mA
Output High Voltage (I_{Load} = −400 μA, V_{CC} = min) (I_{Load} = −150 μA, V_{CC} = min) (I_{Load} = −100 μA, V_{CC} = min)	$\overline{DTACK}$, D0-D7 H2, H4, PB0-PB7, PA0-PA7 PC0-PC7	V_{OH}	V_{SS} + 2.4	–	V
Output Low Voltage (I_{Load} = 8.8 mA, V_{CC} = min) (I_{Load} = 5.3 mA, V_{CC} = min) (I_{Load} = 2.4 mA, V_{CC} = min)	PC3/TOUT, PC5/$\overline{PIRQ}$ D0-D7, $\overline{DTACK}$ PA0-PA7, PB0-PB7, H2, H4, PC0-PC2, PC4, PC6, PC7	V_{OL}	–	0.5	V
Internal Power Dissipation (Measured at T_A = 0°C)		P_{INT}	–	750	mW
Input Capacitance (V_{in} = 0, T_A = 25°C, f = 1 MHz)		C_{in}	–	15	pF

6.5 AC ELECTRICAL SPECIFICATIONS — CLOCK TIMING (See Figure 6-1)

Characteristic	Symbol	8 MHz		10 MHz		12.5 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Frequency of Operation	f	2.0	8.0	2.0	10.0	4.0	12.0	MHz
Cycle Time	t_{cyc}	125	500	100	500	80	250	ns
Clock Pulse Width	t_{CL}	55	250	45	250	35	125	ns
	t_{CH}	55	250	45	250	35	125	
Clock Rise and Fall Times	t_{Cr}	–	10	–	10	–	5	ns
	t_{Cf}	–	10	–	10	–	5	

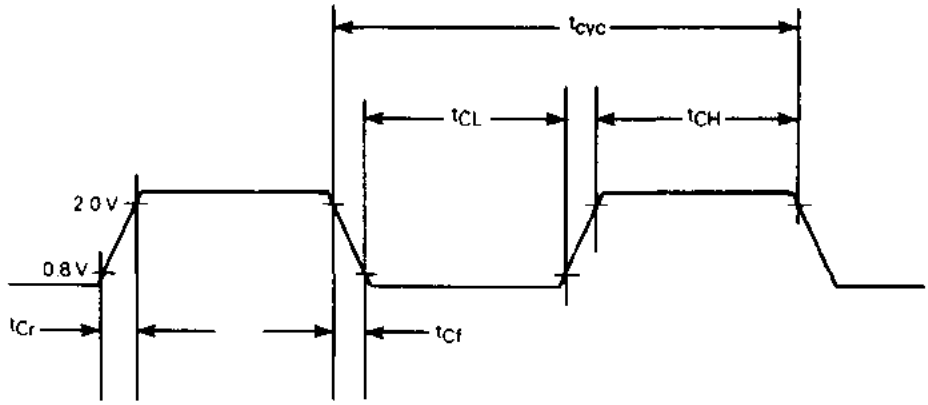


Figure 6-1. Clock Input Timing Diagram

6.6 AC ELECTRICAL SPECIFICATIONS (V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C, unless otherwise noted)

Number	Characteristic	8 MHz		10 MHz		12.5 MHz		Unit
		Min	Max	Min	Max	Min	Max	
1	R/$\overline{W}$, RS1-RS5 Valid to $\overline{CS}$ Low (Setup Time)	0	–	0	–	0	–	ns
2(10)	$\overline{CS}$ Low to R/$\overline{W}$ and RS1-RS5 Invalid (Hold Time)	100	–	65	–	60	–	ns
3(1)	$\overline{CS}$ Low to CLK Low (Setup Time)	30	–	20	–	20	–	ns
4(2)	$\overline{CS}$ Low to Data Out Valid	–	75	–	60	–	55	ns
5	RS1-RS5 Valid to Data Out Valid	–	140	–	100	–	80	ns
6	CLK Low to $\overline{DTACK}$ Low (Read/Write Cycle)	0	70	0	60	0	55	ns
7(3)	$\overline{DTACK}$ Low to $\overline{CS}$ High (Hold Time)	0	–	0	–	0	–	ns
8	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ High to Data Out Invalid (Hold Time)	0	–	0	–	0	–	ns
9	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ High to D0-D7 High Impedance	–	50	–	45	–	45	ns
10	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ High to $\overline{DTACK}$ High	–	50	–	45	–	40	ns
11	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ High to $\overline{DTACK}$ High Impedance	–	100	–	55	–	45	ns
12	Data In Valid to $\overline{CS}$ Low (Setup Time)	0	–	0	–	0	–	ns
13	$\overline{CS}$ Low to Data In Invalid (Hold Time)	100	–	65	–	60	–	ns
14	Port Input Data Valid to H1(H3) Asserted (Setup Time)	100	–	60	–	50	–	ns
15	H1(H3) Asserted to Port Input Data Invalid (Hold Time)	20	–	20	–	20	–	ns
16	Handshake Input H1(H4) Pulse Width Asserted	40	–	40	–	40	–	ns
17	Handshake Input H1(H4) Pulse Width Negated	40	–	40	–	40	–	ns
18	H1(H3) Asserted to H2(H4) Negated (Delay Time)	–	150	–	120	–	100	ns
19	CLK Low to H2(H4) Asserted (Delay Time)	–	100	–	100	–	80	ns
20(4)	H2(H4) Asserted to H1(H3) Asserted	0	–	0	–	0	–	ns
21(5)	CLK Low to H2(H4) Pulse Negated (Delay Time)	–	125	–	125	–	100	ns
22(9,11)	Synchronized H1(H3) to CLK Low on which $\overline{DMAREQ}$ is Asserted	2.5	3.5	2.5	3.5	2.5	3.5	CLK Per
23	CLK Low on which $\overline{DMAREQ}$ is Asserted to CLK Low on which $\overline{DMAREQ}$ is Negated	2.5	3	2.5	3	2.5	3	CLK Per.
24	CLK Low to Port Output Data Valid (Delay Time) (Modes 0 and 1)	–	150	–	120	–	100	ns
25(9,11)	Synchronized H1(H3) to Port Output Data Invalid (Modes 0 and 1)	1.5	2.5	1.5	2.5	1.5	2.5	CLK Per.
26	H1 Negated to Port Output Data Valid (Modes 2 and 3)	–	70	–	50	–	50	ns
27	H1 Asserted to Port Output Data High Impedance (Modes 2 and 3)	0	70	0	70	0	70	ns
28	Read Data Valid to $\overline{DTACK}$ Low (Setup Time)	0	–	0	–	0	–	ns
29	CLK Low to Data Output Valid, Interrupt Acknowledge Cycle	–	120	–	100	–	80	ns
30(7)	H1(H3) Asserted to CLK High (Setup Time)	50	–	40	–	40	–	ns
31	$\overline{PIACK}$ or $\overline{TIACK}$ Low to CLK Low (Setup Time)	50	–	40	–	30	–	ns
32(11)	Synchronized $\overline{CS}$ to CLK Low on which $\overline{DMAREQ}$ is Asserted	3	3	3	3	3	3	CLK Per
33(9,11)	Synchronized H1(H3) to CLK Low on which H2(H4) is Asserted	3.5	4.5	3.5	4.5	3.5	4.5	CLK Per
34	CLK Low to $\overline{DTACK}$ Low Interrupt Acknowledge Cycle (Delay Time)	–	100	–	100	–	80	ns
35	CLK Low to $\overline{DMAREQ}$ Low (Delay Time)	0	120	0	100	0	80	ns
36	CLK Low to $\overline{DMAREQ}$ High (Delay Time)	0	120	0	100	0	80	ns
37(11)	Synchronized H1(H3) to CLK Low on which $\overline{PIRQ}$ is Asserted	3	3	3	3	3	3	CLK Per.

6.6 AC ELECTRICAL SPECIFICATIONS (Continued)

Number	Characteristic	8 MHz		10 MHz		12.5 MHz		Unit
		Min	Max	Min	Max	Min	Max	
38(11)	Synchronized $\overline{CS}$ to CLK Low on which $\overline{PIRQ}$ is High Impedance	3	3	3	3	3	3	CLK Per.
39	CLK Low to $\overline{PIRQ}$ Low or High Impedance	0	250	0	225	0	200	ns
40(8)	TIN Frequency (External Clock) — Prescaler Used	0	1	0	1	0	1	f_{clk} (Hz) (6)
41	TIN Frequency (External Clock) — Prescaler Not Used	0	1/8	0	1/8	0	1/8	f_{clk} (Hz) (6)
42	TIN Pulse Width High or Low (External Clock)	55	—	45	—	45	—	ns
43	TIN Pulse Width Low (Run/Halt Control)	1	—	1	—	1	—	CLK Per.
44	CLK Low to TOUT High, Low, or High Impedance	0	250	0	225	0	200	ns
45	$\overline{CS}$, $\overline{PIACK}$, or $\overline{TIACK}$ High to $\overline{CS}$, $\overline{PIACK}$, or $\overline{TIACK}$ Low	50	—	30	—	30	—	ns

NOTES:

1. This specification only applies if the PI/T had completed all operations initiated by the previous bus cycle when $\overline{CS}$ was asserted. Following a normal read or write bus cycle, all operations are complete within three clocks after the falling edge of the CLK pin on which $\overline{DTACK}$ was asserted. If $\overline{CS}$ is asserted prior to completion of these operations, the new bus cycle, and hence, $\overline{DTACK}$ is postponed.

   If all operations of the previous bus cycle were complete when $\overline{CS}$ was asserted, this specification is made only to insure that $\overline{DTACK}$ is asserted with respect to the falling edge of the CLK pin as shown in the timing diagram, not to guarantee operation of the part. If the $\overline{CS}$ setup time is violated, $\overline{DTACK}$ may be asserted as shown, or may be asserted one clock cycle later.

2. Assuming the RS1-RS5 to data valid time has also expired.

3. This specification imposes a lower bound on $\overline{CS}$ low time, guaranteeing that $\overline{CS}$ will be low for at least 1 CLK period.

4. This specification assures recognition of the asserted edge of H1(H3).

5. This specification applies only when a pulsed handshake option is chosen and the pulse is not shortened due to an early asserted edge of H1(H3).

6. CLK refers to the actual frequency of the CLK pin, not the maximum allowable CLK frequency.

7. If the setup time on the rising edge of the clock is not met, H1(H3) may not be recognized until the next rising of the clock.

8. This limit applies to the frequency of the signal at TIN compared to the frequency of the CLK signal during each clock cycle. If any period of the waveform at TIN is smaller than the period of the CLK signal at that instant, then it is likely that the timer circuit will completely ignore one cycle of the TIN signal.

   If these two signals are derived from different sources they will have different instantaneous frequency variations. In this case the frequency applied to the TIN pin must be distinctly less than the frequency at the CLK pin to avoid lost cycles of the TIN signal. With signals derived from different crystal oscillators applied to the TIN and CLK pins with fast rise and fall times, the TIN frequency can approach 80 to 90% of the frequency of the CLK signal without a loss of a cycle of the TIN signal.

   If these two signals are derived from the same frequency source then the frequency of the signal applied to TIN can be 100% of the frequency at the CLK pin. They may be generated by different buffers from the same signal or one may be an inverted version of the other. The TIN signal may be generated by an 'AND' function of the clock and a control signal.

9. The maximum value is caused by a peripheral access (H1(H3) asserted) and bus access ($\overline{CS}$ asserted) occurring at the same time.

10. See **1.4 BUS INTERFACE OPERATION** for exception.

11. Synchronized means that the input signal has been seen by the PI/T on the appropriate edge of the clock (rising edge for H1(H3) and falling edge for $\overline{CS}$). (Refer to the **1.4 BUS INTERFACE OPERATION** for the exception concerning $\overline{CS}$.)

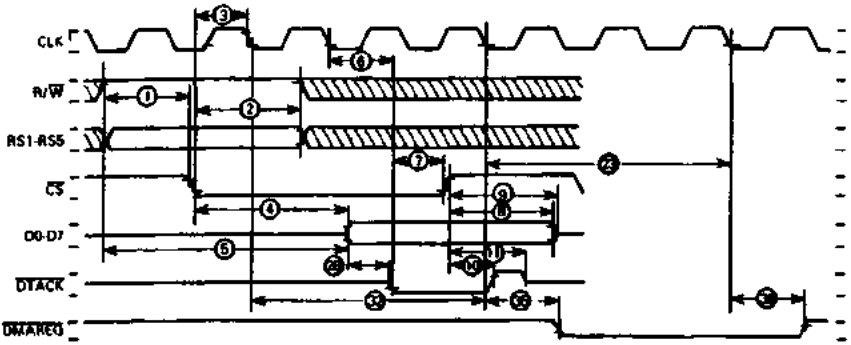


Figure 6-2. Read Cycle Timing Diagram

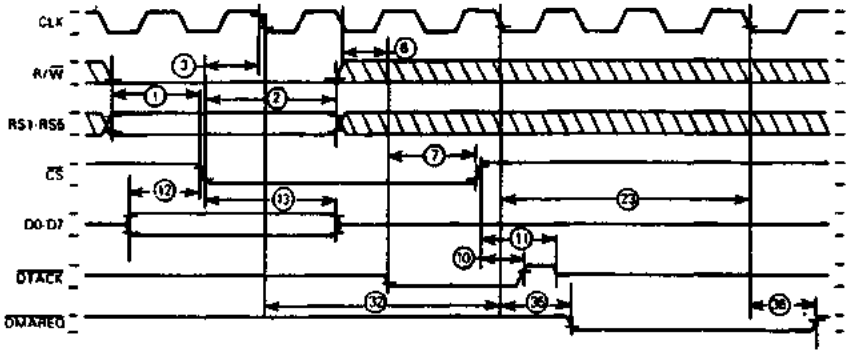
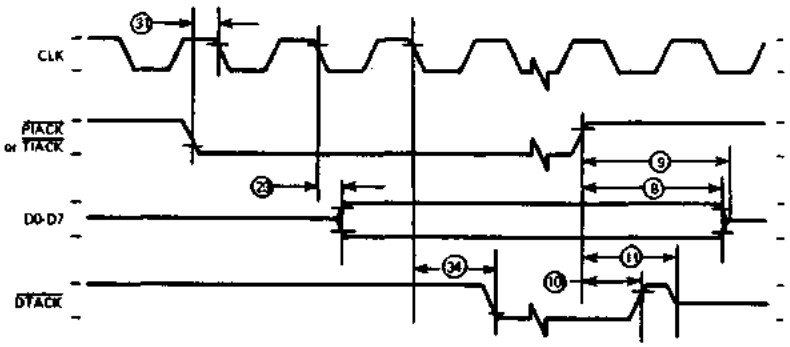


Figure 6-3. Write Cycle Timing Diagram

NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.



NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

Figure 6-4. IACK Timing Diagram

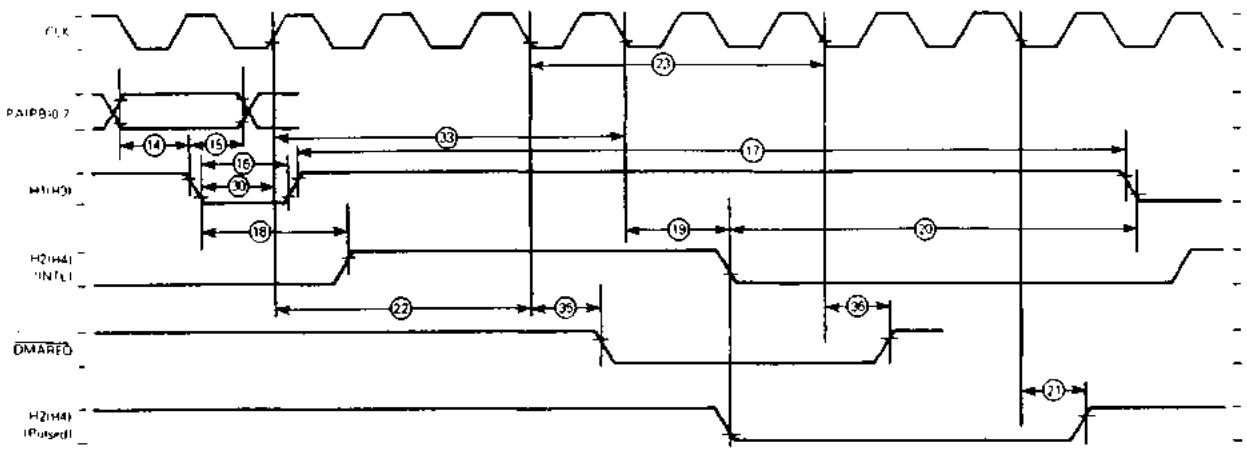


Figure 6-5. Peripheral Input Timing Diagram

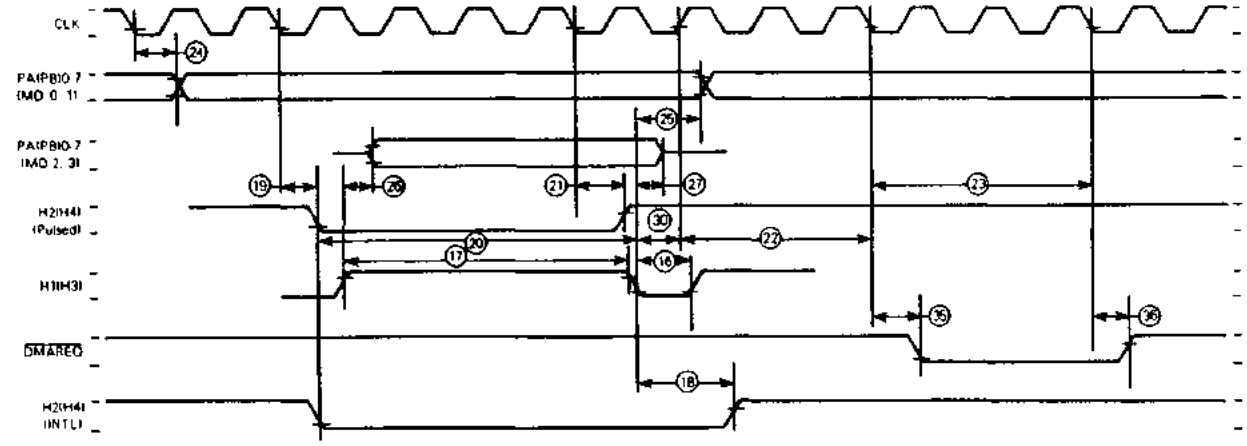


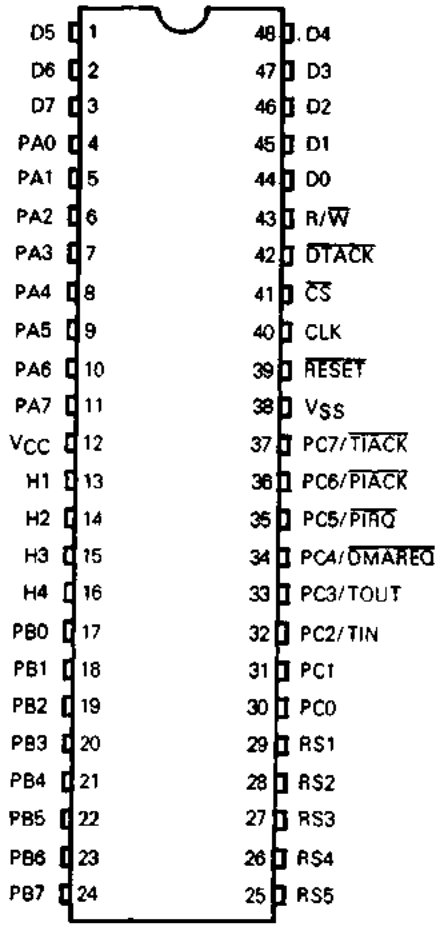
Figure 6-6. Peripheral Output Timing Diagram

NOTES
1. Timing diagram shows H1, H2, H3, and H4 asserted low.
2. Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

SECTION 7
MECHANICAL DATA AND ORDERING INFORMATION

This section contains the pin assignments and package dimensions of the MC68230. In addition, detailed information is provided to be used as a guide when ordering.

7.1 PIN ASSIGNMENT

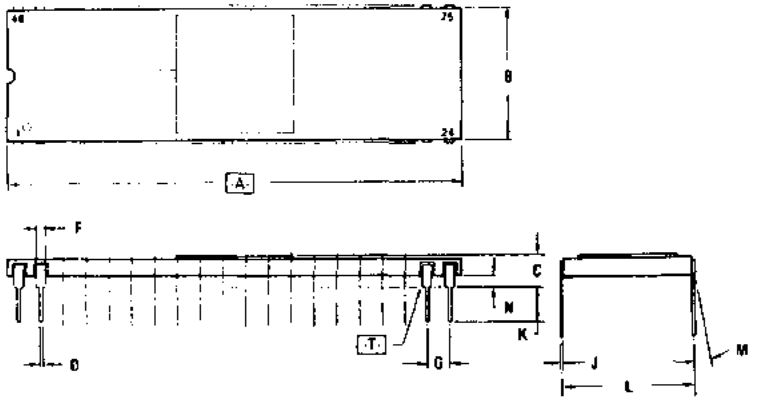


7.2 ORDERING INFORMATION

Package Type	Frequency (MHz)	Temperature	Order Number
Ceramic	8.0	0°C to 70°C	MC68230L8
L Suffix	10.0	0°C to 70°C	MC68230L10
	12.5	0°C to 70°C	MC68230L12
Plastic	8.0	0°C to 70°C	MC68230G8
G Suffix	10.0	0°C to 70°C	MC68230G10
	12.5	0°C to 70°C	MC68230G12

7.3 PACKAGE DIMENSIONS

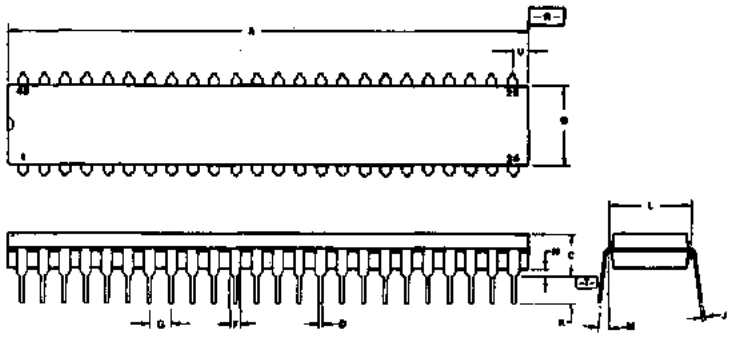
L SUFFIX
CERAMIC PACKAGE
CASE 740-02



NOTES:
1. DIMENSION A IS DATUM.
2. POSTIONAL TOLERANCE FOR LEADS:
   ⌖ Ø 0.25 (0.010) M T A M
3. T IS SEATING PLANE.
4. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	60.35	61.57	2.376	2.424
B	14.63	15.34	0.576	0.604
C	3.05	4.32	0.120	0.160
D	0.381	0.533	0.015	0.021
F	0.762	1.397	0.030	0.055
G	2.54 BSC		0.100 BSC	
J	0.203	0.330	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.99	15.65	0.590	0.616
M	0°	10°	0°	10°
N	1.016	1.524	0.040	0.060

G SUFFIX
PLASTIC PACKAGE
CASE 767-01



NOTES:
1. -R- IS END OF PACKAGE DATUM PLANE.
   -T- IS BOTH A DATUM AND SEATING PLANE.
2. POSITIONAL TOLERANCE FOR LEADS 24 & 25:
   ⌖ 0.35 (0.014) T B Ⓜ R
   POSITIONAL TOLERANCE FOR LEAD PATTERN:
   ⌖ 0.25 (0.010) T B Ⓜ
3. DIM B DOES NOT INCLUDE MOLD FLASH.
4. DIM L IS TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	61.67	61.77	2.428	2.432
B	13.92	14.02	0.548	0.552
C	4.83	5.06	0.190	0.200
D	0.38	0.50	0.015	0.020
F	1.22	1.34	0.048	0.053
G	2.54 BSC		0.100 BSC	
J	0.25	0.30	0.010	0.012
K	3.23	3.37	0.127	0.133
L	15.24 BSC		0.600 BSC	
M	0°	10°	0°	10°
N	0.64	0.88	0.025	0.035
U	1.79 BSC		0.070 BSC	

APPENDIX B

MC3448A Transceiver Data Sheet

MOTOROLA

MC3448A

BIDIRECTIONAL INSTRUMENTATION BUS (GPIB) TRANSCEIVER

This bidirectional bus transceiver is intended as the interface between TTL or MOS logic and the IEEE Standard Instrumentation Bus (488-1978, often referred to as GPIB). The required bus termination is internally provided.

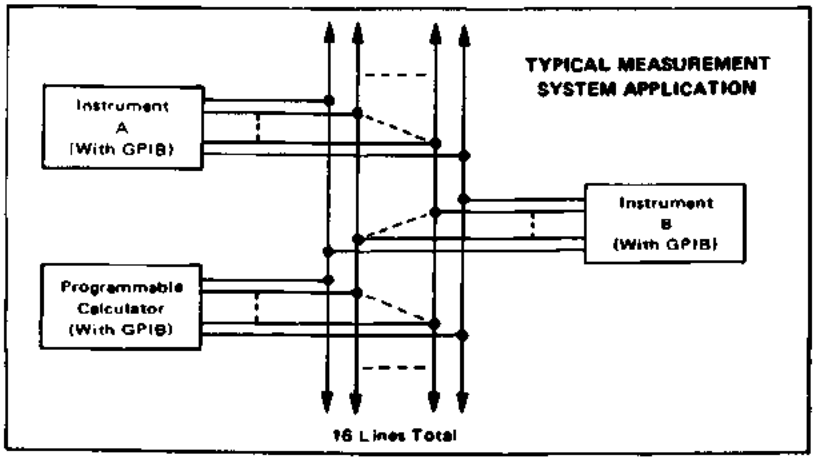
Each driver/receiver pair forms the complete interface between the bus and an instrument. Either the driver or the receiver of each channel is enabled by its corresponding Send/Receive input with the disabled output of the pair forced to a high impedance state. An additional option allows the driver outputs to be operated in an open collector(1) or active pull-up configuration. The receivers have input hysteresis to improve noise margin, and their input loading follows the bus standard specifications.

- Four Independent Driver/Receiver Pairs
- Three-State Outputs
- High Impedance Inputs
- Receiver Hysteresis — 600 mV (Typ)
- Fast Propagation Times — 15–20 ns (Typ)
- TTL Compatible Receiver Outputs
- Single +5 Volt Supply
- Open Collector Driver Output Option(1)
- Power Up/Power Down Protection
  (No Invalid Information Transmitted to Bus)
- No Bus Loading When Power Is Removed From Device
- Required Termination Characteristics Provided

(1) Selection of the "Open Collector" configuration, in fact, selects an open collector device with a passive pull-up load/termination which conforms to Figure 7, IEEE 488-1978 Bus Standard.

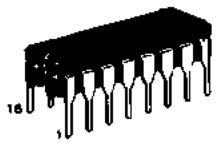
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Driver Output Current	$I_{O(D)}$	150	mA
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

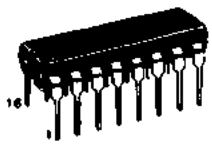


QUAD THREE-STATE BUS TRANSCEIVER WITH TERMINATION NETWORKS

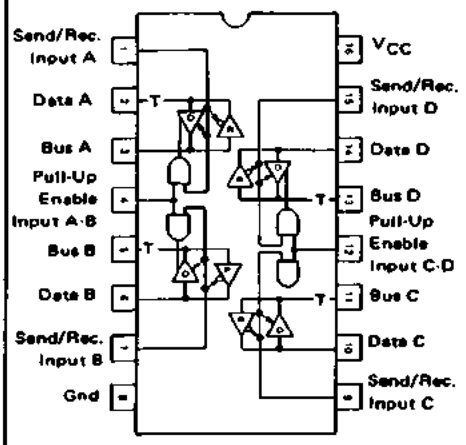
SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 620-02



P SUFFIX
PLASTIC PACKAGE
CASE 648-05



TRUTH TABLE

Send/Rec.	Enable	Info. Flow	Comments
0	X	Bus → Data	—
1	1	Data → Bus	Active Pull Up
1	0	Data → Bus	Open Col.

X = Don't Care

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted 4.75 V ≤ V_{CC} ≤ 5.25 V and 0 ≤ T_A ≤ 70°C; typical values are at T_A = 25°C, V_{CC} = 5.0 V)

Characteristic	Symbol	Min	Typ	Max	Unit
Bus Voltage					V
(Bus Pin Open)($V_{I(S/R)}$ = 0.8 V)	$V_{(BUS)}$	2.75	–	3.7	
($I_{(BUS)}$ = -12 mA)	$V_{IC(BUS)}$	–	–	-1.5	
Bus Current	$I_{(BUS)}$				mA
(5.0 V ≤ $V_{(BUS)}$ ≤ 5.5 V)		0.7	–	2.5	
($V_{(BUS)}$ = 0.5 V)		-1.3	–	-3.2	
(V_{CC} = 0 V, 0 V ≤ $V_{(BUS)}$ ≤ 2.75 V)		–	–	+0.04	
Receiver Input Hysteresis ($V_{I(S/R)}$ = 0.8 V)	–	400	600	–	mV
Receiver Input Threshold					V
($V_{I(S/R)}$ = 0.8 V, Low to High)	$V_{ILH(R)}$	–	1.6	1.8	
($V_{I(S/R)}$ = 0.8 V, High to Low)	$V_{IHL(R)}$	0.8	1.0	–	
Receiver Output Voltage – High Logic State ($V_{I(S/R)}$ = 0.8 V, $I_{OH(R)}$ = -800 µA, $V_{(BUS)}$ = 2.0 V)	$V_{OH(R)}$	2.7	–	–	V
Receiver Output Voltage – Low Logic State ($V_{I(S/R)}$ = 0.8 V, $I_{OL(R)}$ = 16 mA, $V_{(BUS)}$ = 0.8 V)	$V_{OL(R)}$	–	–	0.5	V
Receiver Output Short Circuit Current ($V_{I(S/R)}$ = 0.8 V, $V_{(BUS)}$ = 2.0 V)	$I_{OS(R)}$	-15	–	-75	mA
Driver Input Voltage – High Logic State ($V_{I(S/R)}$ = 2.0 V)	$V_{IH(D)}$	2.0	–	–	V
Driver Input Voltage – Low Logic State ($V_{I(S/R)}$ = 2.0 V)	$V_{IL(D)}$	–	–	0.8	V
Driver Input Current – Data Pins					µA
($V_{I(S/R)}$ = $V_{I(E)}$ = 2.0 V)					
(0.5 ≤ $V_{I(D)}$ ≤ 2.7 V)	$I_{I(D)}$	-200	–	40	
($V_{I(D)}$ = 5.5 V)	$I_{IB(D)}$	–	–	200	
Input Current – Send/Receive					µA
(0.5 ≤ $V_{I(S/R)}$ ≤ 2.7 V)	$I_{I(S/R)}$	-100	–	20	
($V_{I(S/R)}$ = 5.5 V)	$I_{IB(S/R)}$	–	–	100	
Input Current – Enable					µA
(0.5 ≤ $V_{I(E)}$ ≤ 2.7 V)	$I_{I(E)}$	-200	–	20	
($V_{I(E)}$ = 5.5 V)	$I_{IB(E)}$	–	–	100	
Driver Input Clamp Voltage ($V_{I(S/R)}$ = 2.0 V, $I_{IC(D)}$ = -18 mA)	$V_{IC(D)}$	–	–	-1.5	V
Driver Output Voltage – High Logic State ($V_{I(S/R)}$ = 2.0 V, $V_{IH(D)}$ = 2.0 V, $V_{IH(E)}$ = 2.0 V, I_{OH} = -5.2 mA)	$V_{OH(D)}$	2.5	–	–	V
Driver Output Voltage – Low Logic State (Note 1) ($V_{I(S/R)}$ = 2.0 V, $I_{OL(D)}$ = 48 mA)	$V_{OL(D)}$	–	–	0.5	V
Output Short Circuit Current ($V_{I(S/R)}$ = 2.0 V, $V_{IH(D)}$ = 2.0 V, $V_{IH(E)}$ = 2.0 V)	$I_{OS(D)}$	-30	–	-120	mA
Power Supply Current					mA
(Listening Mode – All Receivers On)	I_{CCL}	–	53	85	
(Talking Mode – All Drivers On)	I_{CCH}	–	106	125	

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted)

Propagation Delay of Driver					ns
(Output Low to High)	$t_{PLH(D)}$	–	–	15	
(Output High to Low)	$t_{PHL(D)}$	–	–	17	
Propagation Delay of Receiver					ns
(Output Low to High)	$t_{PLH(R)}$	–	–	25	
(Output High to Low)	$t_{PHL(R)}$	–	–	23	

NOTE 1. A modification of the IEEE 488-1978 Bus Standard changes $V_{OL(D)}$ from 0.4 to 0.5 V maximum to permit the use of Schottky technology.

SWITCHING CHARACTERISTICS (continued) (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time — Send/Receive to Data					ns
Logic High to Third State	$t_{PHZ(R)}$	–	–	30	
Third State to Logic High	$t_{PZH(R)}$	–	–	30	
Logic Low to Third State	$t_{PLZ(R)}$	–	–	30	
Third State to Logic Low	$t_{PZL(R)}$	–	–	30	
Propagation Delay Time — Send/Receive to Bus					ns
Logic High to Third State	$t_{PHZ(D)}$	–	–	30	
Third State to Logic High	$t_{PZH(D)}$	–	–	30	
Logic Low to Third State	$t_{PLZ(D)}$	–	–	30	
Third State to Logic Low	$t_{PZL(D)}$	–	–	30	
Turn-On Time — Enable to Bus					ns
Pull-Up Enable to Open Collector	$t_{POFF(E)}$	–	–	30	
Open Collector to Pull-Up Enable	$t_{PON(E)}$	–	–	20	

PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS

FIGURE 1 — BUS INPUT TO DATA OUTPUT (RECEIVER)

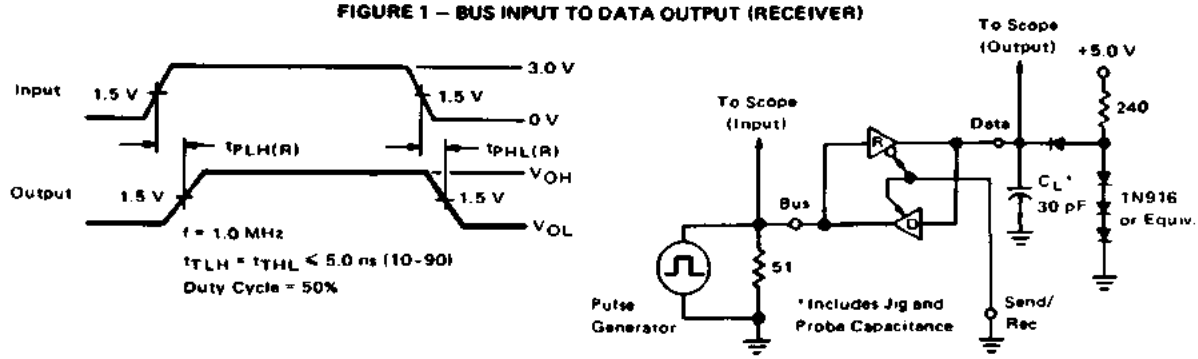


FIGURE 2 — DATA INPUT TO BUS OUTPUT (DRIVER)

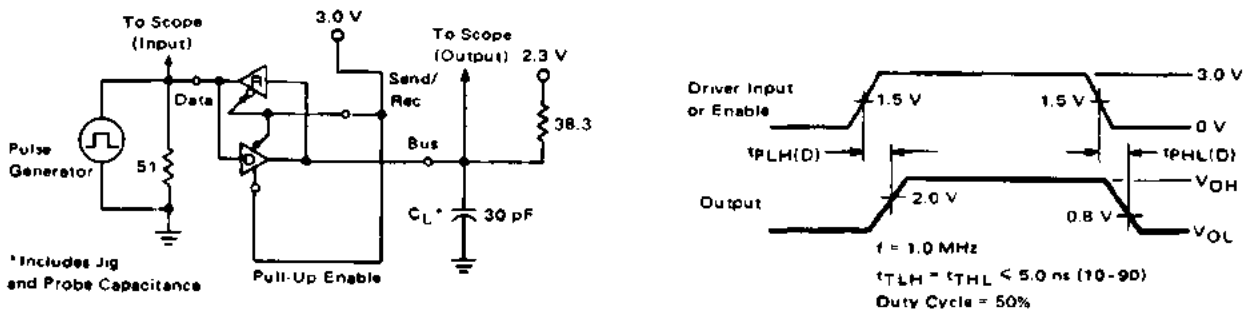


FIGURE 3 — SEND/RECEIVE INPUT TO BUS OUTPUT (DRIVER)

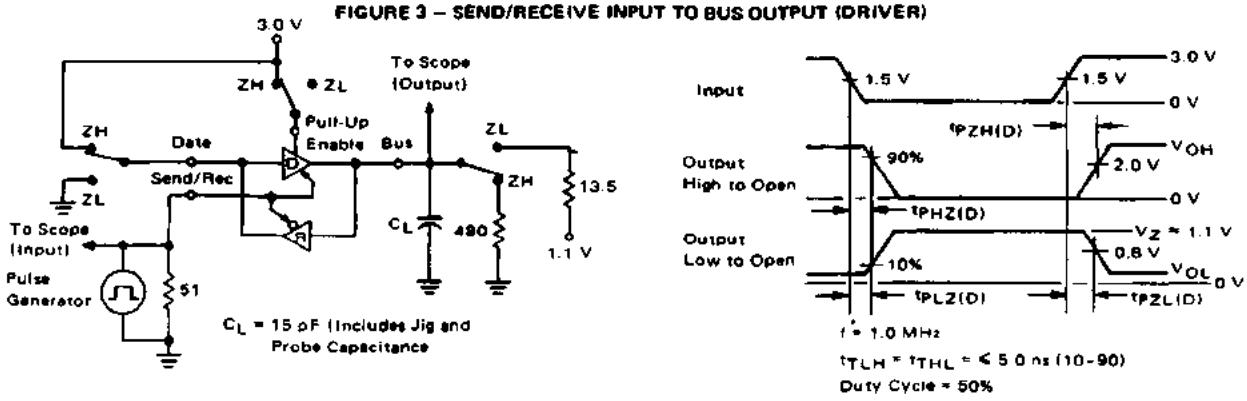


FIGURE 4 – SEND/RECEIVE INPUT TO DATA OUTPUT (RECEIVER)

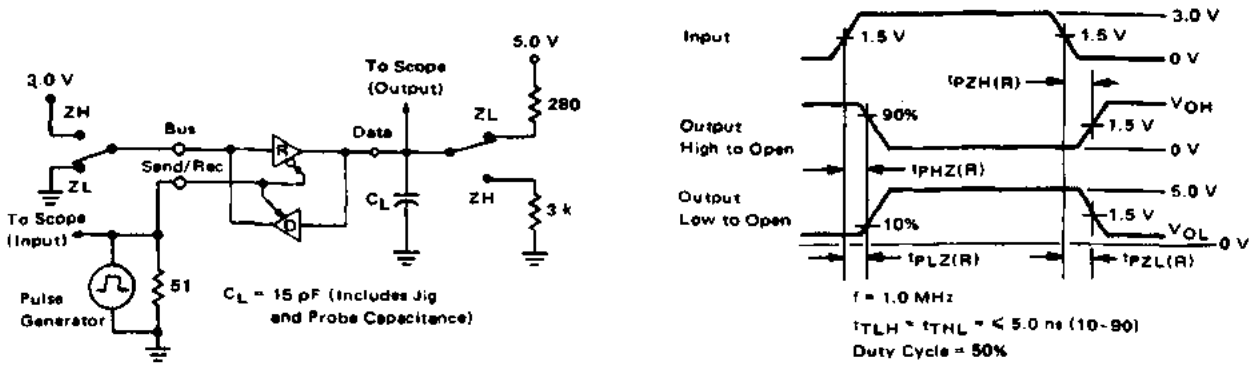


FIGURE 5 – ENABLE INPUT TO BUS OUTPUT (DRIVER)

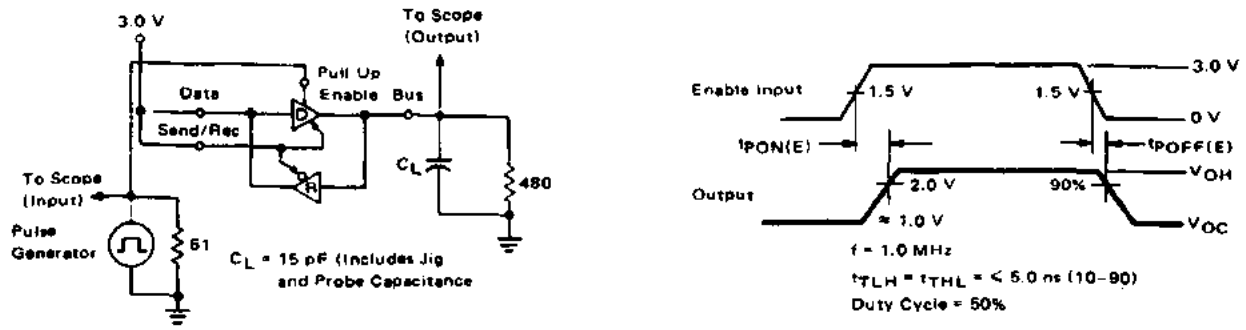


FIGURE 6 – TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS

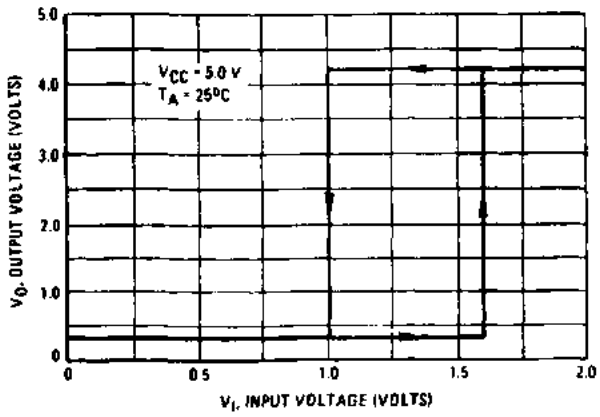


FIGURE 7 – TYPICAL BUS LOAD LINE

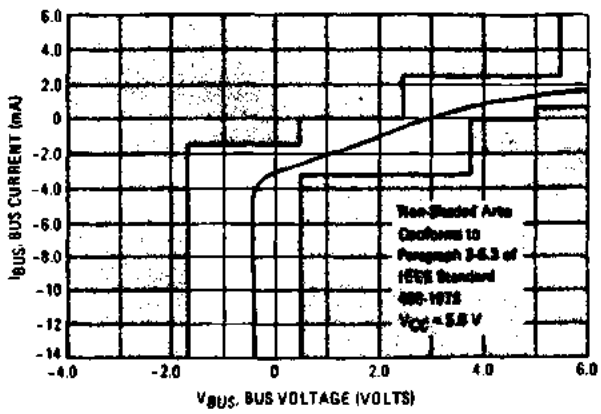
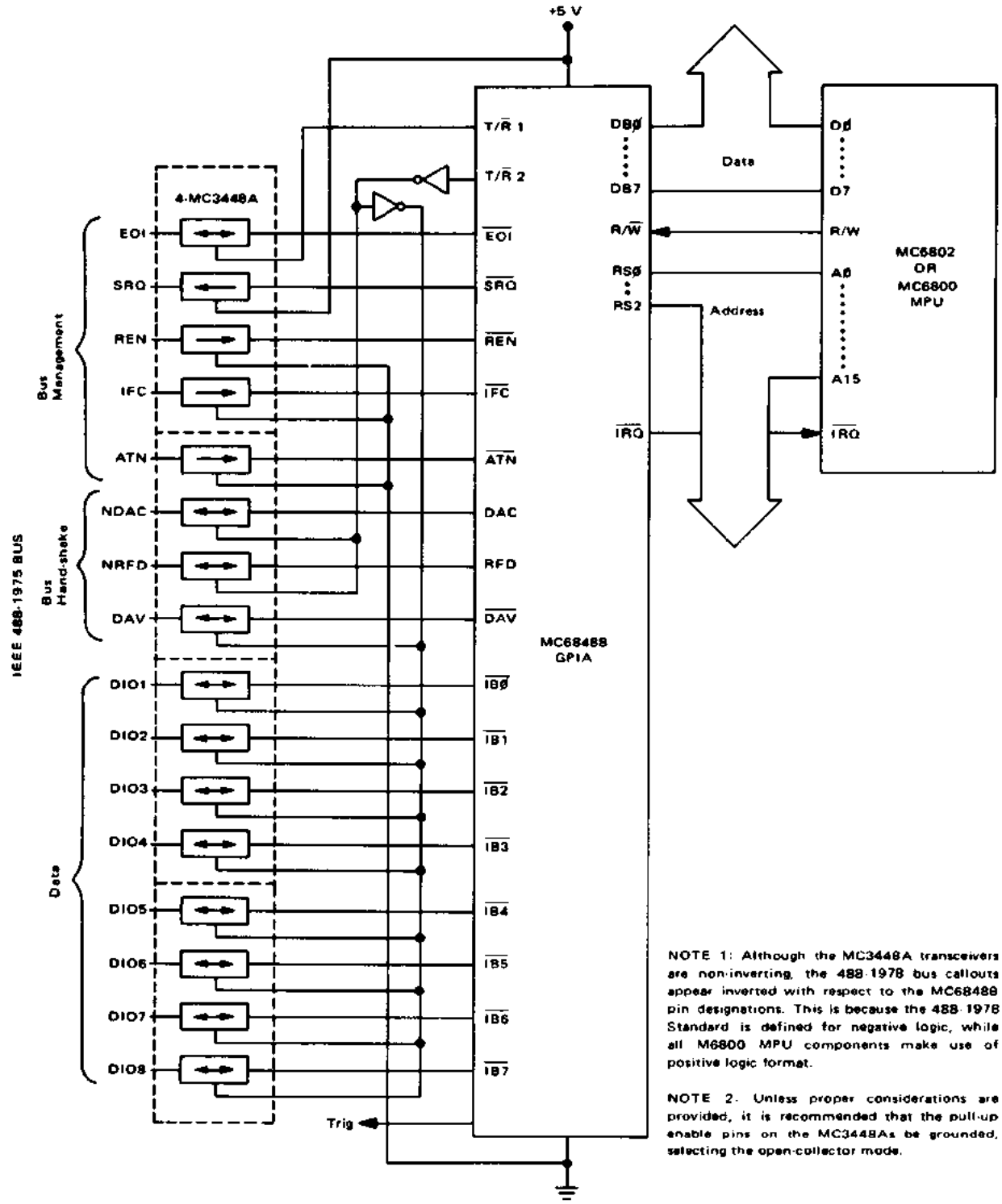


FIGURE 8 – SIMPLE SYSTEM CONFIGURATION



NOTE 1: Although the MC3448A transceivers are non-inverting, the 488-1978 bus callouts appear inverted with respect to the MC68488 pin designations. This is because the 488-1978 Standard is defined for negative logic, while all M6800 MPU components make use of positive logic format.

NOTE 2: Unless proper considerations are provided, it is recommended that the pull-up enable pins on the MC3448As be grounded, selecting the open-collector mode.

MC3450
MC3452

MOTOROLA

Specifications and Applications Information

QUAD MTTL COMPATIBLE LINE RECEIVERS

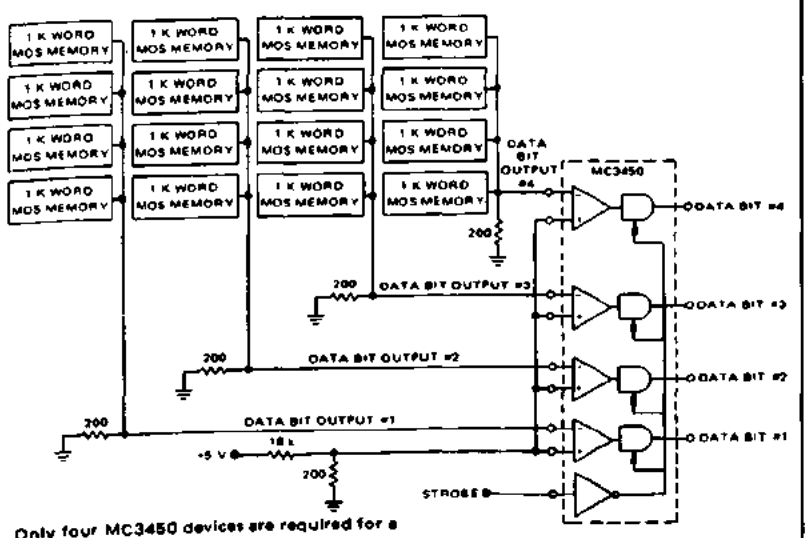
The MC3450 features four MC75107 type active pullup line receivers with the addition of a common three-state strobe input. When the strobe input is at a logic zero, each receiver output state is determined by the differential voltage across its respective inputs. With the strobe high, the receiver outputs are in the high impedance state.

The MC3452 is the same as the MC3450 except that the outputs are open collector which permits the implied "AND" function.

The strobe input on both devices is buffered to present a strobe loading factor of only one for all four receivers and inverted to provide best compatability with standard decoder devices.

- Receiver Performance Identical to the Popular MC75107/MC75108 Series
- Four Independent Receivers with Common Strobe Input
- Implied "AND" Capability with Open Collector Outputs
- Useful as a Quad 1103 type Memory Sense Amplifier

FIGURE 1 – A TYPICAL MOS MEMORY SENSING APPLICATION FOR A 4-K WORD BY 4-BIT MEMORY ARRANGEMENT EMPLOYING 1103 TYPE MEMORY DEVICES



Only four MC3450 devices are required for a 4-k word by 16-bit memory system.

QUAD LINE RECEIVERS WITH COMMON THREE-STATE STROBE INPUT

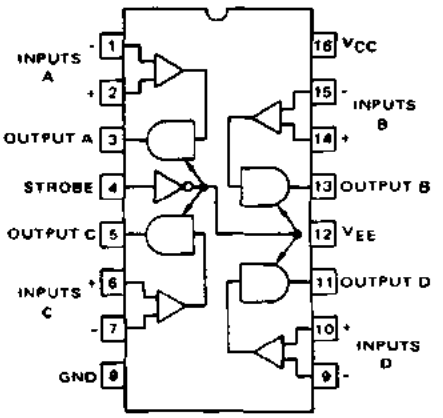
SILICON MONOLITHIC INTEGRATED CIRCUITS



L SUFFIX
CERAMIC PACKAGE
CASE 620-02

P SUFFIX
PLASTIC PACKAGE
CASE 648-05

CONNECTION DIAGRAM



TRUTH TABLE

INPUT	STROBE	OUTPUT MC3450	OUTPUT MC3452
$V_{ID} \geq$ +25 mV	L	H	Off
	H	Z	Off
-25 mV $\leq V_{ID} \leq$ +25 mV	L	I	I
	H	Z	Off
$V_{ID} \leq$ -25 mV	L	L	L
	H	Z	Off

L = Low Logic State
H = High Logic State
Z = Third (High Impedance) State
I = Indeterminate State

APPENDIX C

MVME340 REGISTER EQUATE FILE

The following equate file specifies the addresses of all MVME340 registers for use with MC68000 assembler programs. Note that the base address of the MVME340 module is set to $FF0000 in this file and must be changed for the actual user configuration.

```
*****************************************************************************
*        MVME340 MODULE BASE ADDRESS                                        *
*****************************************************************************
BASE340  EQU     $FF0000      MVME340 BASE ADDRESS = $FF0000

*****************************************************************************
*        PI/T 1 REGISTERS                                                   *
*****************************************************************************
PIT1     EQU     BASE340      PI/T 1 BASE ADDRESS
PGCR1    EQU     PIT1         PI/T 1 PORT GENERAL CONTROL REGISTER
PSRR1    EQU     PIT1+$2      PI/T 1 PORT SERVICE REQUEST REGISTER
PADDR1   EQU     PIT1+$4      PI/T 1 PORT A DATA DIRECTION REGISTER
PBDDR1   EQU     PIT1+$6      PI/T 1 PORT B DATA DIRECTION REGISTER
PCDDR1   EQU     PIT1+$8      PI/T 1 PORT C DATA DIRECTION REGISTER
PISBR1   EQU     PIT1+$A      PI/T 1 PORT INTERRUPT STATUS/ID BYTE REGISTER
PACR1    EQU     PIT1+$C      PI/T 1 PORT A CONTROL REGISTER
PBCR1    EQU     PIT1+$E      PI/T 1 PORT B CONTROL REGISTER
PADR1    EQU     PIT1+$10     PI/T 1 PORT A DATA REGISTER
PBDR1    EQU     PIT1+$12     PI/T 1 PORT B DATA REGISTER
PAAR1    EQU     PIT1+$14     PI/T 1 PORT A ALTERNATE REGISTER
PBAR1    EQU     PIT1+$16     PI/T 1 PORT B ALTERNATE REGISTER
PCDR1    EQU     PIT1+$18     PI/T 1 PORT C DATA REGISTER
PSR1     EQU     PIT1+$1A     PI/T 1 PORT STATUS REGISTER
TCR1     EQU     PIT1+$20     PI/T 1 TIMER CONTROL REGISTER
TISBR1   EQU     PIT1+$22     PI/T 1 TIMER INTERRUPT STATUS/ID BYTE REGISTER
CPRH1    EQU     PIT1+$26     PI/T 1 COUNTER PRELOAD REGISTER HIGH
CPRM1    EQU     PIT1+$28     PI/T 1 COUNTER PRELOAD REGISTER MID
CPRL1    EQU     PIT1+$2A     PI/T 1 COUNTER PRELOAD REGISTER LOW
CNTRH1   EQU     PIT1+$2E     PI/T 1 COUNT REGISTER HIGH
CNTRM1   EQU     PIT1+$30     PI/T 1 COUNT REGISTER MID
CNTRL1   EQU     PIT1+$32     PI/T 1 COUNT REGISTER LOW
TSR1     EQU     PIT1+$34     PI/T 1 TIMER STATUS REGISTER

*****************************************************************************
*        PI/T 2 REGISTERS                                                   *
*****************************************************************************
PIT2     EQU     BASE340+$1   PI/T 2 BASE ADDRESS
PGCR2    EQU     PIT2         PI/T 2 PORT GENERAL CONTROL REGISTER
PSRR2    EQU     PIT2+$2      PI/T 2 PORT SERVICE REQUEST REGISTER
PADDR2   EQU     PIT2+$4      PI/T 2 PORT A DATA DIRECTION REGISTER
PBDDR2   EQU     PIT2+$6      PI/T 2 PORT B DATA DIRECTION REGISTER
PCDDR2   EQU     PIT2+$8      PI/T 2 PORT C DATA DIRECTION REGISTER
PISBR2   EQU     PIT2+$A      PI/T 2 PORT INTERRUPT STATUS/ID BYTE REGISTER
PACR2    EQU     PIT2+$C      PI/T 2 PORT A CONTROL REGISTER
PBCR2    EQU     PIT2+$E      PI/T 2 PORT B CONTROL REGISTER
```

```
PADR2    EQU     PIT2+$10     PI/T 2 PORT A DATA REGISTER
PBDR2    EQU     PIT2+$12     PI/T 2 PORT B DATA REGISTER
PAAR2    EQU     PIT2+$14     PI/T 2 PORT A ALTERNATE REGISTER
PBAR2    EQU     PIT2+$16     PI/T 2 PORT B ALTERNATE REGISTER
PCDR2    EQU     PIT2+$18     PI/T 2 PORT C DATA REGISTER
PSR2     EQU     PIT2+$1A     PI/T 2 PORT STATUS REGISTER
TCR2     EQU     PIT2+$20     PI/T 2 TIMER CONTROL REGISTER
TISBR2   EQU     PIT2+$22     PI/T 2 TIMER INTERRUPT STATUS/ID BYTE REGISTER
CPRH2    EQU     PIT2+$26     PI/T 2 COUNTER PRELOAD REGISTER HIGH
CPRM2    EQU     PIT2+$28     PI/T 2 COUNTER PRELOAD REGISTER MID
CPRL2    EQU     PIT2+$2A     PI/T 2 COUNTER PRELOAD REGISTER LOW
CNTRH2   EQU     PIT2+$2E     PI/T 2 COUNT REGISTER HIGH
CNTRM2   EQU     PIT2+$30     PI/T 2 COUNT REGISTER MID
CNTRL2   EQU     PIT2+$32     PI/T 2 COUNT REGISTER LOW
TSR2     EQU     PIT2+$34     PI/T 2 TIMER STATUS REGISTER

*************************************************************************
*        PI/T 3 REGISTERS                                               *
*************************************************************************
PIT3     EQU     BASE340+$41  PI/T 3 BASE ADDRESS
PGCR3    EQU     PIT3         PI/T 3 PORT GENERAL CONTROL REGISTER
PSRR3    EQU     PIT3+$2      PI/T 3 PORT SERVICE REQUEST REGISTER
PADDR3   EQU     PIT3+$4      PI/T 3 PORT A DATA DIRECTION REGISTER
PBDDR3   EQU     PIT3+$6      PI/T 3 PORT B DATA DIRECTION REGISTER
PCDDR3   EQU     PIT3+$8      PI/T 3 PORT C DATA DIRECTION REGISTER
PISBR3   EQU     PIT3+$A      PI/T 3 PORT INTERRUPT STATUS/ID BYTE REGISTER
PACR3    EQU     PIT3+$C      PI/T 3 PORT A CONTROL REGISTER
PBCR3    EQU     PIT3+$E      PI/T 3 PORT B CONTROL REGISTER
PADR3    EQU     PIT3+$10     PI/T 3 PORT A DATA REGISTER
PBDR3    EQU     PIT3+$12     PI/T 3 PORT B DATA REGISTER
PAAR3    EQU     PIT3+$14     PI/T 3 PORT A ALTERNATE REGISTER
PBAR3    EQU     PIT3+$16     PI/T 3 PORT B ALTERNATE REGISTER
PCDR3    EQU     PIT3+$18     PI/T 3 PORT C DATA REGISTER
PSR3     EQU     PIT3+$1A     PI/T 3 PORT STATUS REGISTER
TCR3     EQU     PIT3+$20     PI/T 3 TIMER CONTROL REGISTER
TISBR3   EQU     PIT3+$22     PI/T 3 TIMER INTERRUPT STATUS/ID BYTE REGISTER
CPRH3    EQU     PIT3+$26     PI/T 3 COUNTER PRELOAD REGISTER HIGH
CPRM3    EQU     PIT3+$28     PI/T 3 COUNTER PRELOAD REGISTER MID
CPRL3    EQU     PIT3+$2A     PI/T 3 COUNTER PRELOAD REGISTER LOW
CNTRH3   EQU     PIT3+$2E     PI/T 3 COUNT REGISTER HIGH
CNTRM3   EQU     PIT3+$30     PI/T 3 COUNT REGISTER MID
CNTRL3   EQU     PIT3+$32     PI/T 3 COUNT REGISTER LOW
TSR3     EQU     PIT3+$34     PI/T 3 TIMER STATUS REGISTER

*************************************************************************
*        MODULE REGISTERS                                               *
*************************************************************************
ILR1     EQU     BASE340+$81  PI/T 1 INTERRUPT LEVEL REGISTER
ILR2     EQU     BASE340+$83  PI/T 2 INTERRUPT LEVEL REGISTER
ILR3     EQU     BASE340+$85  PI/T 3 INTERRUPT LEVEL REGISTER
MCR      EQU     BASE340+$87  MODULE CONTROL REGISTER
PLDR12   EQU     BASE340+$89  PI/T 1/2 PERIPHERAL LINE DIRECTION REGISTER
PLDR3    EQU     BASE340+$8B  PI/T 3 PERIPHERAL LINE DIRECTION REGISTER
DCCR     EQU     BASE340+$8D  DRIVER CHARACTERISTIC CONTROL REGISTER
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