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PRPMC750 Processor PMC Module

Installation and Use Manual

PRPMC750A/IH2

May 2000

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This manual provides both general and functional descriptions of the product along with connector pin assignments and specifications for the PrPMC750 Processor PMC Module.

Summary of Changes

The product name has changed from PPMC750 to PrPMC750.

The table below has been changed to reflect 8M Flash for all model numbers.

The minimum air flow requirement has been changed from 150 LFM to 450 LFM, see *Airflow Requirements* on page B-1.

The information contained in this manual applies to the PrPMC750 board, in the following model configurations:

Model Number	CPU/Speed	Major Differences
PRPMC750-1131	750, 233MHz	32MB DRAM, 1M L2 Cache, 8M Flash, Std Size, ECC
PRPMC750-1141	750, 233MHz	64MB DRAM, 1M L2 Cache, 8M Flash, Std. Size, ECC
PRPMC750-1231	750, 350MHz	32MB DRAM, 1M L2 Cache, 8M Flash, Std. Size, ECC
PRPMC750-1241	750, 350MHz	64MB DRAM, 1M L2 Cache, 8M Flash, Std. Size, ECC
PRPMC750-1251	750, 350MHz	128MB DRAM, 1M L2 Cache, 8M Flash, Std. Size, ECC

This manual is intended for anyone who designs OEM systems, supplies additional capability to existing compatible systems, or works in a lab environment for experimental purposes. It is important to note that a basic knowledge of computers and digital logic is assumed.

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Ground the Instrument.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. If the equipment is supplied with a three-conductor AC power cable, the power cable must be plugged into an approved three-contact electrical outlet, with the grounding wire (green/yellow) reliably connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards and local electrical regulatory codes.

Do Not Operate in an Explosive Atmosphere.

Do not operate the equipment in any explosive atmosphere such as in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment could result in an explosion and cause injury or damage.

Keep Away From Live Circuits Inside the Equipment.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified service personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Service personnel should not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, such personnel should always disconnect power and discharge circuits before touching components.

Use Caution When Exposing or Handling a CRT.

Breakage of a Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, do not handle the CRT and avoid rough handling or jarring of the equipment. Handling of a CRT should be done only by qualified service personnel using approved safety mask and gloves.

Do Not Substitute Parts or Modify Equipment.

Do not install substitute parts or perform any unauthorized modification of the equipment. Contact your local Motorola representative for service and repair to ensure that all safety features are maintained.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the equipment. Contact your local Motorola representative for service and repair to ensure that safety features are maintained.

Observe Warnings in Manual.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.



WARNING

To prevent serious injury or death from dangerous voltages, use extreme caution when handling, testing, and adjusting this equipment and its components.

Flammability

All Motorola PWBs (printed wiring boards) are manufactured with a flammability rating of 94V-0 by UL-recognized manufacturers.

EMI Caution



CAUTION

This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference (EMI) if not installed and used with adequate EMI protection.

CE Notice (European Community)



WARNING

This is a Class A product. In a domestic environment, this product may cause radio interference, in which case the user may be required to take adequate measures.

Motorola Computer Group products with the CE marking comply with the EMC Directive (89/336/EEC). Compliance with this directive implies conformity to the following European Norms:

EN55022 “Limits and Methods of Measurement of Radio Interference Characteristics of Information Technology Equipment”; this product tested to Equipment Class A

EN50082-1:1997 “Electromagnetic Compatibility—Generic Immunity Standard, Part 1. Residential, Commercial and Light Industry”

System products also fulfill EN60950 (product safety) which is essentially the requirement for the Low Voltage Directive (73/23/EEC).

Board products are tested in a representative system to show compliance with the above mentioned requirements. A proper installation in a CE-marked system will maintain the required EMC/safety performance.

In accordance with European Community directives, a "Declaration of Conformity" has been made and is on file within the European Union. The "Declaration of Conformity" is available on request. Please contact your sales representative.

This product is not a workstation per the European Ergonomic Standard.

Kein Bildschirmarbeitsplatz nach dem Europäischen Ergonomie Standard.

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Use only shielded cables when connecting peripherals to assure that appropriate radio frequency emissions compliance is maintained.

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Conventions Used in This Manual

The following typographical conventions are used in this document:

bold

is used for user input that you type just as it appears; it is also used for commands, options and arguments to commands, and names of programs, directories and files.

italic

is used for names of variables to which you assign values. Italic is also used for comments in screen displays and examples, and to introduce new terms.

`courier`

is used for system output (for example, screen displays, reports), examples, and system prompts.

<Enter>, <Return> or <CR>

represents the carriage return or Enter key.

Ctrl

represents the Control key. Execute control characters by pressing the Ctrl key and the letter simultaneously, for example, **Ctrl-d**.

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Preparation and Installation

1

Introduction

This chapter provides a brief description of the PrPMC750 Processor PMC Module and instructions for preparing and installing the hardware including the optional SDRAM memory mezzanine module.

In this manual, the name PrPMC750 refers to all models of the PrPMC750 series boards unless otherwise specified. These are add-on modules intended for use with any host carrier board that will accept a PMC or processor PMC module.

PrPMC750 Description

The PrPMC750 is a Processor PCI Mezzanine Card (processor PMC) board (refer to the VITA-32-199x Processor PMC Standard for Processor PCI Mezzanine cards for more information). It is based on the PowerPC MPC750 processor and the Hawk PCI-Host bridge/system memory controller. The PrPMC750 features 1MB of L2 Cache, one bank of SDRAM (32MB to 128MB) onboard with memory expansion capability, and 8MB of FLASH.

Four 64-pin PMC connectors on the PrPMC750 are used to connect the PrPMC750 to the host board. One right angle 20-pin connector, located on the primary side of the PrPMC750, provides an interface to the async serial port. The processor JTAG/COP port, along with the RESET# and ABORT# signals, are used for debug support. The Serial port and JTAG/COP interfaces, along with the ABORT_L signal, are also routed to the PMC P14 connector for carrier board access.

The PrPMC750 may be purchased with an optional 140-pin AMP connector installed on the bottom side of the board to provide a receptacle for the memory expansion capability. The presence of this connector increases the side two component height measurement and places it outside the standard height.

Monarch and Non-Monarch Processor PMCs

The traditional concept of host/master and slave/target processors changes with the inception of the processor PMC because the arbiter, or clock source, is traditionally located on the host board and does not reside on the PrPMC750. The VITA 32 specification defines the terms Monarch and Non-monarch to refer to these two modes of operation for processor PMCs. A Monarch processor PMC is defined as the main PCI bus processor PMC (or CPU) that performs PCI bus enumeration at power-up or reset and acts as the PCI interrupt handler. The Non-monarch is a slave/target processor that does not perform bus enumeration and does not service PCI interrupts, but may generate a PCI interrupt to the host processor.

A system may have one Monarch PrPMC750 and/or one or more Non-monarch PrPMC750s, creating a loosely coupled multiprocessing system. A PrPMC750 operating as a Monarch may be mated to a carrier board with slave processors, PCI, and other I/O devices. A PrPMC750 operating as a Non-monarch may be installed on a carrier with a host processor and other PCI devices, such as an MVME2400 or an MCPN750 board. Different versions of PPCBUG or other operating systems may be required for a PrPMC750 board operating as a Non-monarch versus the monarch mode.

The PrPMC750 software is configured to operate as either a Monarch or Non-monarch by reading the state of the MONARCH# pin on the PrPMC750. This pin is either grounded or left open on the carrier board to enable the desired mode of operation. Refer to the MONARCH# signal explanation on page 3-13 of this manual for more information.

Carrier Board Requirements

A carrier board must provide the standard PCI interface, including 3.3V and 5V power, PCI address/control, a PCI clock, and a PCI arbiter REQ/GNT pair. Refer to the VITA-32-199x spec. The carrier board must also ground the MONARCH# pin to enable the Monarch operating mode. Leaving the MONARCH# pin open will enable the Non-monarch mode.

System Enclosure

The system enclosure requirements are determined by the configuration and architecture of the baseboard (either VME, CompactPCI, or custom), and with some exceptions usually requires only a single slot for both the baseboard and the attached PrPMC750 (in a VME or CompactPCI chassis). The exception would be if the PrPMC750 contained the optional memory mezzanine board, which would place the entire PrPMC750 package 5.3mm over the allowed limit for a single slot, thereby requiring two slots or a customized chassis that would accommodate slightly wider board assemblies into each slot cavity.

Overview of Start-Up Procedures

The following table lists the things you will need to do before you can use this board and tells where to find the information you need to perform each step. Be sure to read this entire chapter and read all Caution and Warning notes before beginning.

Table 1-1. Start-Up Overview

What you need to do ...	Refer to ...
Unpack the hardware	*Unpacking the PrPMC750 Hardware* on page 1-5
Make any settings or adjustments on the PrPMC750 module	*Preparing the PrPMC750 Hardware* on page 1-5
	PrPMC750 Configuration on page 1-5
Prepare any other optional devices or equipment you will be using	For more information on optional devices and equipment, refer to the documentation provided with that equipment
Install the PrPMC750 on the baseboard	*Installation of PrPMC750 on a VME or CompactPCI Board* ***on page 1-8***
Install the Optional Memory Mezzanine on the PrPMC750	*Installation of Optional SDRAM Mezzanine on PrPMC750* ***on page 1-11***
Connect any other optional devices or equipment you will be using	*Connector Pin Assignments* on page 4-1
	For more information on optional devices and equipment, refer to the documentation provided with that equipment

Table 1-1. Start-Up Overview (Continued)

What you need to do ...	Refer to ...
Power up the system	Status Indicators
	You may also wish to obtain the ***PPCBug Diagnostics Manual***, listed in Appendix A, *Related Documentation* on page A-1
Examine the environmental parameters and make any changes needed	ENV - Set Environment
	You may also wish to obtain the ***PPCBug Firmware Package User's Manual***, listed in Appendix A, *Related Documentation* on page A-1
Program the PrPMC750 module and PMCs as needed for your applications	*Preparing the PrPMC750 Hardware* on page 1-5
	You may also wish to obtain the ***PRPMC750 Programmer's Reference Guide***, listed in Appendix A, *Related Documentation* on page A-1

Unpacking the PrPMC750 Hardware

Note If the shipping carton(s) is/are damaged upon receipt, request that the carrier's agent be present during the unpacking and inspection of the equipment.

Unpack the equipment from the shipping carton(s). Refer to the packing list(s) and verify that all items are present. Save the packing material for storing and reshipping of equipment.



Caution Avoid touching areas of integrated circuitry; static discharge can damage these circuits.

Preparing the PrPMC750 Hardware

To produce the desired configuration and ensure proper operation of the PrPMC750, you may need to carry out certain modifications before and after installing the modules.

The following paragraphs discuss the preparation of the PrPMC750 hardware components prior to installing them into a chassis and connecting them.

PrPMC750 Configuration

The PrPMC750 provides software control over most options. By setting bits in control registers after installing the PrPMC750 in a system, you can modify its configuration. The PrPMC750 control registers are described in the *PRPMC750 Processor PMC Module Programmer's Reference Guide* as listed in Table A-1, *Motorola Computer Group Documents*, in Appendix A, *Related Documentation* on page A-1.

Figure 1-1 illustrates the placement of connectors and LED indicators on the PrPMC750. The PrPMC750 has been factory tested and is shipped with the configurations described in the following sections. It contains a factory-installed debug monitor, PPCBug, which operates with those factory settings.

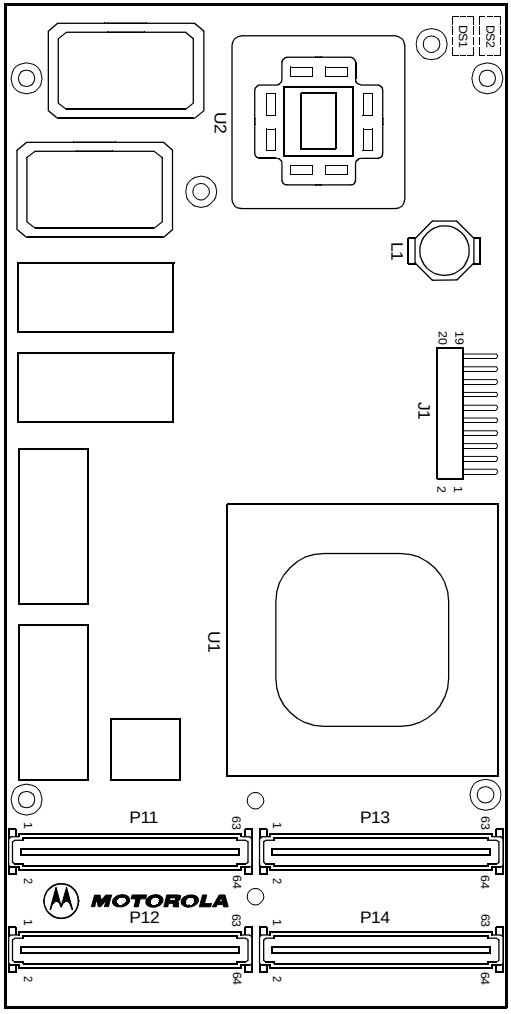


Figure 1-1. PrPMC750 Headers, Connectors, and Components

Installation

The following instructions tell how to install the PrPMC750 on a typical VME or CompactPCI single board computer and how to install the optional memory mezzanine module on the PrPMC750.

ESD Precautions

Motorola strongly recommends that you use an antistatic wrist strap and a conductive foam pad when installing or upgrading a system. Electronic components such as: disk drives, computer boards, and memory modules can be extremely sensitive to ESD. After removing the component from the system or its protective wrapper, place the component on a grounded, static-free surface (if a board, component side up). Do not slide the component over any surface.

If an ESD station is not available, you can avoid damage resulting from ESD by wearing an antistatic wrist strap (available locally) that is attached to an unpainted metal part of the system chassis.

Installation of PrPMC750 on a VME or CompactPCI Board

To install a PrPMC750 mezzanine on an VMEmodule or CompactPCI board, refer to Figure 1-2 and perform the following steps:

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove the chassis or system cover(s) as necessary to gain access to the VMEmodule or CompactPCI board.



Caution

Inserting or removing modules with power applied may result in damage to module components.

Warning

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

3. Carefully remove the VMEmodule or CompactPCI board from its card slot and place it on a clean and adequately protected working surface (preferably an ESD mat) with the backplane connectors facing you.

Caution

Avoid touching areas of integrated circuitry; static discharge can damage the circuits.

4. Place the PrPMC750 mezzanine module on top of the VMEmodule, or CompactPCI board, with the four PMC connectors on the PrPMC750 aligned with the four corresponding connectors on the baseboard. Connectors P11, P12, P13, and P14, at the bottom edge of the PrPMC750, should connect smoothly with the corresponding connectors on the VMEmodule or CompactPCI board.

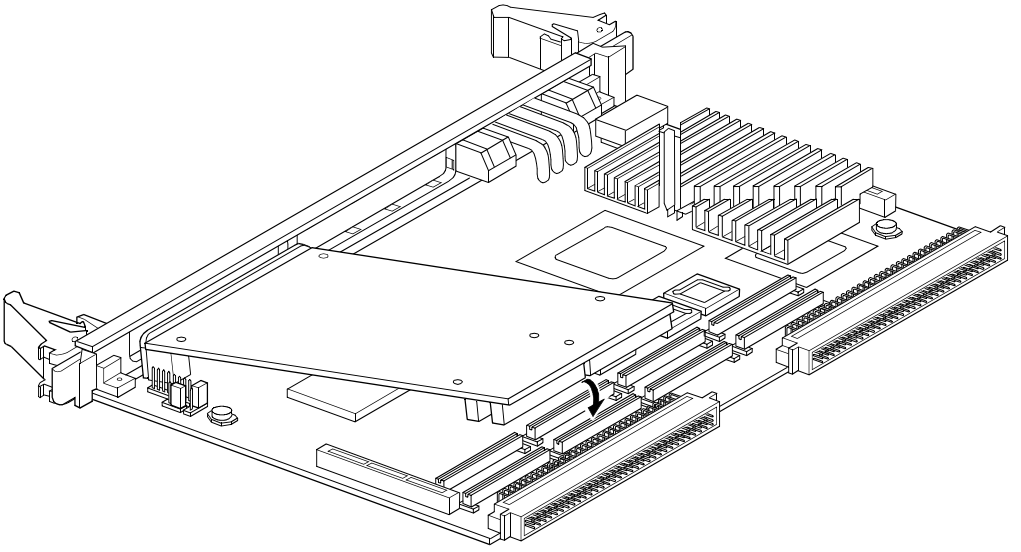


Figure 1-2. Installing a PrPMC750 on a VMEmodule

5. Align the standoffs on the PrPMC750 mezzanine with the VMEmodule or CompactPCI board and install the phillips-head screws through the holes in the base board and the spacers. Tighten the screws.

6. Install the VME or CompactPCI assembly in its proper card slot. Ensure the module is seated properly in the backplane connectors. Do not damage or bend connector pins.

7. Replace the chassis or system cover(s) and connect the system to the AC or DC power source. Turn the equipment power on.

Installation of Optional SDRAM Mezzanine on PrPMC750

The optional SDRAM mezzanine mounts on the backside (side 2) of the PrPMC750 processor module. (Note: this is possible only on a PrPMC750 assembled with the J2 memory expansion connector.) To install an SDRAM mezzanine, refer to Figure 1-3 and proceed as follows:

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the VMEmodule or CompactPCI board.

Caution

Inserting or removing modules with power applied may result in damage to module components.

Warning

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

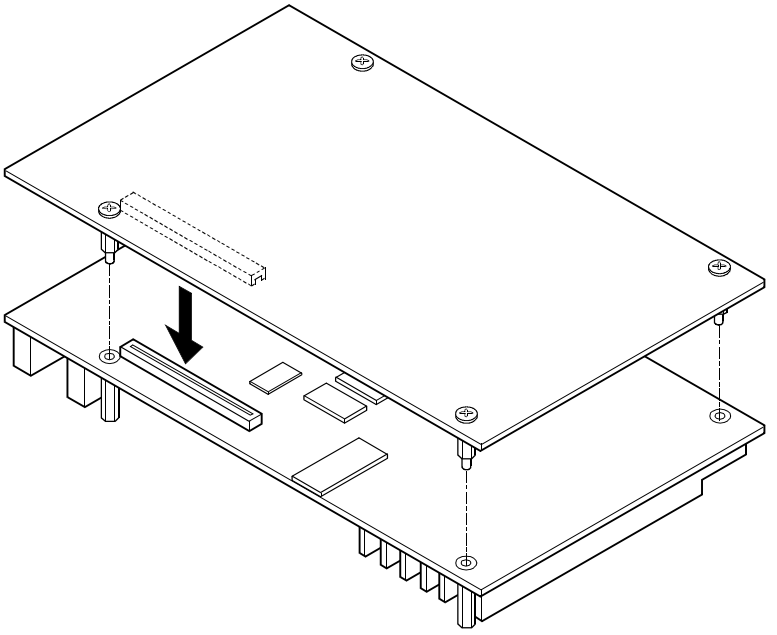


Figure 1-3. Installing SDRAM Mezzanine on PrPMC750

3. Carefully remove the VME or CompactPCI board, with the PrPMC750 installed, from its card slot and place it on a clean and adequately protected working surface (preferably an ESD mat), component side up, with the front panel facing you. Note that the ESD mat should be on a firm surface which does not bow.

Caution

Avoid touching areas of integrated circuitry; static discharge can damage these circuits

4. Remove four short phillips-head screws attached to the four standoffs, from the side of the PrPMC750 facing up. Do not remove the PrPMC750 from the carrier board.
5. Pick up the SDRAM mezzanine module and note the position of the SDRAM connector P1. Also note the position of the PrPMC750 J2 connector. Align the SDRAM connector, P1, with the corresponding connector J2 on the PrPMC750, without actually setting the SDRAM on the PrPMC750.
6. Set the SDRAM mezzanine module on top of the corresponding connector on the PrPMC750 mezzanine. Do NOT press the boards together yet.
7. Visually verify that the four screw/standoffs on the SDRAM mezzanine are aligned with the four standoff holes on the PrPMC750. Do NOT press the boards together yet.



Caution

Failure to properly align the connectors on the SDRAM and the PrPMC750 may result in damage to the module's components.

8. Place your thumbs on the top side of the SDRAM mezzanine module (in the middle of and behind the connector, P1). Press the mezzanine down with both thumbs until the SDRAM and the PrPMC750 click together.
9. Visually verify that the connector is fully seated and the four mezzanine screw/standoffs are protruding through the PrPMC750 PWB and into the standoffs.
10. Tighten the four phillips-head screws at the four corners of the SDRAM module and into the standoffs on the VME or CompactPCI board.
11. Reinstall the VME or CompactPCI assembly in its proper card slot. Be sure the module is seated properly in the backplane connectors. Do not damage or bend connector pins.

Notes When the combined PrPMC750 and memory mezzanine is installed on a VME or CompactPCI board, the total assembly violates the single board height limit. In these situations, the adjacent VME or CompactPCI slot must be left vacant for proper installation and system use.

12. Replace the chassis or system cover(s) and reconnect the system to the AC or DC power source. Turn the equipment power on.

Operating Instructions 2

Introduction

This chapter provides information about powering up the PrPMC750 system, functionality of the status indicators, and I/O ports on the PrPMC750 module.

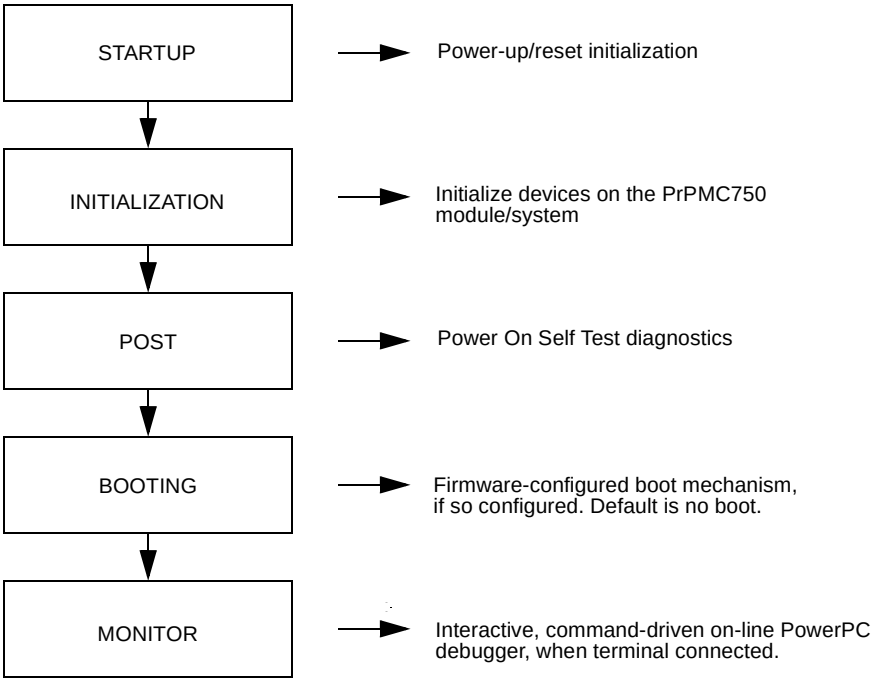
Applying Power

After you have verified that all necessary hardware preparation has been done, that all connections have been made correctly, and that the installation is complete, you can power up the system. The MPU, hardware, and firmware initialization process is performed by the PPCBug firmware at power-up or system reset. The firmware initializes the devices on the PrPMC750 module in preparation for booting the operating system.

The firmware is shipped from the factory with an appropriate set of defaults. In most cases there is no need to modify the firmware configuration before you boot the operating system. Refer to Chapter 6 for further information about modifying defaults.

The following flowchart shows the basic initialization process that takes place during PrPMC750 system start-ups.

For further information on PPCbug, refer to Chapter 5, *PPCBug on page 5-1*, or to the PPCBug documentation listed in Table A-1, *Related Documentation* on page A-1.



PrPMC750

The status indicators (LEDs) and the Debug Serial port of the PrPMC750 are described in the following sections.

Status Indicators

There are two LED (light-emitting diode) status indicators located on the secondary side of the PrPMC750 : **BFL and CPU**.

BFL (DS1)

The *yellow* **BFL** LED indicates board failure; lights when the BRDFAIL* signal line is active.

CPU (DS2)

The *green* **CPU** LED indicates CPU activity; lights when the DBB* (Data Bus Busy) signal line on the processor bus is active.

DEBUG Serial Port

A three wire Debug serial RS232 port (TXD, RXD, GND) is available on the 2mm, 20-pin right-angle header (J1), located on the primary side of the PrPMC750. Refer to Figure 2-1 for pin definitions. An optional J1 to DB9 adapter cable is available from Motorola. Contact your local Motorola Sales Office for more information or to order.

The **DEBUG** port may be used for connecting a terminal to the PrPMC750 to serve as the firmware console for the factory installed debugger, PPCBug. The port is configured as follows:

- 8 bits per character
- 1 stop bit per character
- Parity disabled (no parity)
- Baud rate = 9600 baud (default baud rate at power-up)

After power-up, the baud rate of the **DEBUG** port can be reconfigured by using the debugger's Port Format (**PF**) command. Refer to Chapters 5 and 6 for information about PPCBug.

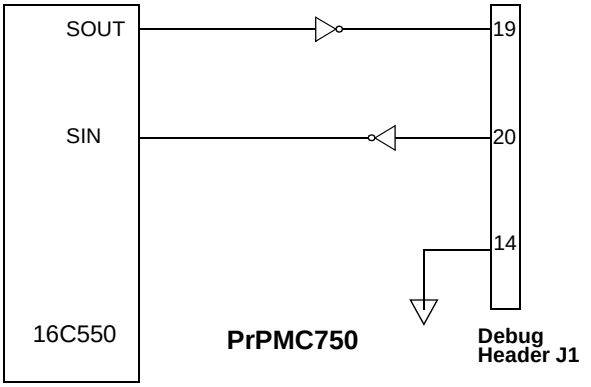


Figure 2-1. PrPMC750 DEBUG Serial Port Configuration

Functional Description 3

Introduction

This chapter describes the PrPMC750 Processor PMC Module on a block diagram level. The *General Description* on page 3-4 provides an overview of the PrPMC750, followed by a detailed description of several blocks of circuitry. Figure 3-1, *PrPMC750 Block Diagram* on page 3-5 shows a block diagram of the overall board architecture.

Detailed descriptions of other PrPMC750 blocks, including programmable registers in the ASICs and peripheral chips, can be found in the *PRPMC750 Processor PMC Module Programmer's Reference Guide* (part number PRPMC750A/PG). Refer to it for a functional description of the PrPMC750 in greater depth.

Features

The following table summarizes the features of the PrPMC750 processor module.

Table 3-1. PrPMC750 Features

Feature	Description
Processor	Single MPC750 Processor Core Frequency up to 366 MHz Bus Clock Frequencies up to 100 MHz. Address and data bus parity
L2 Cache	1MB back side L2 Cache using pipeline burst-mode SRAMS Data bus parity
FLASH	Bank A: 8 MB Soldered on-board using two 32 Mbit devices. Bank B: Second bank of FLASH (up to 64 MB) can be located on host board and accessed through the PMC P14 connector.
SDRAM	Double-Bit-Error detect, Single-Bit-Error correct across 72 bits Single bank of 16-bit wide devices onboard provide 32MB, 64MB, or 128MB SDRAM Optional memory mezzanine adds 32MB to 768MB of SDRAM
Memory Controller	Hawk's SMC (System Memory Controller)
PCI Host Bridge	Hawk's PHB (PCI Host Bridge)
Interrupt Controller	Hawk's MPIC (Multi-Processor Interrupt Controller)

Table 3-1. PrPMC750 Features (Continued)

Feature	Description
PCI Interface	32/64-bit Data 33 MHz 3.3V/5V universal signaling interface P11, P12, P13 and P14 PMC connectors Address/data parity per PCI specification
Form Factor	Single width, standard length PMC (74mm x 149 mm) Height above carrier board: Standard - 13.5mm With mezzanine connector - 15.05mm With memory mezzanine - 18.8mm
SROM	Three 256x8 I^2C SROMs for Vital Product Data, user configuration data, and memory SPD
Debug Support	One 16550-compatible async serial port with RS-232 interface Processor JTAG/COP Interface RESET and ABORT signals Signals routed to 2mm header and PMC connector P14

General Description

The PrPMC750 is a processor PMC module based on Motorola's PowerPlus II architecture. It consists of the MPC750 processor and L2 backside cache, the Hawk System Memory Controller (SMC)/PCI Host Bridge (PHB) ASIC, 8MB of FLASH memory, 32MB to 128MB of ECC-protected SDRAM on board with memory expansion capability, and a debug serial port.

The PrPMC750 module interfaces to the host board PCI bus via the PMC P11, P12, and P13 connectors, which provides a 64-bit PCI interface between the host board and the PrPMC750. The PrPMC750 module draws +5V and +3.3V through the PMC connectors. The onboard Processor Core Power Supply derives the core voltage from the +5V power. The clock generator derives all of the required onboard clocks from the PCI clock input on P11.

The PrPMC750 module has a 2mm header onboard to support module debug. This header provides the interface to the debug serial RS-232 port and an interface to the MPC750 processor JTAG/COP port.

The PrPMC750 module can function as a system controller (Monarch) for the host board or as a slave processor (Non-monarch) PMC, depending on the state of the MONARCH# signal from the PMC connector. When configured as the Monarch, the PrPMC750 will enumerate the PCI bus as well as monitor and service the four PCI interrupts.

The block diagram for the PrPMC750 module is shown in the figure on the next page.

Block Diagram

Figure 3-1 is a block diagram of the PrPMC750's overall architecture.

MPC750 Processor

The PrPMC750 can be ordered with a 233 MHz or a 350 MHz PowerPC MPC750 processor chip.

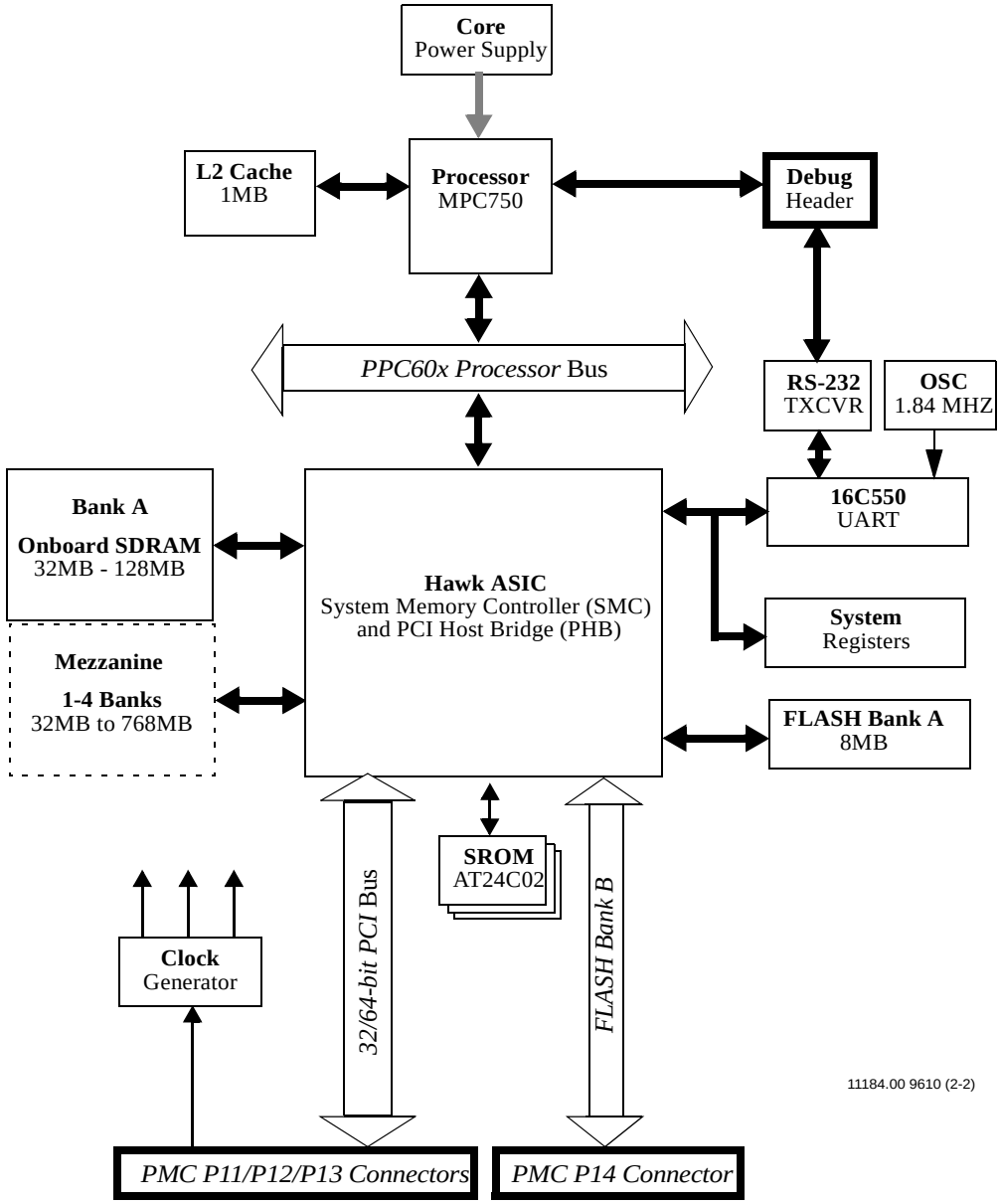


Figure 3-1. PrPMC750 Block Diagram

L2 Cache

The PrPMC750 utilizes a back-side L2 cache structure via the MPC750 processor chip. MPC750 L2 cache is implemented with an onchip 2-way set-associative tag memory and external direct-mapped synchronous SRAMs for data storage. The external SRAMs are accessed through a dedicated 72-bit wide (64 bits of data and 8 bits of parity) L2 cache port. The MPC750 processor supports 256KB, 512KB or 1MB of L2 cache SRAMs. The L2 cache can operate in copyback or writethru modes and supports system cache coherency through snooping. Data parity generation and checking can be disabled by programming the MPC750 accordingly. Refer to the MPC750 Data Sheet for additional information.

Hawk ASIC

The Hawk ASIC provides the bridge function between the PPC60X bus, the system memory, and the PCI Local Bus. The PCI interface provides 32 bit addressing and 64 bit data. PCI 64 bit addressing (dual address cycle) is not supported.

There are four programmable map decoders for each direction to provide flexible address mappings between the PowerPC and the PCI Local Bus. Refer to the *PRPMC750 Programmer's Reference Guide (PRPMC750A/PG)* for additional information and programming details.

The Hawk ASIC contains arbiters for the PPC bus and the PCI bus. The PPC arbiter will be used to arbitrate between the processor and the Hawk PPC bus master for ownership of the PPC bus. The MPC750 processor is connected to the Hawk arbiter CPU0_REQ/CPU0_GNT signal pair (XARB3/XARB0).

The Hawk PCI bus arbiter is disabled. PCI bus arbitration must be provided by the carrier board.

The Hawk ASIC also provides an MPIC Interrupt Controller to handle various interrupt sources. The interrupt sources include the four MPIC Timer Interrupts, the Watchdog timer 1 interrupt, the four PCI interrupts from the PMC connector, the two software interprocessor interrupts, and the UART interrupt. The PrPMC750 can generate an interrupt to the host processor on any of PMC interrupt lines INTA#-INTD# by activating the

Processor 1 interrupt output from MPIC. Refer to the *PRPMC750 Programmer's Reference Guide (PRPMC750A/PG)* for additional information and programming details.

FLASH Memory

The PrPMC750 supports two banks of FLASH memory. Bank A is onboard FLASH while Bank B is optional FLASH located on the carrier board and accessed through the PMC P14 connector.

Onboard Bank A FLASH

The PrPMC750 contains one bank of 16-bit FLASH memory onboard. Bank A consists of two AMD (AM29DL323C) 3.3 volt, FBGA devices configured to operate in byte-wide mode. The total size of the Bank A FLASH is 8Mbytes.

Optional Bank B FLASH

The signal interface for the Hawk ROM/FLASH Bank B, with multiplexed address bus, is routed to the PMC P14 connector to support an optional 16-bit FLASH bank on the carrier board. The Hawk ASIC will support up to 64 Mbytes of FLASH on Bank B. Device loading may restrict this size to less than 64 Mbytes. The reset vector may be sourced by either Bank A or Bank B depending on the state of Hawk ***rom_b_rv*** control bit. When the ***rom_b_rv*** bit is cleared, address range FFF00000-FFFFFFFF maps to Bank A. When ***rom_b_rv*** bit is set, it maps to Bank B. The default state uses Bank A for the reset vector. Bank B may be selected by connecting the BANKB_SEL pin on P14 to 3.3V.

ECC Memory

The PrPMC750 supports one bank of ECC SDRAM onboard and up to four additional banks of SDRAM on an optional memory mezzanine.

Onboard SDRAM

The PrPMC750 onboard ECC SDRAM memory, Bank A, consists of one bank of five, 16-bit wide, 3.3V SDRAM devices in 54-pin TSOPII packages. The total onboard memory size can be 32MB, 64MB or 128MB depending on the memory type used. Refer to the following table for memory options. The SDRAM memory is controlled by the Hawk ASIC, which provides single-bit error correction and double-bit error detection. ECC is calculated over 72-bits. Refer to the *PRPMC750 Processor PMC Module Programmer's Reference Guide (PRPMC750A/PG)* for additional information and programming details. The SDRAM memory bus operates at the same speed as the processor bus.

Table 3-2. Onboard SDRAM Memory Size Options

Bank A SDRAM Memory Size	Device Size	Device Organization	Number of Devices
32 Mbytes	64 Mbit	4Mx16	5
64 Mbytes	128 Mbit	8Mx16	5
128 Mbytes	256 Mbit	16Mx16	5

Optional Memory Mezzanines

The PrPMC750 may be populated with an optional memory expansion connector, which will allow a memory mezzanine card to be attached. The memory mezzanine connector provides signals to support from one to four additional banks of SDRAM on the mezzanine. The memory mezzanine will support two banks of 9 devices and two banks of 5 devices, as shown in Figure 3-2.

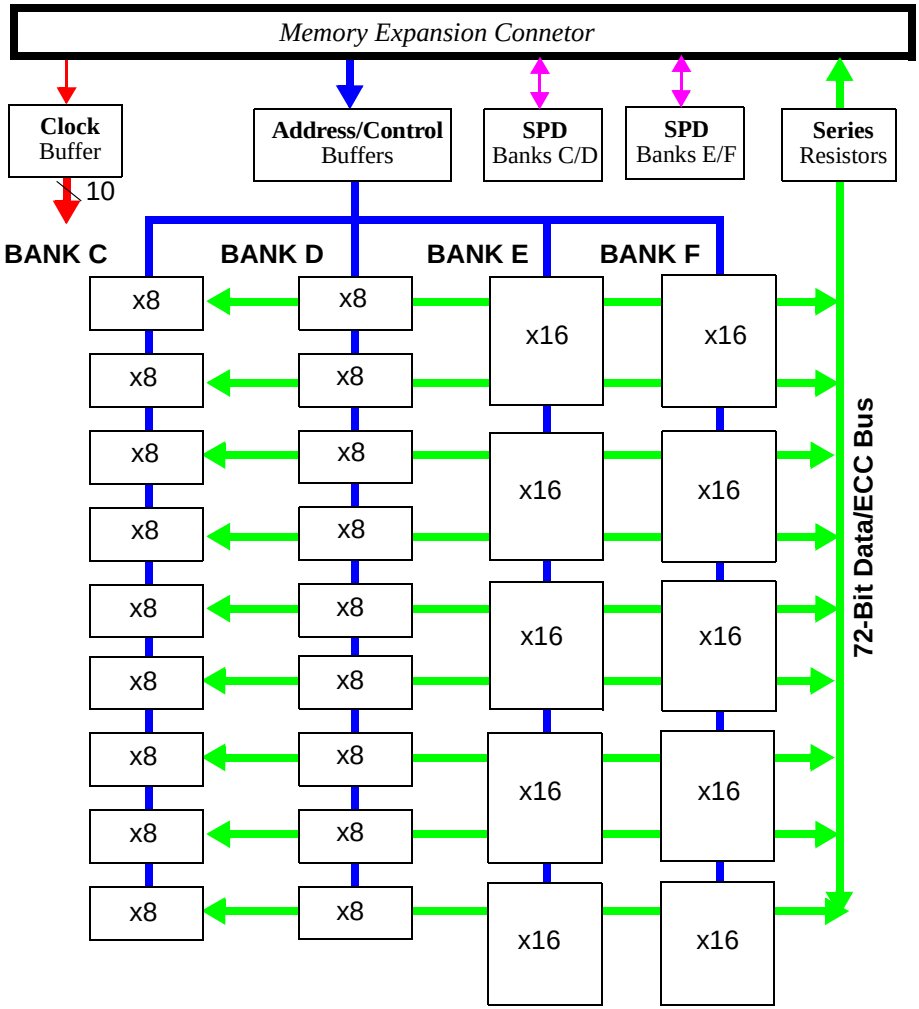


Figure 3-2. Memory Mezzanine Block Diagram

The memory mezzanine will have one or two SPD SROMs installed, depending on the number of memory banks installed; one for banks C and D and one for banks E and F. Each SROM is a 3.3V, 256 x 8, Serial EEPROM device (AT24C02) used for Serial Presence Detect (SPD) memory configuration information.

The memory mezzanine has a MPC952 PLL clock driver implemented as a zero delay buffer. This buffers the SDRAM clock from the PrPMC750 and creates 10 low skew clock outputs to drive the SDRAM devices on the mezzanine.

The addition of the memory mezzanine and the number of banks on the mezzanine may restrict the maximum operating frequency of the PPC/memory bus. The address and control lines are buffered with flow-thru buffers and the data lines are terminated with 10 ohm series resistors. Adding the memory mezzanine connector, which is located on side 2 of the PrPMC750, will extend the side 2 height above the standard 3.5 mm envelope. Therefore, the mezzanine connector is a population option only installed on versions of the PrPMC750 which are required to support memory expansion. Refer to the following table for memory size options per bank. Note that since there is only one SPD SROM for Banks C/D and one for Banks E/F, the bank pairs must use the same memory device if both banks are populated.

Table 3-3. Mezzanine SDRAM Memory Size Options

Mezzanine SDRAM Memory Size	Device Size	Device Organization	Number of Devices	Banks Installed
32 Mbytes	64 Mbit	4Mx16	5	E
64 Mbytes	64 Mbit	8Mx8	9	C
128 Mbytes	64 Mbit	8Mx8	18	C & D
256 Mbytes	128 Mbit	16Mx8	18	C & D
512 Mbytes	256 Mbit	32Mx8	18	C & D
768 Mbytes	256 Mbit	32Mx8	18	C, D
		16Mx16	10	E, F

SROM

The PrPMC750 module contains three 3.3V, 256 x 8 Serial EEPROM devices (AT24C02) onboard. One Serial EEPROM provides for Vital Product Data (VPD) storage of the module hardware configuration, one may be programmed with user defined configuration data, and the other provides for Serial Presence Detect (SPD) memory configuration information. The Serial EEPROMs are accessed through the I^2C port in the Hawk ASIC.

The I^2C port is also routed to the memory expansion connector and to pins on the P14 PMC User I/O connector. The interface to the memory expansion connector allows the processor to determine the configuration of the memory mezzanine. The connection to the PMC connector provides a means to interface to an optional configuration SROM on the carrier board. This will allow the PrPMC750, operating as the System Controller, to determine configuration information from the host board. Refer to the *PRPMC750 Programmer's Reference Guide (PRPMC750A/PG)* for SROM device address assignments and additional system configuration information.

System Registers

The PrPMC750 System Registers include the Status, Module Fail, Module Reset and PCI Interrupt registers, which provide module control and status information. Refer to the *PRPMC750 Programmer's Reference Guide* for additional details.

Timers

Timers on the PrPMC750 board are provided by the Hawk ASIC. These timers are described in the following two subsections.

32-Bit Timers

Four 32-bit timers are provided by Hawk (MPIC) that may be used for system timing or to generate periodic interrupts. Each timer is driven by a divide-by-eight prescaler, which is synchronized to the PPC processor

clock. For a 66.66 MHz processor bus, the timer frequency would be 8.33 MHz. Refer to the *PRPMC750 Programmer's Reference Guide* for additional information and programming details on these timers.

Watchdog Timers

The Hawk ASIC contains two Watchdog timers, WDT1 and WDT2. Each timer is functionally equivalent but independent. These timers will continuously decrement until they reach a count of 0 or are reloaded by software. The time-out period is programmable from 1 microsecond up to 32 minutes. If the timer count reaches 0, a timer output signal will be asserted. The output of Watchdog Timer 1 is routed to an MPIC interrupt. The output of Watchdog Timer 2 is logically ORed onboard to provide a hard reset. The onboard reset logic will provide a minimum 140 millisecond hard reset when the Watchdog Timer 2 output is asserted.

Following a device reset, WDT1 is enabled with a default time-out of 8 seconds and WDT 2 is enabled with a default time-out of 16 seconds. Each timer must be disabled or reloaded by software to prevent a time-out. Software may reload a new timer value or force the timer to reload a previously loaded value. To disable or load/reload a timer requires a two step process. Refer to the *PRPMC750 Programmer's Reference Guide* for additional timer details. PPCBug disables these timers during initialization.

Interrupt Routing and Generation

External interrupts routed to the Hawk MPIC include the four PCI interrupts INTA#-INTD#, four host board interrupts from PMC connector P14, the UART interrupt, and the output from Watchdog Timer 1. The PrPMC750 has the ability to generate any one of the PCI interrupts INTA#-INTD# by asserting the Processor 1 interrupt output from MPIC. The desired PCI interrupt is selected by programming the PCI Interrupt Select register in the System Register space. Refer to the PrPMC750 Programming Model section for the register description and interrupt assignments.

Asynchronous Serial Port

The PrPMC750 module contains one 16C550C UART device for use as a serial debug port. This serial port is wired as an RS-232 interface to the 2mm debug header. An onboard 1.8432 MHz oscillator provides the baud rate clock for the UART. The UART is accessed through the Hawk External Register Set interface. Refer to the Programming Model section for additional information.

Clock Generator

The PrPMC750 module clock generator uses an MPC972 PLL clock driver to provide the clocks for the processor, the Hawk ASIC, and the SDRAMs. All clocks are referenced to the PCI clock input on PMC connector P11.

The processor core and bus speeds listed in this document are based on a 33.33 MHz PCI bus clock input. For the 350 MHz processor version, the clock generator uses a 3x multiplier to generate the processor and memory bus clocks (100 MHz). For the 233 MHz version, a 2x multiplier is used (66 MHz processor bus).

Processor Core Power Supply

The PrPMC750 uses a switching regulator to generate the processor core voltage from the +5V input. The processor core power supply provides 2.6V for the 233 MHz processor version and 2.05V for the 350 MHz processor version.

PCI Interface

The PMC750 module contains four EIA-E700 AAAB connectors which provide a 32/64-bit PCI interface to an IEEE P1386.1 PMC or VITA 32-199x processor PMC compliant carrier board. Connectors P11-P13 provide the 32/64-bit PCI interface while P14 provides an I/O path from the module to the host board. Signals routed to P14 include the I2C bus, the RS-232 debug port, the processor JTAG/COP, and the Bank B FLASH.

PCI bus pullup resistors required by the PCI Revision 2.1 Specification, including 64-bit expansion signals, must be supplied by the carrier board. This is required if the PrPMC750 is operating as a Monarch or Non-monarch.

The following special function PMC pins, as defined by the VITA 32-199x processor PMC specification, are implemented on the PrPMC750 as described in the following sections.

PRESENT# Signal

The PRESENT# signal on the PrPMC750 module is grounded to indicate to the carrier board that the module is installed.

MONARCH# Signal

The MONARCH# input signal allows the carrier board to enable the monarch controller features on the PrPMC750 module. The PrPMC750 will pullup the MONARCH# signal. If the carrier board grounds this pin, the PrPMC750 module will operate as a monarch and provide system initialization and PCI interrupt handling. If the carrier leaves MONARCH# floating, the PrPMC750 will operate as a non-monarch.

INTA#-INTD# Signals

The four PCI interrupt signals are routed to MPIC external interrupt inputs so that they can be monitored by the processor when the PrPMC750 is operating in the Monarch mode. In the non-monarch mode, the PrPMC750 can generate an interrupt to the host board processor on any one PCI interrupt INTA#-INTD# by activating the Processor 1 interrupt output from MPIC. Refer to the interrupt section of the *PRPMC750 Programmer's Reference Guide* for interrupt assignments.

M66EN Signal

The M66EN pin is grounded on the PrPMC750 to request that the carrier board operate at 33 MHz.

RESETOUT_L Signal

The processor PMC RESETOUT_L output signal (P12-60) provides a means for the PrPMC750 to reset the carrier board. The active low open drain RESETOUT_L signal is active whenever the PrPMC750 power-up reset, Watchdog Timer 2 reset, software generated Module reset, or Debug switch reset is active. The PMC PCI reset input signal will not generate RESETOUT_L.

PCI Signaling Voltage Level

The PrPMC750 module is a universal PMC module which will operate with 3.3V or 5V signaling levels. The PMC VIO pins supply the voltage to the Hawk PCI interface clamp diode voltage pins allowing the PCI interface to operate at either voltage level.

Note The PCI clock input signal is a 3.3V only input.

ABORT# and RESET# Signals

The debug header provides ABORT# and RESET# inputs for debug purposes. The ABORT# signal is connected to the MPIC to generate an interrupt and RESET# is ORed with the board reset logic. Each signal is debounced on the PrPMC750 module.

On-Board LED's

The PrPMC750 module provides two LEDs mounted on side 2 of the module for status: CPU and FAIL.

- The green CPU LED is lit when the DBB# signal of processor bus is active.
- The yellow FAIL LED is lit when the MODFAIL signal line is active (software controlled).

Refer to the *PRPMC750 Programmer's Reference Guide* for details of the MODFAIL register.

Memory Maps

Refer to the *PRPMC750 Processor PMC Module Programmer's Reference Guide* for memory maps of the PrPMC750 processor module and the optional SRAM memory mezzanine module. The PrPMC750 is a derivative of the PowerPlus II Single Board Computer (SBC) family. The PRPMC750 Programmer's Reference Guide is based on the PowerPlus II programming model.

Connector Pin Assignments

4

Introduction

This chapter provides connector pin assignments for all connectors on the PrPMC750 board.

Memory Expansion Connector (Optional)

The optional 140-pin AMP 0.6mm Free Height receptacle is used to provide memory expansion capability. This receptacle includes common ground contacts that mate with standard AMP plug assemblies or AMP GIGA plug assemblies with ground plates. This optional connector is installed on the secondary side (side 2) of the module for memory expansion capability. The presence of this connector will violate side 2 component height specification for a standard height processor PMC. The pin assignments for this connector are as follows:

Table 4-1. J2 Memory Expansion Connector Pin Assignments

	J2		
1	GND*	GND*	2
3	DQ00	DQ01	4
5	DQ02	DQ03	6
7	DQ04	DQ05	8
9	DQ06	DQ07	10
11	+3.3V	+3.3V	12
13	DQ08	DQ09	14
15	DQ10	DQ11	16
17	DQ12	DQ13	18
19	DQ14	DQ15	20

Table 4-1. J2 Memory Expansion Connector Pin Assignments

21	GND*	GND*	22
23	DQ16	DQ17	24
25	DQ18	DQ19	26
27	DQ20	DQ21	28
29	DQ22	DQ23	30
31	+3.3V	+3.3V	32
33	DQ24	DQ25	34
35	DQ26	DQ27	36
37	DQ28	DQ29	38
39	DQ30	DQ31	40
41	GND*	GND*	42
43	DQ32	DQ33	44
45	DQ34	DQ35	46
47	DQ36	DQ37	48
49	DQ38	DQ39	50
51	+3.3V	+3.3V	52
53	DQ40	DQ41	54
55	DQ42	DQ43	56
57	DQ44	DQ45	58
59	DQ46	DQ47	60
61	GND*	GND*	62
63	DQ48	DQ49	64
65	DQ50	DQ51	66
67	DQ52	DQ53	68
69	+3.3V	+3.3V	70
71	DQ54	DQ55	72
73	DQ56	DQ57	74
75	DQ58	DQ59	76

Table 4-1. J2 Memory Expansion Connector Pin Assignments

77	DQ60	DQ61	78
79	GND*	GND*	80
81	DQ62	DQ63	82
83	CKD00	CKD01	84
85	CKD02	CKD03	86
87	CKD04	CKD05	88
89	+3.3V	+3.3V	90
91	CKD06	CKD07	92
93	BA0	BA1	94
95	A00	A01	96
97	A02	A03	98
99	GND*	GND*	100
101	A04	A05	102
103	A06	A07	104
105	A08	A09	106
107	A10	A11	108
109	+3.3V	+3.3V	110
111	A12	C0_CS_L	112
113	No Connect	D0_CS_L	114
115	WE_L	E0_CS_L	116
117	RAS_L	F0_CS_L	118
119	GND*	GND*	120
121	CAS_L	SDA	122
123	DQMB0	SCL	124
125	DQMB1	DQMB2	126
127	DQMB3	DQMB4	128
129	+3.3V	+3.3V	130
131	DQMB5	DQMB6	132

Table 4-1. J2 Memory Expansion Connector Pin Assignments

133	DQMB7	CLKEN (+3.3V)	134
135	GND	Reserved	136
137	CLK	Reserved	138
139	GND*	GND*	140

*Common GND pins mate to GIGA assembly with ground plate.

PCI Mezzanine Card (PMC) Connectors

There are four 64-pin EIA E700 AAAB SMT connectors (P11, P12, P13, and P14) on the PrPMC750 to provide the 32/64-bit PCI interface and optional I/O interface to the host board. The P14 connector provides an interface to the Bank B FLASH and I2C bus along with a secondary interface to the serial port and the JTAG/COP port. The pin assignments are as follows.

Table 4-2. PMC Connector P11 Pin Assignments

	P11		
1	TCK	-12V (not used)	2
3	GND	INTA#	4
5	INTB#	INTC#	6
7	PRESENT#	+5V	8
9	INTD#	Not Used	10
11	GND	Not Used	12
13	CLK	GND	14
15	GND	GNT#	16
17	REQ#	+5V	18
19	VIO	AD31	20
21	AD28	AD27	22

Table 4-2. PMC Connector P11 Pin Assignments

23	AD25	GND	24
25	GND	C/BE3#	26
27	AD22	AD21	28
29	AD19	+5V	30
31	VIO	AD17	32
33	FRAME#	GND	34
35	GND	IRDY#	36
37	DEVSEL#	+5V	38
39	GND	LOCK# (not used)	40
41	SDONE#	SBO# (not used)	42
43	PAR	GND	44
45	VIO	AD15	46
47	AD12	AD11	48
49	AD09	+5V	50
51	GND	C/BE0#	52
53	AD06	AD05	54
55	AD04	GND	56
57	VIO	AD03	58
59	AD02	AD01	60
61	AD00	+5V	62
63	GND	REQ64#	64

Table 4-3. PMC Connector P12 Pin Assignments

	P12		
1	+12V (not used)	TRST#	2
3	TMS	TDO	4
5	TDI	GND	6
7	GND	Not Used	8

Table 4-3. PMC Connector P12 Pin Assignments

9	Not Used	Not Used	10
11	MOT_RSVD	+3.3V	12
13	RST#	MOT_RSVD	14
15	+3.3V	MOT_RSVD	16
17	Not Used	GND	18
19	AD30	AD29	20
21	GND	AD26	22
23	AD24	+3.3V	24
25	IDSEL	AD23	26
27	+3.3V	AD20	28
29	AD18	GND	30
31	AD16	C/BE2#	32
33	GND	Not Used	34
35	TDRY#	+3.3V	36
37	GND	STOP#	38
39	PERR#	GND	40
41	+3.3V	SERR#	42
43	C/BE1#	GND	44
45	AD14	AD13	46
47	M66EN	AD10	48
49	AD08	+3.3V	50
51	AD07	Not Used	52
53	+3.3V	Not Used	54
55	MOT_RSVD	GND	56
57	MOT_RSVD	MOT_RSVD	58
59	GND	RESETOUT_L	60
61	ACK64#	+3.3V	62
63	GND	MONARCH#	64

MOT_RSVD = Motorola Reserved pin

Table 4-4. PMC Connector P13 Pin Assignments

	P13		
1	Not Used	GND	2
3	GND	C/BE7#	4
5	C/BE6#	C/BE5#	6
7	C/BE4#	GND	8
9	VIO	PAR64	10
11	AD63	AD62	12
13	AD61	GND	14
15	GND	AD60	16
17	AD59	AD58	18
19	AD57	GND	20
21	VIO	AD56	22
23	AD55	AD54	24
25	AD53	GND	26
27	GND	AD52	28
29	AD51	AD50	30
31	AD49	GND	32
33	GND	AD48	34
35	AD47	AD46	36
37	AD45	GND	38
39	VIO	AD44	40
41	AD43	AD42	42
43	AD41	GND	44
45	GND	AD40	46
47	AD39	AD38	48
49	AD37	GND	50

Table 4-4. PMC Connector P13 Pin Assignments

51	GND	AD36	52
53	AD35	AD34	54
55	AD33	GND	56
57	VIO	AD32	58
59	Not Used	Not Used	60
61	Not Used	GND	62
63	GND	Not Used	64

Table 4-5. PMC Connector P14 Pin Assignments

	P14		
1	I2CSDA	I2CSCL	2
3	TXD	RXD	4
5	CPUTDI	CPUTDO	6
7	CPUTRST_L	GND	8
9	GND	BANKB_SEL	10
11	CPUTCK	CPUTMS	12
13	SRESET_L	CPURST_L	14
15	CHKSTPO_L	FLASHOE_L	16
17	FLASHUWE_L	FLASHCS_L	18
19	FLASHLWE_L	FLASHALE_L	20
21	FLASHBA0	FLASHDBOE_L	22
23	FLASHBA1	GND	24
25	GND	FLASHRA0	26
27	FLASHRA1	FLASHRA2	28
29	FLASHRA3	FLASHRA4	30
31	FLASHRA5	FLASHRA6	32
33	FLASHRA7	FLASHRA8	34
35	FLASHRA9	FLASHRA10	36

Table 4-5. PMC Connector P14 Pin Assignments

37	FLASHRA11	FLASHRA12	38
39	No Connect	GND	40
41	GND	ABORT_L	42
43	HOSTINT0	HOSTINT1	44
45	HOSTINT2	HOSTINT3	46
47	FLASHRD0	FLASHRD1	48
49	FLASHRD2	FLASHRD3	50
51	FLASHRD4	FLASHRD5	52
53	FLASHRD6	FLASHRD7	54
55	FLASHRD8	GND	56
57	GND	FLASHRD9	58
59	FLASHRD10	FLASHRD11	60
61	FLASHRD12	FLASHRD13	62
63	FLASHRD14	FLASHRD15	64

Signal Description for P14

I2CSDA:	I2C bus serial data
I2CSCL:	I2C bus clock
TXD:	RS232 serial port transmit data
RXD:	RS232 serial port receive data
CPUTDI:	Processor RISCwatch TDI
CPUTDO:	Processor RISCwatch TDO
CPUTRST_L:	Processor RISCwatch Test Reset
CPUTCK:	Processor RISCwatch Test Clock
CPUTMS:	Processor RISCwatch Test Mode Select
SRESET_L:	Processor RISCwatch Soft Reset

CPURST_L:	Processor RISCwatch CPU Reset
CHKSTPO_L:	Processor RISCwatch CPU Checkstop Out
BANKB_SEL:	FLASH Bank B reset vector select
FLASHOE_L:	FLASH Output Enable
FLASHUWE_L:	FLASH Upper Byte Write Enable
FLASHLWE_L:	FLASH Lower Byte Write Enable
FLASHCS_L	FLASH Bank B Chip Select
FLASHALE_L	FLASH Address Latch Enable
FLASHDBOE_L	FLASH (optional) Data Buffer Output Enable
FLASHBA(0:1)	FLASH address lines
FLASHRA(0:12)	FLASH address lines
FLASHRD(0:15)	FLASH data lines
ABORT_L	ABORT interrupt
HOSTINT(0:3)	Host interrupts to PrPMC750 MPIC

Debug Header

A 2mm, 20-pin right-angle header, located on side 1 of the PrPMC750, provides the interface to the async serial port and the processor JTAG/COP port, along with the RESET# and ABORT# signals. The Serial port and JTAG/COP interfaces, along with the ABORT_L signal, are also routed to the PMC P14 connector for carrier board access. The pin assignments for this header are as follows.

Table 4-6. J1 Debug Header Pin Assignments

	J1		
1	CPUTDO	RSVD	2
3	CPUTDI	CPUTRST_L	4
5	RSVD	PULLUP	6
7	CPUTCK	RSVD	8
9	CPUTMS	RSVD	10
11	SRESET_L	DEBUGINT_L	12
13	CPURST_L	GND	14
15	CKSTPO_L	GND	16
17	RESET_L	ABORT_L	18
19	TXD	RXD	20

Signal Description for J1

TXD:	RS232 serial port transmit data
RXD:	RS232 serial port receive data
CPUTDI:	Processor RISCwatch TDI
CPUTDO:	Processor RISCwatch TDO
CPUTRST_L:	Processor RISCwatch Test Reset
CPUTCK:	Processor RISCwatch Test Clock

CPUTMS:	Processor RISCwatch Test Mode Select
SRESET_L:	Processor RISCwatch Soft Reset
CPURST_L:	Processor RISCwatch CPU Reset
CHKSTPO_L:	Processor RISCwatch CPU Checkstop out
PULLUP	1K Pullup to 3.3V for RISCwatch probe
ABORT_L	ABORT interrupt
DEBUGINT_L	Debug Interrupt input
RESET_L	Debug Reset input
RSVD	Reserved pins. Do not connect any signals to these pins.

PPCBug Overview

The PPCBug firmware is the layer of software just above the hardware. The firmware provides the proper initialization for the devices on the PrPMC750 module upon power-up or reset.

This chapter describes the basics of PPCBug and its architecture, describes the monitor (interactive command portion of the firmware) in detail, and gives information on actually using the PPCBug debugger and the special commands. A complete list of PPCBug commands appears at the end of the chapter.

Chapter 6 contains information about the CNFG and ENV commands, system calls, and other advanced user topics.

For full user information about PPCbug, refer to the *PPCBug Firmware Package User's Manual* and the *PPC1Bug Diagnostics Manual*, listed in Appendix A, *Related Documentation* on page A-1.

PPCBug Basics

The PowerPC debug firmware, PPCBug, is a powerful evaluation and debugging tool for systems built around the Motorola PowerPC microcomputers. Facilities are available for loading and executing user programs under complete operator control for system evaluation.

PPCBug provides a high degree of functionality, user friendliness, portability, and ease of maintenance.

It achieves good portability and comprehensibility because it was written entirely in the C programming language, except where necessary to use assembler functions.

PPCBug includes commands for:

- Display and modification of memory

- Breakpoint and tracing capabilities
- A powerful assembler and disassembler useful for patching programs
- A self-test at power-up feature which verifies the integrity of the system

PPCBug consists of three parts:

- A command-driven, user-interactive *software debugger*, described in the *PPCBug Firmware Package User's Manual*. It is hereafter referred to as "the debugger" or "PPCBug".
- A command-driven *diagnostics package* for the PrPMC750 hardware, hereafter referred to as "the diagnostics." The diagnostics package is described in the *PPC1Bug Diagnostics Manual.*
- A *user interface* or *debug*/*diagnostics monitor* that accepts commands from the system console terminal.

When using PPCBug, you operate out of either the *debugger directory* or the *diagnostic directory.*

- If you are in the debugger directory, the debugger prompt `<PPC6-Bug>` is displayed and you have all of the debugger commands at your disposal.
- If you are in the diagnostic directory, the diagnostic prompt `<PPC6-Diag>` is displayed and you have all of the diagnostic commands at your disposal as well as all of the debugger commands.

Because PPCBug is command-driven, it performs its various operations in response to user commands entered at the keyboard. When you enter a command, PPCBug executes the command and the prompt reappears. However, if you enter a command that causes execution of user target code (for example, **GO**), then control may or may not return to PPCBug, depending on the outcome of the user program.

Memory Requirements

PPCBug requires a maximum of 768KB of read/write memory (i.e., DRAM). The debugger allocates this space from the top of memory. For example, a system containing 64MB ($04000000) of read/write memory will place the PPCBug memory page at locations $03F40000 to $03FFFFFF.

PPCBug Implementation

PPCBug is written largely in the C programming language, providing benefits of portability and maintainability. Where necessary, assembly language has been used in the form of separately compiled program modules containing only assembler code. No mixed-language modules are used.

Physically, PPCBug is contained in two on-board Flash devices that together provide 8MB of storage. The executable code is checksummed at every power-on or reset firmware entry and the result (which includes a precalculated checksum contained in the Flash devices) is verified against the expected checksum.

MPU, Hardware, and Firmware Initialization

The debugger performs the MPU, hardware, and firmware initialization process. This process occurs each time the PrPMC750 is reset or powered up. The steps below are a high-level outline; not all of the detailed steps are listed.

1. Sets MPU.MSR to known value.
2. Invalidates the MPU's data/instruction caches.
3. Clears all segment registers of the MPU.
4. Clears all block address translation registers of the MPU.
5. Initializes the MPU-bus-to-PCI-bus bridge device.
6. Calculates the external bus clock speed of the MPU.

7. Delays for 750 milliseconds.
8. Determines the CPU base board type.
9. Sizes the local read/write memory (i.e., DRAM).
10. Initializes the read/write memory controller. Sets base address of memory to $00000000.
11. Retrieves the speed of read/write memory.
12. Initializes the read/write memory controller with the speed of read/write memory.
13. Retrieves the speed of read only memory (i.e., Flash).
14. Initializes the read only memory controller with the speed of read only memory.
15. Enables the MPU's instruction cache.
16. Copies the MPU's exception vector table from $FFF00000 to $00000000.
17. Verifies MPU type.
18. Enables the superscalar feature of the MPU (superscalar processor boards only).
19. Verifies the external bus clock speed of the MPU.
20. Determines the debugger's console/host ports and initializes the PC16550A.
21. Displays the debugger's copyright message.
22. Displays any hardware initialization errors that may have occurred.
23. Checksums the debugger object and displays a warning message if the checksum failed to verify.
24. Displays the amount of local read/write memory found.
25. Verifies the configuration data that is resident in NVRAM and displays a warning message if the verification failed.

26. Calculates and displays the MPU clock speed, verifies that the MPU clock speed matches the configuration data, and displays a warning message if the verification fails.
27. Displays the BUS clock speed, verifies that the BUS clock speed matches the configuration data, and displays a warning message if the verification fails.
28. Probes PCI bus for supported network devices.
29. Probes PCI bus for supported mass storage devices.
30. Initializes the memory/IO addresses for the supported PCI bus devices.
31. Executes Self-Test, if so configured. (Default is no Self-Test.)
32. Extinguishes the board fail LED, if Self-Test passed, and outputs any warning messages.
33. Executes boot program, if so configured. (Default is no boot.)
34. Executes the debugger monitor (i.e., issues the `PPC6-Bug>` prompt).

Using PPCBug

PPCBug is command-driven; it performs its various operations in response to commands that you enter at the keyboard. When the `<PPC6-Bug>` prompt appears on the screen, the debugger is ready to accept debugger commands. When the `<PPC6-Diag>` prompt appears on the screen, the debugger is ready to accept diagnostics commands. To switch from one mode to the other, enter **SD**.

What you key in is stored in an internal buffer. Execution begins only after you press the **Return** or **Enter** key. This allows you to correct entry errors, if necessary, with the control characters described in the *PPCBug Firmware Package User's Manual*, Chapter 1.

After the debugger executes the command, the prompt reappears. However, if the command causes execution of user target code (for example, **GO**) then control may or may not return to the debugger,

depending on what the user program does. For example, if a breakpoint has been specified, then control returns to the debugger when the breakpoint is encountered during execution of the user program. Alternately, the user program could return to the debugger by means of the System Call Handler routine RETURN (described in the *PPCBug Firmware Package User's Manual*, Chapter 5). For more information, refer to the **GD**, **GO**, and **GT** command descriptions in the *PPCBug Firmware Package User's Manual*, Chapter 3.

A debugger command is made up of the following parts:

- The command name, either uppercase or lowercase (for example, **MD** or **md**).
- Any required arguments, as specified by command.
- At least one space before the first argument. Precede all other arguments with either a space or a comma.
- One or more options. Precede an option or a string of options with a semicolon (**;**). If no option is entered, the command's default option conditions are used.

Debugger Commands

The individual debugger commands are listed in the following table. The commands are described in detail in the *PPCBug Firmware Package User's Manual*, Chapter 3.

Note You can list all the available debugger commands by entering the Help (**HE**) command alone. You can view the syntax for a particular command by entering **HE** and the command mnemonic, as listed below.

Table 5-1. Debugger Commands

Command	Description
AS	One Line Assembler
BC	Block of Memory Compare
BF	Block of Memory Fill
BI	Block of Memory Initialize
BM	Block of Memory Move
BR	Breakpoint Insert
NOBR	Breakpoint Delete
BS	Block of Memory Search
BV	Block of Memory Verify
CACHE	Modify Cache State
CM	Concurrent Mode
NOCM	No Concurrent Mode
CNFG	Configure Board Information Block
CS	Checksum
CSAR	PCI Configuration Space READ Access
CSAW	PCI Configuration Space WRITE Access
DC	Data Conversion
DS	One Line Disassembler
DU	Dump S-Records
ECHO	Echo String
ENV	Set Environment
FORK	Fork Idle MPU at Address
FORKWR	Fork Idle MPU with Registers
GD	Go Direct (Ignore Breakpoints)

Table 5-1. Debugger Commands (Continued)

Command	Description
GEVBOOT	Global Environment Variable Boot
GEVDEL	Global Environment Variable Delete
GEVDUMP	Global Environment Variable(s) Dump
GEVEDIT	Global Environment Variable Edit
GEVINIT	Global Environment Variable Initialization
GEVSHOW	Global Environment Variable(s) Display
GN	Go to Next Instruction
G, GO	Go Execute User Program
GT	Go to Temporary Breakpoint
HE	Help
IDLE	Idle Master MPU
IOC	I/O Control for Disk
IOI	I/O Inquiry
IOP	I/O Physical (Direct Disk Access)
IOT	I/O Teach for Configuring Disk Controller
IRD	Idle MPU Register Display
IRM	Idle MPU Register Modify
IRS	Idle MPU Register Set
LO	Load S-Records from Host
MA	Macro Define/Display
NOMA	Macro Delete
MAE	Macro Edit
MAL	Enable Macro Listing
NOMAL	Disable Macro Listing
MAR	Load Macros
MAW	Save Macros
MD, MDS	Memory Display
MENU	System Menu
M, MM	Memory Modify

Table 5-1. Debugger Commands (Continued)

Command	Description
MMD	Memory Map Diagnostic
MS	Memory Set
MW	Memory Write
NAB	Automatic Network Boot
NAP	Nap MPU
NBH	Network Boot Operating System, Halt
NBO	Network Boot Operating System
NIOC	Network I/O Control
NIOP	Network I/O Physical
NIOT	Network I/O Teach (Configuration)
NPING	Network Ping
OF	Offset Registers Display/Modify
PA	Printer Attach
NOPA	Printer Detach
PBOOT	Bootstrap Operating System
PF	Port Format
NOPF	Port Detach
PFLASH	Program FLASH Memory
PS	Put RTC into Power Save Mode
RB	ROMboot Enable
NORB	ROMboot Disable
RD	Register Display
REMOTE	Remote
RESET	Cold/Warm Reset
RL	Read Loop
RM	Register Modify
RS	Register Set
RUN	MPU Execution/Status
SD	Switch Directories

Table 5-1. Debugger Commands (Continued)

Command	Description
SET	Set Time and Date
SROM	SROM Examine/Modify
SYM	Symbol Table Attach
NOSYM	Symbol Table Detach
SYMS	Symbol Table Display/Search
T	Trace
TA	Terminal Attach
TIME	Display Time and Date
TM	Transparent Mode
TT	Trace to Temporary Breakpoint
VE	Verify S-Records Against Memory
VER	Revision/Version Display
WL	Write Loop



Caution Although a command to allow the erasing and reprogramming of Flash memory is available to you, keep in mind that reprogramming any portion of Flash memory will erase everything currently contained in Flash, including the PPCBug debugger.

Note NVRAM is located in Flash Bank A on the PrPMC750 board.

Diagnostic Tests

The PPCBug hardware diagnostics are intended for testing and troubleshooting the PrPMC750 module.

In order to use the diagnostics, you must switch to the diagnostic directory. You may switch between directories by using the **SD** (Switch Directories) command. You may view a list of the commands in the directory that you are currently in by using the **HE** (Help) command.

If you are in the debugger directory, the debugger prompt `<PPC6-Bug>` displays, and all of the debugger commands are available. Diagnostics commands cannot be entered at the `<PPC6-Bug>` prompt.

If you are in the diagnostic directory, the diagnostic prompt `<PPC6-Diag>` displays, and all of the debugger and diagnostic commands are available.

PPCBug's diagnostic test groups are listed in the Table 5-2. Note that not all tests are performed on the PrPMC750. Using the **HE** command, you can list the diagnostic routines available in each test group. Refer to the *PPC1Bug Diagnostics Manual* for complete descriptions of the diagnostic routines and instructions on how to invoke them.

Table 5-2. Diagnostic Test Groups

Test Group	Description
CL1283*	Parallel Interface (CL1283) Tests*
DEC**	DEC21x43 Ethernet Controller Tests
HAWK	HAWK Tests
ISABRDGE**	PCI/ISA Bridge Tests
KBD8730x*	PC8730x Keyboard/Mouse Tests*
L2CACHE	Level 2 Cache Tests
NCR**	NCR 53C8xx SCSI-2 I/O Processor Tests
PAR8730x*	Parallel Interface (PC8730x) Test*
UART	Serial Input/Output Tests
PCIBUS	PCI/PMC Generic Tests
RAM	Local RAM Tests
RTC*	MK48Txx Timekeeping Tests

Table 5-2. Diagnostic Test Groups (Continued)

Test Group	Description
SCC*	Serial Communications Controller (Z85C230) Tests*
VGA54xx**	VGA Controller (GD54xx) Tests
VME3**	VME3 (Universe) Tests
Z8536*	Z8536 Counter/Timer Tests*

Notes You may enter command names in either uppercase or lowercase.

Some diagnostics depend on restart defaults that are set up only in a particular restart mode. Refer to the documentation on a particular diagnostic for the correct mode.

Test Sets marked with an asterisk (*) are not available on the PrPMC750.

** PCI devices that are detected will be tested.

* Represent Non-PCI devices that depend on the VPD SROM to determine if a device is expected to be present. These devices are not on the PrPMC750, but could reside on a carrier board.

Modifying the Environment

6

Overview

You can use the factory-installed debug monitor, PPCBug, to modify certain parameters contained in the PrPMC750's Non-Volatile RAM (NVRAM), also known as Battery Backed-up RAM (BBRAM). NVRAM is located in the last 32K of Flash Bank A on the PrPMC750.

- The Board Information Block in NVRAM contains various elements concerning operating parameters of the hardware. Use the PPCBug command **CNFG** to change those parameters.
- Use the PPCBug command **ENV** to change configurable PPCBug parameters in NVRAM.

The **CNFG** and **ENV** commands are both described in the *PPCBug Firmware Package User's Manual*. Refer to that manual for general information about their use and capabilities.

The following paragraphs present additional information about **CNFG** and **ENV** that is specific to the PPCBug debugger, along with the parameters that can be configured with the **ENV** command.

CNFG - Configure Board Information Block

Use this command to display and configure the Board Information Block, which is resident within the NVRAM. The board information block contains various elements detailing specific operational parameters of the PrPMC750. The board structure for the PrPMC750 is as shown in the following example:

```
Board (PWA) Serial Number     = "MOT00xxxxxxx   "
Board Identifier              = "PRPMC750       "
Artwork (PWA) Identifier      = "01-w3394FxxC   "
MPU Clock Speed               = "350            "
Bus Clock Speed               = "100            "
Ethernet Address              = 08003E20xxxx
Primary SCSI Identifier       = "07"
System Serial Number          = "nnnnnnn        "
System Identifier             = "Motorola PRPMC750"
License Identifier            = "nnnnnnnn       "
```

The parameters that are quoted are left-justified character (ASCII) strings, padded with space characters. The quotes (") are displayed to indicate the size of the string. Parameters that are not quoted are considered data strings, and data strings are right-justified. The data strings are padded with zeroes if the length is not met.

The Board Information Block is factory-configured before shipment. There is no need to modify block parameters unless the NVRAM is corrupted.

Refer to the *PRPMC750 Processor PMC Module Programmer's Reference Guide* for the actual location and other information about the Board Information Block.

Refer to the *PPCBug Firmware Package User's Manual* for a description of **CNFG** and examples.

ENV - Set Environment

Use the **ENV** command to view and/or configure interactively all PPCBug operational parameters that are kept in Non-Volatile RAM (NVRAM).

Refer to the *PPCBug Firmware Package User's Manual* for a description of the use of **ENV**. Additional information on registers are contained in your *PRPMC750 Processor PMC Module Programmer's Reference Guide*.

Listed and described below are the parameters that you can configure using **ENV**. The default values shown were those in effect when this publication went to print.

Configuring the PPCBug Parameters

The parameters that can be configured using **ENV** are:

```
Bug or System environment [B/S] = B?
```

B Bug is the mode where no system type of support is displayed. However, system-related items are still available. (Default)

S System is the standard mode of operation and is the default mode if NVRAM should fail. System mode is defined in the *PPCBug Firmware Package User's Manual*.

```
Field Service Menu Enable [Y/N] = N?
```

Y Display the field service menu.

N Do not display the field service menu. (Default)

```
Probe System for Supported I/O Controllers [Y/N] = Y?
```

Y Accesses will be made to the appropriate system buses (e.g., VMEbus, local MPU bus) to determine the presence of supported controllers. (Default)

N Accesses will not be made to the VMEbus to determine the presence of supported controllers.

```
Auto-Initialize of NVRAM Header Enable [Y/N] = Y?
```

Y NVRAM (PReP partition) header space will be initialized automatically during board initialization, but only if the PReP partition fails a sanity check. (Default)

N NVRAM header space will not be initialized automatically during board initialization.

```
Network PReP-Boot Mode Enable [Y/N] = N?
```

Y Enable PReP-style network booting (same boot image from a network interface as from a mass storage device).

N Do not enable PReP-style network booting. (Default)

```
SCSI Bus Reset on Debugger Startup [Y/N] = N?
```

Y Local SCSI bus is reset on debugger setup.

N Local SCSI bus is not reset on debugger setup. (Default)

```
Primary SCSI Bus Negotiations Type [A/S/N] = A?
```

A Asynchronous SCSI bus negotiation. (Default)

S Synchronous SCSI bus negotiation.

N None.

```
Primary SCSI Data Bus Width [W/N] = N?
```

W Wide SCSI (16-bit bus).

N Narrow SCSI (8-bit bus). (Default)

```
Secondary SCSI identifier = 07?
```

Select the identifier. (Default = 07.)

```
NVRAM Bootlist (GEV.fw-boot-path) Boot Enable [Y/N] = N?
```

Y Give boot priority to devices defined in the *fw-boot-path* global environment variable (GEV).

N Do not give boot priority to devices listed in the *fw-boot-path* GEV. (Default)

Note When enabled, the GEV (Global Environment Variable) boot takes priority over all other boots, including Autoboot and Network Boot.

```
NVRAM Bootlist (GEV.fw-boot-path) Boot at power-up only [Y/N] = N?
```

Y Give boot priority to devices defined in the *fw-boot-path* GEV at power-up reset only.

N Give power-up boot priority to devices listed in the *fw-boot-path* GEV at any reset. (Default)

```
NVRAM Bootlist (GEV.fw-boot-path) Boot Abort Delay = 5?
```

The time in seconds that a boot from the NVRAM boot list will delay before starting the boot. The purpose for the delay is to allow you the option of stopping the boot by use of the **BREAK** key. The time value is from 0-255 seconds. (Default = 5 seconds)

```
Auto Boot Enable [Y/N]   = N?
```

Y The Autoboot function is enabled.

N The Autoboot function is disabled. (Default)

```
Auto Boot at power-up only [Y/N] = N?
```

Y Autoboot is attempted at power-up reset only.

N Autoboot is attempted at any reset. (Default)

```
Auto Boot Scan Enable [Y/N]   = Y?
```

Y If Autoboot is enabled, the Autoboot process attempts to boot from devices specified in the scan list (e.g., FDISK/CDROM/TAPE/HDISK). (Default)

N If Autoboot is enabled, the Autoboot process uses the Controller LUN and Device LUN to boot.


```
Auto Boot Scan Device Type List = FDISK/CDROM/TAPE/HDISK?
```

This is the listing of boot devices displayed if the Autoboot Scan option is enabled. If you modify the list, follow the format shown above (uppercase letters, using forward slash as separator).

```
Auto Boot Controller LUN   = 00?
```

Refer to the *PPCBug Firmware Package User's Manual* for a listing of disk/tape controller modules currently supported by PPCBug. (Default = $00)

```
Auto Boot Device LUN    = 00?
```

Refer to the *PPCBug Firmware Package User's Manual* for a listing of disk/tape devices currently supported by PPCBug. (Default = $00)

```
Auto Boot Partition Number = 00?
```

Which disk "partition" is to be booted, as specified in the PowerPC Reference Platform (PRP) specification. If set to zero, the firmware will search the partitions in order (1, 2, 3, 4) until it finds the first "bootable" partition. That is then the partition that will be booted. Other acceptable values are 1, 2, 3, or 4. In these four cases, the partition specified will be booted without searching.

```
Auto Boot Abort Delay = 7?
```

The time in seconds that the Autoboot sequence will delay before starting the boot. The purpose for the delay is to allow you the option of stopping the boot by use of the **BREAK** key. The time value is from 0-255 seconds. (Default = 7 seconds)

```
Auto Boot Default String [NULL for an empty string] = ?
```

You may specify a string (filename) which is passed on to the code being booted. The maximum length of this string is 16 characters. (Default = null string)

```
ROM Boot Enable [Y/N] = N?
```

Y	The ROMboot function is enabled.
N	The ROMboot function is disabled. (Default)

```
ROM Boot at power-up only [Y/N] = Y?
```

Y	ROMboot is attempted at power-up only. (Default)
N	ROMboot is attempted at any reset.

```
ROM Boot Abort Delay = 5?
```

The time in seconds that the ROMboot sequence will delay before starting the boot. The purpose for the delay is to allow you the option of stopping the boot by use of the **BREAK** key. The time value is from 0-255 seconds. (Default = 5 seconds)

```
ROM Boot Direct Starting Address = FFF00000?
```

The first location tested when PPCBug searches for a ROMboot module. (Default = $FFF00000)

```
ROM Boot Direct Ending Address = FFFFFFFC?
```

The last location tested when PPCBug searches for a ROMboot module. (Default = $FFFFFFFC)

```
Network Auto Boot Enable [Y/N] = N?
```

Y The Network Auto Boot (NETboot) function is enabled.

N The NETboot function is disabled. (Default)

```
Network Auto Boot at power-up only [Y/N] = N?
```

Y NETboot is attempted at power-up reset only.

N NETboot is attempted at any reset. (Default)

```
Network Auto Boot Controller LUN = 00?
```

Refer to the *PPCBug Firmware Package User's Manual* for a listing of network controller modules currently supported by PPCBug. (Default = $00)

```
Network Auto Boot Device LUN = 00?
```

Refer to the *PPCBug Firmware Package User's Manual* for a listing of network controller modules currently supported by PPCBug. (Default = $00)

```
Network Auto Boot Abort Delay = 5?
```

The time in seconds that the NETboot sequence will delay before starting the boot. The purpose for the delay is to allow you the option of stopping the boot by use of the **BREAK** key. The time value is from 0-255 seconds. (Default = 5 seconds)

```
Network Auto Boot Configuration Parameters Offset (NVRAM) =
00001000?
```

The address where the network interface configuration parameters are to be saved/retained in NVRAM; these parameters are the necessary parameters to perform an unattended network boot. A typical offset might be $1000, but this value is application-specific. (Default = $00001000)



Caution

If you use the **NIOT** debugger command, these parameters need to be saved somewhere in the offset range $00001000 through $000016F7. The **NIOT** parameters do not exceed 128 bytes in size. The setting of this ENV pointer determines their location. If you have used the same space for your own program information or commands, they will be overwritten and lost.

You can relocate the network interface configuration parameters in this space by using the **ENV** command to change the Network Auto Boot Configuration Parameters Offset from its default of $00001000 to the value you need to be clear of your data within NVRAM.

Note This number is still an offset within NVRAM. However, the NVRAM image for Bug is stored at the end of Flash Bank A (in the last 32K).

```
Memory Size Enable [Y/N] = Y?
```

Y Memory will be sized for Self Test diagnostics. (Default)

N Memory will not be sized for Self Test diagnostics.

```
Memory Size Starting Address = 00000000?
```

The default Starting Address is $00000000.

```
Memory Size Ending Address = 02000000?
```

The default Ending Address is the calculated size of local memory. If the memory start is changed from $00000000, this value will also need to be adjusted.

```
DRAM Speed in NANO Seconds = 60?
```

The default setting for this parameter will vary depending on the speed of the DRAM memory parts installed on the board. The default is set to the slowest speed found on the available banks of DRAM memory.

```
ROM First Access Length (0 - 31) = 10?
```

This is the value programmed into the“ROMFAL” field (Memory Control Configuration Register 8: bits 23-27) to indicate the number of clock cycles used in accessing the ROM. The lowest allowable ROMFAL setting is $00; the highest allowable is $1F. The value to enter depends on processor speed; refer to Chapter 1 or Appendix B for appropriate values. The default value varies according to the system’s bus clock speed.

Note ROM First Access Length is not applicable to the PrPMC750. The configured value is ignored by PPCBug.

```
ROM Next Access Length (0 - 15) = 0?
```

The value programmed into the“ROMNAL” field (Memory Control Configuration Register 8: bits 28-31) to represent wait states in access time for nibble (or burst) mode ROM accesses. The lowest allowable ROMNAL setting is $0; the highest allowable is $F. The value to enter depends on processor speed; refer to Chapter 1 or Appendix B for appropriate values. The default value varies according to the system’s bus clock speed.

Note ROM Next Access Length is not applicable to the PrPMC750. The configured value is ignored by PPCBug.

```
DRAM Parity Enable [On-Detection/Always/Never - O/A/N] = O?
```

O DRAM parity is enabled upon detection. (Default)

A DRAM parity is always enabled.

N DRAM parity is never enabled.

Note This parameter (above) also applies to enabling ECC for DRAM.

```
L2 Cache Parity Enable [On-Detection/Always/Never - O/A/N] = O?
```

O L2 Cache parity is enabled upon detection. (Default)

A L2 Cache parity is always enabled.

N L2 Cache parity is never enabled.

```
PCI Interrupts Route Control Registers (PIRQ0/1/2/3) = 0A0B0E0F?
```

Initializes the PIRQx (PCI Interrupts) route control registers in the IBC (PCI/ISA bus bridge controller). The **ENV** parameter is a 32-bit value that is divided by 4 to yield the values for route control registers PIRQ0/1/2/3. The default is determined by system type.

Note LED/Serial Startup Diagnostic Codes: these codes can be displayed at key points in the initialization of the hardware devices. Should the debugger fail to come up to a prompt, the last code displayed will indicate how far the initialization sequence had progressed before stalling. **Due to limitations imposed by storing the ENV parameters in Flash, the Serial Startup codes are disabled for PrPMC750.** The codes are enabled by an **ENV** parameter:

```
Serial Startup Code Master Enable [Y/N]=N?
```

A line feed can be inserted after each code is displayed to prevent it from being overwritten by the next code. This is also enabled by an **ENV** parameter:

```
Serial Startup Code LF Enable [Y/N]=N?
```

The list of LED/serial codes is included in the section on *MPU, Hardware, and Firmware Initialization* in Chapter 1 of the *PPCBug Firmware Package User's Manual*.

Related Documentation A

Motorola Computer Group Documents

The Motorola publications listed below are referenced in this manual. You can obtain paper or electronic copies of Motorola Computer Group publications by:

- Contacting your local Motorola sales office
- Visiting Motorola Computer Group's World Wide Web literature site, http://www.motorola.com/computer/literature.

Table A-1. Motorola Computer Group Documents

Document Title	Motorola Publication Number
PrPMC750 Processor Programmer's Reference Guide	PRPMC750A/PG
MVME2400-Series VME Processor Module Programmer's Reference Guide	V2400A/PG
MVME2400-Series SBC Installation and Use	V2400A/IH
MCPN750 CompactPCI SBC Installation and Use	MCPN750A/IH
MCPN750 SBC Programmer's Reference Guide	MCPN750A/PG
PPCBug Firmware Package User's Manual (Parts 1 and 2)	PPCBUGA1/UM PPCBUGA2/UM
PPC1Bug Diagnostics Manual	PPC1DIAA/UM

To obtain the most up-to-date product information in PDF or HTML format, visit http://www.motorola.com/computer/literature.

Manufacturers' Documents

For additional information, refer to the following table for manufacturers' data sheets or user's manuals. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice.

Table A-2. Manufacturers' Documents

Document Title and Source	Publication Number
MPC750™ RISC Microprocessor Technical Summary Motorola Literature Distribution Center Telephone: (800) 441-2447 or (303) 675-2140 FAX: (602) 994-6430 or (303) 675-2150 E-mail: ldcformotorola@hibbertco.com	MPC750/D
MPC750™ RISC Microprocessor User's Manual Literature Distribution Center for Motorola Semiconductor Products Telephone: (800) 441-2447 FAX: (602) 994-6430 or (303) 675-2150 E-mail: ldcformotorola@hibbertco.com OR IBM Microelectronics Mail Stop A25/862-1 PowerPC Marketing 1000 River Street Essex Junction, Vermont 05452-4299 Telephone: 1-800-PowerPC Telephone: 1-800-769-3772 FAX: 1-800-POWERfax FAX: 1-800-769-3732	MPC750UM/AD MPR604UMU-01

Table A-2. Manufacturers' Documents (Continued)

Document Title and Source	Publication Number
PowerPC™ Microprocessor Family: The Programming Environments Motorola Literature and Printing Distribution Services P.O. Box 20924 Phoenix, Arizona 85036-0924 Telephone: (602) 994-6561 FAX: (602) 994-6430 OR IBM Microelectronics Mail Stop A25/862-1 PowerPC Marketing 1000 River Street Essex Junction, Vermont 05452-4299 Telephone: 1-800-PowerPC Telephone: 1-800-769-3772 FAX: 1-800-POWERfax FAX: 1-800-769-3732	MPCFPE/D MPRPPCFPE-01
Texas Instruments TI16C550C Asynchronous Communications Element - March 1994. Revised March 1997 Texas Instruments P.O. Box 655303 Dallas, TX 75265	SLLS177C
ATMEL Nonvolitile Memory Data Book Atmel Corporation 2325 Orchord Parkway San Jose, CA 95131 Telephone: (408) 441-0311 FAX: (408) 436-4300 Website: http://www.atmel.com	AT24C04
AM29DL32xC 32 Mbit CMOS 3.0 Volt-only, Simultaneous Operation FLASH Memory AMD One AMD Place Sunnyvale, CA 94088-3453 www.amd.com	21524 Rev B, Oct 98

Related Specifications

For additional information, refer to the following table for related specifications. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice.

Table A-3. Related Specifications

Document Title and Source	Publication Number
IEEE - Common Mezzanine Card Specification (CMC) Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	P1386
IEEE - PCI Mezzanine Card Specification (PMC) Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	P1386.1
IEEE Standard for Local Area Networks: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	IEEE 802.3

Table A-3. Related Specifications (Continued)

Document Title and Source	Publication Number
Peripheral Component Interconnect (PCI) Local Bus Specification, Revision 2.1 PCI Special Interest Group 2575 NE Kathryn St #17 Hillsboro, OR 97124 Telephone: (800) 433-5177 (inside the U.S.) or (503) 693-6232 (outside the U.S.) FAX: (503) 693-8344	PCI Local Bus Specification
Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange (EIA-232-D) Electronic Industries Association Engineering Department 2001 Eye Street, N.W. Washington, D.C. 20006	ANSI/EIA-232-D Standard
PowerPC Reference Platform (PRP) Specification, Third Edition, Version 1.0, Volumes I and II International Business Machines Corporation Power Personal Systems Architecture 11400 Burnet Rd. Austin, TX 78758-3493 Document/Specification Ordering Telephone: 1-800-PowerPC Telephone: 1-800-769-3772 Telephone: 708-296-9332	MPR-PPC-RPU-02
Proposed Standard Physical and Environmental Layers for PCI Processor Mezzanine Cards: processor PMC VITA Standards Organization 7825 E. Gelding Dr. Suite 104 Scottsdale, AZ 85260 www.vita.com	*VITA32 Draft 0.2*

URLs

The following URLs (uniform resource locators) may provide helpful sources of additional information about this product, related services, and development tools. Please note that, while these URLs have been verified, they are subject to change without notice.

- Motorola Computer Group, http://www.motorola.com/computer
- Motorola Computer Group OEM Services, http://www.motorola.com/computer/support

Specifications

This appendix provides general specifications, including mechanical, electrical, and temperature for the PrPMC750 and the memory mezzanine.

Mechanical Characteristics

The mechanical outline of the PrPMC750 module will conform to the dimensions defined by a single wide, standard length PMC module (74mm x 149mm x 10mm stacking height). The side 2 component height of the PrPMC750, without the optional memory mezzanine connector or memory mezzanine, will conform to the standard side 2 height dimension (3.5mm). The PrPMC750 with the memory mezzanine will fit within the tall PMC envelope (20 mm). See Table B-1 on page B-2.

Electrical Characteristics

The voltage requirements and estimated power consumption for the PrPMC750 are shown in the following table. The total power dissipation for the PrPMC750 configured with a 350 MHz processor is 8.6 watts typical, 12.5 watts max.

Airflow Requirements

The PrPMC750 module requires a minimum air flow of 450 LFM when operating at 55 degrees C ambient temperature.

B

Table B-1. PrPMC750 Specifications

Characteristics	Specifications
+3.3Vdc (±5%)	(for MPC750 @ 350MHz/100MHz bus) 1.0A, typical 1.50A, max (for MPC750 @ 233MHz/66MHz bus) 0.80A typical/1.20A maximum
+5.0Vdc (±5%)	(for MPC750 @ 350MHz/100MHz bus) 1.05A, typical, 1.50A max (for MPC750 @ 233MHz/66MHz bus) 1.30A typical, 1.90A, max
Operating temperature (refer to Cooling Requirements section)	0^{o} to 55^{o} C at point of exit of forced air
Storage Temperature	-40^{o} to $+85^{o}$ C
Relative Humidity	5% to 90% (non-condensing)
Physical Dimensions (DRAM Memory module only)	Width: 74mm (2.91 inches) Length: 149mm (5.87 inches) Height (above carrier): Standard: 13.5mm (0.53 inches) with mezzanine connector: 15.05mm (0.59 in.)

Table B-2. Processor PMC Memory Mezzanine Specifications

Characteristics	Specifications
Power requirements (DRAM Memory module only)	(for MPC750 @ 350MHz/100MHz bus) 3.3Vdc (±5%) (@ 100MHz bus) 32MB: 300mA typical, 450mA max 64MB: 400mA typical, 600mA max 128MB: 500mA typical, 750mA max
Operating temperature (refer to Cooling Requirements section)	0^{o} to 55^{o} C at point of exit of forced air
Storage Temperature	-40^{o} to $+85^{o}$ C
Relative Humidity	5% to 90% (non-condensing)
Physical Dimensions (DRAM Memory module only)	Width: 74mm (2.91 inches) Length: 145.8mm (5.74 inches) PrPMC750/Memory Mezzanine height above carrier: 18.8mm (0.74 in)

Cooling Requirements

The PrPMC750 module is specified, designed, and tested to operate reliably when mounted on a carrier board with an incoming air temperature range from 0° to 55° C (32° to 131° F) with forced air cooling at a velocity typically achievable by using a 100 CFM axial fan.

Temperature qualification is performed in a standard Motorola VMEsystem chassis. Thirty-six watt load boards are inserted in two card slots, one on each side, adjacent to the board under test, to simulate a high power density system configuration. An assembly of two axial fans, rates at 100 CFM per fan, is placed directly under the VME card cage. The incoming air temperature is measured between the fan assembly and the card cage, where the incoming airstream first encounters the module under test. Test software is executed in order to exercise the board under test. Case temperatures of critical, high power density integrated circuits are monitored to ensure component vendors specifications are not exceeded.

While the exact amount of airflow required for cooling depends on the ambient air temperature and the type, number, and location of boards and other heat sources, adequate cooling can usually be achieved with 10 CFM and 450 LFM flowing over the module. Less airflow is required to cool the module in environments having lower maximum ambients. Under more favorable thermal conditions, it may be possible to operate the module reliably at higher than 55° C with increased airflow.

It is important to note that there are several factors, in addition to the rated CFM of the air mover, which determine the actual volume and speed of air flowing over a module.

B

EMC Compliance

The PrPMC750 is an add-on module meant to be used in conjunction with standard VME or CompactPCI baseboard applications. As such, it is the responsibility of the OEM to meet the regulatory guidelines as determined by their application.

The PrPMC750 has been tested in conjunction with a standard MCG baseboard and chassis for CE certification and meets the requirements for EN55022 Class A equipment. Compliance was achieved under the following conditions:

- Shielded cables on all external I/O ports.
- Cable shields connected to earth ground via metal shell connectors bonded to a conductive module front panel.
- Conductive chassis rails connected to earth ground. This provides the path for connecting shields to earth ground.
- Front panel screws properly tightened.

For minimum RF emissions, it is essential that the conditions above be implemented. Failure to do so could compromise the EMC compliance of the equipment containing the module.

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