68XX(X) And The STD BUS

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Hopefully you are reading this in the January issue of 68 Micro. With the holiday season upon us and all kinds of things to finish before the end of the year, this is being sent out at the last possible minute. Last month (or two months ago), I said I would discuss the Motorola I/O channel to STD interface board we have developed at BWI, including a description of the circuitry used to connect the two different buses. As I start to write this, it seems it will be better to first give a brief description of the I/O channel, and review some products that use it.

The Motorola Remote I/O Channel (RIOC) is intended to allow the connection of inexpensive input and output devices to VME bus or other high performance computer systems. It is a very simple bus structure that includes 12 address lines (A0 - A11), eight bidirectional data lines (D0 - D7), four prioritized interrupt request lines (INT1* - INT4*), a data strobe line (STB*) , a write line (WT*), a data acknowledge line (XACK*), a 4MHz clock (CLK), and a reset line (IORES*). A "*" after a signal name indicates that the signal is active low. A system includes a single bus master and up to sixteen slave devices. The limitation on the number of slaves is to ensure that the bus drivers are not overloaded.

The I/O channel system bus, or "backplane", is typically a ribbon cable, although it may also be implemented as a regular PC-board type backplane. The cable may be a 50 conductor or 64 conductor cable, and can extend as far as 12 feet. The use of a 64 conductor cable allows the master to supply 5 volt and positive and negative 12 volt power to slave pc boards. If slave subsystems have their own power supplies, the 50 conductor cable carries all the data, address, and control signals. The signals are arranged so that the 50 conductor cable is a subset of the 64 conductor cable, making it relatively easy to interconnect the two types of slaves by splitting a 64 conductor cable into a 50 conductor cable and a 14 conductor cable. Each slave is responsible for decoding and responding to its own I/O address.

Data transfers are accomplished rather simply on the I/O channel. For a read cycle, the master sets up the address lines and then asserts STB*. When the addressed slave has placed the data on the data lines, the slave asserts XACK*. The master deasserts STB* to complete the cycle, followed by the slave deasserting XACK*. A write cycle is similar, except that the master asserts WT* and puts the data to be written on the data lines before asserting STB*, and the slave asserts XACK* when it has latched the data from the data bus. Slaves may interrupt the master by driving one of the interrupt lines low. Each slave which generates interrupts must have a status register the master can read to determine if the slave generated a particular interrupt. The method of clearing an interrupt depends on the design of the particular slave, and may be accomplished by either writing or reading a specified location. Interrupts are normally also cleared whenever the master asserts IORES*, which initializes all the slave devices. The CLK line provides a nominal 4 MHz clock which may be used for timing purposes by the slave devices. Data transfers, however, are asynchronous and do not depend on the CLK signal. For detailed specifications and timing information refer to the I/O Channel Specification Manual, Motorola publication number M68RIOCS/D2.

Motorola provides a number of board level products that can serve as bus masters for the I/O channel. The MVME104 and the MVME110 are two VME bus processor boards that support the I/O channel. The MVME110 is a 68000 based CPU board that includes eight 28-pin sockets for EPROM and static RAM, a 6850 ACIA, and a 6840 counter/timer. The board will function as the system controller in a single CPU system, or can be used in multi-processor systems. Rows A and C of the P2 connector are used for the I/O channel interface. The MVME104 is one of the MVME105 family of CPU boards, and includes a 68010 processor, 512 Kbytes of dual-access dynamic RAM, two 28 pin sockets dedicated to EPROM and two 28 pin sockets that support static RAM or a real-time clock (Dallas Semiconductor type) as well as EPROM. A Zilog