ARTISAN®
TECHNOLOGY GROUP

Your **definitive** source for quality pre-owned equipment.

Artisan Technology Group
(217) 352-9330 | sales@artisantg.com | artisantg.com

Full-service, independent repair center
with experienced engineers and technicians on staff.

We buy your excess, underutilized, and idle equipment
along with credit for buybacks and trade-ins.

Custom engineering
so your equipment works exactly as you specify.

- Critical and expedited services
- In stock / Ready-to-ship
- Leasing / Rentals / Demos
- ITAR-certified secure asset solutions

Expert team | Trust guarantee | 100% satisfaction

All trademarks, brand names, and brands appearing herein are the property of their respective owners.

Find the *Emerson / Motorola MVME5500-0163* at our website: ***Click HERE***

Embedded Computing for
Business-Critical Continuity™

MVME5500 Single Board Computer

Programmer's Reference Guide

P/N: 6806800H16A
October 2009

EMERSON.
Network Power

© 2009 Emerson

All rights reserved.

Trademarks

Emerson, Business-Critical Continuity, Emerson Network Power and the Emerson Network Power logo are trademarks and service marks of Emerson Electric Co. © 2009 Emerson Electric Co. All other product or service names are the property of their respective owners.

Intel® is a trademark or registered trademark of Intel Corporation or its subsidiaries in the United States and other countries.

Java™ and all other Java-based marks are trademarks or registered trademarks of Sun Microsystems, Inc. in the U.S. and other countries.

Microsoft®, Windows® and Windows Me® are registered trademarks of Microsoft Corporation; and Windows XP™ is a trademark of Microsoft Corporation.

PICMG®, CompactPCI®, AdvancedTCA™ and the PICMG, CompactPCI and AdvancedTCA logos are registered trademarks of the PCI Industrial Computer Manufacturers Group.

UNIX® is a registered trademark of The Open Group in the United States and other countries.

Notice

While reasonable efforts have been made to assure the accuracy of this document, Emerson assumes no liability resulting from any omissions in this document, or from the use of the information obtained therein. Emerson reserves the right to revise this document and to make changes from time to time in the content hereof without obligation of Emerson to notify any person of such revision or changes.

Electronic versions of this material may be read online, downloaded for personal use, or referenced in another document as a URL to a Emerson website. The text itself may not be published commercially in print or electronic form, edited, translated, or otherwise altered without the permission of Emerson,

It is possible that this publication may contain reference to or information about Emerson products (machines and programs), programming, or services that are not available in your country. Such references or information must not be construed to mean that Emerson intends to announce such Emerson products, programming, or services in your country.

Limited and Restricted Rights Legend

If the documentation contained herein is supplied, directly or indirectly, to the U.S. Government, the following notice shall apply unless otherwise agreed to in writing by Emerson.

Use, duplication, or disclosure by the Government is subject to restrictions as set forth in subparagraph (b)(3) of the Rights in Technical Data clause at DFARS 252.227-7013 (Nov. 1995) and of the Rights in Noncommercial Computer Software and Documentation clause at DFARS 252.227-7014 (Jun. 1995).

Contact Address

Emerson Network Power - Embedded Computing

2900 South Diablo Way, Suite 190

Tempe, AZ 85282

USA

Contents

About this Manual 9

1 Board Description and Memory Maps 13

1.1 Introduction 13
1.2 Overview 13
1.3 Memory Maps 16
1.3.1 Default Processor Memory Map 16
1.3.2 MOTLoad's Processor Memory Map 17
1.3.3 Default PCI Memory Map 18
1.3.4 MOTLoad's PCI Memory Maps 19
1.3.5 PCI I/O Space Maps 20
1.3.6 System I/O Memory Map 20
1.3.7 System Status Register 1 21
1.3.8 System Status Register 2 22
1.3.9 System Status Register 3 24
1.3.10 Presence Detect Register 24
1.3.11 Configuration Header/Switch Register (S1) 25
1.3.12 Time Base Enable Register 26
1.3.13 Geographical Address Register (S2) 27
1.3.14 COM1 & COM2 Universal Asynchronous Receiver/Transmitter (UART) 28
1.3.15 Real-Time Clock and NVRAM 28
1.4 ISA Local Resource Bus 28

2 Programming Details 29

2.1 Introduction 29
2.2 PCI Configuration Space and IDSEL Mapping 30
2.3 Interrupt Controller 31
2.4 Two-Wire Serial Interface 33
2.5 GT-64260B Initialization 34
2.6 GT-64260B GPP Configuration 34
2.7 GT-64260B Reset Configuration 36
2.8 GT-64260B Device Controller Bank Assignments 39
2.9 System Clock Generators 40
2.10 VPD and User Configuration EEPROMs 40

2.11 Temperature Sensor 41
2.12 Flash Memory 41
2.13 PCI Arbitration Assignments 41
2.14 Other Software Considerations 42
2.14.1 CPU Bus Mode 42
2.14.2 Processor Type Identification 42
2.14.3 Processor PLL Configuration 42
2.14.4 L1, L2, L3 Cache 43

A Vital Product Data 45

A.1 Flash Memory Configuration Data 45
A.2 L3 Cache Configuration Data 47

B Related Documentation 49

B.1 Emerson Network Power - Embedded Computing Documents 49
B.2 Manufacturer's Documents 50
B.3 Related Specifications 52

Safety Notes 53

Sicherheitshinweise 55

Index 59

List of Tables

Table P-1	Supported Model Numbers	9
Table 1-1	MVME5500 Features Summary	13
Table 1-2	Default Processor Memory Map	16
Table 1-3	MOTLoad's Processor Memory Map	17
Table 1-4	Default PCI Memory Map	18
Table 1-5	MOTLoad's PCI 0 Domain Memory Map	19
Table 1-6	MOTLoad's PCI 1 Domain Memory Map	19
Table 1-7	PCI 0 Domain I/O Map	20
Table 1-8	PCI 1 Domain I/O Map	20
Table 1-9	Device Bank 1 I/O Memory Map	20
Table 1-10	System Status Register 1	21
Table 1-11	System Status Register 2	22
Table 1-12	System Status Register 3	24
Table 1-13	Presence Detect Register 3	24
Table 1-14	Configuration Header/Switch Register	25
Table 1-15	TBEN Register	26
Table 1-16	Geographical Address Register	27
Table 2-1	IDSEL Mapping for PCI Devices	30
Table 2-2	GT-64260B External GPP Interrupt Assignments	31
Table 2-3	I2C Bus Device Addressing	33
Table 2-4	GT-64260B GPP Pin Function Assignments	34
Table 2-5	GT-64260B Power-Up Configuration Settings	37
Table 2-6	Device Bank Assignments	39
Table 2-7	Device Bank Timing Parameters	39
Table 2-8	PCI Arbiter Assignments	41
Table 2-9	Processor L3CR Register Assignments	43
Table A-1	Flash 0 Memory Configuration Data	45
Table A-2	Flash 1 Memory Configuration Data	46
Table A-3	L3 Cache Configuration Data	47
Table B-1	Emerson Network Power - Embedded Computing Publications	49
Table B-2	Manufacturers' Documents	50
Table B-3	Specifications	52

List of Tables

List of Figures

Figure 1-1 MVME5500 Block Diagram 15
Figure 1-2 Configuration Header/Switch Register 26
Figure 1-3 Geographical Address Register 27

List of Figures

About this Manual

The MVME5500 Single Board Computer Programmer's Reference Guide provides general programming information, including memory maps, interrupts, and register data for the MVME5500 family of boards. This document should be used by anyone who wants general, as well as technical information about the MVME5500 products.

As of the printing date of this manual, the MVME5500 supports the models listed below.

Table P-1 Supported Model Numbers

Model Number	Description
MVME5500-0161	1 GHz MPC7455 processor, 512 MB SDRAM, Scanbe handles
MVME5500-0163	1 GHz MPC7455 processor, 512 MB SDRAM, IEEE handles

Overview of Contents

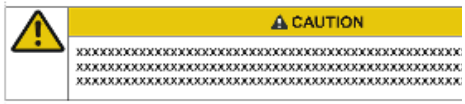
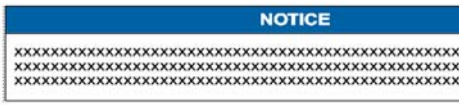
This manual is divided into the following chapters and appendices:

- Chapter 1, *Board Description and Memory Maps*, provides a brief product description and a block diagram. The remainder of the chapter provides information on memory maps and system and configuration registers.
- Chapter 2, *Programming Details*, provides additional programming information including IDSEL mapping, interrupt assignments for the GT-64260B system processor, two-wire serial interface addressing, and other device and system considerations.
- Appendix A, *Vital Product Data*, provides a listing of vital product data (VPD) related to this product.
- Appendix B, *Related Documentation*, provides a listing of related manuals, vendor documentation, and industry specifications.

Conventions

The following table describes the conventions used throughout this manual.

Notation	Description
0x00000000	Typical notation for hexadecimal numbers (digits are 0 through F), for example used for addresses and offsets
0b0000	Same for binary numbers (digits are 0 and 1)
bold	Used to emphasize a word
`Screen`	Used for on-screen output and code related elements or commands in body text
`Courier + Bold`	Used to characterize user input and to separate it from system output
Reference	Used for references and for table and figure descriptions
File > Exit	Notation for selecting a submenu
<text>	Notation for variables and keys
[text]	Notation for software buttons to click on the screen and parameter description
...	Repeated item for example node 1, node 2, ..., node 12
. . .	Omission of information from example/command that is not necessary at the time being
..	Ranges, for example: 0..4 means one of the integers 0,1,2,3, and 4 (used in registers)
|	Logical OR

Notation	Description
	Indicates a hazardous situation which, if not avoided, could result in death or serious injury
	Indicates a hazardous situation which, if not avoided, may result in minor or moderate injury
	Indicates a property damage message
	No danger encountered. Pay attention to important information

Summary of Changes

This manual has been revised and replaces all prior editions.

Part Number	Publication Date	Description
V5500A/PG2	October 2003	Motorola format; Corrected the PCI 0 and 1 domain memory space sizes in Table 1-3 on page 17.
6806800H16A	October 2009	Updated to Emerson format

Comments and Suggestions

We welcome and appreciate your comments on our documentation. We want to know what you think about our manuals and how we can make them better.

Mail comments to us by filling out the following online form:
http://www.emersonnetworkpowerembeddedcomputing.com/ > Contact Us > Online Form

In "Area of Interest" select "Technical Documentation". Be sure to include the title, part number, and revision of the manual and tell us how you used it.

Board Description and Memory Maps

1.1 Introduction

This chapter briefly describes the board level hardware features of the MVME5500 Single Board Computer, including a table of features and a block diagram. The remainder of the chapter provides memory map information including a default memory map, MOTLoad's processor memory map, a default PCI memory map, MOTLoad's PCI memory map, a PCI I/O memory map, and system I/O memory maps.

Programmable registers in the GT-64260B system controller are documented in publication MV-S100414-00 Rev A, which is obtainable from Marvell Technologies, Ltd. Refer to Appendix B, *Related Documentation* for more information.

1.2 Overview

The MVME5500 is a single-board computer based on the PowerPC MPC7455 processor and the Marvell GT-64260B host bridge with a dual PCI interface and memory controller. On-board payload includes two PMC slots, two SDRAM banks, an expansion connector for two additional banks of SDRAM, 8MB boot Flash ROM, one 10/100/1000 Ethernet port, one 10/100 Ethernet port, 32MB expansion Flash ROM, two serial ports, and an NVRAM and real-time clock.

The following table lists the features of the MVME5500.

Table 1-1 MVME5500 Features Summary

Feature	Description
Processor	• Single 1 GHz MPC7455 processor • Bus clock frequency at 133 MHz
L3 Cache	• 2 MB using DDR SRAM • Bus clock frequency at 200 MHz
Flash	• 8MB Flash soldered on board • 32MB expansion Flash soldered on board
System Memory	• Two banks on-board for 512 MB using 256 Mb devices • Expansion connector for a mezzanine board with two banks for 512 MB using 256 Mb devices • Double-bit-error detect, single-bit-error correct across 72 bits • Bus clock frequency at 133 MHz

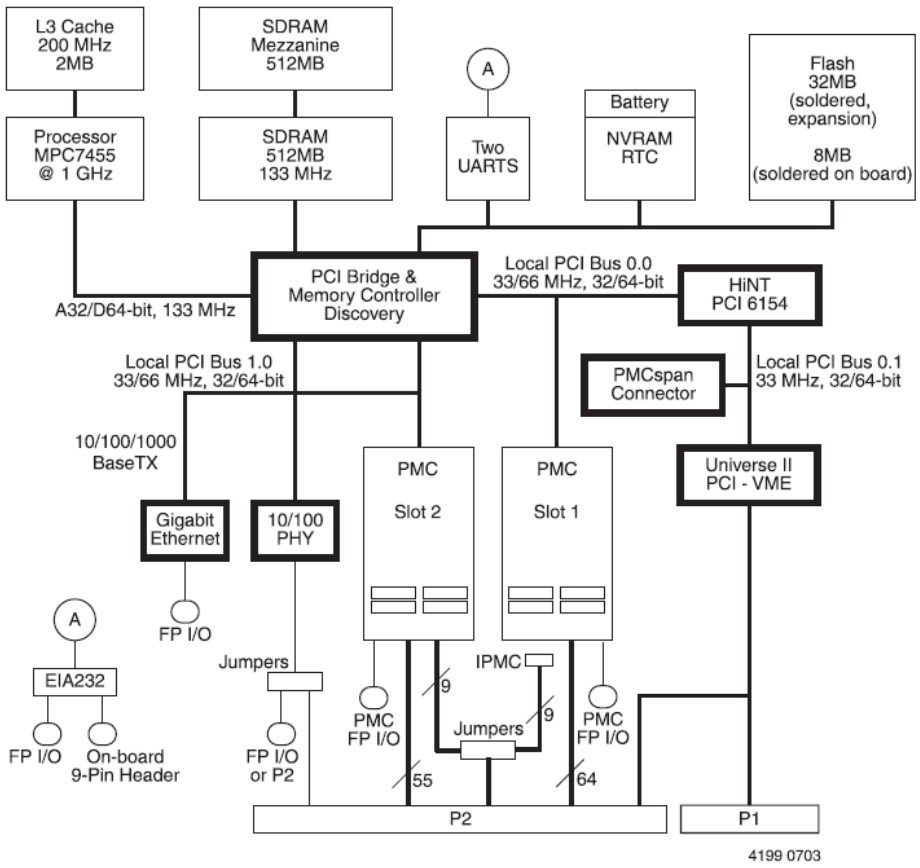
Table 1-1 MVME5500 Features Summary (continued)

Feature	Description
Memory Controller	● Provided by GT-64260B ● Supports one to four banks of SDRAM at up to 1 GB per bank
Processor Host Bridge	● Provided by GT-64260B ● Supports MPX mode or 60x mode
PCI Interfaces	● Provided by GT-64260B ● Two independent 64-bit interfaces, one compliant to PCI spec rev 2.1 (Bus 0.0) and the other compliant to PCI spec rev 2.2 (Bus 1.0) ● Bus clock frequency at 66 MHz
Interrupt Controller	● Provided by GT-64260B ● Interrupt sources internal to GT-64260B ● Up to 32 external interrupt inputs ● Up to seven interrupt outputs
Counters/Timers	Eight 32-bit counters/timers in GT-64260B
I2C	● Provided by GT-64260B ● Master or slave capable ● On-board serial EEPROMs for VPD, SPD, GT-64260B init, and user data storage
NVRAM	32 KB provided by MK48T37
Real Time Clock	Provided by MK48T37
Watchdog Timers	● One in GT-64260B ● One in MK48T37 ● Each watchdog timer can generate interrupt or reset, software selectable
On-board Peripheral Support	● One 10/100/1000BaseT Ethernet interface, one 10/100BaseT Ethernet interface ● Dual 16C550 compatible UARTs
PCI Mezzanine Cards	Two PMC sites (one shared with the expansion memory and has IPMC capability)
PCI Expansion	One expansion connector for interface to PMCspan
Miscellaneous	● Reset/Abort switch ● Front panel status indicators, Run and Board Fail

Table 1-1 MVME5500 Features Summary (continued)

Feature	Description
Form Factor	Standard VME

Figure 1-1 MVME5500 Block Diagram



1.3 Memory Maps

1.3.1 Default Processor Memory Map

When power is first applied or a hard reset has occurred, the GT-64260B has a default address map. Table 1-2 shows the default processor memory map.

Table 1-2 Default Processor Memory Map

Processor Address Start	Processor Address End	Size	Definition
0000 0000	007F FFFF	8 MB	SDRAM Bank 0
0080 0000	00FF FFFF	8 MB	SDRAM Bank 1
0100 0000	017F FFFF	8 MB	SDRAM Bank 2
0180 0000	01FF FFFF	8 MB	SDRAM Bank 3
0200 0000	0FFF FFFF	224 MB	Unassigned
1000 0000	11FF FFFF	32 MB	PCI Bus 0 I/O Space
1200 0000	13FF FFFF	32 MB	PCI Bus 0 Memory Space 0
1400 0000	1BFF FFFF	128 MB	Unassigned
1C00 0000	1C7F FFFF	8 MB	Device Port CS0
1C80 0000	1CFF FFFF	8 MB	Device Port CS1
1D00 0000	1DFF FFFF	16 MB	Device Port CS2
1E00 0000	1FFF FFFF	32 MB	Unassigned
2000 0000	21FF FFFF	32 MB	PCI Bus 1 I/O
2200 0000	23FF FFFF	32 MB	PCI Bus 1 Memory Space 0
2400 0000	25FF FFFF	32 MB	PCI Bus 1 Memory Space 1
2600 0000	27FF FFFF	32 MB	PCI Bus 1 Memory Space 2
2800 0000	29FF FFFF	32 MB	PCI Bus 1 Memory Space 3
2A00 0000	F0FF FFFF	3184 MB	Unassigned
F100 0000	F100 FFFF	64 KB	Internal Registers[1]
F101 0000	F1FF FFFF	16 MB - 64 KB	Unassigned

Table 1-2 Default Processor Memory Map (continued)

Processor Address Start	Processor Address End	Size	Definition
F200 0000	F3FF FFFF	32 MB	PCI Bus 0 Memory Space 1
F400 0000	F5FF FFFF	32 MB	PCI Bus 0 Memory Space 2
F600 0000	F7FF FFFF	32 MB	PCI Bus 0 Memory Space 3
F800 0000	FEFF FFFF	112 MB	Unassigned
FF00 0000	FF7F FFFF	8MB	Device Port CS3
FF80 0000	FFFF FFFF	8 MB	Boot Flash Bank[2]

1. Set by configuration resistors.

2. Selects Flash 0 or Flash 1 depending on the state of the Flash boot bank select jumper.

1.3.2 MOTLoad's Processor Memory Map

MOTLoad's processor memory map is given in the following table.

Table 1-3 MOTLoad's Processor Memory Map

Processor Address Start	Processor Address End	Size	Definition
0000 0000	7FFF FFFF	2 GB	On-Board SDRAM[1]
8000 0000	DFFF FFFF	1.5 GB	PCI 0 Domain Memory Space
E000 0000	EFFF FFFF	256 MB	PCI 1 Domain Memory Space
F000 0000	F07F FFFF	8 MB	PCI 0 Domain I/O Space[2]
F080 0000	F0FF FFFF	8 MB	PCI 1 Domain I/O Space[2]
F100 0000	F10F FFFF	1 MB	GT-64260B Internal Registers
F110 0000	F11F FFFF	1 MB	GT-64260B Device Bus Registers[3]
F120 0000	F1FF FFFF	14 MB	Reserved
F200 0000	FE00 0000	32 MB	Flash Bank 0[4]
FF80 0000	FFFF FFFF	8 MB	Flash Bank 1[4]

1. Maximum size is 2 GB. Actual size depends on the amount of memory installed.

2. Zero-based I/O space.

3. Device chip select 1.

4. Flash 0/Flash 1 can be mapped to device chip select 0 or BOOT chip select depending on the state of the Flash boot bank select header.

1.3.3 Default PCI Memory Map

Table 1-4 is the default PCI memory map for each PCI bus following reset.

Table 1-4 Default PCI Memory Map

PCI Address Start	PCI Address End	Size	Definition
0000 0000	007F FFFF	8 MB	SDRAM Bank 0
0080 0000	00FF FFFF	8 MB	SDRAM Bank 1
0100 0000	017F FFFF	8 MB	SDRAM Bank 2
0180 0000	01FF FFFF	8 MB	SDRAM Bank 3
0200 0000	0FFF FFFF	224 MB	Unassigned
1000 0000	11FF FFFF	32 MB	PCI Bus 1 P2P I/O Space
1200 0000	13FF FFFF	32 MB	PCI Bus 1 P2P Memory Space 0
1400 0000	1400 FFFF	64 KB	Internal Registers
1401 0000	1BFF FFFF	128 MB - 64 KB	Unassigned
1C00 0000	1C7F FFFF	8 MB	Device Port CS0
1C80 0000	1CFF FFFF	8 MB	Device Port CS1
1D00 0000	1DFF FFFF	16 MB	Device Port CS2
1E00 0000	1FFF FFFF	32 MB	Unassigned
2000 0000	21FF FFFF	32 MB	PCI Bus 0 P2P I/O Space
2200 0000	23FF FFFF	32 MB	PCI Bus 0 P2P Memory Space 0
2400 0000	25FF FFFF	32 MB	PCI Bus 0 P2P Memory Space 1
2600 0000	F1FF FFFF	32 MB	Unassigned

Table 1-4 Default PCI Memory Map (continued)

PCI Address Start	PCI Address End	Size	Definition
F200 0000	F3FF FFFF	3264 MB	PCI Bus 1 P2P Memory Space 1
F400 0000	FEFF FFFF	32 MB	Unassigned
FF00 0000	FF7F FFFF	176 MB	Device Port CS3
FF80 0000	FFFF FFFF	8 MB	Boot Flash Bank

1.3.4 MOTLoad's PCI Memory Maps

MOTLoad's PCI memory map for each PCI domain is shown in the following tables.

Table 1-5 MOTLoad's PCI 0 Domain Memory Map

PCI 0 Memory Address Start	PCI 0 Memory Address End	Size	Definition
0000 0000	7FFF FFFF	2 GB	Onboard SDRAM
8000 0000	DFFF FFFF	768 MB	Local PCI 0 Domain Memory Space
F000 0000	FFFF FFFF	256 MB	Reserved

Table 1-6 MOTLoad's PCI 1 Domain Memory Map

PCI 1 Memory Address Start	PCI 1 Memory Address End	Size	Definition
0000 0000	7FFF FFFF	2 GB	Onboard SDRAM
E000 0000	EFFF FFFF	1 GB	Local PCI 1 Domain Memory Space
F000 0000	FFFF FFFF	256 MB	Reserved

1.3.5 PCI I/O Space Maps

The PCI I/O space map for each PCI domain is shown in the following tables.

Table 1-7 PCI 0 Domain I/O Map

PCI 0 I/O Address Start	PCI 0 I/O Address End	Size	Definition
0000 0000	007F FFFF	8 MB	Local PCI Domain I/O Space

Table 1-8 PCI 1 Domain I/O Map

PCI 0 I/O Address Start	PCI 0 I/O Address End	Size	Definition
0000 0000	007F FFFF	8 MB	Local PCI Domain I/O Space

1.3.6 System I/O Memory Map

System resources for the MVME5500 board including system control and status registers, NVRAM/RTC, and the 16550 UARTs are mapped into a 1 MB address range assigned to device bank 1. The region defined by device bank 1 resides within the GT-64260B device bus register's space listed in Table 1-3 on page 17. The memory map is defined in the following table:

Table 1-9 Device Bank 1 I/O Memory Map

Device Bank1 Address Offset	Definition
0 0000	System Status Register 1
0 0001	System Status Register 2
0 0002	System Status Register 3
0 0003	Reserved
0 0004	Presence Detect Register
0 0005	Software Readable Header/Switch
0 0006	Timebase Enable Register
0 0007	Geographical Address Register (VME board)
0 0008 - 0 FFFF	Reserved for future on-board registers
1 0000 - 1 7FFF	M48T37V NVRAM/RTC

Table 1-9 Device Bank 1 I/O Memory Map (continued)

Device Bank1 Address Offset	Definition
2 0000 - 2 0FFF	COM1 16550 UART
2 1000 - 2 1FFF	COM2 16550 UART
2 4000 - F FFFF	Reserved (undefined)

1.3.7 System Status Register 1

The MVME5500 board system status register 1 is used to provide board status information and software control of Abort.

Table 1-10 System Status Register 1

REG	System Status Register 1 - Offset 0x0 0000							
BIT	7	6	5	4	3	2	1	0
FIELD	REF_CLK	BANK_SEL	SAFE_START	ABORT_	FLASH_BSY_	FUSE_STAT	RSVD	RSVD
OPER	R	R	R	R/W	R	R	R	R
RESET	X	X	X	1	X	X	0	0

REF_CLK

Reference clock. This bit reflects the current state of the 28.8 KHz reference clock derived from the 1.8432 MHz UART oscillator divided by 64. This clock may be used as a fixed timing reference.

BANK_SEL

Boot Flash bank select. This bit reflects the current state of the boot Flash bank select jumper. A cleared condition indicates that Flash 0 is the boot bank. A set condition indicates that Flash 1 is the boot bank.

SAFE_START

ENV safe start. This bit reflects the current state of the ENV safe start select jumper. A cleared condition indicates that the ENV settingsprogrammed in NVRAM, VPD, and SPD should be used by thefirmware. A set condition indicates that firmware should use the safe ENV settings.

ABORT_

This bit reflects the current state of the on-board abort signal. Writing a 0 at this bit position asserts the abort interrupt output signal, while writing a 1 at this bit position clears the abort interrupt output signal. Reading a 1 at this bit position indicates that the abort switch is deasserted, while reading a 0 at this bit position indicates that the abort switch is asserted.

FLASH_BSY_

Flash busy. This bit provides the current state of the Flash 0 StrataFlash device status pins. These two open drain output pins are wire ORed. Refer to the appropriate Intel StrataFlash Data Sheet for a description on the function of the status pin.

FUSE_STAT

Fuse status. This bit indicates the status of the soldered, onboard fuses (R199 and R188). A cleared condition indicates that one of the fuses is open. A set condition indicates that all fuses are functional.

1.3.8 System Status Register 2

The MVME5500 board system status register 2 provides board control and status bits.

Table 1-11 System Status Register 2

REG	System Status Register 2 - Offset 0x0 0001							
BIT	7	6	5	4	3	2	1	0
FIELD	BD_FAIL	EEPROM_WP	FLASH_WP	TSTAT_ MASK	RSVD	PCI 0.1_M66EN	PCI 1.0_M66EN	PCI 0.0_M66EN
OPER	R/W	R/W	R/W	R/W	R	R	R	R
RESET	1	1	1	1	0	0	X	X

BD_FAIL

Board fail. This bit is used to control the board fail LED. A set condition illuminates the front panel LED and a cleared condition extinguishes the front-panel LED.

EEPROM_WP

EEPROM write protect. This bit is to provide protection against inadvertent writes to the on-board EEPROM devices. Clearing the bit enables writes to the EEPROM devices. Setting this bit write protects the devices. The devices are write protected following a reset.

FLASH_WP

Flash write protect. This bit is used to provide protection against inadvertent writes to both Flash 0 and Flash 1 memory devices. Clearing this bit enables writes to the Flash devices. Setting this bit write protects the devices. This bit is set during reset and must be cleared by the system software to enable writing of the Flash devices.

TSTAT_MASK

Thermostat mask. This bit is used to mask the DS1621 temperature sensor thermostat output. If this bit is cleared, the thermostat output is enabled to generate an interrupt on GPP 3. If the bit is set, the thermostat output is disabled from generating an interrupt.

PCI0.1_M66EN

PCI Bus 0.1 M66EN. This bit reflects the state of the PCI Bus 0.1 M66EN pin. A cleared condition indicates that PCI Bus 0.0 is operating at 33 MHz. A set condition indicates that the bus is operating at 66 MHz. This bit is always cleared on the MVME5500.

PCI1.0_M66EN

PCI Bus 1.0 M66EN. This bit reflects the state of the PCI Bus 1.0 M66EN pin. A cleared condition indicates that PCI Bus 1.0 is operating at 33 MHz. A set condition indicates that the bus is operating at 66 MHz.

PCI0.0_M66EN

PCI Bus 0.0 M66EN. This bit reflects the state of the PCI Bus 0.0 M66EN pin. A cleared condition indicates that PCI Bus 0 is operating at 33 MHz. A set condition indicates that the bus is operating at 66 MHz.

1.3.9 System Status Register 3

The MVME5500 board system status register 3 provides the board software-controlled reset functions.

Table 1-12 System Status Register 3

REG	System Status Register 3 - Offset 0x0 0002							
BIT	7	6	5	4	3	2	1	0
FIELD	BRD_RST	RSVD	RSVD	RSVD	ABT_INT_MASK	RSVD	RSVD	RSVD
OPER	W	R	R	R	R/W	R	R	R
RESET	0	0	0	0	1	0	0	0

BRD_RST

Board reset. Setting this bit forces a hard reset of the MVME5500 board. This bit clears automatically when the board reset is complete.

ABT_INT_MASK

Abort interrupt mask. This bit is used to mask the abort interrupt. If this bit is set, the abort interrupt is masked so the abort interrupt is not generated. If the bit is cleared, the abort interrupt may be generated.

1.3.10 Presence Detect Register

The MVME5500 board contains a presence detect register that may be read by the system software to determine the presence of optional devices.

Table 1-13 Presence Detect Register 3

REG	Presence Detect Register 2 - Offset 0x0 0004h							
BIT	7	6	5	4	3	2	1	0
FIELD	RSVD	RSVD	RSVD	RSVD	RSVD	PMC_SPANP	PMC2P_	PMC1P_
OPER	R	R	R	R	R	R	R	R

Table 1-13 Presence Detect Register 3 (continued)

REG	Presence Detect Register 2 - Offset 0x0 0004h							
RESET	1	1	1	1	1	X	X	X

PMC_SPANP_

PMC expansion module present. If set, there is no PMC expansion module installed. If cleared, the PMC expansion module is installed.

PMC2P_

PMC module 2 present. If set, there is no PMC module installed in position 2. If cleared, the PMC module is installed.

PMC1P_

PMC module 1 present. If set, there is no PMC module installed in position 1. If cleared, the PMC module is installed.

1.3.11 Configuration Header/Switch Register (S1)

The MVME5500 board has an 8-bit header or switch that may be read by the software.

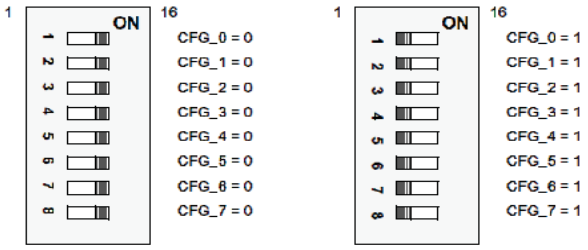
Table 1-14 Configuration Header/Switch Register

REG	Configuration Header/Switch Register - Offset 0x0 0005h							
BIT	7	6	5	4	3	2	1	0
FIELD	CFG_7	CFG_6	CFG_5	CFG_4	CFG_3	CFG_2	CFG_1	CFG_0
OPER	R	R	R	R	R	R	R	R
RESET	X	X	X	X	X	X	X	X

CFG[7-0]

Configuration bits 7-0. These bits reflect the position of the switch installed in the software readable header location. A cleared condition indicates that the switch is ON for the header position associated with that bit and a set condition indicates that the switch is OFF.

Figure 1-2 Configuration Header/Switch Register



1.3.12 Time Base Enable Register

The time base enable (TBEN) register provides the means to control the processor's TBEN input.

Table 1-15 TBEN Register

REG	TBEN Register- Offset 0x0 0006							
BIT	7	6	5	4	3	2	1	0
FIELD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	TBEN0
OPER	R	R	R	R	R	R	R	R/W
RESET	0	0	0	0	0	0	0	1

TBEN0

Processor time base enable. When this bit is cleared, the TBEN pin of the processor is driven low. When this bit is set, the TBEN pin is driven high.

1.3.13 Geographical Address Register (S2)

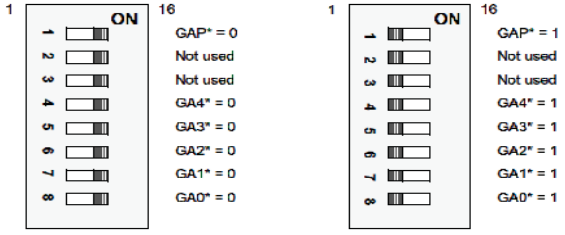
This register reflects the inverted states of the geographical address pins at the 5-row, 160-pin P1 connector. Applications not using the 5-row backplane can use a planar switch (same type as the *Configuration Header/Switch Register (S1)* on page 25) to assign a geographical address according to the following diagram.

The switch positions must all be turned off when the MVME5500 is used in a 5-row backplane.

Table 1-16 Geographical Address Register

REG	Geographical Address Register - 0xFF100007							
BIT	7	6	5	4	3	2	1	0
FIELD	VMEGA0_	VMEGA1_	VMEGA2_	VMEGA3_	VMEGA4_	RSVD	RSVD	VMEGAP_
OPER	R	R	R	R	R	R	R	R
RESET	X	X	X	X	X	X	X	X

Figure 1-3 Geographical Address Register



1.3.14 COM1 & COM2 Universal Asynchronous Receiver/Transmitter (UART)

COM1 and COM2 are PC16550 Universal Asynchronous Receiver/Transmitter (UART) to provide an asynchronous serial interface for test/debug purposes. To facilitate proper baud rate generation, the frequency of the input clock for the PC16550 UART is fixed at 1.8432 MHz. For additional programming details, refer to the *PC16550 Data Sheet*.

1.3.15 Real-Time Clock and NVRAM

The SGS-Thomson M48T37 is used by the MVME5500 board to provide 32 KB of non-volatile static RAM, real-time clock, and watchdog timer functions. The device is accessed as linear memory. Refer to the *MK48T37 Data Sheet* for programming information.

1.4 ISA Local Resource Bus

The ISA local resources exist only if an IPMC712/761 module is mounted on the MVME5500. Refer to the *IPMC712/761 I/O Module Installation and Use*, listed in Appendix B, *Related Documentation*.

Chapter 2

Programming Details

2.1 Introduction

This chapter includes additional programming information for the MVME5500 Single Board Computer. Items discussed include:

- *PCI Configuration Space and IDSEL Mapping* on page 30
- *Interrupt Controller* on page 31
- *Two-Wire Serial Interface* on page 33
- *GT-64260B Initialization* on page 34
- *GT-64260B GPP Configuration* on page 34
- *GT-64260B Reset Configuration* on page 36
- *GT-64260B Device Controller Bank Assignments* on page 39
- *System Clock Generators* on page 40
- *VPD and User Configuration EEPROMs* on page 40
- *Temperature Sensor* on page 41
- *Flash Memory* on page 41
- *PCI Arbitration Assignments* on page 41
- *Other Software Considerations* on page 42

2.2 PCI Configuration Space and IDSEL Mapping

Each PCI device has an associated address line connected via a resistor to its IDSEL pin for configuration space accesses. Table 2-1 shows the IDSEL assignments for the PCI devices on each of the PCI buses on the MVME5500 board along with the corresponding interrupt assignment to the general-purpose port (GPP) pins. Refer to the *GT-64260B System Controller for PowerPC Processors Data Sheet* and the *PCI 6154 (HB2) PCI-to-PCI Bridge Data Book*, both listed in Appendix B, *Related Documentation*, for details on generating configuration cycles on each of the PCI buses

Table 2-1 IDSEL Mapping for PCI Devices

PCI Bus	Device Number Field	PCI AD Line	Physical PCI Device	Device INT# to GPP Interrupt Input			
				INTA#	INTB#	INTC#	INTD#
0.0	0b0_0001	AD11	IPMC	11			
	0b0_0110	AD16	PMC 1(J11,12,13,14)	8	9	10	11
	0b0_0111	AD17	PMC 1 IDSEL B				
	0b0_1010	AD20	HiNT PCI 6154 Bridge				
	0b1_0101	AD31	GT-64260B PCI Bridge				
0.1	0b0_0000	AD16	CA91C142D VME VLINT0	12			
			CA91C142D VME VLINT1	13			
			CA91C142D VME VLINT2	14			
			CA91C142D VME VLINT3	15			
	0b0_0100	AD20	PMC Expansion[1]	12	13	14	15
1.0	0b0_0110	AD16	PMC 2 (J21,22,23,24)	16	17	18	19
	0b0_0111	AD17	PMC 2 IDSEL B				
	0b0_1010	AD20	82C544 Ethernet 1	20			
	0b1_0101	AD31	GT-64260B PCI Bridge				

1. Device-specific interrupt routing is established on the PMCspan board. Refer to the PMCspan PMC Adapter Carrier Board Installationand Use manual, listed in Appendix B, Related Documentation.

2.3 Interrupt Controller

The MVME5500 uses the GT-64260B interrupt controller to handle interrupts internal to the GT-64260B, as well as the external interrupt sources. The GT-64260B has a limited number of directly triggerable interrupt inputs. Each of the GPP pins can be configured for an interrupt input, but the inputs are combined internally in groups of eight inputs (one for each byte lane) for one interrupt source. Therefore, interrupt inputs in each byte lane are essentially shared. Currently defined external interrupting devices and GPP interrupt assignments are shown in Table 2-2.

The GT-64260B has one dedicated processor interrupt output, CPUINT_, which is connected to the primary processor CPU0 INT_L input. Refer to the *GT-64260B System Controller for PowerPC Processors Data Sheet*, listed in Appendix B, *Related Documentation*, for details.

Table 2-2 GT-64260B External GPP Interrupt Assignments

GPP Group	GPP #	Edge/ Level	Polarity	Interrupt Source
0	0	Level	High	COM1 || COM2
	1	Level	Low	Not Used. Pulled High.
	2	Level	Low	Abort Switch
	3	Level	Low	RTC || Thermostat Output
	4	Level	Low	Not Used. Pulled high, tied to GPP27.
	5	Level	Low	Not Used. Pulled high, tied to GPP28.
	6	Level	Low	GT-64260B WDMNI Interrupt. Tied to GPP24.
	7	Level	Low	LXT971A Interrupt (10/100 Mb PHY)

Table 2-2 GT-64260B External GPP Interrupt Assignments (continued)

GPP Group	GPP #	Edge/ Level	Polarity	Interrupt Source
1	8	Level	Low	PMC 1 Interrupt INT A
	9	Level	Low	PMC 1 Interrupt INT B
	10	Level	Low	PMC 1 Interrupt INT C
	11	Level	Low	PMC 1 Interrupt INT D || IPMC INT
	12	Level	Low	VME Interrupt VLINT0
	13	Level	Low	VME Interrupt VLINT1
	14	Level	Low	VME Interrupt VLINT2
	15	Level	Low	VME Interrupt VLINT3
	16	Level	Low	PMC 2 Interrupt INT A
	17	Level	Low	PMC 2 Interrupt INT B
	18	Level	Low	PMC 2 Interrupt INT C
	19	Level	Low	PMC 2 Interrupt INT D
	20	Level	Low	82544 Interrupt
	21	Level	Low	Not Used. Pulled High.
	22	Level	Low	Not Used. Pulled High.
	23	Level	Low	Not Used. Pulled High.
	24			Watchdog Timer NMI Output WDNMI# to GPP6
	25			Watchdog Timer Expired Output WDE#
	26			GT-64260B SROM Initialization Active InitAct
	27	Level	Low	Not Used. Pulled High.
	28			Not Used. Pulled High.
	29			Optional External PPC Bus Arbiter BG1 Enable
	30			Unused. Pulled High.
	31			Unused. Pulled High.

2.4 Two-Wire Serial Interface

A two-wire serial interface for the MVME5500 board is provided by an I^2C compatible serial controller integrated into the GT-64260B system controller. The I^2C serial controller provides two basic functions. The first function is to provide GT-64260B register initialization following a reset. The GT-64260B can be configured (by jumper setting) to automatically read data out of a serial EEPROM following a reset and initialize any number of internal registers. In the second function, the controller is used by the system software to read the contents of the VPD EEPROM contained on the MVME5500 board, along with the SPD EEPROMs, to further initialize the memory controller and other interfaces. For additional details regarding the GT-64260B two-wire serial controller operation, refer to the *GT-64260B System Controller for PowerPC Processors Data Sheet*, listed in Appendix B, *Related Documentation*.

Table 2-3 shows the I^2C devices used for the MVME5500 and the assigned device IDs.

Table 2-3 I^2C Bus Device Addressing

Device Function	Size	Device Address (A2A1A0)	I^2C BUS Address	Notes
Memory SPD (Onboard. Banks A and B.)	256 x 8	000b	$A0	1, 2
Memory SPD (On mezzanine. Banks C and D.)	256 x 8	001b	$A2	1
IPMC VPD	256 x 8	010b	$A4	
GT-64260B Fixed Initialization	256 x 8	011b	$A6	2
Configuration VPD	8K x 8	100b	$A8	2, 3
User VPD	8K x 8	101b	$AA	2, 3
Not Used	NA	110b	$AC	
Not Used	NA	111b	$AE	
DS1621 Temperature Sensor	NA	000B	$90	

Notes:

1. Each SPD defines the physical attributes of each bank or group of banks, that is, if both banks of a group are populated, they will be the same speed and memory size.
2. This device can be write-protected by either setting the EEPROM_WP bit of SSR2 or by placing a jumper on the EEPROM write protect header. The hardware jumper mechanism always takes precedence over the software setting. For 8 KB sized parts, only the upper 2 KB are writeprotectable.
3. This is a 2-byte address serial EEPROM (AT24C64).

2.5 GT-64260B Initialization

Serial EEPROM devices are provided to support optional initialization of the GT-64260B (enabled by an on-board jumper). Using the SROM initialization method, any of the GT-64260B internal registers or other system components (that is, devices on the PCI bus) can be initialized. Initialization takes place by sequentially reading 8-byte address/data pairs from the SROM and writing the 32-bit data to the decoded 32-bit address until the data pattern matching the last serial data item register is read for the SROM (default value = 0xffffffff). The onboard reset logic keeps the processor reset asserted until this initialization process is completed.

2.6 GT-64260B GPP Configuration

The GT-64260B contains a 32-bit GPP. The GPP pins can be configured as general-purpose I/O pins, as external interrupt inputs, or as specific control/status pins for one of the GT-64260B internal devices. After reset, all GPP pins default to general-purpose inputs. Software must then configure each of the pins for the desired function. The following table defines the function assigned to each GPP pin on the MVME5500 board.

Table 2-4 GT-64260B GPP Pin Function Assignments

GPP Number	Input/Output	Function
0	I	COM1/COM2 interrupts (ORed)
1	I	Not Used. Pulled High.
2	I	Abort Interrupt

Table 2-4 GT-64260B GPP Pin Function Assignments (continued)

GPP Number	Input/Output	Function
3	I	RTC and Thermostat Interrupts (ORed)
4	O	Not Used. Pulled high, tied to GPP27.
5	I	Not Used. Pulled high, tied to GPP28.
6	I	GT-64260B WDMNI Interrupt. Tied to GPP24.
7	I	LXT971A Interrupt (10/100Mbit PHY)
8	I	PMC 1 Interrupt INT A
9	I	PMC 1 Interrupt INT B
10	I	PMC 1 Interrupt INT B
11	I	PMC 1 Interrupt INT D/IPMC INT
12	I	VME Interrupt 0
13	I	VME Interrupt 1
14	I	VME Interrupt 2
15	I	VME Interrupt 3
16	I	PMC 2 Interrupt INT A
17	I	PMC 2 Interrupt INT B
18	I	PMC 2 Interrupt INT C
19	I	PMC 2 Interrupt INT D
20	I	82544 Interrupt
21	I	Not Used. Pulled High.
22	I	Not Used. Pulled High.
23	I	Not Used. Pulled High.
24	O	Watchdog Timer NMI Output WDNMI# to GPP6
25	O	Watchdog Timer Expired Output WDE#
26	O	GT-64260B SROM Initialization Active InitAct
27	I	Not Used. Pulled high, tied to GPP4.
28	O	Not Used. Pulled high, tied to GPP5.
29	O	Optional external PPC Bus Arbiter BG1 Enable.

Table 2-4 GT-64260B GPP Pin Function Assignments (continued)

GPP Number	Input/Output	Function
30	I	Not Used. Pulled High.
31	I	Not Used. Pulled High.

2.7 GT-64260B Reset Configuration

The GT-64260B supports two methods of device initialization following reset:

- Pins sampled on the deassertion of reset
- Partial pin sample on deassertion of reset plus serial ROM initialization via the I^2C bus

The MVME5500 board supports both options listed above. An onboard jumper setting is used to select the option. If the pin-sample-only method is selected, then states of the various pins on the device AD bus are sampled when reset is deasserted to determine the desired operating modes. Table 2-5 on page 37 describes the configuration options. Combinations of pullups, pulldowns, and jumpers are used to set the options. Some options are fixed and some are selectable at build time by installing the proper pullup/pulldown resistor. Finally, some options may be selected using onboard jumpers.

Using the SROM initialization method, any of the GT-64260B internal registers or other system components (that is, devices on the PCI bus) can be initialized. Initialization takes place by sequentially reading 8-byte address/data pairs from the SROM and writing the 32-bit data to the decoded 32-bit address until the last serial data item of 0xffffffff is read. If the SROM initialization option is selected, the following pins are still sampled to determine certain operating parameters:

- AD(1) – SROM byte offset width
- AD(3:2) – SROM address
- AD(4) – CPU endianess

- AD(30:28) – PLL settings
- AD(31) – CPU interface voltage

Table 2-5 GT-64260B Power-Up Configuration Settings

Device AD Bus Signal	Select Options	Default Power-Up Settings	Description	State of Bit vs. Function	
AD[0]	Jumper	x	SROM Initialization	0	No SROM Initialization
				1	SROM Initialization Enabled
AD[1]	Resistor	0	SROM Byte Offset Width	0	Up to 8 Bits
AD[3:2]	Resistors	11	SROM Device Address	11	1010011 ($A6)
AD[4]	Fixed	0	CPU Data Endianess	0	Must be Pulled Down
AD[5]	Fixed	1	CPU Interface Clock	1	CPU Interface Synchronous with TClk
AD[6]	Jumper	x	CPU Bus Configuration	0	60x Bus Mode
				1	MPX Bus Mode
AD[8]	Resistor	1	Internal 60x Bus Arbiter	1	Internal Arbiter Enabled
AD[9]	Fixed	0	Multiple GT-64260B Support	0	Not Supported
AD[11:10]	Fixed	11	Multiple GT-64260B Address ID	11	GT Responds to CPU Address A[5:6] = 11
AD[12]	Fixed	0	SDRAM UMA	0	Not Supported
AD[13]	Fixed	0	UMA Device Type	0	UMA Master
AD[15:14]	Fixed	10	BootCS* Device Width	10	32 Bits
AD[16]	Resistor	1	PCI Retry	1	Enable
AD[17]	Fixed	0	PCI_0 Expansion ROM	0	Not Supported
AD[18]	Fixed	0	PCI_1 Expansion ROM	0	Not Supported
AD[22:19]	Fixed	0000	Reserved	000	Must be Pulled Down
AD[23]	Fixed	1	SDClkIn/SDClkOut Select	1	SDClkIn
AD[24]	Resistor	1	Internal Space Default Address	1	0xf100.0000
AD[27:25]	Fixed	000	Reserved	000	Must be Pulled Down
AD[28]	Resistor	0	PLL Tune	0	Tuning Option 0

Table 2-5 GT-64260B Power-Up Configuration Settings (continued)

Device AD Bus Signal	Select Options	Default Power-Up Settings	Description	State of Bit vs. Function	
AD[29]	Resistor	0	PLL Divider	0	Divider Option 0
AD[30]	Resistor	0	PLL Bypass	0	PLL Enabled
AD[31]	Fixed	0	CPU Interface Voltage	0	2.5V

2.8 GT-64260B Device Controller Bank Assignments

The MVME5500 board uses three of the GT-64260B device controller banks for interfacing to various devices. The following tables define the device bank assignments and the programmable device bank timing parameters required for each of the banks used. Note that all device bank timing parameters, except BAdrSkew, have an extension bit that forms the most significant bit of the timing parameter.

Table 2-6 Device Bank Assignments

Device Bank	Data Width	Function
0	32 bit	Flash 0 Soldered Flash or Flash 1 Soldered Flash[1]
1	8 bit	I/O Devices
2	NA	Not used
3	NA	Not used
Boot	32 bit	Flash 1 Soldered Flash or Flash 0 Soldered Flash[1]

1. Determined by Flash boot bank select jumper.

Table 2-7 Device Bank Timing Parameters

Device Bank	GT-64260B Tclk Clock Freq.	Acc2FirstExt - Acc2First	Acc2NextExt - Acc2Next	TurnOffExt - TurnOff	ALE2WrExt - ALE2Wr	WrLowExt - WrLow	WrHighExt - WrHigh	BAdrSkew
Flash 0 (150 ns)	100 MHz	1-1	0-3	0-6	0-3	0-7	0-4	0
	133 MHz	1-6	0-4	0-8	0-3	1-2	0-5	0
Flash 0 (120 ns)	100 MHz	0-e	0-3	0-6	0-3	0-7	0-4	0
	133 MHz	1-2	0-4	0-8	0-3	1-2	0-5	0
Flash 0 (100 ns)	100 MH	0-c	0-3	0-6	0-3	0-7	0-4	0
	133 MH	1-0	0-4	0-8	0-3	1-2	0-5	0
Device Bank1 I/O	100 MHz	0-c	0-a	0-5	0-3	1-0	0-4	0
	133 MHz	1-0	0-e	0-7	0-3	1-3	0-6	0

Table 2-7 Device Bank Timing Parameters (continued)

Device Bank	GT-64260B Tclk Clock Freq.	Acc2FirstExt - Acc2First	Acc2NextExt - Acc2Next	TurnOffExt - TurnOff	ALE2WrExt - ALE2Wr	WrLowExt - WrLow	WrHighExt - WrHigh	BAdrSkew
Flash 1 (90 ns)	100 MHz	0-b	0-b	0-3	0-3	0-4	0-3	0
	133 MHz	0-e	0-e	0-4	0-3	0-5	0-4	0

Flash 0 contains 100 ns, 120 ns, or 150 ns StrataFlash devices. Device speed can be determined from VPD.

2.9 System Clock Generators

The system clock generator functions generate and distribute all of the clocks required for system operation. The clocks for the processor, memory, and PCI devices consist of a clock tree derived from a 66 MHz oscillator and a series of PLL clock generators. The clock tree is designed in such a manner as to maintain the strict edge-to-edge jitter and low clock-to-clock skew required by these devices. Additional clocks required by individual devices are generated near the devices using individual oscillators.

2.10 VPD and User Configuration EEPROMs

The MVME5500 board contains an Atmel AT24C64 vital product data (VPD) EEPROM containing configuration information specific to the board. Typical information that may be present in the VPD is: manufacturer, board revision, build version, date of assembly, memory present, options present, L3 cache information, etc. A second AT24C64 device is available for user data storage.

2.11 Temperature Sensor

The MVME5500 board contains a Maxim DS1621 digital temperature sensor with an I^2C serial bus interface. This device may be used to provide a measure of the ambient temperature of the board.

2.12 Flash Memory

The MVME5500 contains two banks of Flash memory accessed via the device controller contained within the GT-64260B. Flash 1 consists of two soldered 32 Mb devices (E28F320J3A) to give a minimum of 8 MB Flash memory. Flash 0 consists of two Intel StrataFlash 3.3 V devices, configured to operate in 16-bit mode, to form a 32-bit Flash port. This bank contains 64 Mb devices (E28F128J3A) for 32 MB of Flash.

There is a Flash boot bank select jumper on board, which selects either Flash 0 or Flash 1 as the boot bank. No jumper or a jumper installed between pins 1 and 2 selects Flash 0 as the boot bank. A jumper installed between pins 2 and 3 selects Flash 1 as the boot bank.

2.13 PCI Arbitration Assignments

PCI arbitration for PCI Bus 0.0 and PCI Bus 1.0 is handled using logic implemented in PLDs. These arbiters use a rotating priority scheme for fairness and bus parking will always be on the GT-64260B. There are no software programmable modes to these arbiters.

PCI arbitration for PCI Bus 0.1 is provided by the HiNT PCI 6154 secondary side arbiter.

Table 2-8 PCI Arbiter Assignments

PCI Bus Number	REQ/GNT Pair	PCI Device
0.0	0	GT-64260B Host
	1	PMC Req 1
	2	PMC Req 2
	3	PCI-to-PCI Bridge (HiNT PCI 6154)
	4	Not Used

Table 2-8 PCI Arbiter Assignments (continued)

PCI Bus Number	REQ/GNT Pair	PCI Device
0.1	0	PCI/PMC Expansion
	1	VME Controller
1.0	0	GT-64260B Host
	1	PMC Req 1
	2	PMC Req 2
	3	82544
	4	Not Used

2.14 Other Software Considerations

The following subsections discuss software aspects of the CPU bus, processor, and cache that can have an influence on the MVME5500.

2.14.1 CPU Bus Mode

The CPU bus operating mode (60x or MPX) is determined by reading the BMODE bits (bits 16-17) in the processor's Memory Subsystem Control Register (MSSCR0). The power-up state of the BMODE(0:1) pins is captured in these register bits. Refer to the *MPC7450 RISC Microprocessor User's Manual*, listed in Appendix B, *Related Documentation*, for details.

2.14.2 Processor Type Identification

Software can determine the processor version through the version register. The most significant 16 bits (0:15) of the MPC7455 processor version register reads as 0x8001.

2.14.3 Processor PLL Configuration

The processor internal clock frequency (core frequency) is a multiple of the system bus frequency. The processor has five configuration pins, PLL_EXT and PLL_CFG[0:3], for hardware strapping of the processor core frequency (between 2x and 16x of the system bus frequency).

2.14.4 L1, L2, L3 Cache

The processors support on-chip L1 and L2 caches and external L3 cache. L3 cache supports 1 or 2 MB in a variety of SRAM device types. Each processor L3 interface on the MVME5500 consists of two 8 Mb devices (K7D803671B-HC30) providing a total of 2 MB of L3 cache. Data parity checking should be enabled. The following processor L3CR register settings assume a processor speed of 933 MHz and L3 clock speed of 233 MHz.

Table 2-9 Processor L3CR Register Assignments

Apollo L3CR Register	Description	Value
L3SIZ	L3 Size, 2 MB	1
L3RT	L3 SRAM Type, DDR SRAM	00
L3PE	L3 Data Parity Checking Enable, ON	1
L3CLK	L3 Clock Speed; 233 MHz, Divide by 4	110
L3CKSP	L3 Clock Sample Point, 2 Clocks	TBD
L3PSP	L3 P-Clock Sample Point, 3 Clocks	TBD

A.1 Flash Memory Configuration Data

The Flash memory configuration data packet consists of byte fields that indicate the size/organization/type of the Flash memory array. Table A-1 and Table A-2 further describe the Flash memory configuration VPD data packet.

Table A-1 Flash 0 Memory Configuration Data

Byte Offset	Field Size (Bytes)	Field Mnemonic	Field Description
00	2	FMC_MID	Manufacturer's Identifier
02	2	FMC_DID	Manufacturer's Device Identifier
04	1	FMC_DDW	Device Data Width (16 bits on MVME5500)
05	1	FMC_NOD	Number of Devices Present (two on MVME5500)
06	1	FMC_NOC	Number of Columns (Interleaves) (two on MVME5500)
07	1	FMC_CW	Column Width in Bits (16 on MVME5500) This will always be a multiple of the device's data width.
08	1	FMC_WEDW	Write/Erase Data Width (16 on MVME5500) The Flash memory devices must be programmed in parallel when the write/erase data width exceeds the device's data width.
09	1	FMC_BANK	Bank Number of Flash Memory Array: 0 for this bank
0A	1	FMC_SPEED	ROM Access Speed in Nanoseconds
0B	1	FMC_SIZE	Total Bank Size (Should agree with the physical organization above): 07 = 32M

Table A-2 Flash 1 Memory Configuration Data

Byte Offset	Field Size (Bytes)	Field Mnemonic	Field Description
00	2	FMC_MID	Manufacturer's Identifier (FFFF = Undefined/Not-Applicable)
02	2	FMC_DID	Manufacturer's Device Identifier (FFFF = Undefined/Not-Applicable)
04	1	FMC_DDW	Device Data Width (16 bits on MVME5500)
05	1	FMC_NOD	Number of Devices Present (two on MVME5500)
06	1	FMC_NOC	Number of Columns (Interleaves) (two on MVME5500)
07	1	FMC_CW	Column Width in Bits (16 on MVME5500) This will always be a multiple of the device's data width.
08	1	FMC_WEDW	Write/Erase Data Width (16 on MVME5500) The two memory devices must be programmed in parallel when the write/erase data width exceeds the device's data width.
09	1	FMC_BANK	Bank Number of Memory Array: 1 for this bank
0A	1	FMC_SPEED	ROM Access Speed in Nanoseconds
0B	1	FMC_SIZE	Total Bank Size (Should agree with the physical organization above): 03 = 2M for this bank

A.2 L3 Cache Configuration Data

The L3 cache configuration data packet consists of byte fields that indicate the size/organization/type of the L3 cache memory array. Table A-3 further describes the L3 cache memory configuration VPD data packet.

Table A-3 L3 Cache Configuration Data

Byte Offset	Field Size (Bytes)	Field Description
00	1	Which processor is cache connected to: 01 - 1st Processor
01	1	Cache size: 01 - 2 MB
02	1	L3 cache core to cache ratio: (Backside Configurations - setting depends on processor core speed and SRAM capability) 06 - 4:1 (4)
03	1	Cache clock sample point: 02 - 4 clocks
04	1	Processor clock sample point: 03 - 3 clocks
05	1	Sample point override: 00 - sample point override disabled
06	1	SRAM clock control: 00 - SRAM clock control disabled
07	1	SRAM type: 00 - MSUG2 DDR SRAM
08	1	Data bus error detection type: 01 - parity
09	1	Address bus error detection type: 00 - None

Related Documentation

B.1 Emerson Network Power - Embedded Computing Documents

The publications listed below are referenced in this manual. You can obtain electronic copies of Emerson Network Power - Embedded Computing publications by contacting your local Emerson sales office. For released products, you can also visit our Web site http://www.emersonnetworkpower.com/embeddedcomputing. Under **Resources**, select **Technical Documentation**. This site has the latest copies of our product documentation.

Enter the manual you are looking for in the search field. Use either the publication number or the complete name of the product to search for available manuals.

Table B-1 Emerson Network Power - Embedded Computing Publications

Document Title	Publication Number
MVME5500 Single-Board Computer Installation and Use	V5500A/IH
MVME761 Transition Module Installation and Use	VME761A/IH
MVME712M Transition Module Installation and Use	VME712MA/IH
MOTLoad Firmware Package User's Manual	MOTLODA/UM
IPMC712/761 I/O Module Installation and Use	VIPMCA/IH
PMCspan PMC Adapter Carrier Board Installation and Use	PMCSPANA/IH

B.2 Manufacturer's Documents

You can also get additional information from manufacturers' documentation. Note that the information in these documents are subject to change without prior notice.

Table B-2 Manufacturers' Documents

Document Title and Source	Publication Number
MPC7450 RISC Microprocessor User's Manual Literature Distribution Center for Motorola Telephone: 1-800- 441-2447 FAX: (602) 994-6430 or (303) 675-2150 Web Site: http://ewww.motorola.com/webapp/sps/library/prod_lib.jsp E-mail: ldcformotorola@hibbertco.com	MPC7450UM/D Rev 2
MPC7450 RISC Microprocessor Hardware Specification Literature Distribution Center for Motorola Telephone: 1-800- 441-2447 FAX: (602) 994-6430 or (303) 675-2150 Web Site: http://ewww.motorola.com/webapp/sps/library/prod_lib.jsp E-mail: ldcformotorola@hibbertco.com	MPC7450EC/D Rev 3
GT-64260B System Controller for PowerPC Processors Data Sheet Marvell Technologies, Ltd. Web Site: http://www.marvell.com	MV-S100414-00B
Intel 82544EI Gigabit Ethernet Controller with Integrated PHY Data Sheet Intel Corporation Literature Center 19521 E. 32nd Parkway Aurora CO 80011-8141 Web Site: http://www.intel.com/design/litcentr/index.htm	82544.pdf
LXT971A 10/100Mbit PHY Datasheet Intel Corporation Literature Center 19521 E. 32nd Parkway Aurora CO 80011-8141 Web Site: http://www.intel.com/design/litcentr/index.htm	24941402.pdf

Table B-2 Manufacturers' Documents (continued)

Document Title and Source	Publication Number
3 Volt Synchronous Intel StrataFlash Memory 28F640K3, 28F640K18, 28F128K3, 28F128K18, 28F256K3, 28F256K18 (x16) Intel Corporation Literature Center 19521 E. 32nd Parkway Aurora CO 80011-8141 Web Site: http://www.intel.com/design/litcentr/index.htm	290737-003
3 Volt Intel StrataFlash Memory 28F128J3A, 28F640J3A, 28F320J3A Intel Corporation Literature Center 19521 E. 32nd Parkway Aurora CO 80011-8141 Web Site: http://www.intel.com/design/litcentr/index.htm	290667-005
PCI 6154 (HB2) PCI-to-PCI Bridge Data Book PLX Technology, Inc. 870 Maude Avenue Sunnyvale, California 94085 Web Site: http://www.hintcorp.com/products/hint/default.asp	6154_DataBook_v2.0.pdf
TL16C550C Universal Asynchronous Receiver/Transmitter Texas Instruments P. O. Box 655303 Dallas, Texas 75265 Web Site: http://www.ti.com	SLLS177E
3.3V-5V 256Kbit (32Kx8) Timekeeper SRAM ST Microelectronics 1000 East Bell Road Phoenix, AZ 85022 Web Site: http://eu.st.com/stonline/index.shtml	M48T37V

Table B-2 Manufacturers' Documents (continued)

Document Title and Source	Publication Number
2-Wire Serial CMOS EEPROM Atmel Corporation San Jose, CA Web Site: http://www.atmel.com/atmel/support/	AT24C02 AT24C04 AT24C64 AT24C256 AT24C512
Universe II User Manual Tundra Semiconductor Corporation Web Site: http://www.tundra.com/page.cfm?tree_id=100008#Universe II (CA91C042)	8091142_MD300_01.pdf

B.3 Related Specifications

Refer to the table below for related specifications. Note that the information in these documents are subject to change without notice.

Table B-3 Specifications

Document Title and Source	Publication Number
VITA http://www.vita.com/	
VME64 Specification	ANSI/VITA 1-1994
VME64 Extensions	ANSI/VITA 1.1-1997
2eSST Source Synchronous Transfer	VITA 1.5-199x
PCI Special Interest Group (PCI SIG) http://www.pcisig.com/	
Peripheral Component Interconnect (PCI) Local Bus Specification, Revision 2.0, 2.1, 2.2	PCI Local Bus Specification

Safety Notes

This section provides warnings that precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed during all phases of operation, service, and repair of this equipment. You should also employ all other safety precautions necessary for the operation of the equipment in your operating environment. Failure to comply with these precautions or with specific warnings elsewhere in this manual could result in personal injury or damage to the equipment.

Emerson intends to provide all necessary information to install and handle the product in this manual. Because of the complexity of this product and its various uses, we do not guarantee that the given information is complete. If you need additional information, ask your Emerson representative.

The product has been designed to meet the standard industrial safety requirements. It must only be used in its specific area of office telecommunication industry, industrial control, and development. It must not be used in safety critical components, life supporting devices or on aircraft.

Only personnel trained by Emerson or persons qualified in electronics or electrical engineering are authorized to install, remove or maintain the product. The information given in this manual is meant to complete the knowledge of a specialist and must not be used as replacement for qualified personnel.

Keep away from live circuits inside the equipment. Operating personnel must not remove equipment covers. Only factory authorized service personnel or other qualified service personnel is allowed to remove equipment covers for internal subassembly or component replacement or any internal adjustment.

Do not install substitute parts or perform any unauthorized modification of the equipment or the warranty may be voided. Contact your local Emerson representative for service and repair to make sure that all safety features are maintained.

Emerson and our suppliers take significant steps to make sure that there are no bent pins on the backplane or connector damage to the boards prior to leaving the factory. Bent pins caused by improper installation or by inserting boards with damaged connectors could void the Emerson warranty for the backplane or boards.

This product operates with dangerous voltages that can cause injury or death. Use extreme caution when handling, testing, and adjusting this equipment and its components.

EMC

FCC Class A
This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules, EN55022. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, can cause harmful interference to radio communications.
Operation of this equipment in a residential area is likely to cause harmful interference in which case the user is required to correct the interference at his own expense.
Use only shielded cables when connecting peripherals to assure that appropriate radio frequency emissions compliance is maintained. Installed blades must have the face plates installed and all vacant slots in the shelf must be covered.

For applications where this product is provided without a face plate, or where the face plate has been removed, your system chassis/enclosure must provide the required electromagnetic interference (EMI) shielding to maintain EMC compliance.

Board products are tested in a representative system to show compliance with the above mentioned requirements. A proper installation in a compliant system maintains the required performance.

As soon as you modify the product or change the default configuration you are responsible for complying with all relevant regulatory standards.

Battery

Product Damage
Incorrect replacement of lithium batteries can result in a hazardous explosion.
When exchanging the on-board lithium battery, make sure that the new and the old battery are exactly the same battery models.
If the respective battery model is not available, contact your local Emerson sales representative for the availability of alternative officially approved battery models.

Sicherheitshinweise

Dieses Kapitel enthält Hinweise, die potentiell gefährlichen Prozeduren innerhalb dieses Handbuchs vorrangestellt sind. Beachten Sie unbedingt in allen Phasen des Betriebs, der Wartung und der Reparatur des Systems die Anweisungen, die diesen Hinweisen enthalten sind. Sie sollten außerdem alle anderen Vorsichtsmaßnahmen treffen, die für den Betrieb des Systems innerhalb Ihrer Betriebsumgebung notwendig sind. Wenn Sie diese Vorsichtsmaßnahmen oder Sicherheitshinweise, die an anderer Stelle diese Handbuchs enthalten sind, nicht beachten, kann das Verletzungen oder Schäden am System zur Folge haben.

Emerson ist darauf bedacht, alle notwendigen Informationen zum Einbau und zum Umgang mit dem System in diesem Handbuch bereit zu stellen. Da es sich jedoch bei dem System um ein komplexes Produkt mit vielfältigen Einsatzmöglichkeiten handelt, können wir die Vollständigkeit der im Handbuch enthaltenen Informationen nicht garantieren. Falls Sie weitere Informationen benötigen sollten, wenden Sie sich bitte an die für Sie zuständige Geschäftsstelle von Emerson.

Das Produkt erfüllt die für die Industrie geforderten Sicherheitsvorschriften und darf ausschließlich für Anwendungen in der Telekommunikationsindustrie, im Zusammenhang mit Industriesteuerungen und in der Entwicklung verwendet werden. Es darf nicht in sicherheitskritischen Anwendungen, lebenserhaltenden Geräten oder in Flugzeugen verwendet werden.

Einbau, Wartung und Betrieb dürfen nur von durch Emerson ausgebildetem oder im Bereich Elektronik oder Elektrotechnik qualifiziertem Personal durchgeführt werden. Die in diesem Handbuch enthaltenen Informationen dienen ausschließlich dazu, das Wissen von Fachpersonal zu ergänzen, können dieses jedoch nicht ersetzen.

Halten Sie sich von stromführenden Leitungen innerhalb des Systems fern. Entfernen Sie auf keinen Fall die Systemabdeckung. Nur werksseitig zugelassenes Wartungspersonal oder anderweitig qualifiziertes Wartungspersonal darf die Systemabdeckung entfernen, um Systemkomponenten zu ersetzen oder andere Anpassungen vorzunehmen.

Installieren Sie keine Ersatzteile oder führen Sie keine unerlaubten Veränderungen am System durch, sonst verfällt die Garantie. Wenden Sie sich für Wartung oder Reparatur bitte an die für Sie zuständige Geschäftsstelle von Emerson. So stellen Sie sicher, dass alle sicherheitsrelevanten Aspekte beachtet werden.

Emerson und unsere Zulieferer unternehmen größte Anstrengungen um sicherzustellen, dass sich Pins und Stecker von Boards vor dem Verlassen der Produktionsstätte in einwandfreiem Zustand befinden. Verbogene Pins, verursacht durch fehlerhafte Installation oder durch Installation von Boards mit beschädigten Steckern kann die durch Emerson gewährte Garantie für Boards und Backplanes erlöschen lassen.

Dieses Produkt wird mit gefährlichen Spannungen betrieben, die zu Verletzungen und Tod führen können. Seien Sie im Umgang mit dem Produkt und beim Testen und Anpassen des Produktes und seiner Komponenten äußerst vorsichtig.

EMV

FCC Class A
Das Produkt wurde getestet und erfüllt die für digitale Geräte der Klasse A gültigen Grenzwerte gemäß den FCC-Richtlinien Abschnitt 15 bzw. EN 55022 Klasse A. Diese Grenzwerte sollen einen angemessenen Schutz vor Störstrahlung beim Betrieb des Produkts in Geschäfts-, Gewerbe- sowie Industriebereichen gewährleisten. Das Produkt arbeitet im Hochfrequenzbereich und erzeugt Störstrahlung. Bei unsachgemäßem Einbau und anderem als in diesem Handbuch beschriebenen Betrieb können Störungen im Hochfrequenzbereich auftreten.
Diese Einrichtung kann im Wohnbereich Funkstörungen verursachen; in diesem Fall kann vom Betreiber verlangt werden, angemessene Maßnahmen durchzuführen und dafür aufzukommen.
Benutzen Sie zum Anschließen von Peripheriegeräten ausschließlich abgeschirmte Kabel. So stellen Sie sicher, dass ausreichend Schutz vor Störstrahlung vorhanden ist. Die Blades müssen mit der Frontblende installiert und alle freien Steckplätze müssen mit Blindblenden abgedeckt sein.
Änderungen, die nicht ausdrücklich von Emerson erlaubt sind, können Ihr Recht das System zu betreiben zunichte machen.

Wenn dieses Produkt ohne Frontblende ausgeliefert wird oder wenn die Frontblende entfernt wird, muss Ihr System die notwendigenSchutzmechnismen gegen elektromagnetische interferenzen bereitstellen, um die Einhaltung der eletromagnetischen Verträglichkeit des Systems zu gewährleisten.

Boardprodukte werden in einem repräsentativen System getestet, um zu zeigen, dass das Board den oben aufgeführten EMV-Richtlinien entspricht. Eine ordnungsgemäße Installation in einem System, welches die EMV-Richtlinien erfüllt, stellt sicher, dass das Produkt gemäß den EMV-Richtlinien betrieben wird.

Sobald Sie das Produkt oder seine Standardkonfiguration verändern, müssen Sie dafür sorgen, dass alle relevanten Richtlinien eingehalten werden.

Batterie

Beschädigung des Produktes
Fehlerhafter Austausch von Lithium-Batterien kann zu gefährlichen Explosionen führen.
Wenn Sie die Lithium-Batterie auf dem Produkt austauschen, stellen Sie sicher, dass die alte und die neue Batterie vom gleichen Typ sind.
Ist der Batterietyp nicht verfügbar, wenden Sie sich an Emerson um herauszufinden, welcher Batterietyp offiziell alternativ verwendet werden darf.

Index

B
block diagram 15

C
cache 43
comments and suggestions 11
configuration header 25
contact address 11
conventions 10
core frequency 42
CPU bus mode 42

D
documentation
    related 49

F
features 13
feedback 11
flash memory 41
    configuration data 45

G
geographical address register 27
GPP configuration 34
GPP interrupt assignments 31
GT-64260B initialization 34
GT-64260B system controller 30
    device bank timing parameters 39
    device controller banks 39
    GPP configuration 34
    interrupt controller 31
    power-up config 37
    reset configuration 36

I
I2C bus device addressing 33
IDSEL mapping 30
initialization
    GT-64260B 34
interrupt controller 31

L
L1, L2, L3 cache 43
L3 cache configuration data 47

M
manufacturers' documents 50
memory map
    default PCI 18
    MOTLoad PCI 19
    MOTLoad processor 17
    processor 16
    system I/O 20
memory maps 16

N
NVRAM 28

P
PCI arbiter 41
PCI arbitration assignments 41
PCI configuration space 30
PLL clock generators 40
presence detect register 24
processor bus mode 42
processor version register 43

R
real-time clock 28
register
    geographical address 27
    presence detect 24
    switch (S1) 25
    system status 1 21
    system status 2 22
    system status 3 24
    time base enable 26
related documentation 49
RTC 28

S
space map
    PCI I/O 20
system clock generators 40
system status register 1 21
system status register 2 22
system status register 3 24

T
temperature sensor 41

time base enable register 26
two-wire serial interface 33

U
UART 28

V
vital product data (VPD) 45
flash memory 45
L3 cache 47

HOW TO REACH LITERATURE AND TECHNICAL SUPPORT:

For literature, training, and technical assistance and support programs, visit
www.emersonnetworkpower.com/embeddedcomputing

Emerson Network Power.
The global leader in enabling Business-Critical Continuity™

www.emersonnetworkpower.com/embeddedcomputing

- AC Power Systems
- Connectivity
- DC Power Systems
- **Embedded Computing**
- Embedded Power
- Integrated Cabinet Solutions
- Outside Plant
- Power Switching & Control
- Precision Cooling
- Services
- Site Monitoring
- Surge & Signal Protection

Emerson, Business-Critical Continuity, Emerson Network Power and the Emerson Network Power logo are trademarks and service marks of Emerson Electric Co.
All other product or service names are the property of their respective owners.
© 2009 Emerson Electric Co.

Artisan Technology Group is an independent supplier of quality pre-owned equipment

Gold-standard solutions

Extend the life of your critical industrial, commercial, and military systems with our superior service and support.

We buy equipment

Planning to upgrade your current equipment? Have surplus equipment taking up shelf space? We'll give it a new home.

Learn more!

Visit us at **artisantg.com** for more info on price quotes, drivers, technical specifications, manuals, and documentation.

Artisan Scientific Corporation dba Artisan Technology Group is not an affiliate, representative, or authorized distributor for any manufacturer listed herein.

We're here to make your life easier. How can we help you today?

(217) 352-9330 | sales@artisantg.com | artisantg.com

ARTISAN® TECHNOLOGY GROUP