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ES1130.2
Simulation Controller Board
User's Guide

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1 Introduction

This section contains information about the basic features and areas of implementation of the ES1130.2 Simulation Controller Board. A block diagram is also included here to show the schematic layout of the board.

note

Some components of the board may be damaged or destroyed by electrostatic discharges. Please keep the board in its storage package until it is installed. The board should only be taken from its package, configured and installed at a working place that is protected against static discharge.

1.1 Functions

The ES1130.2 Simulation Controller Board is a universal processor module for VMEbus systems. The module is composed of two PowerPC processors: an MPC750, the high-performance main processor, and an MPC860T which acts as a communication processor. The two processors are linked using a Dual-Ported RAM. Each of the two processors has its own Flash ROM as program memory and its own RAM.

The MPC750 processor is equipped with a VMEbus interface. The VMEbus interface is designed for both master and slave access. The board can also be used as the system controller.

The MPC860T communication processor has an Ethernet interface. The interface can either be operated with 10 or 100 MBit/s. The data rate is recognized automatically.

The board has the following features:

- fully adapted to automotive requirements, temperature range of -40 .... 85°C
- high-performance main processor
  - MPC750 PowerPC with L2 cache
  - SDRAM (SO-DIMM)
  - Flash memory
  - EEPROM
  - Dual-Ported RAM to the VME bus (slave)

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- VMEbus interface
  - master interface: A16:D16, A24:D16, A40:MD32
  - slave interface: A24:D16, A40:MD32
  - interrupt controller
  - system controller with automatic activation
  - bus timer: BTO (256)
  - auto-ID configuration
- high-performance host interface via Ethernet
  - PowerPC MPC860T
  - SRAM
  - Flash memory
  - Ethernet 10/100 MBit/s, automatic recognition
  - Dual-Ported RAM to the MPC750
- JTAG interface as a test interface
- extension socket

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The following figure shows the front panel and the position of the plug connector.



Fig. 1-1 Front Panel

1.2 Areas of Implementation

The ES1130.2 Simulation Controller Board can be used in VMEbus systems wherever high performance is necessary. The Ethernet interface provides a simple link to host PCs.

Possible areas of implementation include:

- high-performance simulation processor for real-time applications.
- control of VMEbus boards for data acquisition and signal generation.

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1.3 Block Diagram

The following figure shows you a block diagram of the ES1130.2 Simulation Controller Board.

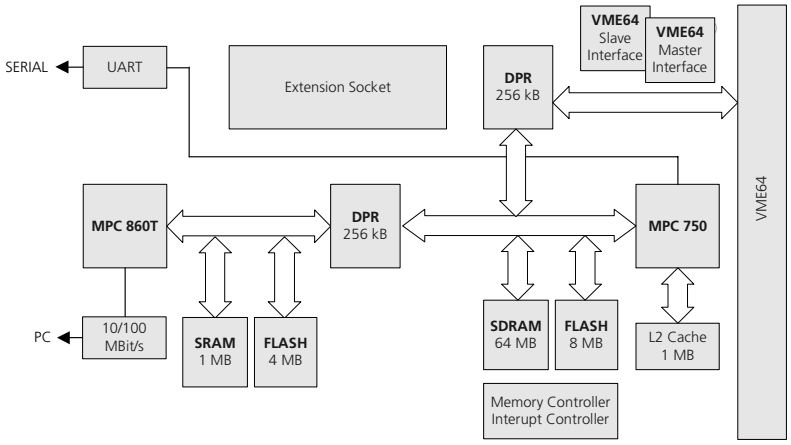


Fig. 1-2 Block Diagram

In the block diagram, you can see the communication processor (MPC860T) and the main processor, MPC750. Both processors have their own memory areas which are composed of Flash ROM and RAM. Data is exchanged between the processors via the shared Dual-Ported RAM.

The communication processor, MPC860T, is equipped with an Ethernet interface. The Ethernet interface can be operated with 10 or 100 MBit/s.

The connection to the VMEbus takes place via an interface of the main processor, MPC750. The interface allows both master and slave access attempts to the VMEbus.

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2 Hardware

This section contains a detailed functional description, the pin allocation of the connectors and the technical data of the board.

2.1 Functional Description

This section describes each feature of the ES1130.2 Simulation Controller Board. You will find information on the following subjects:

- main processor, MPC750
- VMEbus interface
- communication processor, MPC860T
- Ethernet interface
- Dual-Ported RAM
- power supply

2.1.1 Main Processor - MPC750

The MPC750 processor is the central processing unit of the board. It works at a clock rate of 366 MHz.

The following sections provide you with detailed information on the components of this unit.

Memory

The MPC750 can address the following memory areas.

Memory Area	Size
SDRAM	64 MBytes
VMEbus master A24	16 MBytes
VMEbus master A40	1 GByte
Dual-Ported RAM to the MPC860T	256 KBytes
Dual-Ported RAM to the VMEbus	256 KBytes
EEPROM	8 KBytes
Flash ROM	8 MBytes

Tab. 2-1 Memory Areas of the MPC750

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32-Bit-Counter (Decrementer)

The MPC750 has two 32-bit counters at its disposal. The counters are loaded with a start value by writing to register addresses. Once the relevant release bits have been set in the status register, the counters are counted downwards at a rate of 16.66 MHz. The overflow from 0 to -1 results in an interrupt.

Watchdog

The board's watchdog can be programmed to the intervals 4027 ms, 1007 ms, 252 ms and 63 ms. Once the supply voltage has been switched on, the longest interval is set and the watchdog released. The watchdog can be locked via a bit in the status register but can only be released by a switch-on cycle. A certain byte sequence has to be written to the watchdog service register to reset the watchdog.

Interrupt Controller

The MPC750 can react to interrupts from different sources. The following interrupt sources can occur:

- interrupt of the 32-bit counters
- interrupts from the VMEbus
- MPC860T communication interrupt
- VMEbus slave communication interrupt

Different interrupt levels can be assigned to the different interrupt sources using registers. Fixed vectors and priorities are allocated to the interrupt levels.

Interrupt level 0 has the highest priority and interrupt level 15 the lowest.

Every interrupt level can be released or locked individually using an interrupt mask register.

Board Control and Status Register (BCSR)

The board control and status register is composed of different registers with which different features and statuses of the board can be controlled or read.

The following are some of the available registers:

- configuration register board
- status register board
- interrupt controller: configuration and mask register
- counter
- system time
- VMEbus configuration and control register

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- watchdog service register

The registers are used by the board's firmware for controlling and monitoring the hardware functions.

2.1.2 VMEbus Interface

The VMEbus interface can act both as a master and as a slave interface.

The board is linked as a VMEbus slave using shared memory areas which are in the address space of the VMEbus and MPC750.

Master Interface

The master interface can execute A16, A24 and A40 accesses. Please consult the following table for the size of the allocated memory areas and the relevant address modifiers.

Memory Area	Modifier	Size
A24 supervisory BLT	3F	16 MBytes
A24 supervisory program	3E	16 MBytes
A24 supervisory data	3D	16 MBytes
A24 non-privileged BLT	3B	16 MBytes
A24 non-privileged program	3A	16 MBytes
A24 non-privileged data	39	16 MBytes
CR/CSR	2F	16 MBytes
A16 non-privileged access	29	64 KBytes
A16 supervisory access	2D	64 KBytes
Vector fetch	-	14 bytes
A40	34	1 GByte

Tab. 2-2 Access Variants of the VMEbus Master Interface

It is allowed for the MPC750 as VMEbus master to access the card-specific configuration ROM / control and status register area (CR/CSR) in A24 mode.

The MPC750 is *not*, however, allowed to access the card-specific Dual-Ported RAM as VMEbus master. This memory area can be read and written directly.

Before there is a master access to the VMEbus, the requester level and mode have to be set via the board control and status register. The ES1130.2 Simulation Controller Board supports a single-level arbiter.

The requester mode is oriented to the particular implementation. The setting "release on request" is the most sensible for single-master systems.

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In A40 mode, the MPC750 can address the entire A40 address space of the VMEbus. The larger A40 address space is mapped to the smaller MPC750 address space via a segment register. The VMEbus A40 address is composed of the bottom 30 bits of the MPC750 access address and 10 bits from the segment register.

Slave Interface

The VMEbus slave interface allows the VMEbus to access the Dual-Ported RAM shared by the MPC750 and VMEbus.

The slave interface supports both A24 and A40 access attempts. The basic address via which the Dual-Ported RAM can be accessed by the VMEbus, is determined via a register in the CR/CSR area.

The Dual-Ported RAM is *not* allowed to be accessed via the proprietary VMEbus master interface.

Configuration ROM / Control and Status Register (CR/CSR) Slave

The CR/CSR slave makes various configuration and status registers available for the configuration of the board in concurrence with the VME64 norm.

The address position of the CR/CSR area is determined by the auto-ID cycle after the supply voltage has been switched on.

The CR/CSR registers can be divided into the following areas:

- configuration ROM in concurrence with the VME64 norm
- card-specific configuration ROM
- card-specific control and status register
- control and status register in concurrence with the VME64 norm

VMEbus Slot1 Controller

The ES1130.2 Simulation Controller Board can independently recognize whether it should act as a system controller or not. The ES1130.2 assumes this function if it is in Slot1.

2.1.3 MPC860T Communication Processor

The MPC860T communication processor controls data transfer via the Ethernet interface. It has its own Flash ROM and SRAM, as well as an internal interrupt logic.

Data is exchanged between the MPC860T communication processor and the main processor, MPC750, via the shared Dual-Ported RAM.

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The MPC860T makes several other functions available:

- board reset
- reset of the MPC750
- reset of the Ethernet interface driver
- /SYSRES of the VMEbus
- switching of the boot memory for the MPC750 from Flash or Dual-Ported RAM
- switching of the boot memory from Flash or Dual-Ported RAM
- programming interface for firmware, EPLD and FPGA
- BDM interface

2.1.4 Ethernet Interface

The board is equipped with an Ethernet interface in concurrence with the 10/100BaseT standard. To be able to come up to the requirements of operation in automotive vehicles, a plug connector is used that does not actually conform to this standard.

The Ethernet interface is responsible for the connection of the ES1130.2 Simulation Controller Board to a host processor. The interface can be operated either with 10 or 100 MBit/s, half or full-duplex. Switching takes place automatically.

Every ES1130.2 Simulation Controller Board is equipped with an individual Ethernet address (MAC address) and a standard IP address. The standard settings of the board when it is delivered to the customer can be found in the section "Ethernet, IP Address and Subnet Mask" on page 19.

note

The PC connection cable CBE100-3 which is part of the delivery scope of the ES1130.2 Simulation Controller Board is only suitable for the direct connection to a host system.

2.1.5 Dual-Ported RAM

The Dual-Ported RAM is used for the data exchange between the main processor, MPC750, and the communication processor, MPC860T. The access of the two processors to the shared memory area is controlled by a semaphore register.

The MPC860T can determine whether the MPC750 loads its boot program from the Flash memory or from the Dual-Ported RAM after a reset via an output. This mechanism makes it possible to load programs for the MPC750 via the Ethernet interface of the MPC860T.

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2.1.6 Power Supply

The board has its own +3.3 V voltage regulator. This means it can be operated in card cages which only make +5 V supply voltage available. If the card cage makes +3.3 V available, the card automatically switches to the external supply with +3.3 V.

2.2 Hardware Configuration

The board has *no* jumpers or solder straps which have to be configured.

2.3 Displays

The meaning of the LEDs on the front panel is given in the following tables.

LED	Status	Meaning				
MCD		MPC750: **M**aster **C**PU **D**isplay				
	Off	Normal operation				
	On	Reset on MPC750 (independent from the source)				
	Blinking	- receiving L1-Message while active L1-Loader - Failure: exeption, dependent on vector				
MCI		MPC750: **M**aster **C**PU **I**nterrupt				
	On	Interrupt on MPC750				
MSF		VMEBus: **M**odule/**S**ys**f**ail				
	Off	Normal operation				
	On	Failure: SysFail on VMEbus generated; (no failure while boot up or reset)				
SCD		MPC860: **S**lave **C**PU **D**isplay				
	Off	Normal operation				
	On	Error status firmware				
	Blinking	Activity of Ethernet-Link:	LED-Status (in msec)			
			on	off	on	off
		- no Link:	100	100	100	100
		- 10 MBit-Link Half Duplex:	100	500	100	500
		- 100 MBit-Link Half Duplex:	500	500	500	500
		- 100 MBit-Link Full Duplex:	500	100	500	500

Tab. 2-3 Meaning of the front panel LEDs

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2.4 Pin Allocation

This section contains the pin allocation of the front-facing connector and the backplane connector of the ES1130.2 Simulation Controller Board.

2.4.1 "Serial" Plug Connector

The "Serial" plug connector has three lines for the serial interface of the MPC750 main processor.

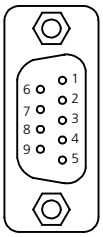


Fig. 2-1 "Serial" Plug Connector

Pin	Function	Pin	Function
1	reserved	2	RxD
3	TxD	4	reserved
5	GND	6	open
7	reserved	8	reserved
9	open		

Tab. 2-4 "Serial" Pin Allocation

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2.4.2 "PC" Plug Connector

The "PC" plug connector contains the lines for the Ethernet interface. The plug connector is designed as a eight-pin Lemo socket of size 1B.

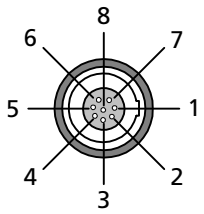


Fig. 2-2 "PC" Plug Connector

Pin	Function	Pin	Function
1	n.c.	5	TX-
2	n.c.	6	RX-
3	n.c.	7	n.c.
4	RX+	8	TX+

Tab. 2-5 "PC" Pin Allocation

2.4.3 Backplane Connector

The following table shows the allocation of the 160-pin backplane connector. The signals marked "/" are low-active.

Pin	Row z	Row a	Row b	Row c	Row d
1	open	D00	/BBSY	D08	open
2	GND	D01	/BCLR	D09	open
3	open	D02	/ACFAIL	D10	open
4	GND	D03	/BG0IN	D11	open
5	open	D04	/BG0OUT	D12	open
6	GND	D05	/BG1IN	D13	open
7	open	D06	/BG1OUT	D14	open
8	GND	D07	/BG2IN	D15	open
9	open	GND	/BG2OUT	GND	/GAP
10	GND	SYSCLK	/BG3IN	/SYSFAIL	open

Tab. 2-6 VME 64 Pin Allocation

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Pin	Row z	Row a	Row b	Row c	Row d
11	open	GND	/BG3OUT	/BERR	open
12	GND	/DS1	/BR0	/SysReset	open
13	open	/DS0	/BR1	/LWORD	open
14	GND	/WRITE	/BR2	AM5	open
15	open	GND	/BR3	A23	open
16	GND	/DTACK	AM0	A22	open
17	open	GND	AM1	A21	open
18	GND	/AS	AM2	A20	open
19	open	GND	AM3	A19	open
20	GND	/IACK	GND	A18	open
21	open	/IACKIN	res.	A17	open
22	GND	/IACKOUT	res.	A16	open
23	open	AM4	GND	A15	open
24	GND	A07	/IRQ7	A14	open
25	open	A06	/IRQ6	A13	open
26	GND	A05	/IRQ5	A12	open
27	open	A04	/IRQ4	A11	open
28	GND	A03	/IRQ3	A10	open
29	open	A02	/IRQ2	A09	open
30	GND	A01	/IRQ1	A08	open
31	open	-12 V	+5 V Stby	+12 V	open
32	GND	+5 V	+5 V	+5 V	open

Tab. 2-6 VME 64 Pin Allocation

2.5 PC Connection Cable

A special cable is needed to connect the ES1130.2 Simulation Controller Board to the PC: the cable is perfectly adapted to the requirements (resulting from the high transfer rates).

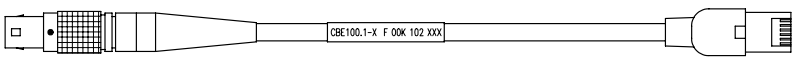


Fig. 2-3 PC Connection Cable CBE100-X

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The following table provides you with more information on other available types of cable and their order numbers.

Order Designation	Abbreviation	Order Number
PC connection cable, 3 m	CBE100-3	F 00K 102 559
PC connection cable, 8 m	CBE100-8	F 00K 102 571
PC connection cable, 20 m	CBE100-20	F 00K 102 570

2.6 Technical Data

This section contains the technical data on the ES1130.2 Simulation Controller Board in tabular form.

MPC750 Main Processor

Microprocessor	MPC750 PowerPC, 366 MHz, 64-bit 1 MByte L2 cache, bus rate 66 MHz
Memory	64-MByte SDRAM (SO-DIMM, 64 bit/burst) 8-MByte Flash (64-bit) 8-KByte parallel EEPROM 256-KByte Dual-Ported RAM to the VMEbus 256-KByte Dual-Ported RAM to the MPC860T
Function modules	2 counters, 32-bit, programmable Watchdog, programmable Interrupt controller, programmable

MPC860T Communication Processor

Microprocessor	MPC860T PowerPC, bus rate 50 MHz
Memory	1-MByte SRAM 4-MByte Flash 256-KByte Dual-Ported RAM to the MPC750

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Ethernet, IP Address and Subnet Mask

Type	10/100BaseT, automatic configuration
Ethernet address (MAC)	Individual for each board
IP address	192.168.40.11
Subnet mask	255.255.255.0

VMEbus

Type	Master interface and slave interface
Access types: master interface	A16:D16; A24:D16; A40:MD32
Access types: slave interface	A24:D16; A40:MD32
Interrupter	2 interrupters; levels 1 to 7, programmable
Interrupt handler	2 interrupt handlers; levels 1 to 7, programmable
System controller	Automatic Slot1 detection
Bus timer	BTO (256)
Configuration	Auto-ID procedure

Power Supply

With exclusive powering with +5 V	+5 (-0.125, +0.25) V DC, max. 2400 mA
With powering with +3.3 V and +5 V	+3.3 V DC, ±5%, max. 3600 mA +5 (-0.125, +0.25) V DC, max. 500 mA

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Environmental Conditions

Ambient temperature during operation	-40 °C to +85 °C (extended temperature range)
Storage temperature	-55 °C to +85 °C
Relative humidity	0 to 95%, no condensation

Plug Connectors

Backplane	160-pin DIN 41612
Front panel	Ethernet: 8-pin Lemo, size 1B

Physical Dimensions

Circuit board	100 x 160 mm²
Front panel	Height: 3 U Width: 4 HP

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3 Firmware

This section contains the description of the ES1130.2 Simulation Controller Board firmware. As the ES1130.2 board contains two processors, the implemented firmware is also divided into two separate parts:

- the MPC860T firmware establishes the communication between the host PC and the control processor, MPC750. Additional tasks are:
  - booting the MPC750 processor
  - loading the programs for the MPC750
  - updating the programmable devices (FPGA and EPLDs)
  - controlling firmware updates
- the Flash memory of the MPC750 contains a small loader which provides the following functionality:
  - controlling the boot procedure
  - loading the program code into the SDRAM
  - programming the program code into the Flash

Additional system programs are linked together and loaded with the program code of the MPC750. The system programs have the following tasks:

- starting and stopping the main program
- communicating with the main program
- logging data streams

3.1 Communicating with the Host PC

The communication between the host PC and the ES1130.2 Simulation Controller Board is based on the L1 protocol. According to this protocol, every message contains 20 bytes of header information followed by a data field of up to 15980 bytes length limiting the maximum length of the whole message to 16000 bytes.

The following figure shows the structure of a message.

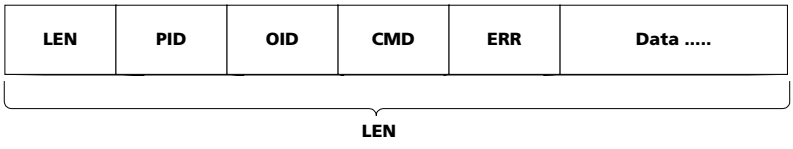


Fig. 3-1 Structure of a Message According to L1 Protocol

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The terms have the following significance:

Field	Significance
LEN	Length of complete message in bytes
PID	Process ID for addressing distributed software components
OID	ID for addressing objects of each software component
CMD	Command for the object to execute
ERR	Error code from the executed command (return value)
Data	Data

Tab. 3-1 Message Fields

The L1-protocol communication is always triggered by the host PC. Protocol handling follows a simple handshake scheme, i.e. each message has to be answered before the next request may be sent. A time-out mechanism prevents communication deadlocks.

The firmware of the MPC860T and the MPC750 implements a small set of commands to control the program execution. All other messages are transferred directly to the main program of the MPC750.

The following two tables provide you with an overview of the commands implemented in the firmware:

Field	Significance
StopPPC	Resets the MPC750
GetID	Requests ID of hardware and firmware
Program-RamFast	Downloads the main program for the MPC750 into the DPRAM
StartPPC	Sets "Boot from DPRAM" for the MPC750 Triggers the MPC750 mailbox interrupt Starts the MPC750 Waits for "MPC750 boot acknowledge" Sets "Boot from Flash" for the MPC750

Tab. 3-2 Commands for the Firmware of the MPC860T

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Field	Significance
GetID	Requests ID of hardware and firmware
Program-RamFast	Downloads the main program for the MPC750 into the SDRAM
EraseFlash	Erases the MPC750 Flash memory
Program-RomFast	Programs the main program of the MPC750 in the Flash memory
StartPPC	Starts the main program of the MPC750

Tab. 3-3 Commands for the Firmware of the MPC750

The TCP/IP protocol forms the communication layer beneath the L1 protocol. The MPC860T firmware implements a socket to establish the communication link.

3.1.1 Program Execution

After power-on both processors boot from their Flash memory. The following sections give a short introduction to the firmware functionality of both controllers.

3.1.2 MPC860T

Once switched on the processor initializes all the relevant peripherals, e.g. the RS232 and Ethernet interfaces. A system task is started that waits for a communication link to be established. The host PC initiates the establishing of the TCP/IP connection. It uses the default address 192.168.40.11 and port 18001 of the ES1130.2 Simulation Controller Board.

Once the connection has been established, additional data channels can be created with different port numbers. Currently one extra socket is created as a data channel with the port number 18002.

After setting up the communication, the MPC860T acts as a transparent gateway for the incoming L1 messages from the host. Only the commands from the table "Commands for the Firmware of the MPC860T" on page 22 are evaluated by the MPC860T firmware.

If the host communication breaks down for any reason, all related tasks on the MPC860T are shut down and restarted. Afterwards a new communication session may be established by the host.

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3.1.3 MPC750

A reset triggers the MPC750 to boot from its Flash memory. After initializing the processor, the loader is copied into the SDRAM and executed there. The loader then copies the main program together with the system code into the SDRAM and the starts the main program in the SDRAM.

This kind of main program always resides in the Flash memory because the ES1130.2 Simulation Controller Board is delivered with a standard main program and this can only be replaced by programming a new standard main program.

Loading and/or programming a new main program works as follows:

- the MPC860T resets the MPC750 and switches to "boot from DPRAM"
- a new loader is written to the DPRAM and the MPC750 is started. This loader is then copied into the SDRAM and executes from there and
- the loader writes the main program into the SDRAM (standard download) or programs the code into the Flash memory (standalone code).

The downloading procedure looks slightly different if an ES1120 System Controller Board acts as a system controller and takes over communication with the host PC. In this case, the MPC750 receives the program code to be loaded via the dual-ported RAM of the VMEbus interface.

Once the load procedure is completed, the main program is started. All L1 commands apart from those in "Commands for the Firmware of the MPC750" on page 23 are forwarded to this main program.

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