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EXC-1553PC/E

User's Manual

EXCALIBUR SYSTEMS

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MIL-STD-1553 TEST AND SIMULATION BOARD

FEATURES

* OPERATES AS BC,RT,BC/CONCURRENT-RT OR MONITOR
* MULTIPLE PROTOCOL CAPABILITY (ie 1553A, B, F-16, MaCair)
* ERROR INJECTION CAPABILITY :
  - BIT COUNT
  - WORD COUNT
  - INCORRECT SYNC
  - PARITY
  - INCORRECT RT ADDRESS
  - NON-CONTIGUOUS DATA
* MULTI-MODE TRIGGERABLE MONITOR
* REAL-TIME OPERATION
* COMPATIBLE WITH PC, XT®, and AT® (286,386...) COMPUTERS
* MULTIPLE-RT SIMULATION (UP TO 32 REMOTE TERMINALS)
* PROGRAMMABLE BROADCAST MODE
* MEMORY-MAPPED, DUAL-PORT RAM
* MENU-DRIVEN SOFTWARE AVAILABLE
* EASY TO INSTALL AND OPERATE
* _C_ SOFTWARE LIBRARY INCLUDED
* EXTENSIVE INTERRUPT FEATURES

The EXC-1553PC/E is an intelligent MIL-STD-1553 interface card for PC, XT, and AT compatible computers. It allows for the testing and simulation of the MIL-STD-1553 bus. The user has direct access to all control registers and data blocks. The user controls the operation of the card by accessing the memory-mapped control registers. The EXC-1553PC/E contains an 18kx8 [true dual-ported] RAM for data blocks, control registers, and look-up tables. The PCE comes complete with menu-driven software, a C-driver software library with source codes, and 1553 adapter cables.

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TABLE OF CONTENTS

Introduction .....page 1
Installation .....page 2
1553 Bus Connections .....page 2

Bus Controller Operation .....page 3
- Memory Map .....page 4
- Message Block Formats .....page 13
- Continuous or One Shot Message Transfers .....page 16
- Program example .....page 18
- Control Register Definitions .....page 19

Remote Terminal Operation .....page 27
- Memory Map .....page 28
- Data Block Look-Up Table .....page 29
- How to Create the Address to the Table .....page 30
- Active RT Table .....page 31
- Message Stack .....page 33
  - Message Status Word .....page 34
  - Time Tag .....page 36
- Mode Codes .....page 38
- Broadcast Mode .....page 38
- Error Injection Features .....page 39
- Program example .....page 40
- Control Register Definitions .....page 41

Bus Controller / Concurrent-RT Operation .....page 48
- Memory Map .....page 49
- Remote Terminal Simulation .....page 58
- Message Block Formats .....page 59
- Continuous or One Shot Message Transfers .....page 62
- Program example .....page 64
- Control Register Definitions .....page 65

Bus Monitor Operation .....page 73
- Sequential Mode Memory Map .....page 74
- Sequential Link-List Memory Map .....page 75
- Fixed Block Operation .....page 76
- Link-List Operation .....page 78
- Look-Up Table Memory Map .....page 80
- Look-Up Table Operation .....page 81
- Message Status Word (all BM modes) .....page 84
- Time Tag .....page 86
- Trigger Operation (Seq. Fixed Block Mode Only) .....page 87
- Program example (all BM modes) .....page 90
- Control Register Definitions (all BM modes) .....page 92

1553 A / B / F-16 / Multi-Protocol Considerations .....page 98
Switching Modes of Operation .....page 98
Board Layout .....page 99
Led Indicators .....page 99
Dip Switch Settings .....page 99
- Factory Default Dip Switch Settings .....page 102

Connectors .....page 103
Power Requirements .....page 105
Ordering Information .....page 105

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INTRODUCTION

The EXC-1553PC/E is a memory-mapped MIL-STD-1553 interface card which operates within PC, XT and AT-compatible machines including 286,386,486.. -based models. The "PCE" is the perfect solution for developing and testing 1553 interfaces and for performing system simulation of the 1553 bus. The user has access to all control registers and can modify various parameters and data in Real Time. The board has four modes of operation ; Bus Controller, Remote Terminal (Multiple - up to 32 RT_s), BC with Concurrent RT operation (up to 32 RT_s), and a Triggerable Monitor.

The boards can operate within different 1553 protocol environments (e.g. MIL-STD-1553 A,B, F-16 and MaCair). This flexibility emerges from the extensive programmability of the 1553-related parameters such as Response Time, Status Word content, etc. Error injection capability exists in the BC, RT, and BC/Concurrent-RT modes.

Figure 1 shows the block diagram of the EXC-1553PC/E card.

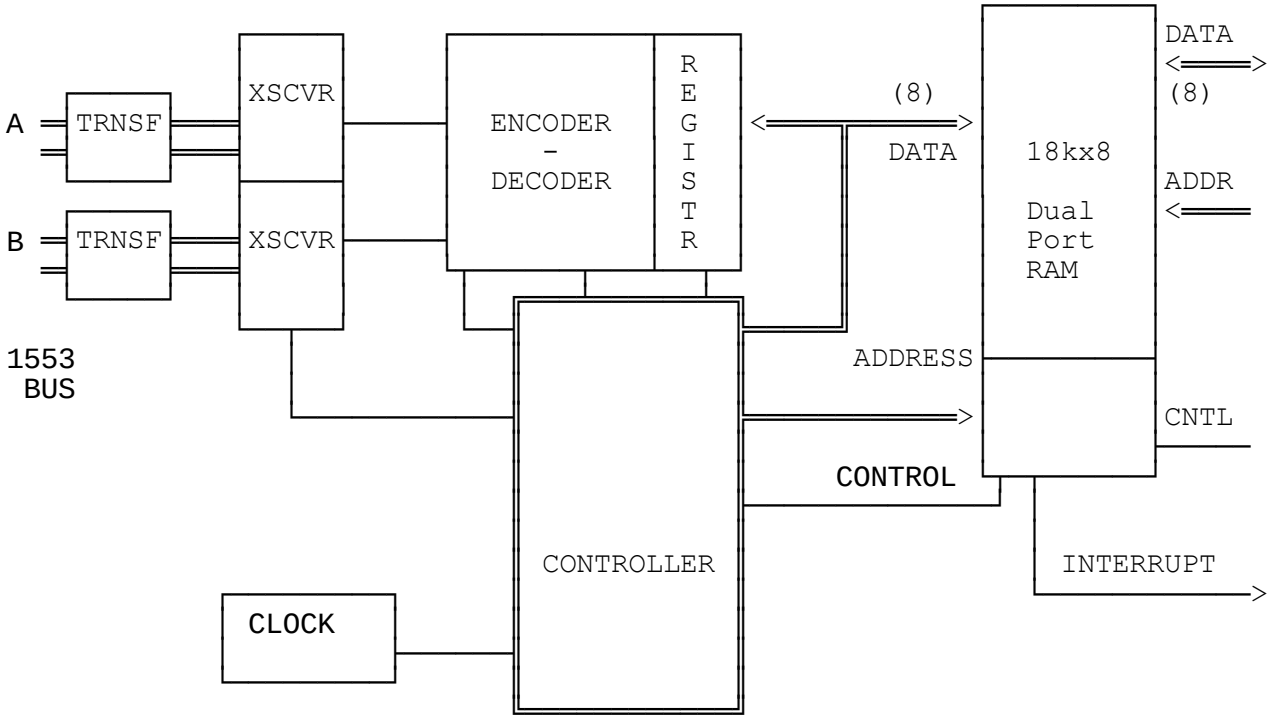


Figure 1. EXC-1553PC/E BLOCK DIAGRAM

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INSTALLATION

Before installing the card it is very important to determine which half segment of memory is available on the users computer. A variety of programs such as SYSINFO may be used to determine what memory segments are in use by the BIOS and any other adapter cards may be in the computer.

Note: If a segment which is already in use is used for the EXC-1553PC/E the card will exhibit unpredictable behavior. It may work in some modes but not others or may seem to work fine but will exhibit occasional errors or it may not function at all.

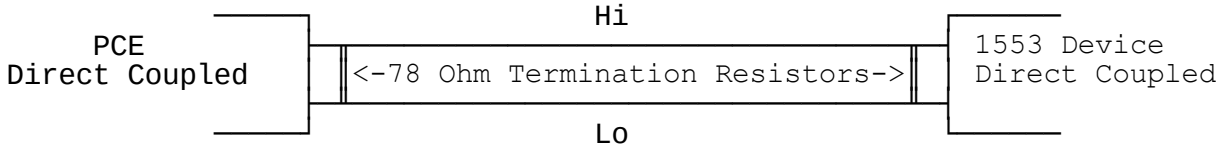
Once a free segment is found, dip switch U49 should be set accordingly. Switch 7 of U49 should be set to the appropriate computer type (286 and older or 386 and newer). The Board Configuration dip switch U20 should be set to the user_s specification. The Interrupt Level dip switch U48 should be set to the required IRQ line, if using interrupts.

1553 devices may be connected to the 1553 bus either directly (Direct Coupled) or via a bus coupling stub (Transformer Coupled). Dip switches U30, U51 must be used to inform the card which coupling method is being used for each bus the card is connected to.

Once all the dip switches are set properly, **make certain the computer is turned off** and insert the card into any 8 or 16 bit slot. Once the card is installed, the DB9 to 1553 twinax adapter cables should be attached to the card and to the bus. The cables may be connected and disconnected to the card while power to the computer is turned on but not while the card is transmitting over the bus.

1553 BUS CONNECTIONS

For short distances, direct coupling may be used to connect the EXC-1553PC/E directly to another 1553 device. The user must make certain that the cable connecting the two devices is properly terminated with 78 Ohm resistors to insure data integrity (see illustration).



One Bus Shown

For users wishing to operate in the more standard Transformer Coupling mode, stub coupler devices are available from a number of manufacturers. North Hills Electronics, Inc. supplies a three stub coupler (PN# DB30010) as well as 78 ohm terminators (PN# RT500078). Two terminators are required for each coupler which services a single bus (e.g. BUS A).

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BC OPERATION

In the BC mode, the EXC-1553PC/E can be programmed to transmit multiple messages in either a "one-shot", "N-times" or in a "loop" mode. Errors can be injected into the messages on a message-by-message basis. In addition, the user can pre-program the inter-message gap time of each message.

The user programs the message transfers by loading a [relocatable] stack with instructions. Each instruction block contains four words. Many instruction stacks can be created and reside simultaneously within the dual-port memory. The user simply points to the _active_ instruction stack by programming the Instruction Stack Pointer.

NOTE:

The user should use the following sequence to determine whether the board is installed AND ready to operate:

* Check the Board ID register (test for value = 45 Hex)

* Check Board Status Register (test for Board Ready bit = _1_)

The board is installed and ready when BOTH of these registers contain the correct values (as written above). This sequence should be used after power-on and software reset operations. For Software Reset operations; these values should be set to ZERO by the user immediately prior to writing to the [software] Board Reset Register.

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BC MEMORY MAP

	RESET INTERRUPT REG.	7001 (H)
	BOARD RESET REGISTER	7000 (H)
	▒▒▒▒▒▒▒▒ RESERVED ▒▒▒▒▒▒▒▒	6FFF (H) … 4000 (H)
	BOARD CONFIGURATION REG.	3FFF (H)
	BOARD ID REGISTER	3FFE (H)
	BOARD STATUS REGISTER	3FFD (H)
	START REGISTER	3FFC (H)
	INTERRUPT CONDITION REG.	3FFB (H)
	MESSAGE STATUS REGISTER	3FFA (H)
	reserved	3FF9 (H) … 3FF7 (H)
	LOOP COUNT REGISTER	3FF6 (H)
	BIT COUNT REGISTER	3FF5 (H)
	WORD COUNT REGISTER	3FF4 (H)
	BC RESPONSE TIME REGISTER	3FF3 (H)
**	VARIABLE AMPLITUDE REG	3FF2 (H)
	STACK POINTER - HI	3FF1 (H)
	STACK POINTER - LO	3FF0 (H)
	FRAME TIME - HI	3FEF (H)
	FRAME TIME - LO	3FEE (H)
	FRAME TIME RESOLUTION - HI	3FED (H)
	FRAME TIME RESOLUTION - LO	3FEC (H)
	INSTRUCTION COUNTER	3FEB (H)
	reserved	3FEA (H) … 3E81 (H)
	FIRMWARE REVISION REG.	3E80 (H)
	reserved	… 3400 (H)
	STACK(S) AND MESSAGE BLOCK AREA	33FF (H) … 0000 (H)

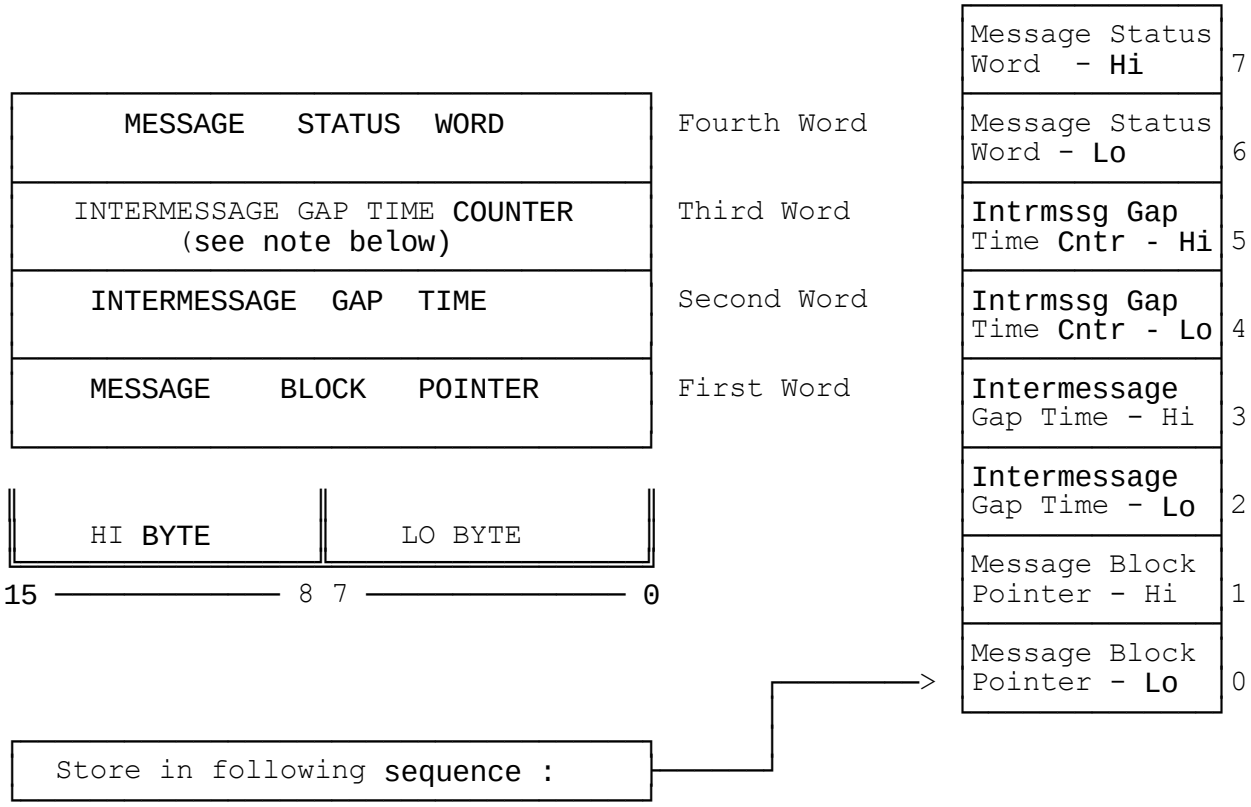
** _-V_ Option

BC Mode

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INSTRUCTION STACK

The user programs the EXC-1553PC/E via the Instruction Stack. The stack is divided into instruction blocks - each containing four words. The figure below illustrates one instruction block.



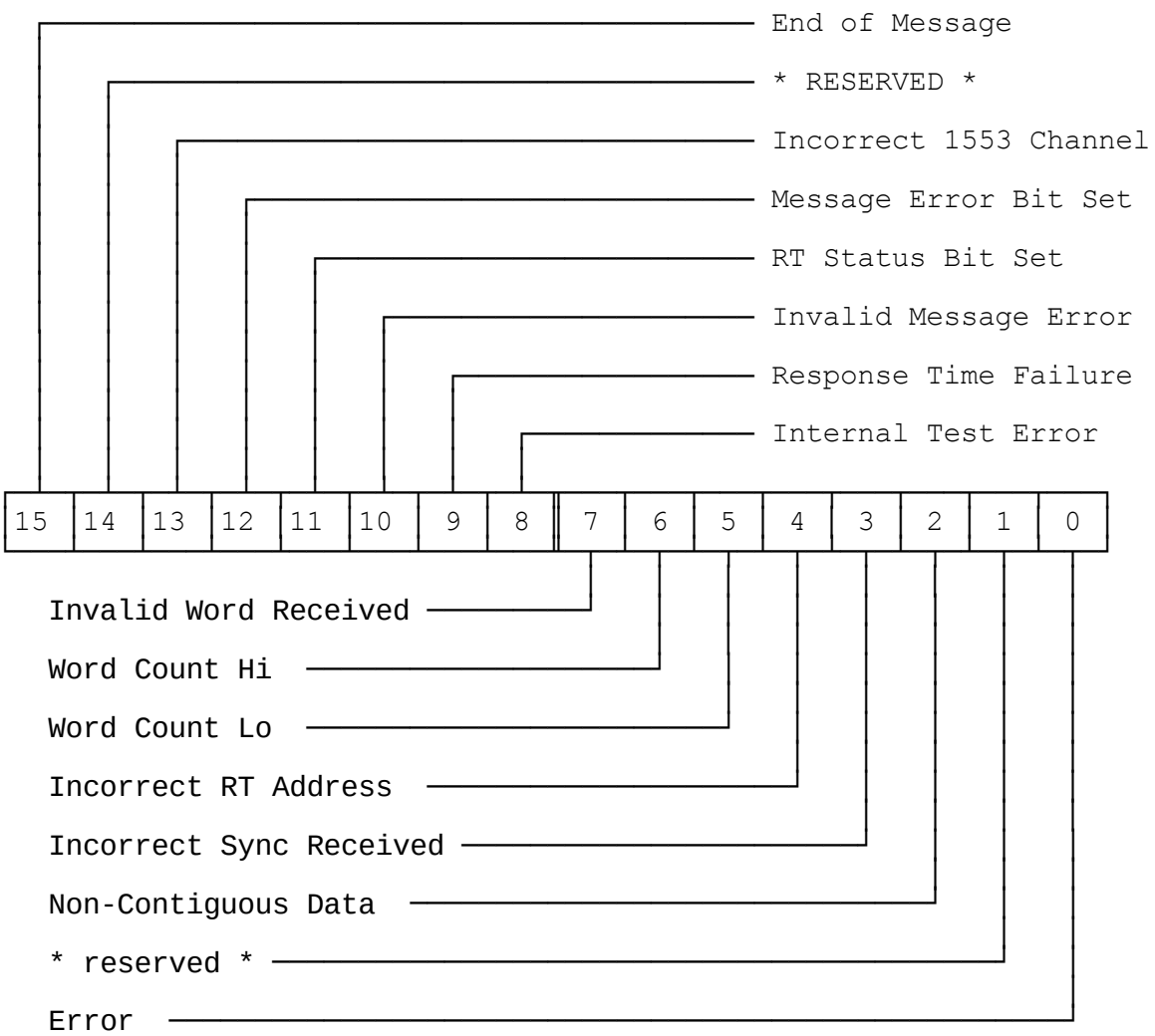
NOTE:

The Intermessage Gap Time Counter, found within EPROM revisions 6.5 and above increases the MAXIMUM intermessage gap time. The counter determines the number of the times that the Intermessage Gap Time value is used (ie If the counter equals "0" then the gap time is per the contents of the Intermessage Gap Time location. If the gap time counter equals "1" then the gap time equals the Intermessage gap time value x 2, etc.

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MESSAGE STATUS WORD	Read by user

The Message Status Word indicates the status of the message transfer. This word is created by the Board and is NOT the 1553 "STATUS WORD".
The format of the Message Status word is shown below:



NOTE: A LOGIC _1_ INDICATES OCCURRENCE OF STATUS FLAG

BC Mode

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Message Status Word Definitions:

15	End of Message	INDICATES THAT THE MESSAGE TRANSFER HAS BEEN COMPLETED
14	Reserved	SET TO LOGIC _0_
13	Incorrect Channel	INDICATES THAT THE REMOTE TERMINAL RESPONSE WAS NOT RECEIVED ON THE ACTIVE 1553 CHANNEL
12	Message Error Bit Set	INDICATES THE _MESSAGE ERROR BIT_ (BIT _10_) WITHIN THE RT STATUS WORD WAS SET
11	RT Status Bit Set	INDICATES THAT A BIT WAS SET WITHIN THE RT STATUS WORD (OTHER THAN THE _MESSAGE ERROR BIT_). The ERROR bit is NOT set in conjunction with this bit.
10	Invalid Message	INDICATES THAT A 1553 _MESSAGE LEVEL_ ERROR OCCURRED (i.e. Word Count, Incorrect Sync) - detailed below
09	Response Time Error	INDICATES THAT THE RT RESPONDED LATE (See: PROGRAMMABLE BC RESPONSE TIME REGISTER)
08	Internal Test Error	INDICATES THAT THE CARD FAILED ITS INTERNAL SELF-TEST PROCEDURE
07	Invalid Word	INDICATES THE RECEPTION OF AT LEAST ONE INVALID 1553 WORD (i.e. Bit Count, Manchester code, Parity)
06	Word Ct Hi	INDICATES THAT THE RT TRANSMITTED TOO MANY WORDS
05	Word Ct Lo	INDICATES THAT THE RT TRANSMITTED TOO FEW WORDS
04	Incorrect RT Address	INDICATES THAT THE RECEIVED 1553 STATUS WORD DID NOT CONTAIN THE CORRECT _RT ADDRESS_
03	Incorrect Sync	INDICATES THAT THE SYNC OF EITHER THE STATUS OR DATA WORD(s) WAS INCORRECT
02	Non-Contiguous	INDICATES OCCURRENCE OF AN INVALID GAP BETWEEN RECEIVED 1553 WORDS
01	Reserved	SET TO LOGIC _0_
00	ERROR	INDICATES THE OCCURRENCE OF AN ERROR (DEFINED WITHIN ONE OF THE OTHER MESSAGE STATUS BIT LOCATIONS)

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Intermessage Gap Time Written by user

The Intermessage Gap Time Value is a sixteen bit word which allows the user to insert a unique intermessage delay time between the current message and the next message. The minimum Intermessage Gap Time is approximately 120 µsec. If the Gap Time value written is less than 120µsec, the board will transmit the message with the minimum delay. The resolution of this word is: 155 nsec. per bit.

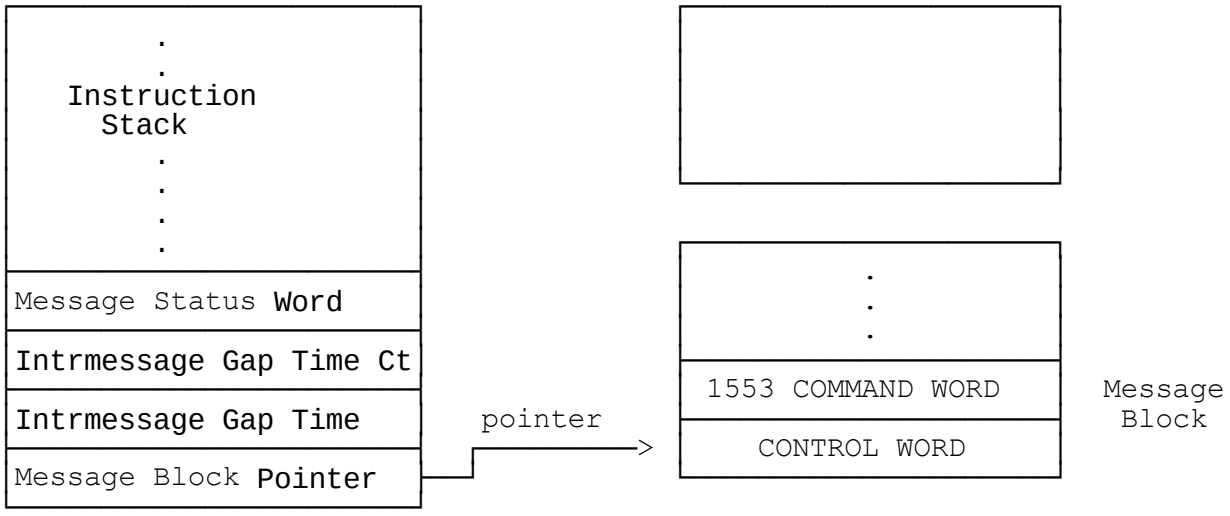
Intermessage Gap Time Counter Written by user

The Intermessage Gap Time Counter (IGT_Counter) is a sixteen bit word which allows the user to increase the Intermessage Gap Time by repeating the number of times the Intermessage Gap Time Value is used. If the counter equals "0", for example, then the gap time is NOT repeated and is per the contents of the Intermessage Gap Time location. If the gap time counter equals "1" then the gap time is repeated once and equals the Intermessage gap time value x 2, etc.

* Notes: 1) This feature is available within the EPROM revision 6.5 and above.
2) To ensure maximum intermessage gap time accuracy when using the IGT_Counter, the value within the Intermessage Gap Time Word should be maximized and that within the IGT_Counter minimized, for a given desired intermessage gap time.

Message Block Pointer Written by user

The Message Block Pointer is a sixteen bit word which points to the beginning of a 1553 Message Block.



BC Mode

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The user loads the Message Block anywhere within the Instruction STACK/MESSAGE BLOCK AREA (see: BC Memory Map). Message Blocks do NOT have to be stored in sequential locations within the memory since the Message Block Pointers "point" to the Message Blocks in sequence.

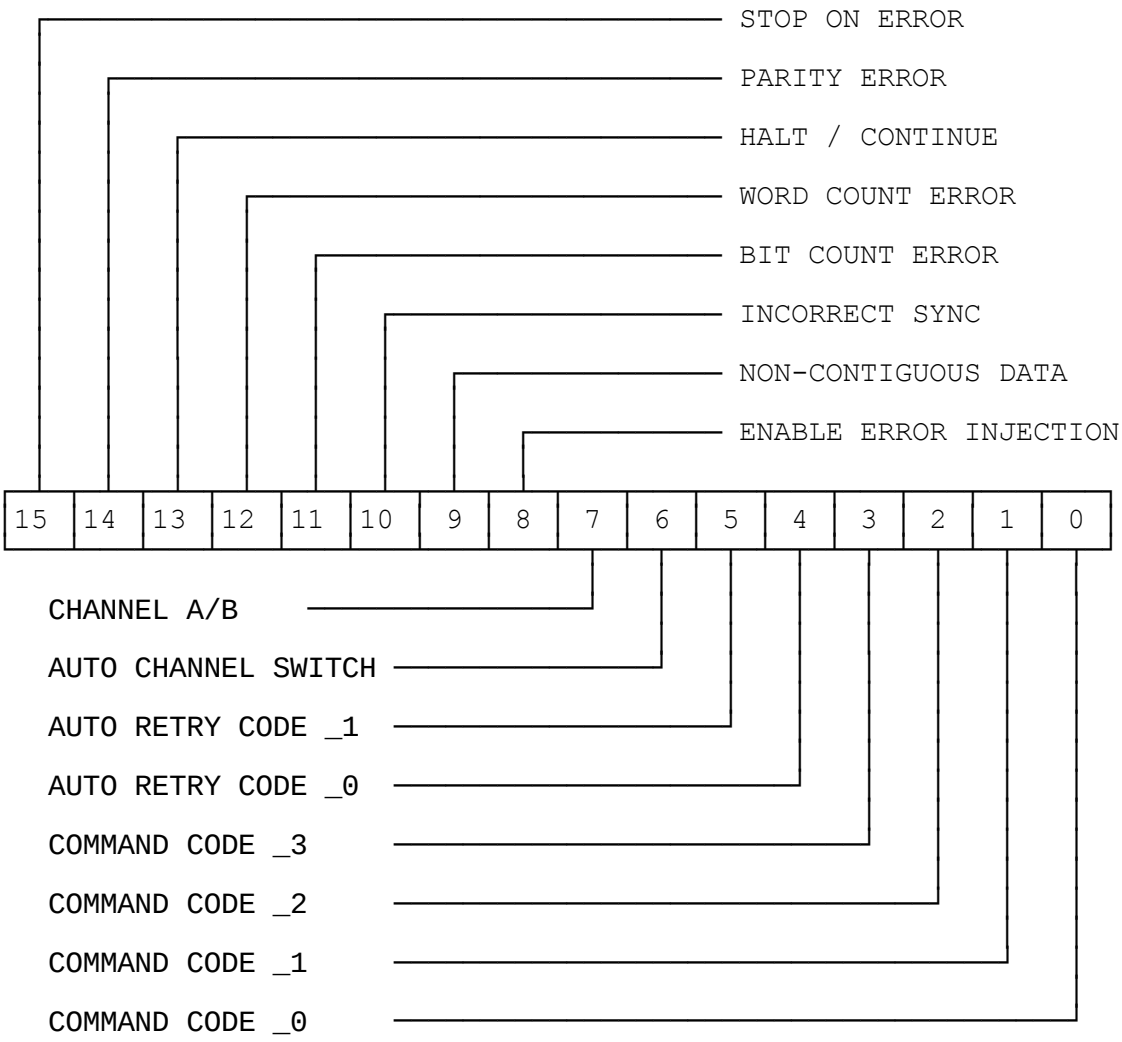
Each block contains a 1553 message plus its Control Word. This Control Word is written into the FIRST word of each block. The Control Word instructs the EXC-1553PC/E as to the type of message to be transmitted (i.e. RT to RT, Mode Code, Broadcast, Error injection, etc.). The size of the message block is not fixed and is dependent upon the size of the message itself.

The description of the various message block formats (ie BC to RT, RT to BC and RT to RT) are illustrated in the section titled "Message Block Formats".

The description of each bit within the Control Word follows.

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Control Word



NOTE : A LOGIC _1_ ENABLES THE FUNCTION, A _0_ DISABLES THE FUNCTION

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Control Word Definitions:

15	Stop on Error	MESSAGE ERROR STOPS THE BC OPERATION. THE USER CAN RESTART BY WRITING TO THE INSTRUCTION COUNT AND "START
14	Parity Er	SELECTS _EVEN_ PARITY WITHIN 1553 WORDS
13	Halt / Continue	1=HALT. This stops BC transfer operation. This bit MUST BE reset (_0_) in order to RUN or CONTINUE (see text)
12	Wd Count Error	TRANSMITS LESS or MORE WORDS THAN ARE INSTRUCTED BY THE WORD COUNT FIELD (see: Word Count Register) THIS FUNCTION IS VALID FOR _BC_ to _RT_ messages only.
11	Bit Count Error	TRANSMITS INVALID NUMBER OF BITS WITHIN 1553 WORDS (see: Bit Count Register)
10	Incorrect Sync	TRANSMITS INCORRECT SYNC . DATA-TYPE SYNC IS TRANSMITTED WITHIN THE COMMAND WORD
09	Non-Contg Data	FIRST 1553 DATA WORD IS TRANSMITTED WITH INVALID GAP TIME (BETWEEN COMMAND AND DATA WORD)
08	En.Error Injection	ENABLES THE ERROR INJECTION CAPABILITY WITHIN THE MESSAGE (MUST be SET in addition to actual Error)
07	CHANNEL A / B	SELECTS ACTIVE 1553 CHANNEL. LOGIC _1_ SELECTS CHANNEL _A_ WHILE A LOGIC _0_ SELECTS CHANNEL _B_
06	Auto Chnl Switch	ON ERROR, THE BC WILL RETRY MESSAGE TRANSFER ON ALTERNATE CHANNEL (* AUTO-RETRY MUST BE SELECTED *)
05-04	Auto Rtry Code	ON ERROR, SELECTS THE NUMBER OF RETRIES BEFORE TRANSFER OF NEXT MESSAGE Code _1 _0 0 0 **0 -No Retry** 0 1 1 - 1 Retry 1 0 2 - 2 Retry 1 1 **1 - 3 Retry**
03-00	COMMAND CODE	0000 - **TRANSMIT COMMAND (RT to BC)** 0001 - RECEIVE COMMAND (BC to RT) 0010 - RT to RT COMMAND 0011 - MODE CODE 0100 - BROADCAST RECEIVE COMMAND 0101 - BROADCAST RT to RT COMMAND 0110 - BROADCAST MODE CODE 0111 - SKIP MESSAGE (see text) 1000 - JUMP COMMAND (see text)

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HALT Operation

The user normally sets this bit to a logic _0_ before writing to the Start Register. The user may, in real-time (during BC execution), set this bit (to a logic_1_). The board, when operating on that particular Message Block_s Control Word, will HALT transfer operations until the bit is reset to a logic _0_.

When the board detects that the HALT bit is set, it sets the "WAIT FOR CONTINUE" bit within the Message Status Register (see: Control Register Section). This bit can be used by the user in order to know when the board has arrived at this Instruction block. When the board detects that the Halt bit has been reset by the user(continue mode), the board will then reset the "WAIT FOR CONTINUE" bit within the Message Status Register and continue BC operation.

It is important to note that this function can only be implemented within Message Blocks which have NOT [AS YET] BEEN EXECUTED BY THE BOARD.

Note: This operation can be used in conjunction with the JUMP feature described below.

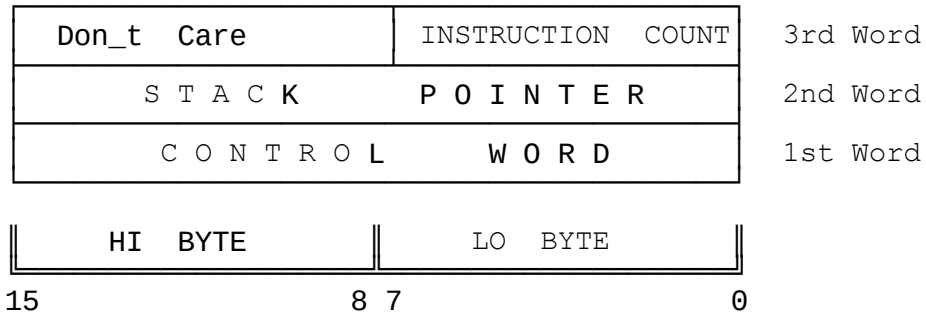
SKIP Message Operation (EPROM Rev 6.5 & above)

The SKIP MESSAGE command allows the user to easily skip a message defined in a certain Message Block by only modifying the Command field within the Control Word. This allows the user to selectively send a message within the current frame. The Intermessage Gap Time associated with the SKIP Message has no effect.

JUMP Command Operation

The EXC-1553PC/E allows the user to modify the BC transfer cycle by setting the "JUMP" command within the Control Word. The Jump command instructs the board to operate on a New instruction stack or New stack entry within the same stack. This Control word is followed by a Stack Pointer word instead of the usual 1553 Command Word. In addition, the Stack Pointer is followed by an Instruction Count value. The Jump command is tested AFTER the board has tested the HALT/CONTINUE bit within the Control Word. The Intermessage Gap Time associated with the JUMP command has no effect.

The memory location sequence is illustrated below:



BC Mode

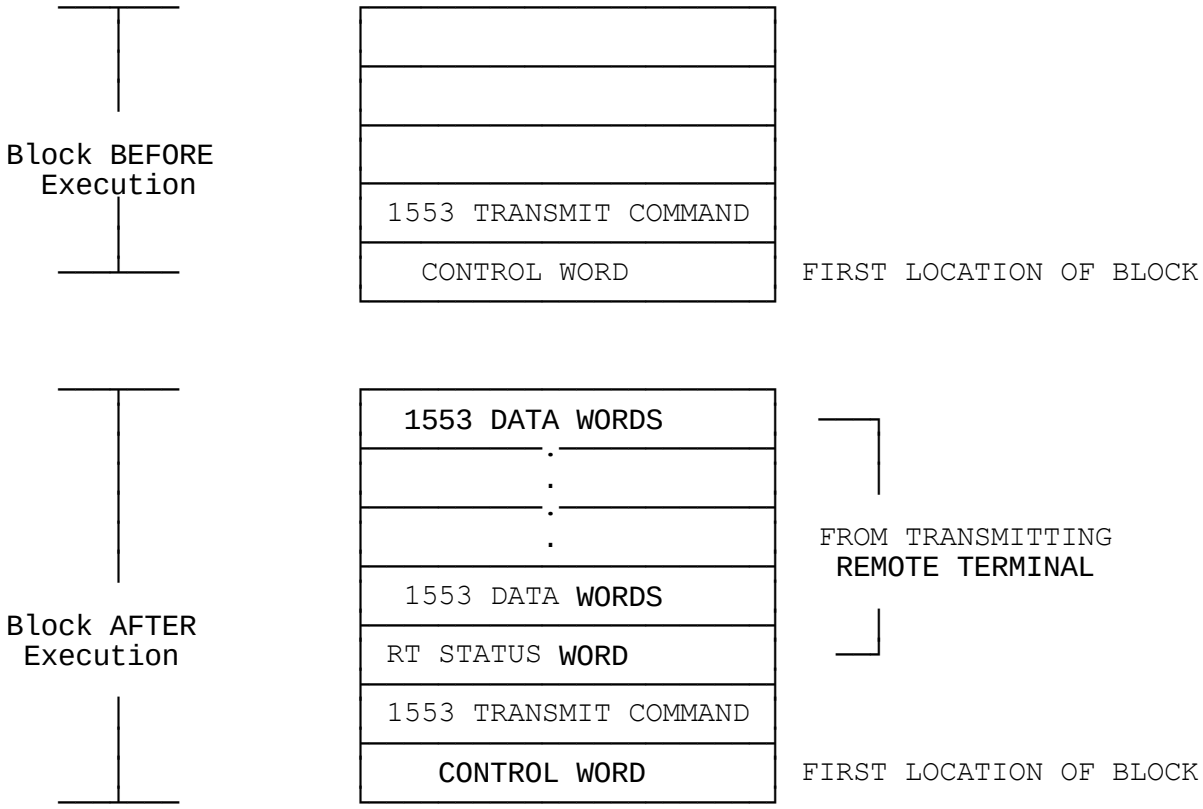
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MESSAGE BLOCK FORMATS

The Message Block contains, or Will contain following RT response, the entire 1553 message as it appears on the 1553 bus - including Command Word(s), Data Words, and Status Word(s).

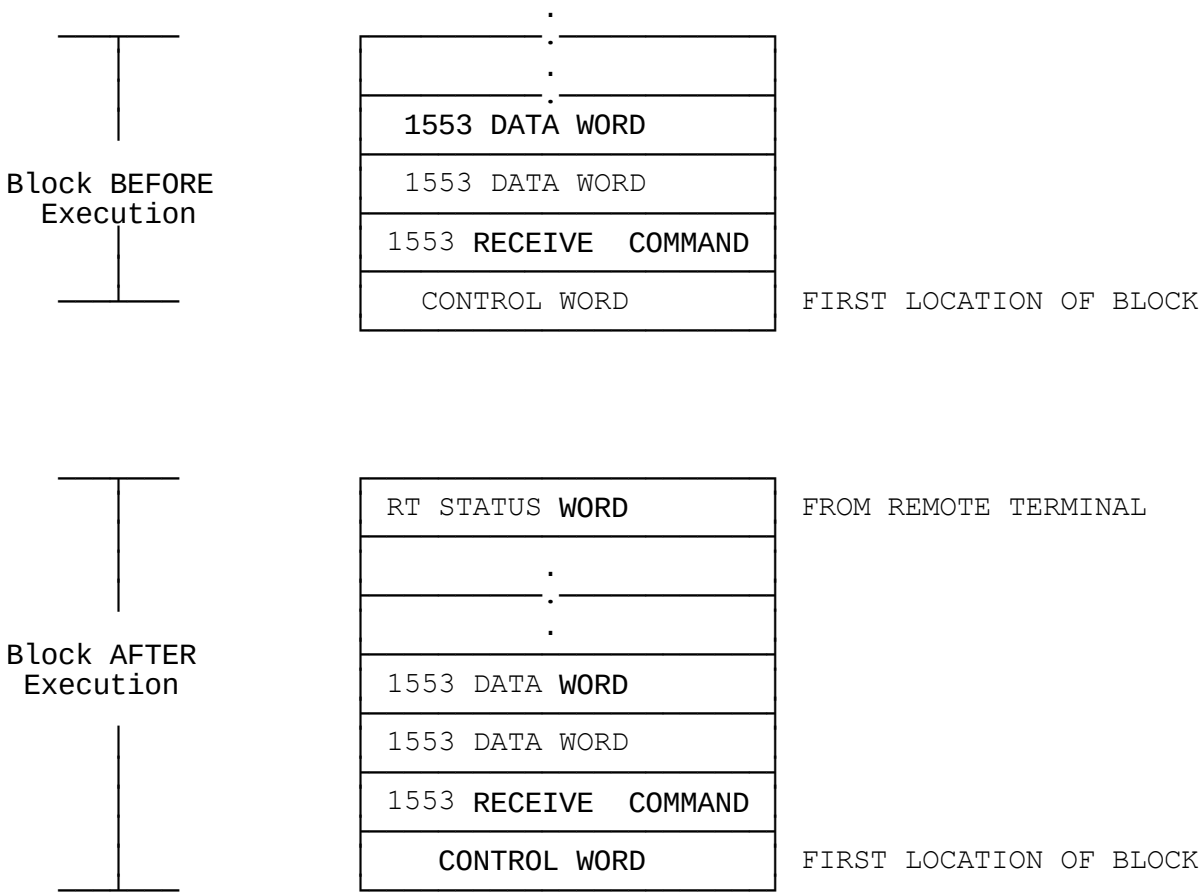
Examples #1

TRANSMIT COMMAND



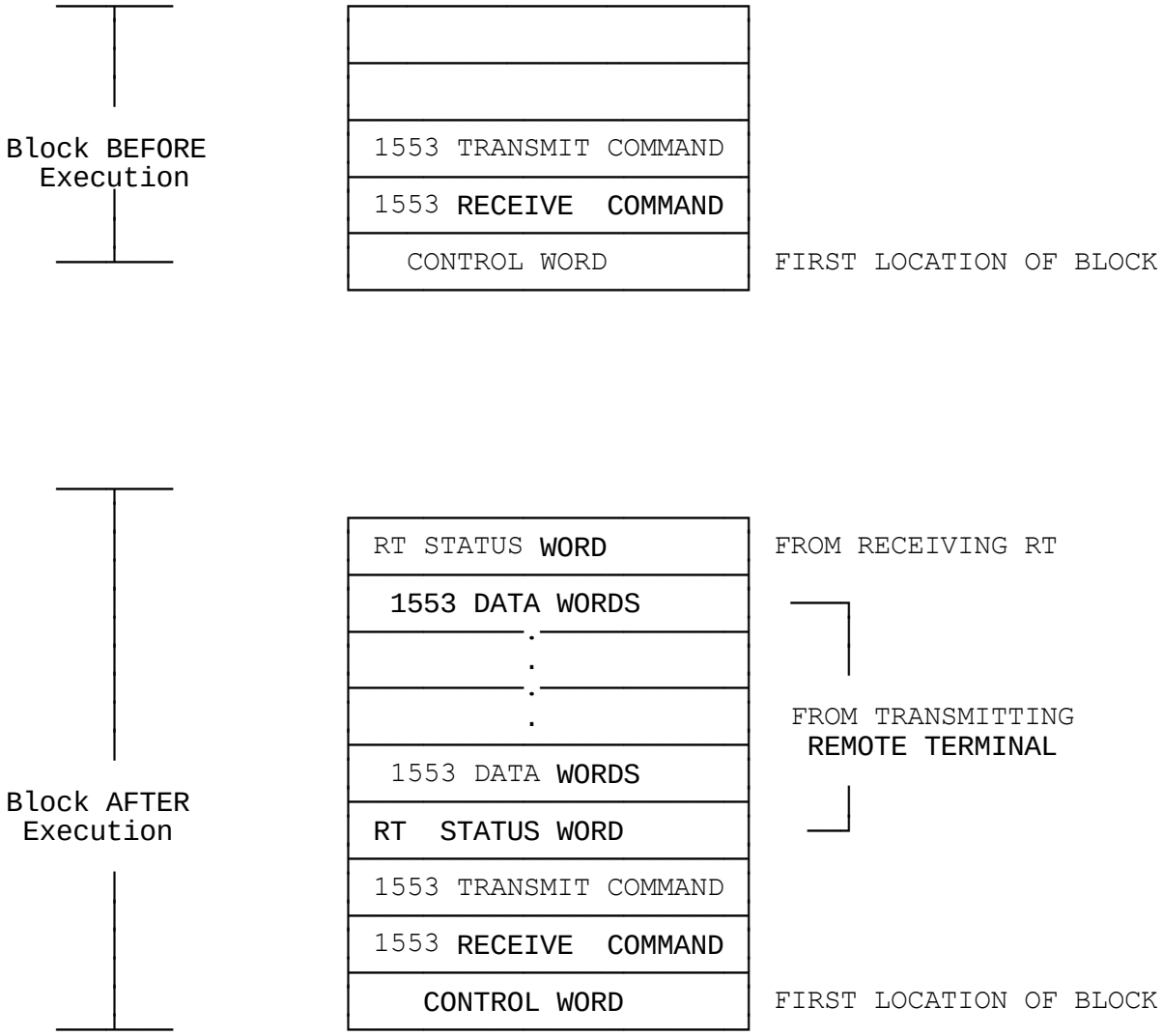
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Examples | #2 | RECEIVE COMMAND



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Examples | #3 | RT to RT COMMAND



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CONTINUOUS or ONE-SHOT MESSAGE TRANSFERS

The EXC-1553PC/E offers the capability of transferring all programmed messages once, for _N_ times or in a continuous loop which can be halted under software control.

In the One-Shot mode, the board transfers all messages [after receipt of a "START" command], sets the Message Complete Bit within the Message Status Register, issues an Interrupt [if programmed] and waits for a new "START". This mode is selected via the Start Register (see Start Register definition).

In the _N_ Times Mode, the user loads the Loop Count Register with the number of times to TRANSMIT the message frame and sets the LOOP and START bits within the Start Register. The user can select to transmit from one to 255 times (see Loop Count and Start Registers). The time between frames is predetermined via Frame Time Register (see below).

In the Continuous mode, the EXC-1553PC/E will re-transmit the message frame at a predetermined, user-programmable rate. This mode is selected via the Start Register and the Loop Count Register (see Register definitions). In this mode, all messages relating to the [active] Stack Pointer and Instruction Counter are continuously "looped" until the user halts the board_s operation (see Start Register definition).

The "loop" time or Frame Time is a function of two Control register pairs; the Frame Time Registers (Hi and Lo) and the Frame Time Resolution Registers (Hi and Lo). The internal Frame Time counter is loaded upon receipt of a "START" command with the 16-bit value found within the Frame Time Registers (Hi and Lo). The Frame Time counter is decremented every N x 155 nsec. - where N is the value of Frame Time Resolution Registers (Hi and Lo). After the execution of all instructions (1 frame), the EXC-1553PC/E will wait until the internal Frame Time Counter reaches ZERO before re-transmitting the next frame.

NOTE: If the Frame time is less than the time required to transmit all messages [within 1 frame], the subsequent frames will be transmitted with the minimum delay between them. The minimum delay is 120µsec approximately measured as dead time on the bus.

The user can implement the desired Frame time by programming the appropriate combinations of the two register pairs. An example using one method is illustrated below.

BC Mode

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EXAMPLE: FRAME TIME CALCULATION

Given: User requires a Frame Time of 500msec.

Operation:

Select Frame Time Resolution of 3225 (Dec) ----- 0C99(H).
Frame Time Resolution = 3225 x 155 nsec. = 500 µsec (.5 msec)

Subsequently; the Frame Time Register value must equal to :
(500 msec (desired time) / .5 msec = 1000 (Dec))-1 --> 03E7(H)
Count-1

Load Frame Time Register Lo = E7 (H)		(before "START")
Load Frame Time Register Hi = 03		(" ")
Load Frame Time Resolution Register Lo	= 99 (Hex)	(" ")
Load Frame Time Resolution Register Hi	= 0C	(before "START")

Note: It is recommanded that the user maximize the Resolution Register value vis-a-vis the Frame Time Register value to achieve the greatest possible precision.

MODE CODES

The EXC-1553PC/E handles all Dual-Redundant 1553B Mode Codes. This is to say that the Word Count field is decoded according to MIL-STD-1553B. The two quad-redundant mode codes, "Selected Transmitter Shutdown" and "Override Selected Transmitter Shutdown" are not implemented by the board.

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PROGRAM EXAMPLE BC MODE

note: ALL values are in HEX unless stated

```
10 POKE &H3FFF,01      _ LOAD CONFIGURATION REG. = BC MODE
20 POKE &H3FF0,00      _ LOAD STACK POINTER REGISTERS WITH "0000"
30 POKE &H3FF1,00      _ (STACK NOW BEGINS AT ADDRESS:0000)
40 POKE &H3FF2,xx      _ LOAD VARIABLE AMPLITUDE REGISTER (_-V_ OPTION)
35 POKE &H3FF3,xx      _ LOAD BC RESPONSE TIME-OUT REGISTER

40 POKE &H00,00        _ POINTER TO FIRST MESSAGE. LOCATION OF MESSAGE
50 POKE &H01,01        _ IS 0100(H)
60 POKE &H02,xx        _ LOAD INTERMESSAGE GAP TIME LOCATION
70 POKE &H03,xx        _

80 POKE &H08,&H40      _ POINTER TO SECOND MESSAGE. LOCATION OF MESSAGE
90 POKE &H09,01        _ IS 0140(H)
100 POKE &H0A,xx       _ LOAD INTERMESSAGE GAP TIME LOCATION
110 POKE &H0B,xx       _

120 POKE &H100,&H80   _ LOAD CONTROL WORD WITH: TX COMMAND, BUS A,
130 POKE &H101,00     _ AND NO ERRORS INJECTED
140 POKE &H102,&H23   _ LOAD COMMAND WORD: 0C23
150 POKE &H103,&H0C   _

160 POKE &H140,02     _ LOAD CONTROL WORD WITH: RT to RT COMMAND, BUS B,
170 POKE &H141,00     _ AND NO ERRORS INJECTED
190 POKE &H142,&H23   _ LOAD  FIRST [RECEIVE] COMMAND WORD: 0823
200 POKE &H143,08     _
210 POKE &H144,&H43   _ LOAD SECOND [TRANSMIT] COMMAND WORD: 0C43
220 POKE &H145,&H0C

230 POKE &H3FEB,2      _ LOAD INSTRUCTION COUNTER WITH "2" (2 MESSAGES)
240 POKE &H3FEE,xx     _ LOAD FRAME TIME REGISTERS
245 POKE &H3FEF,xx     _
250 POKE &H3FEC,xx     _ LOAD FRAME TIME RESOLUTION REGISTERS
255 POKE &H3FED,xx     _
260 POKE &H3FF6,4      _ LOAD LOOP COUNT REGISTER WITH "4" (TRANSMIT
                       _ THESE TWO MESSAGES 4 TIMES AND STOP)
270 POKE &H3FFC,5      _ LOAD START REGISTER WITH "5". STARTS MESSAGE
                       _ TRANSFERS IN LOOP MODE.

280 STOP
```


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CONTROL REGISTER DEFINITIONS

RESET INTERRUPT REGISTER 7001(H)

Writing to this register will reset the Interrupt signal to the computer. The Data field is ignored. This register should be written to at the beginning of a user-written, interrupt service routine.

BOARD RESET REGISTER 7000(H)

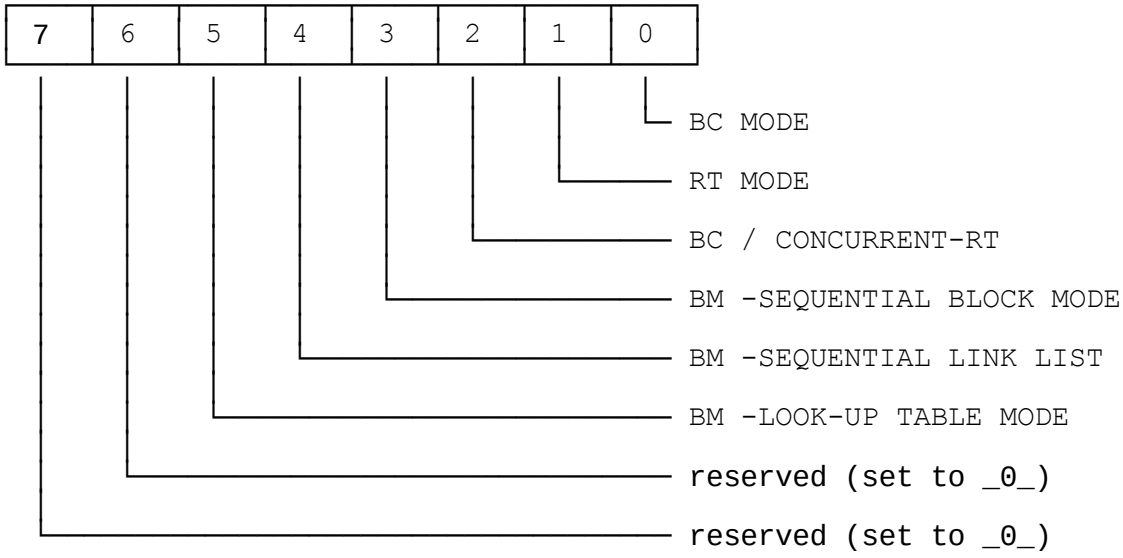
Writing to this location will RESET the EXC-1553PC/E board. The board will act as if POWER had been switched off then on. The data field is ignored.
NOTE: _RESET_ ERASES ALL MEMORY LOCATIONS WITHIN THE DUAL-PORT RAM !!! The Board Status, the Board ID, Firmware Revision and Variable Amplitude registers are written by the board after the reset operation has been completed.

(example: POKE &H7000,xx)

BOARD CONFIGURATION REGISTER 3FFF(H)

Set the desired bit to a logic _1_

The operating mode of the board is set via this register. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).



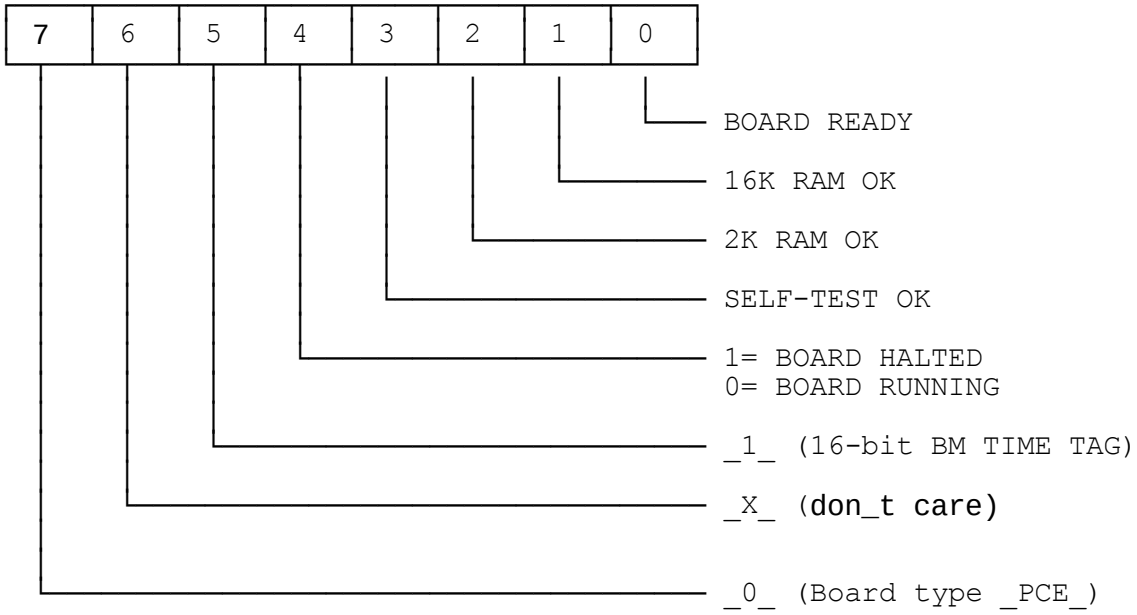
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BOARD ID REGISTER 3FFE(H)

This register contains a fixed value which can be read by a user_s initialization routine to detect the presence of the EXC-1553PC/E card.
The one-byte value of this register is: 45 (Hex) ; ASCII _E_.

BOARD STATUS REGISTER 3FFD(H)

This register indicates the status of the EXC-1553PC/E card. In addition, this register indicates option selection as defined below. (Status bits are active _1_). This register should not be modified by the user.

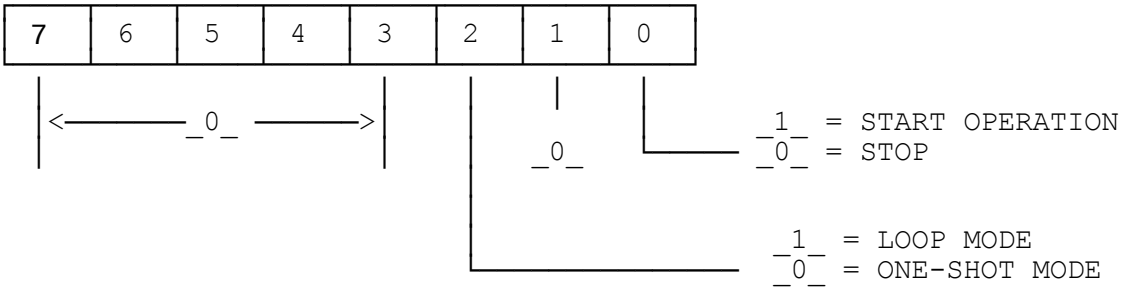


NOTE: Bit "04" (Board Halted) is set by the board after the user "stops" the current operation (by resetting the START bit within the Start Register). The user must check this bit first before modifying registers which first require a "STOP" operation. The board resets this bit after receiving a subsequent START command (by writing to the Start Register). This bit is a new feature available within EPROM revisions starting with 6.5. The condition of this bit after power-on or software reset is a logic "1".

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START REGISTER 3FFC(H)

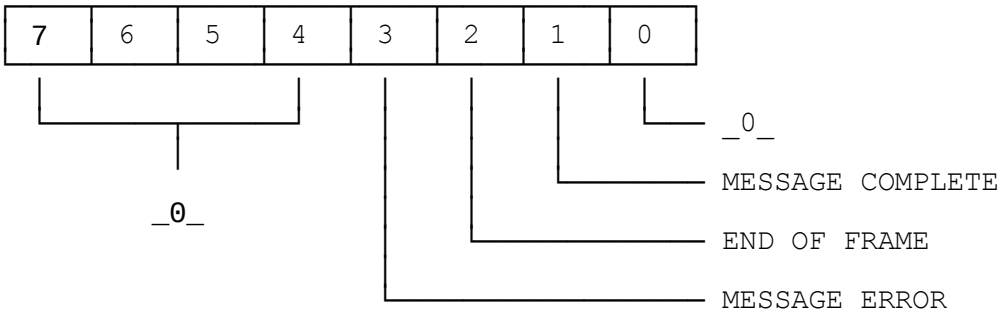
This register controls the _START/STOP_ operation of the EXC-1553PC/E. Writing to this register with the appropriate bit set begins the Bus Controller transfer operation. When operating in the "Loop" or "N Times" mode, the user must set the Start and Loop bits within this register. The "loop" and "N-times" number is selected via the Loop Count Register. In the One-Shot and "N-Times" modes, the board RESETS the Start bit within the register after ALL messages have been transferred. The board does not reset any bit while in the Continuous loop mode. Write "0" to bit "00" to halt the LOOP operation between messages. Write, instead, a "0" to bit "02" in order to halt the operation at the end of the entire frame (this bit is not tested between message transfers). See the related bit (data bit "04") within the Board Status Register which indicates when the board has been halted.



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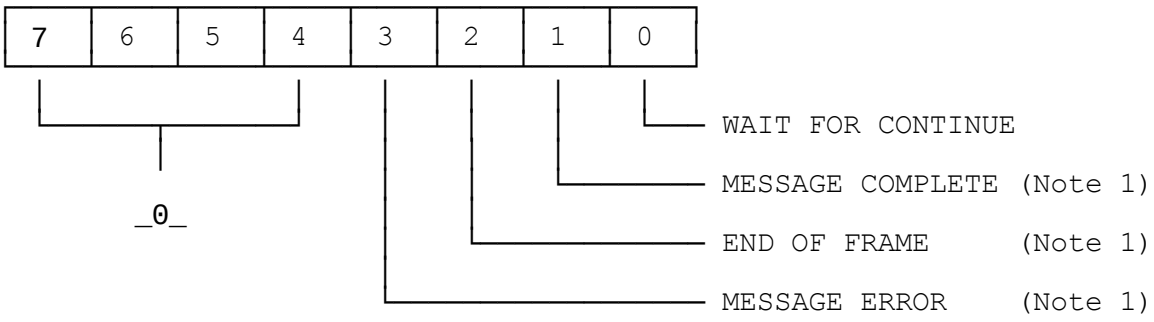
INTERRUPT CONDITION REGISTER 3FFB(H)

This register allows the user to set different interrupt triggers. When a condition that has been enabled within this register occurs, an interrupt will be generated. The user may check the Message Status Register to determine which condition caused the interrupt. A logic _1_ enables the interrupt condition. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).



MESSAGE STATUS REGISTER 3FFA(H)

This register indicates the status of the EXC-1553PC/E card. The figure below illustrates the definition of each Status bit. A logic _1_ indicates active condition.



WAIT FOR CONTINUE - A message with the halt bit set has been encountered. The user must reset the the halt bit in the Control word to continue.

MESSAGE COMPLETE - The last word of a message has been sent.

END OF FRAME - The last word of the last message in a frame has been sent.

MESSAGE ERROR - A message has been sent resulting in the error bit being set in Message Status Word.

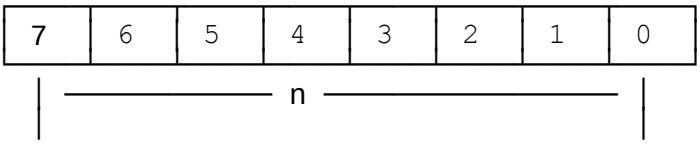
Note: 1) Status bits are NOT reset by the board and should be reset by the user after reading them.

BC Mode

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LOOP COUNT REGISTER 3FF6(H)

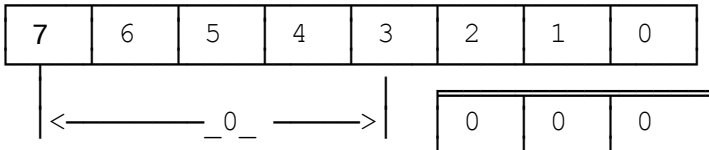
This register is used in conjunction with the Loop Bit in the Start Register. If that bit is set, the user sets this register to specifiy the number of times the Message Frame will be tranmsitted. A value of zero is interpreted as a request for continuous looping.
This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).



Value = 0 : Transmits in continuous loop
Value = 1-255 : Sends message frame _n_ times (1 to 255) as defined

BIT COUNT REGISTER 3FF5(H)

Sets the number of total bit times within the 1553 word ; including Sync(3) and Parity(1). When NO error is selected (see: Control Word), this register is ignored (20-bit word is selected). This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).



7	6	5	# of bits	
0	0	0	17	-3
0	0	1	18	-2
0	1	0	19	-1
0	1	1	20	
1	0	0	21	+1
1	0	1	22	+2
1	1	0	23	+3

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WORD COUNT REGISTER 3FF4(H)

This register controls the number of 1553 words (+/- 3) within the message. The variation is relative to the 1553 Command Word_s WORD COUNT FIELD. The "resulting" message must contain at least ONE 1553 Data Word. When NO error is selected (see: Control Word), this register is ignored. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

7	6	5	4	3	2	1	0

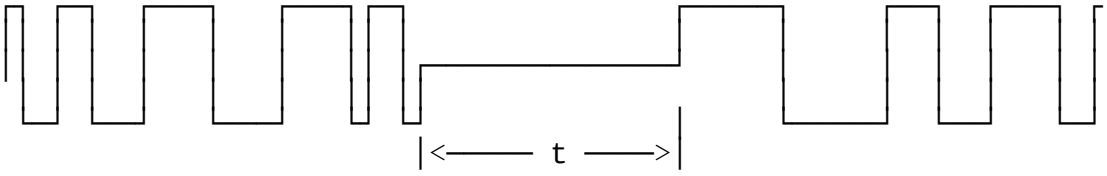
|<———— see table ————>|

(No Word Count Error injected) -

-3	FD (H)
-2	FE (H)
-1	FF (H)
0	00 (H)
+1	01 (H)
+2	02 (H)
+3	03 (H)

BC RESPONSE TIME REGISTER 3FF3(H)

This register sets the Bus Controller_s RESPONSE TIME WINDOW. This value determines the maximum [wait] time until an RT_s Status Response is considered "INVALID" by the BC. The resolution of this register is 155 nsec. per bit. This time is measured as the "DEAD TIME" on the 1553 bus. The minimum time is approx. 2 µsec. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).



Example: To set up a BC response time of 14µsec, write a 90 to this register: 90 * 0.155 = ~14µsec.

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VARIABLE AMPLITUDE REGISTER 3FF2(H) (_-V_ Option)

This register specifies the amplitude of the 1553 output signal. The signal can be programmed from 0 volts up to 7.5volts (p-p) - measured on the 1553 bus with specified 1553 coupling and 35ohm load (two 70 ohm termination resistors were used). A higher Transmit [output] amplitude will appear on the 1553 bus if 78 ohm termination resistors are used. The register has a resolution of 30mv/bit (p-p) on the bus. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register). For EPROM Revisions 6.5 and above this register defaults to FFH after Reset, providing maximum amplitude.

STACK POINTER - HI & LO 3FF1, 3FF0(H)

The Stack Pointer points to the Instruction Stack. The Instruction Stack can reside anywhere within locations 0000(H) and 33FF(H). This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

FRAME TIME REGISTERS - HI & LO 3FEF, 3FEE(H)

These registers contain the 16-bit Frame Time Value for Continuous and N-times Modes Operation. The value written to this register is multiplied by the value set within the Frame Time Resolution Registers pair described below. The value set must be equal to the desired multiplication factor - 1. See: CONTINUOUS or ONE-SHOT MESSAGE TRANSFERS described above. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

FRAME TIME RESOLUTION REGISTER - HI & LO 3FED, 3FEC(H)

This 16-bit value represents the resolution of the Frame Time Counter in increments of 155 nsec. See CONTINUOUS or ONE-SHOT MESSAGE TRANSFERS described above. The _HI_ register contains the MSB , the _LO_ register contains the LSB. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

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INSTRUCTION COUNTER	3FEB(H)

The Instruction Counter is loaded with the number of instructions (1553 Messages) to execute in the current frame. The value must be greater than _0_ before beginning transmission (by writing to the _START REGISTER_). Load _1_ for one message, _2_ for two messages, etc. The EXC-1553PC/E updates this register by decrementing the value and writing it back to the memory. This register must be set before issuing a START to the board. This register is decremented and updated by the board at the end of each message transfer. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register). When in the "loop mode", this register cycles from the initial value to "0" for the first frame. Subsequent frames have this register cycle from the "initial value-1" down to "0" instead of from the initial value.

FIRMWARE REVISION REGISTER	3E80(H)

This register indicates the revision level of the on-board firmware. The value 0110 0011 would be read as revision level: 6.3

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RT OPERATION

The EXC-1553PC/E can be configured to simulate up to 32 Remote Terminals. The user selects which terminal(s) are operating ["ACTIVE"]. The EXC-1553PC/E handles all message transfers subsequent to receiving a "START" command (see Control Registers). In addition, errors can be injected into the message responses. The RT data transfers operates via a 2Kx8 Look Up Table which points to one of 200 data blocks. The user loads the 1553 data blocks with transmit data and reads the received 1553 data from the pre-assigned blocks.

The EXC-1553PC/E can operate within various 1553 environments since most 1553 parameters such as Response Time, Status Word content,etc. are user-programmable. The EXC-1553PC/E also allows the user to enable or disable the 1553 BROADCAST function - reserving RT address 31 (11111) or utilizing all 32 RT addresses by disallowing Broadcast Commands (see DIP SWITCH Settings).

The user can specify whether or not the Remote Terminal should transmit its 1553 Status Word at the end of a message even if INVALID DATA WORDS [only "invalid" - as specified by 1553] were received within the message. This feature is selected via the Status Response Register (see: Control Registers).

The user can program the 1553 Mode Code Subaddress Identifier (see Mode Code Control Register) so that either _11111_, _00000_, or both , can be used to indicate that the 1553 Command Word is a Mode Code.

The ["PCE"] Remote Terminal transmits its 1553 Status Word in approximately 7µsec. (measured as: "dead time on the bus"); a value which can be INCREASED via the RT Response Time Register. A "FAST" adapter board is available which reduces the minimum time to approximately 4usec. This adapter is free of charge (consult factory).

The board will respond properly to messages received with an intermessage gap of greater than 15µsec measured as dead time on the bus. In addition the minimum intermessage gap time between a broadcast message and the subsequent 1553 command is 35µsec.

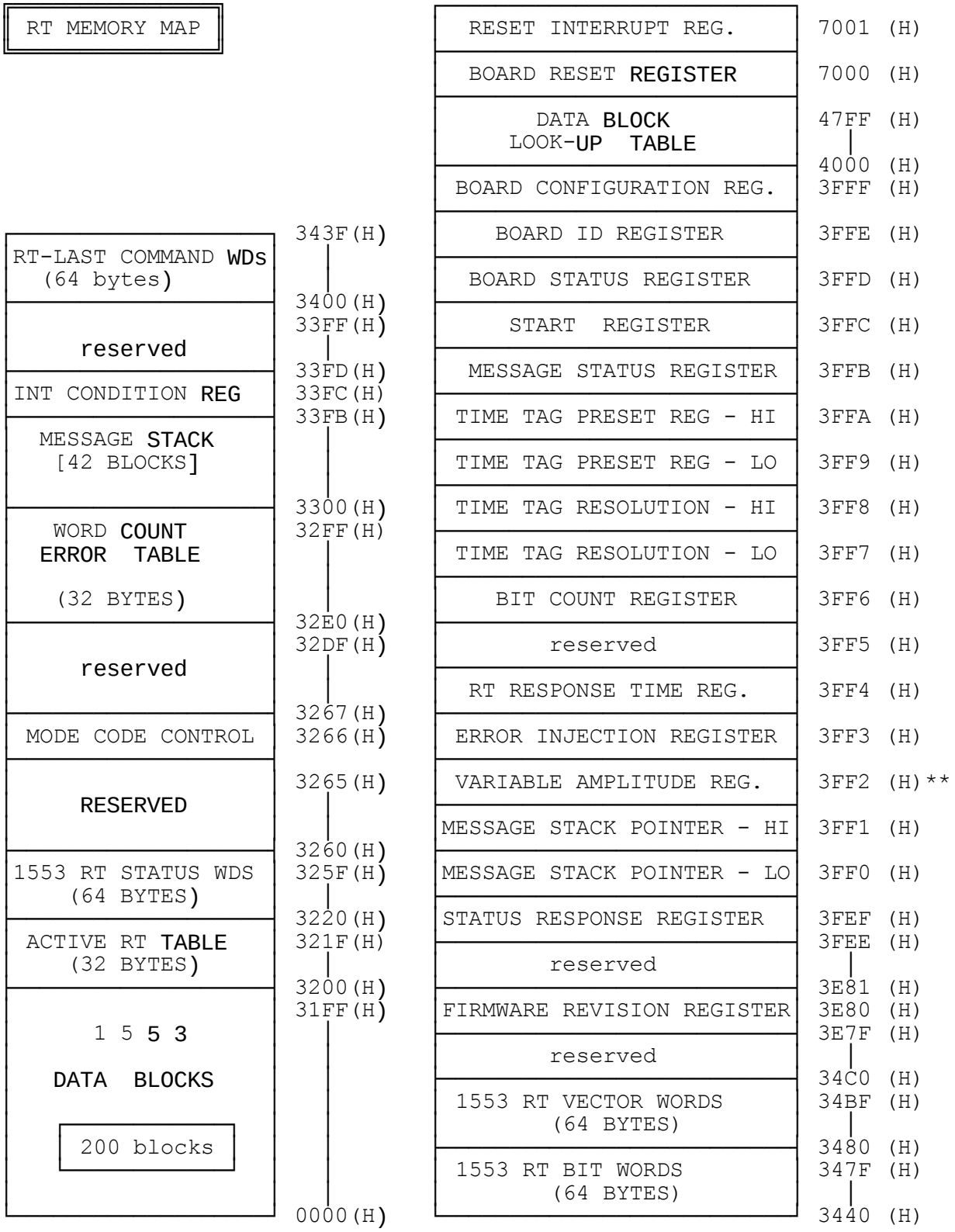
NOTE:

The user should use the following sequence to determine whether the board is installed AND ready to operate:

* Check the Board ID register (test for value = 45 Hex)
* Check Board Status Register (test for Board Ready bit = _1_)

The board is installed and ready when BOTH of these registers contain the correct values (as written above). This sequence should be used after power-on and software reset operations. For Software Reset operations; these values should be set to ZERO by the user immediately prior to writing to the [software] Board Reset Register.

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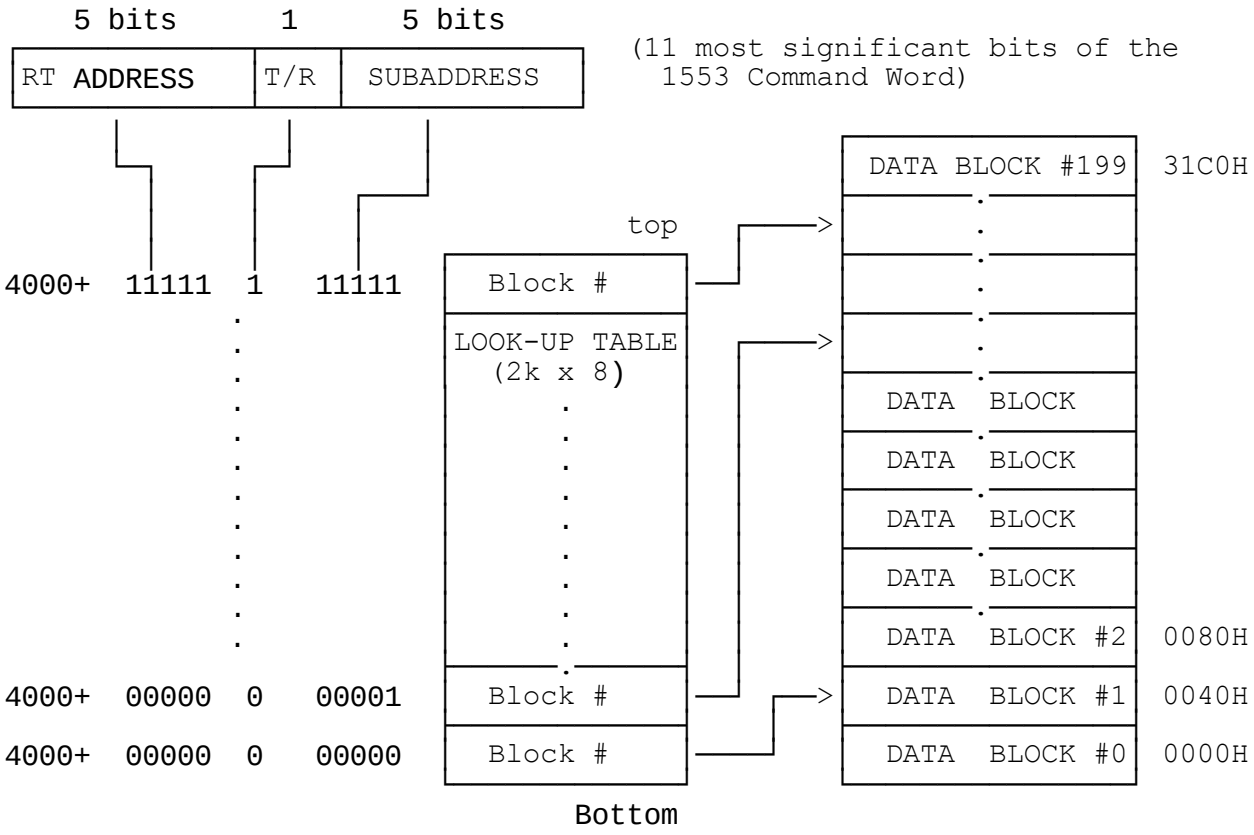
** _-V_ Option

RT Mode

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DATA BLOCK LOOK-UP TABLE 4000 --> 47FF (H)

The received Command word_s RT Address, T/R bit, and Subaddress Fields are used to index into the [user-programmed] look-up table. Each entry in the table represents a "DATA BLOCK NUMBER" (from 0 to 199 decimal.). Each block can contain up to 32, 1553 data words (64 bytes). Data Block _0_ starts at address _0000_, while Data Block _1_ begins at address _0040_, etc.



Important Note For RT to RT messages

When the board is simulating both RT_s in an RT to RT message transfer, the simulated receiving RT_s data block is not updated with the transmit data. (The data IS transmitted over the 1553 bus).

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HOW TO CREATE THE ADDRESS TO THE TABLE

1. Isolate the ELEVEN (most significant) bits of the 1553 Command Word (RT Address, T/R, and Subaddress Field).

Example: Allocate a data block for a 1553 Receive message to RT#5, SA3.

RT Address = 5 T/R= 0 (Rcv) Subaddress = 3

0 0 1 | 0 1 | 0 | 0 | 0 0 1 1 (LSB)

The Hex representation = 143 (H)

2. Add this value to the base address of the Look-Up Table (4000H).

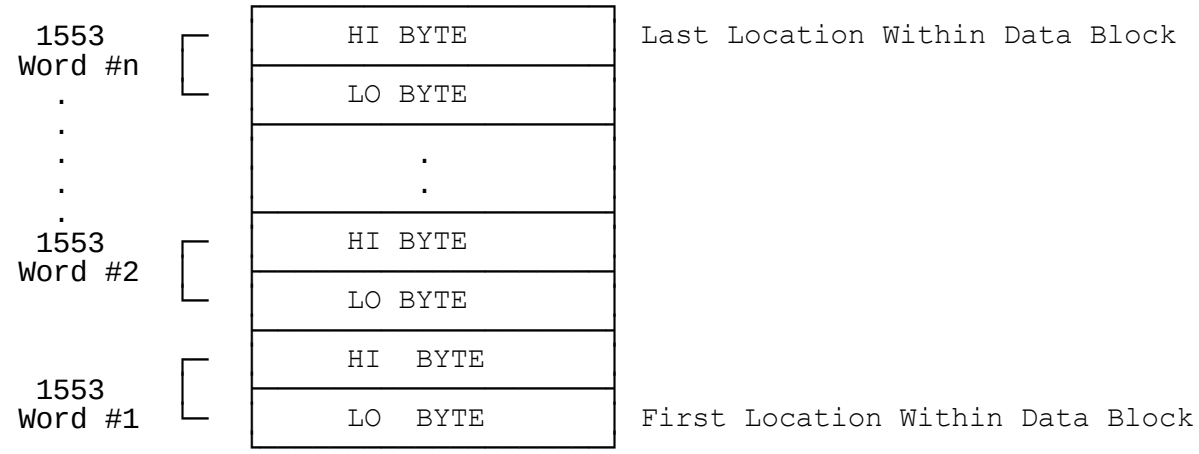
```
    4000 (H)
 +   143 (H)
-------------
    4143 (H)
```

3. Write the Data Block NUMBER to this location

4."POKE &H4143,01", for example, allocates block #1 for this message_s data. Read the 1553 data out by reading Block #1 which resides [starting] at address 0040(H). Each data block, beginning at address "0000" is 64 bytes long (for up to 32 1553 data words). The address of a block is obtained by multiplying its Block Number by 64 (40Hex).

DATA STORAGE

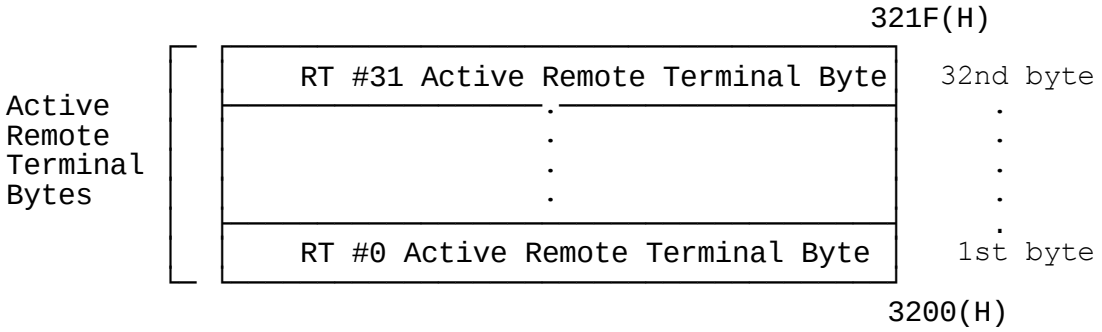
The data words must be stored in the following sequence within the data block:



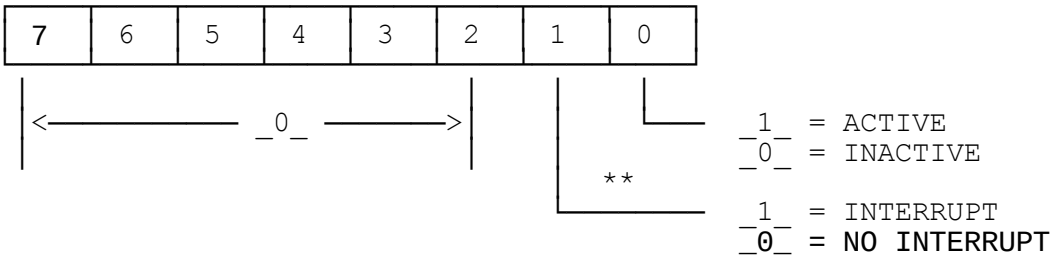
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ACTIVE RT TABLE 3200 --> 321F (H)

These 32 locations (bytes) contain the list of Active Remote Terminals. Each RT which is to be simulated is selected by setting bit _00_ within the Active Remote Terminal Byte to a logic _1_. The first Active RT byte relates to RT #0, the next to RT #1, while the last location relates to RT #31.



ACTIVE REMOTE TERMINAL BYTE DEFINITION:



** = User must set this interrupt bit and the bit within the Interrupt Condition Register in order to generate an interrupt to the computer.

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1553 RT STATUS WORDS	3220 ---> 325F (H)

These locations are reserved for the [32] 1553 RT STATUS Words. The user loads the desired STATUS Words into related locations within the block. The first two bytes relate to RT #0, the next two bytes to RT #1, while the last two locations relate to RT #31. Load LO-byte then HI-byte.
For each RT, which is to be simulated, all 16 bits must be defined within its STATUS word.

The user defined STATUS word is sent, whenever the RT has to respond with a STATUS Word.

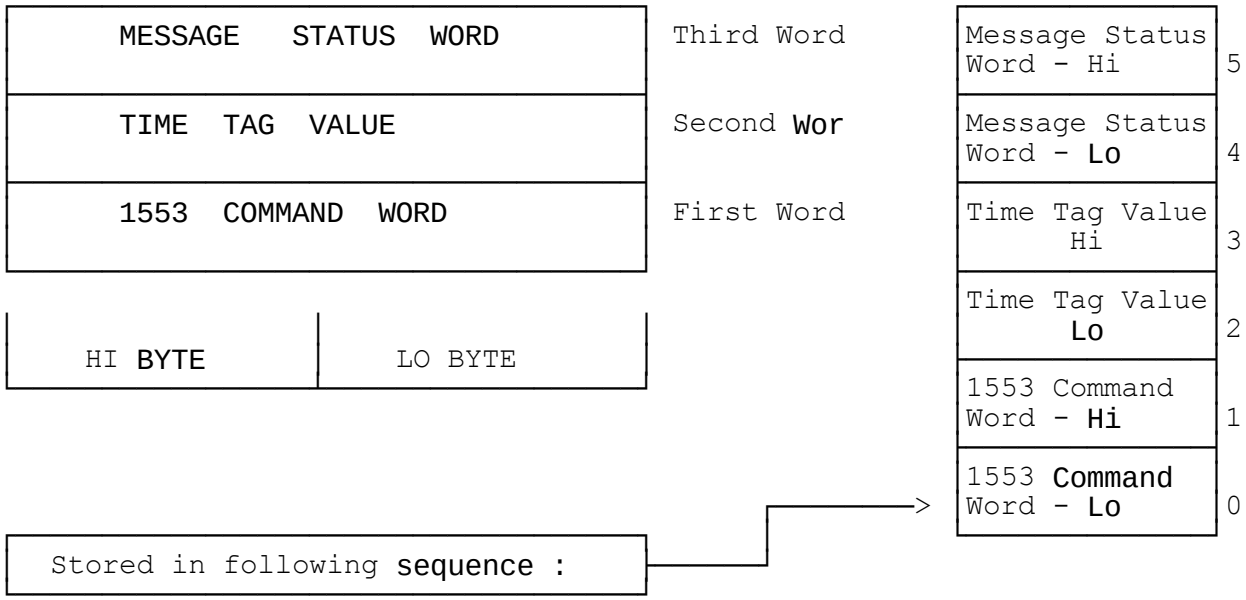
Note: The 1553B Format for the STATUS word is defined in following

Bit #	Bit Name
15-11	RT Address
10	Message Error
9	Instrumentation
8	Service Request
7-5	Reserved
4	Broadcast
3	Busy
2	Subsystem Flag
1	Dynamic Bus
0	Terminal Flag

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MESSAGE STACK

The EXC-1553PC/E generates a Message Stack within the dual-port memory. This stack contains information which can be utilized by the user for post processing of the Remote Terminal messages. The stack is divided into 42 blocks - each containing three words. The stack operates as a Circular Buffer. The Message Stack Pointer points to the beginning of the [next] unused block. Only "ACTIVE" RT messages are stored. The figure below illustrates one instruction block.



NOTE : RT to RT message

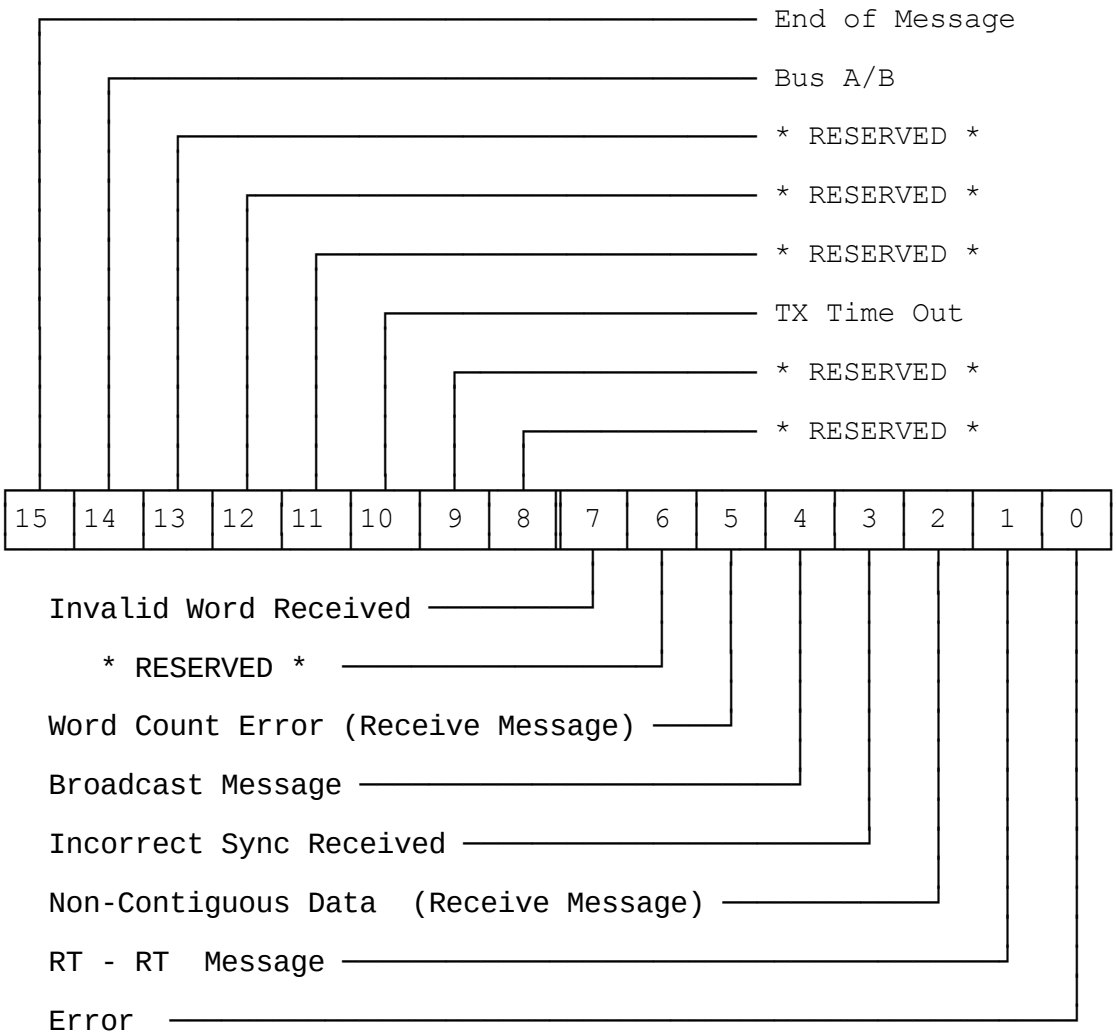
In the event that an RT to RT message is received - whereby the board operates as BOTH RT_s, the Message Stack would be updated as follows:

1.Two Message Stack Blocks are utilized
2.The 1553 "Receive" Command Word is written into the FIRST Message Stack Block
3.The RT-RT bits within BOTH Message Status Words will be set (=1)
4.The Time Tag Word within the SECOND stack block is updated by the board as is the SECOND Message Status Word. The _RT to RT_ bit is the only bit within the FIRST Message Status Word which is updated (active).
5.The 1553 "Transmit" Command Word is written into the SECOND message block

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MESSAGE STATUS WORD

The Message Status Word indicates the status of the message transfer. This word is created by the Board and is NOT the 1553 "STATUS WORD". The contents of the Message Status word are shown below:



NOTE: A LOGIC _1_ INDICATES OCCURRENCE OF STATUS FLAG

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Message Status Word Definitions:

15	End of Message	INDICATES THAT THE MESSAGE TRANSFER HAS BEEN COMPLETED
14	Bus A/B	INDICATES ON WHICH BUS THE MESSAGE WAS TRANSFERRED. _0_ = BUS B ; _1_ = BUS A
13	Reserved	SET TO LOGIC _0_
12	Reserved	SET TO LOGIC _0_
11	Reserved	SET TO LOGIC _0_
10	Tx Time Out	CARD,ACTING AS RECEIVER IN RT-RT MESSAGE, DID NOT SENSE A TRANSMITTER STATUS WORD (within 14 µsec)
09	Reserved	SET TO LOGIC _0_
08	Reserved	SET TO LOGIC _0_
07	Invalid Word	INDICATES THE RECEPTION OF AT LEAST ONE INVALID 1553 WORD (i.e. Bit Count, Manchester code, Parity)
06	Reserved	SET TO LOGIC _0_
05	Word Ct Error	INDICATES THAT AN INCORRECT NUMBER OF WORDS WERE RECEIVED WITHIN THE MESSAGE
04	Broadcast Message	INDICATES THAT A BROADCAST COMMAND WORD HAS BEEN RECEIVED
03	Incorrect Sync	INDICATES THAT THE SYNC OF EITHER THE COMMAND OR THE DATA WORD(s) WAS INCORRECT
02	Non-Contiguous	INDICATES OCCURRENCE OF AN INVALID GAP BETWEEN RECEIVED 1553 WORDS
01	RT - RT Message	INDICATES THAT AN _RT to RT_ MESSAGE HAS BEEN RECEIVED
00	ERROR	INDICATES THE OCCURRENCE OF AN ERROR (DEFINED WITHIN ONE OF THE OTHER MESSAGE STATUS BIT LOCATIONS)

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Time Tag (Read by user)

The Time Tag Value is a 16-bit word which may be used to determine the time elapsed since _START_ or to determine the time between the 1553 messages. The internal Time Tag counter is loaded upon receipt of a "START" command with the 16-bit value found within the "Time Tag Preset Registers" (Hi and Lo). The Time Tag counter is incremented every "N x 155 nsec" - where N is the value of "Time Tag Resolution Registers" (Hi and Lo). The timer is not updated during the reception of the message and as such measures the time from the end of a message until the beginning of the next message. The counter "continues" to run between messages is not reset between messages.

EXAMPLE:

Given:

```
 Time Tag Preset Register Lo = 00            (initialized before "START")
 Time Tag Preset Register Hi = 00            (      "       "       "   )
 Time Tag Resolution Register Lo = 0C (H)    (      "       "       "   )
 Time Tag Resolution Register Hi = 00        (initialized before "START")

 Time Tag Value Lo = 40 (Hex)                (value read during or after
 Time Tag Value Hi = 10 (Hex)                 message transfers)

Time Elapsed (since "START"):    1040 (Hex)  *  ( 000C(Hex) * 155 nsec.)=
                                   4160 (dec)  *  ( 12  * 155 nsec)=
                                                  =  7737 µsec
                                                  =  7.73  msec.
```

1553 Command Word

This location contains the 1553 Command Word associated with the message. Only ACTIVE RT 1553 Command Words are stored !!.

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RT LAST COMMAND WORDS 3400 ---> 343F (H)

These locations are reserved for the [32] 1553 Last Command Words. The EXC-1553PC/E writes these locations at the end of each message transfer (for "active" RT_s only). The first two bytes relate to RT #0, the next two bytes to RT #1, while the last two locations relate to RT #31. Read : LO-byte, then HI-byte. These words are used for the implementation of the _Transmit Last Command Word_ Mode Code.

1553 RT BIT WORDS 3440 ---> 347F (H)

These locations are reserved for the [32] 1553 Bit Words. The user loads the desired Bit Words into the related locations within the block. The first two bytes relate to RT #0, the next two bytes to RT #1, while the last two locations relate to RT #31. Load LO-byte then HI-byte. These words are used for the implementation of the _Transmit Bit Word_ Mode Code.

1553 RT VECTOR WORDS 3480 ---> 34BF (H)

These locations are reserved for the [32] 1553 Vector Words. The user loads the desired Vector Words into the related locations within the block. The first two bytes relate to RT #0, the next two bytes to RT #1, while the last two locations relate to RT #31. Load LO-byte then HI-byte. These words are used for the implementation of the _Transmit Vector Word_ Mode Code.

RT TO RT MESSAGES

When the board is operating as both RT_s in an "RT to RT" transfer, then:

1. The board transmits both 1553 Status and Data words out onto the bus.
2. The Transmit Data Block is NOT copied [by the board] into the

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MODE CODES

The user can program the Subaddress code that will indicate the reception of a Mode Command. Either or both of the following codes can be used: _11111_ and _00000_. The user must program the Mode Code Control Register as described within the Control Register section.

The EXC-1553PC/E handles all Dual-Redundant 1553B Mode Codes. This is to say that the Word Count field is decoded according to MIL-STD-1553B. One of the Mode Codes (SYNCHRONIZE WITH DATA WORD) is operated upon as a "standard" message transfer - using the Data Block Look-Up Table. In such a case, the Command Word_s RT Address, T/R bit and Subaddress fields are used as a pointer to the look-up table. The table entries that are addressed when the T/R bit =_0_ and Subaddress = _00000_ or _11111_ should contain a Data Block Number (0-199) as TO where the _Synchronize With Data Word_s data word should be stored.

Mode Codes such as : Transmit Last Command, Transmit Vector Word, and Transmit Bit Word are accomplished by using the dedicated blocks within the on-board memory. (Described above)

BROADCAST MODE

The EXC-1553PC/E can operate within the Broadcast environment by selecting the appropriate Dip Switch setting as defined within the section on _DIP SWITCH SETTINGS_.

When operating in the BROADCAST mode, the user must set the RT ACTIVE Look-Up Table entry RELATING TO RT #31 as NOT ACTIVE !. The EXC-1553PC/E will then test the Broadcast Dip Switch to see whether the board is operating in the Broadcast mode.

In addition (while operating in the Broadcast mode) the board will store the received message into a 1553 data block area as is done with "standard" message formats (RT address, T/R bit, and Subaddress are used as a pointer to the Data Block Look-Up table memory).

Note: When operating in the Broadcast Mode, the Broadcast bits within the 1553 Status Words are NOT updated by the board_s processor. In addition the minimum intermessage gap time between the broadcast command and the subsequent 1553 command is approximately 35µsec.

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ERROR INJECTION FEATURES

The EXC-1553PC/E card allows two types of error injection; Global (for all RT_s) and a "per RT" error. The Global errors such as Parity, Sync, Non-Contiguous Data and Bit Count are detailed in the Error Injection Register description. These errors are either "ON" or "OFF" for all RT_s. The ability to inject a 1553 Word Count error, however, is on a per RT basis.

WORD COUNT ERROR TABLE 32E0 --> 32FF (H)

The Word Count error is selected by writing to the Word Count Error Table. This table contains 32 bytes (one per Remote Terminal). The first byte relates to RT #0, the second to RT #1, while the last location relates to RT #31. The contents of each location controls the number of 1553 words
(+/- 3 words) within the message. The variation is an offset - relative to the 1553 Command Word_s WORD COUNT FIELD. The "resulting" message (if an error is programmed) must contain at least ONE data word. This table is defaulted to _00_ by the board upon powewr-on or software reset. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify the contents and then issue a "START" (see Start Register).

32FF(H)

WRD CNT ERR for RT# 31
WRD CNT ERR for RT# 30
. . .
WRD CNT ERR for RT# 0

32E0(H)

WORD COUNT ERROR BYTE DEFINITION:

OFFSET	TABLE VALUE
-3 Words	FD (H)
-2 Words	FE (H)
-1 Word	FF (H)
0 (No Word Count Error injected) ——>	00 (H)
+1 Word	01 (H)
+2 Words	02 (H)
+3 Words	03 (H)

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note: all values are in HEX unless stated

```
10 POKE &H3FFF,02      _ LOAD CONFIGURATION REG. = RT MODE
15 POKE &H3FF2,xx      _ LOAD VARIABLE AMPLITUDE REGISTER (_-V_ OPTION)
20 POKE &H3201,1       _ ENABLE RT#1
30 POKE &H3204,1       _ ENABLE RT#4

40 POKE &H3222,00      _ LOAD STATUS WORD (RT#1) WITH _0800_
50 POKE &H3223,08      _
60 POKE &H3228,00      _ LOAD STATUS WORD (RT#4) WITH _2000_
70 POKE &H3229,&H20    _

80 POKE &H3FF7,xx      _ LOAD TIME TAG RESOLUTION REGISTER
90 POKE &H3FF8,xx      _
100 POKE &H3FF9,00     _ LOAD TIME TAG PRESET REGISTER
110 POKE &H3FFA,00     _

120 POKE &H3266,00     _ LOAD MODE CODE CONTROL REG = SA 00000&11111
130 POKE &H3FF3,00     _ NO GLOBAL ERROR INJECTION

140 POKE &H4xxx,xx     _ LOAD LOOK-UP TABLE WITH BLOCK NUMBER FOR DATA
                       _ STORAGE
150 POKE &H4xxx,xx     _ LOAD LOOK-UP TABLE WITH BLOCK NUMBER FOR DATA
                       _ STORAGE

160 POKE &H3FFC,1      _ LOAD START REGISTER WITH "1". STARTS RT MODE
170 STOP
```


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CONTROL REGISTER DEFINITIONS

RESET INTERRUPT REGISTER 7001(H)

Writing to this register will reset the Interrupt signal to the computer. The Data field is ignored. This register should be written to at the beginning of a user-written, interrupt service routine.

BOARD RESET REGISTER 7000(H)

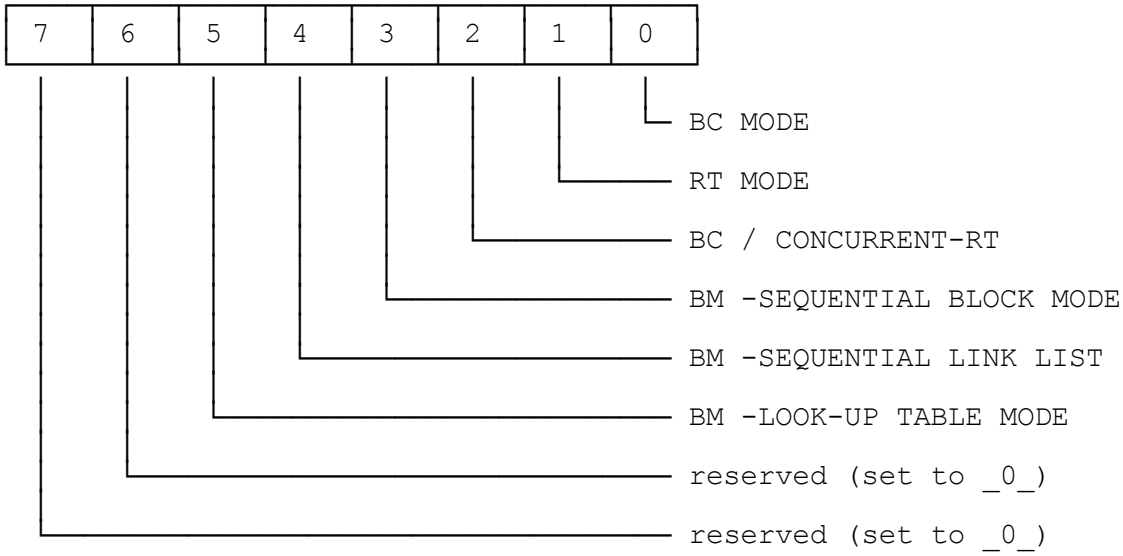
Writing to this location will RESET the EXC-1553PC/E board. The board will act as if POWER had been switched off then on. The data field is ignored.
NOTE: _RESET_ ERASES ALL MEMORY LOCATIONS WITHIN THE DUAL-PORT RAM !!! The Board Status, the Board ID, Firmware Revision and Variable Amplitude registers are written by the board after the reset operation has been completed.

EX. > POKE &H7000,xx

BOARD CONFIGURATION REGISTER 3FFF(H)

Set the desired bit to a logic _1_

The operating mode of the board is set via this register. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).



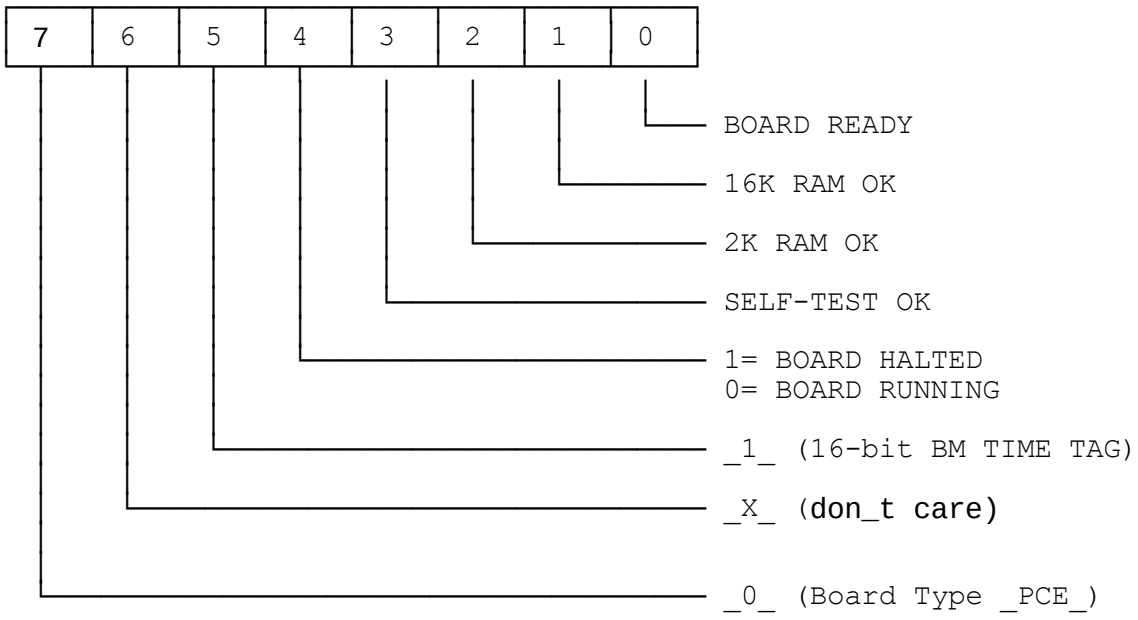
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BOARD ID REGISTER 3FFE(H)

This register contains a fixed value which can be read by a user_s initialization routine to detect the presence of the EXC-1553PC/E card.
The one-byte value of this register is: 45 (Hex) ; ASCII _E_.

BOARD STATUS REGISTER 3FFD(H)

This register indicates the status of the EXC-1553PC/E card. In addition, this register indicates option selection as defined below. (Status bits are active _1_).

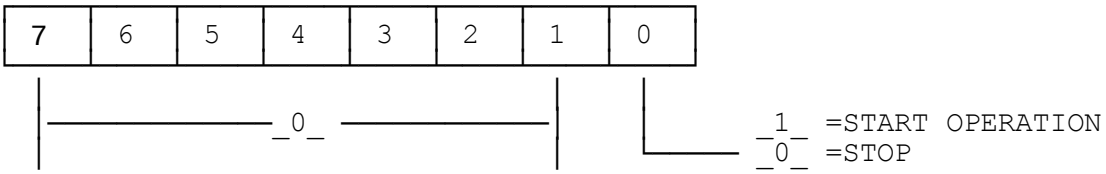


NOTE: Bit "04" (Board Halted) is set by the board after the user "stops" the current operation (by resetting the START bit within the Start Register). The user must check this bit first before modifying registers which first require a "STOP" operation. The board resets this bit after receiving a subsequent START command (by writing to the Start Register). This bit is a new feature available within EPROM revisions starting with 6.5. The condition of this bit after power-on or software reset is a logic "1".

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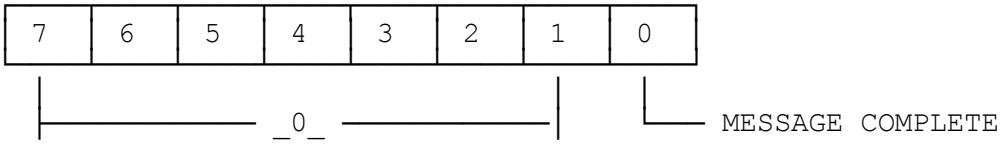
START REGISTER 3FFC(H)

This register controls the _START / STOP_ operation of the EXC-1553PC/E. The user can Start - then Stop the RT operation, modify RT parameters (example: the Error Injection register or Response Time), and then re-issue a new Start in real-time. See note on the Board Status Register (Board Halted/Running) ;Bit 04.



MESSAGE STATUS REGISTER 3FFB(H)

This register indicates that a 1553 message has been received. The figure below illustrates the placement of the status bit. A logic _1_ indicates active condition (bit is also set for messages with errors).



Note: Message Complete bit is NOT reset by the board and should be reset by the user after reading it.

TIME TAG PRESET REGISTER - HI & LO 3FFA, 3FF9(H)

These registers contain the INITIAL VALUE of the Time Tag Counter. The _HI_ register contains the MSB , the _LO_ register contains the LSB (see Message Stack Description). This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

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TIME TAG RESOLUTION REGISTER - HI & LO 3FF8, 3FF7(H)

This 16-bit value represents the resolution of the Time Tag Counter in increments of 155 nsec. See Time Tag description above. (The _HI_ register contains the MSB , the _LO_ register contains the LSB). This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

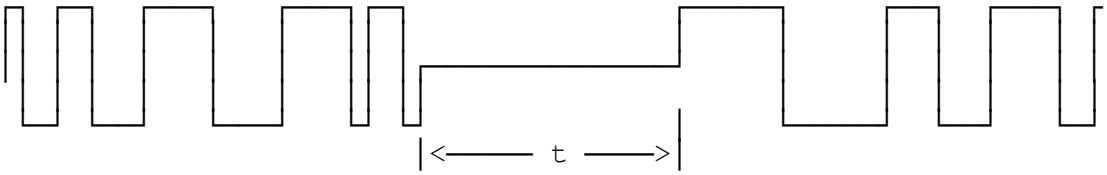
BIT COUNT REGISTER 3FF6(H)

Sets the number of total bits within the 1553 word ; including Sync(3) & Parity(1). This register is utilized by the board only if the "Bit Count Error bit" is set within the Error Injection Register. If the bit is not set, then a [valid] 20 bit word is transmitted regardless of the contents of this register. This feature is valid for messages which contain at least 3 1553 data words and has an RT Response Time Register value greater than _00_. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

CONTENTS OF REGISTER:	NUMBER OF BITS:
00	18 BITS (-2 BITS)
01	22 BITS (+2 BITS)

RT RESPONSE TIME REGISTER 3FF4(H)

This register sets the RESPONSE TIME of the Remote Terminal. The resolution of this register is 155 nsec. per bit. This time is measured as the "DEAD TIME" on the 1553 bus. The minimum time is equal to approximately 7.0 µsec which is achieved by writing a 0 to this register. The value in the register is ADDED to the minimum time. An adapter card is available (free of charge) which reduces the minimum Response Time to approximately 4.0 µsec. Write a "00" in order to use the minimum [4usec] response time. Any value above zero will result in a response value equal to 7usec plus the contents of the register. The actual Response Time will be ±1µsec tolerance. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

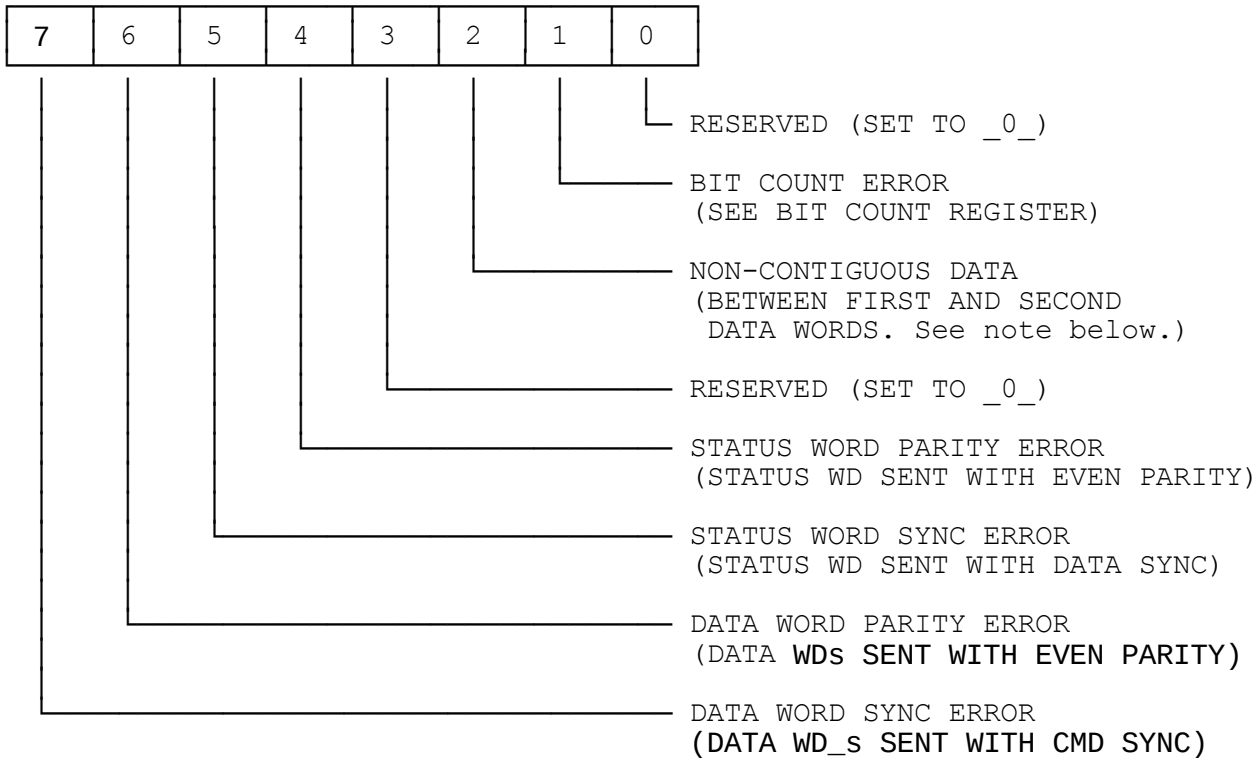


Example: To request a response time of 9µsec, write 13 to this register.
13 * 0.155 = ~2µsec + 7µsec = 9µsec

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ERROR INJECTION REGISTER 3FF3(H)

The Error Injection register is a global register which allows the user to select the type of error to be injected within a transmitted message. This register is read by the EXC-1553PC/E upon the receipt of a "START" (by writing to the Start Register). To modify this register: issue a "STOP", modify and then re-issue a START (see: START Register).



Note: Non-contiguous data error is not available when the board is operating as both RT_s in an RT to RT message transfer.

VARIABLE AMPLITUDE REGISTER 3FF2(H) (_-V_ Option)

This register specifies the amplitude of the 1553 output signal. The signal can be programmed from 0 volts up to 7.5volts (p-p) - measured on the 1553 bus with specified 1553 coupling and 35ohm load (two 70 ohm termination resistors were used). A higher Transmit [output] amplitude will appear on the 1553 bus if 78 ohm termination resistors are used. The register has a resolution of 30mv/bit (p-p) on the bus. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register). For EPROM Revisions 6.5 and above this register defaults to FFH after Reset, providing maximum amplitude.

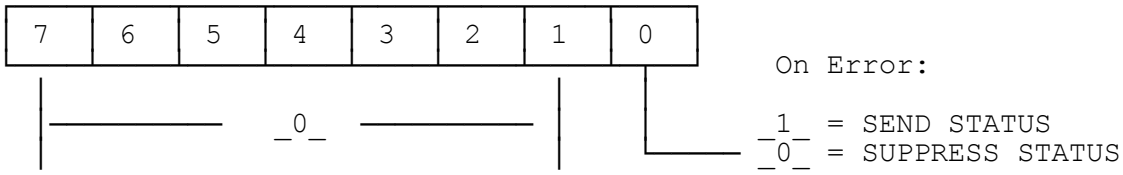
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MESSAGE STACK POINTER 3FF1, 3FF0 (H)

The Stack Pointer indicates the Message Stack position. This pointer is updated (incremented by _6_) after the entire message has been received. This word "circulates" with the Message between 3300(H) to 33F6(H). It is initialized to _3300 (H)_.

STATUS RESPONSE REGISTER 3FEF (H)

This register is used to control the Status Response mode of operation. The user can select to respond with a 1553 Status Word [following a receive message] EVEN if an INVALID 1553 Data Word was received. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

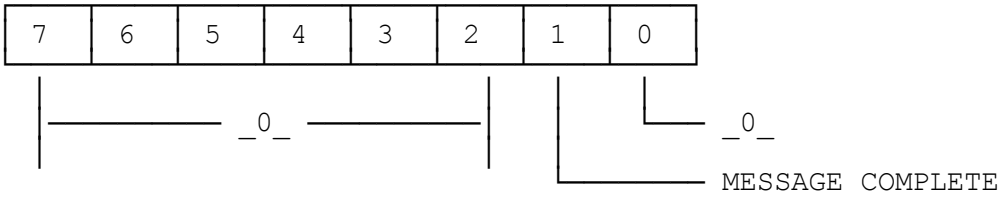


FIRMWARE REVISION REGISTER 3E80 (H)

This register indicates the revision level of the on-board firmware. The value 0110 0011 would be read as revision level: 6.3

INTERRUPT CONDITION REGISTER 33FC (H)

This register allows the user to set an interrupt trigger. A logic _1_ enables the interrupt condition. When Message Complete is enabled an interrupt will be generated at the end of processing for every message directed to an RT being simulated by the board for which the Interrupt Bit in its Active RT Table entry has been set. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).



RT Mode

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MODE CODE CONTROL REGISTER	3266 (H)

This register allows the user to determine which 1553 Subaddress value indicates the reception of a 1553 Mode command. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

7	6	5	4	3	2	1	0
——— _0_ ———							

0	0	- _11111_ and _00000_
0	1	- _00000_ Only
1	0	- _11111_ Only
1	1	- _00000_ and _11111_

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BC / CONCURRENT-RT OPERATION

The EXC-1553PC/E can operate as the Bus Controller and up to 32 Remote Terminals. The user loads the messages and the Instruction Stack as per the BC Operation.

In the Concurrent RT Mode, the user also loads the message blocks with the RT_s 1553 Status and data words. These words must be loaded into the appropriate locations within the message blocks - in the sequence that the 1553 words appear on the 1553 bus.
NOTE : THIS IS ONLY FOR THOSE REMOTE TERMINALS WHICH THE USER IS ACTIVELY SIMULATING !! For those RT_s which are not ACTIVE (not simulated by the EXC-1553PC/E within a single message), the user must leave the related locations blank within the associated 1553 message blocks.

The Remote Terminals simulated in this mode have a minimum Response Time of approximately 4µsec. (measured as: "dead time" on the bus).

NOTE:

The user should use the following sequence to determine whether the board is installed AND ready to operate:

* Check the Board ID register (test for value = 45 Hex)
* Check Board Status Register (test for Board Ready bit = _1_)

The board is installed and ready when BOTH of these registers contain the correct values (as written above). This sequence should be used after power-on and software reset operations. For Software Reset operations; these values should be set to ZERO by the user immediately prior to writing to the [software] Board Reset Register.

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BC & CONCURRENT RT MEMORY MAP

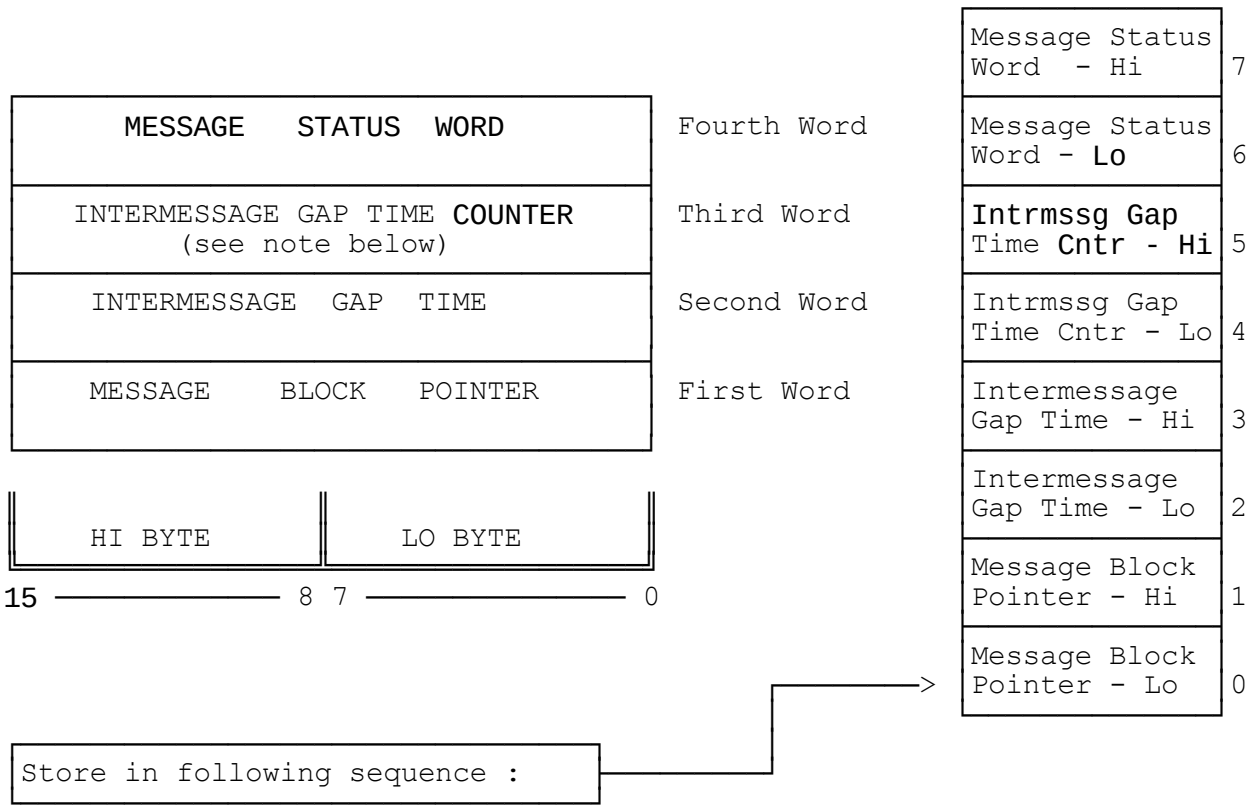
RESET INTERRUPT REG.	7001 (H)
BOARD RESET REGISTER	7000 (H)
reserved	6FFF (H) ... 4000 (H)
BOARD CONFIGURATION REG.	3FFF (H)
BOARD ID REGISTER	3FFE(H)
BOARD STATUS REGISTER	3FFD (H)
START REGISTER	3FFC (H)
INTERRUPT CONDITION REG.	3FFB (H)
MESSAGE STATUS REGISTER	3FFA (H)
RT RESPONSE TIME REGISTER	3FF9 (H)
reserved	3FF8 (H)
reserved	3FF7 (H)
LOOP COUNT REGISTER	3FF6 (H)
BIT COUNT REGISTER	3FF5 (H)
WORD COUNT REGISTER	3FF4 (H)
BC RESPONSE TIME REGISTER	3FF3 (H)
** _-V_ Option ** VARIABLE AMPLITUDE REG.	3FF2 (H)
STACK POINTER - HI	3FF1 (H)
STACK POINTER - LO	3FF0 (H)
FRAME TIME - HI	3FEF (H)
FRAME TIME - LO	3FEE (H)
FRAME TIME RESOLUTION - HI	3FED (H)
FRAME TIME RESOLUTION - LO	3FEC (H)
INSTRUCTION COUNTER	3FEB (H)
reserved	3FEA (H) ... 3E81 (H)
FIRMWARE REVISION REGISTER	3E80 (H)

reserved	3E7F(H) ... 3420(H)
ACTIVE RT TABLE (32 bytes)	341F(H) ... 3400(H)
INSTRUCTION and MESSAGE BLOCK AREA	33FF(H) ... 0000 (H)

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INSTRUCTION STACK

The user programs the EXC-1553PC/E via the Instruction Stack. The stack is divided into instruction blocks - each containing four words. The figure below illustrates one instruction block.



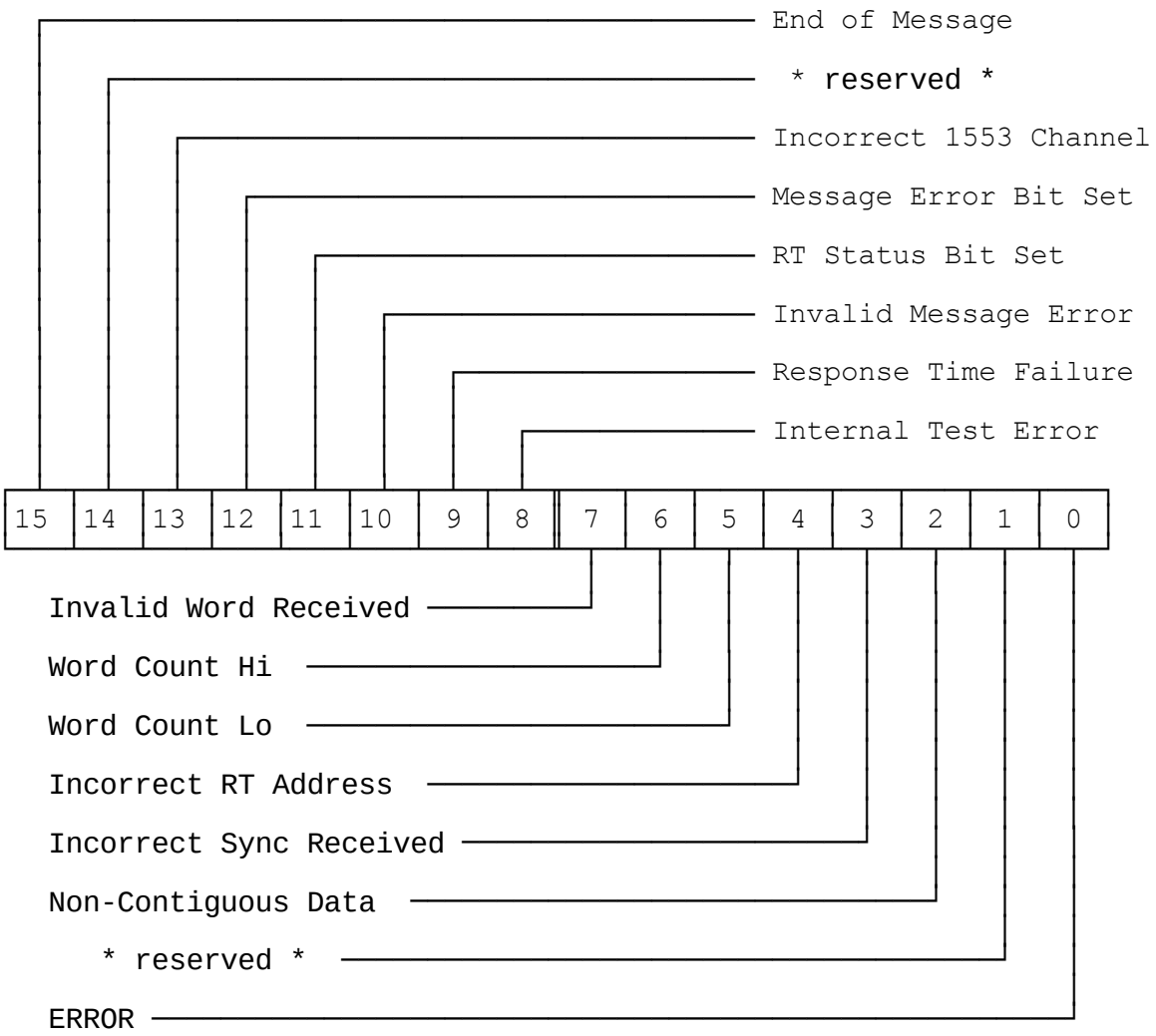
NOTE:

The Intermessage Gap Time Counter, found within EPROM revisions 6.5 and above increases the MAXIMUM intermessage gap time. The counter determines the number of the times that the Intermessage Gap Time value is used (ie If the counter equals "0" then the gap time is per the contents of the Intermessage Gap Time location. If the gap time counter equals "1" then the gap time equals the Intermessage gap time value x 2, etc.

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MESSAGE STATUS	Read by user

The Message Status Word indicates the status of the message transfer. This word is created by the Board and is NOT the 1553 "STATUS WORD". The contents of the Message Status word is shown below:



NOTE: A LOGIC _1_ INDICATES OCCURRENCE OF STATUS FLAG

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Message Status Word Definitions:

15	End of Message	INDICATES THAT THE MESSAGE TRANSFER HAS BEEN COMPLETED
14	Reserved	SET TO LOGIC _0_
13	Incorrect Channel	INDICATES THAT THE REMOTE TERMINAL RESPONSE WAS NOT RECEIVED ON THE ACTIVE 1553 CHANNEL
12	Message Error Bit Set	INDICATES THE _MESSAGE ERROR BIT_ (BIT _10_) WITHIN THE RT STATUS WORD WAS SET
11	RT Status Bit Set	INDICATES THAT A BIT WAS SET WITHIN THE RT STATUS WORD (OTHER THAN THE _MESSAGE ERROR BIT_). The ERROR bit is NOT set in conjunction with this bit.
10	Invalid Message	INDICATES THAT A 1553 _MESSAGE LEVEL_ ERROR OCCURRED (i.e. Word Count, Incorrect Sync) - detailed below.
09	Response Time Error	INDICATES THAT THE RT RESPONDED LATE (See: PROGRAMMABLE BC RESPONSE TIME REGISTER)
08	Internal Test Error	INDICATES THAT THE CARD FAILED ITS INTERNAL SELF-TEST PROCEDURE
07	Invalid Word	INDICATES THE RECEPTION OF AT LEAST ONE INVALID 1553 WORD (i.e. Bit Count, Manchester code, Parity)
06	Word Ct Hi	INDICATES THAT THE RT TRANSMITTED TOO MANY WORDS
05	Word Ct Lo	INDICATES THAT THE RT TRANSMITTED TOO FEW WORDS
04	Incorrect RT Address	INDICATES THAT THE RECEIVED 1553 STATUS WORD DID NOT CONTAIN THE CORRECT _RT ADDRESS_
03	Incorrect Sync	INDICATES THAT THE SYNC OF EITHER THE STATUS OR DATA WORD(s) WAS INCORRECT
02	Non-Contiguous	INDICATES OCCURRENCE OF AN INVALID GAP BETWEEN RECEIVED 1553 WORDS
01	Reserved	SET TO A LOGIC _0_
00	ERROR	INDICATES THE OCCURRENCE OF AN ERROR (DEFINED WITHIN ONE OF THE OTHER MESSAGE STATUS BIT LOCATIONS)

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Intermessage Gap Time	Written by user

The Intermessage Gap Time Value is a sixteen bit word which allows the user to insert a unique intermessage delay time between the current message and the next message. The minimum Intermessage Gap Time is approximately 120µsec. If the Gap Time value written is less than 120µsec, the board will transmit the message with the minimum delay. The resolution of this word is: 155 nsec. per bit.

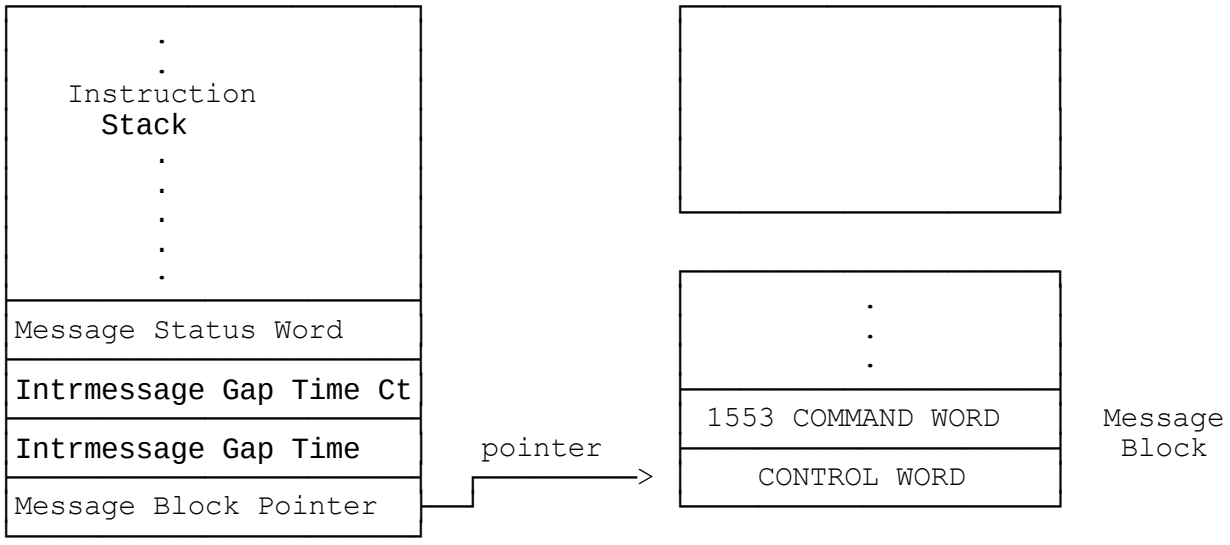
Intermessage Gap Time Counter	Written by user

The Intermessage Gap Time Counter (IGT_Counter) is a sixteen bit word which allows the user to increase the Intermessage Gap Time by repeating the number of times the Intermessage Gap Time Value is used. If the counter equals "0", for example, then the gap time is NOT repeated and is per the contents of the Intermessage Gap Time location. If the gap time counter equals "1" then the gap time is repeated once and equals the Intermessage gap time value x 2.

Notes: 1) This feature is available within the EPROM revisions 6.5 above
2) To ensure maximum intermessage gap time accuracy when using the IGT_Counter, the value within the Intermessage Gap Time Word should be maximized and that within the IGT_Counter minimized, for a given desired intermessage gap time.

Message Block Pointer	Written by user

The Message Block Pointer is a sixteen bit word which points to the beginning of a 1553 Message Block.



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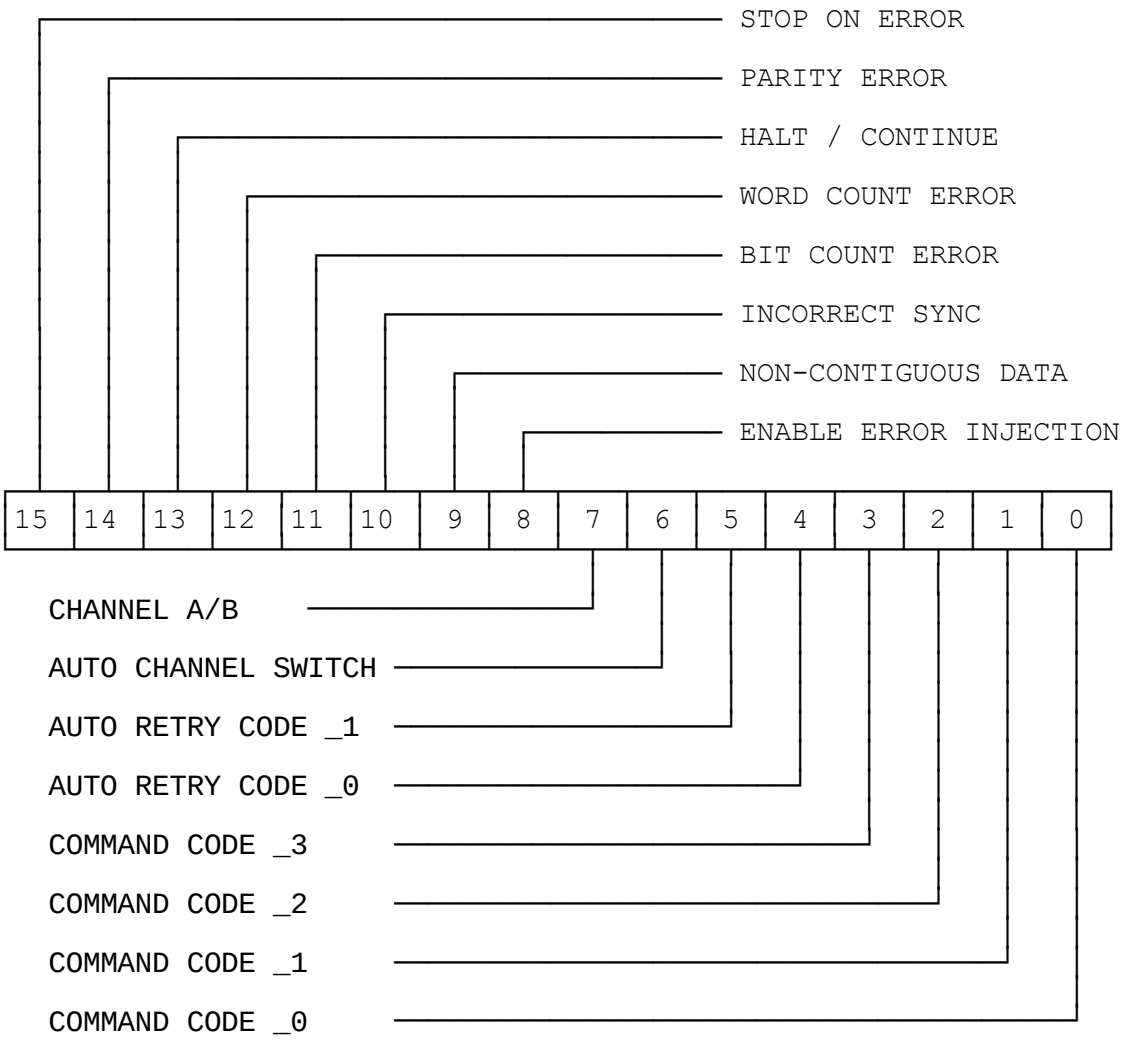
The user loads the Message Block anywhere within the Instruction STACK/MESSAGE BLOCK AREA (see: Memory Map). Message Blocks do NOT have to be stored in sequential locations within the memory since the Message Block Pointers "point" to the Message Blocks in sequence.

Each block contains a 1553 message plus its Control Word. This Control Word is written into the FIRST word of each block. The Control Word instructs the EXC-1553PC/E as to the type of message to be transmitted (i.e. RT to RT, Mode Code, Broadcast, Error injection, etc.). The size of the message block is not fixed and is dependent upon the size of the message itself.

The description of each bit within the Control Word follows:

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Control Word



NOTE : A LOGIC _1_ ENABLES THE FUNCTION, A _0_ DISABLES THE FUNCTION.

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Control Word Definitions:

15	Stop on Error	MESSAGE ERROR STOPS THE BC/RT OPERATION. THE USER CAN RESTART BY WRITING TO THE INSTRUCTION COUNT AND "START"
14	Parity Er	SELECTS _EVEN_ PARITY WITHIN 1553 WORD
13	Halt / Continue	1= HALT. This stops BC/RT transfer operation. This bit MUST BE reset (_0_) in order to RUN or CONTINUE. (see text)
12	Wd Count Error	TRANSMITS LESS or MORE WORDS THAN ARE INSTRUCTED BY THE WORD COUNT FIELD (see: Word Count Register). THIS FUNCTION IS VALID FOR _BC to RT_ MESSAGES ONLY.
11	Bit Count Error	TRANSMITS INVALID NUMBER OF BITS WITHIN 1553 WORDS (see: Bit Count Register)
10	Incorrect Sync	TRANSMITS INCORRECT SYNC . DATA-TYPE SYNC IS TRANSMITTED WITHIN THE COMMAND WORD
09	Non-Contg Data	FIRST 1553 DATA WORD IS TRANSMITTED WITH INVALID GAP TIME (BETWEEN COMMAND AND DATA WORD)
08	En.Error Injection	ENABLES THE ERROR INJECTION CAPABILITY WITHIN THE MESSAGE (MUST be SET in addition to actual Error)
07	CHANNEL A / B	SELECTS ACTIVE 1553 CHANNEL. LOGIC _1_ SELECTS CHANNEL _A" WHILE A LOGIC _0_ SELECTS CHANNEL _B_
06	Auto Chnl Switch	ON ERROR, THE BC WILL RETRY MESSAGE TRANSFER ON ALTERNATE CHANNEL (* AUTO-RETRY MUST BE SELECTED *)
05-04	Auto Rtry Code	ON ERROR, SELECTS THE NUMBER OF RETRIES BEFORE TRANSFER OF NEXT MESSAGE Code _1 _0 0 0 -No Retry 0 1 - 1 Retry 1 0 - 2 Retry 1 1 - 3 Retry
03-00	COMMAND CODE	0000 - TRANSMIT COMMAND (RT to BC) 0001 - RECEIVE COMMAND (BC to RT) 0010 - RT to RT COMMAND 0011 - MODE CODE 0100 - BROADCAST RECEIVE COMMAND 0101 - BROADCAST RT to RT COMMAND 0110 - BROADCAST MODE CODE 0111 - SKIP MESSAGE (see text) 1000 - JUMP COMMAND (see text)

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HALT Operation

The user normally sets this bit to a logic _0_ before writing to the Start Register. The user may, in real-time (during execution), set this bit (to a logic_1_). The board, when operating on that particular Message Block_s Control Word, will HALT transfer operations until the bit is reset to a logic _0_.

When the board detects that the HALT bit is set, it sets the "WAIT FOR CONTINUE" bit within the Message Status Register (see: Control Register Section). This bit can be used by the user in order to know when the board has arrived at this Instruction block. When the board detects that the Halt bit has been reset (continue mode), the board will then reset the "WAIT FOR CONTINUE" bit within the Message Status Register.

It is important to note that this function can only be implemented within Message Blocks which have NOT [AS YET] BEEN EXECUTED BY THE BOARD.

Note: This operation can be used in conjunction with the JUMP feature described below.

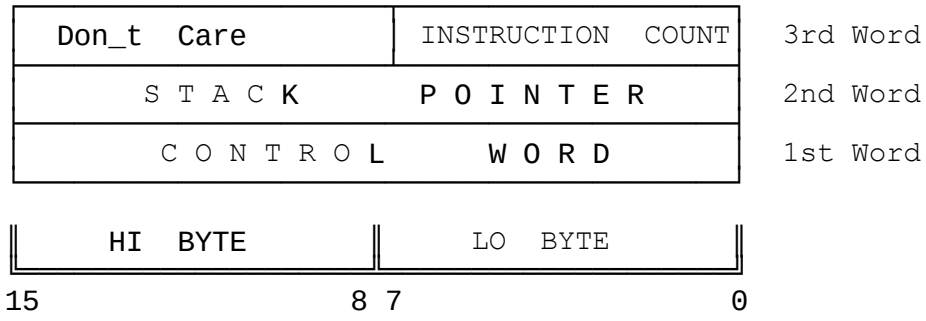
SKIP Message Operation (EPROM Rev 6.5 and above)

The SKIP MESSAGE command allows the user to easily skip a message defined in a certain Message Block by only modifying the Command field within the Control Word. This allows the user to selectively send a message within the current frame. The Intermessage Gap Time associated with the SKIP Message has no effect.

JUMP Command Operation

The EXC-1553PC/E allows the user to modify the BC transfer cycle by setting the "JUMP" command within the Control Word. The Jump command instructs the board to operate on a New instruction stack or New stack entry within the same stack. This Control word is followed by a Stack Pointer word instead of the usual 1553 Command Word. In addition, the Stack Pointer is followed by an Instruction Count value. The Jump command is tested AFTER the board has tested the HALT/CONTINUE bit within the Control Word. The Intermessage Gap Time associated with the JUMP command has no effect.

The memory location sequence is illustrated below:

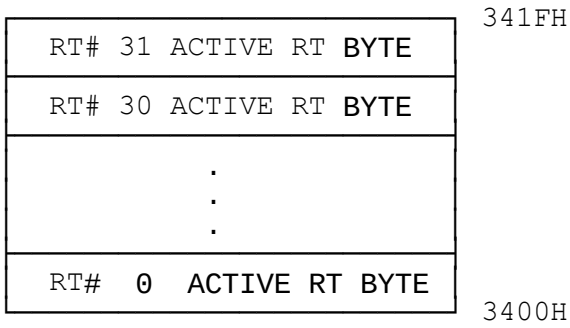


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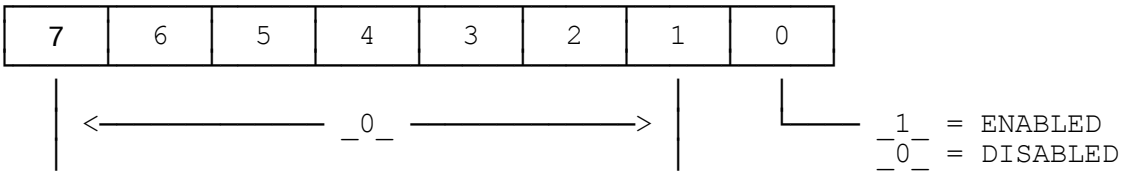
REMOTE TERMINAL SIMULATION

In the case where the board is simulating both the Bus Controller and one or more Remote Terminals, the user must write (into the Message Block) the simulated Remote Terminal 1553 Status Word and Data word(s) in the sequence in which it appears over the 1553 bus (see MESSAGE BLOCK FORMATS).

The user instructs the board as to which Remote Terminals are to be simulated by writing to the (32- byte) Active Remote Terminal Table. Each entry within the 32-byte table relates to a specific Remote Terminal. The first location relates to RT #00, while the last location relates to RT #31 (for a total of 32 locations). Writing a value _01_ to the table entry ENABLES the Remote Terminal simulation by the board. A value of _00_ written to the table disables the simulation by the board.



ACTIVE REMOTE TERMINAL BYTE DEFINITION



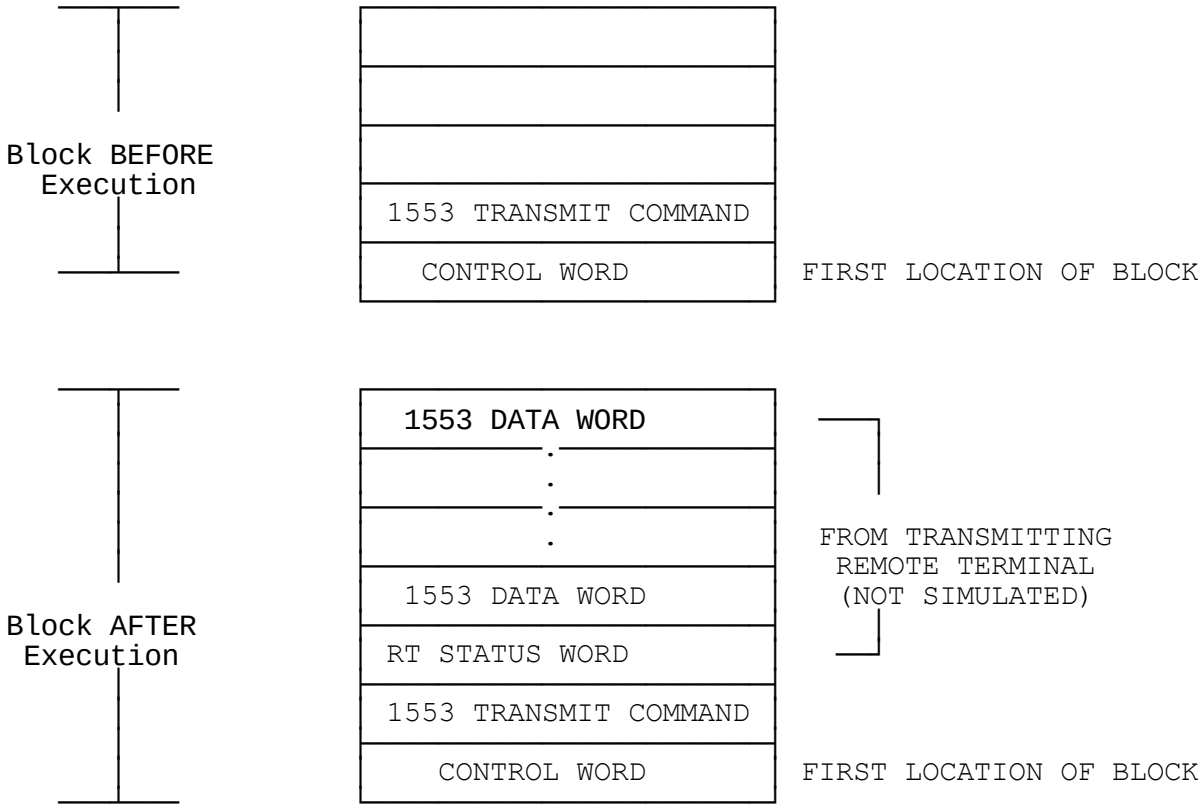
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MESSAGE BLOCK FORMATS

The Message Block contains, or will contain following message transfer, the entire 1553 message as it appears on the 1553 bus - including Command Word(s), Data Words, and Status Word(s).

Examples #1

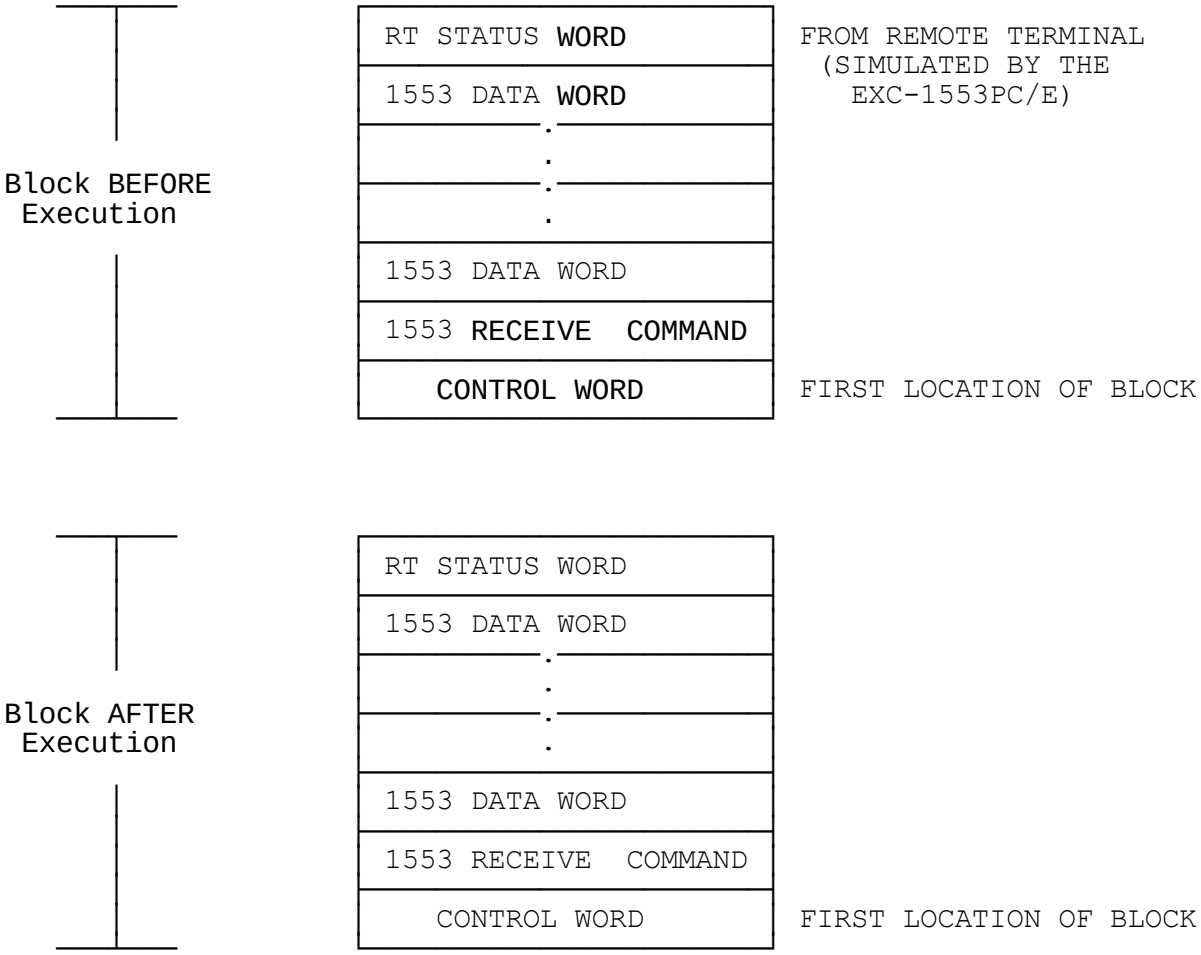
TRANSMIT COMMAND
OPERATING AS BC ONLY



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Examples | #2

RECEIVE COMMAND
OPERATING AS **BOTH** BC AND RECEIVING RT

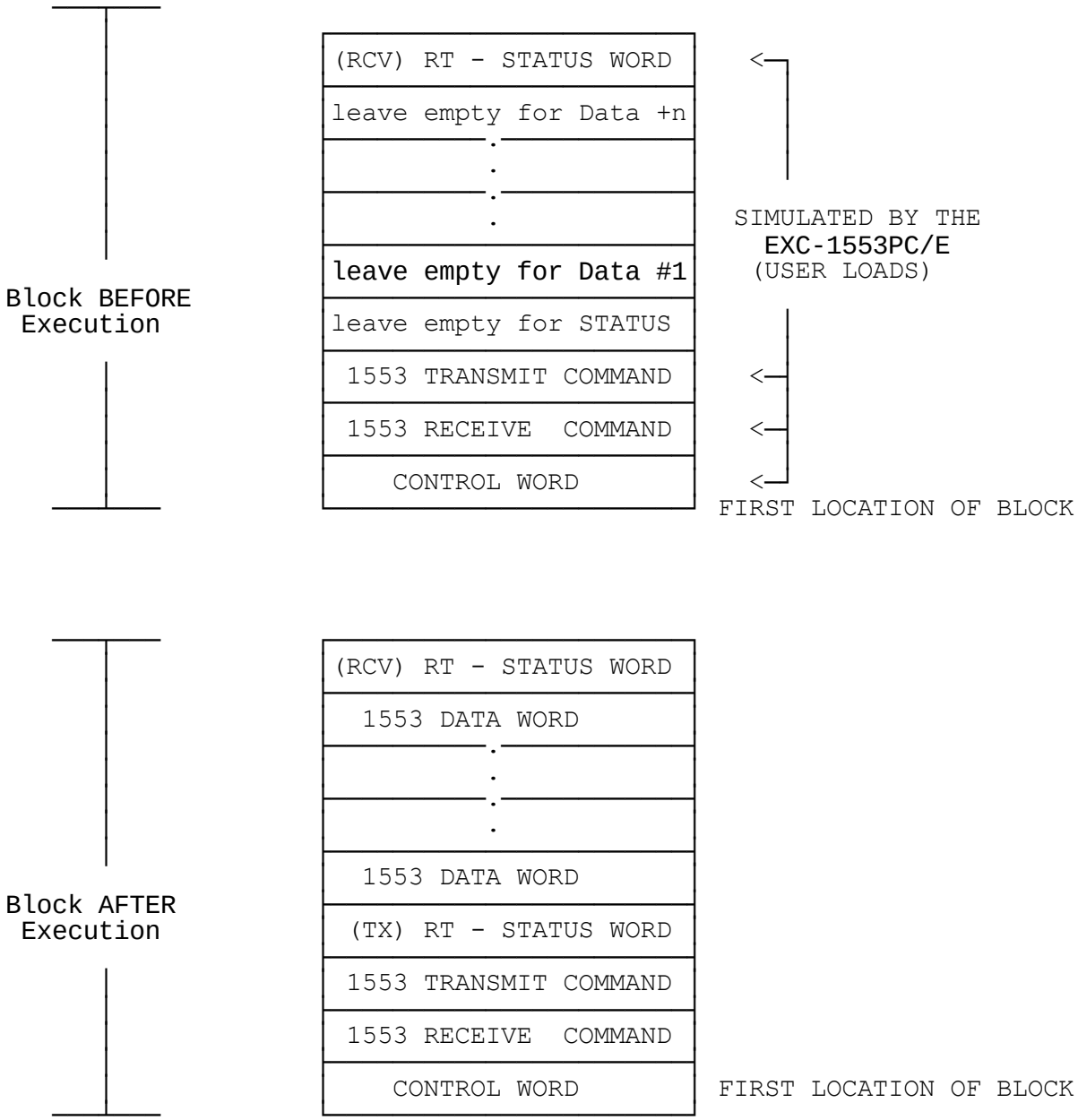


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Examples | #3

RT to RT COMMAND

OPERATING AS BC and RECEIVING RT



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CONTINUOUS or ONE-SHOT MESSAGE TRANSFERS

The EXC-1553PC/E offers the capability of transferring all programmed messages once, in a continuous loop, or for _N number of times_.

In the One-Shot mode, the board transfers all messages [after receipt of a "START" command], sets the Message Complete Bit within the Message Status Register, issues an Interrupt [if programmed] and waits for a new "START". This mode is selected via the Start Register (see Start Register definition).

In the _N_ Times Mode, the user loads the Loop Count Register with the number of times to transmit the messages [frame] and sets the LOOP and START bits within the Start Register. The user can select to transmit from one to 255 times (see: Start and Loop Count Registers). The time between frames is predetermined via frame Time Register (see below).

In the Continuous mode, the EXC-1553PC/E will re-transmit the message frame at a predetermined, user-programmable rate. This mode is selected via the Start Register and the Loop Count Register (see Register definitions). In this mode, all messages relating to the [active] Stack Pointer and Instruction Counter are continuously "looped" until the user halts the board_s operation (see Start Register definition).

The "loop" time or Frame Time is a function of two Control register pairs; the Frame Time Registers (Hi and Lo) and the Frame Time Resolution Registers (Hi and Lo). The internal Frame Time counter is loaded upon receipt of a "START" command with the 16-bit value found within the Frame Time Registers (Hi and Lo). The Frame Time counter is decremented every N x 155 nsec - where N is the value of Frame Time Resolution Registers (Hi and Lo). After the execution of all instructions (1 frame), the EXC-1553PC/E will wait until the internal Frame Time Counter reaches ZERO before re-transmitting the next frame.

NOTE: If the Frame time is less than the time required to transmit all messages [within 1 frame], the subsequent frame will be transmitted with the minimum delay between them. The minimum delay is 120 µsec approximately measured as dead time on the bus.

The user can implement the desired Frame time by programming the appropriate combinations of the two register pairs. An example using one method is illustrated below.

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EXAMPLE: FRAME TIME CALCULATION

Given: User requires a Frame Time of 500msec.

Operation:

Select Frame Time Resolution of 3225 (Dec) ----- 0C99(H).
Frame Time Resolution = 3225 x 155 nsec. = 500 µsec (.5 msec)

Subsequently; the Frame Time Register value must equal to :

(500 msec (desired time) / .5 msec = 1000 (Dec))-1 --> 03E7(H)
Count-1

Load Frame Time Register Lo = E7 (H) (before "START")
Load Frame Time Register Hi = 03 (" ")
Load Frame Time Resolution Register Lo = 99 (Hex) (" ")
Load Frame Time Resolution Register Hi = 0C (before "START")

Note: It is recommended that the user maximize the Resolution Register value vis-a-vis the Frame Time Register value to achieve the greatest possible precision.

MODE CODES

The EXC-1553PC/E handles all Dual-Redundant 1553B Mode Codes. This is to say that the Word Count field is decoded according to MIL-STD-1553B. The two, quad-redundant mode codes, "Selected Transmitter Shutdown" and "Override Selected Transmitter Shutdown" are not implemented by the board.

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PROGRAM EXAMPLE BC/CONCURRENT-RT MODE

```
10 POKE &H3FFF,04      _ LOAD CONFIGURATION REG. = BC/RT MODE
20 POKE &H3FF0,00      _ LOAD STACK POINTER REGISTERS WITH "0000"
30 POKE &H3FF1,00      _ (STACK NOW BEGINS AT ADDRESS:0000)
35 POKE &H3FF2,HFF     _ LOAD VARIABLE AMPLITUDE REGISTER (_-V_ OPTION)

40 POKE &H00,00        _ POINTER TO FIRST MESSAGE (LOCATION OF MESSAGE
50 POKE &H01,01        _ IS 0100(H) )
60 POKE &H02,xx        _ LOAD INTERMESSAGE GAP TIME LOCATION
70 POKE &H03,xx        _

80 POKE &H08,&H40      _ POINTER TO SECOND MESSAGE (LOCATION OF MESSAGE
90 POKE &H09,01        _ IS 0140(H) )
100 POKE &H0A,xx       _ LOAD INTERMESSAGE GAP TIME LOCATION
110 POKE &H0B,xx       _

120 POKE &H100,&H80    _ LOAD CONTROL WORD WITH: TX COMMAND, BUS A,
130 POKE &H101,00      _ AND NO ERRORS INJECTED
140 POKE &H102,&H23    _ LOAD COMMAND WORD: 0C23
150 POKE &H103,&H0C    _

160 POKE &H104,&H00    _ LOAD STATUS WORD: 0800
170 POKE &H105,&H08    _
180 POKE &H106,&Hxx    _ LOAD DATA WORD: xxxx
190 POKE &H107,&Hxx    _
200 POKE &H108,&Hyy    _ LOAD DATA WORD: yyyy
210 POKE &H109,&Hyy    _
220 POKE &H10A,&Hzz    _ LOAD DATA WORD: zzzz
230 POKE &H10B,&Hzz    _

240 POKE &H140,02      _ LOAD CONTROL WORD WITH: RT to RT COMMAND, BUS B,
250 POKE &H141,00      _ AND NO ERRORS INJECTED
260 POKE &H142,&H23    _ LOAD  FIRST [RECEIVE] COMMAND WORD: 3823H
270 POKE &H143,&H38    _
280 POKE &H144,&H43    _ LOAD SECOND [TRANSMIT] COMMAND WORD: 1C43H
290 POKE &H145,&H1C

300 POKE &H3FEB,2      _ LOAD INSTRUCTION COUNTER WITH "2" (2 MESSAGES)

310 POKE &H3FEC,xx     _ LOAD FRAME TIME RESOLUTION REGISTERS
320 POKE &H3FED,xx     _

330 POKE &H3FEE,xx     _ LOAD FRAME TIME REGISTERS
340 POKE &H3FEF,XX     _

                       _ ENABLE RT_s VIA THE ACTIVE RT TABLE.
                       _ BOARD WILL SIMULATE THESE REMOTE TERMINALS
350 POKE &H3401,1      _ ENABLE RT#1

360 POKE &H3FFC,1      _ LOAD START REGISTER WITH "1". STARTS MESSAGE
                         TRANSFERS IN ONE-SHOT MODE.

370 STOP
```


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CONTROL REGISTER DEFINITIONS

RESET INTERRUPT REGISTER 7001(H)

Writing to this register will reset the Interrupt signal to the PC.
The Data field is ignored. This register should be written to at the beginning of a user-written, interrupt service routine.

BOARD RESET REGISTER 7000(H)

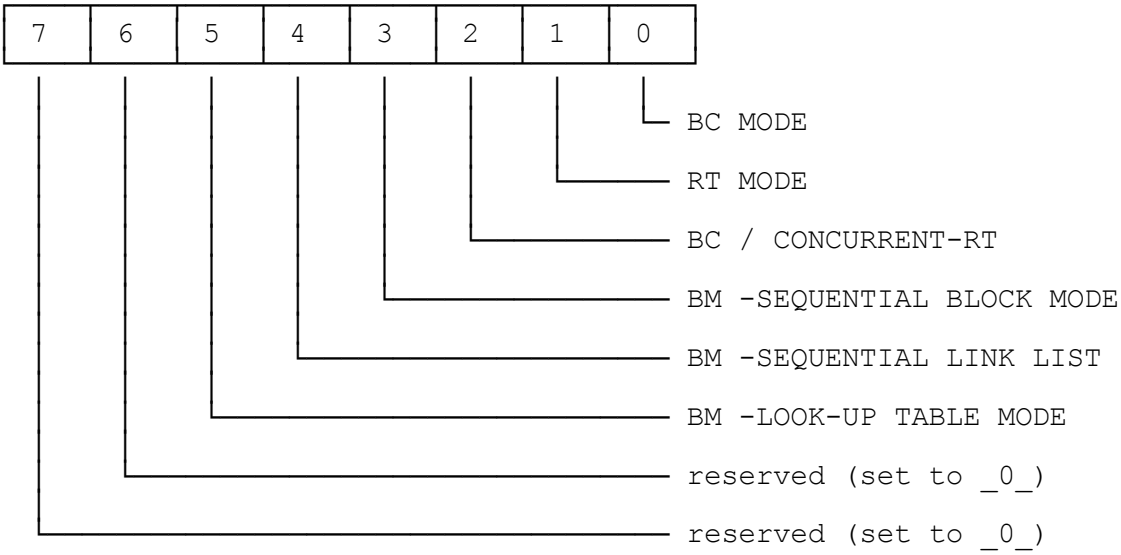
Writing to this location will RESET the EXC-1553PC/E board. The board will act as if POWER had been switched off then on. The data field is ignored.
NOTE: _RESET_ ERASES ALL MEMORY LOCATIONS WITHIN THE DUAL-PORT RAM !!! The Board Status, the Board ID, Firmware Revision and Variable Amplitude registers are written by the board after the reset operation has been completed.

(example: POKE &H7000,xx)

BOARD CONFIGURATION REGISTER 3FFF(H)

* set the desired bit to a logic _1_

The operating mode of the board is set via this register. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).



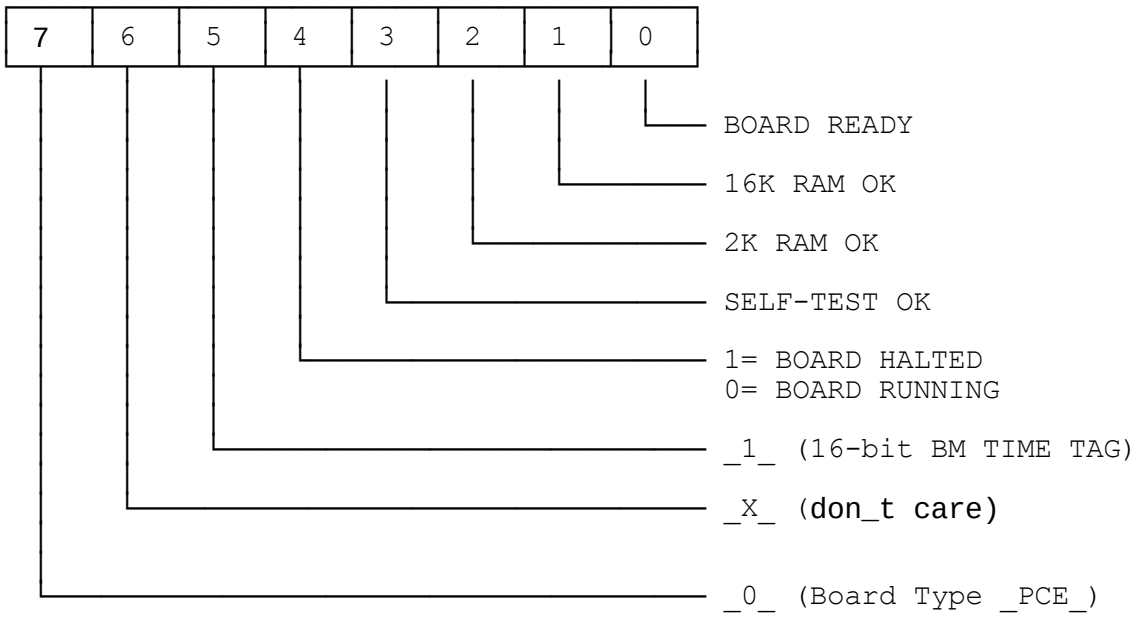
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BOARD ID REGISTER 3FFE(H)

This register contains a fixed value which can be read by a user_s initialization routine to detect the presence of the EXC-1553PC/E card.
The one-byte value of this register is: 45 (Hex) ; ASCII _E_.

BOARD STATUS REGISTER 3FFD(H)

This register indicates the status of the EXC-1553PC/E card. In addition, this register indicates option selection as defined below. (Status bits are active _1_).

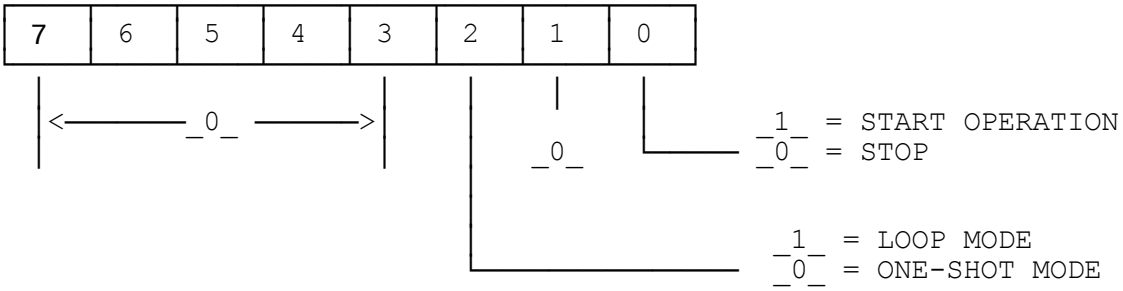


NOTE: Bit "04" (Board Halted) is set by the board after the user "stops" the current operation (by resetting the START bit within the Start Register). The user must check this bit first before modifying registers which first require a "STOP" operation. The board resets this bit after receiving a subsequent START command (by writing to the Start Register). This bit is a new feature available within EPROM revisions starting with 6.5. The condition of this bit after power-on or software reset is a logic "1".

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START REGISTER 3FFC(H)

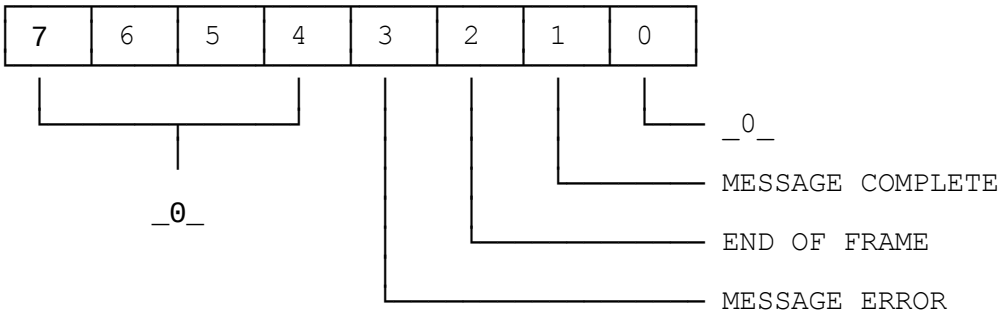
This register controls the _START/STOP_ operation of the EXC-1553PC/E. Writing to this register with the appropriate bit set begins the Bus Controller transfer operation. When operating in the "Loop" or "N Times" mode, the user must set the Start and Loop bits within this register. The "loop" and "N-times" number is selected via the Loop Count Register. In the One-Shot and "N-Times" modes, the board RESETS the Start bit within the register after ALL messages have been transferred. The board does not reset any bit while in the Continuous loop mode. Write "0" to bit "00" to halt the LOOP operation between messages. Write, instead, a "0" to bit "02" in order to halt the operation at the end of the entire frame (this bit is not tested between message transfers). See the related bit (data bit "04") within the Board Status Register which indicates when the board has been halted.



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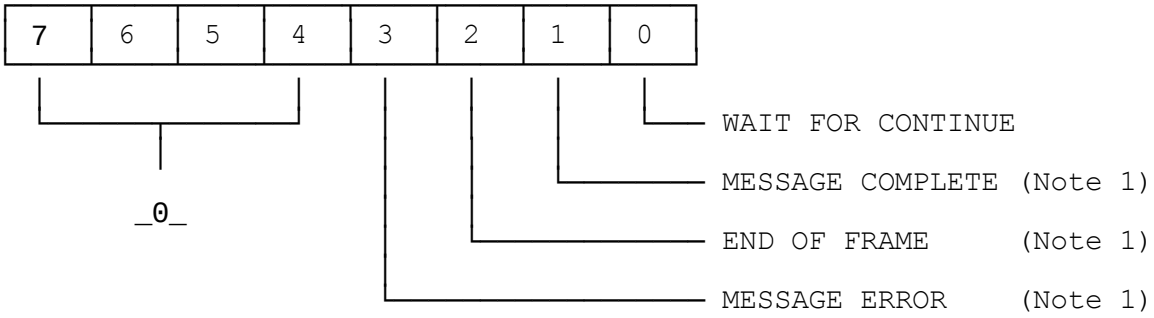
INTERRUPT CONDITION REGISTER 3FFB(H)

This register allows the user to set different interrupt triggers. When a condition that has been enabled within this register occurs, an interrupt will be generated. The user may check the Message Status Register to determine which condition caused the interrupt. A logic _1_ enables the interrupt condition. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).



MESSAGE STATUS REGISTER 3FFA(H)

This register indicates the status of the EXC-1553PC/E card. The figure below illustrates the definition of each Status bit. A logic _1_ indicates active condition.



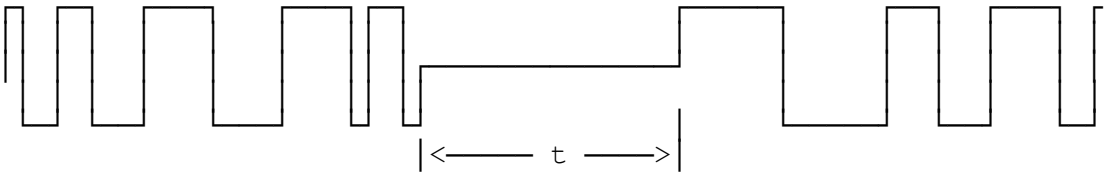
WAIT FOR CONTINUE - A message with the halt bit set has been encountered. The user must reset the halt bit in the Control word to continue.
MESSAGE COMPLET - The last word of a message has been sent
END OF FRAME - The last word of the last message in a frame has been sent
MESSAGE ERROR - A message has been sent resulting in the error bit being set in the Message Status Word

Notes: 1) Status Bits are NOT reset by the board !

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RT RESPONSE TIME REGISTER 3FF9(H)

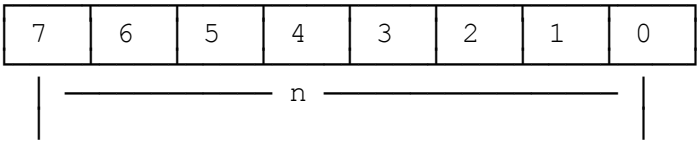
This register sets the RESPONSE TIME of the Remote Terminal. The resolution of this register is 155 nsec. per bit. This time is measured as the "DEAD TIME" on the 1553 bus. The minimum time is equal to approximately 4 µsec. The value in the register is ADDED to the minimum time. The actual Response Time will be ±1µsec tolerance. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).



Example: To set up a RT response time of 9µsec, write 32 to this register;
32 * 0.155 = ~5µsec + 4µsec = 9µsec

LOOP COUNT REGISTER 3FF6(H)

This register is used in conjunction with the Loop Bit in the Start Register. If that bit is set, the user sets this register to specify the number of times the Message Frame will be transmitted. A value of zero is interpreted as a request for continuous looping. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).



Value = 0 : Transmits in continuous loop
Value = 1-255 : Sends message frame _n_ times (1 to 255) as defined

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BIT COUNT REGISTER 3FF5(H)

Sets the number of total bits within the 1553 word ; including Sync(3) and Parity(1). When NO error is selected (see: Control Word), this register is ignored (20-bit word is selected). This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

7	6	5	4	3	2	1	0	# of bits	
<————				_0_			———>		
					0	0	0	17	-3
					0	0	1	18	-2
					0	1	0	19	-1
					0	1	1	20	
					1	0	0	21	+1
					1	0	1	22	+2
					1	1	0	23	+3

WORD COUNT REGISTER 3FF4(H)

This register controls the number of 1553 words (+/- 3) within the message. The variation is relative to the 1553 Command Word_s WORD COUNT FIELD. The "resulting" message must contain at least ONE 1553 Data Word. When NO error is selected (see: Control Word), this register is ignored. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

7	6	5	4	3	2	1	0
<————			see	table			————>

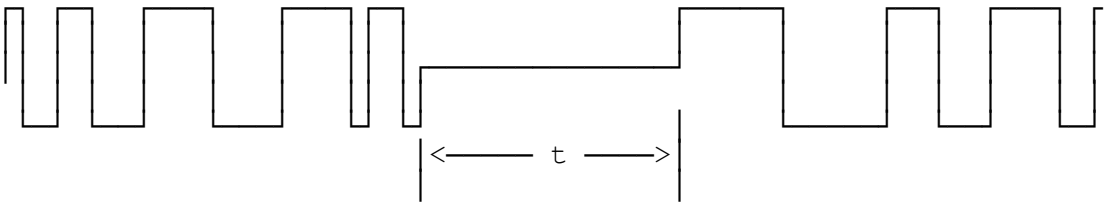
(No Word Count Error injected) -

-3	FD (H)
-2	FE (H)
-1	FF (H)
0	00 (H)
+1	01 (H)
+2	02 (H)
+3	03 (H)

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BC RESPONSE TIME REGISTER 3FF3(H)

This register sets the Bus Controller_s RESPONSE TIME WINDOW. This value determines the maximum [wait] time until an RT_s Status Response is considered "INVALID" by the BC. The resolution of this register is 155 nsec. per bit. This time is measured as the "DEAD TIME" on the 1553 bus. The minimum time is approx. 2 µsec. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).



Example: To set up a BC response time of 14µsec, write a 90 to this register; 90 * 0.155 = ~14µsec

VARIABLE AMPLITUDE REGISTER 3FF2(H) (_-V_ Option)

This register specifies the amplitude of the 1553 output signal. The signal can be programmed from 0 volts up to 7.5volts (p-p) - measured on the 1553 bus with specified 1553 coupling and 35ohm load (two 70 ohm termination resistors were used). A higher Transmit [output] amplitude will appear on the 1553 bus if 78 ohm termination resistors are used. The register has a resolution of 30mv/bit (p-p) on the bus. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register). For EPROM Revisions 6.5 and above this register defaults to FFH after Reset, providing maximum amplitude.

STACK POINTER - HI & LO 3FF1, 3FF0(H)

The Stack Pointer points to the Instruction Stack. The Instruction Stack can reside anywhere within locations 0000(H) and 33FF(H). This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

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FRAME TIME REGISTERS - HI & LO 3FEF, 3FEE(H)

These registers contain the 16-bit Frame Time Value for Continuous and N-times Modes Operation. The value written to this register is multiplied by the value set within the Frame Time Resolution Registers pair described below. The value set must be equal to the desired multiplication factor -1. See: CONTINUOUS or ONE-SHOT MESSAGE TRANSFERS described above. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

FRAME TIME RESOLUTION REGISTER - HI & LO 3FED, 3FEC(H)

This 16-bit value represents the resolution of the Frame Time Counter in increments of 155 nsec. See CONTINUOUS or ONE-SHOT MESSAGE TRANSFERS described above. The _HI_ register contains the MSB , the _LO_ register contains the LSB. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

INSTRUCTION COUNTER 3FEB(H)

The Instruction Counter is loaded with the number of instructions (1553 Messages) to execute in the current frame. The value must be greater than _0_ before beginning transmission (by writing to the _START REGISTER_). Load _1_ for one message, _2_ for two messages, etc. The EXC-1553PC/E updates this register by decrementing the value and writing it back to the memory at the end of each message transfer. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register). When in the "loop mode", this register cycles from the initial value to "0" for the first frame. Subsequent frames have this register cycle from the "initial value -1" down to "0" instead of from the initial value.

FIRMWARE REVISION REGISTER 3E80(H)

This register indicates the revision level of the on-board firmware. The value 0110 0011 would be read as revision level: 6.3

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BUS MONITOR OPERATION

The Bus Monitor can operate in two basic modes of operation. The first is the sequential mode - whereby 1553 Message Blocks are stored in sequential locations within memory. This mode includes two methods of operation. The first is called the FIXED BLOCK operation because the 1553 messages are stored at "fixed" sequential blocks within the memory. The second is called the LINK-LIST operation whereby the 1553 messages are "packed" one after another within the memory - separated by a header. Trigger capability is available within the Sequential Fixed Block Mode.

The second mode of operation utilizes a Look-Up table approach. In this mode, each 1553 message can be stored in a unique Message Block. The user-programmable Look-Up table is addressed by the EXC-1553PC/E upon receipt of a 1553 Command Word. The Command Word_s RT Address, T/R bit, and Subaddress fields make up the 11-bit pointer to the Look-Up table. This equates to a table totalling 2048 locations. The desired mode of operation is programmed via the Configuration Register.

The board will record properly messages received with an intermessage gap of greater than 10µsec, measured as dead time on the bus. In addition the minimum intermessage gap time between a broadcast message and the subsequent 1553 command is 35µsec.

NOTE:

The user should use the following sequence to determine whether the board is installed AND ready to operate:

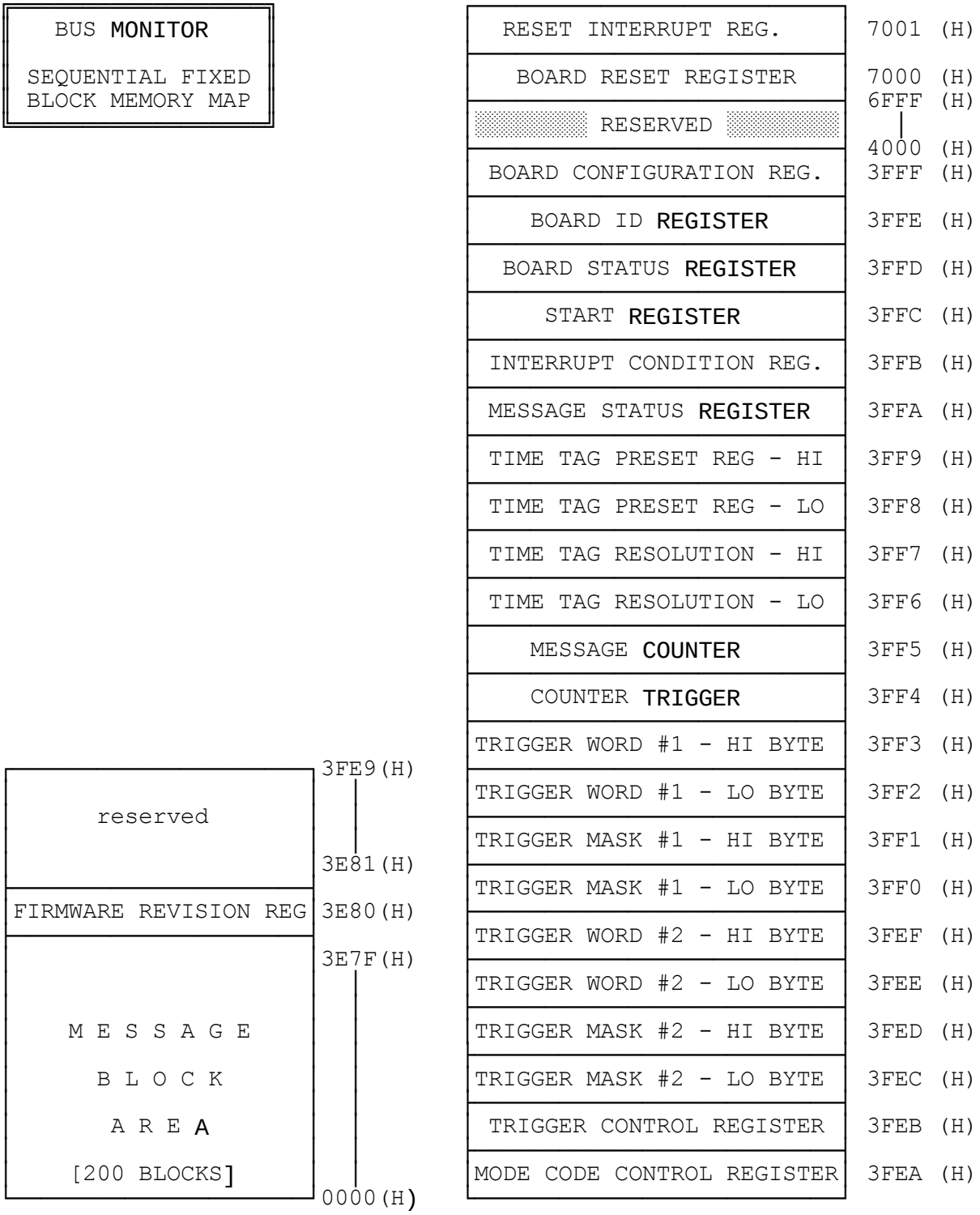
* Check the Board ID register (test for value = 45 Hex)
* Check Board Status Register (test for Board Ready bit = _1_)

The board is installed and ready when BOTH of these registers contain the correct values (as written above). This sequence should be used after power-on and software reset operations. For Software Reset operations; these values should be set to ZERO by the user immediately prior to writing to the [software] Board Reset Register.

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BUS **MONITOR**

SEQUENTIAL FIXED BLOCK MEMORY MAP

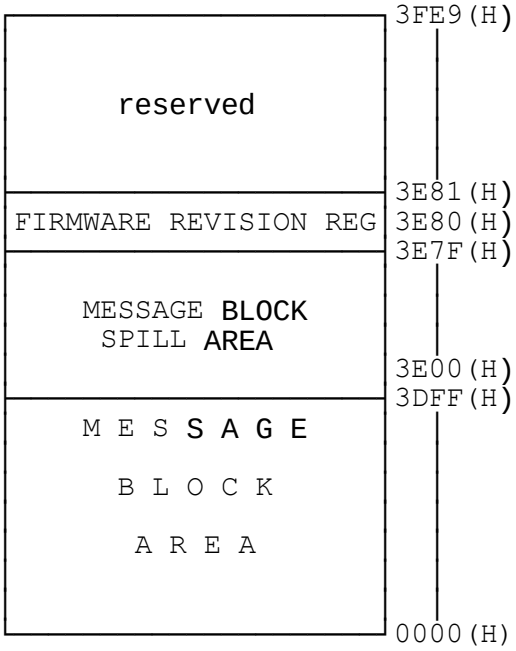


BM

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BUS **MONITOR**

SEQUANTIAL LINK
LIST MEMORY MAP



RESET INTERRUPT REG.	7001 (H)
BOARD RESET REGISTER	7000 (H)
RESERVED	6FFF (H) — 4000 (H)
BOARD CONFIGURATION REG.	3FFF (H)
BOARD ID **REGISTER**	3FFE (H)
BOARD STATUS **REGISTER**	3FFD (H)
START **REGISTER**	3FFC (H)
INTERRUPT CONDITION REG.	3FFB (H)
MESSAGE STATUS **REGISTER**	3FFA (H)
TIME TAG PRESET REG - HI	3FF9 (H)
TIME TAG PRESET REG - LO	3FF8 (H)
TIME TAG RESOLUTION - HI	3FF7 (H)
TIME TAG RESOLUTION - LO	3FF6 (H)
reserved	3FF5 (H)
reserved	3FF4 (H)
reserved	3FF3 (H)
reserved	3FF2 (H)
reserved	3FF1 (H)
reserved	3FF0 (H)
reserved	3FEF (H)
reserved	3FEE (H)
reserved	3FED (H)
reserved	3FEC (H)
reserved	3FEB (H)
MODE CODE CONTROL REGISTER	3FEA (H)

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SEQUENTIAL MODES

SEQUENTIAL MODES: MESSAGE BLOCK AREA

The Message Block Area is partitioned into either blocks of fixed length or into a _LINK LIST_ organized memory. The partitioning is determined by the Configuration Register.

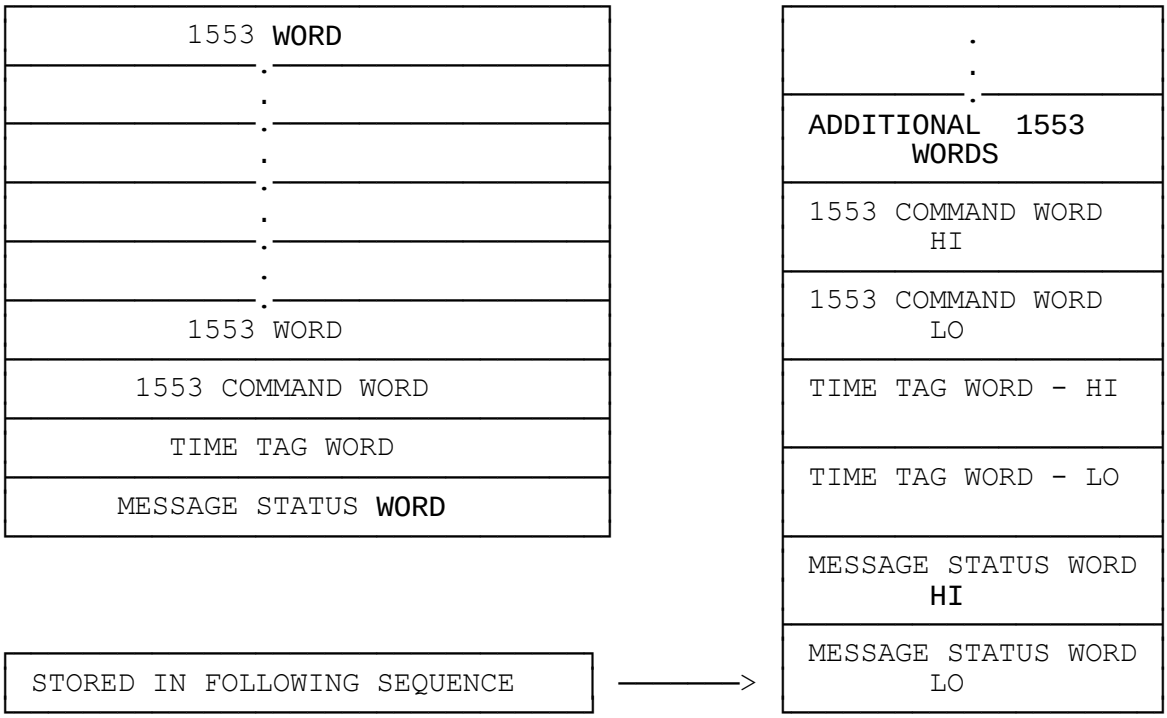
FIXED BLOCK OPERATION

In this mode, the Message Block Area is divided into 200 blocks - each consisting of 80 bytes. The first block starts at address 0000(H), the second at 0050(H),the third at 00A0(H), etc. The Trigger option can be used in this mode only (see Trigger Operation).

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BUS MONITOR MESSAGE BLOCK FIXED BLOCK MODE

The figure below illustrates the contents of the Message Block:



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In this mode, the Message Block Area appears to be one continuous block of data. The first two locations within the memory form the Message HEADER. This header contains the address of the NEXT Message Block Header. The Header of the LAST 1553 block received will contain _XXFF_("End of File") indicating that no more messages have been stored.

After each message has been processed and stored in memory, the HEADER of the preceding message block will be updated from _XXFF_ to the address of the newly stored message (points to the Header within the block). This method allows for the storage of more data than can be realized using the fixed-block mode of operation.

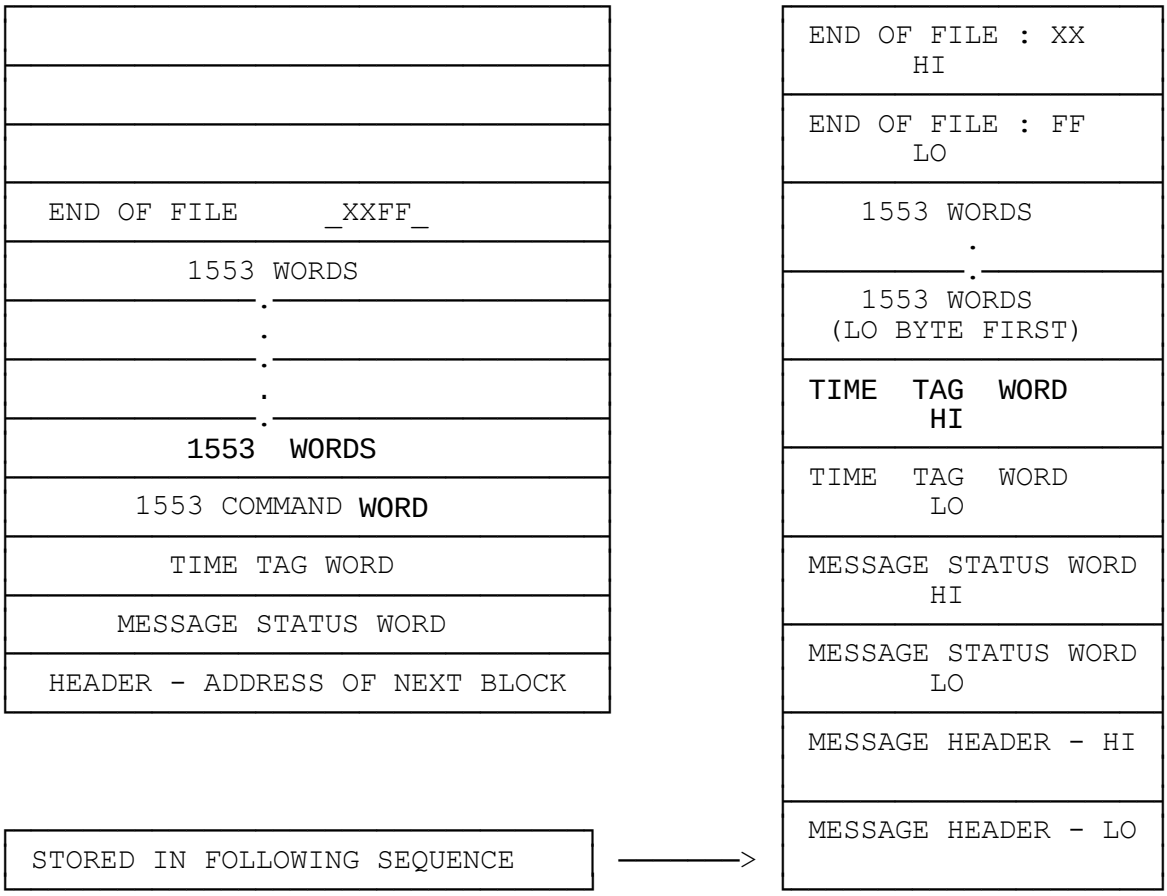
Special care is to be taken with the message appearing at the end of the Message Block Area. Since the buffer never wraps around in mid message and a message may start at any address up to 3DFEH, the final message in the buffer may extend passed the end of the standard Message Block Area into the Message Block Spill Area. The next message will start at the first location of the Message Block Area (0000H).

The figure below illustrates the contents of the Message Block:

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BUS MONITOR MESSAGE BLOCK

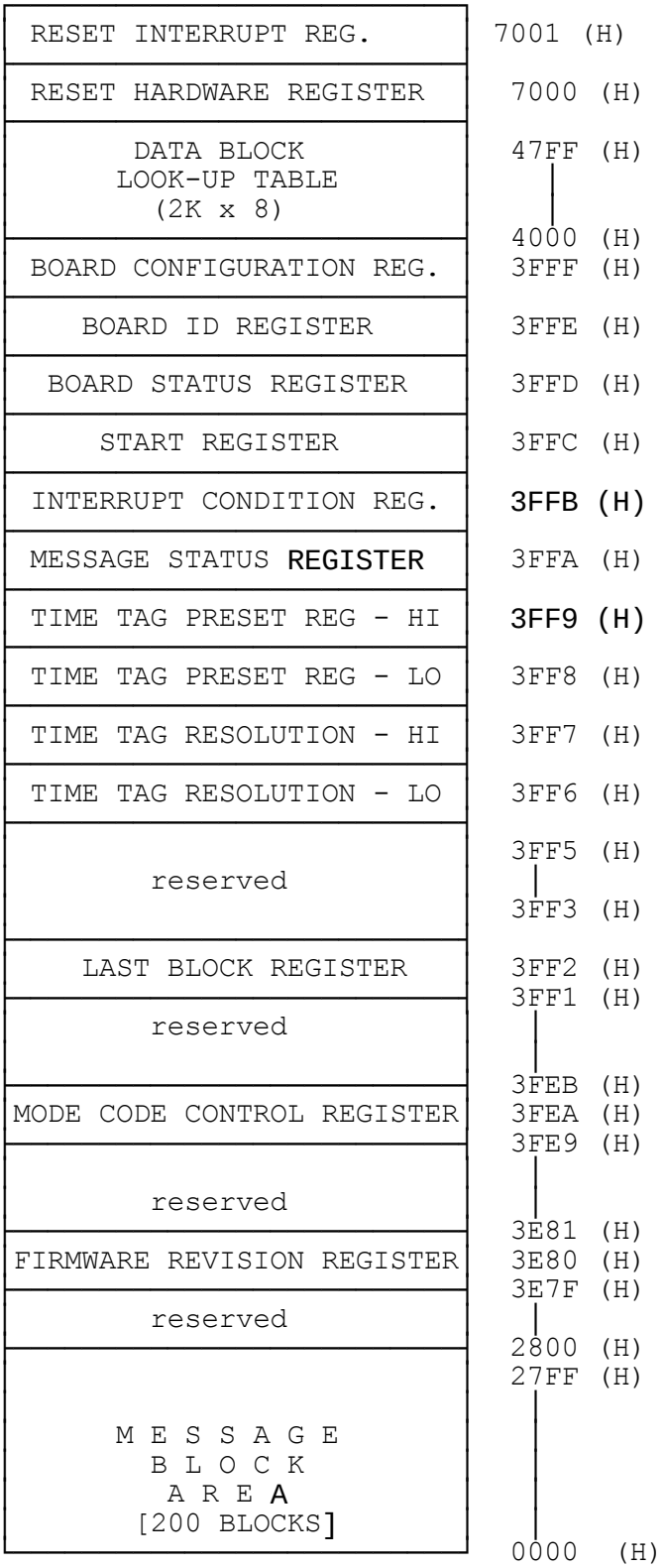
LINK-LIST MODE



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BUS **MONITOR**

LOOK-UP TABLE
MEMORY MAP

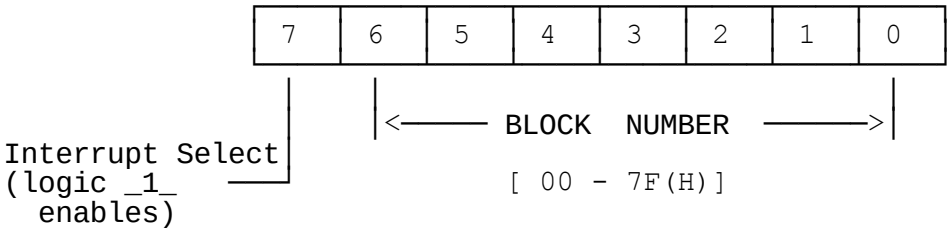


BM

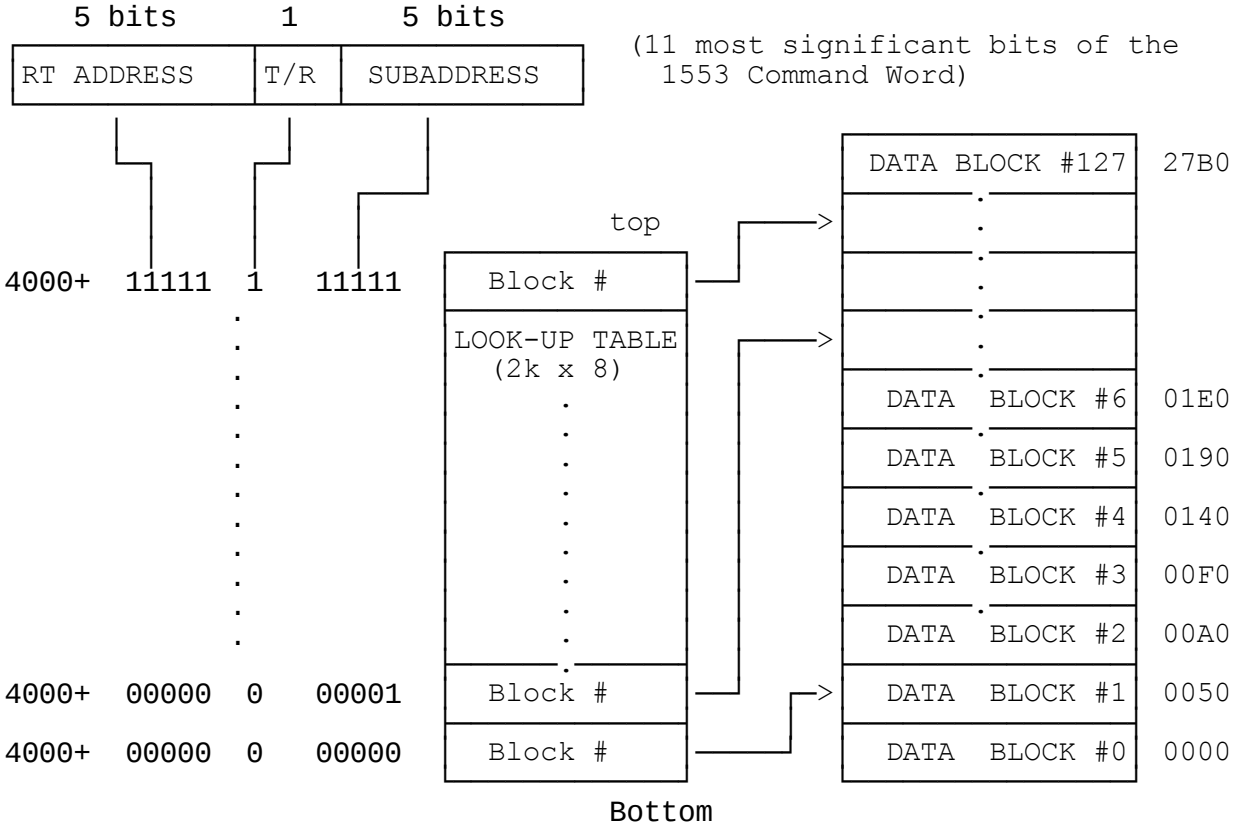
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LOOK-UP TABLE OPERATION

In this mode of operation, the EXC-1553PC/E can store 128 unique messages. This is accomplished via a 2k x 8 Look-Up Table within the on-board memory. Each [table] byte is divided into a 7-bit Block Number and an Interrupt Select bit as shown below. The table is loaded with Data Block Numbers (0-127 decimal) each consisting of 80 bytes. The first block starts at address 0, the second at 50H, etc. The user can select which messages will set the interrupt flag via the Interrupt Select bit. The Interrupt Condition register must also be programmed.



When a 1553 message is received, the Command Word_s RT Address, T/R bit and Subaddress fields are used as an 11-bit index to the look-up table. This index is used to extract the Data Block Number from the look-up table.



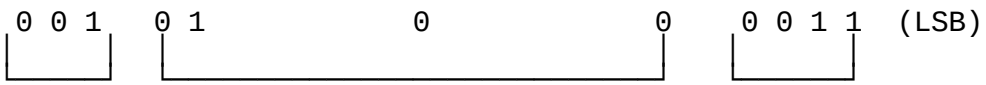
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HOW TO CREATE THE ADDRESS TO THE TABLE

1. Isolate the ELEVEN (most significant) bits of the 1553 Command Word
   (RT Address, T/R, and Subaddress Field).

Example:

RT Address = 5 T/R= 0 (RCV) Subaddress = 3



The Hex representation = 143 (H)

2. Add this value to the base address of the Look-Up Table (4000H).

```
    4000 (H)
 +   143 (H)
-------------
    4143 (H)
```

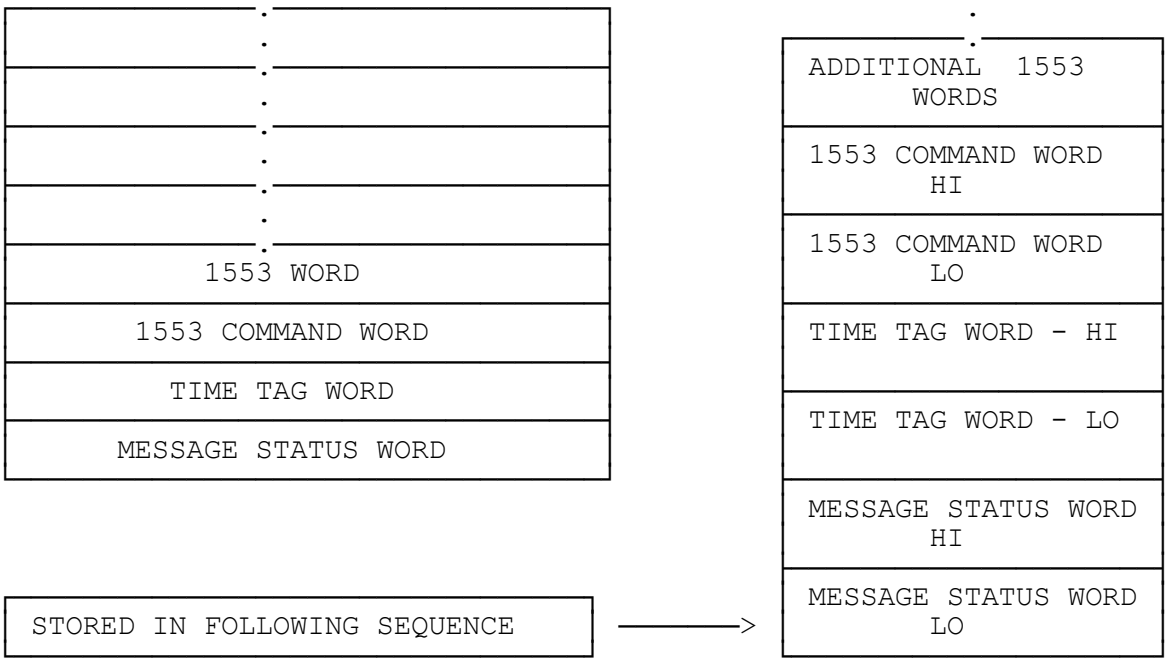
3. Write Data Block number to this location

(i.e. POKE &H4143,xx writes an 8-bit (Block Number) value to the
Look-up Table address: &H4143)

Block #0 is located at address 0000H
Block #1 is located at address 0050H
The location of the block is obtained by multiplying the block number by 50(H).

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The figure below illustrates the contents of the Message Block:

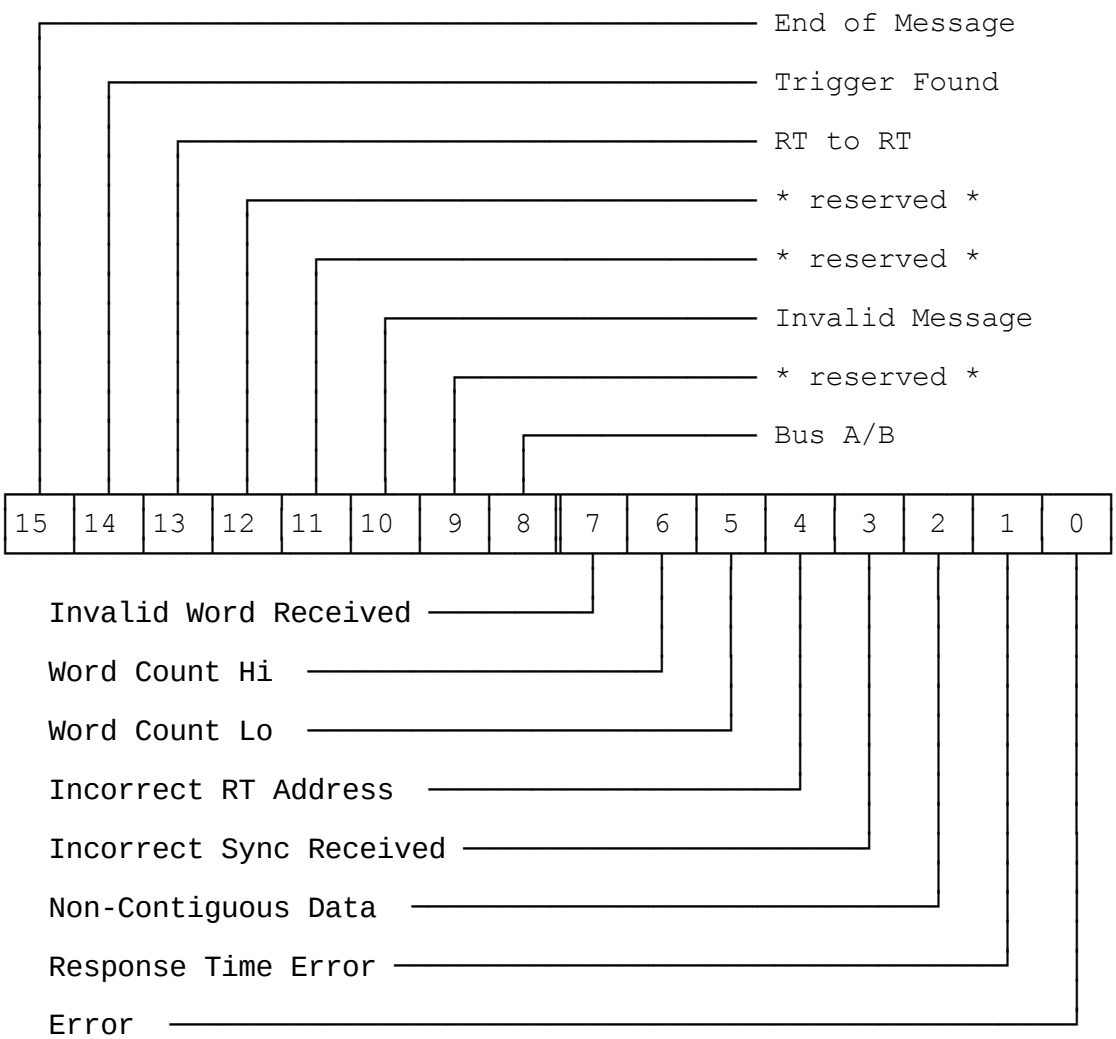


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MESSAGE STATUS WORD

Note: For ALL Modes

The Message Status Word indicates the status of the message transfer. This word is created by the Board and is NOT the 1553 "STATUS WORD".
The format of the Message Status word is shown below:



NOTE: A LOGIC _1_ INDICATES OCCURRENCE OF STATUS FLAG

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Message Status Word Definitions:

15	End of Message	INDICATES THAT THE MESSAGE TRANSFER HAS BEEN COMPLETED
14	Trigger Found *	INDICATES RECEPTION AND STORAGE OF TRIGGER MESSAGE. VALID FOR SEQUENTIAL FIXED BLOCK MODE WITH _STORE AFTER_ AND _STORE ONLY_ OPERATIONS (see note below)
13	RT to RT	INDICATES RECEPTION OF A RT to RT MESSAGE
12	Reserved	SET TO LOGIC _0_
11	Reserved	SET TO LOGIC _0_
10	Invalid Message	INDICATES THAT A 1553 _MESSAGE LEVEL_ ERROR OCCURRED (i.e. Word Count, Incorrect Sync) - detailed below
09	Reserved	SET TO LOGIC _0_
08	Bus A/B	INDICATES ON WHICH BUS THE MESSAGE WAS TRANSFERRED. _0_ = Bus B; _1_ = Bus A
07	Invalid Word	INDICATES THE RECEPTION OF AT LEAST ONE INVALID 1553 WORD (i.e. Bit Count, Manchester code, Parity)
06	Word Ct Hi	INDICATES THAT THE RT TRANSMITTED TOO MANY WORDS
05	Word Ct Lo	INDICATES THAT THE RT TRANSMITTED TOO FEW WORDS
04	Incorrect RT Addr.	INDICATES THAT THE RECEIVED 1553 STATUS WORD DID NOT CONTAIN THE CORRECT _RT ADDRESS_
03	Incorrect Sync	INDICATES THAT THE SYNC OF EITHER THE STATUS OR DATA WORD(s) WAS INCORRECT
02	Non-Contiguous	INDICATES OCCURRENCE OF AN INVALID GAP BETWEEN RECEIVED 1553 WORDS
01	Response Time Err	INDICATES A RESPONSE TIME ERROR HAS OCCURRED WITHIN THE MESSAGE. THIS BIT WILL ALSO BE ACTIVE FOR A BROADCAST COMMAND AND SHOULD BE IGNORED TOGETHER WITH THE ERROR BIT
00	ERROR	INDICATES THE OCCURRENCE OF AN ERROR (DEFINED WITHIN ONE OF THE OTHER MESSAGE STATUS BIT LOCATIONS)

* Note: Trigger Found (Bit 14)
STORE ONLY MODE - Each Trigger Message will have this bit set.
STORE AFTER MODE - ONLY FIRST Trigger Message will have this bit set.

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Time Tag	(Read by user)

The Time Tag Value is a 16-bit word which may be used to determine the time elapsed since _START_ or to determine the time between the 1553 messages. The internal Time Tag counter is loaded upon receipt of a "START" command with the 16-bit value found within the "Time Tag Preset Registers" (Hi and Lo). The Time Tag counter is incremented every "N x 155 nsec". - where N is the value of "Time Tag Resolution Registers" (Hi and Lo).

EXAMPLE:

Given:

```
 Time Tag Preset Register Lo = 00            (initialized before "START")
 Time Tag Preset Register Hi = 00            (      "       "       "   )
 Time Tag Resolution Register Lo = 0C (H)    (      "       "       "   )
 Time Tag Resolution Register Hi = 00        (initialized before "START")

 Time Tag Value Lo = 40 (Hex)                (value read during or after
 Time Tag Value Hi = 10 (Hex)                 message transfers)

Time Elapsed (since "START"):    1040 (Hex)  *  ( 000C(Hex) * 155 nsec.)=
                                   4160 (dec)  *  ( 12  * 155 nsec)=
                                                  =  7737 µsec
                                                  =  7.73  msec.
```


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TRIGGER OPERATION

SEQUENTIAL FIXED BLOCK MODE ONLY

The EXC-1553PC/E can be programmed to store messages in the following manner:

1. STORE ALL (STORES ALL 1553 MESSAGES-NO TRIGGERS ACTIVE)
2. STORE ONLY (ONLY MESSAGES WHICH MEET THE TRIGGER CONDITION)
3. STORE AFTER (AFTER RECEIPT OF A TRIGGER MESSAGE - STORES TRIGGER MESSAGE, too)

The user can define up to 2 triggers. Each trigger is defined using two registers: the TRIGGER WORD and TRIGGER MASK registers. The TRIGGER WORD register defines a 1553 Command Word value or a Message Status Word value which triggers storage as defined above, while the TRIGGER MASK register allows the user to define which bit(s) of the TRIGGER WORD are relevant or are to be ignored ("Don_t Care"). See detailed description within the Control Register section below).

In this way, the user can define a trigger as being a unique 1553 message (by using the 1553 Command Word as the trigger) or via the status of the message (by using the Message Status word). Using the Message Status Word as the trigger source allows for storage of, for example, all messages on Bus A, or only messages with errors, or messages with errors received over Bus B, etc.

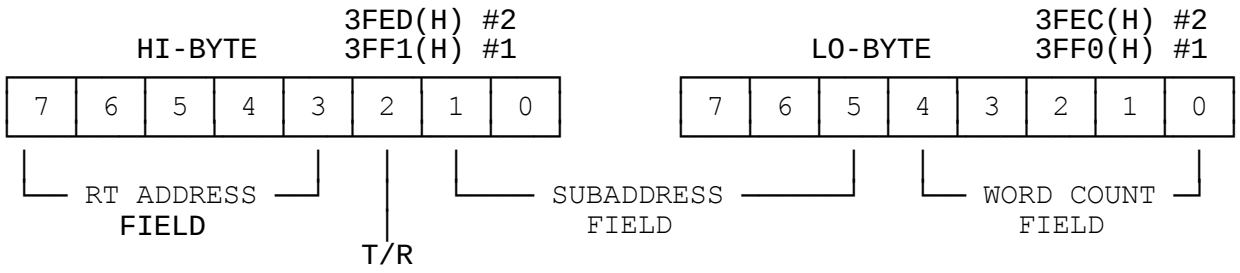
The trigger source, mode and conditions are set via the TRIGGER CONTROL REGISTER (see Control Register Definitions). The Trigger Word and Mask Registers must be written before issuing a START to the board. To modify these registers, the user must first set the "Initialize" bit within the START Register (10H), modify the registers and then issue a "START" (01H).

The user can define which trigger is active (Trigger #1, Trigger #2, or BOTH) via the Trigger Control Register. The Trigger Mask Registers (see below) MUST be defined when using the trigger function.

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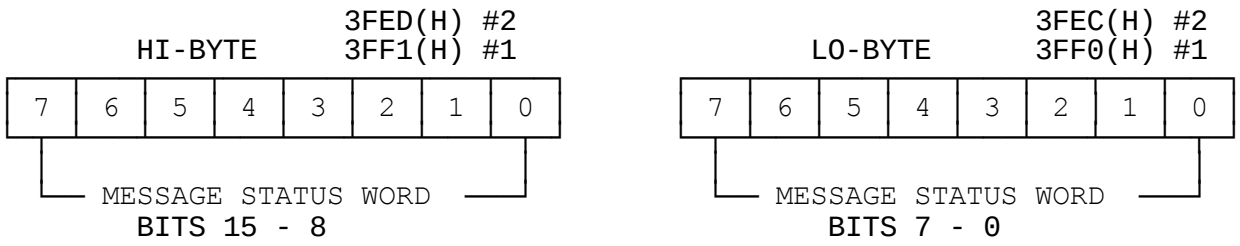
TRIGGER MASK REGISTERS (1 and 2)

USING THE 1553 COMMAND WORD



1 = Use Value From Trigger Word Register
0 = Don_t Care

USING THE MESSAGE STATUS WORD

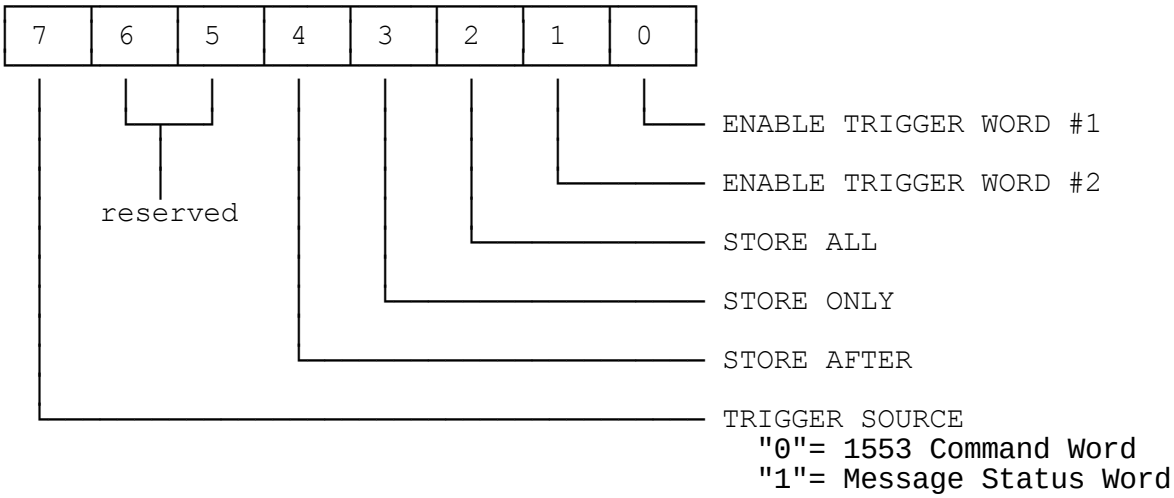


See the definition of the Message Status Word described in this section.

1 = Use Value From Trigger Word Register
0 = Don_t Care

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TRIGGER CONTROL REGISTER	3FEB(H)	SEQUENTIAL FIXED BLOCK MODE ONLY



Notes:

1. A logic "1" selects function
2. The Trigger Source selection bit (Command or Message Status Word) is available in EPROM revisions 6.5 and above. This bit is not used in earlier revisions.

EXAMPLE:

User defines the Command Word _0825_(H) as Trigger Word #1 (Receive Command for RT#1 , Subaddress #1 and 5 words) but selects to ignore the Word Count Field and disables Trigger Word #2. In addition, the user wants to store only message type(s) defined by Trigger Word #1.

Load Trigger Word-Hi Register #1 with the Value : 08 (Hex)
Load Trigger Word-Lo Register #1 with the Value : 25 (Hex)
Load Trigger Mask-Hi Register #1 with the Value : FF (Hex)
Load Trigger Mask-Lo Register #1 with the Value : E0 (Hex)
Load Trigger Control Register with the Value : 09 (Hex)

Note: ONE of the bits; Store All, Store Only, Store After MUST be set if Trigger(s) are utilized.

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PROGRAM EXAMPLE — BUS MONITOR SEQUENTIAL FIXED BLOCK MODE

```
10 POKE &H3FFF,08       _ LOAD CONFIGURATION REG; BM SEQ BLOCK MODE

20 POKE &H3FF6,xx       _ LOAD TIME TAG RESOLUTION REG LO; xx
30 POKE &H3FF7,xx       _ LOAD TIME TAG RESOLUTION REG HI; xx
40 POKE &H3FF8,00       _ LOAD TIME TAG PRESET REGISTER LO; 00
50 POKE &H3FF9,00       _ LOAD TIME TAG PRESET REGISTER HI; 00
```

(See example above regarding the use of Triggers)

```
60 POKE &H3FF0,xx         _ LOAD TRIGGER MASK #1 ; LO :xx
70 POKE &H3FF1,xx         _ LOAD TRIGGER MASK #1 ; HI :xx
80 POKE &H3FF2,xx         _ LOAD TRIGGER WORD #1 ; LO :xx
90 POKE &H3FF3,xx         _ LOAD TRIGGER WORD #1 ; HI :xx
100 POKE &H3FEB,xx        _ LOAD TRIGGER CONTROL REGISTER

110 POKE &H3FEA,00        _ LOAD MODE CODE CONTROL REG; 1_s AND 0_s

120 POKE &H3FFC,01        _ START
```

Note: Messages are read from memory starting from address _0000_.

PROGRAM EXAMPLE — BUS MONITOR SEQUENTIAL LINK LIST MODE

```
10 POKE &H3FFF,&H10     _ LOAD CONFIGURATION REG; BM LINK-LIST MODE

20 POKE &H3FF6,xx       _ LOAD TIME TAG RESOLUTION REG LO; xx
30 POKE &H3FF7,xx       _ LOAD TIME TAG RESOLUTION REG HI; xx
40 POKE &H3FF8,00       _ LOAD TIME TAG PRESET REGISTER LO; 00
50 POKE &H3FF9,00       _ LOAD TIME TAG PRESET REGISTER HI; 00

110 POKE &H3FEA,00      _ LOAD MODE CODE CONTROL REG; 1_s  AND  0_s

120 POKE &H3FFC,01      _ START
```

Note: Messages are read from memory starting from address _0000_.

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PROGRAM EXAMPLE — BUS MONITOR LOOK-UP TABLE MODE

```
10 POKE &H3FFF,&H20    _ LOAD CONFIGURATION REG; BM LOOK-UP TABLE

20 POKE &H3FF6,xx      _ LOAD TIME TAG RESOLUTION REG LO; xx
30 POKE &H3FF7,xx      _ LOAD TIME TAG RESOLUTION REG HI; xx
40 POKE &H3FF8,00      _ LOAD TIME TAG PRESET REGISTER LO; 00
50 POKE &H3FF9,00      _ LOAD TIME TAG PRESET REGISTER HI; 00
60 POKE &H3FEA,00      _ LOAD MODE CODE CONTROL REG; 1_s  AND  0_s

70 POKE &H4143,00      _ SETUP LOOK-UP TABLE: RT5/RCV/SA3 to BLK0
80 POKE &H4144,01      _ SETUP LOOK-UP TABLE: RT5/RCV/SA4 to BLK1

90 POKE &H3FFC,01      _ START
```

Note: Messages are read from memory according to address pointer derived from Command Word - see example in the section "Look-Up Table Operation".

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CONTROL REGISTER DEFINITIONS

RESET INTERRUPT REGISTER 7001(H)

Writing to this register will reset the Interrupt signal to the computer. The Data field is ignored. This register should be written to at the beginning of a user-written, interrupt service routine.

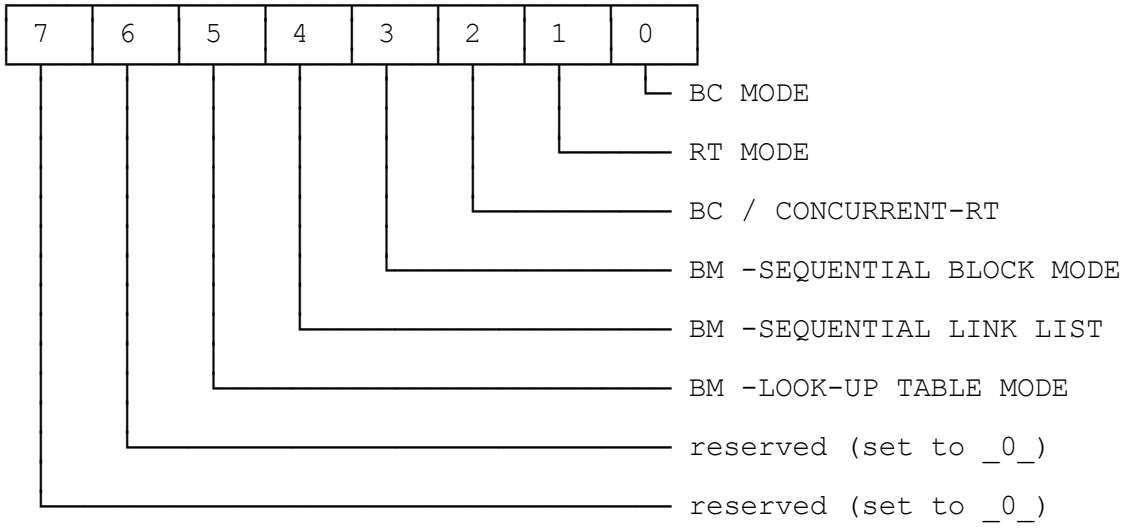
BOARD RESET REGISTER 7000(H)

Writing to this location will RESET the EXC-1553PC/E board. The board will act as if POWER had been switched off then on. The data field is ignored.
NOTE: _RESET_ ERASES ALL MEMORY LOCATIONS WITHIN THE DUAL-PORT RAM !!! The Board Status, the Board ID and Firmware Revision registers are written by the board after the reset operation has been completed (ex.: POKE &H7000,xx).

BOARD CONFIGURATION REGISTER 3FFF(H)

Set the desired bit to a logic _1_

The operating mode of the board is set via this register. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).



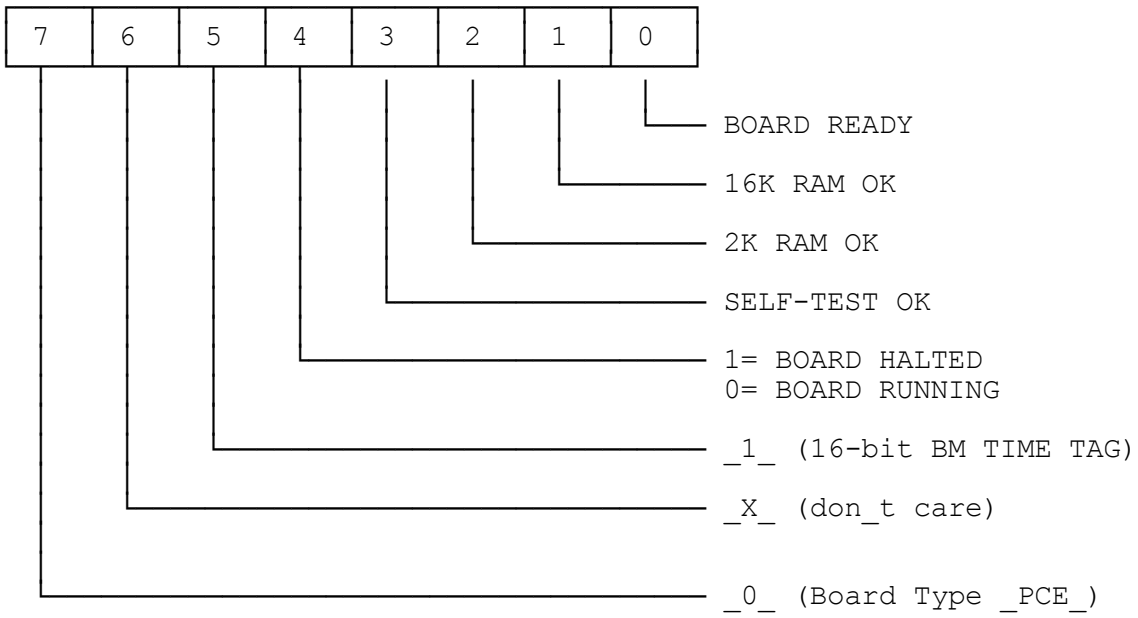
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BOARD ID REGISTER 3FFE(H)

This register contains a fixed value which can be read by a user_s initialization routine to detect the presence of the EXC-1553PC/E card.
The one-byte value of this register is: 45 (Hex) ; ASCII _E_.

BOARD STATUS REGISTER 3FFD(H)

This register indicates the status of the EXC-1553PC/E card. In addition, this register indicates option selection as defined below. (Status bits are active _1_).



NOTE: Bit "04" (Board Halted) is set by the board after the user "stops" the current operation (by resetting the START bit within the Start Register). The user must check this bit first before modifying registers which first require a "STOP" operation. The board resets this bit after receiving a subsequent START command (by writing to the Start Register). This bit is a new feature available within EPROM revisions starting with 6.5. The condition of this bit after power-on or software reset is a logic "1".

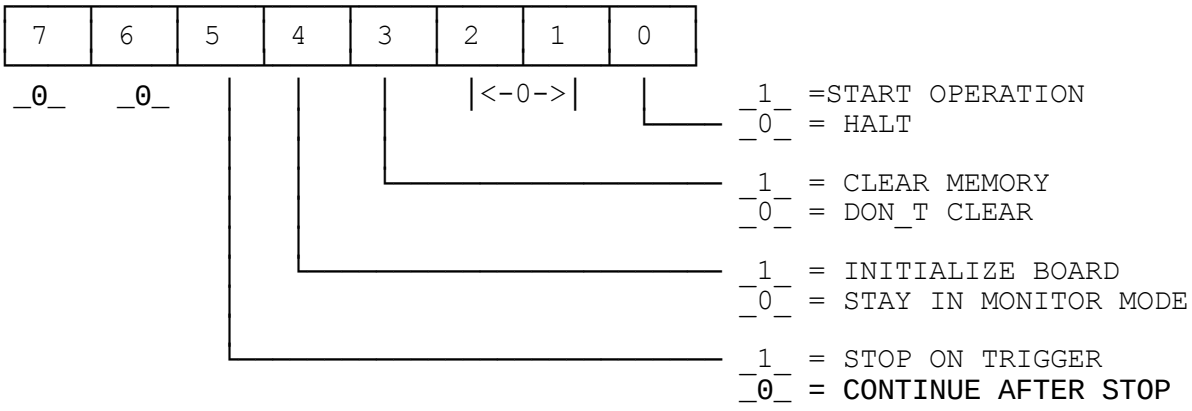
This bit is set on two conditions:

A) when a HALT is issued (set bit "00" of Start Register to a logic "0").
B) when an INITIALIZE BOARD is issued (see START REGISTER)

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START REGISTER 3FFC(H)

This register controls the _START / HALT_ operation of the EXC-1553PC/E. See the related bit (data bit "04") within the Board Status Register which indicates when the board has been halted. Writing to this register with the appropriate bit set executes one of the functions as listed below:



NOTES:

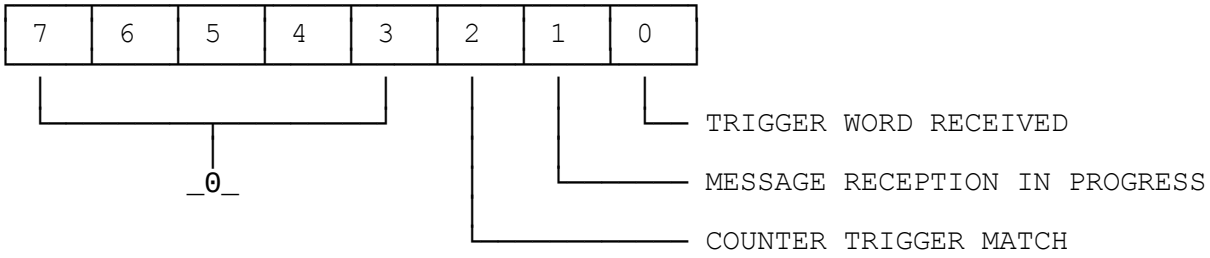
1. The "Clear Memory" and "Initialize Board" bits are tested by the EXC-1553PC/E board only when the "Start/Halt" bit is _0_. The "Clear Memory" function clears the 1553 message Blocks and all "readable" control registers. The "Initialize Board" function enables the user to re-initialize the board, change the board_s mode of operation (modify the Configuration Register) and start [again]. Monitor modes of operation can not be switched by "stopping" and "starting" the board (START/HALT bit) without also setting the Initialize Board bit.

2. The STOP ON TRIGGER/CONTINUE bit is used in the Sequential Fixed Block Mode ONLY. This bit is tested when the Message Counter equals the Message Counter Trigger. The board will stop storage of 1553 messages if this bit is then a _1_. Setting this bit to a _0_ will then allow the board to continue monitoring operations. You must first "continue" before "HALTING" the board (setting START/HALT bit to a _0_)

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INTERRUPT CONDITION REGISTER 3FFB(H)

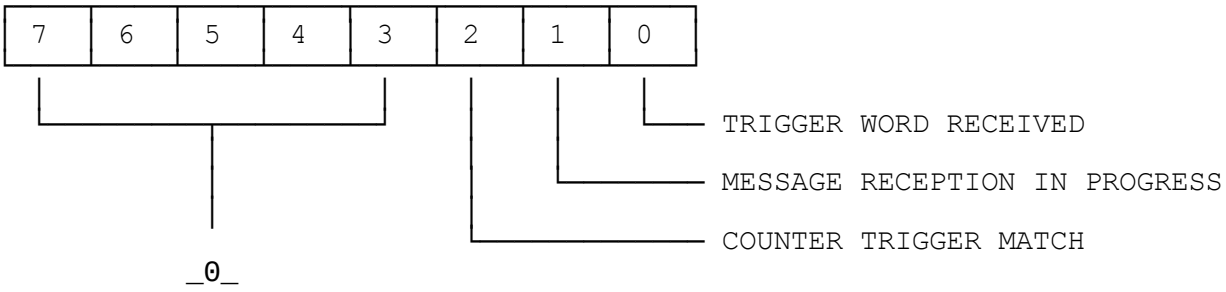
This register allows the user to set different interrupt triggers. When a condition that has been enabled within this register occurs, an interrupt will be generated. The user may check the Message Status Register to determine which condition caused the interrupt. A logic _1_ enables the interrupt condition. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).



Notes:
1. Trigger Word Received - Valid for Sequential Fixed Block Mode only.
2. Counter Trigger Match - Valid for Sequential Fixed Block Mode only.
3. Message Reception in Progress - Valid for all Modes.

MESSAGE STATUS REGISTER 3FFA(H)

This register indicates the status of the EXC-1553PC/E card. The figure below illustrates the definition of each Status bit. A logic _1_ indicates active condition.



NOTE:
Status bits are NOT reset by the board. The user is advised to reset these bits after reading them.

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TIME TAG PRESET REGISTER - HI & LO	3FF9, 3FF8(H)

These registers contain the INITIAL VALUE of the Time Tag Counter. The _HI_ register contains the MSB , the _LO_ register contains the LSB (see Message Block Description above). This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

TIME TAG RESOLUTION REGISTER - HI & LO	3FF7, 3FF6(H)

This 16-bit value represents the resolution of the Time Tag Counter in increments of 155 nsec. See Time Tag description above. (The _HI_ register contains the MSB , the _LO_ register contains the LSB). This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

MESSAGE COUNTER REGISTER	3FF5(H)	SEQUENTIAL FIXED BLOCK MODE ONLY

This register indicates the current Message Block number (0-199). The value is incremented by the board upon reception of each message. Note that the first counter increment [to _1_] - which indicates that the first message has been received and stored - occurs at the beginning of the second 1553 message transfer operation. Check the Message Status Word of the FIRST Message Block in order to determine the arrival of the first 1553 message (the End of Message bit within the Message Status Word will be set).

COUNTER TRIGGER REGISTER	3FF4(H)	SEQUENTIAL FIXED BLOCK MODE ONLY

This register allows the user to know when a specific message block number has been updated by the EXC-1553PC/E. This register is loaded by the user with a value that when equal to the Message Counter, will set a bit within the Message Status Register and or set an interrupt (if programmed within the Interrupt Condition Register). This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register). In addition, the board can be programmed to STOP monitoring when the Counter Trigger is equal to the Message Counter (see: STOP/CONTINUE bit within the Start Register).

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LAST BLOCK REGISTER	3FF2 (H)	LOOK-UP TABLE MODE ONLY

This register indicates the [LOOK-UP TABLE] block number of the current 1553 message. This register can be utilized to identify the location of that message. This register is updated at the beginning of each message reception.

MODE CODE CONTROL REGISTER	3FEA(H)

This register allows the user to determine which 1553 Subaddress value indicates the reception of a 1553 Mode command. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

7	6	5	4	3	2	1	0
_0_						0	0 - _11111_ and _00000_
						0	1 - _00000_ Only
						1	0 - _11111_ Only
						1	1 - _00000_ and _11111_

FIRMWARE REVISION REGISTER	3E80(H)

This register indicates the revision level of the on-board firmware. The value 0110 0011 would be read as revision level: 6.3

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1553 A /B / MULTI-PROTOCOL CONSIDERATIONS

The EXC-1553PC/E offers the user a wide range of options that can be utilized for various 1553 applications. The flexibility of the EXC-1553PC/E does not come at the expense of complicated software or development time for the user as the board is memory mapped and easy to use. The various options are controlled via control registers which are described within this document.

Examples of user selectable parameters:

1. RT can return Status Word [even] if the received 1553 Data Words were not valid (note: the word count was correct).

2. Selectable Broadcast mode

3. Variable Response Time

4. Select Mode Code Subaddress (_00000_, _11111_, or both)

5. 1553A RT Timing

6. Sinusoidal or Trapezoidal 1553 waveform (see Options)

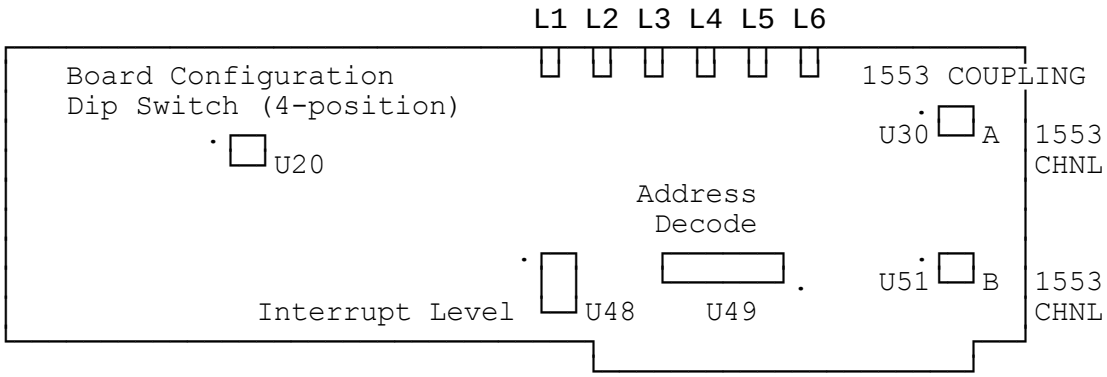
7. User can define all bits within the 1553 Status Word

SWITCHING MODES OF OPERATION

The user can switch between modes of operation (ex. between Bus Controller and Remote Terminal) by "HALTING" the operation of the board (VIA THE START REGISTER), modify the Configuration Register ,setup the memory as required, and then set the START bit within the Start Register.

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BOARD LAYOUT



LED INDICATORS:

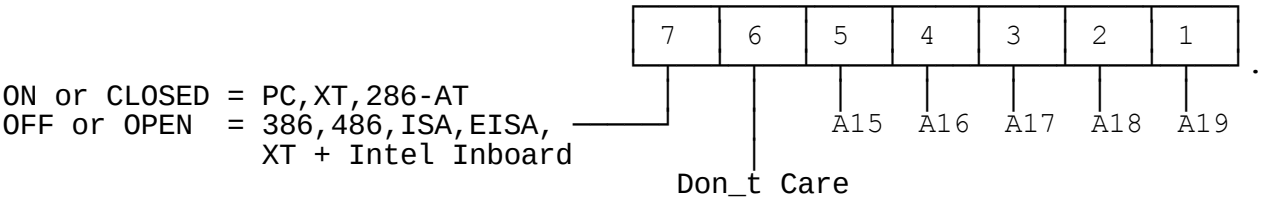
L1 = Board Ready
L2 = BM mode is active
L3 = RT mode is active or BM mode if L2 is lit
L4 = BC or BC/RT mode is active
L5 = 1553 Bus B active
L6 = 1553 Bus A active

DIP SWITCH SETTINGS

The EXC-1553PC/E board contains 5 Dip Switches which control the following functions: Address Decoding of board within the PC system, Interrupt level selection, the Board Configuration and the 1553 Coupling selectors. The position and definition of each switch is described below.

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Address Decode / Computer Type Switch (U49)



The EXC-1553PC/E board is memory-mapped into the address space of the PC_s processor. The board recognizes 20 address bits found on the expansion connector. The PC_s processor "talks" to the board as if it was part of its system memory (standard size: 640k of dynamic memory). The board occupies half of one segment. Set the EXC-1553PC/E to the desired address by setting the switches "OPEN" or "OFF" to represent a logic _1_ and "CLOSED" or "ON" to represent a logic _0_.

EXAMPLE: To address the board within Segment _D_, address:D0000(H), SET:
A19 - OFF, A18 - OFF, A17 - ON, A16 - OFF, [* A15 - ON or OFF]
(OPEN) (OPEN) (CLOSED) (OPEN)

NOTE: * A15 : The EXC1553PC/E allows up to 2 cards to be addressed within the same Segment of memory. One card will be addressed at [relative] address _0000_ (SET A15 switch : On or CLOSED). The other card will be addressed from [relative] location _8000_(Hex) (SET A15 switch: OFF or OPEN). In such a case, for example, the Message, Data Block area of the board would be addressed from _8000_H (see Memory Maps).

Interrupt Level Switch (U48)

note: These are PC/XT interrupt levels.

1	IRQ 2
2	IRQ 3
3	IRQ 4
4	IRQ 5
5	IRQ 6
6	IRQ 7
7	— RESERVED

Set the desired Interrupt Request Level by switching [ONLY] 1 selector to the "ON" or "CLOSED" position. ALL OTHER SWITCH SELECTORS MUST BE "OPEN" or "OFF".

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Board Configuration Switch	(U20)

.

1	- Enhanced or Emulation Mode
2	- Broadcast Mode (RT Mode only)
3	- reserved
4	- Self Test Mode

This switch selects the various Systems modes of the EXC-1553PC/E board. The following table defines the Switch settings and the functions that they control.

	FUNCTION
1	ENHANCED or EMULATION MODE SELECT
	ON or CLOSED: Selects the Enhanced Mode of operation as defined within this document. OFF or OPEN: Selects the Emulation Mode of operation (contact factory for details)

	FUNCTION
2	BROADCAST MODE SELECT (RT Mode Only)
	OFF or OPEN: Broadcast option: IN USE. This bit indicates to the board that a Remote Terminal Address of _11111_ relates to a 1553 BROADCAST Command. NO RT STATUS WORD WILL BE TRANSMITTED. ON or CLOSED: Broadcast option: NOT IN USE. This bit indicates to the board that a Remote Terminal Address of _11111_ is a valid RT Address and will be responded to with a 1553 Status Word.

	FUNCTION
3	reserved

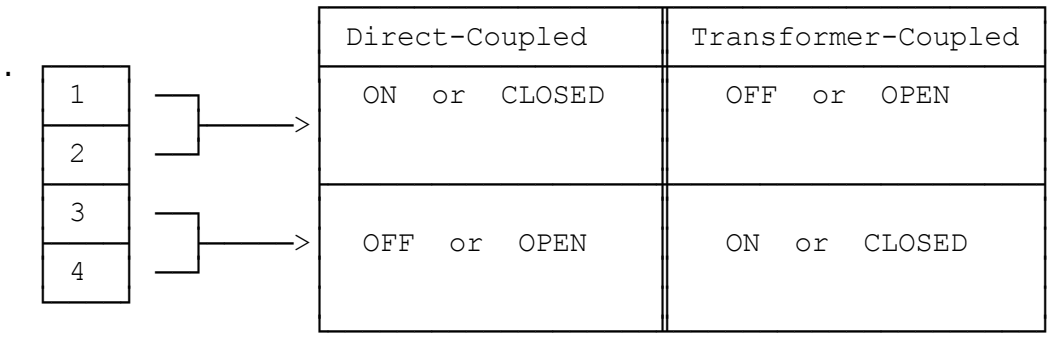
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	FUNCTION
4	POWER-ON DELAY / NORMAL MODE
	OFF or OPEN: ACTIVE. This bit instructs the EXC-1553PC/E to first test the internal memories and LED_s (numbers 1-4) and then to insert a Time Delay of approx. 40 seconds before responding to PC instructions. This option exists for the following reason: Since the board is memory-mapped, the power-on self-test done by the PC computer BIOS might write, inadvertently, into the board_s memory - "starting" the 1553 operation. The time delay assures that the board_s processor ignores any PC accesses (writes) until the completion of the PC self-test. ON or CLOSED: INACTIVE. The board, after completing its internal memory self-test, will wait for a user "start" (approx. 15 sec.)

1553 Coupling Mode Select (U30, U51)

These 2 switches (the top; Switch _A_ for 1553 Channel _A_, the bottom; switch _B_ for 1553 Channel _B_) select the coupling mode to the 1553 Bus. The EXC-1553PC/E can be either DIRECT or TRANSFORMER-coupled to the 1553 BUS.

Refer to this diagram for ALL 1553 coupling switches.



Factory Default Dip Switch Settings

U20 - all ON
U49 - Segment D0; 386/486... type computer
U48 - No interrupts
U30,U51 - Transformer Coupled

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CONNECTORS

The board contains two DB-9 connectors, labeled J1 and J2. Each board is shipped with two adapter cables that convert the DB-9 to a standard 1553 [miniature] female twinax type. The adapter cables comes wired and ready to connect to the 1553 bus. The 1553 connectors will mate, for example, with the Trompeter _PL75_ male twinax connector (Not Supplied).

J1		J2	
1		1	
2		2	
3		3	
4	1553 BUS A*	4	1553 BUS B*
5	1553 BUS A	5	1553 BUS B
6	SHIELD	6	SHIELD
7		7	
8		8	
9		9	

Notes: 1) * = DATA BUS LO

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PC-BUS EDGE CONNECTORS PINOUT

XT/AT

Pin #	Signal Name
A1	
A2	D7
A3	D6
A4	D5
A5	D4
A6	D3
A7	D2
A8	D1
A9	D0
A10	I/OCHRDY
A11	
A12	A19
A13	A18
A14	A17
A15	A16
A16	A15
A17	A14
A18	A13
A19	A12
A20	A11
A21	A10
A22	A9
A23	A8
A24	A7
A25	A6
A26	A5
A27	A4
A28	A3
A29	A2
A30	A1
A31	A0

Pin #	Signal Name
B1	GND
B2	RESET
B3	+5V
B4	IRQ2(9)
B5	
B6	
B7	-12V
B8	
B9	+12V
B10	GND
B11	MEMW-
B12	MEMR-
B13	
B14	
B15	
B16	
B17	
B18	
B19	
B20	
B21	IRQ7
B22	IRQ6
B23	IRQ5
B24	IRQ4
B25	IRQ3
B26	
B27	
B28	ALE
B29	+5V
B30	
B31	GND

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POWER REQUIREMENTS

BOARD TYPE	+5v	+12v	-12v
EXC-1553PC/E	1.4A	-	150ma
EXC-1553PC/E-V	1.4A	150ma	150ma

ORDERING INFORMATION

PART NUMBER:

EXC-1553PC/E ; Standard card with trapezoidal transceivers

EXC-1553PC/E-V ; Standard card with variable-amplitude, "Universal" transceivers

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