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EXC-1553PC/EP

MIL-STD-1553
Test and Simulation Board
for PC Compatible Computers

User's Manual

EXCALIBUR SYSTEMS

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1 Introduction

Chapter 1 provides an overview of the EXC-1553PC/EP avionics communication board. The following topics are covered:

1.1	Overview		page 1-1
	1.1.1	MIL-STD-1553A/B/Multiprotocol Considerations	page 1-3
	1.1.2	MIL-STD-1760B Considerations	page 1-4
1.2	1553 Bus Connections		page 1-4
1.3	Installation		page 1-5
	1.3.1	Software Installation	page 1-5
	1.3.2	Board Installation	page 1-5

1.1 Overview

The EXC-1553PC/EP is an intelligent, memory-mapped MIL-STD-1553 interface board for all PC compatible computers. This board provides a total solution for developing and testing 1553 interfaces and for performing system simulation of the MIL-STD-1553 bus. The EXC-1553PC/EP board contains a 32K × 8 (true dual-ported) RAM for data blocks, control registers, and look-up tables. The concurrent 1553 Monitor has an additional 32K × 8 true dual-port RAM, dedicated to the Monitor function. The board gives the user direct access to all control registers and data blocks; to modify various parameters and data in real time. Operation of the board is controlled by accessing the memory-mapped control registers.

The board supports Minor Frame operation and Asynchronous Frame operation. Error injection capabilities include zero-crossing and Manchester bit errors. The board provides a data integrity value, which indicates that a message is currently being transmitted, and the user should not alter it at this time.

The EXC-1553PC/EP comes complete with GUI software, a C-driver software library including source code, and 1553 adapter cables.

The Excalibur board can be ordered with MIL-STD-1760B options that implement Checksum Error Detections and Error Injection.

See Ordering Information, see page 10-1 for the exact part numbers.

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EXC-1553PC/EP Board Features:

- Operates as BC, RT, BC/Concurrent-RT or BM
- Handles 4µsec intermessage gap times in all modes
- Loopback Mode facilitates 1553 cable testing
- Real-time operation
- ISA and EISA bus compatibility
- Multiple protocol capability (i.e. 1553A, B, F-16, McAir)
- Multiple-RT simulation (up to 32 remote terminals)
- In RT mode, selective enabling of primary and alternate buses for each active RT
- Programmable broadcast mode
- Multi-mode triggerable BM
- Variable amplitude transceiver [McAir/1553-compatible] (standard feature)
- Hardware Time Tag circuit with programmable resolution for use in RT and BM modes
- RT mode has 16-bit time tag
- BM mode has a 16-bit or 32- bit Time Tag
- Time Tag Counter can be read by the user in real time
- XT and AT interrupts (standard feature)
- Interrupt sharing: EXC-1553PC/EP boards can be connected together and share common interrupt lines (standard feature)
- Optional concurrent bus monitor (EXC-1553PC/EPM)
- Optional independent bus monitor (EXC-1553PC/EPMI): allows concurrent monitoring of an independent, dual-redundant, 1553 channel
- Error injection capability:
  - Bit count
  - Word count
  - Incorrect sync.
  - Parity
  - Incorrect RT address
  - Non-contiguous data
- Data Integrity value
- Minor Frame operation
- Asynchronous Frame operation

1760 Options:

- Checksum Error detections
- Checksum Error injections

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The board has four modes of operation:

- Bus Controller (BC) mode
- Multiple Remote Terminal (RT) mode (up to 32 RTs)
- BC with Concurrent RT operation (up to 32 RTs)
- Triggerable BM mode

The EXC-1553PC/EP board can be ordered in eight variations:

- Half-size board without a concurrent bus monitor (cannot be added)
- Full-size board without a concurrent bus monitor (can be added later)
- Full-size board with a non-independent, concurrent bus monitor (independent concurrent monitor can be added later)
- Full-size board with an independent, concurrent bus monitor

All the above can be ordered with MIL-STD-1760B options.

See Ordering Information, page 10-1, for the exact part numbers.

1.1.1 MIL-STD-1553A/B/Multiprotocol Considerations

The EXC-1553PC/EP offers a wide range of options that can be used for various 1553 applications. The various options are controlled via control registers that are described in Global Control Registers, page 2-2, and Control Register Definitions in each of the mode of operations chapters:

Remote Terminal Operation	page 4-17
BC/Concurrent-Remote Terminal Operation	page 5-20
Bus Monitor Operation	page 6-16

Examples of user selectable parameters are:

- Select whether or not an RT will return a status word in the event a message containing a data word error is received by the RT.
- Selectable broadcast mode
- Variable response time
- Variable transmit amplitude
- Select mode code subaddress (00000, 11111, or both)
- 1553A RT timing
- Define each bit in the 1553 Status word

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1.1.2 MIL-STD-1760B Considerations 1760 Option Only

MIL-STD-1760B implements an enhanced MIL-STD-1553 digital interface for the transfer of digital messages to the remote terminal. The enhancements include additional error detection in the form of checksum. Checksum is mandated on critical control messages and provisional on the remainder of the messages. Implementing this level of error detection ensures a higher degree of error free data integrity requirements than only odd parity provides.

The 1760 option implements checksum error detection capabilities. Checksums are computed as each data word is sent or received. If the checksum flag is set on an outgoing message, the checksum will be sent in place of the last data word. On an incoming message, the computed checksum is checked against the last data word received. If it does not match, the Checksum Error bit is set in the Message Status word.

The1760 option has the additional feature of checksum error injection in BC mode. The user can set the checksum to intentionally send an error, giving the additional capability to test for checksum errors on the receiving RTs.

1.2 1553 Bus Connections

For short distances, the EXC-1553PC/EP may be coupled directly to another 1553 device. To ensure data integrity, be sure that the cable connecting the two devices is properly terminated with 78-ohm resistors (see Figure 1-1).

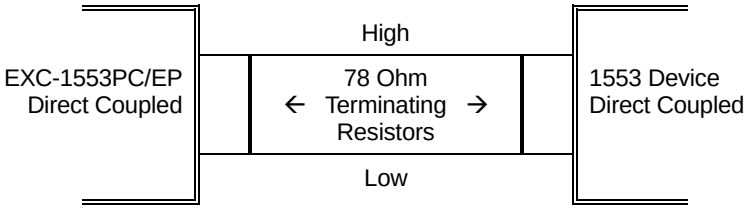


Figure 1-1 Direct Coupled Connection (One Bus Shown)

To operate in the more standard Transformer coupling mode, use stub coupler devices, which are available from Excalibur Systems, Inc. We supply a three-stub coupler (PN# ESI310) and 78-ohm terminators (PN# ESIT5078). Two terminators are required for each coupler, which services a single bus, e.g. BUS A (see Figure 1-2).

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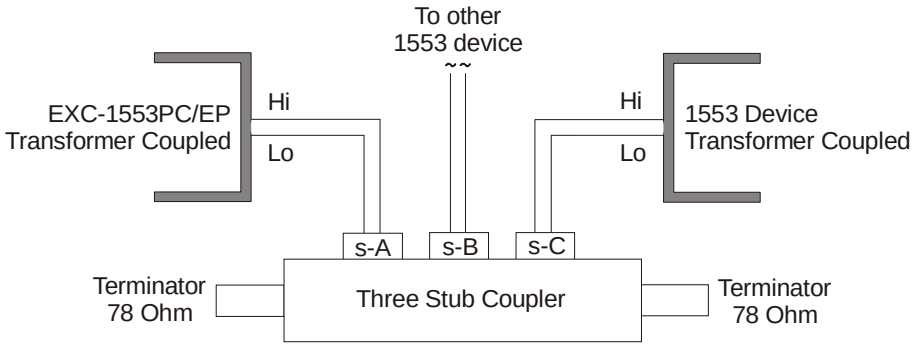


Figure 1-2 Transformer Coupled Connection (One Bus Shown)

1.3 Installation

EXC-1553PC/EP installation includes adding the software for each system and installing the board.

1.3.3 Software Installation

The EXC-1553PC/EP is delivered with software compatible with several operating systems. For information about installing the accompanying software drivers, see the **ReadMe.txt** file on the *Galahad Software Tools* diskettes that came with the board.

The standard software included with an Excalibur board is for Windows 95. Software for other operating systems can be downloaded from our website:http://www.mil-1553.com/.

1.3.4 Board Installation

Before installing the board, it is very important to determine which half-segment of memory is available. For instructions how to determine the board base address, see the **ReadMe.txt** file on the *Galahad Software Tools* diskettes that came with the board.

WARNING *Always wear a suitably grounded electrostatic discharge wrist strap whenever handling the Excalibur board.*

To install the EXC-1553PC/EP:

1. Set DIP switch SW2 according to the memory segment selected. Switch contact 7 of DIP switch SW2 should be set to the appropriate computer type (286 and older or 386 and newer). Set the Board Configuration DIP switch SW1 according to your specification (see DIP Switches, page 9-3).

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2. 1553 devices may be connected to the 1553 bus either directly (direct-coupled) or via a bus-coupling stub (transformer coupled). Use DIP switches SW3, SW4, SW5, and SW6 to set the coupling mode to the 1553 bus(es) (see DIP Switches, page 9-3).
3. **Make certain the computer power source is disconnected**. Insert the EXC-1553PC/EP board into any 8- or 16-bit slot (see Figure 1-3).

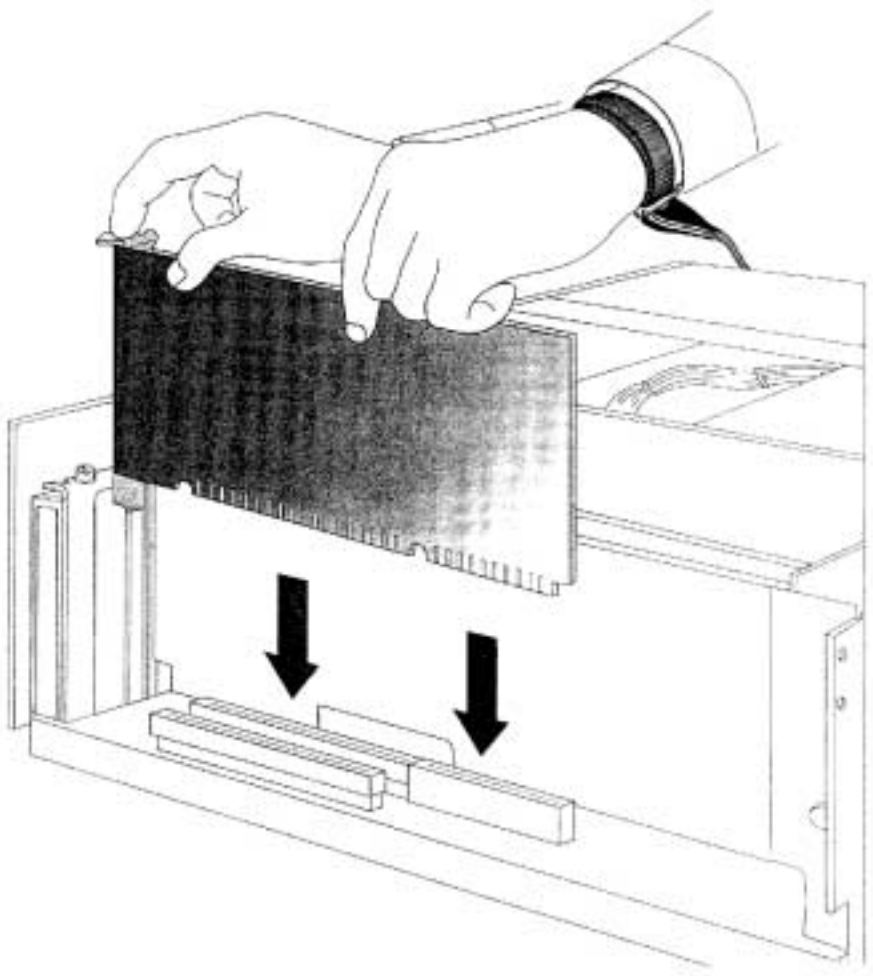


Figure 1-3 Inserting the Excalibur PC Board

4. If AT interrupts are to be used (i.e., IRQ greater than 7), a 16-bit slot must be used. If only XT interrupts are to be used, no loss in speed or functionality will occur if an 8-bit slot is used.
5. Attach the 1553 adapter cables to the board's DB-9 connectors and to the bus. The cables may be connected to and disconnected from the board while power to the computer is turned on, but not while the board is transmitting over the bus.

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2 PC Architecture

Chapter 2 describes the PC architecture. The following topics are covered:

2.1	General Memory Map	page 2-1
2.2.	Global Control Registers	page 2-2

2.1 General Memory Map

The board occupies 32K x 8 bytes of the PC's memory. This memory is mapped to any half-segment boundary (e.g., D000, D800, etc.) of the PC's memory space via DIP-switch SW2. When the Concurrent Monitor option is installed, an additional 32K bytes of memory are available for controlling the concurrent monitor. The board still uses only 32K bytes of PC memory. This is implemented via a bank switching mechanism. At any given time only 32K bytes of the board's memory is available.

The 32K bytes associated with the BC, RT, BC/Concurrent-RT and non-concurrent BM are referred to as bank 0. The 32K bytes associated with the concurrent BM are referred to as bank 1. Only one bank is accessible to the user at any time. Use the Bank Select Register, page 2-4, to specify which bank you want to access.

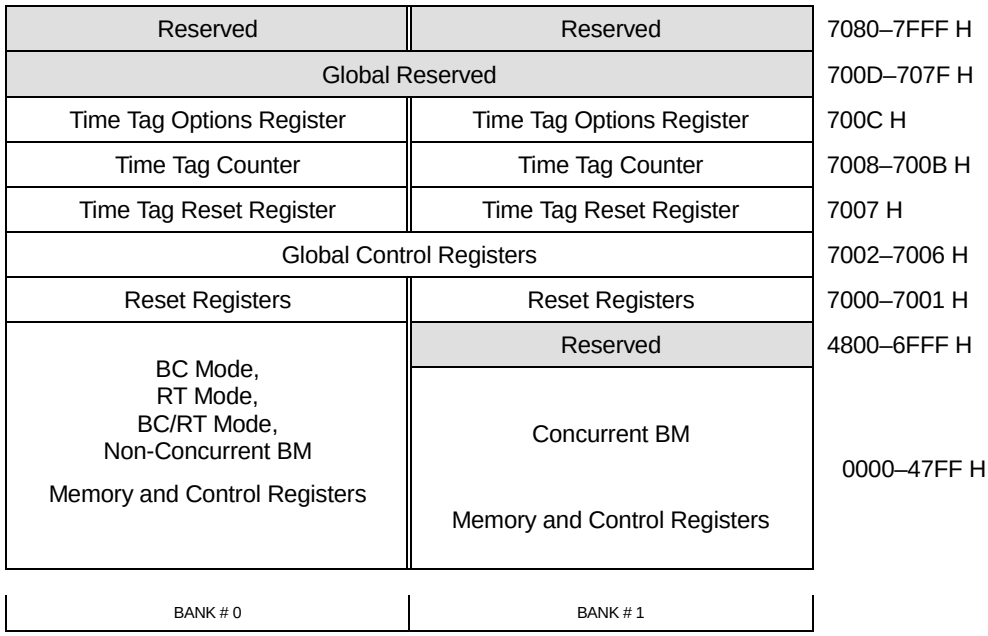


Figure 2-1 General Memory Map

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2.2 Global Control Registers

Set the Global Control registers at any time from both bank 0 and bank 1. This section includes a description of each individual register.

2.2.1 Global Software Reset Register

Address: 7002 (H)

Set the Global Software Reset register to reset both sections of the board at the same time, independent of the state of the Bank Select register (data field = don't care).

NOTE Global Software Reset erases all locations in dual-port RAM. Board status, Board ID, Firmware Revision and Variable Amplitude registers are written by the board after the reset operation is completed.

2.2.2 Zero Crossing Register

Address: 7003 (H)

Set the Zero Crossing register to specify the options described in Table 2-1 Zero Crossing Register: Write Operation. This register can be modified at any time (without having to start and stop board operation).

The Zero Crossing register is reset at power-up (all bits set to 0). This register is not affected by a software reset.

This register is decoded at address 7003 (H) regardless of the contents of the Bank Select register.

The Zero Crossing register write and read definitions are explained below.

ZERO CROSSING REGISTER WRITE OPERATION

Bit	Description
07	0
06	Reserved. Set to 0.
05	0
04	EXC-1553PC/EPMI Control Bit: 0 = Non-Independent BM Channel Selected 1 = Independent BM Channel Selected
00-03	Zero Crossing Code (see Table 2-2 below)

Table 2-1 Zero Crossing Register: Write Operation

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ZERO CROSSING CODE

The EXC-1553PC/EP board sets the Zero Crossing timing, allowing the user to test for proper operation with both valid and invalid Zero Crossing timing. Invalid Zero Cross timing creates an invalid word.

The board checks the register between transmissions of every word.

When activated, Zero Crossing and Manchester errors are inserted into the first bit of every word that is transmitted by the board. This includes Command, Status and Data words.

Bit Position				Operation Selected
Bit 3	Bit 2	Bit 1	Bit 0	
0	0	0	0	No Zero Crossing Deviation (No Error)
0	0	0	1	+150 nsec from 0 (Absolute Limit — No Error)
0	0	1	1	–150 nsec from 0 (Absolute Limit — No Error)
0	1	0	1	+190 nsec from 0 (Above 1553 Limit)
0	1	1	1	–190 nsec from 0 (Below 1553 Limit)
1	0	0	0	Manchester High-Bit Error
1	0	0	1	Manchester Low-Bit Error
1	0	1	0	Manchester Dead Bit Error

Table 2-2 Zero Crossing Code Selections

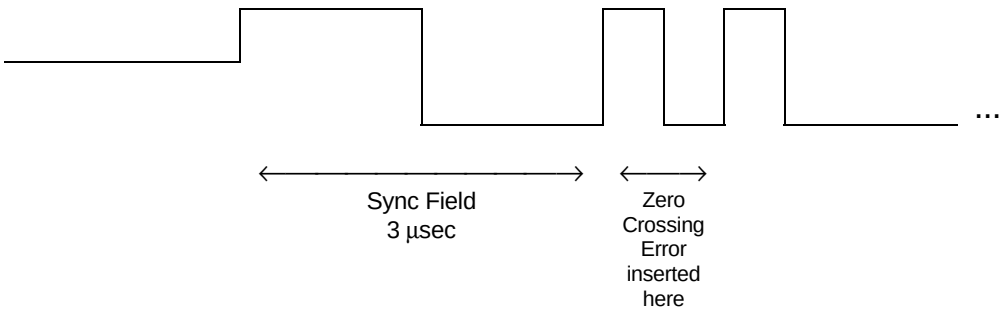


Figure 2-2 Zero Crossing Operation

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ZERO CROSSING REGISTER READ OPERATION

Read the Zero Crossing register to get the information described in Table 2-3 below.

Bit	Description
07	Bank Select Status bit (reflects status of bank area): 0 = Bank 0 Selected 1 = Bank 1 Selected
06	Reserved Status Bit
05	Independent Concurrent-BM Option (EXC-1553PC/EPMI): 0 = Not Installed 1 = Installed
04	EXC-1553PC/EPMI Status Bit (reflects status of EXC-1553PC/EPMI Control bit): 0 = Not Installed or Not Active 1 = Active
00-03	Zero Crossing Code Status (reflects status of Zero Crossing Code bits)

Table 2-3 Zero Crossing Register: Read Operation

2.2.3 Bank Select Register

Address: 7004 (H) WRITE

Set bit 00 of the Bank Select register to select whether Bank 0 or Bank 1 will be active.

Bit	Description
01-07	X (Don't Care)
00	0 = Bank 0 Active. Bank 0 supports BC, RT, BC/Concurrent-RT, and Non-Concurrent BM modes. 1 = Bank 1 Active. Bank 1 supports Concurrent BM memory access. Use with EXC-1553PC/EPM or EXC-1553PC/EPMI with Concurrent BM option installed.

Bank Select Register

The Bank Select register is decoded at address 7004 (H) regardless of the contents of the Bank Select register.

Bit 00 of the Bank Select register is set to 0 at power-up. The Bank Select register is not affected by a software reset.

Check the status of the Bank Select bit by reading address 7003 (H), bit 07. See Zero Crossing Register Read Operation.

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2.2.4 Concurrent Start Register

Address: 7005 (H) WRITE

Set the Concurrent Start register to start the operation of the BC, RT, BC/Concurrent-RT, or non-concurrent BM at the same time as the Concurrent BM. Starting both sections of the board simultaneously assures that they will be synchronized.

When using the Concurrent Start register, the standard Start registers of the dual-port RAM must be set to logic 0.

To stop the selected operation(s), follow the normal procedure described under the respective Start register. Set the Concurrent Start register to start the Concurrent Start operation.

Bit	Description
00-07	X (Don't Care)

Concurrent Start Register

NOTE 1. The Concurrent Start register is decoded at address 7005 (H) regardless of the contents of the Bank Select register.

2. For Printed Circuit Board versions C and above, you can also start concurrently by sending a low TTL pulse of 100 nsec minimum to the EXSTART$ pin (see Connectors, page 9-6).

2.2.5 Interrupt Level Select Register

Address: 7006 (H) WRITE

Set the Interrupt Level Select register to select the Interrupt level of both sections of the board [BC, RT, BC/Concurrent-RT, non-concurrent BM (bank 0), and the Concurrent BM (bank 1)]. The Interrupt Request levels of the BC, RT, BC/Concurrent-RT section, and the concurrent BM section can be selected independently of one another.

Bit	Description
04-07	Interrupt 1 Level Select (see Table 2-4)
00-03	Interrupt 0 Level Select (see Table 2-4)

Interrupt Level Select Register

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Interrupt 1				Interrupt 0				
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Description**
0	0	0	0	0	0	0	0	No Interrupt Selected
0	0	0	1	0	0	0	1	No Interrupt Selected
0	0	1	0	0	0	1	0	Interrupt Level 2
0	0	1	1	0	0	1	1	Interrupt Level 3
0	1	0	0	0	1	0	0	Interrupt Level 4
0	1	0	1	0	1	0	1	Interrupt Level 5
0	1	1	0	0	1	1	0	Interrupt Level 6
0	1	1	1	0	1	1	1	Interrupt Level 7
1	0	0	0	1	0	0	0	No Interrupt Selected
1	0	0	1	1	0	0	1	No Interrupt Selected
1	0	1	0	1	0	1	0	Interrupt Level 10
1	0	1	1	1	0	1	1	Interrupt Level 11
1	1	0	0	1	1	0	0	Interrupt Level 12
1	1	0	1	1	1	0	1	No Interrupt Selected
1	1	1	0	1	1	1	0	Interrupt Level 14
1	1	1	1	1	1	1	1	Interrupt Level 15

Table 2-4 Interrupt Level Selections

An interrupt may be caused either by an on-board interrupt condition or by the transfer of an interrupt from another board. Similarly, a board may choose to either issue an interrupt through its own PC edge connector or pass it to another board.

The Interrupt Level Select register is decoded at address 7006 (H) regardless of the contents of the Bank Select register.

If both sources select the same interrupt request level, the board will issue an interrupt on that level for both sides. The interrupt levels for the two sources are internally ORed. In such a case, to determine which side issued the interrupt, read the relevant Control registers for both sides.

The Interrupt Level Select register is set to 00 on power-up (no interrupts selected). The register is not affected by a software reset.

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SHARING INTERRUPT LINES

By sharing interrupt lines, the EXC-1553PC/EP board can be connected to other EXC-1553PC/EP boards.

To receive an interrupt while either of the two EXC-1553PC/EP boards is monitoring a message with its respective concurrent BM, connect the External Interrupt Output line of board A to the External Interrupt In line of board B. Board B's Interrupt Level Select register will be set to the desired interrupt; board A's Interrupt Level Select registers will be set to 0. In this way, two boards can use the same interrupt request level.

Example Multiple EXC-1553PC/EP Boards Sharing a Single Interrupt

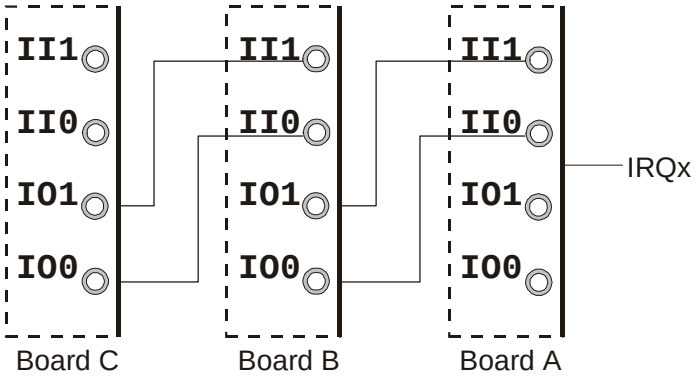


Figure 2-3 Sharing an Interrupt

To share an interrupt, connect external wires between numbered pads as shown.

Only board A selects the interrupt level (via the Interrupt Level Select register).

When an interrupt occurs, check all three boards to find the source of the interrupt. To clear the interrupt, write to the appropriate Interrupt Reset register.

To determine the source of the interrupt, read the Interrupt Status registers on the EXC-1553PC/EP boards. Then issue an Interrupt Reset [write to location 7001 (H)] to the appropriate board. See Interrupt Reset Register, 4-18.

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Input	Interrupt	Output
Concurrent Bus BM— Internal Source or External Interrupt IN #1 (II1/E2 pad on the board)	Interrupt #1	External Interrupt OUT #1 (IO1/E5 pad on the board)
BC, RT, BC/RT, non-concurrent Bus BM— Internal Source or External Interrupt IN #0 (II0/E3 pad on the board)	Interrupt #0	External Interrupt OUT #0 (IO0/E4 pad on the board)

Table 2-5 Interrupt Inputs and Outputs

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3 Bus Controller Operation

In this manual the Bus Controller (BC) Mode is included in BC/Concurrent-RT mode. Refer to Chapter 5 BC/Concurrent-Remote Terminal Operation, for information regarding BC Mode.

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4 Remote Terminal Operation

Chapter 4 describes EXC-1553PC/EP operation in Remote Terminal (RT) mode. The following topics are covered:

RT Memory Map	page 4-3
Data Block Look-Up Table	page 4-4
Active RT Table	page 4-6
1553 RT Status Words	page 4-7
Message Stack	page 4-8
RT Last Command Words	page 4-11
1553 RT BIT Words	page 4-11
1553 RT Vector Words	page 4-11
Alter Table	page 4-12
Mode Codes	page 4-12
Broadcast Mode	page 4-13
Error Injection Features	page 4-13
1760 Header Word **[1760 Option only]**	page 4-15
Program Example: RT Mode	page 4-16
Control Register Definitions	page 4-17

The EXC-1553PC/EP can be configured to simulate up to 32 remote terminals. The user can select which terminal(s) are operating (active), and in addition, inject errors into message responses.

After receiving the Start command, the board handles the transfer of all messages (see Start Register, page 4-20). Data associated with a particular RT subaddress combination is transferred via a 2K x 8 look-up table, which points to one of 200 data blocks. Load data blocks associated with transmit commands with 1553 data to transmit, and read received 1553 data from data blocks associated with receive commands.

The board will respond properly to messages received with an intermessage gap of 4 µsec.

The user can choose whether the remote terminal should transmit its 1553 status word at the end of a message, even if the message contains *invalid* data words (invalid as specified by MIL-STD-1553). Use the Status Response register to activate or disable this feature (see Status Response Register, page 4-25).

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The remote terminal transmits its 1553 status word in approximately 4 µsec. Use the RT Response Time register to increase the time it takes the remote terminal to transmit the 1553 status word.

The board provides a data integrity value, which indicates that a message is currently being transmitted. Do not alter it at this time. Check this value *before* attempting to change the data words of the message (see Alter Table, page 4-12).

Since most 1553 parameters, such as Response Time, Status Word Content, etc. are user-programmable, the board can operate in various 1553 environments. The board also allows the user to enable or disable the 1553 Broadcast function. If broadcasting is enabled, RT address 31 (11111) is reserved; if broadcasting is disabled, all 32 RT addresses are available (see DIP Switches, page 9-3).

Program the 1553 Mode Code subaddress identifier (see Mode Code Control Register, page 4-28) so that, either, 31, 0, or both are used to indicate that the 1553 Command Word is a Mode Code.

TO DETERMINE THAT THE BOARD IS INSTALLED AND READY TO OPERATE:

Perform the following procedure after a power-up or a software reset.

1. Check the Board ID register (test for value = 45 H).
2. Check the Board Status register (test for Board Ready bit = 1).

The board is installed and ready when both registers contain the correct values (as written above). For software reset operations, set these values to 0 immediately prior to writing to the (software) Board Reset register.

NOTE Throughout this manual, writing a 1 to the Start register is referred to as “issuing a Start command.”

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4.1 RT Memory Map

Figure 4-1 illustrates the RT memory usage.

Time Tag Options Register	700C H		
Time Tag Counter	7008-700B H		
Time Tag Reset Register	7007 H	Reserved	3E86-3EBF H
Interrupt Reset Register	7001 H	Board Options Register (16 bits)	3E84 H
Software Reset Register	7000 H	Reserved	3E81-3E83 H
Data Block Look-Up Table	4000-47FF H	Firmware Revision Register	3E80 H
Board Configuration Register	3FFF H	Reserved	3650-3E7F H
Board ID Register	3FFE H	Alter Table	34C0–364F H
Board Status Register	3FFD H	1553 RT Vector Words	3480-34BF H
Start Register	3FFC H	1553 RT Bit Words	3440-347F H
Message Status Register	3FFB H	RT Last Command Words	3400-343F H
Reserved	3FF8 H	Reserved	33FD-33FF H
Time Tag Resolution Register	3FF7 H	Interrupt Condition Register	33FC H
Bit Count Register	3FF6 H	Message Stack (42 Blocks)	3300-33FB H
Reserved	3FF5 H	Word Count Error Table	32E0-32FF H
RT Response Time Register	3FF4 H	Reserved	3267-32DF H
Error Injection Register	3FF3 H	Mode Code Control	3266 H
Variable Amplitude Register	3FF2 H	Checksum Blocks Register (16 bits) *	3264 H
Message Stack Pointer (16 bits)	3FF0 H	Reserved	3260-3263 H
Status Response Register	3FEF H	1553 RT Status Words	3220-325F H
Reserved	3F40-3FEE H	Active RT Table (32 Bytes)	3200-321F H
1760 Header Value Table *	3F00-3F3F H	1553 Data Blocks (200 Blocks)	0000-31FF H
1760 Header Exist Table *	3EC0-3EFF H		

Figure 4-1 RT Memory Map

*1760 option only

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4.2 Data Block Look-Up Table

Address: 4000–47FF (H)

The received command word's RT Address, T/R Bit, and Subaddress fields are used to index the entries in the (user-programmed) look-up table. Each entry in the table represents a data block number (from 0 to 199 decimal). Each block can contain up to 32 1553 data words (64 bytes). Data Block 0 begins at address 0000, Data Block 1 begins at address 0040 (H), etc.

	(11 most significant bits of the 1553 command word)					
Base Address	(5 bits) **RT address**	(1 bit) **T/R**	(5 bits) **Sub-address**	**Look-up table (2K x 8)**	**Data block**	**Hex address of data block**
4000+	11111	1	11111	Block #	Data Block 199	31C0
	•	•	•	•	•	
	•	•	•	•	•	
	•	•	•	•	•	
4000+	00000	0	00001	Block #	Data Block 1	0040
4000+	00000	0	00000	Block #	Data Block 0	0000

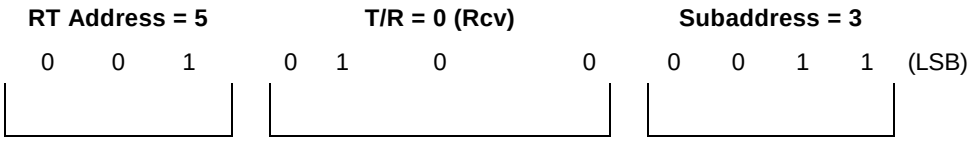
Figure 4-2 Data Block Look-Up Table

NOTE For RT-to-RT messages:
When the board is simulating both RTs in an RT-to-RT message transfer, the simulated receiving RT's data block is not updated with the transmit data. (The data is transmitted over the 1553 bus.)

To create the address to the table

1. Isolate the eleven (most significant) bits of the 1553 command word (RT Address, T/R, and Subaddress field), and determine their hex value.

Example To allocate a data block for a 1553 receive message to RT#5, Subaddress 3.



Hex representation = 143 (H)

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2. Add the hex value of this part of the command word to the base address of the look-up table (4000H).

```
  4000   (H)
+ 143    (H)
-------------
  4143   (H)
```

3. Write the data block number to this location.

Example `POKE &H4143,01` allocates block #1 for the data of this message. Read the 1553 data out by reading block #1, which starts at address 0040 (H). Each data block, beginning at address 0000 is 64 bytes long (for up to 32 1553 data words). The address of a block is obtained by multiplying its block number by 64 (40 H).

4.2.1 Data Storage

The data words must be stored and/or read in the following format in the data block:

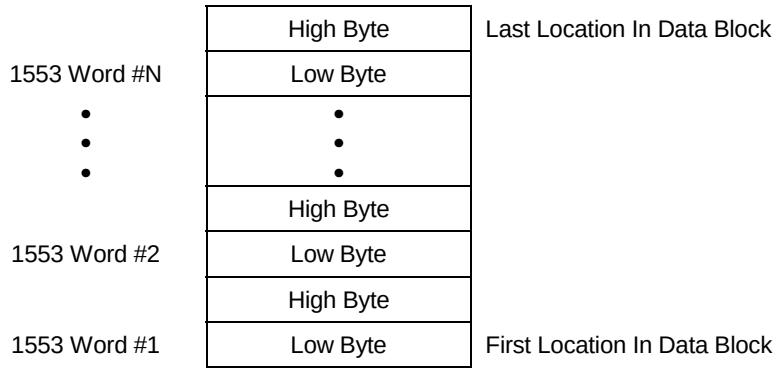


Figure 4-3 Data Storage Sequence

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4.3 Active RT Table

Address: 3200–321F (H)

The 32 locations (bytes) of the Active RT table contain the list of active remote terminals. To select an RT to be simulated, set bit 00 in the Active Remote Terminal byte to logic 1. The first active RT byte relates to RT #0, the next to RT #1, and the last location relates to RT #31.

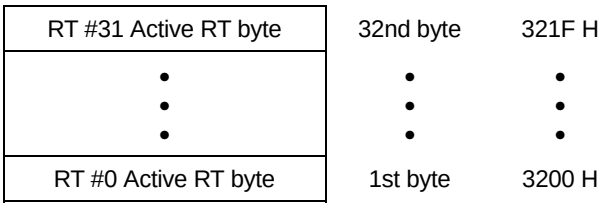


Figure 4-4 Active RT Table: RT Mode

Bit	Bit Name	Description
04-07	**0**	
03	**Inactive Bus B**	1 = Bus B Inactive 0 = Bus B Active If bit 00 is set to 1 and bit 03 is set to 0, the board will respond to all messages received over bus B for this RT; and the board will generate interrupts, if requested to do so. If bit 03 is set to 1, all messages over bus B for this RT will be ignored, regardless of the settings of other bits in this register.
02	**Inactive Bus A**	1 = Bus A Inactive 0 = Bus A Active If bit 00 is set to 1 and bit 02 is set to 0, the board will respond to all messages received over bus A for this RT; and the board will generate interrupts, if requested to do so. If bit 02 is set to 1, all messages over bus A for this RT will be ignored, regardless of the settings of other bits in this register.
01	**Interrupt**	1 = Interrupt 0 = No Interrupt If bit 01 is set to 1, the RT is active and the Interrupt Condition register is enabled, this RT will generate an interrupt.
00	**Active**	1 = Active 0 = Inactive If bit 00 is set to 0, the RT is not active. If it is set to 1, bits 01, 02, and 03 are checked.

Table 4-1 Active RT Byte Definition: RT Mode

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4.4 1553 RT Status Words

Address: 3220–325F (H)

These locations are reserved for the 32 1553 RT Status Words. Load the desired status words into their respective locations in the block. The first two bytes (word) relate to RT #0, the next two bytes (word) to RT #1, while the last two bytes (word) relate to RT #31. Load low byte, then high byte.

For each RT that is to be simulated, all 16 bits of that RT must be defined in its Status Word.

In a **non-1553B environment** (see Status Response Register, page 4-25) the user-defined Status Word is sent whenever the RT has to respond with a Status Word.

In a **1553B environment** (see Status Response Register, page 4-25), the same status word is sent with the following conditions:

Message Error (Bit 10)
In case an error occurred in the previous message, the Status Word will be sent with the Message Error bit set to 1 if the current message is of type Send Status or Send Last Command. This will occur even if you set the Message Error bit to 0.

If you set the Message Error bit to 1, it will always be sent set to 1.

Busy (Bit 03)
The Busy bit is always sent as you defined it. In the case of Transmit commands, when Busy is set to 1, no data words will be transmitted by the RT following the transmission of the status word.

The MIL-STD-1553B Format for the status word is as follows:

Bit	Bit Name
11–15	RT Address
10	Message Error
09	Instrumentation
08	Service Request
05–07	Reserved
04	Broadcast
03	Busy
02	Subsystem Flag
01	Dynamic Bus
00	Terminal Flag

1553B Status Word

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4.5 Message Stack

The board generates a message stack in the dual-port memory. This stack contains information you can use for post-processing of RT messages. The stack is divided into 42 blocks, each containing three words. The stack operates as a circular buffer. The Message Stack Pointer points to the beginning of the (next) unused block. Only active RT messages are stored. Figure 4-5 illustrates one block.

Information is stored in the memory in the following sequence:	Byte Offset
Message Status Word	4
Time Tag Value	2
1553 Command Word	0

Figure 4-5 Message Stack Block Structure

How the board updates an RT-to-RT message:

When an RT-to-RT message is received, where the board is functioning as both RTs, the Message stack is updated as follows:

Two message stack blocks are utilized.

1. The 1553 Receive command word is written into the *first* message stack block.
2. The RT-RT bits in *both* message status words are set to 1.
3. The board updates the Time Tag word in the *second* stack block and the *second* Message Status word. The board updates only the RT-to-RT bit in the *first* Message Status word to Active status.
4. The 1553 Transmit command word is written into the *second* stack block.

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4.5.1 Message Status Word

The Message Status word indicates the status of the message transfer. This word is created by the board. Do not confuse this word with the 1553 Status word (see 1553 RT Status Words, page 4-7). The contents of the Message status word are described below.

NOTE A logic 1 indicates the occurrence of a status flag.

Bit	Bit Name	Description
15	**End Of Message**	Message transfer completed
14	**Bus A/B**	Bus on which the message was transferred: 0 = Bus B 1 = Bus A
13	**Checksum Error**	The computed checksum (on an incoming message) does not match when checked against the last data word received. **[1760 Option only]** See MIL-STD-1760B Considerations, page 1-4
11-12	**Reserved**	Set to 0
10	**Tx Time Out**	Board, acting as receiver in RT-to-RT message, did not sense a transmitter status word (in 14 μsec.)
09	**Reserved**	Set to 0
08	**1760 Header Error**	Header Word received does not match the value set in the Header Value table. **[1760 Option only]** See MIL-STD-1760B Considerations, page 1-4
07	**Invalid Word Received**	At least one invalid 1553 word received (i.e. bit count, Manchester code, parity)
06	**Reserved**	Set to 0
05	**Word Count Error (Receive Message)**	Incorrect number of words received in the message
04	**Broadcast Message**	Broadcast command word received
03	**Incorrect Sync Received**	Sync of either the command or the data word(s) is incorrect
02	**Non-Contiguous Data (Receive Message)**	Invalid gap between received 1553 words
01	**RT-RT Message**	RT-to-RT message received where board was simulating both RTs
00	**Error**	Error occurred. (The error type is defined in one of the other message status bit locations.)

Message Status Word Definitions

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4.5.2 Time Tag Value **Read by User**

The Time Tag value is a 16-bit word that can be used to determine the time elapsed since the Start command was issued or the time between 1553 messages. The Time Tag implementation uses a 32-bit, free-running counter whose resolution is set by the Time Tag Resolution register. (See Time Tag Resolution Register, page 4-21.) This register has a resolution of 4 µsec. per bit.

To determine the Time Tag resolution:

Time Tag Resolution = (register value + 1) x 4 µsec.

Example Register value = 0 → Counter's resolution = 4 µsec
Register value = 4 → Counter's resolution = 20 µsec

To reset the Time Tag counter (to 0) any time, write to the Time Tag Reset Register (see Time Tag Reset Register, page 4-18).

When the first command of each message is received, the value of the 16 lower bits of the Time Tag Counter register are written to dual-port RAM.

NOTE 1. The counter's value can be read any time by reading the Time Tag Counter addresses. (see Time Tag Counter, page 4-17).

2. The counter can also be clocked and/or reset from an external source (see Connectors, page 9-6).

Example How To Calculate Elapsed Time

Time Tag Resolution register = 03 (initialized before Start command)

Time Tag values (read during or after message transfers):

Low = 40 (H)
High = 10 (H)

Time elapsed since Start command
= (Time Tag register value) x (Time Tag Resolution value + 1) x (4 µsec)
= 1040 (H) x (03 + 1) x 4 µsec
= 4160 (Dec) x (4 x 4 µsec) = 66560 µsec (66.56 msec.)

4.5.3 1553 Command Word

The command word location contains the 1553 command word associated with the message.

Only active RT 1553 command words are stored.

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4.5.4 RT-to-RT Messages

When the board is operating as both RTs in an RT-to-RT transfer:

- The board transmits both 1553 Status and Data words onto the bus.
- The board does *not* copy the Transmit data block into the Receiver data block area (pointed to by the look-up table pointer).

4.6 RT Last Command Words

Address: 3400–343F (H)

The Last command word locations are reserved for the 32 1553 Last Command Words. The board writes to these locations at the end of each message transfer (for active RTs only). The first two bytes (word) are for RT #0, the next two bytes (word) are for RT #1, and the last two bytes (word) are for RT #31. Read low byte, then high byte. These words are used for the implementation of the Transmit Last Command Word Mode code.

NOTE Only command words of valid messages containing no errors are recorded in this table.

4.7 1553 RT BIT Words

Address: 3440–347F (H)

The RT BIT word locations are reserved for the 32 1553 BIT words. Load the desired BIT words into the corresponding locations in the block. The first two bytes (word) are for RT #0, the next two bytes (word) are for RT #1, and the last two bytes (word) are for RT #31. Set low byte, then high byte. These words are used to implement the Transmit BIT Word Mode code.

4.8 1553 RT Vector Words

Address: 3480–34BF (H)

The RT Vector Word locations are reserved for the 32 1553 Vector words. Load the desired Vector words into the corresponding locations in the block. The first two bytes (word) are for RT #0, the next two bytes (word) are for RT #1, and the last two bytes (word) are for RT #31. Read low byte, then high byte. These words are used to implement the Transmit Vector word Mode code.

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4.9 Alter Table

Address: 34C0–364F (H)

To ensure data integrity, the board sets a special status value of 7F00 (H) to indicate that the message is currently being transmitted. This is an alert, *not* to alter this message now.

This special status value is stored in a 200-word table in the dual-port RAM, one element for each data block that can be associated with an RT or with multiple RTs. When starting to send out data over the bus (from a specific data block), the board sets the Alter Table entry for this block to the special status value, 7F00 (H), indicating to the user *not* to alter the data associated with this block at this time. When the board has completed sending the data out over the bus, the board resets the Alter Table entry to 0, indicating that data may now be altered.

Check this value *before* attempting to change the data words of the message. Otherwise, the results are indeterminate.

4.10 Mode Codes

The Subaddress code can be programmed to indicate that a Mode command has been received. Either or both of the following codes can be used: 11111 and 00000. Program the Mode Code Control register as described in Mode Code Control Register, page 4-28. The board handles all dual-redundant 1553B Mode codes. The Word Count field is decoded according to MIL-STD-1553B.

One of the Mode codes (Synchronize with Data word) is operated upon as a standard message transfer, using the Data Block look-up table. When the board encounters the Synchronize with Data word Mode code, the command word's RT Address, T/R bit, and Subaddress fields are used as a pointer to the look-up table. The table entries that are addressed when the T/R bit = 0 and Subaddress = 00000 or 11111 should contain a Data Block number (0–199) indicating where the Synchronize with Data Word's data word should be stored.

The data associated with mode codes (Transmit Last Command, Transmit Bit word, and Transmit Vector word) is set using the dedicated blocks in the on-board memory (described in RT Last Command Words, 1553 RT BIT Words and 1553 RT Vector Words, page 4-11).

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4.11 Broadcast Mode

To operate the board in the broadcast environment, select the appropriate DIP switch setting as defined in DIP Switches**,** page 9-3**.**

When operating in Broadcast mode, set the active RT look-up table entry for RT #31 as Not Active. The board tests the Broadcast DIP switch to determine whether the board is operating in Broadcast mode.

In Broadcast mode, the board stores the received message in a 1553 data block area in the same way as standard message formats. RT address, T/R bit, and Subaddress are used as a pointer to the Data Block look-up table memory.

NOTE When operating in Broadcast mode, the Broadcast bits in the 1553 Status words are *not* updated by the board's processor.

4.12 Error Injection Features

The board allows two types of error injection:

- Global (for all RTs)
- Per RT

The global errors such as Parity, Sync, Non-Contiguous data and Bit count are described in Error Injection Register, page 4-24. These errors are either *on* or *off* for all RTs. The ability to inject a 1553 Word Count error, however, can be set per RT.

4.12.1 Word Count Error Table **Address: 32E0–32FF (H)**

The Word Count Error is selected by writing to the Word Count Error table, which contains 32 bytes (one per remote terminal). The first byte is for RT #0, the second to RT #1, and the last byte is for RT #31. The contents of each location, controls the number of 1553 words (±3 words) in the message. The variation is an offset, relative to the 1553 command word's Word Count field. The resulting message (if an error is programmed) must contain at least one data word.

Upon power-up and software reset, the board sets the Word Count Error Table to the default value, 00.

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Set the Word Count Error register before issuing a Start command to the board. To modify the Word Count Error register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 4-20).

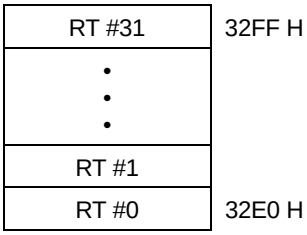


Figure 4-6 Word Count Error Table Addresses

Register Value	Word Count Offset
FD H	–3 Words
FE H	–2 Words
FF H	–1 Word
00 H	No Error Injection
01 H	+1 Word
02 H	+2 Words
03 H	+3 Words

Word Count Error Byte Values

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4.13 1760 Header Word

1760 Option Only

In the MIL-STD-1760B specification, the first data word of a message may be a Header Word, which is used for message identification. The header word is associated with a specific RT subaddress.

To indicate that a specific subaddress will require a Header Word, set the corresponding entry in the 1760 Header Exist table to 1. Then set the corresponding entry in the 1760 Header Value table to the value you expect to receive in the first data word of the message.

The 1760 option provides predefined values, and these are preset on the EXC-1553PC/EP board.

For descriptions of the 1760 Header Value Table and 1760 Header Exist Table, see page 4-26.

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4.14 Program Example: RT Mode

NOTE All values are in HEX unless otherwise stated.

BASIC Instruction	Remarks
`10 POKE &H3FFF,02`	Set Configuration register to RT mode.
`20 POKE &H3FF2,xx`	Set Variable Amplitude register.
`30 POKE &H3201,1`	Enable RT #1.
`40 POKE &H3204,1`	Enable RT #4.
`50 POKE &H3222,00`	Set Status word of RT #1 to 0800.
`60 POKE &H3223,08`	
`70 POKE &H3228,00`	Set Status word of RT #4 to 2000.
`80 POKE &H3229,&H20`	
`90 POKE &H3FF7,xx`	Set Time Tag Resolution register.
`100 POKE &H3266,00`	Set Mode Code Control register to Subaddress 0 & 31.
`110 POKE &H3FF3,00`	Set No global error injection.
`120 POKE &H4xxx,1`	Load block number 1 for data storage into look-up table xxx.
`130 POKE &H4yyy,2`	Load block number 2 for data storage into look-up table yyy.
`140 POKE &H3FFC,1`	Set Start register to 1 to start RT mode.
`150 STOP`	

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4.15 Control Register Definitions

4.15.1 Time Tag Options Register

Address: 700C (H) WRITE ONLY

Set the Time Tag Options register's 00 bit to select the current bank's Time Tag Counter Clock Source. After power-up or software reset, the Time Tag Options register's 00 bit is set to 0. (See General Memory Map, page 2-1 for an explanation of the EXC-1553PC/EP "banks".)

Bit	Description
01–07	Reserved
00	0 = Internal Time Tag Clock 1 = External Time Tag Clock (See EXTTCLKx pin in Connectors, page 9-6).

Time Tag Options Register

4.15.2 Time Tag Counter

Address: 7008–700B (H) READ ONLY

Read the four bytes of the Time Tag Counter to determine the current bank's free-running, 32-bit Time Tag counter value. The counter canbe read at any time.

The counter must be read in the following sequence:

1. 7008 (H)
2. 7009 (H)
3. 700A (H)
4. 700B (H)

7008 (H) contains the LSB; 700B (H) contains the MSB. The Time Tag Resolution register sets the resolution of the counter (see Time Tag Resolution Register, page 4-21).

The counter is reset upon power-up, or software reset and stays reset until a Start command is issued. When a Start command is issued, the counter starts counting. To re-initialize to 0, write to the Time Tag Reset register. When it reaches the value FFFFFFFF (H), the counter wraps around to 0 and continues counting.

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4.15.3 Time Tag Reset Register

Address: 7007 (H) WRITE ONLY

Write to the Time Tag Reset register to reset the current bank's Time Tag Counter (data field = don't care). Immediately after the reset, the counter will start to count from 0.

NOTE The counter can also be reset from an external source (see Connectors, page 9-6).

4.15.4 Interrupt Reset Register

Address: 7001 (H)

To reset the Interrupt signal to the computer for the current bank, write to the Interrupt Reset register at the beginning of a user-written interrupt service routine (data field = don't care).

4.15.5 Software Reset Register

Address: 7000 (H)

Set the Software Reset register to reset the current bank (data field = don't care). See General Memory Map, page 2-1 for an explanation of the EXC-1553PC/EP "banks".

The bank will act as if the power had been switched *off* then *on*. After the reset operation is completed, the board writes to the Board status, the Board ID, Firmware revision, and Variable Amplitude Register registers.

WARNING *Software Reset erases all memory locations in the dual-port RAM.*

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4.15.6 Board Configuration Register

Address: 3FFF (H)

Use the Board configuration register to set the operating mode of the board.

Set the Board Configuration register before issuing a Start command to the board. To modify the Board Configuration register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 4-20).

Hex Value	Operating Mode
01	BC Mode
02	**RT Mode**
04	BC/Concurrent RT
08	BM Sequential Block Mode
10	BM Sequential Link List
20	BM Look-Up Table Mode
40	Reserved
80	Reserved
ED	Internal Loop Test (see Appendix D, Internal Loopback Test, page 11-8)
FF	External Loop Test (see Appendix E, External Loopback Test, page 11-9)

Board Configuration Register Values: RT Mode

4.15.7 Board ID Register

Address: 3FFE (H)

The Board ID register contains a fixed value that can be read by the user's initialization routine to detect the presence of the board. The one-byte value of this register is: 45 (Hex), ASCII value "E".

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4.15.8 Board Status Register

Address: 3FFD (H)

The Board Status register indicates the status of the board. In addition, this register indicates which options have been selected. Do not modify this register. Status bits are active if set to 1.

Bit	Description
07	1 = Board Type is EXC-1553PC/EP
06	X (Don't Care)
05	BM Time Tag Mode: 1 = 16-Bit Mode 0 = 32-Bit Mode
04	1 = Board Halted 0 = Board Running
03	1 = Self-Test OK
02	1 = Timers OK
01	1 = RAM OK
00	1 = Board Ready

Board Status Register

NOTE Board operation stops after the Start bit in the Start Register is cleared. Following this, the board sets bit 04 (Board Halted). Certain registers may be modified only after the Board Halted bit has been set. After receiving a subsequent Start command (by writing to the Start register), the board resets the Board Halted bit. The condition of this bit after power-up or software reset is logic 1.

4.15.9 Start Register

Address: 3FFC (H)

The Start register controls the Start/Stop operation of the board. To Start, and then Stop the RT operation, modify RT parameters (example: the Error Injection register or Response Time), and then issue a new Start command in real time.

For more information about bit 04 (Board Halted/Running) in the Board Status Register, see the note in Board Status Register

Bit	Description
01–07	0
00	1 = Start Operation 0 = Stop Operation

Start Register

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4.15.10 Message Status Register

Address: 3FFB (H)

The Message Status register indicates that a 1553 message has been received. A logic 1 indicates active condition. This bit is also set for messages with errors.

Bit	Description
01–07	0
00	Message Complete

Message Status Register

NOTE After reading, reset the Message Complete bit, the board does not reset this bit.

4.15.11 Time Tag Resolution Register

Address: 3FF7 (H)

The 8-bit value in the Time Tag Resolution register represents the resolution of the Time Tag Counter in units of 4 µsec.

To determine the Time Tag Counter's Resolution:

Time Tag Counter Resolution = (Time Tag Resolution register value + 1) x 4 µsec.

A value of 0 corresponds to a resolution of 4 microseconds; a value of 1 corresponds to a resolution of 8 microseconds, etc.

Set the Time Tag Resolution register before issuing a Start command to the board. To modify the Time Tag Resolution register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 4-20).

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4.15.12 Bit Count Register

Address: 3FF6 (H)

The Bit Count register sets the total number of bits within the 1553 word, including Sync(3) and Parity(1). This register is used by the board only if the Bit Count Error bit is set in the Error Injection register. If the Bit Error Count is not set, a (valid) 20-bit word is transmitted regardless of the contents of the Bit Count register.

Set the Bit Count register before issuing a Start command to the board. To modify the Bit Count register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 4-20).

Bit	Description			
03–07	0			
00–02	**Bit 02**	**Bit 01**	**Bit 00**	**No. of 1553 bits sent per word**
	0	0	0	18 (-2)
	0	0	1	22 (+2)
	0	1	0	19 (-1)
	0	1	1	20
	1	0	0	21 (+1)
	1	0	1	17 (-3)
	1	1	0	23 (+3)

Bit Count Register

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4.15.13 RT Response Time Register

Address: 3FF4 (H)

The RT Response Time register sets the Response Time of the Remote Terminal. The resolution of the Response Time register is 155 nsec. per bit, measured as the dead time on the 1553 bus. The minimum time is approximately 4 µsec., which is achieved by writing a 0 to this register. Any value above zero will result in a Response Time equal to 4 µsec. plus the contents of the register x 155 nsec. The actual response time has a tolerance of ± 1 µsec.

Set the Response Time register before issuing a Start command to the board. To modify the Response Time register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 4-20).

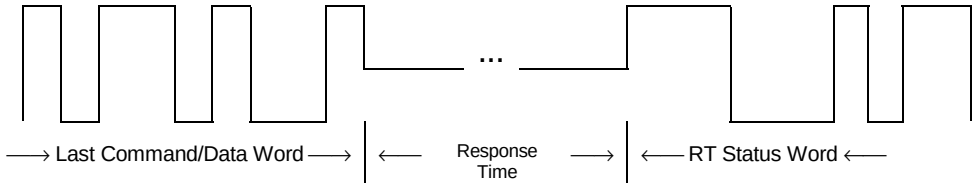


Figure 4-7 RT Response Time Definition

Example Setting RT Response Time Register

To request a response time of 9 µsec:

Write 32 to the RT Response Time register.

[32 x 0.155 ≅ 5 µsec] + 4 µsec = 9 µsec

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4.15.14 Error Injection Register

Address: 3FF3 (H)

The Error Injection register is a global register that allows the user to select the type of error to be injected in a transmitted message. When the board receives a Start command (issued by writing to the Start register), the board reads this register.

To modify the Error Injection register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 4-20).

Bit	Description
07	Data Word Sync Error (Data Words Sent With Command Sync)
06	Data Word Parity Error (Data Words Sent With Even Parity)
05	Status Word Synchronization Error (Status Word Sent With Data Sync)
04	Status Word Parity Error (Status Word Sent With Even Parity)
03	Reserved (Set to 0)
02	Non-Contiguous Data (Between First and Second Data Word)
01	Bit Count Error (see Bit Count Register page 4-22)
00	Reserved (Set to 0)

Error Injection Register

4.15.15 Variable Amplitude Register

Address: 3FF2 (H)

The Variable Amplitude register specifies the amplitude of the 1553 output signal. The signal can be programmed from 0 volts to 7.5 volts (peak-to-peak), when measured on the 1553 bus using 1553 coupling and 35-ohm load (that is, two 70-ohm termination resistors) as specified. If 78-ohm termination resistors are used, a higher Transmit (output) amplitude, will appear on the 1553 bus. The Variable Amplitude register has a resolution of 30 mV/bit (p-p) on the Bus.

Set the Variable Amplitude register before issuing a Start command to the board. To modify the Variable Amplitude register, issue a Stop command, modify, and then issue a Start command (see Start Register, page 4-20).

After a reset, the Variable Amplitude register defaults to FF (H), providing maximum amplitude.

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4.15.16 Message Stack Pointer

Address: 3FF0 (H)

This16-bit Message Stack pointer indicates the Message Stack position. After the entire message is received, the Message Stack pointer is updated (incremented by 6).

This word is initialized to 3300 (H) and circulates in the Message Stack between 3300 (H) to 33F6 (H).

4.15.17 Status Response Register

Address: 3FEF (H)

The Status Response register allows the user to control the Status Response mode of operation.

After a Receive message, respond with a 1553 Status word even if an invalid 1553 Data word was received. The user can also select a 1553 environment, which will affect some 1553 RT Status word bits (see 1553 RT Status Words, page 4-7).

Set the Status Response register before issuing a Start command to the board. To modify the Status Response register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 4-20).

Bit	Description
02–07	0
01	Environment: 0 = 1553B 1 = Non-1553B
00	On Error: 0 = Suppress Status 1 = Send Status

Status Response Register

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4.15.18 1760 Header Value Table

Address: 3F00–3F3F(H)

1760 option only

Write to the 1760 Header Value table to set the value you expect to receive in the first data word of the BC-to-RT or RT-to-RT message. The 1760 option provides predefined values, and these are preset on the EXC-1553PC/EP board (see below). The preset values can be changed by the user.

Address	Hex Value	Associated Subaddress
3F16 H	0400	11
3F1C H	0422	14

Receive Subaddresses: RT Mode

4.15.19 1760 Header Exist Table

Address: 3EC0–3EFF(H)

1760 option only

The 1760 Header Exist Table contains 32 entries corresponding to 32 RT subaddresses. Each entry may be set to indicate whether the board should expect a header word for BC-to-RT or RT-to-RT messages directed to that subaddress.

For those Header Value Table entries for which MIL-STD-1760B provides predefined values, the corresponding Header Exist Table entries are preset on the EXC-1553PC/EP board (see below). To set other values, enable the Header Exist Table entry for this RT (set it to 1) and write the value to the Header Value Table.

Bit	Description
01-15	Reserved
00	1 = Board should expect a Header word. 0 = Board should **not** expect a Header word

1760 Header Exist Table

Address	Hex Value	Associated Subaddress
3ED6 H	0001	11
3EDC H	0001	14

Receive Subaddresses: RT Mode

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4.15.20 Board Options Register

Address: 3E84 (H) READ ONLY

The Board Options register is a 16-bit register in which the low 8 bits are reserved. This register identifies the type of on-board firmware.

Bit	Description
10–15	Reserved
09	1 = 1760
08	1 = 1553
00–07	Reserved

Board Options Register

Address: 3E80 (H)

4.15.21 Firmware Revision Register

The Firmware Revision register indicates the revision level of the on-board firmware. The value 0001 0010 would be read as revision level = 1.2.

4.15.22 Interrupt Condition Register

Address: 33FC (H)

The Interrupt Condition register allows the user to enable an interrupt trigger. The Message Complete bit works in conjunction with the Interrupt bit in the Active RT table. When a message is received by an RT for which the Active RT interrupt bit is set, the board will check the Message Complete bit. If this bit is also set, an interrupt will be generated.

Set the Interrupt Condition register before issuing a Start command to the board. To modify the Interrupt Condition register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 4-20).

Bit	Description
02–07	0
01	1 = Message Complete
00	0

Interrupt Condition Register

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4.15.23 Mode Code Control Register

Address: 3266 (H)

The Mode Code Control register allows the user to specify which 1553 Subaddress value indicates the reception of a 1553 Mode command.

Set the Mode Code Control register before issuing a Start command. To modify the Mode Code Control register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 4-20).

Bit	Description		
02–07	0		
00–01	**Bit 01**	**Bit 00**	**Subaddresses Recognized as Mode Code**
	0	0	31 and 0
	0	1	0
	1	0	31
	1	1	0 and 31

Mode Code Control Register

4.15.24 Checksum Blocks Register

Address: 3264 (H)

1760 option only

Write a value to the Checksum Blocks register to set the data blocks for which the board should compute a checksum value. The board will compute a checksum value for those data blocks whose numerical index is less than the value stored in this register. Maximum value is 200.

Example Write 20 to the Checksum Blocks register when you want data blocks 0–19 to have a checksum value. This will cause the board to do the following:

1. Transmit a checksum value as the last word in the data block (transmit message).
2. Check the last word in the data block for a checksum value (receive message).

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5 BC/Concurrent-Remote Terminal Operation

Chapter 5 describes EXC-1553PC/EP operation in Bus Controller /Concurrent-Remote Terminal mode. The following topics are covered:

BC/Concurrent-RT Memory Map	page 5-3
Instruction Stack	page 5-4
Remote Terminal Simulation	page 5-13
Message Block Formats	page 5-14
Continuous or One-Shot Message Transfers	page 5-17
1760 Header Word **[1760 option only]**	page 5-18
Program Example: BC/Concurrent-RT Mode	page 5-19
Control Register Definitions	page 5-20

The EXC-1553PC/EP can operate simultaneously as the bus controller and up to 32 Remote Terminals. The messages and the instruction stack are loaded as for BC operation.

In BC/Concurrent-RT mode, load message blocks with the RTs 1553 Status and Data words for those Remote Terminals that you are actively simulating. These words must be loaded into the appropriate locations in the message blocks in the sequence that the 1553 words appear on the 1553 bus.

NOTE The requirement for loading the message blocks only applies to RTs that the user is actively simulating. For RTs that are not active (not simulated by the board in a single message), leave the corresponding locations blank in the associated 1553 message blocks.

The Remote Terminals simulated in BC/Concurrent-RT mode have a minimum response time of approximately 4 µsec.

In BC/Concurrent-RT mode, the board supports Minor Frame operation, a message type which functions as a “delay time” message, between groups of messages. Use the Minor Frame to produce a list of messages that will be sent out over the bus at different frequencies. In addition, Asynchronous Frames can be sent, so that in the middle of the transmission of the messages of a frame, the user can transmit another frame and then return to continue transmitting the messages of the previous frame.

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To determine that the board is installed and ready to operate:

Perform the following procedure *after* a power-up or a software reset.

1. Check the Board ID register (test for value = 45 H).
2. Check the Board Status register (test for Board Ready bit = 1).

The board is installed and ready when both registers contain the correct values (as written above). For software reset operations, set these values to 0 immediately prior to writing to the (software) Board Reset register.

NOTE Throughout this manual, writing a 1 to the Start register is referred to as "issuing a Start command."

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5.1 BC/Concurrent-RT Memory Map

Figure 5-1 below illustrates the BC/Concurrent-RT memory usage.

Interrupt Reset Register	7001 H
Software Reset Register	7000 H
Reserved	4000-6FFF H
Board Configuration Register	3FFF H
Board ID Register	3FFE H
Board Status Register	3FFD H
Start Register	3FFC H
Interrupt Condition Register	3FFB H
Message Status Register	3FFA H
RT Response Time Register	3FF9 H
Reserved	3FF7-3FF8 H
Loop Count Register	3FF6 H
Bit Count Register	3FF5 H
Word Count Register	3FF4 H
BC Response Time Register	3FF3 H
Variable Amplitude Register	3FF2 H
Stack Pointer	3FF0 H
Frame Time Register	3FEE H
Frame Time Resolution Register	3FEC H
Instruction Counter	3FEB, 3FEA H
Minor Frame Time Register	3FE8 H
Minor Frame Resolution Register	3FE6 H

Reserved	3F80-3FE5 H
1760 Header Value Table *	3F40-3F7F H
Reserved	3F00-3F3F H
1760 Header Exist Table *	3EC0-3EFF H
Reserved	3E86-3EBF H
Board Options Register (16 bits)	3E84 H
Reserved	3E81-3E83 H
Firmware Revision Register	3E80 H
Reserved	3425-3E7F H
Asynchronous Start Flag Register	3424 H
Asynchronous Frame Pointer Reg.	3422 H
Asynchronous Message Count Reg.	3420 H
Active RT Table (32 Bytes)	3400-341F H
Instruction and Message Block Area	0000-33FF H

Figure 5-1 BC/Concurrent-RT Memory Map

*1760 option only

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5.2 Instruction Stack

Use the Instruction stack to program the board. The stack is divided into instruction blocks, each containing four words. The block contains control information (that the user writes) and status information (that the board writes). Figure 5-2 illustrates one instruction block.

Control and status information is stored in the memory in the following sequence:	**Byte Offset**
Message Status Word	**6**
Intermessage Gap Time Counter	**4**
Intermessage Gap Time	**2**
Message Block Pointer	**0**

Figure 5-2 Instruction Block Structure: BC/Concurrent-RT Mode

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5.2.1 Message Status Word

The Message Status word indicates the status of the message transfer. This word is created by the board. Do not confuse this word with the 1553 Status word (see 1553 RT Status Words page 4-7). The contents of the Message status word are described below.

NOTE A logic 1 indicates occurrence of status flag.

Bit	Bit Name	Description
15	**End Of Message**	Message transfer completed.
14	**Checksum Error**	The computed checksum (on an incoming message) does not match when checked against the last Data Word received. **[1760 Option only]** See MIL-STD-1760B Considerations, page 1-4.
13	**Incorrect 1553 Bus**	Remote Terminal response was not received on the active 1553 bus.
12	**Message Error Bit Set**	Message Error bit (bit 10) in the RT Status word was set.
11	**RT Status Bit Set**	A bit was set in the RT Status word (other than the Message Error bit). The error bit is not set in conjunction with this bit.
10	**Invalid Message Error**	A 1553 message-level error occurred (e.g. Word count, incorrect sync); details in the bits described below.
09	**Response Time Failure**	RT responded late (see BC Response Time Register, page 5-26).
08	**1760 Header Word**	Header Word received does not match the value set in the Header Value table. **[1760 Option only]** See MIL-STD-1760B Considerations, page 1-4
07	**Invalid Word Received**	At least one invalid 1553 word received (e.g., bit count, Manchester code, parity).
06	**Word Count High**	RT transmitted too many words.
05	**Word Count Low**	RT transmitted too few words.
04	**Incorrect RT Address**	1553 Status word received did not contain the correct RT address.
03	**Incorrect Sync Received**	Sync of either the status or data word(s) is incorrect.
02	**Non-Contiguous Data**	Invalid gap between received 1553 words.
01	**Reserved**	Set to 0
00	**Error**	Error occurred. (The error type is defined in one of the other message status bit locations.)

Message Status Word

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NOTE To ensure data integrity, the board sets a special status value of 7F00 (H) to indicate that the message is currently being transmitted. This alerts the user *not* to alter this message now. Check this value *before* attempting to change the data words of the message. Otherwise, the results are indeterminate.

5.2.2 Intermessage Gap Time

The Intermessage Gap Time value is a 16-bit word written by the user, allowing for the insertion of a unique intermessage delay time between the current message and the next message. The minimum Intermessage Gap Time is approximately 4 µsec. The maximum Intermessage Gap Time is approximately 10 msec that can be extended up to approximately 80 sec. using the IGT Counter value (see below). The value in the word is added to this minimum time. The resolution of this word is 155 nsec. per bit.

5.2.3 Intermessage Gap Time Counter

The Intermessage Gap Time counter (IGT_counter) is a 16-bit word written by the user, allowing to increase the Intermessage Gap Time by repeating the number of times the Intermessage Gap Time value is used (bits 00–12). Use bit 13 in this register to instruct the board to generate an interrupt when this specific message completed. Bits 14 and 15 allow the user to generate a checksum and inject an incorrect value into the checksum (see MIL-STD-1760B Considerations, page 1-4).

Bit	Bit Name	Description
15	**Chk_Sum_On**	Generates a checksum **[1760 option only]**
14	**Chk_Sum_Err_Inj**	Injects an incorrect value into the checksum **[1760 option only]**
13	**Int_On_Select_Msg**	1 = Generate an interrupt when this specific message is completed. To set general interrupt conditions, see Interrupt Condition Register page 5-22.
00–12	**IGT_counter**	Write a value to increase the Intermessage Gap Time by repeating the number of times the Intermessage Gap Time value is used. For example, if the counter is set to 0, then the gap time is not repeated; and depends on the contents of the Intermessage Gap Time location. If the gap time counter is 1, then the gap time is repeated once and equals the Intermessage Gap Time value × 2, etc. **Note**: To ensure maximum Intermessage Gap Time accuracy when using the IGT_counter, use the largest possible value for the Intermessage Gap Time word and the smallest value for the IGT_counter, for a given desired intermessage gap time.

Intermessage Gap Time Counter

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5.2.4 Message Block Pointer

The Message Block pointer is a 16-bit word, written buy the user, that points to the beginning of a 1553 message block.

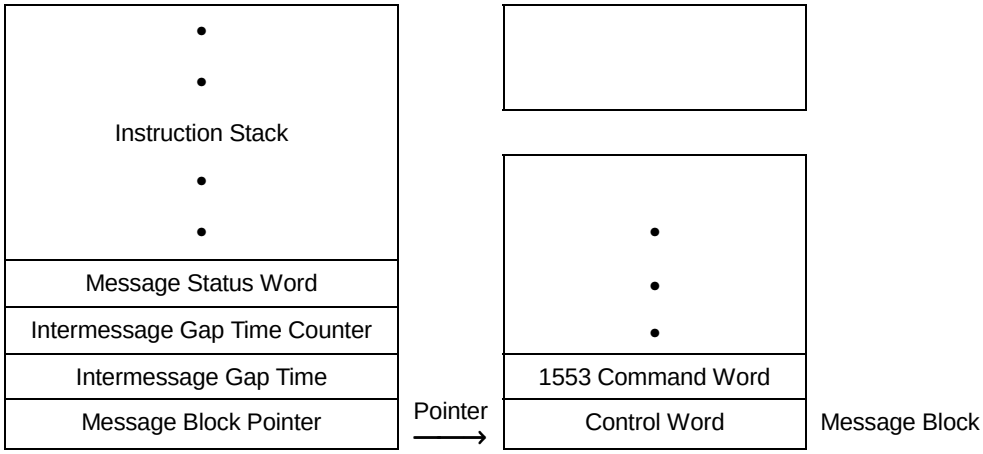


Figure 5-3 Message Block Pointer: BC/Concurrent-RT Mode

5.2.5 Message Block

The message block can be loaded anywhere in the Instruction Stack/Message Block area (see BC/Concurrent-RT Memory Map page 5-3). Message blocks do not have to be stored in sequential locations in the memory since the Message Block pointers “point” to the message blocks in sequence.

Each block contains a 1553 message plus its Control word. This Control word is written into the first word of each block. The Control word instructs the board which type of message to transmit (i.e., RT to RT, Mode code, Broadcast, Error injection, etc.). The size of the message block is variable and depends on the size of the message itself.

The descriptions of the various message block formats (i.e., BC to RT, RT to BC and RT to RT) are illustrated in Message Block Formats, page 5-14.

The description of each bit in the Control word follows.

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5.2.6 Control Word

NOTE Logic 1 enables the function; 0 disables the function.

Bit	Bit Name	Description
15	**Stop On Error**	Message error stops BC operation. You can restart by writing to the Instruction Count register and issuing a Start command.
14	**Parity Error**	Selects Even parity in 1553 word.
13	**Halt/Continue**	1 = Halt; stops BC transfer operation. This bit must be reset to 0 to Run or Continue.
12	**Word Count Error**	Transmits fewer or more words than are indicated by the Word Count field (see Word Count Register, page 5-25). This function is valid for BC to RT messages only.
11	**Bit Count Error**	Transmits invalid number of bits in 1553 words (see Bit Count Register, page 5-24).
10	**Incorrect Sync**	Transmits incorrect sync. Data type Sync is transmitted in the Command word.
09	**Non-Contiguous Data**	Transmits the first 1553 Data word with invalid Gap Time (between Command and Data word).
08	**Error Placement/ Error Injection Enable**	For BC-to-RT, Broadcast Receive, and Mode Code with Data messages, bit 08 selects the Parity, Sync, and Bit Count error injection placements: 0 in Command word 1 in Data words For other error injection types or other message types, this bit must be set (=1) to enable error injection.
07	**Bus A/B**	Selects active 1553 bus: logic 1 selects bus A; logic 0 selects bus B.
06	**Auto Bus Switch**	On error, the BC will retry message transfer on alternate bus. (Note: Auto-retry must be selected.)
04-05	**Auto Retry Code**	On error, selects the number of retries before transferring the next message:

Bit 05	Bit 04	Description
0	0	No Retry
0	1	1 Retry
1	0	2 Retries
1	1	3 Retries

00-03 **Command Code**					
	03	**02**	**01**	**00**	**Description**
	0	0	0	0	Transmit command (RT to BC)
	0	0	0	1	Receive command (BC to RT)
	0	0	1	0	RT-to-RT command
	0	0	1	1	Mode code
	0	1	0	0	Broadcast Receive command
	0	1	0	1	Broadcast RT-to-RT command
	0	1	1	0	Broadcast Mode code
	0	1	1	1	Skip Message (see Skip Message Operation, page 5-9)
	1	0	0	0	Jump command (see Jump Command Operation, page 5-10)
	1	1	1	1	Minor Frame command (see Minor Frame Operation, page 5-11)

BC/RT Control Word

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5.2.7 Halt Operation

Set the Halt Operation bit to logic 0 before writing to the Start register. In real-time (during BC execution) set this bit to logic 1. When operating on that particular message block's Control word, the board will halt transfer operations until the bit is reset to logic 0.

When the board detects that the Halt bit is set, it sets the Wait For Continue bit in the Message Status register (see Control Register Definitions page 5-20). Use the Wait For Continue bit to find out when the board has arrived at the halted instruction block. When the board detects that you have reset the Halt bit (Continue Mode), the board will reset the Wait For Continue bit in the Message Status Register and continue BC operation.

The Halt operation can be implemented only in message blocks that have *not* (as yet) been executed by the board.

NOTE The Halt operation can be used in conjunction with the Jump command described below (see Jump Command Operation, page 5-10).

5.2.8 Skip Message Operation

The Skip Message command allows the user to skip a message defined in a certain message block. To use Skip Message operation, modify the Command field in the Control word. This lets you selectively send a message in the current frame. The "skip" takes place immediately and does not wait until the Intermessage Gap Time expires.

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5.2.9 Jump Command Operation

To modify the board's BC transfer cycle, set the Jump command in the BC Control word. The Jump command instructs the board to operate on a new instruction stack or new stack entry in the same stack. This Control word is followed by a Stack Pointer word instead of the usual 1553 command word. In addition, the stack pointer is followed by an Instruction Count value. The Jump command is tested *after* the board has tested the Halt/Continue bit in the Control word. The "jump" takes place immediately and does not wait until the Intermessage Gap Time expires.

The memory structure of the jump command is illustrated in Figure 5-4 below.

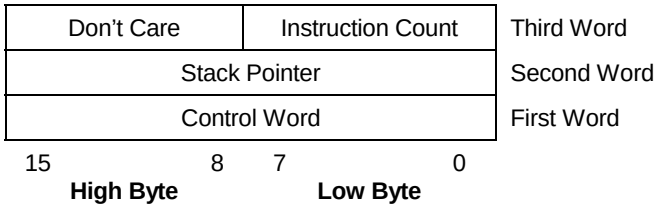


Figure 5-4 Jump Command Memory Structure

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5.2.10 Minor Frame Operation

Use the Minor Frame type of message in the following ways:

- To function as a “delay time” message between groups of messages.
- To produce a list of messages that will be sent out over the bus at different frequencies.

Minor Frame time is defined as the time elapsed from the beginning of a Minor Frame to beginning of the next Minor Frame. To set up Minor Frame operation, begin each Minor Frame with a Minor Frame command (see Minor Frame Time Register and Minor Frame Resolution Register page 5-29). The maximum value possible for the Minor Frame Time is 16 sec.

The example in Figure 5-5 shows a configuration of four minor frames, in which Message A is sent in every frame, Message B is sent in every other frame, and Message C is sent once. Each Minor Frame goes out at 10 msec. (100Hz). If each minor frame is 10 msec. long, Message A is sent every 10 msec., Message B is sent every 20 msec., and Message C is sent every 40 msec.

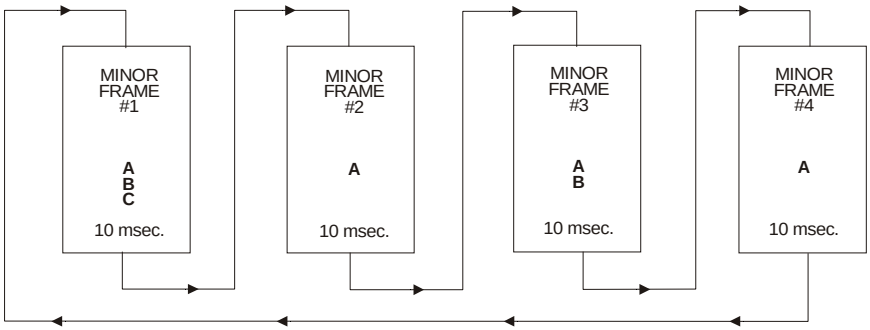


Figure 5-5 Minor Frame Sequencing

NOTE 1. The MINOR_FRAME message does not appear as a real message on the data bus.

2. Frame Time should not exceed the total time of all the minor frames in the minor frame sequence (see Frame Time Register, page 5-27.)

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5.2.11 Asynchronous Frame Operation

During standard operation, the board sets up a frame of messages and then sends them out synchronously over the bus. The user can set up multiple frames of messages, and select which one to send out.

Asynchronous Frame operation allows for the transmission of a frame asynchronously, this means that in the middle of the transmission of the messages of a frame (frame 1), another frame (frame 2) can be transmitted, and then return to continue transmitting the messages of the previous frame (frame 1).

To transmit an asynchronous frame, write the number of messages in the asynchronous frame into the Asynchronous Message Count register, place a pointer to the beginning of the asynchronous frame in the Asynchronous Frame Pointer register, and then set the Asynchronous Start Flag register to a non-zero value. This will send out the asynchronous frame over the bus (see Asynchronous Start Flag Register, Asynchronous Frame Pointer Register, Asynchronous Message Count Register, page 5-31).

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5.3 Remote Terminal Simulation

When the board is simulating both the Bus Controller and one or more Remote Terminals, you must write the simulated Remote Terminal 1553 Status word and Data word(s) into the message block in the sequence in which they are to be transmitted over the 1553 bus (see Message Block Formats, page 5-14).

To indicate to the board that Remote Terminals are to be simulated, write to the 32-byte Active Remote Terminal table. Each entry in the 32-byte table corresponds to a specific Remote Terminal.

The first byte is for RT #0, the second to RT #1, and the last byte is for RT #31 (for a total of 32 locations). A table entry value of 1 enables the Remote Terminal simulation by the board; a value of 0 disables the simulation by the board.

RT #31 Active RT byte	341F H
RT #30 Active RT byte	
• • •	
RT #0 Active RT byte	3400 H

Figure 5-6 Active RT Table: BC/Concurrent-RT Mode

Bit	Description
01-07	0
00	1 = Enabled; 0 = Disabled

Active RT Byte Definition: BC/Concurrent-RT Mode

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5.4 Message Block Formats

The Message block contains, or will contain after response from an RT, the entire 1553 message as it appears on the 1553 bus, including Command word(s), Data word(s), and Status word(s).

Examples of Message block formats follow.

Example No. 1: Transmit Command Operating as BC Only

Block *before* execution

1553 Transmit Command	
Control Word	First Location In Block

Block *after* execution

1553 Data Word	From Transmitting Remote Terminal (Not Simulated)
•	•
•	•
1553 Data Word	•
RT Status Word	From Transmitting Remote Terminal (Not Simulated)
1553 Transmit Command	
Control Word	First Location In Block

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Example No. 2: Receive Command Operating as Both BC and Receiving RT

Block *before* execution

RT Status Word	Simulated By EXC-1553PC/EP (Loaded by User)
1553 Data Word	•
•	•
•	•
1553 Data Word	Simulated By EXC-1553PC/EP (Loaded by User)
1553 Receive Command	
Control Word	First Location In Block

Block *after* execution

RT Status Word	
1553 Data Word	
•	
•	
1553 Data Word	
1553 Receive Command	
Control Word	First Location In Block

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Example No. 3: RT-to-RT Command Operating as BC and Receiving RT

Block *before* execution

(Receive) RT Status Word	Simulated By EXC-1553PC/EP (Loaded By User)
Leave Empty For Data +N	
•	
•	
Leave Empty For Data #1	
Leave Empty For (Transmit) RT Status Word	
1553 Transmit Command	
1553 Receive Command	
Control Word	First Location In Block

Block *after* execution

(Receive) RT Status Word	
1553 Data Word	From Transmitting Remote Terminal (Not Simulated)
•	•
•	•
1553 Data Word	•
(Transmit) RT Status Word	From Transmitting Remote Terminal (Not Simulated)
1553 Transmit Command	
1553 Receive Command	
Control Word	First Location In Block

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5.5 Continuous or One-Shot Message Transfers

The board can transfer all programmed messages once, in a continuous loop, or for *n* number of times.

In One-Shot mode, (after receiving a Start command) the board transfers all messages, sets the Message Complete bit in the Message Status register, issues an interrupt (if programmed), and waits for a new Start command. Use the Start register (see Start Register, page 5-22) to select One-Shot mode.

In *n*-Times mode, load the Loop Count register with the number of times to transmit the messages frame. Then set the Loop and Start bits in the Start register. The user can transmit 1–255 times (see Start Register, page 5-22 and Loop Count Register page 5-24). The time between frames is determined by the Frame Time register (see Frame Time Register page 5-27).

In Continuous Loop mode, the board will retransmit the message frame at a predetermined, user-programmable rate. Use the Start register and the Loop Count register (see Start Register, page 5-22 and Loop Count Register page 5-24) to select Continuous Loop mode. In Continuous Loop mode, all messages relating to the (active) Stack pointer and Instruction counter are continuously looped until you halt the board's operation (see Start Register, page 5-22).

The Loop time or Frame time is a function of two control register pairs: the Frame Time registers (high and low) and the Frame Time Resolution registers (high and low). The internal Frame Time counter is loaded when a Start command with the 16-bit value found in the Frame Time registers (high and low) is received. The Frame Time Counter is decremented every *n* x 155 nsec, where *n* is the value of Frame Time Resolution registers (high and low). After all instructions are executed (1 frame), the board waits until the internal Frame Time counter reaches 0 before transmitting the next frame.

NOTE If the Frame time is less than the time required to transmit all messages within 1 frame, the subsequent frames will be transmitted with the minimum delay between them. The minimum delay is approximately 20 µsec, measured as dead time on the bus.

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To implement the desired Frame time program the appropriate combinations of the two register pairs. An example using one method is described below.

Example Calculating Frame Time

Given: Frame time of 500 msec. is required.

Method:

Select Frame Time Resolution of 3225 (Dec) → 0C99 (H)

Frame Time Resolution = 3225 x 155 nsec = 500 µsec (.5 msec)

Subsequently, the Frame Time register value must be equal to:

$$\frac{[500 \text{ msec (desired time)} \ / \ .5 \text{ msec} = 1000 \text{ (Dec)}] - 1}{\text{Count} - 1} \rightarrow 03E7 \text{ (H)}$$

Before issuing the Start command, set:

- Frame Time register low = E7 (H)
- Frame Time register high = 03 (H)
- Frame Time Resolution register low = 99 (H)
- Frame Time Resolution register high = 0C (H)

5.5.1 Mode Codes

The board handles all dual-redundant 1553B Mode codes; the Word Count field is decoded according to MIL-STD-1553B. The two Quad-Redundant Mode codes, Selected Transmitter Shutdown and Override Selected Transmitter Shutdown, are not implemented by the board.

5.6 1760 Header Word

1760 Option only

With the 1760 option the first data word of a message may be a header word, which is used for message identification. The header word is associated with a specific RT subaddress.

To indicate that a specific subaddress will require a header word, you must set the corresponding entry in the 1760 Header Exist table to 1. Then set the corresponding entry in the 1760 Header Value table to the value you expect to receive in the first data word of the message. The 1760 option provides predefined values, and these are preset on the EXC-1553PC/EP board.

For descriptions of the 1760 Header Value Table and 1760 Header Exist Table, see page 5-30.

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5.7 Program Example: BC/Concurrent-RT Mode

NOTE All values are in HEX unless otherwise stated.

BASIC Instruction	Remarks
`10 POKE &H3FFF,04`	Set Configuration register to BC/RT mode.
`20 POKE &H3FF0,00`	Set Stack Pointer registers to 0000.
`30 POKE &H3FF1,00`	(stack now begins at address: 0000)
`40 POKE &H3FF2,&HFF`	Set Variable Amplitude register.
`50 POKE &H00,00`	Pointer to first message:
`60 POKE &H01,01`	[Location of message is 0100 H]
`70 POKE &H02,xx`	Set Intermessage Gap Time location.
`80 POKE &H03,xx`	
`90 POKE &H08,&H40`	Pointer to second message:
`100 POKE &H09,01`	[Location of message is 0140 H]
`110 POKE &H0A,xx`	Set Intermessage Gap Time location.
`120 POKE &H0B,xx`	
`130 POKE &H100,&H80`	Set Control word to Transmit command,
`140 POKE &H101,00`	Bus A, and no errors injected.
`150 POKE &H102,&H23`	Set Command word to 0C23 H
`160 POKE &H103,&H0C`	
`170 POKE &H104,&H00`	Set Status word to 0800 H
`180 POKE &H105,&H08`	
`190 POKE &H106,&Hxx`	Set Data word to xxxx.
`200 POKE &H107,&Hxx`	
`210 POKE &H108,&Hyy`	Set Data word to yyyy.
`220 POKE &H109,&Hyy`	
`230 POKE &H10a,&Hzz`	Set Data word to zzzz.
`240 POKE &H10b,&Hzz`	
`250 POKE &H140,02`	Set Control word to RT-to-RT command,
`260 POKE &H141,00`	Bus B, and no errors injected.
`270 POKE &H142,&H23`	Set first (Receive) Command word to 3823 H.
`280 POKE &H143,&H38`	
`290 POKE &H144,&H43`	Set second (Transmit) Command word to 1C43 H.
`300 POKE &H145,&H1C`	
`310 POKE &H3FEB,2`	Set Instruction Counter to 2 (i.e. 2 messages)
`320 POKE &H3FEC,xx`	Set Frame Time Resolution registers.
`330 POKE &H3FED,xx`	
`340 POKE &H3FEE,xx`	Set Frame Time registers
`350 POKE &H3FEF,XX`	
`360 POKE &H3401,1`	Enable RT #1. Use the Active RT's Look-up table to enable RTs. Board will simulate enabled RTs.
`370 POKE &H3FFC,1`	Set Start register to 1. Starts message transfers in One-Shot mode.
`380 STOP`	

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5.8 Control Register Definitions

5.8.1 Interrupt Reset Register

Address: 7001 (H)

To reset the Interrupt signal to the computer for the current bank, write to the Interrupt Reset register at the beginning of a user-written interrupt service routine (data field = don't care).

See General Memory Map, page 2-1 for an explanation of the EXC-1553PC/EP "banks".

5.8.2 Software Reset Register

Address: 7000 (H)

Write to the Software Reset register to reset the current bank (data field = don't care). The bank will act as if power had been switched OFF, then ON. The Board status, the Board ID, Firmware revision and Variable Amplitude registers are written by the board after the reset operation has been completed.

WARNING *Reset erases all memory locations in the dual-port RAM.*

5.8.3 Board Configuration Register

Address: 3FFF (H)

Before issuing a Start command to the board, set the operating mode of the board via the Board Configuration register. To modify the Board Configuration register, issue a Stop command, write one of the hex values to the register, and then issue a Start command (see Start Register, page 5-22).

Hex Value	Operating Mode
01	BC Mode
02	RT Mode
04	**BC/Concurrent-RT Mode**
08	BM Sequential Block Mode
10	BM Sequential Link List
20	BM Look-Up Table Mode
40	Reserved
80	Reserved
ED	Internal Loop Test (see Appendix D, Internal Loopback Test, page 11-8)
FF	External Loop Test (see Appendix E, External Loopback Test, page 11-9)

Board Configuration Register Values: BC/RT Mode

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5.8.4 Board ID Register

Address: 3FFE (H)

The Board ID register contains a fixed value that can be read by your initialization routine to detect the presence of the board. The one-byte value of this register is: 45 (Hex), ASCII value "E".

5.8.5 Board Status Register

Address: 3FFD (H)

The Board Status register indicates the status of the board. In addition, this register indicates which options have been selected, as described below. Do not modify this register. Status bits are active if set to 1.

Bit	Description
07	1 = Board Type is EXC-1553PC/EP
06	X (Don't Care)
05	BM Time Tag Mode: 1 = 16-Bit Mode 0 = 32-Bit Mode
04	1 = Board Halted 0 = Board Running
03	1 = Self-Test OK
02	1 = Timers OK
01	1 = RAM OK
00	1 = Board Ready

Board Status Register

NOTE Board operation stops after you clear the Start bit in the Start Register. Following this, the board sets bit 04 (Board Halted). Certain registers may be modified only after the Board Halted bit has been set. After receiving a subsequent Start command (by writing to the Start register), the board resets the Board Halted bit. The condition of this bit after power-up or software reset is logic 1.

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5.8.6 Start Register

Address: 3FFC (H)

The Start register controls the Start/Stop operation of the board. Writing the appropriate bit (bit 00) to the Start register starts the Bus Controller transfer operation.

When operating in Continuous Loop or *n*-Times mode, set the Start and Loop bits in the Start register. The Loop and *n*-Times number are selected via the Loop Count register. In the One-Shot and *n*-Times modes, the board resets the Start bit in the register after *all* messages have been transferred. The board does not reset any bit while in Continuous Loop mode.

To halt the Loop operation between messages, set bit 00 to 0. To halt the operation at the end of the entire frame, set bit 02 to 0 (bit 02 is not tested between message transfers). Related data bit 04 in the Board Status register indicates when the board has been halted (see Board Status Register, page 5-21).

Bit	Description
03-07	0
02	1 = Loop Mode 0 = One-Shot Mode
01	0
00	1 = Start Operation 0 = Stop Operation

Start Register

5.8.7 Interrupt Condition Register

Address: 3FFB (H)

The Interrupt Condition register allows you to set interrupt triggers. When a condition that is enabled in this register occurs, an interrupt is generated. To determine which condition caused the interrupt, check the Message Status register.

Set the Interrupt Condition register before issuing a Start command to the board. To modify the Interrupt Condition register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 5-22).

NOTE The interrupt will be sent at the end of the message for all interrupt conditions.

Bit	Description
04-07	0
03	1 = Message Error
02	1 = End Of Frame
01	1 = Message Complete
00	0

Interrupt Condition Register

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5.8.8 Message Status Register

Address: 3FFA (H)

The Message Status register indicates the status of the current message being processed. The definition of each status bit is given below. Logic 1 indicates that the condition is activated.

Bit	Bit Name	Description
04-07	**0**	
03	**Message Error**	The message has been sent. As a result, the Error bit has been set in the Message Status word.
02	**End Of Frame**	The last word of the last message in the frame has been sent.
01	**Message Complete**	The last word of the message has been sent.
00	**Wait For Continue**	A message with the Halt bit set has been encountered. Reset the Halt bit in the Control word to continue.

Message Status Register

NOTE Status bits are *not* reset by the board. After reading them, the user must reset them.

5.8.9 RT Response Time Register

Address: 3FF9 (H)

The RT Response Time register sets the Remote Terminal's Response Time. The resolution of the Response Time register is 155 nsec. per bit, measured as the dead time on the 1553 bus. The minimum time is approximately 4 µsec. The value in the register is added to the minimum time. The actual Response Time has a tolerance of ±1 µsec.

Set the Response Time register before issuing a Start command to the board. To modify the Response Time register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 5-22).

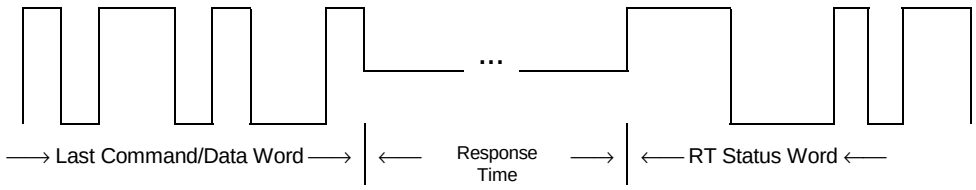


Figure 5-7 RT Response Time Definition

Example Setting the RT Response Time Register

To request a response time of 9 µsec:
Write 32 to the RT Response Time register.
[32 x 0.155 ≅ 5 µsec] + 4 µsec = 9 µsec.

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5.8.10 Loop Count Register

Address: 3FF6 (H)

The Loop Count register is used in conjunction with the Loop bit in the Start register. If the Loop bit in the Start register is set, then set the Loop Count register to specify the number of times the Message frame will be transmitted. A value of 0 is interpreted as a request for continuous looping. Set the Loop Counter register before issuing a Start command to the board. To modify the Loop Counter register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 5-22).

Bit	Value	Description
00-07	**0**	Transmits in Continuous Loop
	1–255	Sends Message Frame *n*-times (1–255) as defined

Loop Count Register

5.8.11 Bit Count Register

Address: 3FF5 (H)

The Bit Count register sets the total number of bits in the 1553 word, including Sync(3) and Parity(1). This register is used by the board only for messages for which the Bit Count Error bit is set in the Control Word of the Message Block (see Control Word, page 5-8). If the Bit Count Error bit is not set, a (valid) 20-bit word is transmitted regardless of the contents of the Bit Count register.

Set the Bit Count register before issuing a Start command to the board. To modify the Bit Count register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 5-22).

Bit	Description			
03–07	0			
00–02	**Bit 02**	**Bit 01**	**Bit 00**	**No. of 1553 bits sent per word**
	0	0	0	17 (-3)
	0	0	1	18 (-2)
	0	1	0	19 (-1)
	0	1	1	20
	1	0	0	21 (+1)
	1	0	1	22 (+2)
	1	1	0	23 (+3)

Bit Count Register

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5.8.12 Word Count Register

Address: 3FF4

The Word Count register controls the number of 1553 data words (± 3) in the message and allows you to inject a Word Count error. The error is an offset relative to the 1553 Command word Word Count field. This register is used by the board only for messages for which the Word Count Error bit is set in the Control word register (see Control Word page 5-8). If the Word Count Error bit is not set, a correct number of words is transmitted regardless of the contents of the Word Count register.

Set the Word Count register before issuing a Start command to the board. To modify the Word Count register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 5-22).

Register Value	Word Count Offset
FD H	–3 Words
FE H	–2 Words
FF H	–1 Word
00 H	No Error Injection
01 H	+1 Word
02 H	+2 Words
03 H	+3 Words

Word Count Register Values

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5.8.13 BC Response Time Register

Address: 3FF3 (H)

The BC Response Time register sets the BC's Response Time window, whose value determines the maximum wait time until an RT's Status Response is considered invalid by the BC. The resolution of the BC Response Time register is 155 nsec. per bit, measured as the dead time on the 1553 bus. The minimum time is approximately 2 μsec.

Set the BC Response Time register before issuing a Start command to the board. To modify the BC Response Time register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 5-22).

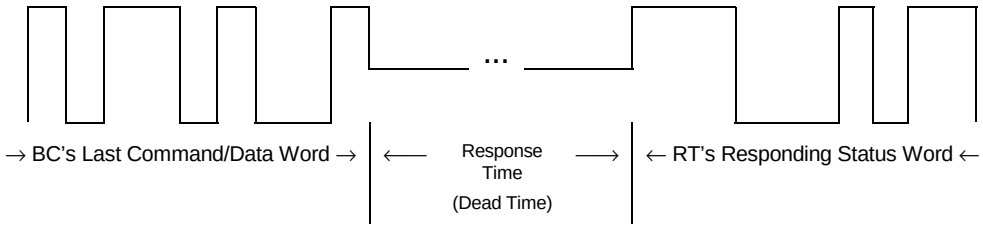


Figure 5-8 BC Response Time Definition

Example Setting the BC Response Time Register:

To set up a BC response time of 14 μsec:
Write 90 to the BC Response Time register.
90 x 0.155 ≅ 14 μsec

5.8.14 Variable Amplitude Register

Address: 3FF2 (H)

The Variable Amplitude register specifies the amplitude of the 1553 output signal. The signal can be programmed from 0 volts to 7.5 volts (peak-to-peak) when measured on the 1553 bus using 1553 direct coupling and 35-ohm load, that is, two 70-ohm termination resistors. If 78-ohm termination resistors are used, a higher transmit (output) amplitude will appear on the 1553 bus. The Variable Amplitude register has a resolution of 30 mV/bit (peak-to-peak) on the bus.

Set the Variable Amplitude register before issuing a Start command to the board. To modify the Variable Amplitude register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 5-22). After a reset, the Variable Amplitude register defaults to FF (H), providing maximum amplitude.

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5.8.15 Stack Pointer

Address: 3FF0 (H)

This 16-bit Stack pointer points to the Instruction stack. The Instruction stack can reside anywhere between the locations 0000 (H) and 33FF (H). Set the Stack Pointer register before issuing a Start command to the board. To modify the Stack Pointer register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 5-22).

5.8.16 Frame Time Register

Address: 3FEE (H)

This Frame Time register contains the 16-bit Frame Time value for Continuous and *n*-Times modes operation. The value written to the Frame Time register is multiplied by the value set in the Frame Time Resolution register described in Calculating Frame Time, page 5-18. The value set must equal the desired multiplication factor – 1.

Set the Frame Time register before issuing a Start command to the board. To modify the Frame Time register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 5-22).

5.8.17 Frame Time Resolution Register

Address: 3FEC (H)

This 16-bit Frame Time Resolution value represents the resolution of the Frame Time counter in increments of 155 nsec. (see also Continuous or One-Shot Message Transfers page 5-17).

Set the Frame Time Resolution register before issuing a Start command to the board. For an example of how to calculate Frame Time and Frame Time Resolution, see Calculating Frame Time, page 5-18. To modify the Frame Time Resolution register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 5-22).

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5.8.18 Instruction Counter

Address: 3FEB, 3FEA (H)

The Instruction Counter must be loaded with the number of instructions (1553 Messages) to execute in the current frame. The value must be greater than 0 before you write to the Start register to begin a transmission. Set the Instruction counter to 1 for one message, 2 for two messages, etc. The board updates the Instruction counter by decrementing the value and writing it back to memory at the end of each message transfer.

Set the Instruction Counter register before issuing a Start command to the board. To modify the Instruction Counter register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 5-22). When in the Continuous Loop mode, the Instruction Counter register cycles from the initial value down to 1.

The low register (3FEA) contains the MSB, the high register (3FEB) contains the LSB. Therefore, for an Instruction Counter less than 256, use the LSB address only, address 3FEB.

The high register is available starting with Firmware revision 4.9.

5.8.19 Minor Frame Time Register

Address: 3FE8 (H) WRITE

This 16-bit Minor Frame Time register is used to set the length of a single minor frame (see Minor Frame Operation page 5-11). The resolution of the Minor Frame Time register is 1 µsec. per bit. The maximum value is approximately 65 msec., which can be extended by the multiplier set in the Minor Frame Time Resolution register described below.

Set the Minor Frame Time register before issuing a Start command to the board. To modify the Minor Frame Time register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 5-22).

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5.8.20 Minor Frame Resolution Register

Address: 3FE6 (H) WRITE

The Minor Frame Resolution is a multiplier of the Minor Frame Time described above. The value written to the Minor Frame Resolution register allows the user to extend the Minor Frame Time beyond the 65 msec. maximum in the Minor Frame Time register. The maximum Minor Frame Resolution is 255. The maximum Minor Frame Time possible using both registers is approximately 16 sec.

Example To generate a Minor Frame Time of 1 sec., set the Minor Frame Time register to F424 (H) (62,500 Dec.), and set the Minor Frame Resolution register to 10 (H) (16 Dec.).

Set the Minor Frame Time Resolution register before issuing a Start command to the board. To modify the Minor Frame Time Resolution register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 5-22).

5.8.21 1760 Header Value Table

Address: 3F40–3F7F(H)

1760 option only

Write to the 1760 Header Value table to set the value you expect to receive in the first data word of the RT-to-BC or RT-to-RT message.

The 1760 option provides predefined values. These are preset on the EXC-1553PC/EP board (see below). The preset values can be reset by the user.

Address	Hex Value	Associated Subaddress
3F42 H	0421	1
3F56 H	0420	11
3F5C H	0423	14

Transmit Subaddresses: BC/Concurrent-RT Mode

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5.8.22 1760 Header Exist Table

Address: 3EC0-3EFF (H)

1760 option only

The 1760 Header Exist table contains 32 entries corresponding to 32 RT subaddresses. Each entry may be set to indicate whether, or not, the board should expect a header word for RT-to-BC or RT-to-RT messages directed to that Subaddress.

For those Header Value Table entries for which MIL-STD-1760B provides predefined values, the corresponding Header Exist Table entries are preset on the EXC-1553PC/EP board (see below). To set other values, enable the Header Exist Table entry for this RT (set it to 1) and write the value to the Header Value Table.

Bit	Description
09-15	Reserved
08	1 = Board should expect a Header word 0 = Board should **not** expect a Header word
00-07	Reserved

1760 Header Exist Table

Address	Hex Value	Associated Subaddress
3EC2 H	0100	1
3ED6 H	0100	11
3EDC H	0100	14

Transmit Subaddresses: BC/Concurrent-RT Mode

5.8.23 Board Options Register

Address: 3E84 (H) READ ONLY

The Board Options register is a 16-bit register in which the low 8 bits are reserved. This register identifies the type of on-board firmware.

Bit	Description
10–15	Reserved
09	1 = 1760
08	1 = 1553
00–07	Reserved

Board Options Register

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5.8.24 Firmware Revision Register

Address: 3E80 (H)

The Firmware Revision register indicates the revision level of the on-board firmware. The value 0001 0010 would be read as revision level: 1.2.

5.8.25 Asynchronous Start Flag Register

Address: 3424 (H) WRITE

To indicate that it is now time to send a selected frame asynchronously, write a 1 to the Asynchronous Start Flag register. The board will automatically reset this value to 0 when it sends the frame.

5.8.26 Asynchronous Frame Pointer Register

Address: 3422 (H) WRITE

To send asynchronously to this register, write the address at the beginning of the selected frame.

5.8.27 Asynchronous Message Count Register

Address: 3420 (H) WRITE

Write the number of messages contained in the Asynchronous Frame. The maximum number of messages allowed in a frame is determined by the amount of available space in the message stack area of the board and the size of the individual messages.

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6 Bus Monitor Operation

Chapter 6 describes EXC-1553PC/EP operation in Bus Monitor mode. The following topics are covered:

Sequential Fixed-Block Memory Map	page 6-3
Sequential Link-List Memory Map	page 6-4
Sequential Mode Message Block Area	page 6-5
Look-Up Table Mode Memory Map	page 6-7
Look-Up Table Mode	page 6-10
Look-Up Table Mode Message Block Area	page 6-10
Message Status Word	page 6-11
Time Tag Value	page 6-12
1760 Header Word **[1760 option only]**	page 6-12
Trigger Operation	page 6-13
Program Examples: Bus Monitor Mode	page 6-14
Control Register Definitions	page 6-16

The Bus Monitor can operate in one of two modes:

Sequential Mode

1553 Message blocks are stored in sequential locations in memory. Sequential mode supports two types of operations:

Fixed-Block operation: 1553 messages are stored at fixed sequential blocks in the memory. Sequential Fixed-Block mode supports Trigger capability.

Link-List operation: 1553 messages are packed one after another in the memory, separated by a header.

Look-Up Table Mode

Each 1553 message is stored in a unique Message block. In Look-Up Table mode, the board addresses the user-programmable look-up table when it receives a 1553 Command word. The Command word's RT address, T/R bit, and Subaddress fields make up the 11-bit pointer to a Look-Up table with 2048 (2K x 8) locations.

Use the Board Configuration register (Board Configuration Register, page 6-17) to program the desired mode of operation.

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NOTE The operation of the non-concurrent bus monitor and the concurrent-monitor found on the board are identical and both provide a user-selectable 16- or 32-bit time tag (selected via a unique DIP switch on the board, see DIP Switches, page 9-3). The memory for each monitor, however, resides in its own memory bank (see Using the Concurrent Monitor Option, page 7-1).

To determine that the board is installed and ready to operate:

Perform the following procedure after a power-up or a software reset.

1. Check the Board ID register (test for value = 45 H).
2. Check the Board Status register (test for Board Ready bit = 1).

The board is installed and ready when both registers contain the correct values (as written above). For software reset operations, set these values to 0 immediately prior to writing to the (software) Board Reset register.

NOTE Throughout this manual, writing a 1 to the Start register is referred to as “issuing a Start command.”

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6.1 Sequential Fixed-Block Memory Map

Time Tag Options Register	700C H
Time Tag Counter	7008-700B H
Time Tag Reset Register	7007 H
Reserved	7002-7006 H
Interrupt Reset Register	7001 H
Software Reset Register	7000 H
Reserved	4000-6FFF H
Board Configuration Register	3FFF H
Board ID Register	3FFE H
Board Status Register	3FFD H
Start Register	3FFC H
Interrupt Condition Register	3FFB H
Message Status Register	3FFA H
Reserved	3FF8-3FF9 H
Time Tag Resolution Register	3FF7 H
Message Counter	3FF5 H
Counter Trigger	3FF4 H
Trigger Word #1 Register	3FF2 H
Trigger Mask #1 Register	3FF0 H
Trigger Word #2 Register	3FEE H
Trigger Mask #2 Register	3FEC H

Trigger Control Register	3FEB H
Mode Code Control Register	3FEA H
Broadcast Control Register	3FE8 H
Reserved	3F80-3FE7 H
1760 Header Value Table *	3F00-3F7F H
1760 Header Exist Table *	3EC0-3EFF H
Reserved	3E90-3EBF H
Monitor Response Time Reg.	3E8E H
Reserved	3E86-3F8D H
Board Options Register	3E84 H
Reserved	3E81-3E83 H
Firmware Revision Register	3E80 H
Message Block Area (200 Blocks)	0000-3EF7 H

Figure 6-1 Bus Monitor: Sequential Fixed-Block Memory Map

* 1760 option only

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6.2 Sequential Link-List Memory Map

Time Tag Options Register	700C H		
Time Tag Counter	7008-700B H		
Time Tag Reset Register	7007 H		
Reserved	7002-7006 H		
Interrupt Reset Register	7001 H		
Software Reset Register	7000 H		
Reserved	4000-6FFF H		
Board Configuration Register	3FFF H	Broadcast Control Register	3FE8 H
Board ID Register	3FFE H	Reserved	3F80-3FE7 H
Board Status Register	3FFD H	1760 Header Value Table *	3F00-3F7F H
Start Register	3FFC H	1760 Header Exist Table *	3EC0-3EFF H
Interrupt Condition Register	3FFB H	Reserved	3E90-3EBF H
Message Status Register	3FFA H	Monitor Response Time Reg.	3E8E H
Reserved	3FF8-3FF9 H	Reserved	3E86-3F8D H
Time Tag Resolution Register	3FF7 H	Board Options Register	3E84 H
End Buffer Pointer (16 bits)	3FF4 H	Reserved	3E81-3E83 H
Next Message Pointer (16 bits)	3FF2 H	Firmware Revision Register	3E80 H
Reserved	3FEB-3FF1 H	Message Block Spill Area	3400-3E7F H
Mode Code Control Register	3FEA H	Message Block Area	0000-33FF H

Figure 6-2 Bus Monitor: Sequential Link-List Memory Map

* 1760 option only

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6.3 Sequential Mode Message Block Area

The Sequential Mode Message Block area is partitioned either into blocks of fixed length or into a link list of blocks of varying lengths. The type of partitioning is determined by the Board Configuration register (see Board Configuration Register, page 6-17).

For a description of the 16- and 32- bit Time Tag function, see Time Tag Value, page 6-12, and Board Configuration DIP Switch (SW1), page 9-3.

6.3.1 Message Block Fixed-Block Operation

In Fixed-Block operation, the Message Block area is divided into 200 blocks of 80 bytes each. The first block starts at address 0000 (H), the second at 0050 (H), the third at 00A0 (H), etc. The Trigger option can be used only in Sequential mode with Fixed-Block operation (see Trigger Operation, page 6-13).

BUS MONITOR MESSAGE BLOCK-FIXED-BLOCK OPERATION

16-Bit Time Tag Mode		**32-Bit Time Tag Mode**	
Information is stored in the memory in the following sequence:	**Byte Offset**	**Information is stored in the memory in the following sequence:**	**Byte Offset**
•		•	
•		•	
•		1553 Data Words	**8**
1553 Data Words		1553 Command Word	**6**
1553 Command Word	**4**	Time Tag Word # 2(MSW)	**4**
Time Tag Word	**2**	Time Tag Word # 1 (LSW)	**2**
Message Status Word	**0**	Message Status Word	**0**

6.3.2 Message Block Link-List Operation

In Link-List operation, the Message Block area is divided into a linked list of message blocks. The length of each message block varies according to message size. The first two locations in each message comprise the message header. This header contains the address of the next Message Block header. The header of the last 1553 block received contains XXFF (End of File), indicating that there are no more messages stored.

After a message is processed and stored in memory, the header of the preceding message block is updated from XXFF to the address (of the header in the block) of the newly stored message. The Link-List method can store more data than Fixed-Block operation.

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Take special care with the last message in the Message Block area. The buffer never wraps around in the middle of a message and a message may start at any address up to 3DFE (H). Therefore, the final message in the buffer may extend past the end of the standard Message Block area into the Message Block Spill area. The End Buffer pointer (see End Buffer Pointer, page 6-22) exists for this special case. The End Buffer pointer points to the address after the last location of the message, indicating the length of the message. The next message will start at the first location of the Message Block area 0000 (H).

The following figures illustrate the contents of the Message block. For a description of the 16 and 32-bit Time Tag function, see Time Tag Value, page 6-12 and Board Configuration DIP Switch (SW1), page 9-3.

BUS MONITOR MESSAGE BLOCK: LINK-LIST OPERATION

16-Bit Time Tag Mode		**32-Bit Time Tag Mode**	
Information is stored in the memory in the following sequence:		**Information is stored in the memory in the following sequence:**	**Byte Offset**
End Of File: XXFF		End Of File: XXFF	**n+1**
1553 Data Word		1553 Data Word	**n**
•		•	
•		•	•
		1553 Data Word	•
1553 Data Word		1553 Command Word	•
1553 Command Word		Time Tag Word #2 (MSW)	•
Time Tag Word	**6**	Time Tag Word #1 (LSW)	**6**
Message Status Word	**4**	Message Status Word.	**4**
Message Header Address of Next Block	**2**	Message Header Address of Next Block	**2**

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6.4 Look-Up Table Mode Memory Map

Time Tag Options Register	700C H
Time Tag Counter	7008-700B H
Time Tag Reset Register	7007 H
Reserved	7002-7006 H
Interrupt Reset Register	7001 H
Software Reset Register	7000 H
Data Block Look-Up Table (2K x 8)	4000-47FF H
Board Configuration Register	3FFF H
Board ID Register	3FFE H
Board Status Register	3FFD H
Start Register	3FFC H
Interrupt Condition Register	3FFB H
Message Status Register	3FFA H
Reserved	3FF8-3FF9 H
Time Tag Resolution Register	3FF7 H
Reserved	3FF3-3FF5 H
Last Block Register	3FF2 H
Reserved	3FEB-3FF1 H
Mode Code Control Register	3FEA H

Broadcast Control Register	3FE8 H
Reserved	3F80-3FE7 H
1760 Header Value Table *	3F00 -3F7F H
1760 Header Exist Table *	3EC0 -3EFF H
Reserved	3E90 -3EBF H
Monitor Response Time Reg.	3E8E H
Reserved	3E86-3F8D H
Board Options Register	3E84 H
Reserved	3E81-3FE3 H
Firmware Revision Register	3E80 H
Reserved	2800-3E7F H
Message Block Area (128 Blocks)	0000-27FF H

Figure 6-3 Bus Monitor: Look-Up Table Mode Memory Map

* 1760 option only

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6.5 Look-Up Table Mode 6-8

In Look-Up Table mode, the board can store 128 unique messages by using a 2K × 8 look-up table in on-board memory. Each (table) byte is divided into a 7-bit block number and an Interrupt Select bit, as described below. Data Block numbers (0-127 decimal) each consisting of 80 bytes are loaded into the table. The first block starts at address 0, the second at 50 (H), etc. Set the Interrupt Select bit to specify which messages will set the interrupt flag. The Interrupt Condition register must also be programmed.

Bit	Description
07	1 = Interrupt Select Bit is Enabled
00-06	Block Numbers (0-127)

Look-Up Table Byte Structure

When a 1553 message is received, the Command word's RT address, T/R Bit, and Subaddress fields are used as an 11-bit index to the look-up table. This index is used to extract the Data block number from the look-up table.

For RT-to-RT messages all the information is stored in both the receiving and the transmitting RTs data blocks.

	(11 most significant bits of the 1553 command word)					
Base Address	(5 bits) **RT address**	(1 bit) **T/R**	(5 bits) **Sub-address**	**Look-up table (2K x 8)**	**Data block**	**Hex address of data block**
4000+	11111	1	11111	Block #	Data Block 127	27B0
	•	•	•	•	•	
	•	•	•	•	•	
	•	•	•	•	•	
4000+	00000	0	00011	Block #	Data Block 3	00F0
4000+	00000	0	00010	Block #	Data Block 2	00A0
4000+	00000	0	00001	Block #	Data Block 1	0050
4000+	00000	0	00000	Block #	Data Block 0	0000

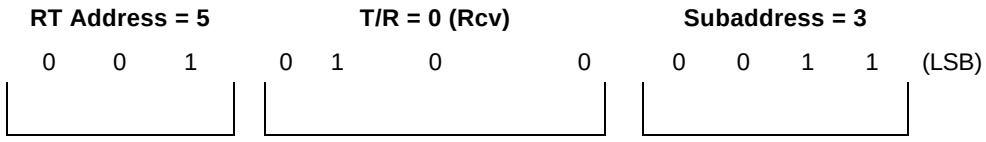
Figure 6-4 Look-Up Table

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To create the address to the table:

1. Isolate the eleven (most significant) bits of the 1553 command word (RT Address, T/R, and Subaddress field), and determine their hex value.

Example To allocate a data block for a 1553 receive message to RT#5, Subaddress #3.



Hex representation = 143

2. Add the hex value of this part of the command word to the base address of the look-up table (4000 H).

```
  4000  (H)
+ 143   (H)
-------------
  4143  (H)
```

3. Write the Data Block number to this location.

Example `POKE &H4143,xx` writes an 8-bit Block Number value to the Look-up table address &H4143. Each data block, beginning at address 0000 is 80 bytes long (for up to 32 1553 data words). The address of a block is obtained by multiplying its block number by 50 (H).

To calculate the block addresses:

- Block 0 is located at location 0000 (H).
- Block 1 is located at location 0050 (H).
- The location of the block is obtained by multiplying the block number by 50 (H).

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6.6 Look-Up Table Mode Message Block Area

BUS MONITOR MESSAGE BLOCK: LOOK-UP TABLE MODE

16-Bit Time Tag Mode		32-Bit Time Tag Mode	
Information is stored in the memory in the following sequence:	**Byte Offset**	**Information is stored in the memory in the following sequence:**	**Byte Offset**
See Appendix B MIL-STD-1553B Word Formats for message Formats		See Appendix B MIL-STD-1553B Word Formats for message Formats	
	6	1553 Command Word	**6**
1553 Command Word	**4**	Time Tag Word #2	**4**
Time Tag Word	**2**	Time Tag Word #1	**2**
Message Status Word - Low	**0**	Message Status Word	**0**

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6.7 Message Status Word

The Message Status word is identical for all Bus Monitor modes. The Message Status word indicates the status of the message transfer. This word is created by the board. Do not confuse it with the 1553 Status word (see 1553 RT Status Words page 4-7). The contents of the Message Status word are described below. A logic 1 indicates the occurrence of a status flag.

Bit	Bit Name	Description
15	**End Of Message**	Message transfer completed.
14	**Trigger Found**	Trigger message was received and stored. This status is valid for Sequential Fixed-Block mode with the following modes: **Store After mode**: the Trigger Found bit will be set only in the *first* Trigger message. **Store Only mode**: the Trigger Found bit will be set in *every* Trigger message. (see Trigger Operation page 6-13).
13	**RT-RT**	RT-to-RT message was received.
12	**Message Error Bit Set**	Message Error bit (bit 10) in the RT Status word was set.
11	**RT Status Bit Set**	A bit other than the Message Error bit in the RT Status word was set. The Error Bit is *not* set in conjunction with this bit.
10	**Invalid Message**	1553 message-level error occurred (Word Count, Incorrect Sync, etc.). Examine the other bits in this table to determine which error occurred.
09	**Checksum Error**	The computed checksum (on an incoming message) does not match when checked against the last data word received. **[1760 option only]** See MIL-STD-1760B Considerations, page 1-4
08	**Bus A/B**	Bus on which the message was transferred: 0 = Bus B 1 = Bus A
07	**Invalid Word Received**	At least one invalid 1553 word received (i.e. bit count, Manchester code, parity).
05-06	**Word Count / Header Error**	See nested table below
04	**Incorrect RT Address**	Received 1553 Status word did not contain the correct RT address.
03	**Incorrect Sync Received**	Sync of either the command or the data word(s) is incorrect.
02	**Non-Contiguous Data**	Invalid gap between received 1553 words.
01	**Response Time Error**	Response Time error occurred in the message.
00	**Error**	Error occurred. (The error type is defined in one of the other message status bit locations.)

Bit 06	Bit 05	Description
0	0	Reserved
0	1	Word Count Low
1	0	Word Count High
1	1	1760 Header Error - Header word received does not match the value set in the Header Value Table. **[1760 option only]**

Message Status Word

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6.8 Time Tag Value

In all Bus Monitor modes, each incoming message has a Time Tag value. The Time Tag value is a 16- or 32-bit word used to determine the time elapsed since the Start command was issued or the time between 1553 messages. To select 16- or 32-bit Time Tag mode, use the dedicated DIP Switch (see DIP Switches, page 9-3). The Time Tag implementation uses a 32-bit, free-running counter whose resolution is fixed at 4 µsec. per bit in 16-bit mode and is programmable in 32-bit mode (see Time Tag Resolution Register, page 6-21). To reset the Time Tag counter, to 0, at any time, write to the Time Tag Reset register (see Time Tag Reset Register, page 6-16).

The Time Tag counter's value is written to the dual-port RAM during the reception of the first command of each message. In 16-bit mode, only the counter's 16 lower bits are written to the dual-port RAM.

NOTE 1. The counter's value can be read at any time at the Time Tag Counter addresses.

2. The counter can also be clocked and/or reset from external source (see Connectors, page 9-6).

6.9 1760 Header Word

1760 Option only

With the 1760 option the first data word of a message may be a header word, which is used for message identification. The header word is associated with a specific RT subaddress.

To indicate that a specific subaddress will require a header word, you must set the corresponding entry in the 1760 Header Exist table to 1. Then set the corresponding entry in the 1760 Header Value table to the value you expect to receive in the first data word of the message. The 1760 option provides predefined values, and these are preset on the EXC-1553PC/EP board.

For descriptions of the 1760 Header Value Table and 1760 Header Exist Table, see page 6-28.

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6.10 Trigger Operation

Only Sequential Fixed-Block mode supports triggers

A trigger is a filter set by the user, to tell the board when and how to store 1553 messages. The board can be programmed to store messages in the following ways:

Store All stores all 1553 messages, without regard to triggers; no triggers are active

Store Only stores only messages that meet the trigger condition

Store After stores only the trigger message and messages that come after the trigger message

Up to two triggers can be defined. Each trigger is defined using two registers:

- Trigger Word register
- Trigger Mask register

Use the Trigger Word Registers to define a particular 1553 Command word or a Message Status word as a trigger; for example, to use the Message Status word as the trigger source to store all messages on bus A, only messages with errors, or messages with errors received over bus B, etc. (see Trigger Word Registers, page 6-23).

The Trigger Mask Registers define which bits of the trigger word, defined in the Trigger Word Registers, are relevant and which can be ignored ("don't care"). The Trigger Mask registers must be defined when using the trigger function (see Trigger Mask Registers, page 6-24).

Set the Trigger Control register to specify the following trigger conditions (see Trigger Control Register, page 6-25):

- Trigger source (1553 Command word or Message Status word)
- Type of storage (Store All, Store Only, or Store After)
- Active trigger word (Trigger Word #1 and/or #2)

Set these registers, before issuing a Start command to the board. To modify these registers, set the Initialize bit in the Start register to 10 (H), modify the Trigger Word, Trigger Mask and Trigger Control registers, then issue a Start command 81 (H).

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6.11 Program Examples: Bus Monitor Mode

Bus Monitor Sequential Fixed-Block Mode

BASIC Instruction	Remarks
`10 POKE &H3FFF,08`	Set the Board Configuration register for Bus Monitor Sequential Fixed-Block mode
`20 POKE &H3FF0,xx`	Set trigger mask #1-low to xx
`30 POKE &H3FF1,xx`	Set trigger mask #1-high to xx
`40 POKE &H3FF2,xx`	Set trigger word #1-low to xx
`50 POKE &H3FF3,xx`	Set trigger word #1-high to xx
`60 POKE &H3FEB,xx`	Set the Trigger Control register (see Trigger Control Register, page 6-25)
`70 POKE &H3FEA,00`	Set the Mode Code Control Register to 1s and 0s (see Mode Code Control Register, page 6-26)
`80 POKE &H3FE8,00`	Set the Broadcast Control register to RT31 = regular (see Broadcast Control Register, page 6-26)
`90 POKE &H3FFC,01`	Start command

Bus Monitor Sequential Link-List Mode

BASIC Instruction	Remarks
`10 POKE &H3FFF,&H10`	Set the Board Configuration register to Bus Monitor Link-List mode (see Board Configuration Register, page 6-17)
`20 POKE &H3FEA,00`	Set the Mode Code Control register to 1s and 0s (see Mode Code Control Register, page 6-26)
`30 POKE &H3FE8,01`	Set the Broadcast Control Register to RT31 = Broadcast (see Broadcast Control Register, page 6-26)
`40 POKE &H3FFC,01`	Start command

NOTE In Sequential Fixed-Block and Sequential Link-list Mode Messages are read from memory starting from address 0000.

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Bus Monitor Look-Up Table Mode

BASIC Instruction	Remarks
`10 POKE &H3FFF,&H20`	Set the Board Configuration register to Bus Monitor Look-Up Table mode
`20 POKE &H3FEA,00`	Set the Mode Code Control register to 1s and 0s (see Mode Code Control Register, page 6-26)
`30 POKE &H3FE8,00`	Set the Broadcast Control register to RT31 = Regular.
`40 POKE &H4143,00`	Set the Look-Up Table so that Command words with Remote Terminal 5, Receive mode, and Subaddress 3 point to Data Block #0 (see Look-Up Table Mode, page 6-10)
`50 POKE &H4144,01`	Set the Look-Up Table so that Command words with Remote Terminal 5, Receive mode, and Subaddress 4 point to Data Block #1 (see Look-Up Table Mode, page 6-10)
`60 POKE &H3FFC,01`	Start Command

NOTE Messages are read from memory according to the address pointer derived from Command word (see Look-Up Table Mode, page 6-10).

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6.12 Control Register Definitions

6.12.1 Time Tag Options Register — Address: 700C (H) WRITE

Set bit 00 of the Time Tag Options register to select the clock source for the current bank's Time Tag counter. The Time Tag Options register will be set to 0 after power-up or software reset.

Bit	Description
01-07	x
00	External Clock Source: 0 = Internal Time Tag Clock 1 = External Time Tag Clock (see EXTTCLKx pin in Connectors, page 9-6)

Time Tag Options Register

6.12.2 Time Tag Counter — Address: 7008–700B (H) READ

Read the four bytes of the Time Tag Counter to determine the current bank's free-running, 32-bit Time Tag counter value. The counter may be read at any time.

The counter must be read in the following sequence:

1. 7008 (H)
2. 7009 (H)
3. 700A (H)
4. 700B (H)

7008 (H) contains the LSB; 700B (H) contains the MSB. The Time Tag Resolution register sets the resolution of the counter (Time Tag Resolution Register, page 6-21).

The counter is reset upon power-up or software reset and stays reset until a Start command is issued. When a Start command is issued, the counter starts counting. To re-initialize to 0, write to the Time Tag Reset register. When it reaches the value FFFF FFFF (H), the counter wraps around to 0 and continues counting.

6.12.3 Time Tag Reset Register — Address: 7007 (H) WRITE

Write to the Time Tag Reset register to reset the current bank's Time Tag Counter (data field = don't care). Immediately after the reset, the counter will start to count from 0.

NOTE The counter can also be reset from an external source (see Connectors, page 9-6).

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6.12.4 Interrupt Reset Register

Address: 7001 (H)

To reset the Interrupt signal to the computer for the current bank, write to the Interrupt Reset register at the beginning of a user-written interrupt service routine (data field = don't care).

6.12.5 Software Reset Register

Address: 7000 (H)

Write to the Software Reset register to reset the current bank (data field = don't care). (See General Memory Map, page 2-1 for an explanation of the EXC-1553PC/EP "banks".) The bank will act as if power had been switched *off* then *on*. After the reset operation is completed, the board writes to the Board status, the Board ID, Firmware Revision and Variable Amplitude registers.

WARNING *Software Reset erases all memory locations in the dual-port RAM.*

6.12.6 Board Configuration Register

Address: 3FFF (H)

Before issuing a Start command to the board, you must set the operating mode of the board via the Board Configuration register. To modify the Board Configuration register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 6-19).

Hex Value	Operating Mode
01	BC Mode
02	RT Mode
04	BC/Concurrent-RT
08	**BM Sequential Block Mode**
10	**BM Sequential Link-List**
20	**BM Look-Up Table Mode**
40	Reserved
80	Reserved
ED	Internal Loop Test (see Appendix D, Internal Loopback Test; page 11-8)
FF	External Loop Test (see Appendix E, External Loopback Test, page 11-9)

Board Configuration Register Values: Monitor Mode

NOTE While in memory bank #1 (Concurrent Bus Monitor) the BC, RT and BC/Concurrent-RT functions are not available.

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6.12.7 Board ID Register

Address: 3FFE (H)

The Board ID register contains a fixed value that can be read by your initialization routine to detect the presence of the board. The one-byte value of this register is: 45 (Hex), ASCII value "E".

6.12.8 Board Status Register

Address: 3FFD (H)

The Board Status register indicates the status of the board. In addition, this register indicates which options have been selected. Do not modify this register. Status bits are active if set to 1.

Bit	Description
07	1 = Board Type is EXC-1553PC/EP
06	X (Don't Care)
05	BM Time Tag Mode: 1 = 16-Bit Mode 0 = 32-Bit Mode
04	1 = Board Halted 0 = Board Running
03	1 = Self-Test OK
02	1 = Timers OK
01	1 = RAM OK
00	1 = Board Ready

Board Status Register

NOTE Board operation stops after the Start bit is cleared in the Start Register. Following this, the board sets bit 04 (Board Halted). Certain registers may be modified only after the Board Halted bit has been set. After receiving a subsequent Start command (by writing to the Start register), the board resets the Board Halted bit. The condition of this bit after power-up or software reset is logic 1.

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6.12.9 Start Register

Address: 3FFC (H)

The Start register controls the Start/Halt operation of the board. For more information about Bit 04 (Board Halted/Running) in the Board Status Register, see the note in Board Status Register, page 6-19.

Write to the Start register with the appropriate bit set to execute one of the functions described below.

Bit	Bit Name	Description
06-07	**Reserved**	Set to 0
05	**Stop on Trigger/ Continue**	This bit is used in Sequential Fixed-Block mode only. 1 = Stop On Trigger. Stop storing 1553 messages when the Message Counter equals the Message Counter Trigger. 0 = Continue After Stop. Continue monitoring operations. You must first set this bit to 1 before Halting the board (setting bit 00 = 0).
04	**Initialize Board**	Set this bit to re-initialize the board, in order to change the board's mode of operation (via the Board Configuration Register, page 6-17). To switch Monitor modes, stop and start the board (Start/Halt bit (bit 00)) and set this bit (bit 04). After the specific function is completed, the board clears this bit and the Start/Halt bit to 0. Board Halted bit (04) of the Board Status register is set when both of the following are true: • A Halt command is issued (bit 00 of this register is set to 0) • An Initialize Board command is issued (this bit is set to 1) 1 = Initialize Board 0 = Stay in Monitor Mode
03	**Clear Memory**	This bit clears the 1553 message blocks and all readable control registers. 1 = Clear Memory 0 = Don't Clear Memory
01-02	**Reserved**	Set to 0
00	**Start/Halt**	1 = Start Operation 0 = Halt Operation

Start Register

NOTE The board tests Clear Memory (bit 03) and Initialize Board (bit 04) only when the Start/Halt bit (bit 00) = 0.

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6.12.10 Interrupt Condition Register

Address: 3FFB (H)

Set the Interrupt Condition register to enable interrupt triggers. When a condition that is enabled in this register occurs, an interrupt is generated. Check the Message Status register to determine which condition caused the interrupt.

Set the Interrupt Condition register before issuing a Start command to the board. To modify the Interrupt Condition register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 6-19).

NOTE For all interrupt conditions, the interrupt will be sent at the end of the message.

Bit	Description
03-07	0
02	1 = Counter Trigger Match (Valid Only in Sequential Fixed-Block Mode)
01	1 = Message Reception in Progress (Valid in All Modes)
00	1 = Trigger Word Received (Valid Only in Sequential Fixed-Block Mode)

Interrupt Condition Register

6.12.11 Message Status Register

Address: 3FFA (H)

The Message Status register indicates the status of the current message being processed. Each status bit is described in the table below. Logic 1 indicates that the condition is activated.

Bit	Description
03-07	0
02	1 = Counter Trigger Match
01	1= Message Reception In Progress
00	1 = Trigger Word Received / Busy Trigger word received is valid only in Sequential Fixed-Block mode. Busy is valid in Linked-List and Look-Up Table mode. The busy bit is set when the board is processing a message. It is set together with message reception in progress, but is reset approximately 5 µsec after the end of each message. For consecutive messages with short intermessage gap times, the busy bit may not be reset between messages.

Message Status Register

NOTE Status bits are *not* reset by the board. Reset them after you have read them.

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6.12.12 Time Tag Resolution Register

Address: 3FF6 (H)

The 8-bit value in the Time Tag Resolution register represents the resolution of the Time Tag Counter in units of 4 µsec.

To determine the Time Tag Counter's Resolution, use the following equation:

Time Tag Counter Resolution= (Time Tag Resolution register value + 1) x 4 µsec.

A value of 0 corresponds to a resolution of 4 microseconds; a value of 1 corresponds to a resolution of 8 microseconds, etc.

Set the Time Tag Resolution register before issuing a Start command to the board. To modify the Time Tag Resolution register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 6-19).

NOTE In Bus Monitor mode, the Time Tag Resolution register is applicable only in 32-bit time tag mode.

6.12.13 Message Counter Register

Address: 3FF5 (H)

Sequential Fixed-Block mode only

Read the Message Counter register to determine the current Message Block number (0–199). The value is incremented by the board as each message is received. The first counter increment (to 1), which indicates that the first message has been received and stored, occurs at the beginning of the *second* 1553 message transfer operation. To determine the arrival of the first 1553 message, check the Message Status word of the *first* Message block. The End of Message bit (bit 15) in the Message Status word will be set.

6.12.14 Counter Trigger Register

Address: 3FF4 (H)

Sequential Fixed-Block mode only

Read the Counter Trigger register to determine when a specific message block number has been updated by the board. Set the Counter Trigger register to a value that when equal to the Message counter will set a bit in the Message status register and set an interrupt (if programmed in the Interrupt Condition register).

Set the Counter Trigger register before issuing a Start command to the board. To modify the Counter Trigger register, issue a Stop command, modify the register, then issue a Start command (see Start Register, page 6-19).

The board can also be programmed to stop monitoring when the Counter Trigger value is equal to the Message Counter (see the Stop/Continue bit in the Start Register, page 6-19).

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6.12.15 End Buffer Pointer

Address: 3FF4 (H)

Link-List mode only

This 16-bit End Buffer pointer points to the address following the last word in the final message in the Message Block area. The End Buffer pointer is updated each time a final message is written into the buffer. Final messages that are longer than the remaining available space in the Message Block area do not wrap around to the start of the buffer. They are spilled into the Message Block Spill area, which is contiguous to the Message Block area.

The value of this register varies from 3400 (H) (end of Message Block area) to 347E (H) (end of Message Block Spill area). Until the first buffer wrap around occurs, this register contains 0000 (H).

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6.12.16 Trigger Word Registers (1 and 2)

Address: 3FF2, 3FEE (H)

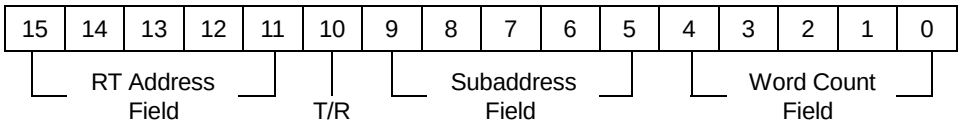
Sequential Fixed-Block mode only

Use the Trigger Word register to define a particular 1553 Command word or a Message Status word as a trigger. Load these locations (illustrated below) with the desired 1553 Command word or Message Status word that will be used as the trigger source. The Trigger Mask Registers must be defined when using the trigger function (see Trigger Mask Registers, page 6-24). To define which trigger is active (Trigger #1, Trigger #2, or both) use the Trigger Control Register (see Trigger Control Register, page 6-25).

Using the 1553 Command Word: Trigger Word Registers

Use a 1553 Command word as a trigger to filter messages based on information found in the Command word. For example, to filter messages from a particular RT, or with a particular word count, set the Trigger Word register with those parameters defined in the 1553 Command word.

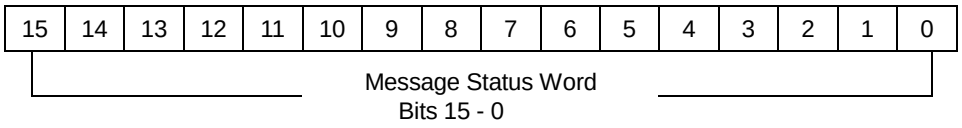
For all "don't care" bits, any value is valid.



Using the Message Status Word: Trigger Word Registers

Use a Message Status word as a trigger to filter messages based on information found in the Message Status word. Do not confuse the Message Status word with the 1553 Status word (see 1553 RT Status Words, page 4-7). For example, to filter messages transferred over bus A (vs. bus B), or error messages, set the Trigger Word register with those parameters defined in the Message Status word. For an explanation of the Message Status Word, see page 6-11.

For all "don't care" bits, any value is valid.



6.12.17 Next Message Pointer

Address: 3FF2 (H)

Link-list mode only

The Next Message pointer is a 16-bit pointer that indicates the address of the 1553 message about to be written. The Next Message pointer register is updated at the end of each message storage operation. It cycles from 0 (H) to 33FE (H).

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6.12.18 Last Block Register

Address: 3FF2 (H)

Look-up Table mode only

Read the Last Block register to determine the (Look-Up Table) block number of the current 1553 message. This register is used to identify the location of the current 1553 message. The Last Block register is updated at the end of each message reception.

6.12.19 Trigger Mask Registers (1 and 2)

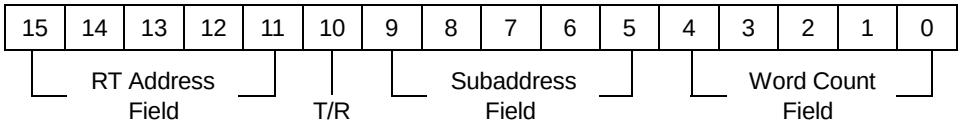
Address: 3FF0, 3FEC (H)

Sequential Fixed-block mode only

Set the Trigger Mask register to define which bits of the trigger word (defined in the Trigger Word register) are relevant and which can be ignored ("don't care"). The Trigger Mask registers must be defined when using the trigger function. All bits in this register should be set to 1, except for those bits you want to be "don't care" in the incoming Command word or Message Status word.

Using the 1553 Command Word: Trigger Mask Registers

Write a 1553 Command word in the Trigger Word register. Write 1s to the Trigger Mask register to the bits that match the corresponding bits in the Trigger Word register, and 0s to the "don't care" bits.

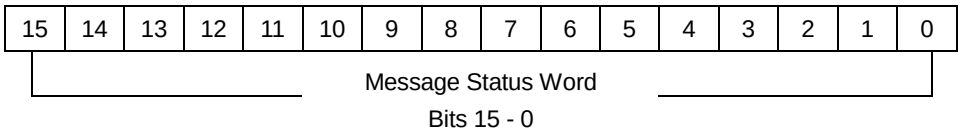


1 = Trigger on corresponding bit value in Trigger Word Register
0 = Corresponding bit value in Trigger Word Register is "Don't Care"

Using the Message Status Word: Trigger Mask Registers

Write a 1553 Command word in the Trigger Word register. Write 1s to the Trigger Mask register to the bits that match the corresponding bits in the Trigger Word register, and 0s to the "don't care" bits.

For an explanation of the Message Status Word, see page 6-11.



1 = Trigger on corresponding bit value in Trigger Word Register
0 = Corresponding bit value in Trigger Word Register is "Don't Care"

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6.12.20 Trigger Control Register

Address: 3FEB (H)

Sequential Fix-block mode only

Set the Trigger Control register to specify the following trigger conditions:

- Trigger source (1553 Command word or Message Status word)
- Type of storage (Store All, Store Only, or Store After)
- Active trigger word (Trigger Word #1 and/or #2)

NOTE Logic 1 enables the function.

Bit	Description
07	Trigger Source: 0 = 1553 Command Word 1 = Message Status Word
05-06	Reserved
04	1 = Store After
03	1 = Store Only
02	1 = Store All
01	1 = Enable Trigger Word #2
00	1 = Enable Trigger Word #1

Trigger Control Register

Defining a Trigger

Conditions:

- Define the Command word 0825 (H) as Trigger word #1 (Receive Command for RT#1, Subaddress #1, and 5 words).
- Ignore the Word Count field.
- Use Trigger word #1 (Disable Trigger word #2).

Procedure:

1. Set Trigger Word #1 register = 0825 (H)
2. Set Trigger Mask #1 register = FFE0 (H)
3. Set Trigger Control register = 09 (H)

NOTE To use trigger(s), at least one of the bits Store All, Store Only, or Store After, must be set.

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6.12.21 Mode Code Control Register

Address: 3FEA (H)

Set the Mode Code Control register to determine which 1553 Subaddress value indicates the reception of a 1553 Mode command.

Set the Mode Code Control register before issuing a Start command to the board. To modify the Mode Code Control register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 6-19).

Bit	Description		
02–07	0		
00–01	**Bit 01**	**Bit 00**	**Subaddresses Recognized as Mode Code**
	0	0	31 and 0
	0	1	0
	1	0	31
	1	1	0 and 31

Mode Code Control Register

6.12.22 Broadcast Control Register

Address: 3FE8 (H)

Write to the Broadcast Control register to select whether RT address 11111 (RT 31) is interpreted as a valid RT number or as a Broadcast address.

Bit	Description
01-07	0
00	1 = Broadcast option is active. RT #31 is Broadcast Address. 0 = Broadcast option is inactive. RT #31 is Regular RT.

Broadcast Control Register

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6.12.23 1760 Header Value Table

Address: 3F00-3F7F(H)

1760 option only

Write to the 1760 Header Value Table to set the value expected to be received in the first data word of the message. The 1760 option provides predefined values. These are preset on the EXC-1553PC/EP board (see below). The preset values can be reset by the user.

The first 32 words [3F00-3F3F (H)] are reserved for Header values associated with BC-to-RT messages. The second 32 words [3F40-3F7F (H)] are reserved for Header values associated with RT-to-BC and RT-to-RT messages.

Address	Hex Value	Associated Subaddress
3F16 H	0400	11
3F1C H	0422	14
3F42 H	0421	1
3F56 H	0420	11
3F5C H	0423	14

Transmit and Receive Subaddresses: BM Mode

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6.12.24 1760 Header Exist Table

Address: 3EC0-3EFF (H)

1760 option only

The 1760 Header Exist Table contains 32 entries corresponding to 32 RT subaddresses. Each entry may be set to indicate whether, or not, the board should expect a header word for messages directed to that subaddress. In Bus Monitor Mode, there is a separate bit to select Header Words for transmit and receive messages.

For those Header Value Table entries for which MIL-STD-1760B provides predefined values, the corresponding Header Exist Table entries are preset on the EXC-1553PC/EP board (see below). To set other values, enable the Header Exist Table entry for this RT (set it to 1) and write the value to the Header Value Table.

Bit	Description
09-15	Reserved
08	1 = Board should expect a Header word in a transmit message (RT-to-BC or RT-to-RT)
	0 = Board should **not** expect a Header word in a transmit message
01-07	Reserved
00	1 = Board should expect a Header word in a receive message (BC-to-RT)
	0 = Board should **not** expect a Header word in a receive message

1760 Header Exist Table

Address	Hex Value	Associate Subaddress
3EC2 H	0100	1
3ED6 H	0101	11
3EDC H	0101	14

Transmit and Receive Subaddresses: BM Mode

6.12.25 Monitor Response Time Register

Address: 3E8E (H)

The Monitor Response Time Register sets the maximum wait time until an RT's Status Response is considered valid by the Monitor.

The Monitor Response Time Register is measured in microseconds. The default value of the register is 14, if not set otherwise by the user.

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6.12.26 Board Options Register

Address: 3E84 (H) READ ONLY

The Board Options register is a 16-bit register in which the low 8 bits are reserved. This register identifies the type of on-board firmware.

Bit	Description
10–15	Reserved
09	1 = 1760
08	1 = 1553
00–07	Reserved

Board Options Register

6.12.27 Firmware Revision Register

Address: 3E80 (H)

The Firmware Revision register indicates the revision level of the on-board firmware. The value 0001 0010 would be read as revision level: 1.2.

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7 Concurrent Monitor Operation

This chapter describes Concurrent Monitor operation, an option available only on the EXC-1553PC/EPM and EXC-1553PC/EPMI boards (see Ordering Information, page 10-1).

7.1 Using the Concurrent Monitor Option

The operation of the concurrent monitor is identical to the operation of the non-concurrent monitor (see Bus Monitor Operation, page 6-1). Both monitors can be used simultaneously, as they operate independently of one another.

On the same 1553 bus, the EPM option allows the user to use the board's BC, RT, or non-concurrent monitor functions in bank 0, concurrently with its bank 1 monitor function. The EPMI option allows the bank 1 monitor to monitor a second, independent dual-redundant 1553 bus.

The EXC-1553PC/EP board utilizes a 32K block of memory from the PC/AT memory map (half of one segment). The memory is divided into two banks of 32K. Write a 1 or a 0 to the Bank Select register to specify which bank you want to access. The BC, RT, and non-concurrent monitor functions reside in bank 0; the concurrent monitor functions reside in bank 1 (see General Memory Map, page 2-1).

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8 Switching Modes of Operation

Many test applications utilizing the EXC-1553PC/EP simulate only one operation mode, i.e., Bus Controller. For these applications, the information in this chapter is not relevant.

If your application requires simulation of more than one mode, the user can switch from one mode of operation to another, i.e., between the Bus Controller and Remote Terminal modes.

To switch between modes of operation:

1. Halt the operation of the board (via the Start register).
2. Modify the Configuration register to the desired mode.
3. Set up the memory as required.
4. Set the Start bit in the Start register.

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9 Mechanical and Electrical Specifications

Chapter 9 describes the mechanical and electrical specifications of the EXC-1553PC/EP board. The following topics are discussed:

Board Layout	page 9-1
LED Indicators	page 9-2
DIP Switches	page 9-3
Connectors	page 9-6
Mechanical Outline	page 9-9
Power Requirements	page 9-10

NOTE Throughout this manual, writing a 1 to the Start register is referred to as "issuing a Start command."

9.1 Board Layout

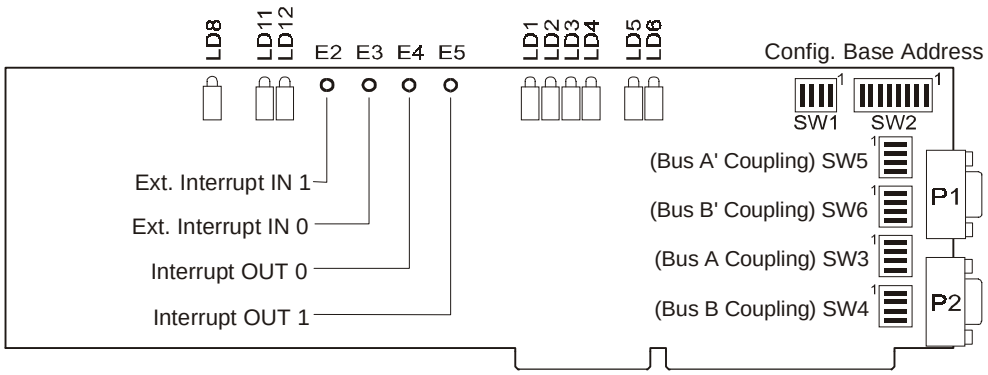


Figure 9-1 EXC-1553PC/EP Board Layout

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9.2 LED Indicators

The EXC-1553PC/EP board contains nine LEDs. The LEDs indicate the bank's operational mode and bus activity. Each LED's function is described below.

9.2.1 BC, RT, Non-Concurrent Monitor, and Concurrent Monitor

LED	Indication
LD1	Board Ready (indicates that both banks are ready)

9.2.2 BC, RT, and Non-Concurrent Monitor

LED	Indication
LD2	Monitor mode is active
LD3	RT mode is active
LD4	BC or BC/RT mode is active
LD5	1553 Bus B active
LD6	1553 Bus A active

9.2.1 Concurrent Bus Monitor

LED	Indication
LD8	Monitor is Active
LD11	1553 Bus B active (BUS B' if Independent Monitor is used)
LD12	1553 Bus A active (BUS A' if Independent Monitor is used)

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9.3 DIP Switches

There are six DIP Switches on the EXC-1553PC/EP board which control the following functions:

- Board Configuration (SW1)
- Address Decoding of board within the PC/AT system (SW2)
- 1553 Coupling selectors (SW3, SW4, SW5, SW6)

The DIP switches are described below.

9.3.1 Board Configuration DIP Switch (SW1)

The Board Configuration DIP switch SW1 selects the various system modes of the EXC-1553PC/EP board.

Switch Contact	Description
1	**Concurrent BM Time Tag Mode (Bank 1):** ON (Closed) = 32-bit time tag mode OFF (Open) = 16-bit time tag mode See Time Tag Value, page 6-12
2	**Broadcast Mode (RT Mode Only):** ON (Closed) = Broadcast option is **not** in use. This switch indicates to the board that the Remote Terminal Address 11111 is a valid RT address. The board will respond to it with a 1553 Status word. OFF (Open) = Broadcast option is **in use**. This switch indicates to the board that Remote Terminal Address 11111 is a 1553 Broadcast command. **No** RT Status word will be transmitted.
3	**Non-Concurrent BM Time Tag Mode (Bank 0):** ON (Closed) = 32-bit time tag mode OFF (Open) = 16-bit time tag mode See Time Tag Value, page 6-12
4	**Power-Up Delay/LED Test Mode:** ON (Closed) = Delay is **not active**. After completing the internal self-test, the board will wait for a user-issued Start command (after approximately 2 seconds). OFF (Open) = Delay is **active**. After completing the internal self-test, the board will test the LEDs (LD1 - LD4) and then insert a time delay of approximately 5 seconds before responding to PC instructions. This option exists to assure that the board's processor ignores any PC accesses (writes) until the PC self-test is complete. Since the board is memory-mapped, the PC BIOS's power-up self-test might inadvertently write in the board's memory, starting the 1553 operation.

Board Configuration DIP Switch (SW1)

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9.3.2 Address Decoding DIP Switch (SW2)

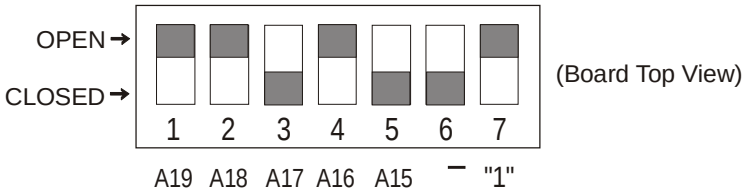
The Address Decoding DIP switch SW2 is used to set the board's base address. The EXC-1553PC/EP board occupies 32K (one-half segment) of memory within the PC's lower one megabyte of memory address space. Switch contacts 1-5 of SW2, corresponding to address lines A19-A15, are used to select the base address of this half segment. Switch contact 6 is reserved, and switch contact 7 selects the computer type.

Switch Contact	Description
1	A19
2	A18
3	A17
4	A16
5	A15
6	Don't Care
7	ON or Closed = PC, XT, 286-AT OFF or Open = 386, 486, ISA, EISA, XT + Intel Inboard

Address Decoding DIP Switch (SW2)

Set DIP switch SW2 to the desired address by setting the switch contacts *open* or *off* to represent logic 1; and *closed* or *on* to represent logic 0 (see example below).

Example To address the board in Segment D, address D0000 (H), set the following switches:



NOTE *A15: *on* or *off*. The EXC-1553PC/EP allows up to two boards to be addressed in the same memory segment. One board is addressed at (relative) address 0000 (by setting A15 switch to *on* or *closed*). The other board is addressed at (relative) location 8000 (H) (by setting A15 switch to *off* or *open*). In this case, for example, the Message Data Block area of the board is addressed from PC offset 8000 (H).

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9.3.3 1553 Coupling Mode Select DIP Switches (SW3, SW4, SW5, SW6)

There are four DIP switches on the EXC-1553PC/EP board which function as 1553 coupling mode selectors. These DIP switches select the coupling mode of the board to the 1553 bus. The board can be either direct- or transformer-coupled.

Each DIP switch corresponds to a bus as follows:

DIP Switch	Channel, Bus
SW3	BUS A of the BC, RT and Non-Independent Monitor
SW4	BUS B of the BC, RT and Non-Independent Monitor
SW5	BUS A' of the Independent Concurrent Monitor (EPMI only)
SW6	BUS B' of the Independent Concurrent Monitor (EPMI only)

Each DIP switch contains four switch contacts, which are used to set the coupling mode, as described below:

Switch Contact	Direct-Coupled Setting	Transformer-Coupled Setting
1	ON (Closed)	OFF (Open)
2	ON (Closed)	OFF (Open)
3	OFF (Open)	ON (Closed)
4	OFF (Open)	ON (Closed)

9.3.4 Factory Default DIP Switch Settings

Following are the factory preset default settings:

SW1 All Closed

SW2 Segment D0, 386/486/ Type Computer

SW3-6 Transformer-Coupled

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9.4 Connectors

The board contains two DB-9 connectors, labeled P1 and P2. Each board is shipped with two adapter cables that convert the DB-9 to a standard 1553 (miniature) female twinax type, which will mate with a Trompeter PL75-type male connector (not supplied). The EPMI option has double type adapter cables. The adapter cables are wired and ready to connect to the 1553 bus.

Excalibur Systems, Inc. carries a complete line of data bus products. Contact us for detailed ordering information.

9.4.1 Connectors P1 and P2 Pinout

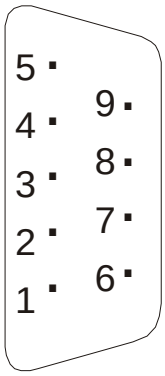


Figure 9-2 Connectors P1 and P2 Layout (Front View)

9.4.2 Connectors P1 and P2 Pin Assignments

Connector P1		Connector P2	
1	BUS_A'_HI	**1**	BUS_B'_HI
2	BUS_A'_LO	**2**	BUS_B'_LO
3	GND	**3**	GND
4	BUS_A_LO	**4**	BUS_B_LO
5	BUS_A_HI	**5**	BUS_B_HI
6	SHIELD	**6**	SHIELD
7	EXTTRST0$	**7**	EXTTRST1$
8	EXTTCLK0	**8**	EXTTCLK1
9	EXSTART$	**9**	Not connected

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9.4.3 Connectors P1 and P2 Signals Description

Signal	Description
BUS_A_HI, BUS_A_LO	Channel #1, Bus A, connection
BUS_B_HI, BUS_B_LO	Channel #1, Bus B, connection
BUS_A'_HI, BUS_A'_LO	Channel #2 (EPMI only), Bus A, connection
BUS_B'_HI, BUS_B'_LO	Channel #2 (EPMI only), Bus B, connection
SHIELD (case)	Provided for 1553 cables shield connection. This signal is connected to the case of the computer through the metal PC bracket on the back end of the board.
EXSTART$	External Start Low Active TTL input (see Concurrent Start Register, page 2-5).
EXTTCLKx	Bank #x External Time Tag Clock TTL input. Provides an option to drive the Time Tag Counter clock from an external source for synchronizing in a multiple-board application. Connect a 250KHz or less clock with respect to the GND pin. Note: The external clock takes effect only after the user activates the EXTTCLK bit in the Time Tag Options register (see Time Tag Options Register, page 4-17 and 6-16).
EXTTRSTx$	Bank #x External Time Tag Reset low active TTL input. Provides an option to reset the Time Tag counter from an external source, to achieve common initialization in a multiple-board application. Apply a low TTL pulse of 100 nsec/min. with respect to the GND pin. **Note**: The reset takes affect only after the board is started in RT or BM mode.
GND	Provides ground reference for the digital signal connections.

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9.4.4 PC Bus Edge Connectors Pinout

XT/AT

Pin	Signal
A1	
A2	D7
A3	D6
A4	D5
A5	D4
A6	D3
A7	D2
A8	D1
A9	D0
A10	I/OCHRDY
A11	
A12	A19
A13	A18
A14	A17
A15	A16
A16	A15
A17	A14
A18	A13
A19	A12
A20	A11
A21	A10
A22	A9
A23	A8
A24	A7
A25	A6
A26	A5
A27	A4
A28	A3
A29	A2
A30	A1
A31	A0

Pin	Signal
B1	GND
B2	RESET
B3	+5V
B4	IRQ2(9)
B5	
B6	
B7	-12V
B8	
B9	+12V
B10	GND
B11	MEMW–
B12	MEMR–
B13	
B14	
B15	
B16	
B17	
B18	
B19	
B20	
B21	IRQ7
B22	IRQ6
B23	IRQ5
B24	IRQ4
B25	IRQ3
B26	
B27	
B28	ALE
B29	+5V
B30	
B31	GND

AT BUS EXTENSION

Pin	Signal
C1	
C2	
C3	
C4	
C5	
C6	
C7	
C8	
C9	
C10	
C11	
C12	
C13	
C14	
C15	
C16	
C17	
C18	

Pin	Signal
D1	
D2	
D3	IRQ10
D4	IRQ11
D5	IRQ12
D6	IRQ15
D7	IRQ14
D8	
D9	
D10	
D11	
D12	
D13	
D14	
D15	
D16	+5V
D17	
D18	GND

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9.5 Mechanical Outline

The EXC-1553PC/EP board can be ordered in eight variations:

- Half-size board without a concurrent bus monitor (cannot be added)
- Full-size board without a concurrent bus monitor (can be added later)
- Full-size board with a non-independent, concurrent bus monitor (independent concurrent monitor can be added later)
- Full-size board with an independent, concurrent bus monitor

All the above can be ordered with MIL-STD-1760 options.

See Ordering Information, page 10-1, for the exact part numbers.

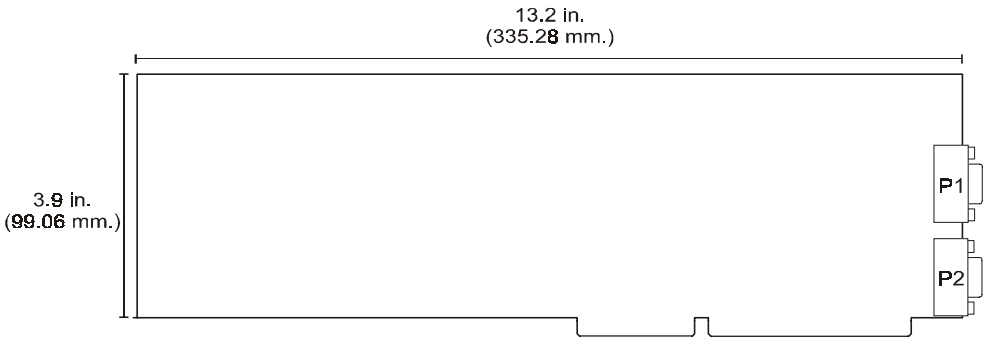


Figure 9-3 EXC-1553PC/EP (Full Size) Board: Mechanical Outline

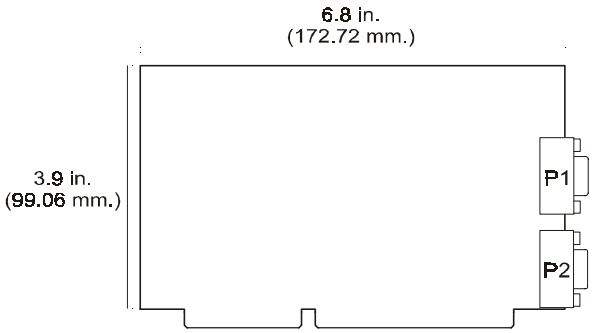


Figure 9-4 EXC-1553PC/EP-H (Half Size) Board: Mechanical Outline

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9.6 Power Requirements

The power required by the EXC-1553PC/EP depends on the options ordered. Power requirements are listed in the following tables:

	+5v	+12v	-12v
EXC-1553PC/EP **EXC-1553PC/EP-H**	1.8A	150mA	150mA

	+5v	+12v	-12v
EXC-1553PC/EPM	2.8A	150mA	150mA

	+5v	+12v	-12v
EXC-1553PC/EPMI	3.0A	180mA	180mA

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10 Ordering Information

Chapter 10 explains how to indicate which options you want when ordering an EXC-553PC/EP board.

The following suffixes can be added to the name of the board (EXC-1553PC/EP) to indicate specific options. The suffixes are added to "EXC-1553PC/EP" in the order in which they appear in the table.

SUFFIX	DESCRIPTION
M	Concurrent monitor option
I	Independent (secondary) concurrent monitor channel option
-H	Half size board
-1760	MIL-STD 1760 options

Ordering examples:

PART NUMBER	DESCRIPTION
EXC-1553PC/EP	MIL-STD-1553 interface board, full size, for PC computers. Supports BC, RT, BC/RT and BM modes.
EXC-1553PC/EPM	MIL-STD-1553 interface board, full size, for PC computers. Supports BC, RT, BC/RT and BM modes. With concurrent monitor.
EXC-1553PC/EPMI	MIL-STD-1553 interface board, full size, for PC computers. Supports BC, RT, BC/RT and BM modes. With independent (secondary) concurrent monitor channel.
EXC-1553PC/EP-H	MIL-STD-1553 interface board, half size, for PC computers. Supports BC, RT, BC/RT and BM modes. Without concurrent monitor.
EXC-1553PC/EP-1760	MIL-STD-1553 interface board, full size, for PC computers. Supports BC, RT, BC/RT and BM modes with MIL-STD 1760 options.

NOTE The Independent Monitor option is only available in conjunction with the Concurrent Monitor option.

The Half-Size Board option is not available with the Concurrent Monitor option.

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11 Appendices

Chapter 11 contains appendices describing the Military Standard 1553B word, Military Standard message formats, firmware revision enhancements, Internal and External loopback tests and customer support. These topics are discussed on the following pages:

MIL-STD-1553B Word Formats	page 11-2
MIL-STD-1553B Message Formats	page 11-3
Firmware Revision Enhancements	page 11-4
Internal Loopback Test	page 11-8
External Loopback Test	page 11-9
Customer Support	page 11-10

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Appendix A MIL-STD-1553B Word Formats

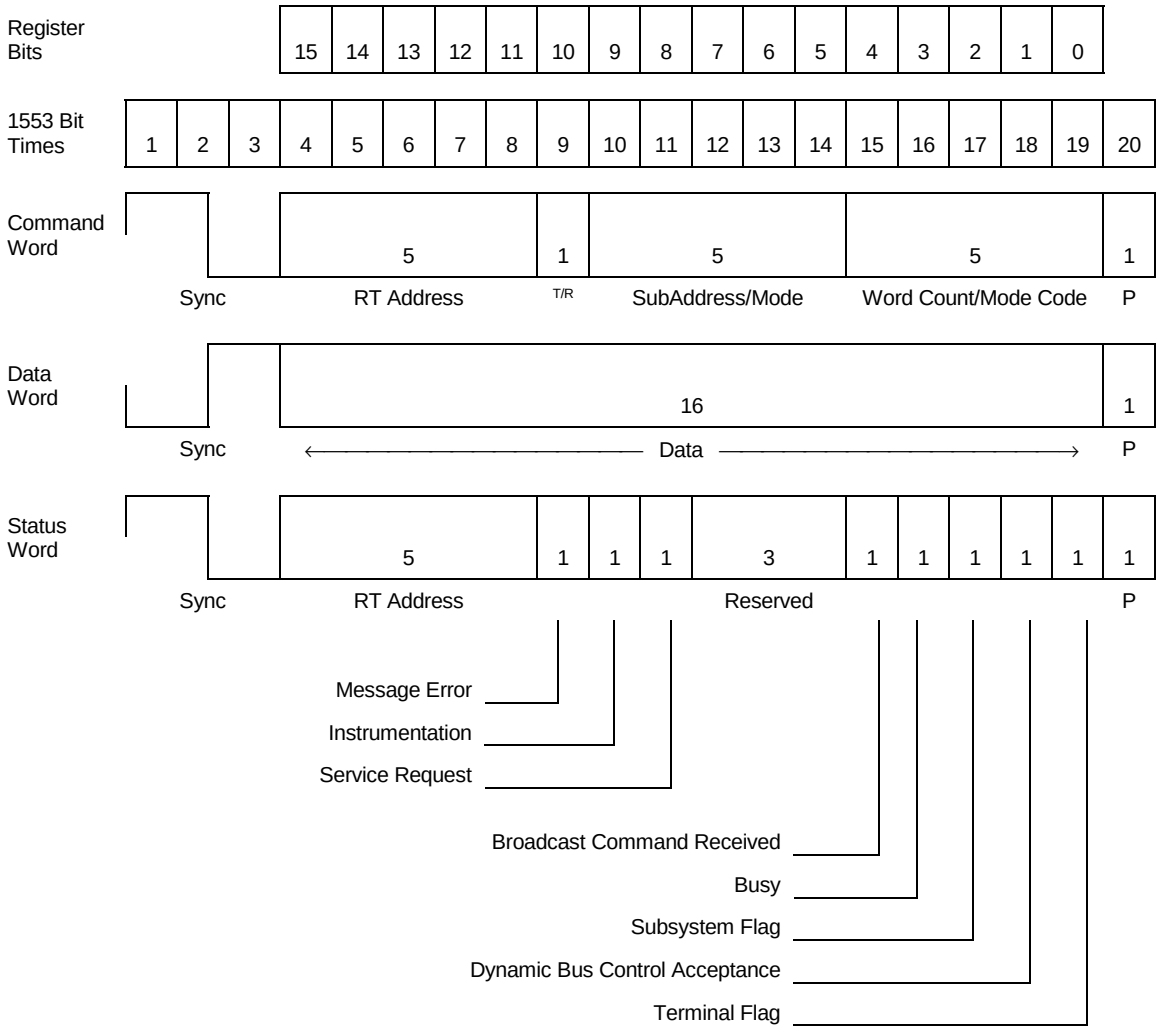


Figure 11-1 MIL-STD-1553B Word Formats

NOTE: T/R = Transmit/Receive
P = Parity

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Appendix B MIL-STD-1553B Message Formats

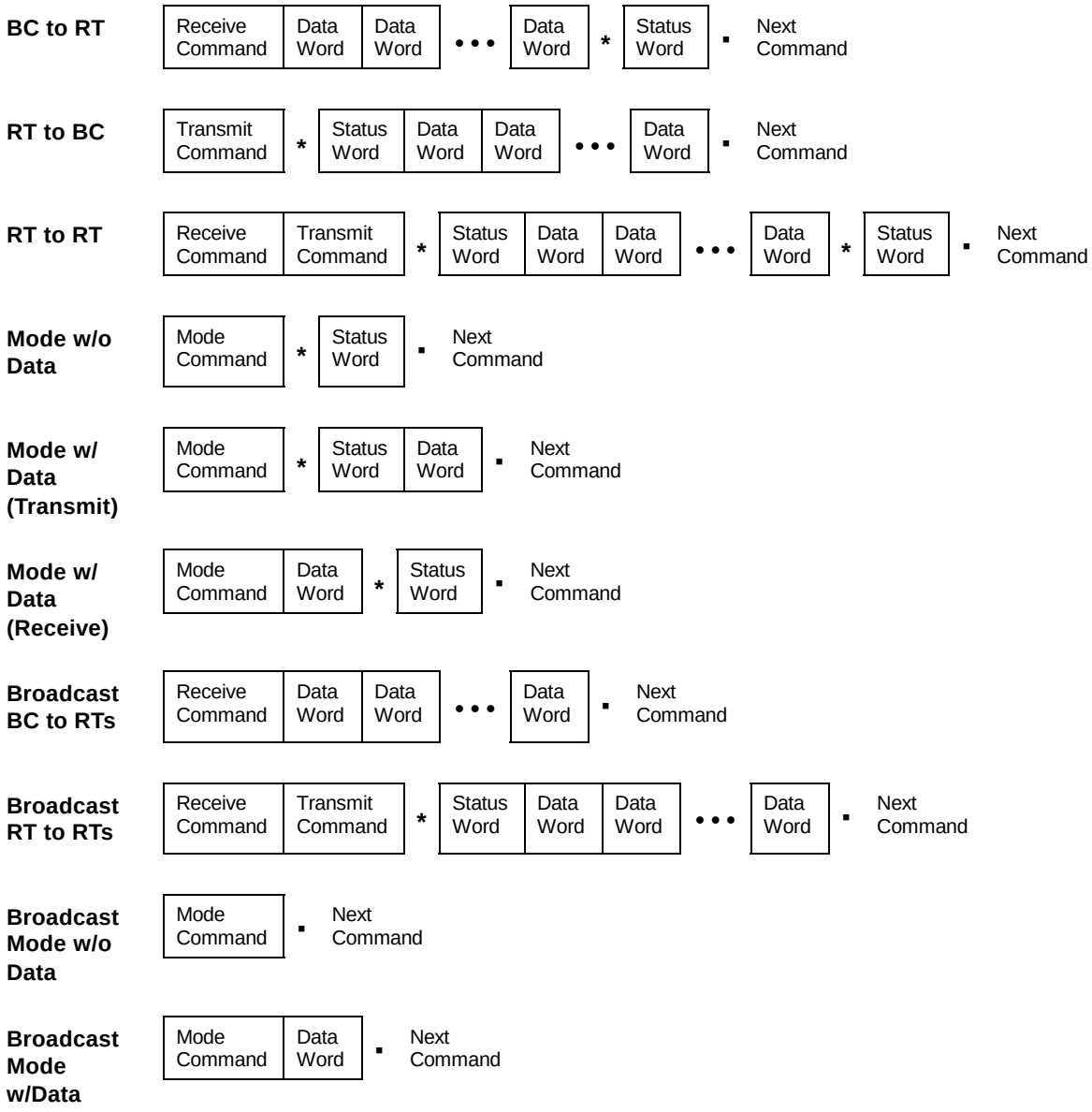


Figure 11-2 MIL-STD-1553B Message Formats

NOTE: * = Response time
▪ = Intermessage gap

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Appendix C Firmware Revision Enhancements

Version Description Document

EXC-1553PC/EP

In keeping with Excalibur's proven record as an industry leader in avionics board-level test and simulation products, Excalibur continuously develops and improves its EXC-1553PC/EP series of MIL-STD-1553 testers.

Excalibur EXC-1553PC/EP boards with firmware revision 3.0 and higher implement major improvements in both hardware and firmware functionality. While these boards are compatible with earlier versions of the board, hardware and firmware enhancements make them more robust and high-performance products.

This appendix describes the enhancements in:

- Firmware revision 3.0+
- Firmware revision 4.0+

The following list of changes is divided into these categories:

- Global changes
- Changes relevant to a particular operational mode:
  - BC mode changes
  - RT mode changes
  - BC/Concurrent RT mode changes
  - Bus Monitor mode changes

NOTE * Items marked with an asterisk represent minor programming changes.

Firmware Revision 3.0+

GLOBAL CHANGES

- The Variable Amplitude register now defaults to 255 (7.5 volts peak-to-peak on the bus) on power up or software reset.
- The Time Tag of each available bank can be read directly by the host, at any time.
- The Time Tag Clock and Time Tag Reset of each available bank can be driven by external signals. This feature enables the synchronization of the Time Tags of multiple boards.
- In the Board Status register, changed the 16K RAM OK and 2K RAM OK bit definitions to RAM OK and Timers OK, respectively.

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- In bank 0,added hardware to allow two separate self-test functions: Internal_Loopback_Test and External_Loopback_Test (requires external loopback cable). Activate the loopback tests by writing appropriate codes to the Board Configuration register and starting the board.
- Board internal operation is significantly faster; as a result, recovery times after power-on and software reset have been greatly decreased.
- Incorporated the functionality of the Emulated RT and Fast BC/RT modes of operation into the regular RT and BC/RT modes. However, to ensure upward compatibility, these two modes continue to be implemented, separately, for downward compatibility purposes. New users should ignore these modes.
- Board firmware is downloadable and may be updated from diskette, as needed.
- Changed the physical position of DIP switches, LEDs, and other components relative to that of older boards.
- Slightly increased the board's +5 Volt power requirements.
- Shortened the length of the EXC-1553PC/EP-H to 6.8 inches.

BC MODE CHANGES

* In BC mode, the programmable Intermessage Gap Time (IGT) range is programmable from 4 µsec (bus dead time) to 665 seconds. The programmed value is added to the minimum 4 µsec (a value of 0 sets the IGT to 4 µsec).
- The Jump command is now included within the BC Command code of the Control word.
- The minimum gap between transmission of the last word in the frame and transmission of the first word in the following frame is now 20 µsecs. (down from 120 µsec).
- Word Count Error Injection allows sending BC to RT messages with up to '0' Data words.
- In the Message Status word, the Internal Test Error bit is reserved.

RT MODE CHANGES

- The RT can handle messages with the minimum 4 µsec Intermessage Gap Time (mid-bit to mid-bit) permitted by the 1553 specification.

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* The RT Time Tag is derived from a 16-bit hardware counter whose resolution may be set in steps of 4 µsec by the 8-bit Time Tag Resolution register. The Time Tag is stored while the Command word is received (in RT-to-RT commands, while the first Command word is received). Note that the Time Tag Preset High and Low, and Time Tag Resolution High registers are no longer implemented.
- Bit Count error injection supports ± 1, 2, or 3 bits.
* The RT response time is fully programmable from 4 µsec to 43.5 µsec (bus dead time).
* Defined a new bit that selects either 1553B or non-1553B environment in the Status Response register.
* Defined two new bits in the Active Remote Terminal byte, which let you ignore messages to a specific RT on one of the buses (A or B), (applies to firmware revision 3.3 and higher).

BC/Concurrent RT Mode Changes

- All changes listed under BC mode also apply to BC/Concurrent RT mode.
* The Message Block Control word is the same as that in BC mode (error placement can be selected either in a Command or Data word).

Bus Monitor Mode Changes

* A new register, the Broadcast Control register, allows the user to instruct the board whether or not to expect Status words on messages directed to RT #31.
* The Time Tag mode (16- or 32-bit) is DIP switch-selectable and is stored during reception of the Command word (the first Command word in the case of RT-to-RT commands). The 16- or 32-bit mode can be selected independently for each bank.
* In the 16-bit Time Tag mode, the resolution is fixed at 4 µsec and the Time Tag Preset and Time Tag Resolution register pairs are not used.
* Defined two new bits in the Message Status word: Message Error Bit Set and RT Status Bit Set. These bits operate as in the BC Message Status word.
- Added additional functionality to bit 00 of the Message Status register. In Bus Monitor Sequential mode this bit operates as a Trigger Word Received bit. In Bus Monitor Link-List and Bus Monitor Look-up modes, bit 00 of the Message Status register operates as a Busy bit.

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Firmware Revision 4.0+

GLOBAL CHANGES

- Added a data integrity function that indicates that a message is currently being transmitted, and should not be altered.

RT MODE CHANGES

- Added the ability to generate an interrupt on broadcast message.

BC/CONCURRENT- RT MODE CHANGES

- Added MINOR_FRAME, a new message type which functions as a "delay time" message, between groups of messages. Use the minor frame to produce a list of messages that will be sent out over the bus at different frequencies.
- Added Asynchronous Frame operation, so that in the middle of the transmission of the messages of a frame, the user can transmit another frame and then return to continue transmitting the messages of the previous frame.
- Added the ability to generate an interrupt after any specific message.
- Added the ability to generate an interrupt after a minor frame is processed.

BUS MONITOR MODE CHANGES

- Added a Time Tag Resolution register to Bus Monitor mode.

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Appendix D Internal Loopback Test

The Internal Loopback Test is used to check the 1553 front-end logic, excluding transceivers and coupling transformers.

To initiate the Internal Loopback Test:

1. Write ED (H) into the Board Configuration Register.
2. Write 1 into the Start Register.
3. Wait for 0 in the Start Register.

The results of this test are returned to the host in dual-port RAM using the following structure beginning at address 0:

struct I_LOOPBACK

{

Definition	Address in Dual-Port RAM	Status Value
usint frame_val;	0	X (not for user)
usint frame_status; frame time counter status	2	8000H passed, 8001H failed
usint resp_status; response time counter status	4	8000H passed, 8001H failed
usint early_val;	6	6 LSB must be 15H
usint receive_data1; first looped word test, using command sync	8	5555H
usint status_1;	A	8000H passed, else failed
usint receive_data2; second looped word test, using data sync	C	AAAAH
usint status_2;	E	8000H passed, else failed
usint mc_status; mode code function test	10	8000H passed, else failed
usint ttag_val_lo;	12	30D4H ± 2
usint ttag_val_hi;	14	0
usint ttag_status; time tag status	16	8000H passed, 8001H failed
usint prl;	18	8 LSB contain the CPU version

} *I_loopback;

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Appendix E External Loopback Test

The External Loopback Test is used to check the 1553 transceivers, transformers and associated bus cables.

NOTE The External Loopback Test requires a loopback cable to connect bus A to bus B.

To initiate the External Loopback test:

1. Write FF (H) into the Board Configuration Register.
2. Write 1 into the Start Register.
3. Wait for 0 in the Start Register.

The results of this test are returned to the host in dual-port RAM using the following structure beginning at address 0:

struct E_LOOPBACK

{

	Definition/ conditions for passing E_loopback test [TX-bus, RX-bus, command or data sync]	Address in Dual-Port RAM	Status Value
usint frame_val;		0	X (not for user)
usint frame_status;	frame time counter status	2	8000H passed, 8001H failed
usint cmd_send[8];		4	cmd_send[0]: 5555H
	TX-A, RX-A, command sync	6	cmd_send[1]:8000H passed, else failed
		8	cmd_send[2]: 1234H
	TX-A, RX-B data sync	A	cmd_send[3]:8000H passed, else failed
		C	cmd_send[4]: 5555H
	TX-B, RX-A command sync	E	cmd_send[5]:8000H passed, else failed
		10	cmd_send[6]: 1234H
	TX-B, RX-B data sync	12	cmd_send[7]:8000H passed, else failed
usint ttag_val_lo		14	30D4H ± 2
usint ttag_val_hi		16	0
usint ttag_status;	time tag status	18	8000H passed, 8001H failed

} *E_loopback;

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Appendix F Customer Support

Excalibur Systems, Inc. is interested in the applications you develop with our products, and we are ready to answer any technical questions you may have.

When you want to talk to us, call the representative nearest you, or contact our corporate headquarters or website as follows:

EXCALIBUR WEBSITE	www.mil-1553.com
EXCALIBUR CORPORATE HEADQUARTERS	Tel.: 1-800-MIL-1553 (Toll Free) Fax.: 516-327-4645 Email: excalibur@mil-1553.com

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