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# EXC-1553PCI/Px

## MIL-STD-1553
## Test and Simulation Board
## for PCI Systems

# User's Manual

EXCALIBUR SYSTEMS

311 Meacham Avenue ◆ Elmont, NY 11003 ◆ Tel. (516) 327-0000 ◆ Fax (516) 327-4645
e-mail: excalibur@mil-1553.com website: www.mil-1553.com

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# 1 Introduction

Chapter 1 provides an overview of the EXC-1553PCI/P*x* avionics communication board. The following topics are covered:



## 1.1 Overview

The EXC-1553PCI/P*x* is an intelligent, MIL-STD-1553 interface board for PCI systems. Available with up to four independent 1553 channels, the EXC-1553PCI/P*x* provides a complete solution for developing and testing 1553 interfaces and performing system simulation of the MIL-STD-1553 bus. All standard variations of the MIL-STD-1553 protocol are handled by the board. Each channel of the EXC-1553PCI/P*x* contains 32k × 8 of dual-port RAM for data blocks, control registers, and look-up tables. All data blocks and control registers are memory mapped and may be accessed in real-time.

Each of the independent dual redundant 1553 channels may be programmed to operate in one of four modes of operation: Bus Controller, Remote Terminal, Bus Controller/Concurrent-RT, and Bus Monitor. The EXC-1553PCI/P*x* comes complete with menu-driven software, a C-driver software library including source code. 1553 adapter cables and couplers are an optional extra.



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**EXC-1553PCI/Px Board Features:**

- Up to four independent 1553 channels
- PCI half-size board

**Features Per Channel:**

- Operates as BC, RT, BC/Concurrent-RT or Triggerable Bus Monitor
- Handles 4µsec. intermessage gap times in all modes
- Real-time operation
- Multiple protocol capability (i.e. 1553A, B, F-16)
- Multiple-RT simulation (up to 32 remote terminals)
- Programmable broadcast mode
- Multi-mode triggerable Monitor
- Extensive interrupt features
- Error injection capability:
  Word count (+/-3 words)
  Incorrect sync.
  Incorrect RT address
  Non-contiguous data

**Examples of user selectable parameters:**

- Select whether an RT will return a status word in the event a message containing a data word error is received by the RT.
- Selectable broadcast mode
- Variable response time
- Variable transmit amplitude
- Select mode code subaddress (00000, 11111, or both)
- 1553A RT timing
- Define each bit in the 1553 Status word

**Each of the board's channels has four modes of operation:**

- Bus Controller (BC) mode
- Multiple Remote Terminal (RT) mode (up to 32 RTs)
- BC with Concurrent RT operation (up to 32 RTs)
- Triggerable Bus Monitor mode

The EXC-1553PCI/P*x* can be ordered with one to four installed channels. See Ordering Information, page 10-1 for the exact part numbers.



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## 1.2 Installation

EXC-1553PCI/P*x* installation includes installing the software for each system and installing the board.

### 1.2.1 Software Installation

The standard software included with the EXC-1553PCI/P*x* is for Windows operating systems. Software compatible with other operating systems is available and can be downloaded from our website: www.mil-1553.com.

For information about installing the accompanying software drivers, see **ReadMe.txt** on the *Galahad Software Tools* diskettes that came with your board.

### 1.2.2 Board Installation

Installation of the EXC-1553PCI/P*x* board is similar to that of all PCI boards. The EXC-1553PCI/P*x* complies with the "Plug and Play" specification of the PCI standard, and as such its absolute address is determined by the BIOS at system start-up.

**WARNING** *You should wear a suitably grounded electrostatic discharge wrist strap whenever handling the Excalibur board and use all necessary antistatic precautionary measures.*

To install the EXC-1553PCI/P*x*:

1. 1553 devices may be connected to the 1553 bus either directly (direct-coupled) or via a bus-coupling stub (transformer coupled). Use jumpers JP1-16 to set the coupling mode to the 1553 bus(es) (see Jumpers, page 9-3).
2. *Make certain the computer power source is disconnected*. Insert the EXC-1553PCI/P*x* board into any PCI-compatible slot.
3. Attach the user-constructed 1553 bus cable to the board and to the bus. The cable may be connected to and disconnected from the board while power to the computer is turned on, but not while the board is transmitting over the bus.



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## 1.3 1553 Bus Connections

For short distances, the EXC-1553PCI/P*x* may be coupled directly to another 1553 device. To ensure data integrity, you must make certain that the cable connecting the two devices is properly terminated with 78 Ohm resistors (see Figure 1-1).

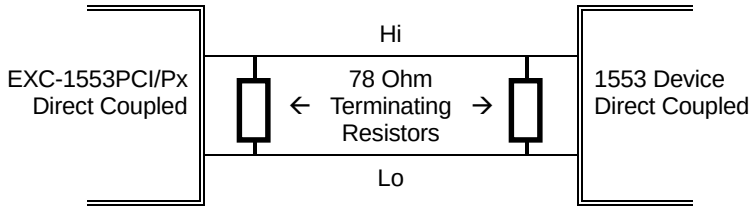


**Figure 1-1 Direct Coupled Connection (One Bus Shown)**

If operating in the more standard Transformer coupling mode, use stub coupler devices, which are available from Excalibur Systems, Inc. Two terminators are required for each coupler, which services a single bus [e.g. BUS A] (see Figure 1-2). For more information about couplers see our website: www.mil-1553.com.

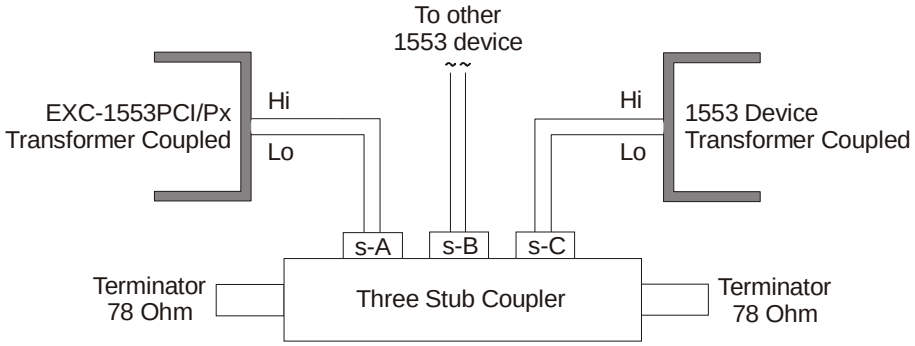


**Figure 1-2 Transformer Coupled Connection (One Bus Shown)**



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# 2 PCI Architecture

Chapter 2 describes the PCI architecture. The following topics are covered:



## 2.1 Memory Structure

The EXC-1553PCI/P*x* requests five memory blocks: the first memory block is 256 bytes in size and contains a memory mapping of the PCI Configuration Space Header region. The remaining four memory blocks are 32Kb each in size and contain dual-port RAM for the 1553 channels.

For more detail on the memory block allocations, see Base Address Registers, page 2-7.

The EXC-1553PCI/P*x* does not use any I/O space.



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## 2.2 PCI Configuration Space Header

The EXC-1553PCI/P*x* includes a PCI Configuration Space Header, as required by the PCI specification. The registers contained in this header enable software to set up the Plug and Play operation of the board, and set aside system resources.

The mailbox at address 40H contains the Interrupt Status Register.

| | | | | |
|---|---|---|---|---|
| Reserved = 0s | | | Interrupt Status | 40 H |
| MAX_LAT | MIN_GNT | Interrupt Pin | Interrupt Line | 3C H |
| Reserved = 0s | | | | 38 H |
| Reserved = 0s | | | Cap. pointer | 34 H |
| Expansion ROM Base Address (not used) | | | | 30 H |
| Subsystem ID | | Subsystem Vendor ID | | 2C H |
| Cardbus CIS Pointer (not used = 0s) | | | | 28 H |
| Base Address Register #5 (not used) | | | | 24 H |
| Base Address Register #4 (Channel 3) | | | | 20 H |
| Base Address Register #3 (Channel 2) | | | | 1C H |
| Base Address Register #2 (Channel 1) | | | | 18 H |
| Base Address Register #1 (Channel 0) | | | | 14 H |
| Base Address Register #0 PCI Configuration Space | | | | 10 H |
| BIST | Header Type = 0 | Latency Timer | Cache Line Size | 0C H |
| Class Code | | | Rev ID | 08 H |
| Status Register | | Command Register | | 04 H |
| Device ID | | Vendor ID | | 00 H |
| **31 24** | **23 16** | **15 08** | **07 00** | |

**Figure 2-3 PCI Configuration Space Header**



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## 2.3 PCI Configuration Registers

This section describes the registers contained in the PCI Space Header.

### 2.3.1 Vendor Identification Register (VID) Address: 00–01 (H)

**Power-up value:** 1405 H

**Size:** 16 bits

The Vendor Identification register contains the PCI Special Interest Group vendor identification number assigned to Excalibur Systems. .

### 2.3.2 Device Identification Register (DID) Address: 02–03 (H)

**Power-up value:** 1103 H

**Size:** 16 bits

The Device Identification register contains the EXC-1553PCI/P*x* device identification number.



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### 2.3.3 PCI Command Register (PCICMD) Address: 04–05 (H)

**Power-up value:** 0000 H

**Size:** 16 bits

The PCI Command register contains the PCI Command.

| Bit | Bit Name | Description |
|---|---|---|
| **10-15** | **Reserved** | Set to 0s |
| **09** | **Fast Back-to Back Enable** | Always set to 0 |
| **08** | **System Error Enable** | Always set to 0 |
| **07** | **Address Stepping Support** | Always set to 1 |
| **06** | **Parity Error Enable** | Always set to 0 |
| **05** | **VGA Palette Snoop Enable** | Always set to 0 |
| **04** | **Memory Write and Invalidate Enable** | Always set to 0 |
| **03** | **Special Cycle Enable** | Always set to 0 |
| **02** | **Bus Master Enable** | Always set to 0 |
| **01** | **Memory Access Enable** | Always set to 1 |
| **00** | **I/O Access Enable** | Since the PCI/P*x* board does not use I/O space, the value of this register is ignored. |

**PCI Command Register**



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### 2.3.4 PCI Status Register (PCISTS) Address: 06–07 (H)

**Power-up value:** 0080 H

**Size:** 16 bits

The PCI Status register contains the PCI status information.

| Bit | Bit Name | Description |
|---|---|---|
| 15 | Detected Parity Error | This bit is set whenever a parity error is detected. It functions independently from the state of Command Register Bit 6. This bit may be cleared by writing a 1 to this location. |
| 14 | Signaled System Error | Not used |
| 13 | Received Master Abort | Not used |
| 12 | Received Target Abort | Not used |
| 11 | Signaled Target Abort | This bit is set whenever this device aborts a cycle when addressed as a target. This bit can be reset by writing a 1 to this location. |
| 09-10 | Device Select (DEVSEL#) Timing Status | Set to 10 (slow timing) |
| 08 | Data Parity Reported | Not used |
| 07 | Fast Back-to-Back Capable | Set to 1 |
| 06 | Reserved | |
| 05 | 66MHz capable | Set to 0 |
| 04 | Capability List enable | Set to 1 |
| 00-03 | Reserved | |

**PCI Status Register**

### 2.3.5 Revision Identification Register (RID) Address: 08 (H)

**Power-up value:** 01 H

**Size:** 8 bits

The Revision Identification register contains the revision identification number of the EXC-1553PCI/P*x*.



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### 2.3.6 Class Code Register (CLCD)

**Address: 09-0B (H)**

**Power-up value:** FF0000 H

**Size:** 24 bits

The Class code Register value indicates that the EXC-1553PCI/P*x* does not fit into any of the defined class codes.

### 2.3.7 Cache Line Size Register (CALN)

**Address: 0C (H)**

**Power-up value:** 00 H

**Size:** 8 bits

Not used

### 2.3.8 Latency Timer Register (LAT)

**Address: 0D (H)**

**Power-up value:** 00 H

**Size:** 8 bits

Not used

### 2.3.9 Header Type Register (HDR)

**Address: 0E (H)**

**Power-up value:** 00 H

**Size:** 8 bits

The EXC-1553PCI/P*x* is a single function PCI device.

### 2.3.10 Built-In Self-Test Register (BIST)

**Address: 0F (H)**

**Power-up value:** 00 H

**Size:** 8 bits

The Built-In Self-Test register is not implemented in the EXC-1553PCI/P*x*.



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### 2.3.11 Base Address Registers (BADR) Address: 10, 14, 18, 1C, 20, 24 (H)

**Power-up value:** 00000000 H for each

**Size:** 32 bits

The Base Address Registers are used by the system BIOS to determine the number, size and base addresses of memory pages required by the board, within host address space.

Five memory pages are required by the EXC-1553PCI/P*x:* one for the PCI Configuration Space Header and four for the 1553 channels.

| Register | Offset | Size | Function |
|---|---|---|---|
| Base Address Register 0 | 10 H | 256 Byte | PCI Configuration Space Header |
| Base Address Register 1 | 14 H | 32 Kb | MIL-STD-1553 Channel 0 |
| Base Address Register 2 | 18 H | 32 Kb | MIL-STD-1553 Channel 1 |
| Base Address Register 3 | 1C H | 32 Kb | MIL-STD-1553 Channel 2 |
| Base Address Register 4 | 20 H | 32 Kb | MIL-STD-1553 Channel 3 |

**Table 2-1 Base Address Registers Definition**

Each Base Address Register contains 32 bits:

| Bit | Description |
|---|---|
| **04-31** | Address of memory region (with lower 4 bits removed) |
| **03** | Always 0 – memory is not prefetchable |
| **01-02** | Always 0 – memory may be mapped anywhere |
| **00** | Always 0 – indicates memory space |

**Base Address Register**

### 2.3.12 Cardbus CIS Pointer Address: 28 (H)

**Power-up value:** 00000000 H

**Size:** 32 bits

The Cardbus Pointer is not implemented on the EXC-1553PCI/P*x*.



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### 2.3.13 Subsystem ID

**Address: 2C (H)**

**Power-up value:** 0000 H

**Size:** 16 bits

### 2.3.14 Subvendor ID

**Address: 2E (H)**

**Power-up value:** 0000 H

**Size:** 16 bits

### 2.3.15 Expansion ROM Base Address Register (XROM)

**Address: 30 (H)**

**Power-up value:** 00000000 H

**Size:** 32 bits

The Expansion ROM Space is not implemented on the EXC-1553PCI/P*x*.

### 2.3.16 Reserved

**Address: 34-3A (H)**

**Power-up value:** 0000000000000000 H

**Size:** 64 bits

### 2.3.17 Interrupt Line Register (INTLN)

**Address: 3C (H)**

**Power-up value:** 0B H

**Size:** 8 bits

The Interrupt Line register indicates the interrupt routing for the PCI Controller. The value of this register is system-architecture specific. For *x*86-based PCs, the values in this register correspond with the established interrupt numbers associated with the dual 8259 controllers used in those machines; the values of 0 to F (H) correspond with the IRQ numbers 0 through 15, and the values from 10(H) to FE(H)are reserved. The value of 255 signifies either “unknown” or “no connection” for the system interrupt.



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### 2.3.18 Interrupt Pin Register (INTPIN)

**Address: 3D (H)**

**Power-up value:** 01 H

**Size:** 8 bits

Set to INTA#

### 2.3.19 Minimum Grant Register (MINGNT)

**Address: 3E (H)**

**Power-up value:** 00 H

**Size:** 8 bits

The Minimum Grant register is not implemented on the EXC-1553PCI/P*x*.

### 2.3.20 Maximum Latency Register (MAXLAT)

**Address: 3F (H)**

**Power-up value:** 00 H

**Size:** 8 bits

The Maximum Latency register is not implemented on the EXC-1553PCI/P*x*.



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### 2.3.21 Interrupt Status Register

**Address: 40 (H)**

**Power-up value:** 00000000 H

**Size:** 32 bits

**Attribute** Read only

During an interrupt, the Interrupt Status Register indicates which 1553 channels are interrupting. The interrupts may be reset by writing to the relevant channel's Interrupt Reset Register [7001(H)]. After the interrupt is reset by writing to the relevant Interrupt Reset Registers, the bits in the Interrupt Status Register will automatically be reset.

| Bit | Description |
|---|---|
| **31-4** | Always set to 0 |
| **03** | 1 = Interrupt from channel 3 |
| **02** | 1 = Interrupt from channel 2 |
| **01** | 1 = Interrupt from channel 1 |
| **00** | 1 = Interrupt from channel 0 |

**Interrupt Status Register**



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# 3 Bus Controller Operation

In this manual the Bus Controller (BC) mode is included in BC/Concurrent-RT mode. Refer to Chapter 5 BC/Concurrent-RT Operation, page 5-1, for information regarding BC mode.



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# 4 Remote Terminal Operation

Chapter 4 describes EXC-1553PCI/P*x* operation in Remote Terminal (RT) mode. The information in this chapter applies to all 1553 channels present on the board. All addresses referred to in this chapter are offset from the base address of the channel accessed (see Base Address Registers, page 2-7). The following topics are covered:



The EXC-1553PCI/P*x* can be configured to simulate up to 32 remote terminals. The user selects which terminal(s) are operating (active). In addition, errors can be injected into message responses.

After receiving the Start command, the board handles the transfer of all messages (see Control Register Definitions, page 4-15). Data associated with a particular RT subaddress combination is transferred via a 2K x 8 Look-up table, which points to one of 200 data blocks. You load data blocks associated with transmit commands with 1553 data to transmit, and read received 1553 data from data blocks associated with receive commands.

The board will respond properly to messages received with an intermessage gap of 4 µsec.

The user chooses whether the remote terminal should transmit its 1553 status word at the end of a message, even if the message contains *invalid* data words (invalid as specified by MIL-STD-1553). Use the Status Response register to activate or disable this feature. (See Control Register Definitions, page 4-15.)



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The remote terminal transmits its 1553 status word in approximately 4 μsec. Use the RT Response Time register to increase the time it takes the remote terminal to transmit the 1553 status word.

Since most 1553 parameters, such as response time, status word content, etc. are user-programmable, the board can operate in various 1553 environments. The board also allows you to enable or disable the 1553 Broadcast function. If broadcasting is enabled, RT address 31 (11111) is reserved; if broadcasting is disabled, all 32 RT addresses are available (see Options Select Register, page 4-16).

The 1553 Mode Code subaddress identifier (see Mode Code Control Register, page 4-22) can be programmed so that either 31, 0, or both are used to indicate that the 1553 command word is a Mode code.

Perform the following procedure after a power-up or a software reset.

To determine whether the board is installed and ready to operate:

1. Check the Board ID register (test for value = 45 H).
2. Check the Board Status register (test for Board Ready bit = 1).

The board is installed and ready when both registers contain the correct values (as written above). For software reset operations, set these values to 0 immediately prior to writing to the (software) Board Reset register.

**NOTE** Throughout this manual, writing a 1 to the Start register is referred to as “issuing a Start command.”



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## 4.1 RT Memory Map

Figure 4-1 illustrates the RT memory usage.

| | | | |
|---|---|---|---|
| Reserved | 700D – 7FFF H | | |
| Time Tag Options | 700C | | |
| Time Tag Counter Word 1 | 700A – 700B H | | |
| Time Tag Counter Word 0 | 7008-7009 H | | |
| Time Tag Reset Register | 7007 H | | |
| Reserved | 7004 – 7006 H | Status Response Register | 3FEF H |
| Options Select Register | 7003 H | Reserved | 3E86 – 3FEE H |
| Global Software Reset Register | 7002 H | Boards Option Register | 3E84 H |
| Interrupt Reset Register | 7001 H | Reserved | 3E81 – 3E83 H |
| Software Reset Register | 7000 H | Firmware Revision Register | 3E80 H |
| Data Block Look-Up Table | 4000 – 47FF H | Reserved | 34C0 – 3E7F H |
| Board Configuration Register | 3FFF H | 1553 RT Vector Words (64 Bytes) | 3480 – 34BF H |
| Board ID Register | 3FFE H | 1553 RT Bit Words (64 Bytes) | 3440 – 347F H |
| Board Status Register | 3FFD H | RT Last Command Words (64 Bytes) | 3400 – 343F H |
| Start Register | 3FFC H | Reserved | 33FD – 33FF H |
| Message Status Register | 3FFB H | Interrupt Condition Register | 33FC H |
| Reserved | 3FF8 H | Message Stack (42 Blocks) | 3300 – 33FB H |
| Time Tag Resolution Register | 3FF7 H | Word Count Error Table (32 Bytes) | 32E0 – 32FF H |
| Reserved | 3FF5 – 3556 H | Reserved | 3267 – 32DF H |
| | | Mode Code Control | 3266 H |
| RT Response Time Register | 3FF4 H | Reserved | 3260 – 3265 H |
| Error Injection Register | 3FF3 H | 1553 RT Status Words (64 Bytes) | 3220 – 325F H |
| Reserved | 3FF2 H | Active RT Table (32 Bytes) | 3200 321F H |
| Message Stack Pointer | 3FF0 – 3FF1 H | 1553 Data Blocks (200 Blocks) | 0000 – 31FF H |

**Figure 4-1 RT Memory Map**



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## 4.2 Data Block Look-Up Table

**Address: 4000–47FF (H)**

The received command word's RT Address, T/R Bit, and Subaddress fields are used to index the entries in the (user-programmed) look-up table. Each entry in the table represents a data block number (from 0 to 199 decimal). Each block can contain up to 32 1553 Data Words (64 bytes). Data Block 0 begins at address 0000, Data Block 1 begins at address 0040 (H), etc.

| | (11 most significant bits of the 1553 command word) | | | | | |
|---|---|---|---|---|---|---|
| **Base Address** | **RT address (5 bits)** | **T/R (1 bit)** | **Sub-address (5 bits)** | **Look-up table (2K x 8)** | **Data block** | **Hex address of data block** |
| 4000+ | 11111 | 1 | 11111 | Block # | Data Block 199 | 31C0 |
| | • | • | • | • | • | |
| | • | • | • | • | • | |
| | • | • | • | • | • | |
| 4000+ | 00000 | 0 | 00001 | Block # | Data Block 1 | 0040 |
| 4000+ | 00000 | 0 | 00000 | Block # | Data Block 0 | 0000 |

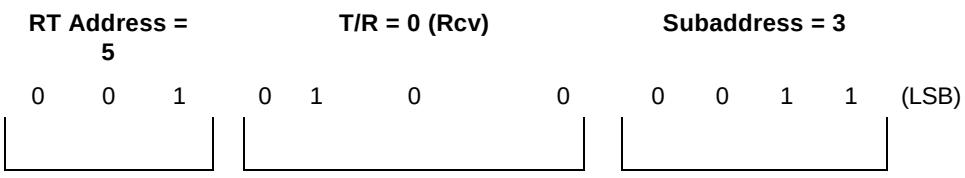
**Figure 4-2 Data Block Look-Up Table**

**NOTE** For RT-to-RT messages:
When the board is simulating both RTs in an RT-to-RT message transfer, the simulated receiving RT's data block is not updated with the transmit data. (The data is transmitted over the 1553 bus.)

TO CREATE THE ADDRESS TO THE TABLE

1. Isolate the eleven (most significant) bits of the 1553 command word (RT Address, T/R, and Subaddress field), and determine their hex value.

**Example** To allocate a data block for a 1553 receive message to RT#5, Subaddress 3.




Hex representation = 143 (H)



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2. Add the hex value of this part of the command word to the base address of the look-up table (4000H).

```
  4000   (H)
+ 143    (H)
-------
  4143   (H)
```

3. Write the data block number to this location.

**Example** `POKE &H4143, 01` allocates block #1 for the data of this message. Read the 1553 data out by reading block #1, which starts at address 0040 (H). Each data block, beginning at address 0000 is 64 bytes long (for up to 32 1553 data words). The address of a block is obtained by multiplying its block number by 64 (40 H).

### 4.2.1 Data Storage

The data words must be stored and/or read in the following format in the data block:

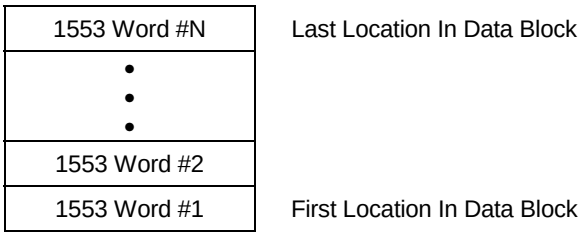


**Figure 4-3 Data Storage Sequence**

## 4.3 Active RT Table

**Address: 3200–321F (H)**

The 32 locations (bytes) of the Active RT table contain the list of active remote terminals. To select an RT to be simulated, set bit 00 in the Active Remote Terminal byte to logic 1. The first active RT byte relates to RT #0, the next to RT #1, and the last location relates to RT #31.

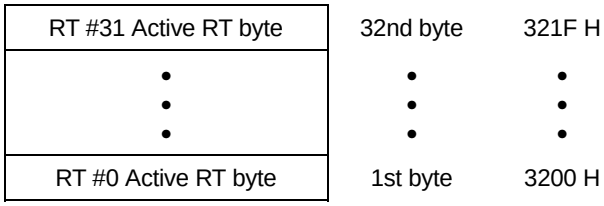


**Figure 4-4 Active RT Table: RT Mode**



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| Bit | Bit Name | Description |
|---|---|---|
| **04-07** | **0** | |
| **03** | **Inactive Bus B** | 1 = Bus B Inactive<br>0 = Bus B Active<br><br>If bit 00 is set to 1 and bit 03 is set to 0, the board will respond to all messages received over bus B for this RT; and the board will generate interrupts, if requested to do so.<br><br>If bit 03 is set to 1, all messages over bus B for this RT will be ignored, regardless of the settings of other bits in this register. |
| **02** | **Inactive Bus A** | 1 = Bus A Inactive<br>0 = Bus A Active<br><br>If bit 00 is set to 1 and bit 02 is set to 0, the board will respond to all messages received over bus A for this RT; and the board will generate interrupts, if requested to do so.<br><br>If bit 02 is set to 1, all messages over bus A for this RT will be ignored, regardless of the settings of other bits in this register. |
| **01** | **Interrupt** | 1 = Interrupt<br>0 = No Interrupt<br><br>If bit 01 is set to 1, the RT is active and the Interrupt Condition register is enabled, this RT will generate an interrupt. |
| **00** | **Active** | 1 = Active<br>0 = Inactive<br><br>If bit 00 is set to 0, the RT is not active. If it is set to 1, bits 01, 02, and 03 are checked. |

**Active RT Byte Definition: RT Mode**



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## 4.4 1553 RT Status Words

**Address: 3220-325F (H)**

These locations are reserved for the 32 1553 RT status words. Load the desired status words into their respective locations in the block. The first word relates to RT #0, the next word to RT #1, while the last word relates to RT #31.

For each RT that is to be simulated, all 16 bits of that RT must be defined in its status word.

In a non-1553B environment (see Status Response Register, page 4-21) the user-defined status word is sent whenever the RT has to respond with a status word.

In a 1553B environment (see Status Response Register, page 4-21), the same status word is sent with the following conditions:

**Message Error (Bit 10)** — In case an error occurred in the previous message, the Status Word will be sent with the Message Error bit set to 1 if the current message is of type Send Status or Send Last Command. This will occur even if you set the Message Error bit to 0.

If you set the Message Error bit to 1, it will always be sent set to 1.

**Busy (Bit 03)** — The Busy bit is always sent as you defined it. In the case of Transmit commands, when Busy is set to 1, no data words will be transmitted by the RT following the transmission of the status word.

The MIL-STD-1553B Format for the Status Word is as follows:

| Bit | Bit Name |
|---|---|
| **11-15** | RT Address |
| **10** | Message Error |
| **09** | Instrumentation |
| **08** | Service Request |
| **05-07** | Reserved |
| **04** | Broadcast |
| **03** | Busy |
| **02** | Subsystem Flag |
| **01** | Dynamic Bus |
| **00** | Terminal Flag |

**1553B Status Word**



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## 4.5 Message Stack

The board generates a message stack in the dual-port memory. This stack contains information that can be used for post-processing of RT messages. The stack is divided into 42 blocks, each containing three words. The stack operates as a circular buffer. The Message Stack Pointer points to the beginning of the (next) unused block. Only active RT messages are stored. Figure 4-5 illustrates one block.

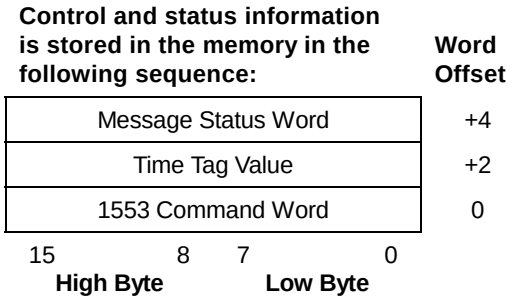


**Figure 4-5 Message Stack Block Structure**

### HOW THE BOARD UPDATES AN RT-TO-RT MESSAGE

When an RT-to-RT message is received, where the board is functioning as both RTs, the Message stack is updated as follows:

Two message stack blocks are utilized.

1. The 1553 Receive command word is written into the *first* message stack block.
2. The RT-RT bits in *both* message status words are set to 1.
3. The board updates the Time Tag word in the *second* stack block and the *second* Message Status word. The board updates only the RT-to-RT bit in the *first* Message Status word to Active status.
4. The 1553 Transmit command word is written into the *second* stack block.



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### 4.5.1 Message Status Word

The Message Status word indicates the status of the message transfer. This word is created by the board. Do not confuse this word with the 1553 Status word (see1553 RT Status Words page 4-7). The contents of the Message status word are described below.

**NOTE** A logic 1 indicates the occurrence of a status flag.

| Bit | Bit Name | Description |
|---|---|---|
| **15** | **End Of Message** | Message transfer completed |
| **14** | **Bus A / B** | Bus on which the message was transferred:<br>0 = Bus B<br>1 = Bus A |
| **11-13** | **Reserved** | Set to 0 |
| **10** | **Tx Time Out** | Board, acting as receiver in RT-to-RT message, did not sense a transmitter status word (in 14 µsec.) |
| **09** | **Reserved** | Set to 0 |
| **08** | **Reserved** | Set to 0 |
| **07** | **Invalid Word Received** | At least one invalid 1553 word received (i.e. bit count, Manchester code, parity) |
| **06** | **Reserved** | Set to 0 |
| **05** | **Word Count Error (Receive Message)** | Incorrect number of words received in the message |
| **04** | **Broadcast Message** | Broadcast command word received |
| **03** | **Incorrect Sync Received** | Sync of either the command or the data word(s) is incorrect |
| **02** | **Non - Contiguous Data (Receive Message)** | Invalid gap between received 1553 words |
| **01** | **RT-RT Message** | RT-to-RT message received where board was simulating both RTs |
| **00** | **Error** | Error occurred (The error type is defined in one of the other message status bit locations.) |

**Message Status Word**



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### 4.5.2 Time Tag

**READ BY USER**

The Time Tag value is a 16-bit word that can be used to determine the time elapsed since the Start command was issued or the time between 1553 messages. The Time Tag uses a 32-bit, free-running counter whose resolution is set by the Time Tag Resolution register. This register has a resolution of 4 µsec. per bit. The equation to determine the Time Tag resolution = (register value + 1) x 4 µsec. Note that only the lower 16 bits of the counter are written to dual-port RAM.

**Example**

Register value = 0 → Counter's resolution = 4 µsec

Register value = 4 → Counter's resolution = 20 µsec

To reset the Time Tag counter (to 0) any time, write to the Time Tag Reset Register (see Control Register Definitions," page 4-15).

When the first command of each message is received, the value of the 16 lower bits of the Time Tag Counter register, are written to dual-port RAM.

**NOTE** 1. The counter's value can be read any time by reading the Time Tag Counter addresses (see Control Register Definitions, page 4-15).

2. The counter can also be clocked and/or reset from an external source (see Connectors, page 9-5).

**Example** How To Calculate Elapsed Time

Time Tag Resolution register = 03 (initialized before Start command)

Time Tag values (read during or after message transfers):

Low = 40 (H)
High = 10 (H)

Time elapsed since Start command
= (Time Tag register value) x (Time Tag Resolution value + 1) x (4 µsec)
= 1040 (H) x (03 + 1) x 4 µsec
= 4160 (Dec) x (4 x 4 µsec) = 66560 µsec (66.56 msec.)

### 4.5.3 1553 Command Word

The command word location contains the 1553 command word associated with the message.

Only active RT 1553 command words are stored.



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### 4.5.4 RT-To-RT Messages

When the board is operating as both RTs in an RT-to-RT transfer:

- The board transmits both 1553 Status and Data words onto the bus.
- The board does *not* copy the Transmit data block into the Receiver data block area (pointed to by the look-up table pointer).

## 4.6 RT Last Command Words

**Address: 3400-343F (H)**

The Last command word locations are reserved for the (32) 1553 Last command words. The board writes to these locations at the end of each message transfer (for active RTs only). The first word is for RT #0, the next word is for RT #1, and the last word is for RT #31. These words are used for the implementation of the Transmit Last Command Word Mode code.

**NOTE** Only command words of valid messages containing no errors are recorded in this table.

## 4.7 1553 RT BIT Words

**Address: 3440-347F (H)**

The RT BIT word locations are reserved for the 32 1553 BIT words. Load the desired BIT words into the corresponding locations in the block. The first word is for RT #0, the next word is for RT #1, and the last word is for RT #31. These words are used to implement the Transmit BIT Word Mode code.

## 4.8 1553 RT Vector Words

**Address: 3480-34BF (H)**

The RT Vector Word locations are reserved for the 32 1553 Vector words. Load the desired Vector words into the corresponding locations in the block. The first word is for RT #0, the next word is for RT #1, and the last word is for RT #31. These words are used to implement the Transmit Vector word Mode code.



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## 4.9 Mode Codes

The user can program the Subaddress code that will indicate that a Mode command has been received. Either or both of the following codes can be used: 11111 and 00000. You must program the Mode Code Control register as described in Control Register Definitions, page 4-15.

The board handles all dual-redundant 1553B Mode codes. The Word Count field is decoded according to MIL-STD-1553B. One of the Mode codes (Synchronize with Data word) is operated upon as a standard message transfer, using the Data Block look-up table. When the board encounters the Synchronize with Data word Mode code, the command word's RT Address, T/R bit, and Subaddress fields are used as a pointer to the look-up table. The table entries that are addressed when the T/R bit = 0 and Subaddress = 00000 or 11111 should contain a Data Block number (0–199) indicating where the Synchronize with Data Word's data word should be stored.

The data associated with mode codes (Transmit Last Command, Transmit Bit word, and Transmit Vector word) is set using the dedicated blocks in the on-board memory (described in RT Last Command Words, 1553 RT BIT Words, and 1553 RT Vector Words, page 4-11).

## 4.10 Broadcast Mode

To operate the board in the broadcast environment, select the appropriate bit setting as defined in Options Select Register, page 4-16.

When operating in Broadcast mode, you must set the active RT look-up table entry for RT #31 as Not Active. The board reads the Options Select Register to determine whether the board is operating in Broadcast mode.

In Broadcast mode, the board stores the received message in a 1553 data block area in the same way as standard message formats. RT address, T/R bit, and Subaddress are used as a pointer to the Data Block look-up table memory.

**NOTE** When operating in Broadcast mode, the Broadcast bits in the 1553 Status Words are *not* updated by the board's processor.



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## 4.11 Error Injection Features

The board allows two types of error injection:

- Global (for all RTs)
- Per RT

The global errors such as Sync and Non-Contiguous data are described in Error Injection Register, page 4-20. These errors are either ON or OFF for all RTs. The ability to inject a 1553 Word Count error, however, can be set per RT.

### 4.11.1 Word Count Error Table

**Address: 32E0–32FF (H)**

The Word Count Error is selected by writing to the Word Count Error table, which contains 32 bytes (one per remote terminal). The first byte is for RT #0, the second to RT #1, and the last byte is for RT #31. The contents of each location controls the number of 1553 words (±3 words) in the message. The variation is an offset, relative to the 1553 command word's Word Count field. The resulting message (if an error is programmed) must contain at least one data word.

Upon power-up and software reset, the board sets the Word Count Error Table to the default value, 00.

You must set the Word Count Error register before issuing a Start command to the board. To modify the Word Count Error register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 4-18).

| | |
|---|---|
| RT #31 | 32FF H |
| • • • | |
| RT #1 | |
| RT #0 | 32E0 H |

**Figure 4-6 Word Count Error Table Addresses**

| Register Value | Word Count Offset |
|---|---|
| FD H | –3 Words |
| FE H | –2 Words |
| FF H | –1 Word |
| 00 H | No Error Injection |
| 01 H | +1 Word |
| 02 H | +2 Words |
| 03 H | +3 Words |

**Word Count Error Byte Values**



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## 4.12 Program Example: RT Mode

**NOTE** All values are in HEX unless otherwise stated.

| BASIC Instruction | Remarks |
|---|---|
| `10 POKE &H3FFF,02` | Set the Configuration register to RT mode. |
| `20 POKE &H3FF2,xx` | Set the Variable Amplitude register. |
| `30 POKE &H3201,1` | Enable RT #1. |
| `40 POKE &H3204,1` | Enable RT #4. |
| `50 POKE &H3222,00` | Set the Status word of RT #1 to 0800. |
| `60 POKE &H3223,08` | |
| `70 POKE &H3228,00` | Set the Status word of RT #4 to 2000. |
| `80 POKE &H3229,&H20` | |
| `90 POKE &H3FF7,xx` | Set the Time Tag Resolution register. |
| `100 POKE &H3266,00` | Set the Mode Code Control register to Subaddress 0 & 31. |
| `110 POKE &H3FF3,00` | Set No global error injection. |
| `120 POKE &H4xxx,1` | Load block number 1 for data storage into look-up table xxx. |
| `130 POKE &H4yyy,2` | Load block number 2 for data storage into look-up table yyy. |
| `140 POKE &H3FFC,1` | Set the Start register to 1 to start RT mode. |
| `150 STOP` | |



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## 4.13 Control Register Definitions

### 4.13.1 Time Tag Options Register

**Address: 700C (H) WRITE ONLY**

Set the Time Tag Options Register's 00 bit to select the current bank's Time Tag Counter Clock Source. After power-up or software reset, the Time Tag Options Register's bit 00 is set to 0. (i.e. Internal Clock Source).

For external Time Tag Clock source, see Communication I/O Signals Description of Connector JI, page 9-7.

| Bit | Description |
|---|---|
| 01-07 | Reserved |
| 00 | 0 = Internal Time Tag Clock<br>1 = External Time Tag Clock |

**Time Tag Options Register**

### 4.13.2 Time Tag Counter

**Address: 7008–700B (H) READ ONLY**

Read the two 16-bit words of the Time Tag counter to determine the current free-running, 32-bit Time Tag counter value. You may read the counter at any time.

The counter must be read in the following sequence:

1. Read 7008 H (16 bit, read only)
2. Read 700A H (16 bit, read only)

7008 H contains the lo word; 700A H contains the hi word. The Time Tag resolution register sets the resolution of the counter (Time Tag Resolution Register, page 4-18).

The counter is reset upon power-up, or software reset and stays reset until a Start command is issued. When a Start command is issued, the counter starts counting. To re-initialize to 0, write to the Time Tag Reset register. When it reaches the value FFFFFFFF (H), the counter wraps around to 0 and continues counting.

### 4.13.3 Time Tag Reset Register

**Address: 7007 (H) WRITE ONLY**

Write to the Time Tag Reset register to reset the channel's Time Tag Counter (data field = don't care). Immediately after the reset, the counter will start to count from 0.

**NOTE** The counter can also be reset from an external source (see Connectors page 9-5).



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### 4.13.4 Options Select Register

**Address: 7003 (H)**

Write to the Options Select register to select whether RT address 11111 (RT 31) is interpreted as a valid RT address or as a Broadcast address.

| Bit | Description |
|---|---|
| **01–07** | 0 |
| **00** | 1 = Broadcast option is active. RT #31 is a Broadcast Address. No RT Status Word will be transmitted.<br>0 = Broadcast option is inactive. RT #31 is a Regular RT. |

**Options Select Register**

### 4.13.5 Global Software Reset Register

**Address: 7002 (H)**

Write to the Global Software Reset register to reset all channels present on the board, simultaneously (data field = don't care).

**NOTE** Global Software Reset erases all locations in dual-port RAM. Board status, Board ID, and Firmware Revision are written by the board after the reset operation is completed.

### 4.13.6 Interrupt Reset Register

**Address: 7001 (H)**

To reset the Interrupt signal generated by the channel, write to the Interrupt Reset register at the beginning of a user-written interrupt service routine (data field = don't care).

### 4.13.7 Software Reset Register

**Address: 7000 (H)**

Write to the Software Reset register to reset the channel (data field = don't care). The Board status, the Board ID, Firmware revision are written by the board after the reset operation has been completed.

**WARNING** *Reset erases all memory locations in the dual-port RAM.*



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### 4.13.8 Board Configuration Register

**Address: 3FFF (H)**

Use the Board configuration register to set the operating mode of the board.

You must set the Board Configuration register before issuing a Start command to the board. To modify the Board Configuration register, issue a Stop command, modify the register, then issue a Start command (see Start Register,page 4-18).

| Hex Value | Operating Mode |
|---|---|
| **02** | RT Mode |

**Board Configuration Register Value: RT Mode**

### 4.13.9 Board ID Register

**Address: 3FFE (H)**

The Board ID register contains a fixed value that can be read by your initialization routine to detect the presence of the board. The one-byte value of this register is: 45 (Hex), ASCII value “E”.

### 4.13.10 Board Status Register

**Address: 3FFD (H)**

The Board Status register indicates the status of the board. In addition, this register indicates which options have been selected. Do not modify this register. Status bits are active if set to 1.

| Bit | Description |
|---|---|
| **07** | 1 = Board Type is EXC-1553PCI/Px |
| **06** | X (Don’t Care) |
| **05** | X (Don’t Care) |
| **04** | 1 = Board Halted<br>0 = Board Running |
| **03** | 1 = Self-Test OK |
| **02** | 1 = Timers OK |
| **01** | 1 = RAM OK |
| **00** | 1 = Board Ready |

**Board Status Register**

**NOTE** Board operation stops after you clear the Start bit in the Start Register. Following this, the board sets bit 04 (Board Halted). Certain registers may be modified only after the Board Halted bit has been set. After receiving a subsequent Start command (by writing to the Start register), the board resets the Board Halted bit. The condition of this bit after power-up or software reset is logic 1.



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### 4.13.11 Start Register

**Address: 3FFC (H)**

The Start register controls the Start/Stop operation of the board. The user can Start, then Stop the RT operation, modify RT parameters (example: the Error Injection register or Response Time), and then issue a new Start command in real time.

For more information about Bit 04 (Board Halted/Running) in the Board Status Register, see the note in Board Status Register.

| Bit | Description |
|---|---|
| **01-07** | 0 |
| **00** | 1 = Start Operation<br>0 = Stop |

**Start Register**

**NOTE** To start, send a low TTL pulse of 100 nsec minimum to the EXSTART*x*n pin (see Connectors, page 9-5).

### 4.13.12 Message Status Register

**Address: 3FFB (H)**

The Message Status register indicates that a 1553 message has been received. A logic 1 indicates active condition. This bit is also set for messages with errors.

| Bit | Description |
|---|---|
| **01-07** | 0 |
| **00** | Message Complete |

**Message Status Register**

**NOTE** After reading, reset the Message Complete bit; the board does not reset this bit.

### 4.13.13 Time Tag Resolution Register

**Address: 3FF7 (H)**

The 8-bit value in the Time Tag Resolution register represents the resolution of the Time Tag Counter in units of 4 µsec.

To determine the Time Tag Counter's Resolution, use the following equation:

= (Time Tag Resolution register value + 1) x 4 µsec.

A value of 0 corresponds to a resolution of 4 microseconds; a value of 1 corresponds to a resolution of 8 microseconds, etc.

The user must set the Time Tag Resolution register before issuing a Start command to the board. To modify the Time Tag Resolution register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 4-18).



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### 4.13.14 RT Response Time Register

**Address: 3FF4 (H)**

The RT Response Time register sets the Response Time of the Remote Terminal. The resolution of the Response Time register is 155 nsec per bit, measured as the dead time on the 1553 bus. The minimum time is approximately 4 µsec., which is achieved by writing a 0 to this register. Any value above zero will result in a Response Time equal to 4 µsec. plus the contents of the register x 155 nsec. The actual response time has a tolerance of ± 1 µsec.

Set the Response Time register before issuing a Start command to the board. To modify the Response Time register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 4-18).

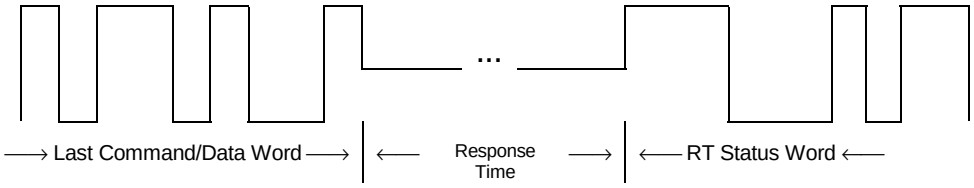


**Figure 4-7 RT Response Time Definition**

**Example** Setting the RT Response Time Register

To request a response time of 9 µsec:

Write 32 to the RT Response Time register.

[32 x 0.155 ≅ 5 µsec] + 4 µsec = 9 µsec



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### 4.13.15 Error Injection Register

**Address: 3FF3 (H)**

The Error Injection Register is a global register that allows you to select the type of error to be injected in a transmitted message. When the board receives a Start command (issued by writing to the Start register), the board reads this register.

To modify the Error Injection register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 4-18).

| Bit | Description |
|---|---|
| **07** | Data Word Sync Error (Data Words Sent With Command Sync) |
| **06** | Reserved (Set to 0) |
| **05** | Status Word Synchronization Error (Status Word Sent With Data Sync) |
| **04** | Reserved (Set to 0) |
| **03** | Reserved (Set to 0) |
| **02** | Non-Contiguous Data (Between First and Second Data Word) |
| **01** | Reserved (Set to 0) |
| **00** | Reserved (Set to 0) |

**Error Injection Register**

### 4.13.16 Message Stack Pointer

**Address: 3FF0–3FF1 (H)**

The Message Stack pointer indicates the Message Stack position. After the entire message is received, the Message Stack pointer is updated (incremented by 6). This word is initialized to 3300 (H) and circulates in the Message Stack between 3300 (H) to 33F6 (H).



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### 4.13.17 Status Response Register

**Address: 3FEF (H)**

The Status Response register is used to control the Status Response mode of operation.

After a Receive message, the user can respond with a 1553 Status word even if an invalid 1553 Data word was received. A 1553 environment can be selected which will affect some 1553 RT Status word bits (see1553 RT Status Words, page 4-7).

Set the Status Response register before issuing a Start command to the board. To modify the Status Response register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 4-18).

| Bit | Description |
|---|---|
| **02–07** | 0 |
| **01** | Environment:<br>0 = 1553B<br>1 = Non-1553B |
| **00** | On Error:<br>0 = Suppress Status<br>1 = Send Status |

**Status Response Register**

### 4.13.18 Board Options Register

**Address: 3E84 (H) READ ONLY**

The Board Options Register is a 16-bit register in which the low 8 bits are reserved. This register identifies the type of on-board firmware.

| Bit | Description |
|---|---|
| **10-15** | Reserved |
| **09** | 1 = 1760 |
| **08** | 1 = 1553 |
| **00-07** | Reserved |

**Board Options Register**

### 4.13.19 Firmware Revision Register

**Address: 3E80 (H)**

The Firmware Revision register indicates the revision level of the on-board firmware. The value 0001 0010 would be read as revision level = 1.2.



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### 4.13.20 Interrupt Condition Register

**Address: 33FC (H)**

The Interrupt Condition register allows you to enable an interrupt trigger. The Message Complete bit works in conjunction with the Interrupt bit in the Active RT table. When a message is received by an RT for which the Active RT interrupt bit is set, the board will check the Message Complete bit. If this bit is also set, an interrupt will be generated.

Set the Interrupt Condition register before issuing a Start command to the board. To modify the Interrupt Condition register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 4-18).

| Bit | Description |
|---|---|
| **02-07** | 0 |
| **01** | Message Complete |
| **00** | 0 |

**Interrupt Condition Register**

### 4.13.21 Mode Code Control Register

**Address: 3266 (H)**

The Mode Code Control register allows you to specify which 1553 Subaddress value indicates the reception of a 1553 Mode command.

Set the Mode Code Control register before issuing a Start command to the board. To modify the Mode Code Control register, issue a Stop command, modify the register, then issue a Start command (see Start Register, page 4-18).

| Bit | Description | | |
|---|---|---|---|
| **02-07** | 0 | | |
| **00-01** | **Bit 01** | **Bit 00** | **Subaddresses Recognized as Mode Code** |
| | 0 | 0 | 31 and 0 |
| | 0 | 1 | 0 |
| | 1 | 0 | 31 |
| | 1 | 1 | 0 and 31 |

**Mode Code Control Register**



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# 5 BC/Concurrent-RT Operation

Chapter 5 describes EXC-1553PCI/P*x* operation in Bus Controller/Concurrent-Remote Terminal mode. The information in this chapter applies to all 1553 channels present on the board. All addresses referred to in this chapter are offset from the base address of the channel accessed (see Base Address Registers, page 2-7).

The following topics are covered:



The EXC-1553PCI/P*x* can simultaneously operate as the bus controller and up to 32 Remote Terminals. The messages and the instruction stack are loaded as for BC operation.

In Concurrent-RT mode, load message blocks with the RT's 1553 Status and Data words for those Remote Terminals that you are actively simulating. These words must be loaded into the appropriate locations in the message blocks in the sequence that the 1553 words appear on the 1553 bus.

**NOTE** The requirement for loading the message blocks only applies to RTs that you are actively simulating. For RTs that are not active (not simulated by the board), leave the corresponding locations blank in the associated 1553 message blocks.

The Remote Terminals simulated in BC/Concurrent-RT mode have a minimum response time of approximately 4 µsec.



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TO DETERMINE WHETHER THE BOARD IS INSTALLED AND READY TO OPERATE, perform the following procedure after a power-up or a software reset.

1. Check the Board ID register (test for value = 45 H).
2. Check the Board Status register (test for Board Ready bit = 1).

The board is installed and ready when both registers contain the correct values (as written above). For software reset operations, set these values to 0 immediately prior to writing to the (software) Board Reset register.

**NOTE** Throughout this manual, writing a 1 to the Start register is referred to as “issuing a Start command.”



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## 5.1 BC/Concurrent-RT Memory Map

Figure 5-1 below illustrates the BC/Concurrent-RT memory usage.

| | | | |
|---|---|---|---|
| Reserved | 7004 - 7FFF H | | |
| Options Select Register | 7003 H | | |
| Global Software Reset Register | 7002 H | | |
| Interrupt Reset Register | 7001 H | | |
| Software Reset Register | 7000 H | | |
| Reserved | 4000 - 6FFF H | | |
| Board Configuration Register | 3FFF H | Frame Time Resolution Register | 3FEC - 3FED H |
| Board ID Register | 3FFE H | Instruction Counter | 3FEA - 3FEB H |
| Board Status Register | 3FFD H | Minor Frame Time | 3FE8 H |
| Start Register | 3FFC H | Reserved | 3FE7 H |
| Interrupt Condition Register | 3FFB H | Minor Frame Resolution | 3FE6 H |
| Message Status Register | 3FFA H | Reserved | 3E86 – 3FE5 H |
| RT Response Time Register | 3FF9 H | Boards Option Register | 3E84 H |
| Reserved | 3FF7 - 3FF8 H | Reserved | 3E81 - 3F83 H |
| Loop Count Register | 3FF6 H | Firmware Revision Register | 3E80 H |
| Bit Count | 3FF5 H | Reserved | 3426 - 3E7F H |
| Word Count Register | 3FF4 H | Asynchronous Start Flag | 3424 H |
| BC Response Time Register | 3FF3 H | Asynchronous Frame Pointer | 3422 H |
| Reserved | 3FF2 H | Asynchronous Message Counter | 3420 H |
| Stack Pointer | 3FF0 - 3FF1 H | Active RT Table (32 Bytes) | 3400 - 341FH |
| Frame Time Register | 3FEE - 3FEF H | Instruction and Message Block Area | 0000 - 33FF H |

**Figure 5-1 BC/Concurrent-RT Memory Map**



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## 5.2 Instruction Stack

Use the Instruction Stack to program the board. The stack is divided into instruction blocks, each containing four words. The block contains control information (that the user writes) and status information (that the board writes). Figure 5-2 illustrates one instruction block.

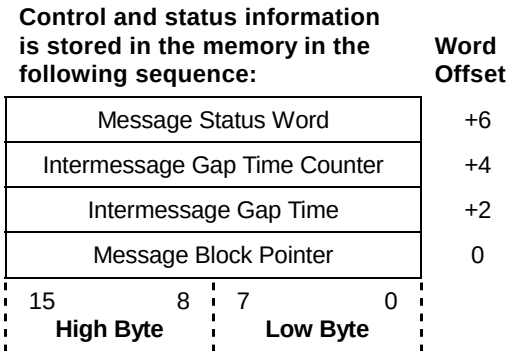


**Figure 5-2 Instruction Block Structure: BC/Concurrent-RT Mode**



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### 5.2.1 Message Status Word

The Message Status word indicates the status of the message transfer. This word is created by the board. Do not confuse this word with the 1553 Status word (see 1553 RT Status Words, page 4-7). The contents of the Message status word are described below.

**NOTE** A logic 1 indicates occurrence of status flag.

| Bit | Bit Name | Description |
|---|---|---|
| **15** | **End Of Message** | Message transfer completed |
| **14** | **Reserved** | Set to 0 |
| **13** | **Incorrect 1553 Bus** | Remote Terminal response was not received on the active 1553 bus. |
| **12** | **Message Error Bit Set** | Message Error bit (bit 10) in the RT Status word was set. |
| **11** | **RT Status Bit Set** | A bit was set in the RT Status word (other than the Message Error bit). The error bit is not set in conjunction with this bit. |
| **10** | **Invalid Message Error** | A 1553 message-level error occurred (e.g. Word count, incorrect sync); details in the bits described below. |
| **09** | **Response Time Failure** | RT responded late (see BC Response Time Register, page 5-26). |
| **08** | **Reserved** | Set to 0 |
| **07** | **Invalid Word Received** | At least one invalid 1553 word received (e.g., bit count, Manchester code, parity). |
| **06** | **Word Count High** | RT transmitted too many words. |
| **05** | **Word Count Low** | RT transmitted too few words. |
| **04** | **Incorrect RT Address** | 1553 Status word received did not contain the correct RT address. |
| **03** | **Incorrect Sync Received** | Sync of either the status or data word(s) is incorrect. |
| **02** | **Non-Contiguous Data** | Invalid gap between received 1553 words. |
| **01** | **Reserved** | Set to 0 |
| **00** | **Error** | Error occurred. (The error type is defined in one of the other message status bit locations.) |

**Message Status Word**



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### 5.2.2 Intermessage Gap Time

The Intermessage Gap Time value is a 16-bit word that you write that allows you to insert a unique intermessage delay time between the current message and the next message. The minimum Intermessage Gap Time is approximately 4 µsec measured as dead time on the bus. The value in the word is added to this minimum time. The resolution of this word is 155 nsec per bit.

### 5.2.3 Intermessage Gap Time Counter

The Intermessage Gap Time counter (IGT_counter) is a 16-bit word that you write that allows you to increase the Intermessage Gap Time by repeating the number of times the Intermessage Gap Time value is used. For example, if the counter is set to 0, then the gap time is not repeated; and depends on the contents of the Intermessage Gap Time location. If the gap time counter is 1 then the gap time is repeated once and equals the Intermessage Gap Time value × 2, etc.

**NOTE** To ensure maximum Intermessage Gap Time accuracy when using the IGT_counter, use the largest possible value for the Intermessage Gap Time word and the smallest value for the IGT_counter, for a given desired intermessage gap time.

### 5.2.4 Message Block Pointer

The Message Block pointer is a 16-bit word that you write that points to the beginning of a 1553 message block.

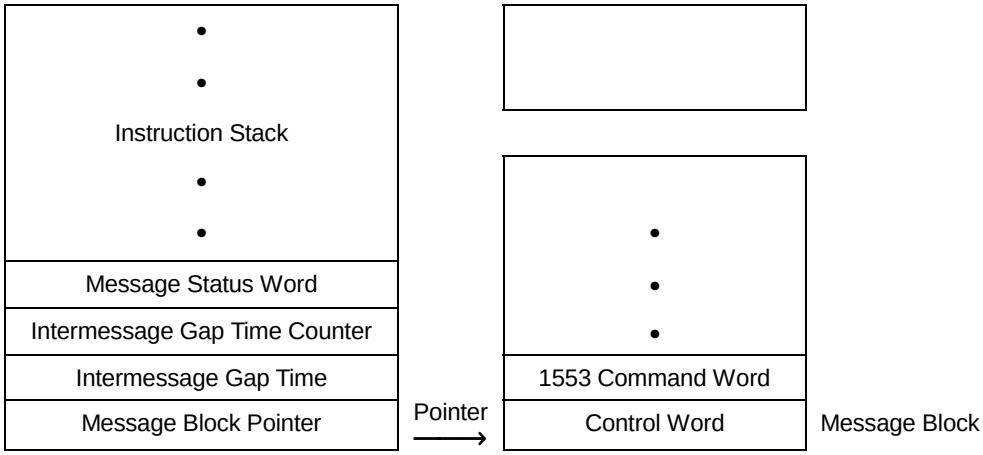


**Figure 5-3 Message Block Pointer: BC/Concurrent: RT Mode**



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### 5.2.5 Message Block

The load the message block can be loaded anywhere in the Instruction Stack/Message Block area (see BC/Concurrent-RT Memory Map, page 5-3). Message blocks do not have to be stored in sequential locations in the memory since the Message Block pointers “point” to the message blocks in sequence.

Each block contains a 1553 message plus its Control word. This Control word is written into the first word of each block. The Control word instructs the board which type of message to transmit (i.e., RT to RT, Mode code, Broadcast, Error injection, etc.). The size of the message block is variable and depends on the size of the message itself.

The descriptions of the various message block formats (i.e., BC to RT, RT to BC and RT to RT) are illustrated in Message Block Formats, page 5-13.

The description of each bit in the Control word follows.



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### 5.2.6 Control Word

**NOTE** Logic 1 enables the function; 0 disables the function.

| Bit | Bit Name | Description |
|---|---|---|
| **15** | **Stop On Error** | Message error stops BC operation. Restart by writing to the Instruction Count register and issuing a Start command. |
| **14** | **Even Parity** | Selects Even parity in 1553 Word |
| **13** | **Halt/Continue** | 1 = Halt; stops BC transfer operation. This bit must be reset to 0 to Run or Continue. |
| **12** | **Word Count Error** | Transmits fewer or more words than are indicated by the Word Count field (see Word Count Register, page 5-25). This function is valid for BC to RT messages only. |
| **11** | **Bit Count Error** | Transmits invalid number of bits in 1553 words (see Bit Count Register, page 5-24. |
| **10** | **Incorrect Sync** | Transmits incorrect sync. Data type Sync is transmitted in the Command word. |
| **09** | **Non-Contiguous Data** | Transmits the first 1553 Data word with invalid Gap Time (between Command and Data word). |
| **08** | **Error Placement/ Error Injection Enable** | For BC-to-RT, Broadcast Receive, and Mode Code with Data messages, bit 08 selects the Parity, Sync and Bit Count error injection placement:<br>0 in Command word<br>1 in Data words<br>For other error injection types or other message types, this bit must be set (=1) to enable error injection. |
| **07** | **Bus A/B** | Selects active 1553 bus: logic 1 selects bus A; logic 0 selects bus B. |
| **06** | **Auto Bus Switch** | On error, the BC will retry message transfer on alternate bus. (Note: Auto-retry must be selected.) |
| **04-05** | **Auto Retry Code** | On error, selects the number of retries before transferring the next message: |

| Bit 05 | Bit 04 | Description |
|---|---|---|
| 0 | 0 | No Retry |
| 0 | 1 | 1 Retry |
| 1 | 0 | 2 Retries |
| 1 | 1 | 3 Retries |

**00-03 Command Code**

| 03 | 02 | 01 | 00 | Description |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Transmit command (RT to BC) |
| 0 | 0 | 0 | 1 | Receive command (BC to RT) |
| 0 | 0 | 1 | 0 | RT-to-RT command |
| 0 | 0 | 1 | 1 | Mode code |
| 0 | 1 | 0 | 0 | Broadcast Receive command |
| 0 | 1 | 0 | 1 | Broadcast RT-to-RT command |
| 0 | 1 | 1 | 0 | Broadcast Mode code |
| 0 | 1 | 1 | 1 | Skip Message (see Skip Message Operation, page 5-9) |
| 1 | 0 | 0 | 0 | Jump command (see Jump Command Operation, page 5-9) |
| 1 | 1 | 1 | 1 | Minor Frame Command (see Minor Frame Operation, page 5-10). |

**BC/RT Control Word**



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### 5.2.7 Halt Operation

Normally set the Halt Operation bit to logic 0 before writing to the Start register. In real-time (during BC execution), y set this bit to logic 1. When operating on that particular message block's Control word, the board will halt transfer operations until the bit is reset to logic 0.

When the board detects that the Halt bit is set, it sets the Wait For Continue bit in the Message Status register (see Control Register Definitions, page 5-18). Use the Wait For Continue bit to find out when the board has arrived at the halted instruction block. When the board detects that you have reset the Halt bit (Continue Mode), the board will reset the Wait For Continue bit in the Message Status Register and continue BC operation.

The Halt operation can be implemented only in message blocks that have *not* (as yet) been executed by the board.

**NOTE** The Halt operation can be used in conjunction with the Jump command described below (see Jump Command Operation page 5-9).

### 5.2.8 Skip Message Operation

The Skip Message command allows you to skip a message defined in a certain message block. All you have to do is modify the Command field in the Control word. This lets you selectively send a message in the current frame. The "skip" takes place immediately and does not wait until the Intermessage Gap Time expires.

### 5.2.9 Jump Command Operation

Modify the board's BC transfer cycle by setting the Jump command in the BC Control word. The Jump command instructs the board to operate on a new instruction stack or new stack entry in the same stack. This Control word is followed by a Stack Pointer word instead of the usual 1553 command word. In addition, the stack pointer is followed by an Instruction Count value. The Jump command is tested *after* the board has tested the Halt/Continue bit in the Control word. The "jump" takes place immediately and does not wait until the Intermessage Gap Time expires.



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The memory structure of the jump command is illustrated below.

| | | |
|---|---|---|
| Don't Care | Instruction Count | Third Word |
| Stack Pointer | | Second Word |
| Control Word | | First Word |

**Jump Command Memory Structure**

### 5.2.10 Minor Frame Operation

The Minor Frame type of message is used in the following ways:

- To function as a "delay time" message between groups of messages.
- To produce a list of messages that will be sent out over the bus at different frequencies.

Minor frame time is defined as the time elapsed from the beginning of a minor frame to beginning of the next minor frame. To set up minor frame operation, you must begin each minor frame with a minor frame command (see Minor Frame Time Register and Minor Frame Resolution Register, page 5-28). The maximum value possible for the Minor Frame Time is 16 sec.

The example in Figure 5-4 shows a configuration of four minor frames, in which Message A is sent in every frame, Message B is sent in every other frame, and Message C is sent once. Each minor frame goes out at 10 msec (100Hz). If each minor frame is 10 msec long, Message A is sent every 10 msec, Message B is sent every 20 msec, and Message C is sent every 40 msec.

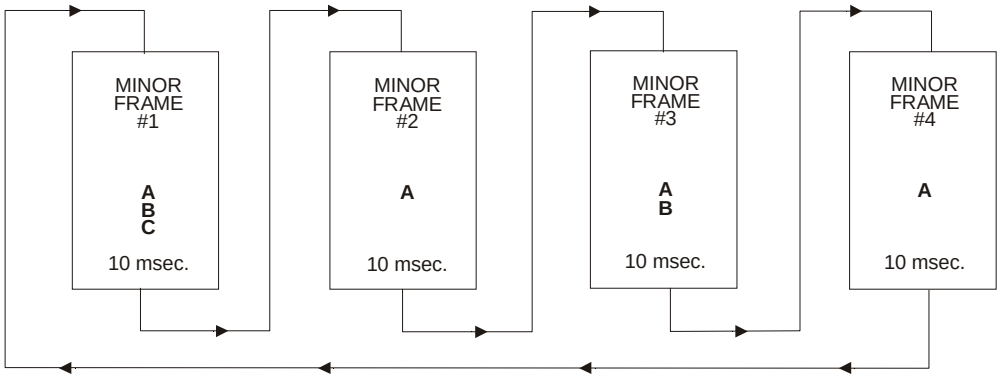


**Figure 5-4 Minor Frame Sequencing**

**NOTE** 1. The MINOR_FRAME message does not appear as a real message on the data bus.

2. Frame Time should not exceed the total time of all the minor frames in the minor frame sequence (see Frame Time Register, page 5-27).



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### 5.2.11 Asynchronous Frame Operation

During standard operation, the board sets up a frame of messages and then sends them out synchronously over the bus. Set up multiple frames of messages, and select which one to send out.

Asynchronous Frame operation allows you to transmit a frame asynchronously, meaning that in the middle of the transmission of the messages of a frame (frame 1), Transmit another frame (frame 2), and then return to continue transmitting the messages of the previous frame (frame 1).

To transmit an asynchronous frame, you must write the number of messages in the asynchronous frame into the Asynchronous Message Count register, place a pointer to the beginning of the asynchronous frame in the Asynchronous Frame Pointer register, and then set the Asynchronous Start Flag register to a non-zero value. This will send out the asynchronous frame over the bus (see Asynchronous Start Flag Register, Asynchronous Frame Pointer Register, Asynchronous Message Count Register page 5-29).



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## 5.3 Remote Terminal Simulation

When the board is simulating both the Bus Controller and one or more Remote Terminals, you must write the simulated Remote Terminal 1553 Status word and Data word(s) into the message block in the sequence in which they are to be transmitted over the 1553 bus (see Message Block Formats, page 5-13).

To indicate to the board that Remote Terminals are to be simulated, write to the 32- byte Active Remote Terminal table. Each entry in the 32-byte table corresponds to a specific Remote Terminal.

The first byte is for RT #0, the second to RT #1, and the last byte is for RT #31 (for a total of 32 locations). A table entry value of 1 enables the Remote Terminal simulation by the board; a value of 0 disables the simulation by the board.

| | |
|---|---|
| RT #31 Active RT byte | 341F H |
| RT #30 Active RT byte | |
| • • • | |
| RT #0 Active RT byte | 3400 H |

**Figure 5-5 Active RT Table: BC/Concurrent: RT Mode**

| Bit | Description |
|---|---|
| **01-07** | 0 |
| **00** | 1 = Enabled;<br>0 = Disabled |

**Active RT Byte Definition: BC/Concurrent-RT Mode**



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## 5.4 Message Block Formats

The Message block contains, or will contain after response from an RT, the entire 1553 message as it appears on the 1553 bus, including Command word(s), Data word(s), and Status word(s).

Examples of Message block formats follow.

**Example No. 1: Transmit Command Operating as BC Only**

**Block *before* execution**

| | |
|---|---|
| | |
| | |
| | |
| 1553 Transmit Command | |
| Control Word | First Location In Block |

**Block *after* execution**

| | |
|---|---|
| 1553 Data Word | From Transmitting Remote Terminal (Not Simulated) |
| • | • |
| • | • |
| 1553 Data Word | • |
| RT Status Word | From Transmitting Remote Terminal (Not Simulated) |
| 1553 Transmit Command | |
| Control Word | First Location In Block |



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**Example No. 2: Receive Command Operating as Both BC and Receiving RT**

**Block *before* execution**

| | |
|---|---|
| RT Status Word | Simulated By EXC-1553PCI/Px (Loaded by User) |
| 1553 Data Word | • |
| • | • |
| • | • |
| 1553 Data Word | Simulated By EXC-1553PCI/Px (Loaded by User) |
| 1553 Receive Command | |
| Control Word | First Location In Block |

**Block *after* execution**

| | |
|---|---|
| RT Status Word | |
| 1553 Data Word | |
| • | |
| • | |
| 1553 Data Word | |
| 1553 Receive Command | |
| Control Word | First Location In Block |



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**Example No. 3: RT-to-RT Command Operating as BC and Receiving RT**

**Block *before* execution**

| | |
|---|---|
| (Receive) RT Status Word | Simulated By EXC-1553PCI/Px (Loaded By User) |
| Leave Empty For Data +N | |
| • | |
| • | |
| Leave Empty For Data #1 | |
| Leave Empty For (Transmit) RT Status Word | |
| 1553 Transmit Command | |
| 1553 Receive Command | |
| Control Word | First Location In Block |

**Block *after* execution**

| | |
|---|---|
| (Receive) RT Status Word | |
| 1553 Data Word | From Transmitting Remote Terminal (Not Simulated) |
| • | • |
| • | • |
| 1553 Data Word | • |
| (Transmit) RT Status Word | From Transmitting Remote Terminal (Not Simulated) |
| 1553 Transmit Command | |
| 1553 Receive Command | |
| Control Word | First Location In Block |

## 5.5 Continuous or One-Shot Message Transfers

The board can transfer all programmed messages once, in a continuous loop, or for *n* number of times.

In One-Shot mode, (after receiving a Start command) the board transfers all messages, sets the Message Complete bit in the Message Status register, issues an interrupt (if programmed), and waits for a new Start command. Use the Start register (see Start Register, page 5-21) to select One-Shot mode.

In *n*-Times mode, load the Loop Count register with the number of times to transmit the messages (frame) and set the Loop and Start bits in the Start register. Transmit 1–255 times (see Start Register, page 5-21 and Loop Count Register, page 5-23). The time between frames is determined by the Frame Time register (see Frame Time Register, page 5-27).



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In Continuous Loop mode, the board will retransmit the message frame at a predetermined, user-programmable rate. Use the Start Register and the Loop Count Register (see Start Register, page 5-21 and Loop Count Register, page 5-23) to select Continuous Loop mode. In Continuous Loop mode, all messages relating to the (active) Stack pointer and Instruction counter are continuously looped until you halt the board's operation (see Start Register, page 5-21).

The Loop Time or Frame Time is a function of two control register pairs: the Frame Time registers (high and low) and the Frame Time Resolution registers (high and low). The internal Frame Time counter is loaded when a Start command with the 16-bit value found in the Frame Time registers (high and low) is received. The Frame Time counter is decremented every *n* x 155 nsec, where *n* is the value of Frame Time Resolution registers (high and low). After all instructions are executed (1 frame), the board waits until the internal Frame Time counter reaches 0 before transmitting the next frame.

**NOTE** If the Frame Time is less than the time required to transmit all messages within 1 frame, the subsequent frames will be transmitted with the minimum delay between them. The minimum delay is approximately 20 µsec, measured as dead time on the bus.

To implement the desired Frame Time, program the appropriate combinations of the two register pairs. An example is described below.

**Example** Calculating Frame Time

**Given:** Frame Time of 500 msec is required.

**Method:**

Select Frame Time Resolution of 3225 (Dec) → 0C99 (H)

Frame Time Resolution = 3225 x 155 nsec = 500 µsec (.5 msec)

Subsequently, the Frame Time register value must be equal to:

$$\frac{[500\ \text{msec (desired time)} \ /\ .5\ \text{msec} = 1000\ \text{(Dec)}] - 1}{\text{Count} - 1} \rightarrow 03E7\ \text{(H)}$$

Before issuing the Start command, set:

- Frame Time register low = E7 (H)
- Frame Time register high = 03
- Frame Time Resolution register low = 99 (Hex)
- Frame Time Resolution register high = 0C



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### 5.5.1 Mode Codes

The board handles all dual-redundant 1553B Mode codes; the Word Count field is decoded according to MIL-STD-1553B. The two Quad-Redundant Mode codes, Selected Transmitter Shutdown and Override Selected Transmitter Shutdown, are not implemented by the board.

## 5.6 Program Example: BC/Concurrent-RT Mode

**NOTE** All values are in HEX unless otherwise stated.

| BASIC Instruction | Remarks |
|---|---|
| `10 POKE &H3FFF,04` | Set the Configuration register to BC/RT mode. |
| `20 POKE &H3FF0,00` | Set the Stack Pointer registers to 0000. |
| `30 POKE &H3FF1,00` | (stack now begins at address: 0000) |
| `40 POKE &H3FF2,&HFF` | Set the Variable Amplitude register. |
| `50 POKE &H00,00` | Pointer to first message: |
| `60 POKE &H01,01` | [Location of message is 0100 (H)] |
| `70 POKE &H02,xx` | Set the Intermessage Gap Time location. |
| `80 POKE &H03,xx` | |
| `90 POKE &H08,&H40` | Pointer to second message: |
| `100 POKE &H09,01` | [Location of message is 0140 (H)] |
| `110 POKE &H0A,xx` | Set the Intermessage Gap Time location. |
| `120 POKE &H0B,xx` | |
| `130 POKE &H100,&H80` | Set the Control word to Transmit command, |
| `140 POKE &H101,00` | Bus A, and no errors injected. |
| `150 POKE &H102,&H23` | Set the command word to 0C23. |
| `160 POKE &H103,&H0C` | |
| `170 POKE &H104,&H00` | Set the Status word to 0800. |
| `180 POKE &H105,&H08` | |
| `190 POKE &H106,&Hxx` | Set the Data word to xxxx. |
| `200 POKE &H107,&Hxx` | |
| `210 POKE &H108,&Hyy` | Set the Data word to yyyy. |
| `220 POKE &H109,&Hyy` | |
| `230 POKE &H10a,&Hzz` | Set the Data word to zzzz. |
| `240 POKE &H10b,&Hzz` | |
| `250 POKE &H140,02` | Set the Control word to RT-to-RT command, |
| `260 POKE &H141,00` | Bus B, and no errors injected. |
| `270 POKE &H142,&H23` | Set the first (Receive) command word to 3823H. |



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| BASIC Instruction | Remarks |
|---|---|
| `280 POKE &H143,&H38` | |
| `290 POKE &H144,&H43` | Set the second (Transmit) command word to 1C43H. |
| `300 POKE &H145,&H1C` | |
| `310 POKE &H3FEB,2` | Set the Instruction Counter to 2 (i.e., 2 messages) |
| `320 POKE &H3FEC,xx` | Set the Frame Time Resolution registers. |
| `330 POKE &H3FED,xx` | |
| `340 POKE &H3FEE,xx` | Set the Frame Time registers |
| `350 POKE &H3FEF,XX` | |
| `360 POKE &H3401,1` | Enable RT #1. Use the Active RT's look-up table to enable RTs. Board will simulate enabled RTs. |
| `370 POKE &H3FFC,1` | Set the Start register to 1. Starts message transfers in One-Shot mode. |
| `380 STOP` | |

## 5.7 Control Register Definitions

### 5.7.1 Options Select Register **Address: 7003 (H)**

Write to the Options Select register to select whether RT address 11111 (RT 31) is interpreted as a valid RT address or as a Broadcast address.

| Bit | Description |
|---|---|
| **01–07** | 0 |
| **00** | 1 = Broadcast option is active. RT #31 is a Broadcast Address. No RT Status word will be transmitted.<br>0 = Broadcast option is inactive. RT #31 is a Regular RT. |

**Options Select Register**

### 5.7.2 Global Software Reset Register **Address: 7002 (H)**

Write to the Global Software Reset register to reset all channels present on the board, simultaneously (data field = don't care).

**NOTE** Global Software Reset erases all locations in dual-port RAM. Board status, Board ID, and Firmware Revision registers are written by the board after the reset operation is completed.



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### 5.7.3 Interrupt Reset Register

**Address: 7001 (H)**

To reset the Interrupt signal generated by the channel, write to the Interrupt Reset register at the beginning of a user-written interrupt service routine (data field = don't care).

### 5.7.4 Software Reset Register

**Address: 7000 (H)**

Write to the Software Reset register to reset the channel (data field = don't care). The Board status, the Board ID, and Firmware revision registers are written by the board after the reset operation has been completed.

**WARNING** *Reset erases all memory locations in the dual-port RAM.*

### 5.7.5 Board Configuration Register

**Address: 3FFF (H)**

Before issuing a Start command to the board, set the operating mode of the board via the Board Configuration register. To modify the Board Configuration register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 5-21).

| Hex Value | Operating Mode |
|---|---|
| **04** | BC/Concurrent-RT |

**Board Configuration Register Value: BC/RT Mode**

### 5.7.6 Board ID Register

**Address: 3FFE (H)**

The Board ID register contains a fixed value that can be read by your initialization routine to detect the presence of the board. The one-byte value of this register is: 45 (Hex), ASCII value "E".



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### 5.7.7 Board Status Register

**Address: 3FFD (H)**

The Board Status register indicates the status of the board. In addition, this register indicates which options have been selected, as described below. Do not modify this register. Status bits are active if set to 1.

| Bit | Description |
|---|---|
| **07** | 1 = Board Type is EXC-1553PCI/Px |
| **06** | X (Don't Care) |
| **05** | X (Don't Care) |
| **04** | 1 = Board Halted<br>0 = Board Running |
| **03** | 1 = Self-Test OK |
| **02** | 1 = Timers OK |
| **01** | 1 = RAM OK |
| **00** | 1 = Board Ready |

**Board Status Register**

**NOTE** Board operation stops after you clear the Start bit in the Start Register. Following this, the board sets bit 04 (Board Halted). Certain registers may be modified only after the Board Halted bit has been set. After receiving a subsequent Start command (by writing to the Start register), the board resets the Board Halted bit. The condition of this bit after power-up or software reset is logic 1.



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### 5.7.8 Start Register

**Address: 3FFC (H)**

The Start register controls the Start/Stop operation of the board. Writing the appropriate bit (bit 0) to the Start register starts the Bus Controller transfer operation. When operating in Continuous Loop or *n*-Times mode, set the Start and Loop bits in the Start register. The Loop and *n*-Times number are selected via the Loop Count register. In the One-Shot and *n*-Times modes, the board resets the Start bit in the register after *all* messages have been transferred. The board does not reset any bit while in Continuous Loop mode. To halt the Loop operation between messages, set bit 00 to 0. In order to halt the operation at the end of the entire frame, set bit 02 to 0 (bit 02 is not tested between message transfers). Related data bit 04 in the Board Status register indicates when the board has been halted (see Board Status Register, page 5-20).

| Bit | Description |
|---|---|
| **03-07** | 0 |
| **02** | 1 = Loop Mode<br>0 = One-Shot Mode |
| **01** | 0 |
| **00** | 1 = Start Operation<br>0 = Stop |

**Start Register**

**NOTE** It is also possible to start operation of the board by sending a low TTL pulse of 100 nsec minimum to the EXSTART*x*n pin (see Connectors, page 9-5).



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### 5.7.9 Interrupt Condition Register

**Address: 3FFB (H)**

The Interrupt Condition register allows you to set interrupt triggers. When a condition occurs that is enabled in this register, an interrupt is generated. A logic 1 enables the interrupt condition. To determine which condition caused the interrupt, check the Message Status register.

Set the Interrupt Condition register before issuing a Start command to the board. To modify the Interrupt Condition register, issue a Stop command, modify the register, and then issue a Start command (see Start Register page 5-21).

**NOTE** The interrupt will be sent at the end of the message for all interrupt conditions.

| Bit | Description |
|---|---|
| **04-07** | 0 |
| **03** | Message Error |
| **02** | End Of Frame |
| **01** | Message Complete |
| **00** | 0 |

**Interrupt Condition Register**

### 5.7.10 Message Status Register

**Address: 3FFA (H)**

The Message Status register indicates the status of the current message being processed. The definition of each status bit is given below. Logic 1 indicates that the condition is activated.

| Bit | Bit Name | Description |
|---|---|---|
| **04-07** | **0** | |
| **03** | **Message Error** | The message has been sent. As a result, the Error bit has been set in the Message Status word. |
| **02** | **End Of Frame** | The last word of the last message in the frame has been sent. |
| **01** | **Message Complete** | The last word of the message has been sent. |
| **00** | **Wait For Continue** | A message with the Halt bit set has been encountered. Reset the Halt bit in the Control word to continue. |

**Message Status Register**

**NOTE** Status bits are *not* reset by the board. After reading them, you must reset them.



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### 5.7.11 RT Response Time Register

**Address: 3FF9 (H)**

The RT Response Time register sets the Remote Terminal's Response Time. The resolution of the Response Time register is 155 nsec. per bit, measured as the dead time on the 1553 bus. The minimum time is approximately 4 µsec. The value in the register is added to the minimum time. The actual Response Time has a tolerance of ±1 µsec.

Set the Response Time register before issuing a Start command to the board. To modify the Response Time register, issue a Stop command, modify the register, and then issue a Start command (see Start Register page 5-21).

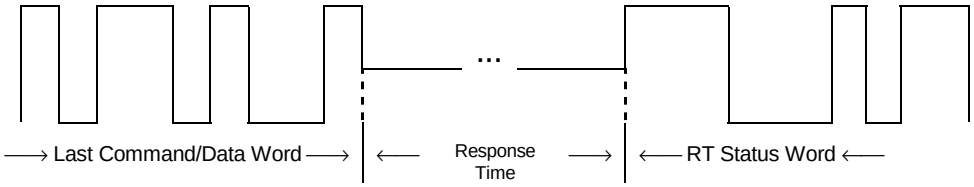


**Figure 5-6 RT Response Time Definition**

**Example** Setting the RT Response Time Register

To request a response time of 9 µsec:

Write 32 to the RT Response Time register.

[32 x 0.155 ≅ 5 µsec] + 4 µsec = 9 µsec.

### 5.7.12 Loop Count Register

**Address: 3FF6 (H)**

The Loop Count register is used in conjunction with the Loop bit in the Start register. If the Loop bit in the Start register is set, then set the Loop Count register to specify the number of times the Message frame will be transmitted. A value of zero is interpreted as a request for continuous looping. Set the Loop Counter register before issuing a Start command to the board. To modify the Loop Counter register, issue a Stop command, modify the register, and then issue a Start command (see Start Register page 5-21).

| Bit | Value | Description |
|---|---|---|
| **00-07** | **0** | Transmits in Continuous Loop. |
| | **1-255** | Sends Message Frame *n*-times (1–255) as defined. |

**Loop Count Register**



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### 5.7.13 Bit Count Register

**Address: 3FF5 (H)**

The Bit Count Register sets the total number of bits in the 1553 word, including Sync(3) and Parity(1). This register is used by the board only for messages for which the Bit Count Error bit is set in the Control Word of the Message Block (see Control Word, page 5-8). If the Bit Count Error bit is not set, a (valid) 20-bit word is transmitted regardless of the contents of the Bit Count Register.
Set the Bit Count Register before issuing a Start command to the board. To modify the Bit Count Register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 5-21).

| Bit | Description | | | |
|---|---|---|---|---|
| **03–07** | 0 | | | |
| **00–02** | **Bit 02** | **Bit 01** | **Bit 00** | **No. of 1553 bits sent per word** |
| | 0 | 0 | 0 | 17 (-3) |
| | 0 | 0 | 1 | 18 (-2) |
| | 0 | 1 | 0 | 19 (-1) |
| | 0 | 1 | 1 | 20 |
| | 1 | 0 | 0 | 21 (+1) |
| | 1 | 0 | 1 | 22 (+2) |
| | 1 | 1 | 0 | 23 (+3) |

**Bit Count Register**



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### 5.7.14 Word Count Register

**Address: 3FF4 (H)**

The Word Count register controls the number of 1553 data words (±3) in the message and allows you to inject a Word Count error. The error is an offset relative to the 1553 command word Word Count field. This register is used by the board only for messages for which the Word Count Error bit is set in the Control word register (see Control Word, page 5-8). If the Word Count Error bit is not set, a correct number of words are transmitted regardless of the contents of the Word Count register.

Set the Word Count register before issuing a Start command to the board. To modify the Word Count register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 5-21).

| Register Value | Word Count Offset |
|---|---|
| FD H | –3 Words |
| FE H | –2 Words |
| FF H | –1 Word |
| 00 H | No Error Injection |
| 01 H | +1 Word |
| 02 H | +2 Words |
| 03 H | +3 Words |

**Word Count Register Values**



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### 5.7.15 BC Response Time Register

**Address: 3FF3 (H)**

The BC Response Time register sets the BC's Response Time window, whose value determines the maximum (wait) time until an RT's Status Response is considered invalid by the BC. The resolution of the BC Response Time register is 155 nsec. per bit, measured as the dead time on the 1553 bus. The minimum time is approximately 2 µsec.

Set the BC Response Time register before issuing a Start command to the board. To modify the BC Response Time register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 5-21).

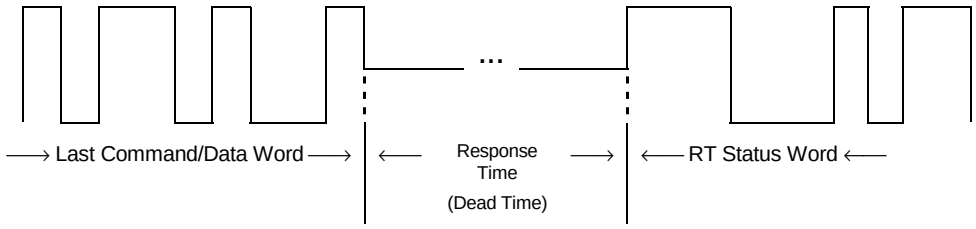


**Figure 5-7 BC Response Time Definition**

**Example** Setting the BC Response Time Register

To set up a BC response time of 14 µsec:

Write 90 to the BC Response Time register.

90 x 0.155 ≅ 14 µsec

### 5.7.16 Stack Pointer

**Address: 3FF0–3FF1 (H)**

The Stack pointer points to the Instruction stack. The Instruction stack can reside anywhere between the locations 0000 (H) and 33FF (H). Set the Stack Pointer register before issuing a Start command to the board. To modify the Stack Pointer register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 5-21).



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### 5.7.17 Frame Time Register

**Address: 3FEE-3FEF (H)**

The Frame Time Register contains the 16-bit Frame Time value for Continuous and *n*-Times modes operation. The value written to the Frame Time Register is multiplied by the value set in the Frame Time Resolution register pair described below. The value set must equal the desired multiplication factor – 1 (see Calculating Frame Time, page 5-16).

Set the Frame Time register before issuing a Start command to the board. To modify the Frame Time register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 5-21).

### 5.7.18 Frame Time Resolution Register

**Address: 3FEC-3FED (H)**

The 16-bit Frame Time Resolution value represents the resolution of the Frame Time counter in increments of 155 nsec. The high register contains the MSB, the low register contains the LSB (see also Continuous or One-Shot Message Transfers, page 5-15).

Set the Frame Time Resolution register before issuing a Start command to the board. For an example of how to calculate Frame Time and Frame Time Resolution, see Calculating Frame Time, page 5-16. To modify the Frame Time Resolution register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 5-21).

### 5.7.19 Instruction Counter

**Address: 3FEB, 3FEA (H)**

The Instruction Counter must be loaded with the number of instructions (1553 Messages) to execute in the current frame. The value must be greater than 0 before the user writes to the Start register to begin a transmission. Set the Instruction counter to 1 for one message, 2 for two messages, etc. The board updates the Instruction counter by decrementing the value and writing it back to memory at the end of each message transfer.

Set the Instruction Counter register before issuing a Start command to the board. To modify the Instruction Counter register, issue a Stop command, modify the register, then issue a Start command (see Start Register, page 5-21). When in the Continuous Loop mode, the Instruction Counter register cycles from the initial value down to 1.

The low register (3FEA) contains the MSB; the high register (3FEB) contains the LSB. Therefore, for an Instruction Counter less that 256, use the LSB only, address 3FEB.



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### 5.7.20 Minor Frame Time Register

**Address: 3FE8 (H) WRITE**

The 16-bit Minor Frame Time register is used to set the length of a single minor frame (see Minor Frame Operation, page 5-10). The resolution of the Minor Frame Time register is 1 µsec. per bit. The maximum value is approximately 65 msec., which can be extended by the multiplier set in the Minor Frame Time Resolution register described below.

The Minor Frame Time register must be set before issuing a Start command to the board. To modify the Minor Frame Time register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 5-21).

### 5.7.21 Minor Frame Resolution Register

**Address: 3FE6 WRITE**

The Minor Frame Resolution is a multiplier of the Minor Frame Time described above. The value written to the Minor Frame Resolution register allows the user to extend the Minor Frame Time beyond the 65 msec. maximum in the Minor Frame Time register. The maximum Minor Frame Resolution is 255. The maximum Minor Frame Time possible using both registers is approximately 16 sec.

**Example** To generate a Minor Frame Time of 1 sec., set the Minor Frame Time register to F424 (H) (62,500 Dec.), and set the Minor Frame Resolution register to 10 (H) (16 Dec.).

The Minor Frame Time Resolution register must be set before issuing a Start command to the board. To modify the Minor Frame Time Resolution register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page ).

### 5.7.22 Board Options Register

**Address: 3E84 (H) READ ONLY**

The Board Options Register is a 16-bit register in which the low 8 bits are reserved. This register identifies the type of on-board firmware.

| Bit | Description |
|---|---|
| **10-15** | Reserved |
| **09** | 1 = 1760 |
| **08** | 1 = 1553 |
| **00-07** | Reserved |

**Board Options Register**



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### 5.7.23 Firmware Revision Register

**Address: 3E80 (H)**

The Firmware Revision register indicates the revision level of the on-board firmware. The value 0001 0010 would be read as revision level: 1.2.

### 5.7.24 Asynchronous Start Flag Register

**Address: 3424 (H) WRITE**

Write a 1 to the Asynchronous Start Flag register to indicate that it is now time to send a selected frame asynchronously. The board will automatically reset this value to 0 when it sends the frame.

### 5.7.25 Asynchronous Frame Pointer Register

**Address: 3422 (H) WRITE**

The Asynchronous Frame Pointer register points to the beginning of the selected frame that the user scheduled to send asynchronously.

### 5.7.26 Asynchronous Message Count Register

**Address: 3420 (H) WRITE**

Write to the Asynchronous Message Count register to set how many messages to send, when sending the asynchronous frame over the data bus. The maximum number of messages allowed in a frame is determined by the amount of available space in the message stack area of the board and the size of the individual messages.



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# 6 Bus Monitor Operation

Chapter 6 describes EXC-1553PCI/P*x* operation in Bus Monitor mode. The information in this chapter applies to all 1553 channels present on the board, except where indicated otherwise. All addresses referred to in this chapter are offset from the base address of the channel accessed (see Base Address Registers, page 2-7). The following topics are covered:



The Bus Monitor can operate in one of two modes:

### Sequential mode

1553 Message blocks are stored in sequential locations in memory. Sequential mode supports two types of operations:

Fixed-Block operation: 1553 messages are stored at fixed sequential blocks in the memory. Sequential Fixed-Block mode supports Trigger capability.

Link-List operation: 1553 messages are packed one after another in the memory, separated by a header.

### Look-Up Table mode

Each 1553 message is stored in a unique Message block. In Look-Up Table mode, the board addresses the user-programmable look-up table when it receives a 1553 Command word. The Command word's RT address, T/R bit, and Subaddress fields make up the 11-bit pointer to a Look-Up table with 2048 (2K x 8) locations.

Use the Board Configuration register (Board Configuration Register, page 6-21) to program the desired mode of operation.



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### TO DETERMINE WHETHER THE BOARD IS INSTALLED AND READY TO OPERATE:

Perform the following procedure after a power-up or a software reset.

1. Check the Board ID register (test for value = 45 H).
2. Check the Board Status register (test for Board Ready bit = 1).

The board is installed and ready when both registers contain the correct values (as written above). For software reset operations, set these values to 0 immediately prior to writing to the (software) Board Reset register.

**NOTE** Throughout this manual, writing a 1 to the Start register is referred to as “issuing a Start command.”



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## 6.1 Sequential Fixed-Block Memory Map

| | |
|---|---|
| Time Tag Options | 700C H |
| Time Tag Counter Word 1 | 700A – 700B H |
| Time Tag Counter Word 0 | 7008 – 7009 H |
| Time Tag Reset Register | 7007 H |
| Reserved | 7004 – 7006 H |
| Options Select | 7003 H |
| Global Software Reset Register | 7002 H |
| Interrupt Reset Register | 7001 H |
| Software Reset Register | 7000 H |
| Reserved | 4000 – 6FFF H |
| Board Configuration Register | 3FFF H |
| Board ID Register | 3FFE H |
| Board Status Register | 3FFD H |
| Start Register | 3FFC H |
| Interrupt Condition Register | 3FFB H |
| Message Status Register | 3FFA H |
| Reserved | 3FF8 – 3FF9 H |
| Time Tag Resolution | 3FF7 H |
| Reserved | 3FF6 H |
| Message Counter | 3FF5 H |
| Counter Trigger | 3FF4 H |
| Trigger Word #1 | 3FF2 – 3FF3 H |
| Trigger Mask #1 | 3FF0 – 3FF1 H |
| Trigger Word #2 | 3FEE – 3FEF H |
| Trigger Mask #2 | 3FEC – 3FED H |
| Trigger Control Register | 3FEB H |
| Mode Code Control Register | 3FEA H |
| Broadcast Control Register | 3FE8 H |

| | |
|---|---|
| Reserved | 3E90 – 3FE7 H |
| Monitor Response Time Reg. | 3E8E H |
| Reserved | 3E86 – 3F8D H |
| Boards Option Register | 3E84 E |
| Reserved | 3E81 – 3E83 H |
| Firmware Revision Register | 3E80 H |
| Message Block Area (200 Blocks) | 0000 – 3EF7 H |

**Figure 6-1 BM: Sequential Fixed-Block Memory Map**



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## 6.2 Sequential Link-List Memory Map

| | |
|---|---|
| Time Tag Options | 700C H |
| Time Tag Counter Word 1 | 700A – 700B H |
| Time Tag Counter Word 0 | 7008 - 7009 H |
| Time Tag Reset Register | 7007 H |
| Reserved | 7004 – 7006 H |
| Options Select | 7003 H |
| Global Software Reset Register | 7002 H |
| Interrupt Reset Register | 7001 H |
| Software Reset Register | 7000 H |
| Reserved | 4000 – 6FFF H |
| Board Configuration Register | 3FFF H |
| Board ID Register | 3FFE H |
| Board Status Register | 3FFD H |
| Start Register | 3FFC H |
| Interrupt Condition Register | 3FFB H |
| Message Status Register | 3FFA H |
| Reserved | 3FF8 – 3FF9 H |
| Time Tag Resolution | 3FF7 H |
| Reserved | 3FF6 H |
| End Buffer Pointer | 3FF4 – 3FF5 H |
| Next Message Pointer | 3FF2 – 3FF3 H |
| Reserved | 3FEB – 3FF1 H |
| Mode Code Control Register | 3FEA H |
| Broadcast Control Register | 3FE8 H |

| | |
|---|---|
| Reserved | 3E90 – 3FE7 H |
| Monitor Response Time Reg. | 3E8E H |
| Reserved | 3E86 – 3F8D H |
| Boards Option Register | 3E84 E |
| Reserved | 3E81 – 3E83 H |
| Firmware Revision Register | 3E80 H |
| Message Block Spill Area | 3400 – 3E7F H |
| Message Block Area | 0000-3DFF H |

**Figure 6-2 BM: Sequential Link-List Memory Map**



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## 6.3 Sequential Mode Message Block Area

The Sequential Mode Message Block area is partitioned either into blocks of fixed length or into a link list of blocks of varying lengths. The type of partitioning is determined by the Board Configuration register (see Board Configuration Register, page 6-21).

For a description of the Time Tag function, see Time Tag Word, page 6-12.

### 6.3.1 Message Block Fixed-Block Operation

In Fixed-Block operation, the Message Block area is divided into 200 blocks of 80 bytes each. The first block starts at address 0000 (H), the second at 0050 (H), the third at 00A0 (H), etc. The Trigger option can be used only in Sequential mode with Fixed-Block operation (see Trigger Operation, page 6-13).

| Information is stored in the memory in the following sequence: | Word Offset |
|---|---|
| 1553 Data Word | • |
| • | • |
| • | • |
| • | • |
| 1553 Data Word | +8 |
| 1553 Command Word | +6 |
| Time Tag Word 1 | +4 |
| Time Tag Word 0 | +2 |
| Message Status Word | 0 |

**Figure 6-3 Bus Monitor Message Block: Fixed-Block Operation**



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### 6.3.2 Message Block Link-List Operation

In Link-List operation, the Message Block area is divided into a linked list of message blocks. The length of each message block varies according to message size. The first two locations in each block comprise the message header. This header contains the address of the next Message Block header. The header of the last 1553 block received contains XXFF (End of File), indicating that there are no more messages stored. After a message is processed and stored in memory, the header of the preceding message block is updated from XXFF to the address (of the header in the block) of the newly stored message.

The Link-List method can store more data than Fixed-Block operation.

Take special care with the last message in the Message Block area. Since the buffer never wraps around in the middle of a message and a message may start at any address up to 3DFE (H), the final message in the buffer may extend past the end of the standard Message Block area into the Message Block Spill area. The End Buffer pointer (End Buffer Pointer, page 6-26) exists for this special case. The End Buffer pointer points to the address after the last location of the message, indicating the length of the message. The next message will start at the first location of the Message Block area (0000H).

The following figures illustrate the contents of the Message block. For a description of the Time Tag function, see Time Tag Word, page 6-12.

| Information is stored in the memory in the following sequence: | Word Offset |
|---|---|
| End Of File: XXFF | • |
| 1553 Data Word | • |
| • | • |
| • | • |
| • | • |
| 1553 Data Word | +A |
| 1553 Command Word | +8 |
| Time Tag Word 1 | +6 |
| Time Tag Word 0 | +4 |
| Message Status Word | +2 |
| Message Header - Address of Next Block | 0 |

**Figure 6-4 Bus Monitor Message Block: Link-List Operation**



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## 6.4 Look-Up Table Mode Memory Map

| | | | |
|---|---|---|---|
| Time Tag Options | 700C H | | |
| Time Tag Counter Word 1 | 700A – 700B H | | |
| Time Tag Counter Word 0 | 7008 – 7009 H | | |
| Time Tag Reset Register | 7007 H | | |
| Reserved | 7004 – 7006 H | | |
| Options Select | 7003 H | | |
| Global Software Reset Register | 7002 H | | |
| Interrupt Reset Register | 7001 H | | |
| Software Reset Register | 7000 H | | |
| Data Block Look-Up Table (2K x 8) | 4000 – 47FF H | | |
| Board Configuration Register | 3FFF H | | |
| Board ID Register | 3FFE H | | |
| Board Status Register | 3FFD H | | |
| Start Register | 3FFC H | Reserved | 3E90 – 3FE7 H |
| Interrupt Condition Register | 3FFB H | | |
| Message Status Register | 3FFA H | Monitor Response Time Reg. | 3E8E H |
| Reserved | 3FF8 – 3F9 H | Reserved | 3E86 – 3F8D H |
| Time Tag Resolution | 3FF7 H | | |
| Reserved | 3FF3 – 3FF6 H | Board Options Register | 3E84 H |
| Last Block Register | 3FF2 H | Reserved | 3E81 – 3E83 H |
| Reserved | 3FEB – 3FF1 H | Firmware Revision Register | 3E80 H |
| Mode Code Control Register | 3FEA H | Reserved | 2800 – 3E7F H |
| Broadcast Control Register | 3FE8 H | Message Block Area (128 Blocks) | 0000 – 27FF H |

**Figure 6-5 BM Look-Up Table Mode Memory Map**



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## 6.5 Look-Up Table Mode

In Look-Up Table mode, the board can store 128 unique messages by using a 2K × 8 Look-up table in on-board memory. Each byte in the table is divided into a 7-bit block number and an Interrupt Select bit, as described below. Data Block numbers (0 – 127 decimal) each consisting of 80 bytes are loaded into the table. The first block starts at address 0, the second at 50 (H), etc. Set the Interrupt Select bit to specify which messages will set the interrupt flag. The Interrupt Condition register must also be programmed.

| Bit | Description |
|---|---|
| **07** | 1 = Interrupt Select Bit is Enabled |
| **00-06** | Block Numbers (0-127) |

**Look-Up Table Byte Structure**

When a 1553 message is received, the Command word's RT address, T/R Bit, and Subaddress fields are used as an 11-bit index to the Look-up table. This index is used to extract the Data block number from the Look-up table.

For RT-to-RT messages all the information is stored in both the receiving and the transmitting RTs data blocks.

| | (11 most significant bits of the 1553 command word) | | | | | |
|---|---|---|---|---|---|---|
| **Base address** | **RT address (5 bits)** | **T/R (1 bit)** | **Sub-address (5 bits)** | **Look-Up table (2K x 8)** | **Data block** | **Hex address of data block** |
| 4000+ | 11111 | 1 | 11111 | Block # | Data Block 127 | 27B0 |
| | • | • | • | • | • | |
| | • | • | • | • | • | |
| | • | • | • | • | • | |
| 4000+ | 00000 | 0 | 00011 | Block # | Data Block 3 | 00F0 |
| 4000+ | 00000 | 0 | 00010 | Block # | Data Block 2 | 00A0 |
| 4000+ | 00000 | 0 | 00001 | Block # | Data Block 1 | 0050 |
| 4000+ | 00000 | 0 | 00000 | Block # | Data Block 0 | 0000 |

**Figure 6-6 Look-Up Table**



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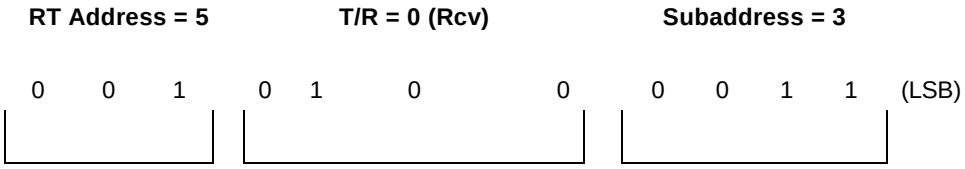
TO CREATE THE ADDRESS TO THE TABLE:

1. Isolate the eleven (most significant) bits of the 1553 command word (RT Address, T/R, and Subaddress field), and determine their hex value.

**Example** To allocate a data block for a 1553 receive message to RT#5, Subaddress #3.




Hex representation = 143

2. Add the hex value of this part of the command word to the base address of the look-up table (4000H).

```
  4000  (H)
+ 143   (H)
-------------
  4143  (H)
```

3. Write the Data Block number to this location.

**Example** `POKE &H4143,xx` writes an 8-bit Block Number value to the look-up table address &H4143. Each data block, beginning at address 0000 is 80 bytes long (for up to 32 1553 data words). The address of a block is obtained by multiplying its block number by 50 (H).

THE BLOCK ADDRESSES ARE CALCULATED AS FOLLOWS:

- Block 0 is located at location 0000 (H).
- Block 1 is located at location 0050 (H).
- The location of the block is obtained by multiplying the block number by 50 H.



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## 6.6 Look-Up Table Mode Message Block Area

| Information is stored in the memory in the following sequence: | Byte Offset |
|---|---|
| See Appendix B for Message Formats | +78<br>•<br>•<br>•<br>+8 |
| 1553 Command Word | +6 |
| Time Tag Word 1 | +4 |
| Time Tag Word 0 | +2 |
| Message Status Word | 0 |

**Figure 6-7 Bus Monitor Message Block: Look-Up Table Mode**



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## 6.7 Message Status Word

The Message Status word is identical for all Bus Monitor modes. The Message Status word indicates the status of the message transfer. This word is created by the board. Do not confuse it with the 1553 Status word (see 1553 RT Status Words, page 4-7). The contents of the Message Status word are described below.

**NOTE** A logic 1 indicates the occurrence of a status flag.

| Bit | Bit Name | Description |
|---|---|---|
| **15** | **End Of Message** | Message transfer completed. |
| **14** | **Trigger Found** | Trigger message was received and stored. This status is valid for Sequential Fixed-Block mode with the following modes:<br>**Store After** mode: the Trigger Found bit will be set only in the *first* Trigger message.<br>**Store Only** mode: the Trigger Found bit will be set in *every* Trigger message. (See Trigger Operation, page 6-13) |
| **13** | **RT-RT** | RT-to-RT message was received. |
| **12** | **Message Error Bit Set** | Message Error bit (bit 10) in the RT Status word was set. |
| **11** | **RT Status Bit Set** | A bit other than the Message Error bit in the RT Status word was set. The Error Bit is *not* set in conjunction with this bit. |
| **10** | **Invalid Message** | 1553 message-level error occurred (Word Count, Incorrect Sync, etc.). Examine the other bits in this table to determine which error occurred. |
| **09** | **Reserved** | Set to 0 |
| **08** | **Bus A/B** | Bus on which the message was transferred:<br>0 = Bus B<br>1 = Bus A |
| **07** | **Invalid Word Received** | At least one invalid 1553 word received (i.e. bit count, Manchester code, parity). |
| **06** | **Word Count High** | RT transmitted too many words. |
| **05** | **Word Count Low** | RT transmitted too few words. |
| **04** | **Incorrect RT Address** | Received 1553 Status word did not contain the correct RT address. |
| **03** | **Incorrect Sync Received** | Sync of either the command or the data word(s) is incorrect. |
| **02** | **Non-Contiguous Data** | Invalid gap between received 1553 words. |
| **01** | **Response Time Error** | Response Time error occurred in the message. |
| **00** | **Error** | Error occurred. (The error type is defined in one of the other message status bit locations.) |

**Message Status Word**



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## 6.8 Time Tag Word

In all Bus Monitor modes, each incoming message is stored with a Time Tag value. The Time Tag value is a 32-bit word used to determine the time elapsed since the Start command was issued or the time between 1553 messages. The Time Tag uses a 32-bit, free running counter whose resolution is fixed at 4 usec. per bit. Reset the Time Tag counter (to 0) any time by writing to the Time Tag Reset register (see Time Tag Reset Register, page 6-19).

The Time Tag counter's value is written to the dual-port RAM during the reception of the (first) command of each message.

**NOTE** In addition to reading the Time Tag value in the message stack, the user can also read the counter's value at any time in the Time Tag counter (see Time Tag Counter, page 6-19).



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## 6.9 Trigger Operation

### Only Sequential Fixed-Block mode supports triggers

A trigger is a filter the user can set to tell the board when and how to store 1553 messages. The board can be programmed to store messages in the following ways:

**Store All** Stores all 1553 messages, without regard to triggers; no triggers are active

**Store Only** Stores only messages that meet the trigger condition

**Store After** Stores only the trigger message and messages that come after the trigger message

The user can define up to two triggers. Each trigger is defined using two registers:

- Trigger Word Register
- Trigger Mask Register

Use the Trigger Word Register to define a particular 1553 Command word or a Message Status word as a trigger. For example, use the Message Status word as the trigger source to store all messages on bus A, only messages with errors, or messages with errors received over bus B, etc. (see Trigger Word Registers, page 6-14).

The Trigger Mask Register defines which bits of the trigger word (defined in the Trigger Word register) are relevant and which can be ignored (“don’t care”). The Trigger Mask registers must be defined when using the trigger function (see Trigger Mask Registers, page 6-15.)

Set the Trigger Control Register to specify the following trigger conditions (see Trigger Control Register, page 6-16):

- Trigger source (1553 Command word or Message Status word)
- Type of storage (Store All, Store Only, or Store After)
- Active trigger word (Trigger Word 1 and/or 2)

Set the registers - Trigger Word, Trigger Mask and Trigger Control - before issuing a Start command to the board. To modify these registers, set the Initialize bit in the Start register to 10 (H), modify the Trigger Word, Trigger Mask and Trigger Control registers, then issue a Start command 01 (H).



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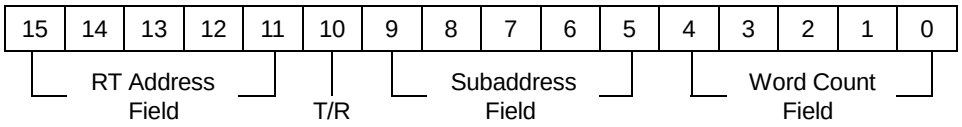
### 6.9.1 Trigger Word Registers (1 and 2) **Address: 3FF2, 3FEE (H)**

Use the Trigger Word register to define a particular 1553 Command word or a Message Status word as a trigger. Load these locations (illustrated below) with the desired 1553 Command word or Message Status word, which will be used as the trigger source. You must also define the Trigger Mask Registers when using the trigger function (see Trigger Mask Registers, page 6-15.). Define which trigger is active (Trigger 1, Trigger 2, or both) via the Trigger Control Register (see Trigger Control Register, page 6-16).

#### Using the 1553 Command Word—Trigger Word Registers

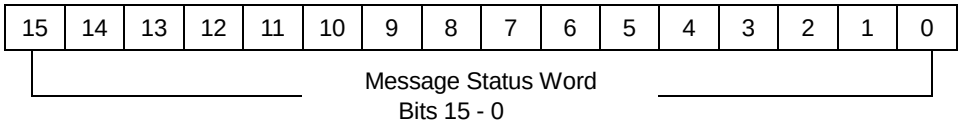
Use a 1553 Command word as a trigger when you want to filter messages based on information found in the Command word. For example, if you want to filter messages from a particular RT, or with a particular word count, set the Trigger Word register with those parameters defined in the 1553 Command word.




#### Using the Message Status Word—Trigger Word Registers

Use a Message Status word as a trigger when you want to filter messages based on information found in the Message Status word. Do not confuse the Message Status word with the 1553 Status word (see 1553 RT Status Words, page 4-7). For example, if you want to filter messages transferred over bus A (vs. bus B), or error messages, set the Trigger Word register with those parameters defined in the Message Status word.

For an explanation of the Message Status Word, see page 6-11.



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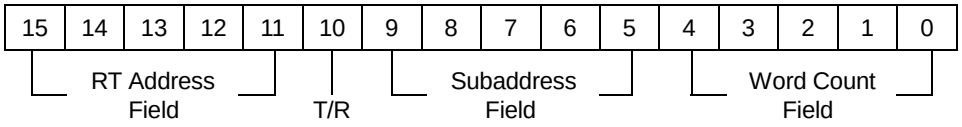
### 6.9.2 Trigger Mask Registers (1 and 2) **Address: 3FF0, 3FEC (H)**

Set the Trigger Mask register to define which bits of the trigger word (defined in the Trigger Word register) are relevant and which can be ignored ("don't care"). You must define the Trigger Mask registers when using the trigger function. All bits in this register should be set to 1, except for those bits you want to be "don't care" in the incoming Command word or Message Status Word.

#### Using the 1553 Command Word—Trigger Mask Registers

After setting the Trigger Word register with a 1553 Command word, write 0s to the bits in the Trigger Mask register that you want to be "don't care" in the 1553 Command word trigger.



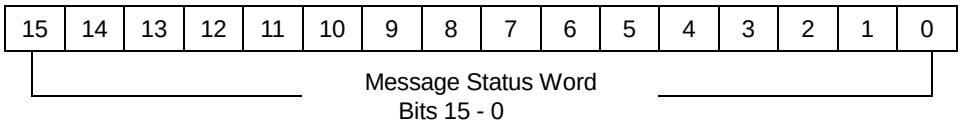

1 = Trigger on corresponding bit value in Trigger Word Register

0 = Corresponding bit value in Trigger Word Register is "Don't Care"

#### Using the Message Status Word—Trigger Mask Registers

After setting the Trigger Word register with a Message Status word, write 0s to the bits in the Trigger Mask register that you want to be "don't care" in the Message Status word trigger.

For an explanation of the Message Status Word, see page 6-11.




1 = Trigger on corresponding bit value in Trigger Word Register

0 = Corresponding bit value in Trigger Word Register is "Don't Care"



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### 6.9.3 Trigger Control Register

**Address: 3FEB (H)**

The Trigger Control register is relevant only in Sequential Fixed-Block mode. Set the Trigger Control register to specify the following trigger conditions:

- Trigger source (1553 Command word or Message Status word)
- Type of storage (Store All, Store Only, or Store After)
- Active trigger word (Trigger Word 1 and/or 2)

**NOTE**
1. Logic 1 enables the function.
2. To use trigger(s), at least one of the bits Store All, Store Only, or Store After, must be set.

| Bit | Description |
|---|---|
| **07** | Trigger Source:<br>0 = 1553 Command Word<br>1 = Message Status Word |
| **05-06** | Reserved |
| **04** | 1 = Store After |
| **03** | 1 = Store Only |
| **02** | 1 = Store All |
| **01** | 1 = Enable Trigger Word #2 |
| **00** | 1 = Enable Trigger Word #1 |

**Trigger Control Register**

### 6.9.4 Defining a Trigger - Example

Conditions:

- Define the Command word 0825 (H) as Trigger word #1 (Receive Command for RT#1, Subaddress #1, and 5 words).
- Ignore the Word Count field.
- Use Trigger word 1 (Disable Trigger word 2).

Procedure:

1. Set Trigger Word 1 register = 0825 (H)
2. Set Trigger Mask 1 register = FFE0 (H)
3. Set Trigger Control register = 09 (H)



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## 6.10 Program Examples: BM Mode

**Bus Monitor Sequential Fixed-Block Mode**

| BASIC Instruction | Remarks |
|---|---|
| `10 POKE &H3FFF,08` | Set the Board Configuration register for Bus Monitor Sequential Fixed-Block mode. |
| `20 POKE &H3FF0,xx` | Set trigger mask #1—low to xx. |
| `30 POKE &H3FF1,xx` | Set trigger mask #1—high to xx. |
| `40 POKE &H3FF2,xx` | Set trigger word #1—low to xx. |
| `50 POKE &H3FF3,xx` | Set trigger word #1—high to xx. |
| `60 POKE &H3FEB,xx` | Set the Trigger Control register (see Trigger Control Register, page 6-16). |
| `70 POKE &H3FEA,00` | Set the Mode Code Control Register to 1s and 0s (see Mode Code Control Register page6-27). |
| `80 POKE &H3FE8,00` | Set the Broadcast Control register to RT31 = regular (see Broadcast Control Register, page 6-28). |
| `90 POKE &H3FFC,01` | Start command. |

**NOTE** Messages are read from memory starting from address 0000.

**Bus Monitor Sequential Link-List Mode**

| BASIC Instruction | Remarks |
|---|---|
| `10 POKE &H3FFF,&H10` | Set the Board Configuration register to Bus Monitor Link-List mode (see Board Configuration Register page 6-21). |
| `20 POKE &H3FEA,00` | Set the Mode Code Control register to 1s and 0s (see Mode Code Control Register page6-27). |
| `30 POKE &H3FE8,01` | Set the Broadcast Control Register to RT31 = Broadcast (see Board Configuration Register page 6-21). |
| `40 POKE &H3FFC,01` | Start command. |

**NOTE** Messages are read from memory starting from address 0000.



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**Bus Monitor Look-Up Table Mode**

| BASIC Instruction | Remarks |
|---|---|
| `10 POKE &H3FFF,&H20` | Set the Board Configuration register to Bus Monitor Look-Up Table mode. |
| `20 POKE &H3FEA,00` | Set the Mode Code Control register to 1s and 0s (see Mode Code Control Register page6-27). |
| `30 POKE &H3FE8,00` | Set the Broadcast Control register to RT31 = Regular. |
| `40 POKE &H4143,00` | Set the Look-Up Table so that Command words with Remote Terminal 5, Receive mode, and Subaddress 3 point to Data Block #0 (see Look-Up Table Mode, page 6-8). |
| `50 POKE &H4144,01` | Set the Look-Up Table so that Command words with Remote Terminal 5, Receive mode, and Subaddress 4 point to Data Block #1 (see Look-Up Table Mode, page 6-8). |
| `60 POKE &H3FFC,01` | Start Command. |

**NOTE** Messages are read from memory according to the address pointer derived from Command word (see Look-Up Table Mode, page 6-8).

## 6.11 Control Register Definitions

### 6.11.1 Time Tag Options Register

**Address: 700C (H) WRITE ONLY**

Set the Time Tag Options Register's 00 bit to select the current bank's Time Tag Counter Clock Source. After power-up or software reset, the Time Tag Options Register's 00bit is set to 0.

For external Time Tag Clock source, see Communication I/O Signals Description of Connector JI, page 9-7.

| Bit | Description |
|---|---|
| **01-07** | Reserved |
| **00** | 0 = Internal Time Tag Clock<br>1 = External Time Tag Clock |

**Time Tag Options Register**



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### 6.11.2 Time Tag Counter

**Address: 7008–700B (H) READ ONLY**

Read the two 16-bit words of the Time Tag counter to determine the current free-running, 32-bit Time Tag counter value. You may read the counter at any time.

THE COUNTER MUST BE READ IN THE FOLLOWING SEQUENCE:

1. Read 7008 H (16 bit, read only)
2. Read 700A H (16 bit, read only)

7008 H contains the lo word; 700A H contains the hi word. The resolution of the counter is 4 µsec. per bit.

The counter is reset upon power-up, or software reset and stays reset until a Start command is issued. When a Start command is issued, the counter starts counting. To re-initialize to 0, write to the Time Tag Reset register. When it reaches the value FFFFFFFF (H), the counter wraps around to 0 and continues counting.

### 6.11.3 Time Tag Reset Register

**Address: 7007 (H) WRITE ONLY**

Write to the Time Tag Reset register to reset the channel's Time Tag Counter (data field = don't care). Immediately after the reset, the counter will start to count from 0.

**NOTE** The counter can also be reset from an external source (see Connectors, page 9-5).



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### 6.11.4 Options Select Register

**Address: 7003 (H)**

The Concurrent BM control bit of the Options Select Register is only relevant for users of the EXC-1553PCI/P2, P3 and P4 boards. The EXC-1553PCI/P*x* provides that a second channel (Channel 1 or Channel 3) may be set up to operate as Concurrent Monitors on the 1553 bus connected to Channels 0 and Channels 2. When configured in this way, Channel 0 may operate as a BC and/or RT while Channel 1 will concurrently monitor the Channel 0 1553 bus. Similarly, Channel 2 may operate as a BC and/or RT while Channel 3 will concurrently monitor the Channel 2 1553 bus.

The Options Select Register is used to select the bus to which Channels 1 and Channels 3 are connected. On reset, Channels 1 and Channels 3 are set to monitor their own buses.

**NOTE** Channels 0 and Channels 2 are always connected to their own 1553 buses in Monitor Mode, independent of the state of this register.

OPTIONS SELECT REGISTER FOR **CHANNEL 1**

| Bit | Description |
|---|---|
| **02-07** | Don't care |
| **01** | Concurrent BM control bit (only for EXC-1553PCI/P2, P3, P4 configuration).<br>1 = Select Channel 1 as Concurrent BM of Channel 0<br>0 = Select Channel 1 as Independent BM Channel |
| **00** | Don't care |

OPTIONS SELECT REGISTER FOR **CHANNEL 3**

| Bit | Description |
|---|---|
| **02-07** | Don't care |
| **01** | Concurrent BM control bit (only for EXC-1553PCI/P4 configuration).<br>1 = Select Channel 3 as Concurrent BM of Channel 2<br>0 = Select Channel 3 as Independent BM Channel |
| **00** | Don't care |

**Options Select Register**



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### 6.11.5 Global Software Reset Register

**Address: 7002 (H)**

Write to the Global Software Reset register to reset all channels present on the card, simultaneously (data field = don't care).

**NOTE** Global Software Reset erases all locations in dual-port RAM. Board status, Board ID, and Firmware Revision registers are written by the board after the reset operation is completed.

### 6.11.6 Interrupt Reset Register

**Address: 7001 (H)**

To reset the Interrupt signal generated by the channel, write to the Interrupt Reset register at the beginning of a user-written interrupt service routine (data field = don't care).

### 6.11.7 Software Reset Register

**Address: 7000 (H)**

Write to the Software Reset register to reset the channel (data field = don't care). The Board status, the Board ID, and Firmware revision registers are written by the board after the reset operation has been completed.

**WARNING** *Reset erases all memory locations in the dual-port RAM.*

### 6.11.8 Board Configuration Register

**Address: 3FFF (H)**

Before issuing a Start command to the board, set the operating mode of the board via the Board Configuration register. To modify the Board Configuration register, issue a Stop command, modify the register, and then issue a Start command (see Start Register, page 6-23).

| Hex Value | Operating Mode |
|---|---|
| **08** | BM Sequential Block |
| **10** | BM Sequential Link-List |
| **20** | BM Look-Up Table |

**Board Configuration Register Values: Monitor Mode**



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### 6.11.9 Board ID Register

**Address: 3FFE (H)**

The Board ID register contains a fixed value that can be read by your initialization routine to detect the presence of the board. The one-byte value of this register is: 45 (Hex), ASCII value “E”.

### 6.11.10 Board Status Register

**Address: 3FFD (H)**

The Board Status register indicates the status of the board. In addition, this register indicates which options have been selected. Do not modify this register. Status bits are active if set to 1.

| Bit | Description |
|---|---|
| **07** | 1 = Board Type is EXC-1553PCI/Px |
| **06** | X (Don’t Care) |
| **05** | X (Don’t Care) |
| **04** | 1 = Board Halted<br>0 = Board Running |
| **03** | 1 = Self-Test OK |
| **02** | 1 = Timers OK |
| **01** | 1 = RAM OK |
| **00** | 1 = Board Ready |

**Board Status Register**

**NOTE** Board operation stops after you clear the Start bit in the Start Register. Following this, the board sets bit 04 (Board Halted). Certain registers may be modified only after the Board Halted bit has been set. After receiving a subsequent Start command (by writing to the Start register), the board resets the Board Halted bit. The condition of this bit after power-up or software reset is logic 1.



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### 6.11.11 Start Register

**Address: 3FFC (H)**

The Start Register controls the Start/Halt operation of the board. Refer to the Board Halted bit (Data bit 04) in Board Status Register, page 6-22, which indicates when the board has been halted.

Set the Start Register to execute one of the functions described below.

| Bit | Description |
|---|---|
| **06-07** | 0 |
| **05** | 1 = Stop On Trigger<br>0 = Continue After Stop |
| **04** | 1 = Initialize Board<br>0 = Stay in Monitor Mode |
| **03** | 1 = Clear Memory<br>0 = Don't Clear Memory |
| **01-02** | 0 |
| **00** | 1 = Start Operation<br>0 = Halt |

**Start Register**

**NOTE**

1. The board tests Clear Memory (bit 03) and Initialize Board (bit 04) only when the Start /Halt bit (bit 00) = 0.

   Clear Memory clears the 1553 message blocks and all readable control registers. The Initialize Board bit enables you to re-initialize the board, change the board's mode of operation (modify the Board Configuration register) and restart.

   To switch Monitor modes, you must stop and start the board (Start/Halt bit = bit 00) and set the Initialize Board bit (bit 04). After the specific function is completed, the board sets the Initialize Board bit and the Start/Halt bit to 0.

2. The Stop On Trigger/Continue bit (bit 05) is used in Sequential Fixed-Block mode only. The Stop On Trigger/Continue bit is tested when the Message counter equals the Message Counter Trigger. If Stop On Trigger/Continue bit = 1, the board will stop storing 1553 messages. Setting Stop On Trigger/Continue bit = 0 allows the board to continue monitoring operations. You must first Continue (set bit 05 = 1) before Halting the board (setting bit 00 = 0).



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3. Bit 04 of the Board Status register is set if one of the following is true:
   - A Halt command is issued (bit 00 is set to 0)
   - An Initialize Board command is issued (bit 04 is set to 1)
4. It is also possible to start operation of the board by sending a low TTL pulse of 100 nsec minimum to the EXSTART*x*n pin. (See Connectors, page 9-5).

### 6.11.12 Interrupt Condition Register

**Address: 3FFB (H)**

Set the Interrupt Condition register to enable interrupt triggers. When a condition enabled in this register occurs, an interrupt is generated. Logic 1 enables the interrupt condition. Check the Message Status register to determine which condition caused the interrupt.

Set the Interrupt Condition register before issuing a Start command to the board. To modify the Interrupt Condition register, issue a Stop command, modify the register, then issue a Start command (see Start Register, page 6-23).

**NOTE** For all interrupt conditions, the interrupt will be sent at the end of the message.

| Bit | Description |
|---|---|
| **03-07** | 0 |
| **02** | 1 = Counter Trigger Match (Valid Only in Sequential Fixed-Block Mode) |
| **01** | 1 = Message Reception in Progress (Valid in All Modes) |
| **00** | 1 = Trigger Word Received (Valid Only in Sequential Fixed-Block Mode) |

**Interrupt Condition Register**



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### 6.11.13 Message Status Register

**Address: 3FFA (H)**

The Message Status register indicates the status of the current message being processed. Each status bit is described in the table below. Logic 1 indicates that the condition is activated.

| Bit | Description |
|---|---|
| **03-07** | 0 |
| **02** | 1 = Counter Trigger Match |
| **01** | 1 = Message Reception In Progress |
| **00** | 1 = Trigger Word Received/Busy |
| | Trigger word received is valid only In Sequential Fixed-Block mode. |
| | Busy is valid in Linked-List and Look-Up Table mode. The busy bit is set when the board is processing a message. It is set together with message reception in progress, but is reset approximately 5 µsec. after the end of each message. For consecutive messages with short intermessage gap times, the busy bit may not be reset between messages. |

**Message Status Register**

**NOTE** Status bits are *not* reset by the board. Reset them after reading them.

### 6.11.14 Time Tag Resolution Register

**Address: 3FF7 (H)**

The 8-bit value in the Time Tag Resolution register represents the resolution of the Time Tag Counter in unites of 4 µsec.

To determine the Time Tag Counter's resolution, use the equation:

= (Time Tag Resolution register value + 1) x 4 µsec.

A value of 0 corresponds to a resolution of 4 microseconds; a value of 1 corresponds to a resolution of 8 microseconds, etc.

The user must set the Time Tag Resolution register before issuing a Start command to the board. To modify the register, issue a Stop command, modify the register, and then issue a Start command. (see Start Register, page 6-23).



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### 6.11.15 Message Counter Register

**Address: 3FF5 (H)**

**Sequential Fixed-Block mode only**

Read the Message Counter register to determine the current Message Block number (0 - 199). The value is incremented by the board as each message is received. The first counter increment (to 1), which indicates that the first message has been received and stored, occurs at the beginning of the *second* 1553 message transfer operation. To determine the arrival of the first 1553 message, check the Message Status word of the *first* Message block. The End of Message bit (bit 15) in the Message Status word will be set.

### 6.11.16 Counter Trigger Register

**Address: 3FF4 (H)**

**Sequential Fixed-Block mode only**

Read the Counter Trigger register to determine when a specific message block number has been updated by the board. Set the Counter Trigger register to a value that when equal to the Message counter will set a bit in the Message status register and set an interrupt (if programmed in the Interrupt Condition register).

Set the Counter Trigger register before issuing a Start command to the board. To modify the Counter Trigger register, issue a Stop command, modify the register, then issue a Start command
(see Start Register, page 6-23)

The user can also program the board to stop monitoring when the Counter Trigger value is equal to the Message Counter (see the Stop/Continue bit in the Start Register, page 6-23).

### 6.11.17 End Buffer Pointer

**Address: 3FF4–3FF5 (H)**

**Link-List mode only**

The End Buffer pointer points to the address following the last word in the final message in the Message Block area. The End Buffer pointer is updated each time a final message is written into the buffer. Final messages that are longer than the remaining available space in the Message Block area do not wrap around to the start of the buffer. They are spilled into the Message Block Spill area, which is contiguous to the Message Block area. The value of this register varies from 3400 (H) (end of Message Block area) to 347E (H) (end of Message Block Spill area). Until the first buffer wrap around occurs, this register contains 0000 (H).



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### 6.11.18 Next Message Pointer

**Address: 3FF2–3FF3 (H)**

**Link-List mode only**

The Next Message pointer is a 16-bit pointer that indicates the address of the 1553 message about to be written. The Next Message pointer register is updated at the end of each message storage operation. It cycles from 0 (H) to 33FE (H).

### 6.11.19 Last Block Register

**Address: 3FF2 (H)**

**Look-Up Table mode only**

Read the Last Block register to determine the (Look-Up Table) block number of the current 1553 message. This register is used to identify the location of the current 1553 message. The Last Block register is updated at the end of each message reception.

### 6.11.20 Mode Code Control Register

**Address: 3FEA (H)**

Set the Mode Code Control register to specify which 1553 Subaddress value indicates the reception of a 1553 Mode command.

Set the Mode Code Control register before issuing a Start command to the board. To modify the Mode Code Control register, issue a Stop command, modify the register, and then issue a Start command (see Start Register page 6-23).

| Bit | Description | | |
|---|---|---|---|
| 02-07 | 0 | | |
| 00-01 | **Bit 01** | **Bit 00** | **Subaddresses Recognized as Mode Code** |
| | 0 | 0 | 31 and 0 |
| | 0 | 1 | 0 |
| | 1 | 0 | 31 |
| | 1 | 1 | 0 and 31 |

**Mode Code Control Register**



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### 6.11.21 Broadcast Control Register

**Address: 3FE8 (H)**

Write to the Broadcast Control register to select whether RT address 11111 (RT 31) is interpreted as a valid RT address or as a Broadcast address.

| Bit | Description |
|---|---|
| **01-07** | 0 |
| **00** | 1 = Broadcast option is active. RT #31 is a Broadcast Address. |
| | 0 = Broadcast option is inactive. RT #31 is a Regular RT. |

**Broadcast Control Register**

### 6.11.22 Monitor Response Time Register

**Address: 3E8E (H)**

The Monitor Response Time Register sets the maximum wait time until an RT's Status Response is considered valid by the Monitor.

The Monitor Response Time Register is measured in microseconds. The default value of the register is 14, in not otherwise set by the user.

### 6.11.23 Boards Options Register

**Address: 3E84 (H)**

The Module Options register is a 16-bit register in which the low 8 bits are reserved. This register identifies the type of on-module firmware.

| Bit | Description |
|---|---|
| **10-15** | Reserved |
| **09** | 1 = 1760 |
| **08** | 1 = 1553 |
| **00-07** | Reserved |

**Board Options Register**

### 6.11.24 Firmware Revision Register

**Address: 3E80 (H)**

The Firmware Revision register indicates the revision level of the on-board firmware. The value 0001 0010 would be read as revision level: 1.2.



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# 7 Concurrent Monitor Option

Chapter 7 describes Concurrent Monitor operation, an option available only on the EXC-1553PCI/PM*x* module.

The following topics are covered:



On the PM*x* module the Concurrent Monitor operates automatically when the module is started in either RT or BC/RT modes. This monitor is not available when the module is not running in one of the above modes. It operates in sequential fixed block mode (the 1553 Message blocks are stored in sequential locations in memory). The storing of messages starts at the first block.

See Ordering Information, page 10-1 for part number details.

## 7.1 Concurrent Monitor Memory Map

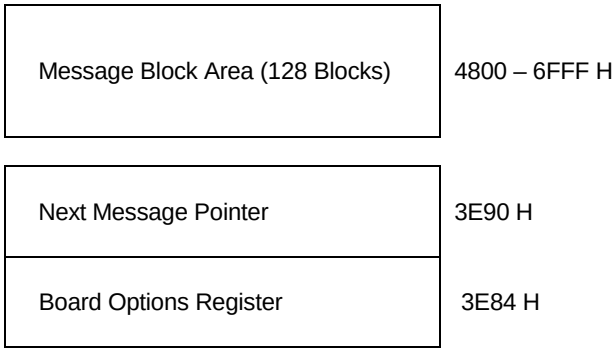


**Figure 7-1 Concurrent Monitor Memory Map**



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## 7.2 Message Block Area

The Message Block area is divided into 128 blocks of 80 bytes each. The first block starts at address 4800 (H), the second at 4850 (H), the third at 48A0 (H), etc.

| | |
|---|---|
| Block #127 | 6FA0 H |
| • • • | |
| Block #2 | 48A0 H |
| Block #1 | 4850 H |
| Block #0 | 4800 H |

### 7.2.1 Message Block Structure

Each message block occupies 40 words. These 40 words include a message status word, two time tag words and all the 1553 message words.

| |
|---|
| 1553 Data Word |
| • |
| • |
| 1553 Data Word |
| 1553 Command Word |
| Time Tag Word #2 (MSB) |
| Time Tag Word #1 (LSB) |
| Message Status Word |

**Concurrent Monitor Message Block Structure**



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### 7.2.2 Message Status Word

The Message Status word indicates the status of the message transfer. The module creates this word. Do not confuse it with the 1553 Status word. (See 1553 RT Status Words, page 4-7.) The contents of the Message Status word are shown below.

**NOTE**
1. Note that the Message Status word is different in RT/Concurrent Monitor mode and BC-RT/Concurrent Monitor mode.
2. A logic 1 indicates the occurrence of a status flag.

| Bit | Bit Name | Description |
|---|---|---|
| **15** | **End Of Message** | Message transfer completed. |
| **14** | **Bus A / B** | Bus on which the message was transferred (1 = BUS A) |
| **13** | **Reserved** | Set to 0 |
| **12** | **Message Error Bit Set** | Message Error bit (bit 10) in the RT Status word was set. |
| **11** | **RT Status Bit Set** | A bit other than the Message Error bit in the RT Status word was set. The Error bit is not set in conjunction with this bit. |
| **10** | **TX Time Out** | The module, acting as receiver in RT-to-RT message, did not sense a transmitter status word. |
| **09** | **Response Error** | Response time error occurred in the message, even if no RT is active on the module. |
| **08** | **Invalid Message RT/Concurrent Monitor** | 1553 message-level error occurred (e.g., Word Count, Sync Error). See other bits set for the exact error. For example: an RT-to-RT message which contains two receive messages. |
| **07** | **Invalid Word Received** | At least one invalid 1553 word received (i.e. bit count, Manchester code, parity). |
| **06** | **Reserved** | Set to 0 |
| **05** | **Word Count Error** | Incorrect number of words received in the message. |
| **04** | **Incorrect RT Address** | Received 1553 Status word did not contain the correct RT address. |
| **03** | **Sync Error** | Sync of either the command or the data word(s) is incorrect. |
| **02** | **Non-Contiguous Data** | Invalid gap between received 1553 words. |
| **01** | **RT2RT Message** | RT-to-RT message was received. |
| **00** | **Error** | Error occurred. (The error type is defined in one of the other message status bit locations.) |

**Message Status Word: RT/Concurrent Monitor**



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| Bit | Bit Name | Description |
|---|---|---|
| **15** | **End Of Message** | Message transfer completed. |
| **14** | **Bus A / B** | Bus on which the message was transferred (1 = BUS A) |
| **13** | **Reserved** | Set to 0 |
| **12** | **Message Error Bit Set** | Message Error bit (bit 10) in the RT Status word was set. |
| **11** | **RT Status Bit Set** | A bit other than the Message Error bit in the RT Status word was set. The Error bit is not set in conjunction with this bit. |
| **10** | **Invalid Message** | 1553 message-level error occurred (e.g., Word Count, Sync Error). See other bits set for the exact error. For example: an RT- to-RT message which contains two receive messages. |
| **09** | **Response Error** | Response time error occurred in the message, even if no RT is active on the module. |
| **08** | **Reserved** | Set to 0 |
| **07** | **Invalid Word Received** | At least one invalid 1553 word received (i.e. bit count, Manchester code, parity). |
| **06** | **Word Count High** | RT transmitted too many words. |
| **05** | **Word Count Low** | RT transmitted too few words. |
| **04** | **Incorrect RT Address** | Received 1553 Status word did not contain the correct RT address. |
| **03** | **Sync Error** | Sync of either the command or the data word(s) is incorrect. |
| **02** | **Non-Contiguous Data** | Invalid gap between received 1553 words. |
| **01** | **RT2RT Message** | RT-to-RT message was received. |
| **00** | **Error** | Error occurred. (The error type is defined in one of the other message status bit locations.) |

**Message Status Word: BC-RT/Concurrent Monitor**

**NOTE** The message contents are valid only after the Message Status Word has been written, which is indicated by the End of Message bit being turned on.



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### 7.2.3 1553 Message Words

The 1553 message words are stored in the sequence they appear on the bus, i.e., 1553 Command words, 1553 Status words, 1553 Data words - all according to the order of the specific type of message.

## 7.3 Control Register Definitions

### 7.3.1 Next Message Pointer

**Address: 3E90 (H)**

The Next Message pointer is a 16-bit pointer that indicates the address of the 1553 message about to be written. The Next Message pointer register is updated at the end of each message storage operation. It cycles from 4800 (H) to 6FFE (H).

### 7.3.2 Module Options Register

**Address: 3E84 (H)**

The Module Options register is a 16-bit register in which the low 8 bits are reserved. This register identifies the type of on-module firmware.

| Bit | Description |
|---|---|
| **10-15** | Reserved |
| **09** | 1 = 1760 |
| **08** | 1 = 1553 |
| **00-07** | Reserved |

**Board Options Register**



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# 8 Switching Modes of Operation

Many test applications utilizing the EXC-1553PCI/P*x* simulate only one operation mode, i.e., Bus Controller. For these applications, the information in this chapter is not relevant.

If your application requires simulation of more than one mode, switch from one mode of operation to another, i.e., between the Bus Controller and Remote Terminal modes.

TO SWITCH BETWEEN MODES OF OPERATION:

1. Halt the operation of the board (via the Start register).
2. Modify the Configuration register to the desired mode.
3. Set up the memory as required.
4. Set the Start bit in the Start register.



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# 9 Mechanical and Electrical Specifications

Chapter 9 describes the mechanical and electrical specifications of the EXC-1553PCI/P*x* board. The following topics are discussed:



## 9.1 Board Layout

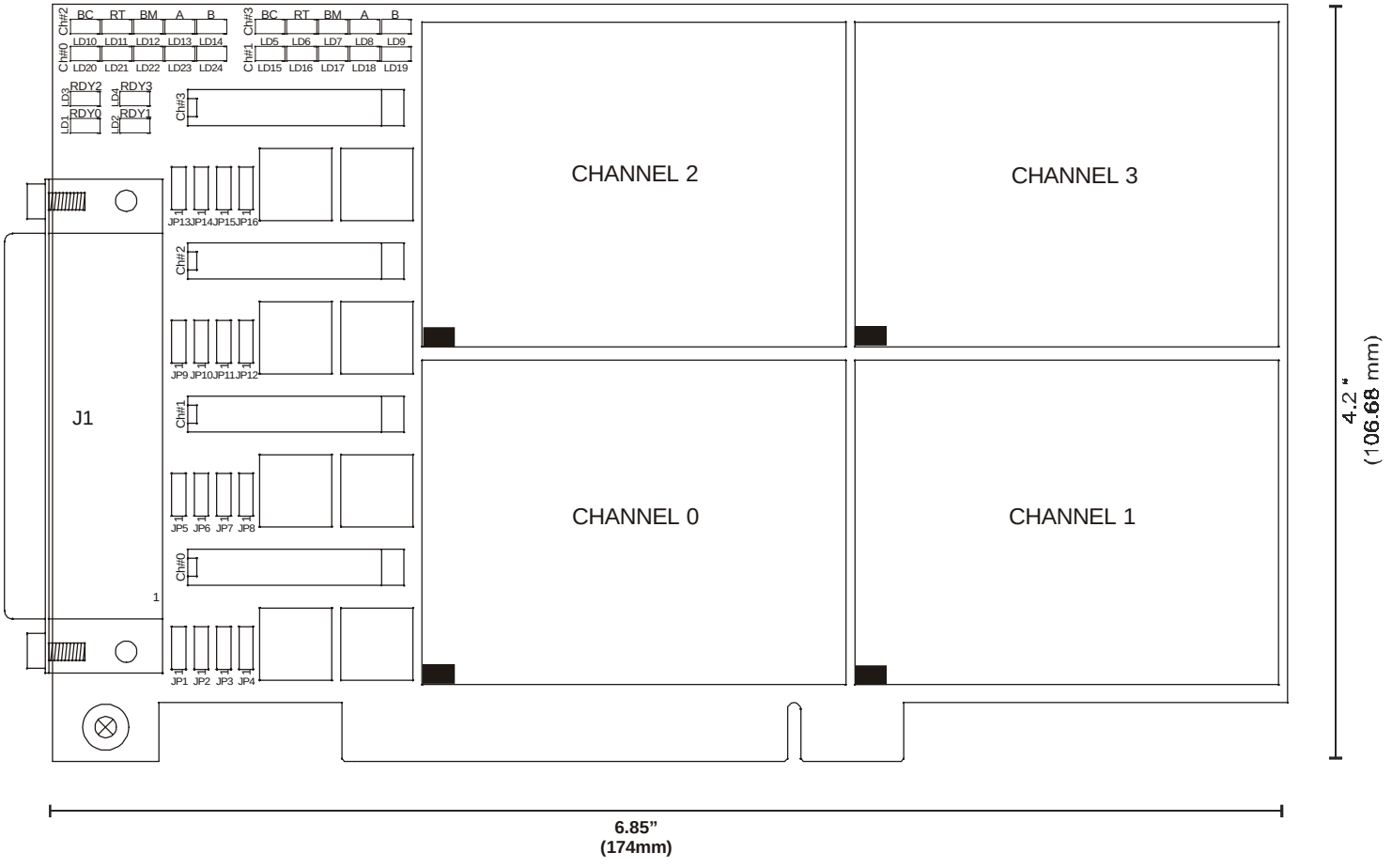


**Figure 9-1 EXC-1553PCI/P*x* Board Layout**



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## 9.2 LED Indicators

The EXC-1553PCI/P*x* board contains 24 LEDs. The LEDs indicate each channel's operational mode and bus activity. The function of each LED is described below.

| | Channel No. | | | |
|---|---|---|---|---|
| **Indication** | **0** | **1** | **2** | **3** |
| Channel Ready | LED1 | LED2 | LED3 | LED4 |
| BC Mode Active | LED20 | LED15 | LED10 | LED5 |
| RT Mode Active | LED21 | LED16 | LED11 | LED6 |
| Monitor Mode Active | LED22 | LED17 | LED12 | LED7 |
| Bus A Active | LED23 | LED18 | LED13 | LED8 |
| Bus B Active | LED24 | LED19 | LED14 | LED9 |

**Table 9-1 LED Indicators**



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# 9.3 Jumpers: Rev B Board

### 9.3.1 Channel *x* 1553 Coupling Mode Select Jumpers [JP1 - JP16]

The board can be either direct or transformer coupled to the 1553 Bus. Groups of four jumpers select the coupling mode for each channel.

Table 9-2 defines the jumper settings for all 16 jumpers.

| Coupling Mode | Jumper Settings | |
|---|---|---|
| | **JP2,4,6,8,10,12,14,16,** | **JP1,3,5,7,9,11,13,15,** |
| **Direct Coupled** | short 1 – 2 | short 2 – 3 |
| **Transfer Coupled** | short 2 – 3 | short 1 - 2 |

**Table 9-2 Jumper Settings Required to Select Coupling Mode**

Table 9-3 defines the jumper groups for each channel.

| Channel | Bus | Jumper Group |
|---|---|---|
| **0** | A | JP1, JP2 |
| **0** | B | JP3, JP4 |
| **1** | A | JP5, JP6 |
| **1** | B | JP7, JP8 |
| **2** | A | JP9, JP10 |
| **2** | B | JP11, JP12 |
| **3** | A | JP13, JP14 |
| **3** | B | JP15, JP16 |

**Table 9-3 Channel Jumper Groups**

**Example** To set Channel 2 to transformer-coupled, short pins 1 and 2 of JP9 and JP11 and short pins 2 and 3 of JP10 and JP12.

### 9.3.2 Factory Default Jumper Settings

The following are the factory preset default settings:

| | | | |
|---|---|---|---|
| **JP1, 3, 5, 7, 9, 11, 13, 15** | Pins 1 & 2 | Shorted | Transformer-Coupled mode |
| **JP2, 4, 6, 8, 10, 12,14, 16** | Pins 2 & 3 | Shorted | Transformer–Coupled mode |



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# 9.4 Jumpers: Rev C Board

## 9.4.1 Channel *x* 1553 Coupling Mode Select Jumpers: Rev C

The board can be either direct or transformer coupled to the 1553 Bus. Groups of four jumpers select the coupling mode for each channel.

Table 9-4 defines the jumper settings for all 16 jumpers.

| Coupling Mode | Jumper Settings |
|---|---|
| | **JP1 – JP16** |
| **Direct Coupled** | short 2 – 3 |
| **Transfer Coupled** | short 1 - 2 |

**Table 9-4 Jumper Settings Required to Select Coupling Mode: Rev C**

Table 9-5 defines the jumper groups for each channel.

| Channel | Bus | Jumper Group |
|---|---|---|
| **0** | A | JP1, JP2 |
| **0** | B | JP3, JP4 |
| **1** | A | JP5, JP6 |
| **1** | B | JP7, JP8 |
| **2** | A | JP9, JP10 |
| **2** | B | JP11, JP12 |
| **3** | A | JP13, JP14 |
| **3** | B | JP15, JP16 |

**Table 9-5 Channel Jumper Groups: Rev C**

**Example** To set Channel 2 to transformer coupled, short pins 1 and 2 of JP9, JP10, JP11 and JP12.

## 9.4.2 Factory Default Jumper Settings

The following are the factory preset default settings:

| | | | |
|---|---|---|---|
| **JP1, JP16** | Pins 1 & 2 | Shorted | Transformer-Coupled mode |



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## 9.5 Connectors

The EXC-1553PCI/P*x* board contains all communication I/O signals on one female high density DB-62-pin connector (J1) (P/N: HDL-62SLC PCB). Mating connectors (P/N: HDT 62-PD) with plastic hoods are included. The connectors pinouts and signals description are described below.

### 9.5.1 Connector J1 Pinout

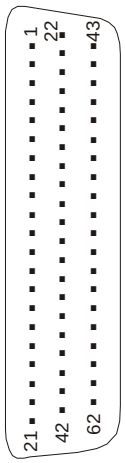


**Figure 9-2 Connector J1 Pinout (Connector Front View)**



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### 9.5.2 Connector J1 Pin Assignments

| | | | | | |
|---|---|---|---|---|---|
| **1** | BUSAL1 | **22** | SHIELD | **43** | BUSAL2 |
| **2** | BUSAH1 | **23** | SHIELD | **44** | BUSAH2 |
| **3** | BUSBL1 | **24** | SHIELD | **45** | BUSBL2 |
| **4** | BUSBH1 | **25** | SHIELD | **46** | BUSBH2 |
| **5** | EXSTART1n | **26** | DIGITAL GND | **47** | EXSTART2n |
| **6** | BUSAL3 | **27** | SHIELD | **48** | BUSAL4 |
| **7** | BUSAH3 | **28** | SHIELD | **49** | BUSAH4 |
| **8** | BUSBL3 | **29** | SHIELD | **50** | BUSBL4 |
| **9** | BUSBH3 | **30** | SHIELD | **51** | BUSBH4 |
| **10** | EXSTART3n | **31** | SHIELD | **52** | EXSTART4n |
| **11** | N/C | **32** | DIGITAL GND | **53** | N/C |
| **12** | N/C | **33** | SHIELD | **54** | N/C |
| **13** | N/C | **34** | SHIELD | **55** | N/C |
| **14** | N/C | **35** | SHIELD | **56** | N/C |
| **15** | N/C | **36** | SHIELD | **57** | N/C |
| **16** | N/C | **37** | DIGITAL GND | **58** | N/C |
| **17** | EXTCLK1 | **38** | EXTCLK2 | **59** | EXTCLK3 |
| **18** | EXTCLK4 | **39** | N/C | **60** | N/C |
| **19** | EXTGRST1n | **40** | EXTGRST2n | **61** | EXTGRST3n |
| **20** | EXTGRST4n | **41** | N/C | **62** | N/C |
| **21** | N/C | **42** | DIGITAL GND | | |

N/C = Not Connected



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### 9.5.3 Communication I/O Signals Description of Connector JI

| Signal | Description |
|---|---|
| BUSAHI_1<br>BUSALO_1 | Channel #1, Bus A, connection. |
| BUSBHI_1<br>BUSBLO_1 | Channel #1, Bus B, connection. |
| BUSAHI_2<br>BUSALO_2 | Channel #2, Bus A, connection. |
| BUSBHI_2<br>BUSBLO_2 | Channel #2, Bus B, connection. |
| BUSAHI_3<br>BUSALO_3 | Channel #3, Bus A, connection. |
| BUSBHI_3<br>BUSBLO_3 | Channel #3, Bus B, connection. |
| BUSAHI_4<br>BUSALO_4 | Channel #4, Bus A, connection. |
| BUSBHI_4<br>BUSBLO_4 | Channel #4, Bus B, connection. |
| SHIELD (case) | Provided for 1553 cables shield connection. This signal is connected to the case of the computer. |
| EXTGRSTxn | Channel x External Time Tag Reset low active TTL input. Provides an option to reset the Time Tag counter from an external source. This signal can also be used for simultaneously resetting the Time Tag counter in a multiple channel application. Apply a low TTL pulse of 100 nsec/min. With respect to the GND pin. Note: The reset takes affect only after the board is started in RT or BM mode. |
| EXSTARTxn | External Start Low Active TTL input, (see Start Register, page 5-21) |
| EXTCLKx | Channel #x External Time Tag Clock TTL input. Provides an option to drive the Time Tag Counter Clock from an external source for synchronizing in a multiple-board application. Connect a 250KHz or less clock with respect to the GND pin.<br>**Note:** The external clock takes effect only after you activate the EXTCLK bit in the Time Tag Options register. (see Time Tag Options Register, page 6-18). |
| GND | Provides ground reference for the digital signal connections. |



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## 9.6 Power Requirements

The EXC-1553PCI/P*x* power requirements are listed in the following table:

| | +5v |
|---|---|
| **EXC-1553PCI/P1** | 1.2A |
| **EXC-1553PCI/P2** | 2.2A |
| **EXC-1553PCI/P3** | TBD |
| **EXC-1553PCI/P4** | TBD |

**Table 9-6 Power Requirements**



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# 10 Ordering Information

Chapter 10 explains how to indicate which options you want when ordering a EXC-1553PCI/P*x* board.

The following suffixes must be added to the name of the board (EXC-1553PCI/Px) to indicate the specific options. The suffixes are added to EXC-1553PCI/P*x* in the order in which they appear in the table.

| Suffix | Description |
|---|---|
| **M** | Concurrent Monitor option |
| **x** | Number of channels: 1 - 4 |
| **-E** | Ruggedized, extended temperature operation (-40° – +85°C) |
| **-1760** | MIL-STD-1760 options |

ORDERING EXAMPLES

| PART NUMBER | DESCRIPTION |
|---|---|
| **EXC-1553PCI/P1** | Single Channel MIL-STD-1553 interface board for PCI systems. Supports BC, RT, BC/Concurrent-RT and BM modes. |
| **EXC-1553PCI/P2** | Dual Channel MIL-STD-1553 interface board for PCI systems. Supports BC, RT, BC/Concurrent-RT and BM modes. |
| **EXC-1553PCI/PM3** | Three-Channel MIL-STD-1553 interface board for PCI systems. Supports BC, RT, BC/Concurrent-RT and BM modes with Concurrent Monitor option in RT and BC/RT modes. |
| **EXC-1553PCI/P4 -E** | Four-Channel MIL-STD-1553 interface board for PCI systems. Supports BC, RT, BC/Concurrent-RT and BM modes with extended temperature option. (-40°C - +85°C) |
| **EXC-1553PCI/P1-1760** | Single Channel MIL-STD-1553 interface board for PCI systems. Supports BC, RT, BC/Concurrent-RT and BM modes with MIL-STD-1760 option. |



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# 11 Appendices

Chapter 11 contains appendices describing the Military Standard 1553B word, Military Standard message formats and internal and external loop back tests. The following topics are included:





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# Appendix A MIL-STD-1553B Word Formats

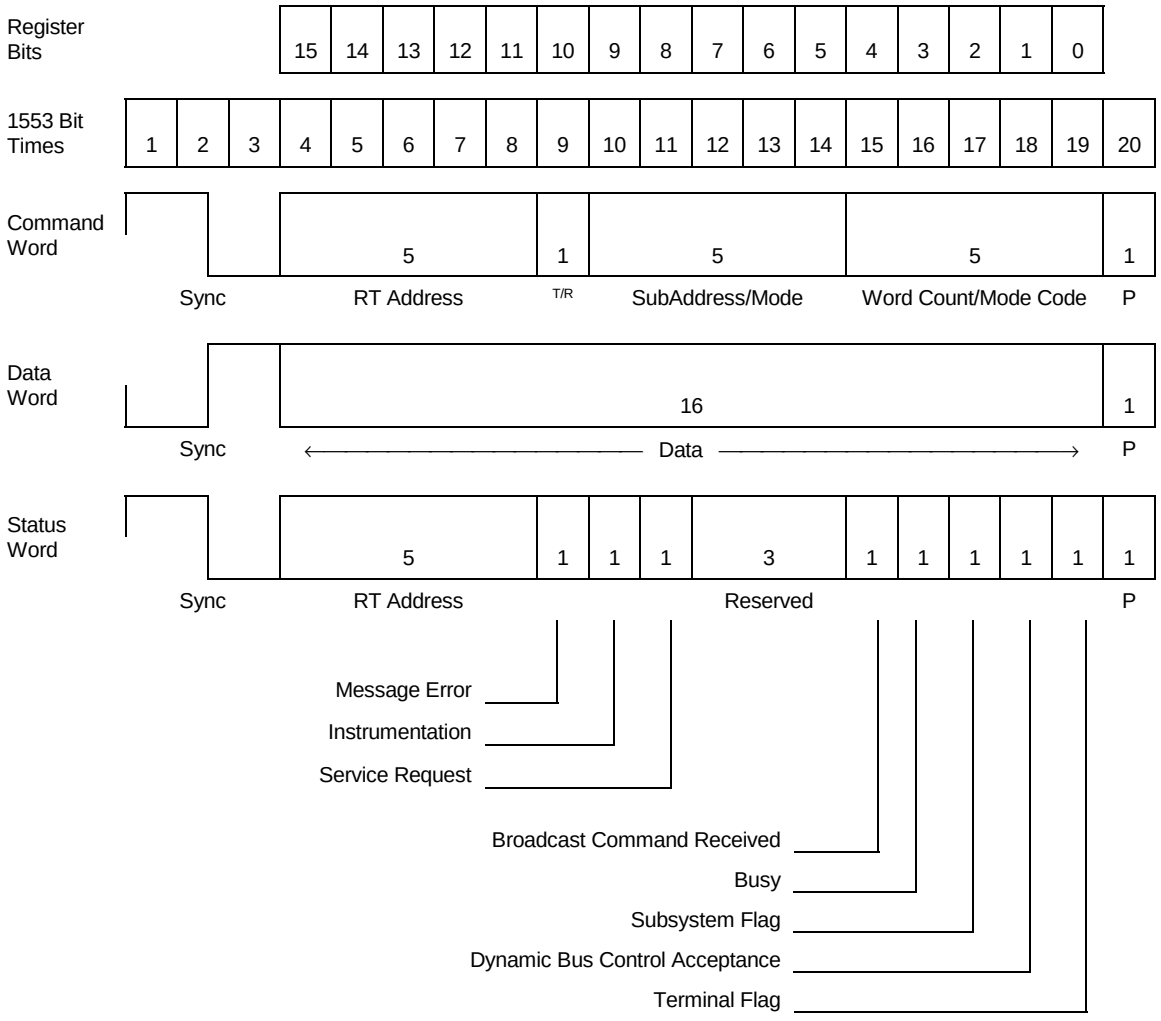


**Figure 11-1 MIL-STD-1553B Word Formats**

NOTE: T/R = Transmit/Receive
P = Parity



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# Appendix B MIL-STD-1553B Message Formats

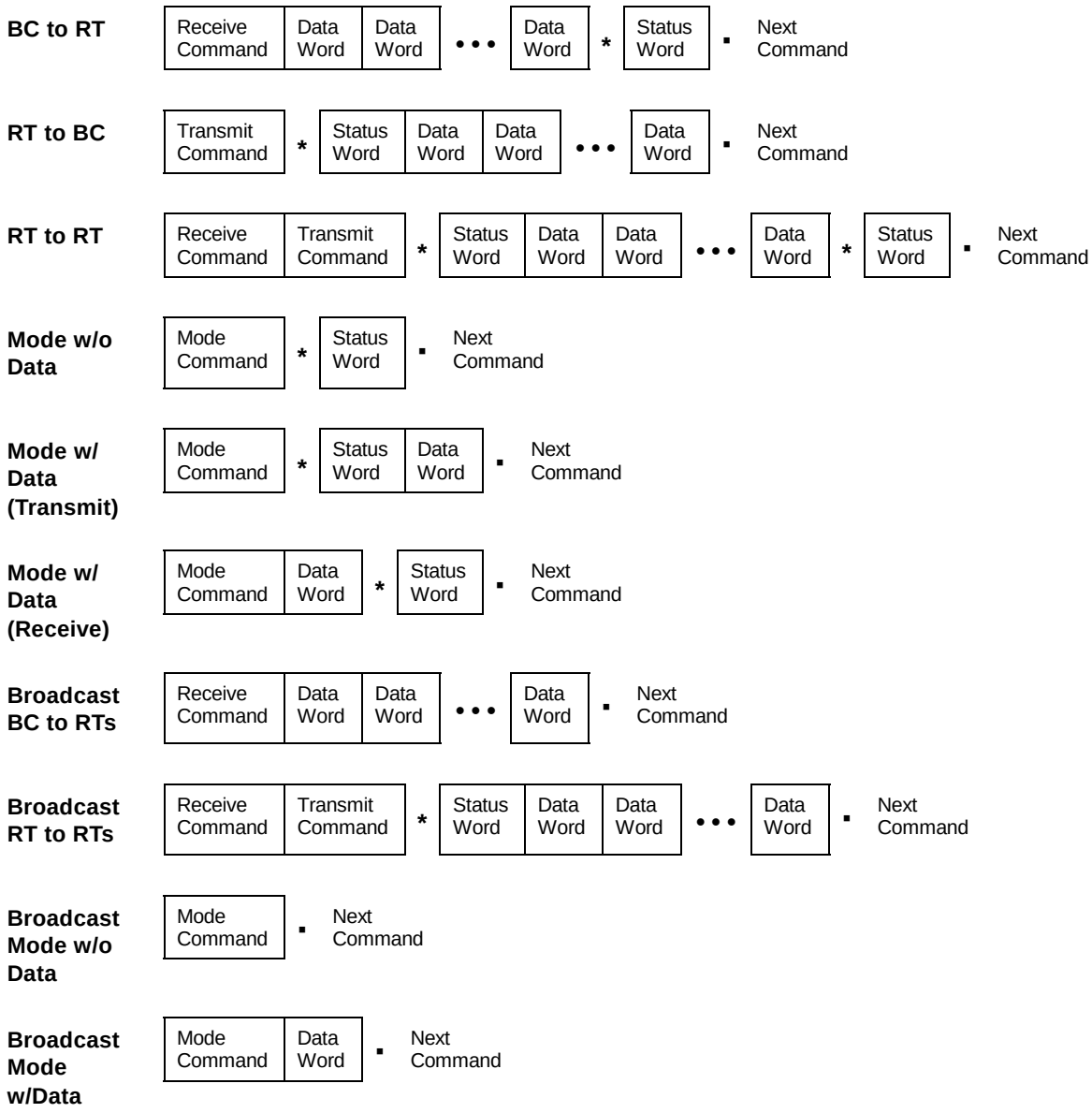


**Figure 11-2 MIL-STD-1553B Message Formats**

NOTE: * = Response time
▪ = Intermessage gap



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# Appendix C Internal Loopback Test

The Internal Loopback Test is used to check the 1553 front-end logic, excluding transceivers and coupling transformers.

To initiate the Internal Loopback Test:

1. Write ED (H) into the Board Configuration Register.
2. Write 1 into the Start Register.
3. Wait for 0 in the Start Register.

The results of this test are returned to the host in dual-port RAM using the following structure beginning at address 0:

struct I_LOOPBACK

{

| Definition | | Address in Dual-Port RAM | Status Value |
|---|---|---|---|
| usint frame_val; | | 0 | X (not for user) |
| usint frame_status; | frame time counter status | 2 | 8000H passed, 8001H failed |
| usint resp_status; | response time counter status | 4 | 8000H passed, 8001H failed |
| usint early_val; | | 6 | 6 LSB must be 15H |
| usint receive_data1; | first looped word test, using command sync | 8 | 5555H |
| usint status_1; | | A | 8000H passed, else failed |
| usint receive_data2; | second looped word test, using data sync | C | AAAAH |
| usint status_2; | | E | 8000H passed, else failed |
| usint mc_status; | mode code function test | 10 | 8000H passed, else failed |
| usint ttag_val_lo; | | 12 | 30D4H ± 2 |
| usint ttag_val_hi; | | 14 | 0 |
| usint ttag_status; | time tag status | 16 | 8000H passed, 8001H failed |
| usint prl; | | 18 | 8 LSB contain the CPU version |

} *I_loopback;



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# Appendix D External Loopback Test

The External Loopback Test is used to check the 1553 transceivers, transformers and associated bus cables.

**NOTE** The External Loopback Test requires a loopback cable to connect bus A to bus B.

To initiate the External Loopback test:

1. Write FF (H) into the Board Configuration Register.
2. Write 1 into the Start Register.
3. Wait for 0 in the Start Register.

The results of this test are returned to the host in dual-port RAM using the following structure beginning at address 0:

struct E_LOOPBACK

{

| | Definition/ conditions for passing E_loopback test [ TX-bus, RX-bus, command or data sync] | Address in Dual-Port RAM | Status Value |
|---|---|---|---|
| usint frame_val; | | 0 | X (not for user) |
| usint frame_status; | frame time counter status | 2 | 8000H passed, 8001H failed |
| usint cmd_send[8]; | | 4 | cmd_send[0]: 5555H |
| | TX-A, RX-A, command sync | 6 | cmd_send[1]:8000H passed, else failed |
| | | 8 | cmd_send[2]: 1234H |
| | TX-A, RX-B data sync | A | cmd_send[3]:8000H passed, else failed |
| | | C | cmd_send[4]: 5555H |
| | TX-B, RX-A command sync | E | cmd_send[5]:8000H passed, else failed |
| | | 10 | cmd_send[6]: 1234H |
| | TX-B, RX-B data sync | 12 | cmd_send[7]:8000H passed, else failed |
| usint ttag_val_lo | | 14 | 30D4H ± 2 |
| usint ttag_val_hi | | 16 | 0 |
| usint ttag_status; | time tag status | 18 | 8000H passed, 8001H failed |

} *E_loopback;



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