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Find the *Excalibur Systems EXC-1553VXI/E-V-NM* at our website: *Click HERE*

MIL-STD-1553 TEST AND SIMULATION BOARDS

FOR VME AND VXI COMPUTERS

FEATURES

* OPERATES AS BC,RT,BC/CONCURRENT-RT AND TRIGGERABLE CONCURRENT BUS MONITOR
* MULTIPLE PROTOCOL COMPATIBILITY (i.e. MIL-STD-1553 A,B,F-16, MaCair)
* HANDLES 4 µsec INTERMESSAGE GAP TIMES IN ALL MODES
* ERROR INJECTION CAPABILITY:
  - BIT COUNT
  - WORD COUNT
  - INCORRECT SYNC
  - PARITY
  - INCORRECT RT ADDRESS
  - NON-CONTIGUOUS DATA
  - ZERO CROSSING/MANCHESTER ERRORS
* OPTIONAL `WPG' PIGGYBACK FOR EXTENSIVE ERROR INJECTION (50nsec RESOLUTION) IN BC
* MULTI-MODE TRIGGERABLE MONITOR
* COMPATIBLE WITH VME AND VXI COMPUTERS
* MULTIPLE-RT SIMULATION (UP TO 32 REMOTE TERMINALS)
* PROGRAMMABLE BROADCAST MODE
* MEMORY-MAPPED, DUAL-PORT 64Kx8 RAM INTERFACE
* "B" AND "C" SIZE CARDS
* EASY TO INSTALL AND OPERATE
* REAL-TIME OPERATION
* NO SOFTWARE DRIVER REQUIRED
* EXTENSIVE INTERRUPT FEATURES

The EXC-1553VME/E-V is an intelligent MIL-STD-1553 interface card for VME and VXI computers. It facilitates the testing and simulation of the MIL-STD-1553 bus. Various 1553 protocols are handled by the card. The user has direct access to all control registers and data blocks. The user controls the operation of the card by accessing the memory-mapped control registers. The EXC-1553VME/E-V contains a 64Kx8 dual-ported RAM for data blocks, control registers, and look-up tables. The EXC-1553VME/E-V is also available without Concurrent Monitoring capability (see Ordering Information).

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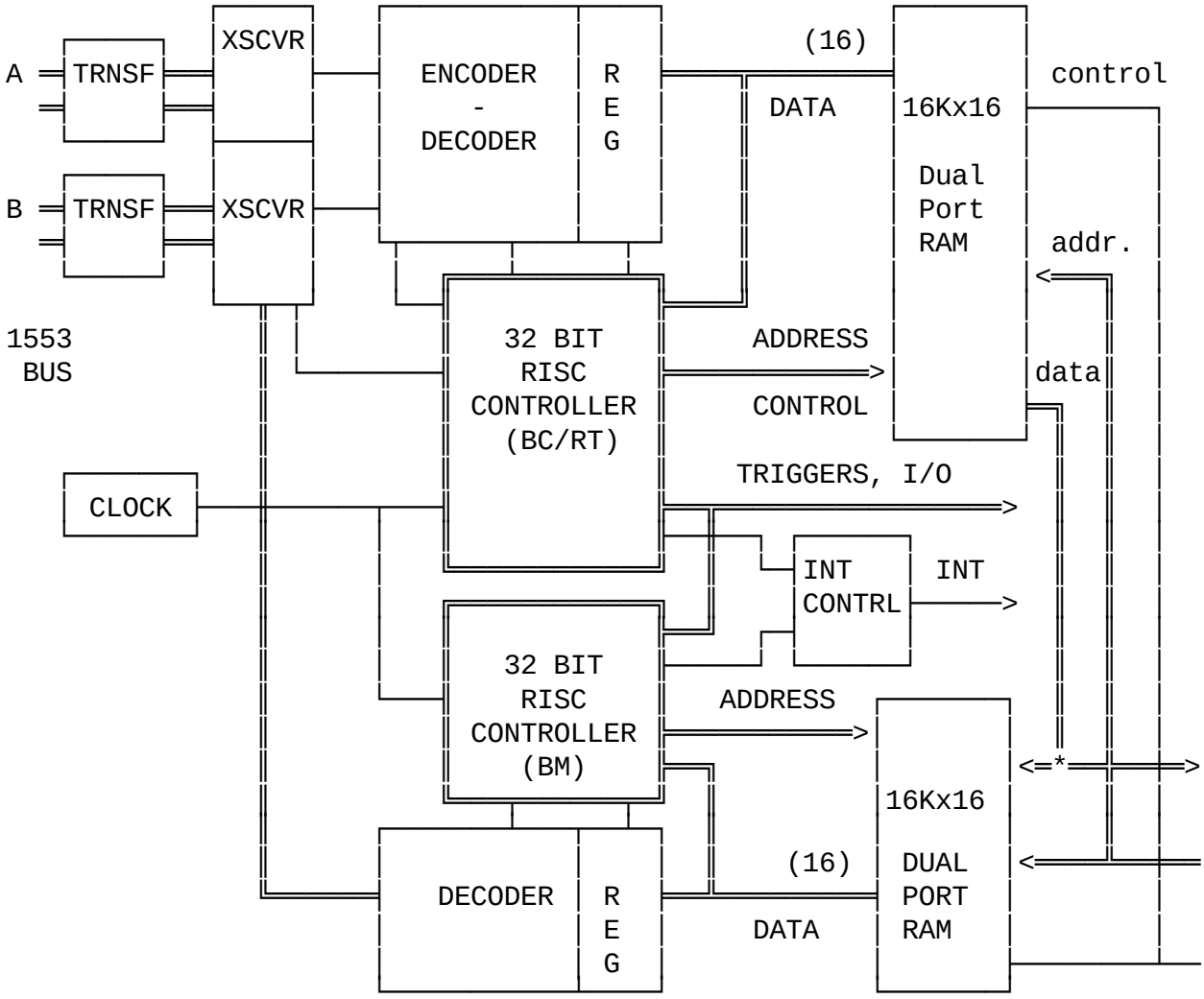
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INTRODUCTION

The EXC-1553VME/E-V and the EXC-1553VXI/E-V are memory-mapped MIL-STD-1553 interface cards which operate within VME and VXI systems. The name "EXC-1553VME/E-V" will be used as a generic name throughout this document and denotes both boards. The EXC-1553VME/E-V is the perfect solution for developing and testing 1553 interfaces and for performing system simulation of the 1553 bus. The user has access to all control registers and can modify various parameters and data in real time. The board has four modes of operation: Bus Controller, Remote Terminal (Multiple - up to 32 RT's), BC with Concurrent RT operation, and a [CONCURRENT] Bus Monitor. 32Kx8 of true, dual-port RAM is allocated for the BC, RT, and BC/Concurrent RT modes. An additional 32Kx8 of true, dual-port RAM is allocated for the Bus Monitor.
Note that the EXC-1553VME/E-V is also available without the Bus Monitor function ("-NM" suffix, see Ordering Information). All sections of this manual relating to Monitor Mode operation should be ignored by users of the "-NM" boards.

Figure 1 shows the block diagram of the EXC-1553VME/E-V card.



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Figure 1. EXC-1553VME/E-V BLOCK DIAGRAM

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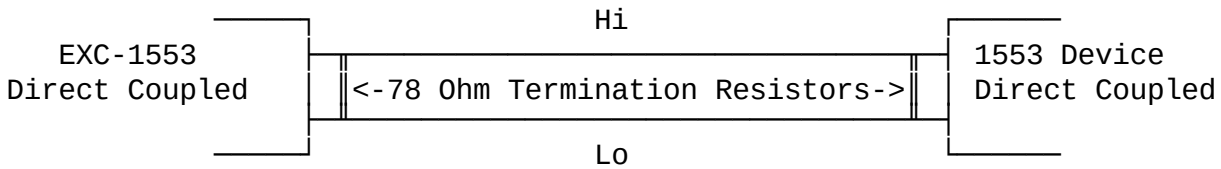
INSTALLATION

Before installing the card it is very important to determine which 64 byte section of A16 address space is available for the cards VME/VXI Configuration Registers. When this is determined, the SW3 dipswitch should be set accordingly (see dipswitch section for instructions on setting the dipswitch). The user should also decide if A24 or A32 address space is to be used and set the appropriate jumper (JP2).

1553 devices may be connected to the 1553 bus either directly (Direct Coupled) or via a bus coupling stub (Transformer Coupled). Dip switches SW1 and SW2 must be used to inform the card which coupling method is being used for each bus the card is connected to.

1553 BUS CONNECTIONS

For short distances, direct coupling may be used to connect the EXC-1553VME/VXI directly to another 1553 device. The user must make certain that the cable connecting the two devices is properly terminated with 78 Ohm resistors to insure data integrity (see illustration).



One Bus Shown

For users wishing to operate in the more standard Transformer Coupling mode, stub coupler devices are available from a number of manufacturers. North Hills Electronics, Inc. supplies a three stub coupler (PN# DB30010) as well as 78 ohm terminators (PN# RT500078). Two terminators are required for each coupler which services a single bus (e.g. BUS A).

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VME/VXI INTERFACE

The board interfaces to the computer via a 16-bit data bus which can be accessed in bytes or words. The board may be accessed by using addresses in the form:

For accessing VME/VXI Configuration registers:

XXXX (H) (A16 mode) with ADDRESS MODIFIER CODES: 29, 2D

For accessing Data Storage Area and Control Registers:

XX XXXX (H) (A24 mode) with ADDRESS MODIFIER CODES: 39, 3A, 3D, 3E
or
XXXX XXXX (H) (A32 mode) with ADDRESS MODIFIER CODES: 09, 0A, 0D, 0E

The memory map is divided into two distinct blocks:

1. VME/VXI Configuration Registers.
2. 1553 Message Storage Area and Control Registers.

The VME/VXI Configuration Registers are used for setting up the board within the user's VME or VXI system. The 1553 Message Storage Area and Control Registers are used to control the operation of the board on the 1553 bus.

VME/VXI Configuration Registers

The VME/VXI Configuration registers are located within a 64 byte block in the A16 address space between the addresses 49152 (dec.) and 65472 (dec.). The base address of the Configuration registers is determined by the following equation:

```
Base Address (dec.) = V*64 + 49152 (dec.)
```

V, the "Logical Address" of the card, is an integer which varies between 0 and 255 and is defined by the user via the 8 pole dipswitch SW3 (see the section on dipswitch setup at the end of this manual). In order to ensure correct operation of the board within the user's VME or VXI system the Configuration registers must be (re-)initialized after power up or after assertion of SYSRESET*. For a full explanation of the VXI Configuration registers and other topics relating to

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operation of the VXI bus refer to the "VXI Bus System Specification".

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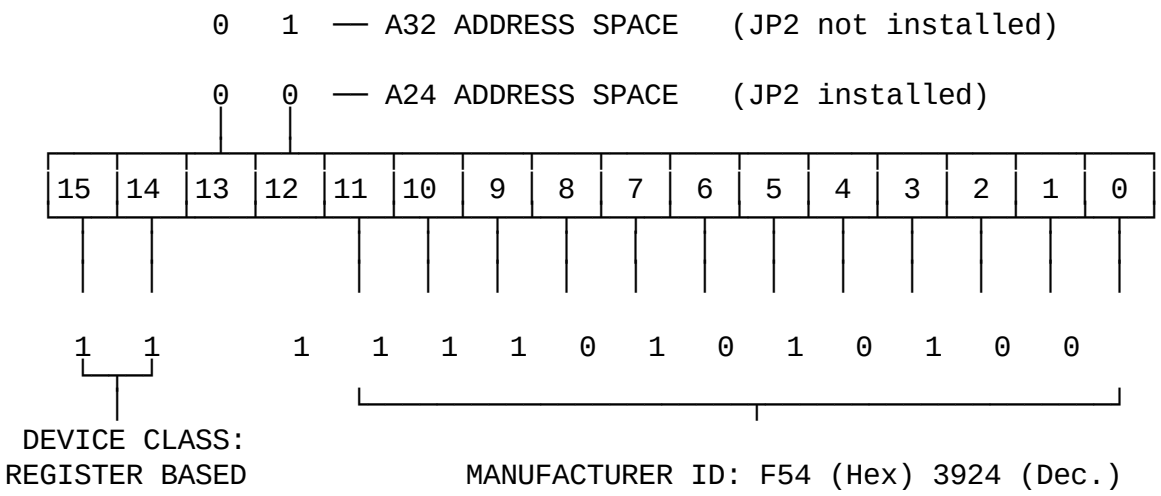
Configuration Register Memory Map

IDVECTBM	BASE + 22 (H)
IDVECTBCRT	BASE + 20 (H)
OFFSET REGISTER	BASE + 06 (H)
STATUS/CONTROL REGISTER	BASE + 04 (H)
DEVICE TYPE	BASE + 02 (H)
ID REGISTER	BASE + 00 (H)

ID REGISTER (VXI only)

BASE + 00 READ ONLY

The contents of this 16-bit register provides the following information about the board's configuration.

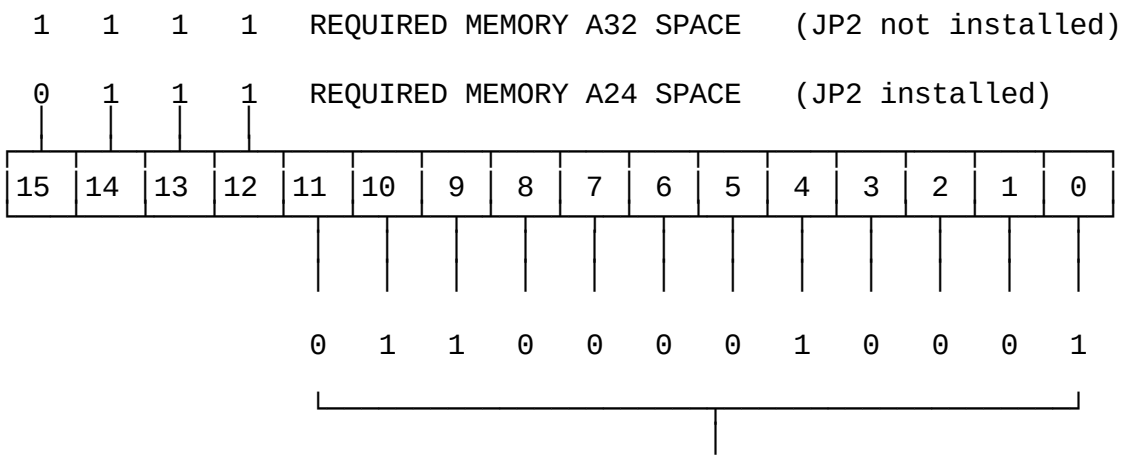


Note: This register contains the same value whether set up for VME or VXI installation. The VXI specification requires all VXI devices to identify themselves via an ID register. This location is not defined under the VME specification.

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DEVICE TYPE REGISTER (VXI only)	BASE + 02 READ ONLY

This 16 bit register contains a fixed Device Type Identifier as well as a four bit field which reflects the Required Memory usage of the card.



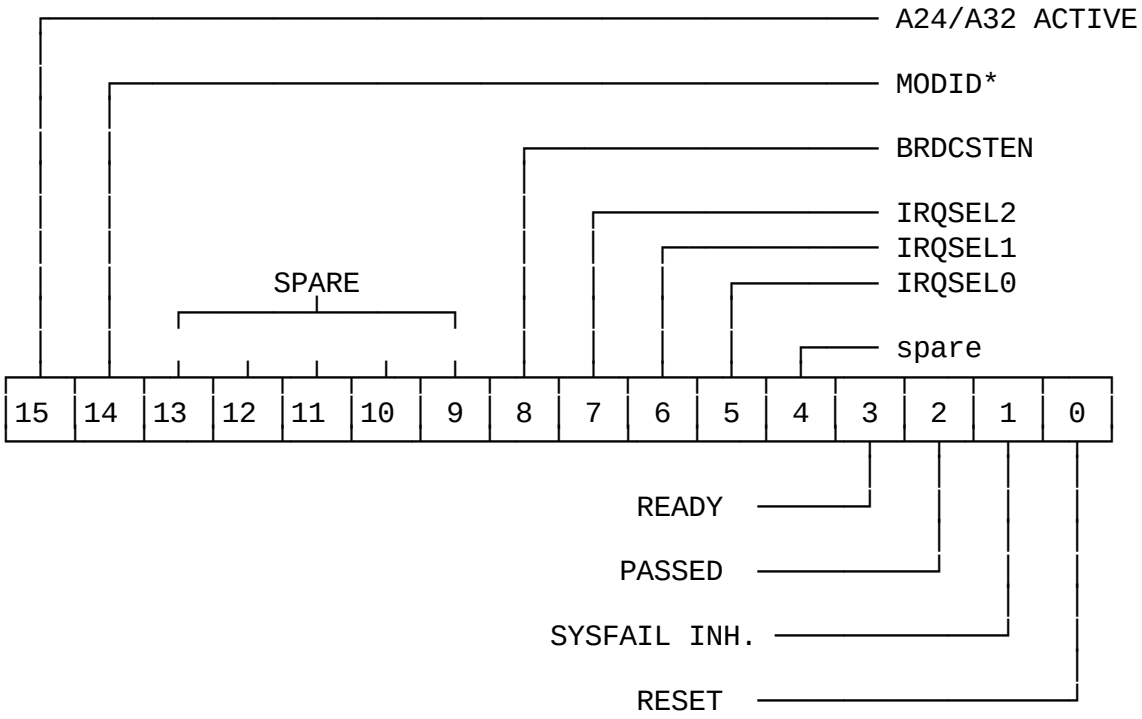
MODEL CODE: 611 (Hex) 1553 (Dec)

Note: This register contains the same value whether set up for VME or VXI installation. The VXI specifications requires the user to let the system know how much memory the device requires. This is known as the 'm' value in VXI parlance. This location is not defined under the VME specification.

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STATUS REGISTER (VXI and VME)	BASE + 04 READ ONLY

A read of this 16 bit register provides information as defined below.



Note: The READY, PASSED, SYSFAIL INHIBIT and RESET functions are included to maintain compliance with the VXI specification. It is recommended that VME users make use of the software reset (Card Initialization) handshake mechanism described in the main body of this manual.

RESET	Indicates the state of the RESET bit in the Control Reg.
SYSFAIL INHIBIT	Indicates the state of the SYSFAIL INHIBIT line in the Control Register.
PASSED	Upon powerup a "0" indicates that the card is either executing or has failed it's self test. A "1" indicates that the self test has successfully completed. Upon software reset this bit will be "1" during self test and "0" only if it fails the test.
READY	A "1" indicates that the power up sequence has completed and that the card is ready to accept commands
IRQSEL 2-0	Indicates the state of the IRQSEL2-0 bits in the Control Register
BRDCSTEN	Indicates the state of the BRDCSTEN bit in the Control Reg.
MODID*	Indicates the inverted value of the VXI bus "MODID" line.

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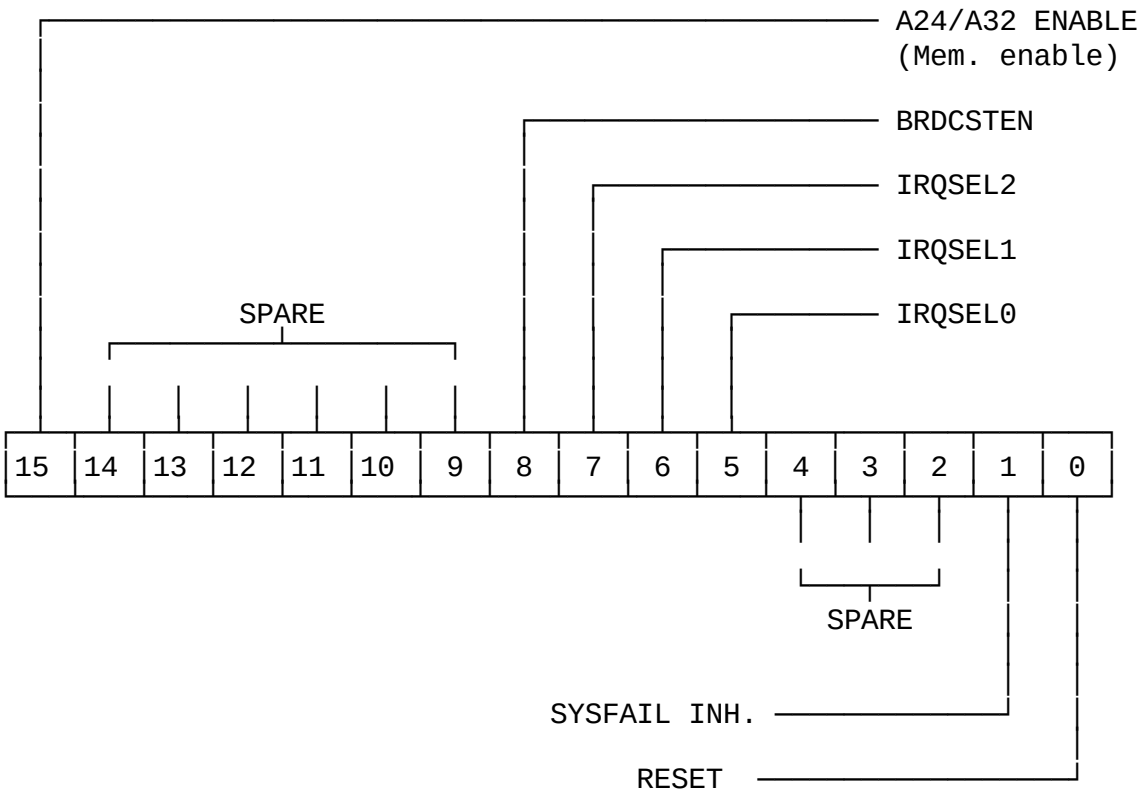
A24/A32 ACTIVE	Indicates the state of the A24/A32 ENABLE bit in the Control Register.

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CONTROL REGISTER (VXI and VME)

BASE + 04 WRITE ONLY

Writing to this 16-bit register causes the actions listed below to be executed by the card. Note that all bits in this register are set to "0" after assertion of VME bus line SYSRESET*.



RESET

Writing a "1" to this bit forces the card into the "RESET" state. The user must not write a "0" into this bit for at least 100 microseconds after writing a "1" into it. That is, once in the "RESET" state, the card must remain in this state for at least 100 usec. While in the "RESET" state the card is completely inactive and will not respond to any commands. Upon releasing the card from the "RESET" state (write "0" to this bit), the card will perform its self test routines. The board may also be reset via the Card Initialization Register defined within the main body of this manual. This second method is the preferred mechanism for resetting the card.

SYSFAIL INHIBIT

If JP1 is shorted (see Jumpers) writing a "1" to this bit disables the card from driving the VME bus line SYSFAIL*, otherwise it has no effect.

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IRQSEL 2-0

Writing to these bits selects which one of the VME bus Interrupt Request lines IRQ1* -- IRQ7* will be driven active when the card generates an interrupt. The following table shows the relationship between IRQSEL 2—0 and IRQ7-1.

SELECTED INTERRUPT LINE	IRQSEL2	IRQSEL1	IRQSEL0
NONE	0	0	0
IRQ1*	0	0	1
IRQ2*	0	1	0
IRQ3*	0	1	1
IRQ4*	1	0	0
IRQ5*	1	0	1
IRQ6*	1	1	0
IRQ7*	1	1	1

NOTE: USING INTERRUPTS

The Interrupt generated on the selected IRQ* line is the "logical OR" of all interrupt generating sources on the card. An interrupt which was generated by the BM will result in the interrupt routine whose vector resides in IDVECTBM to be executed. The card will place the value in the IDVECTBM register, called the STATUS/ID, onto the VME data lines when issuing the interrupt. The user's processor will use this value to determine which entry in the user's interrupt vector table to jump to. Within this interrupt routine the actual source of the interrupt can be determined by polling the Message Status register. Likewise, an interrupt which was generated by the BC or RT or BCRT will result in the interrupt routine whose vector resides in IDVECTBCRT to be executed. Within this interrupt routine the actual source of the interrupt can be determined by polling the Message Status register.

If both the BM and the BCRT generate interrupts simultaneously, the BCRT has higher priority and its STATUS/ID will appear first. After the user services the interrupt request for the BCRT, a second interrupt will be generated for the BM.

For all interrupts, the interrupt request is cleared automatically at the end of the interrupt acknowledge cycle. This method is referred to within the VME specification as ROAK (Release on AcKnowledge).

BRDCSTEN (1553 Broadcast option enable)

Writing a "1" to this bit enables the 1553 bus "BROADCAST" function in RT mode. When enabled the RT Address "11111" represents a "BROADCAST" Command. Writing a "0" disables the "BROADCAST" function and RT Address "11111" is treated as a valid RT Address in RT mode.

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A24/A32 ENABLE

(Memory enable)

Writing a "1" to this bit enables access to the card's A24 or A32 VME bus registers and memory. If this bit is set to "0" none of the on card registers and memory which are resident in the A24 or A32 address spaces may be accessed. The Configuration registers, of course remain accessible regardless of the state of this bit, as they reside in the A16 address space of the card.

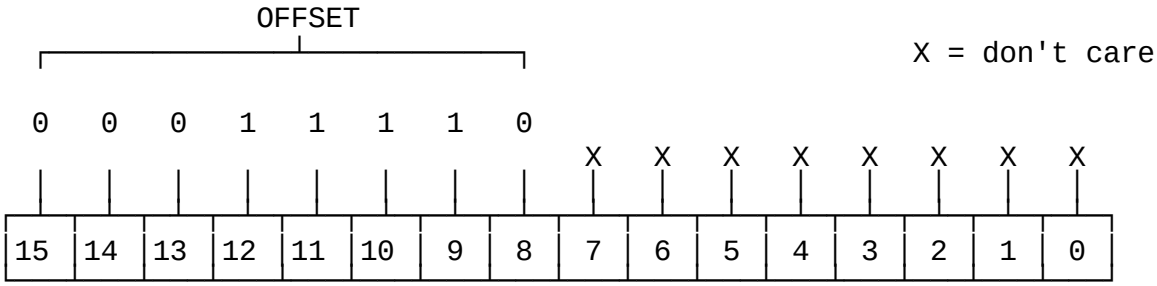
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OFFSET REGISTER (VXI and VME) BASE + 06 READ/WRITE

This 16 bit read/write register defines the base address of the card's A24 and A32 memory and registers. If A24 addressing is used the 8 most significant bits of the Offset register are the values of the 8 most significant bits of the card's memory and register addresses and the 8 least significant bits of the register are not used. If A32 addressing is used the Offset register represents the 16 most significant bits of the card's memory and register addresses. Thus, the Offset register bits 15 through 8 map to the address lines A23 through A16 for the A24 Address Space, and to lines A31 through A16 for the A32 Address Space.

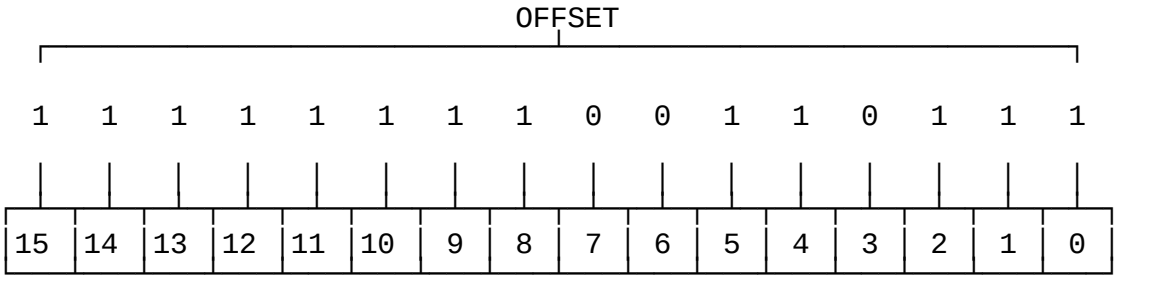
A24 ADDRESSING EXAMPLE

required base address = 1E 0000 H;
write 1E H to Offset register



A32 ADDRESSING EXAMPLE

required base address = FF37 0000 H;
write FF37 H to Offset register

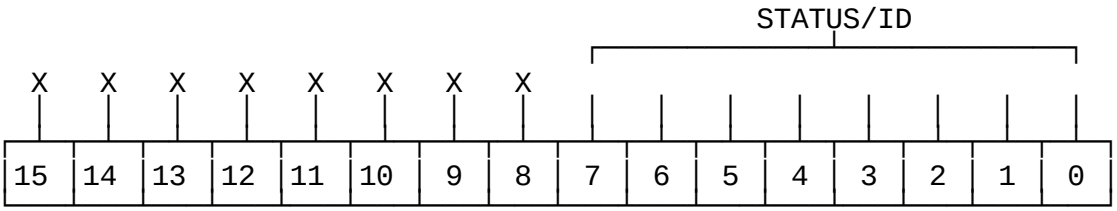


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IDVECTBCRT REGISTER (VXI and VME)

BASE + 20(H) READ/WRITE

In the case of an interrupt generated by the BUS CONTROLLER, REMOTE TERMINAL, or BUS CONTROLLER CONCURRENT REMOTE TERMINAL, the 8 least significant bits of this 16 bit register, known as the STATUS/ID, are used as the interrupt vector during the ensuing interrupt acknowledge cycle. The card is a D08(0) INTERRUPTER, and as a result will place these 8 bits on lines D00-D07 of the VME bus during the interrupt acknowledge cycle.

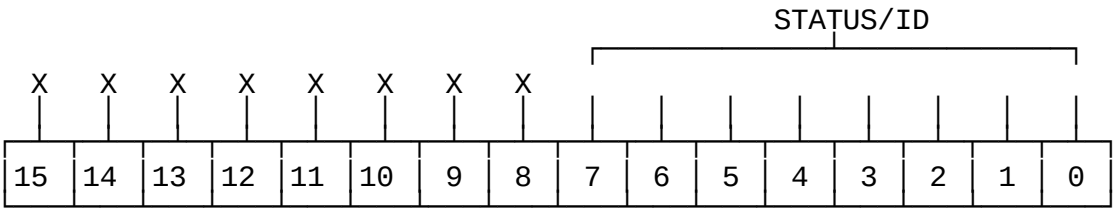


X = don't care

IDVECTBM REGISTER (VXI and VME)

BASE + 22(H) READ/WRITE

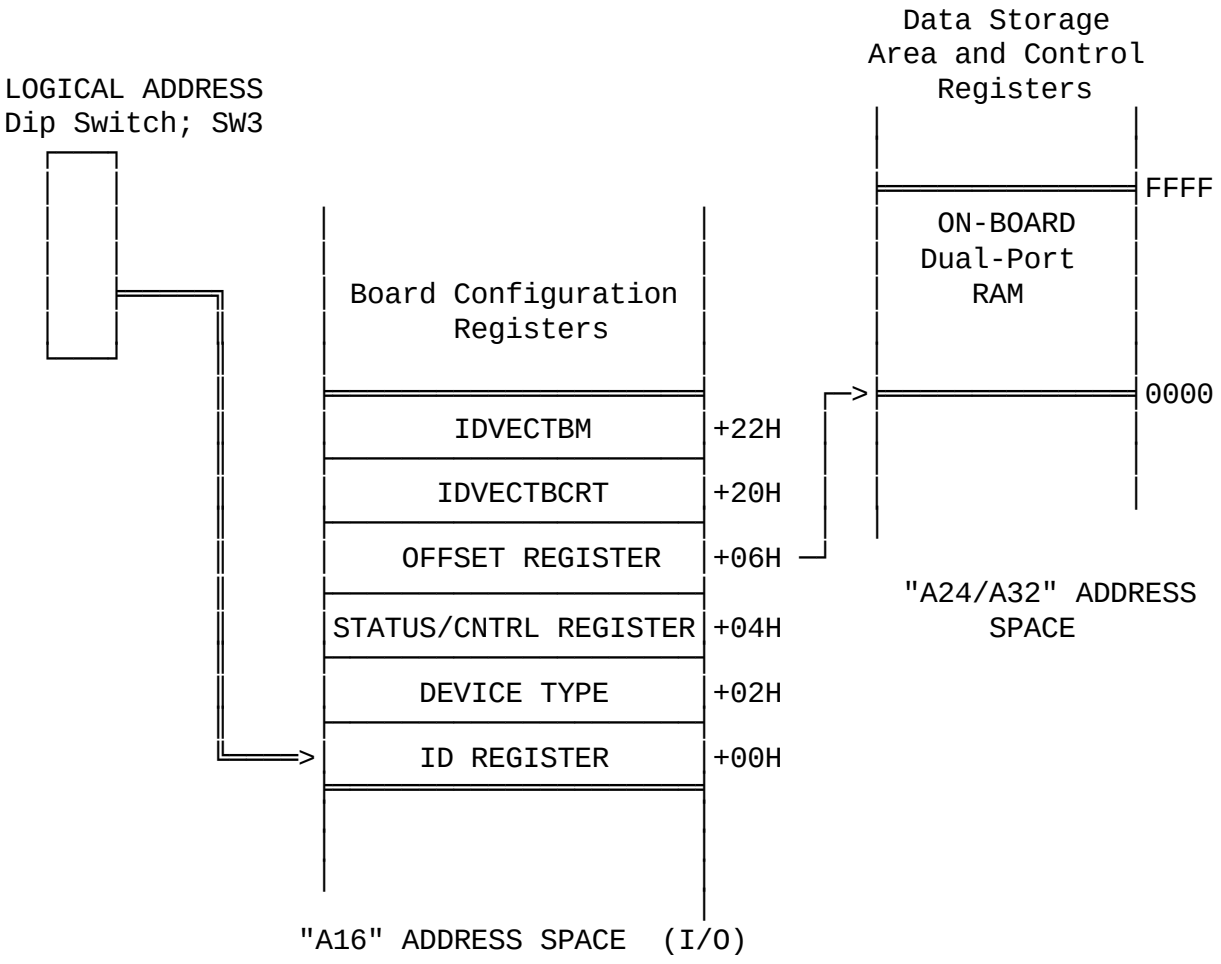
In the case of an interrupt generated by the BUS MONITOR the 8 least significant bits of this 16 bit register, known as the STATUS/ID, are used as the interrupt vector during the ensuing interrupt acknowledge cycle. The card is a D08(0) INTERRUPTER, and as a result will place these 8 bits on lines D00-D07 of the VME bus during the interrupt acknowledge cycle.



X = don't care

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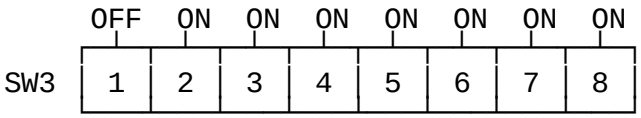
DUAL-PORT RAM ADDRESS MAPPING DIAGRAM



A16 ADDRESSING EXAMPLE

Given:
Required configuration registers base address = E000(H)

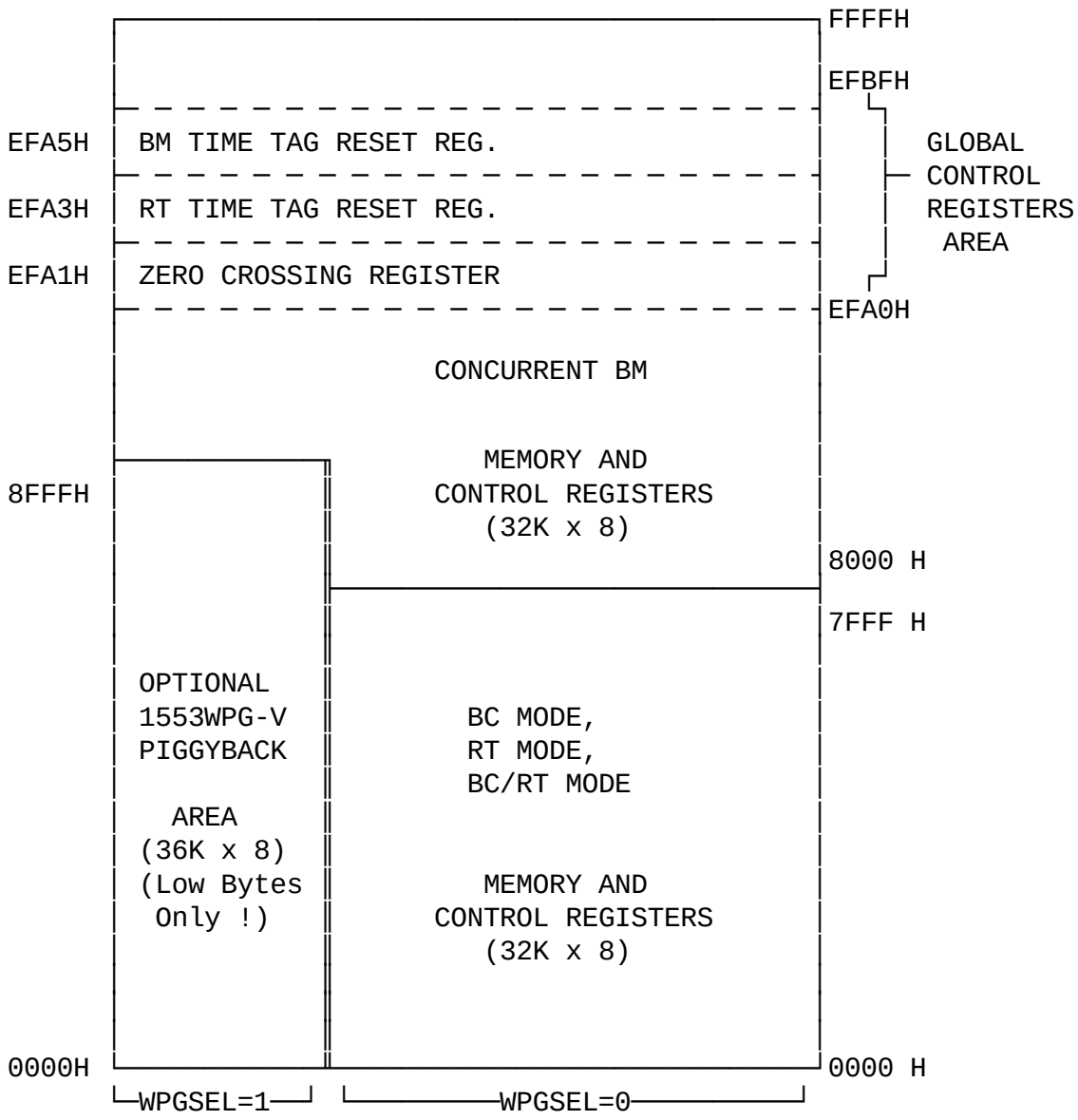
Then:
Set dip-switch SW3 to LOGICAL ADDRESS = 80(H)



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GENERAL MEMORY MAP

The board occupies 64Kx8 of the VME A24 or A32 memory map, which are mapped via the Offset Register within the VME/VXI Configuration Registers. Note that the optional Word Pattern Generator (1553WPG-V) is also accessed at this area. For more information regarding the 1553WPG-V refer to the section describing the WPGSEL bit within the Zero Crossing Register and to the section "Optional 1553WPG-V Piggyback".



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1553 Message Storage Area and Control Registers

The 1553 Message Storage Area and Control Registers reside in 32Kx16 of true dual-port RAM. It is within this 32K of dual-port RAM that the user controls the operation of the card on the 1553 bus. The 32Kx16 RAM may be further divided into two blocks of 16kx16. The first block is used in the BUS CONTROLLER (BC), REMOTE TERMINAL (RT), and BUS CONTROLLER CONCURRENT REMOTE TERMINAL (BC/RT) modes of operation, and the second block of 16Kx16 RAM is used only in the BUS MONITOR (BM) mode of operation. It should be noted that the BUS MONITOR operates independently of the other three modes of operation and the user may choose to disable it or enable it alone or with either one of the BC, RT, BC/RT modes of operation.

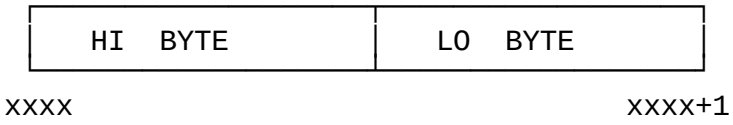
When accessing the 1553 message and data areas, it is recommended that the user use word addressing as is the case with 16-bit control registers. When accessing 8-bit control registers, it is recommended that the user use byte addressing since there is a possibility of inadvertently overwriting a byte-wide register (which resides next to the desired register) when using 16-bit word addressing.

All 16-bit words (1553 words and 16-bit control registers) contained within the board's dual-port RAM are stored in the following manner:

* The HI byte is accessed at EVEN addresses, while the LO byte is accessed at ODD addresses. *

Example

The Bus Controller's Stack Pointer is located at address : xxxx



Note that all addresses listed in the remainder of this document are given relative to the Base Address written by the user into Offset Register as described in "Configuration Registers".

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BC MODE OPERATION

In the BC mode, the EXC-1553VME/E-V can be programmed to transmit multiple messages in either a "one-shot", "N-times" or in a "loop" mode. Errors can be injected into the messages on a message-by-message basis. In addition, the user can pre-program the inter-message gap time of each message.

The user programs the message transfers by loading a [relocatable] stack with instructions. Each instruction block contains four words. Many instruction stacks can be created and reside simultaneously within the dual-port memory. The user simply points to the "active" instruction stack by programming the instruction Stack Pointer. The card contains 16Kx16 of true, dual-port RAM which is allocated for the BC mode.

The EXC-1553VME/E-V can operate within different 1553 protocol environments (e.g. MIL-STD-1553 A, B, F-16, and MaCair). This flexibility emerges from the extensive programmability of the 1553-related parameters such as Response Time, Status Word content, etc.

NOTE:

The user should use the following sequence to determine whether the board is installed AND ready to operate:

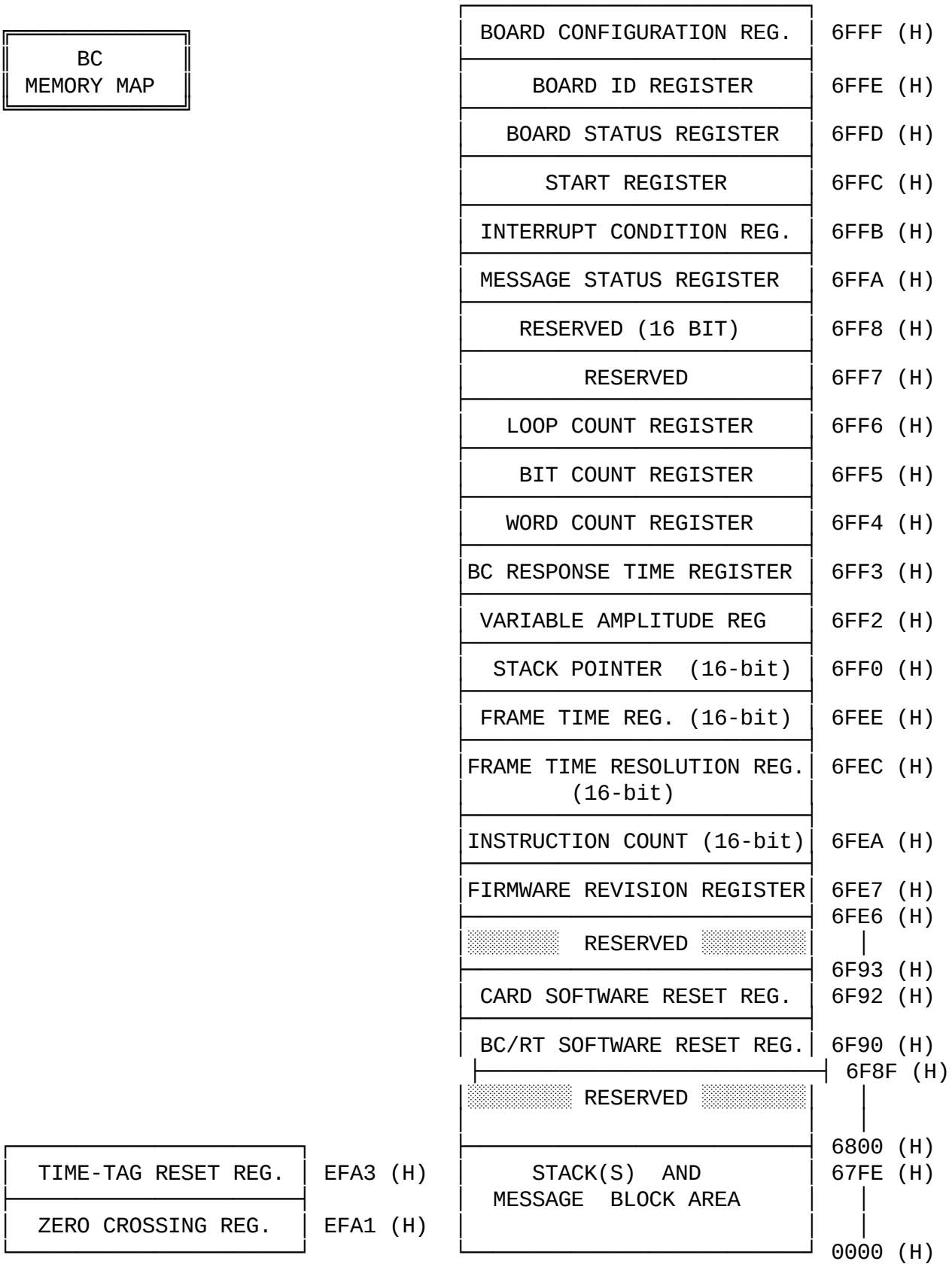
* Check the Board ID register (test for value = 45 Hex)

* Check Board Status Register (test for Board Ready bit = "1")

The board is installed and ready when BOTH of these registers contain the correct values (as written above). This sequence should be used after power-on and Software Reset operations. For Software Reset operations, these values should be set to ZERO by the user immediately prior to writing to the Initialization Register.

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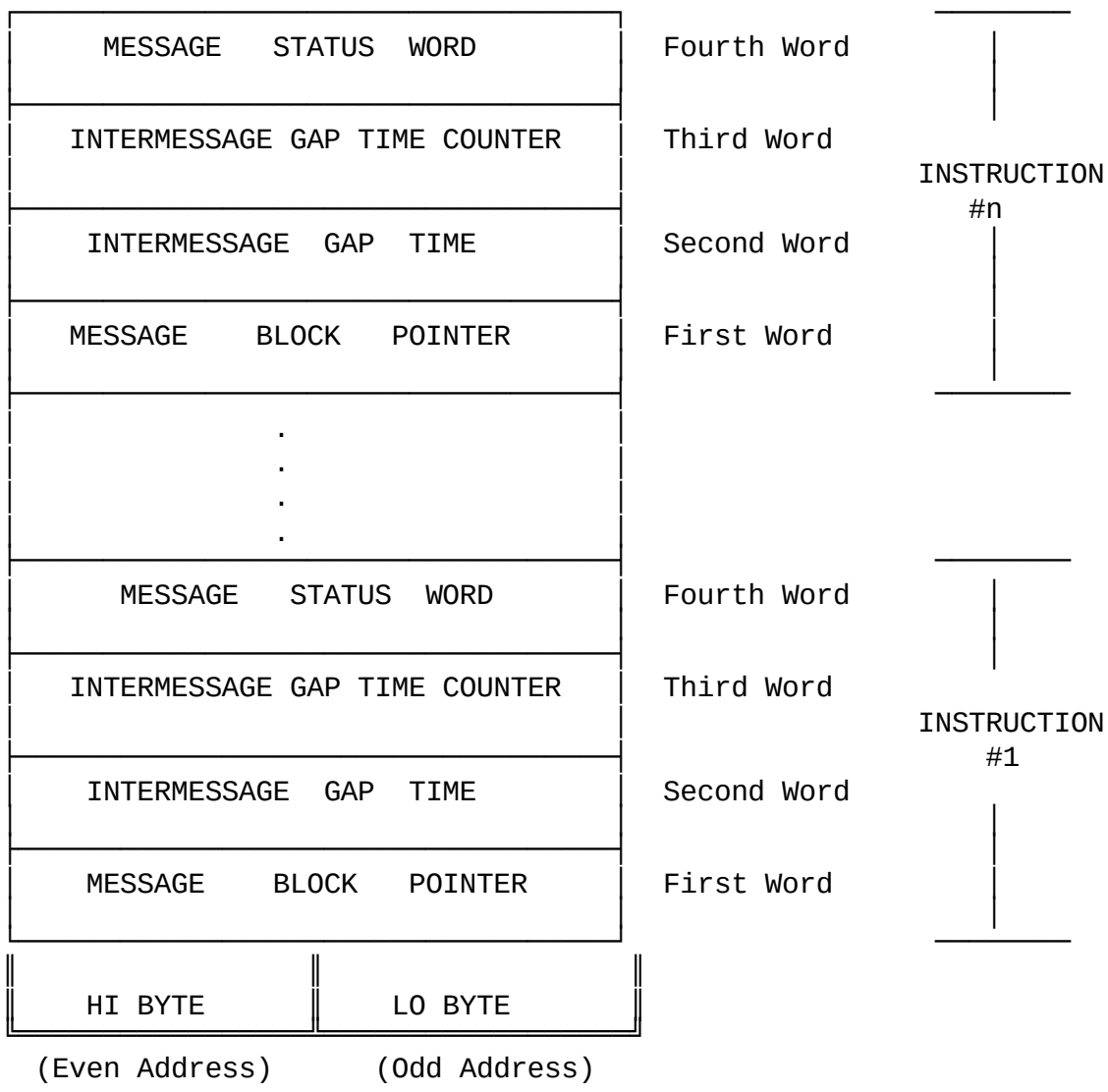
The figure below shows the memory map of the EXC-1553VME/E-V in the BC Mode of operation.



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INSTRUCTION STACK

The user programs the EXC-1553VME/E-V via the Instruction Stack. The stack is divided into instruction blocks - each containing four words. Each block relates to one 1553 message transfer. The block contains "control" information (written by the user) and status information (written by the board). The figure below illustrates the instruction blocks.

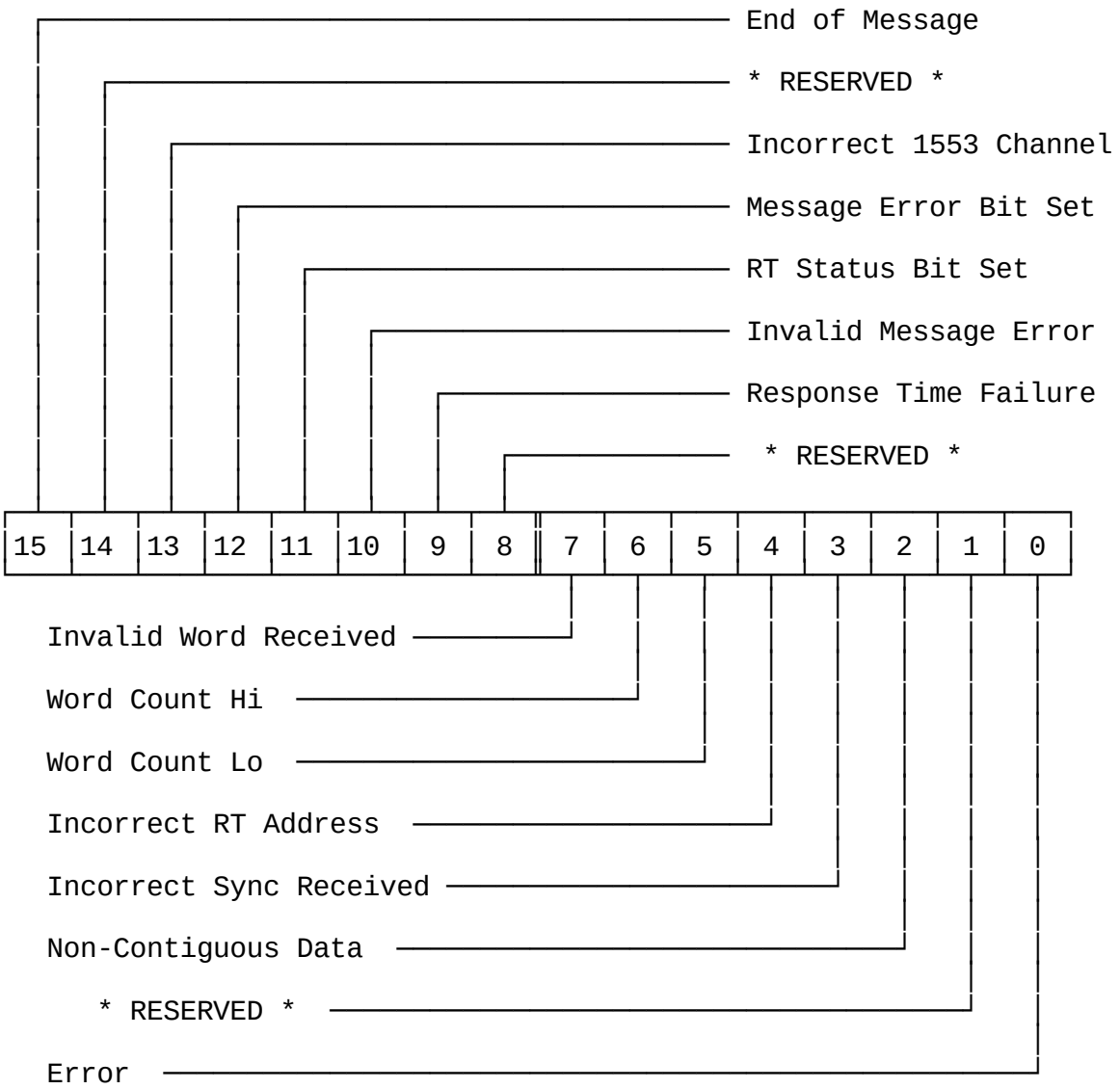


BC Mode

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MESSAGE STATUS WORD

The Message Status Word indicates the status of the message transfer. This word is created by the Board and is NOT the 1553 "STATUS WORD".
The contents of the Message Status word are shown below:



NOTE: A LOGIC "1" INDICATES AN "ACTIVE" CONDITION

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Message Status Word Definitions:

15	END OF MESSAGE	Indicates that the message transfer has been completed
14	RESERVED	Set to logic '0'
13	INCORRECT CHANNEL	Indicates that the remote terminal response was not received on the active 1553 channel
12	MESSAGE ERR. BIT SET	Indicates the 'MESSAGE ERROR BIT' (bit '10') within the RT status word was set
11	RT STATUS BIT SET	Indicates that a bit was set within the RT status word (other than the 'MESSAGE ERROR BIT'). The ERROR bit is NOT set in conjunction with this bit.
10	INVALID MESSAGE	Indicates that a 1553 'message level' error occurred (i.e. Word count, incorrect sync) - detailed below
09	RESPONSE TIME ERROR	Indicates that the RT responded late (see: Programmable BC Response Time Register)
08	RESERVED	Set to '0'
07	INVALID WORD	Indicates the reception of at least one invalid 1553 word (i.e. Bit count, manchester code, parity)
06	WORD CT HI	Indicates that the RT transmitted too many words
05	WORD CT LO	Indicates that the RT transmitted too few words
04	INCORRECT RT ADDRESS	Indicates that the received 1553 status word did not contain the correct 'RT address'
03	INCORRECT SYNC	Indicates that the sync of either the status or data word(s) was incorrect
02	NON-CONTIGUOUS	Indicates occurrence of an invalid gap between received 1553 words
01	RESERVED	Set to logic '0'
00	ERROR	Indicates the occurrence of an error (defined within one of the other message status bit locations)

BC Mode

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Intermessage Gap Time	Written by user

The Intermessage Gap Time Value is a sixteen bit word which allows the user to insert a unique intermessage delay time between the current message and the next message. The minimum Intermessage Gap Time is approximately 4µsec measured as dead time on the bus. The value in the word is ADDED to this minimum time. The resolution of this word is 155 nanoseconds per bit.

Intermessage Gap Time Counter	Written by user

The Intermessage Gap Time Counter (IGT_Counter) is a sixteen bit word which allows the user to increase the Intermessage Gap Time by repeating the number of times the Intermessage Gap Time Value is used. If the counter equals "0", for example, the gap time is NOT repeated and is per the contents of the Intermessage Gap Time word. If the gap time counter equals "1" then the gap time is repeated once and equals the Intermessage gap time value x 2, etc.

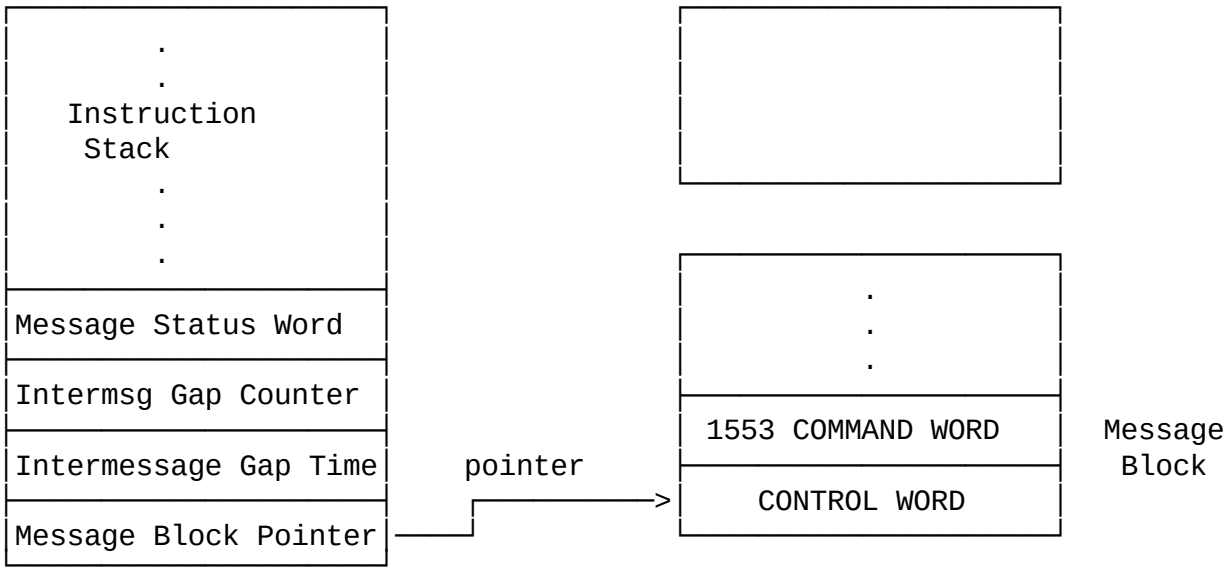
Note: To ensure maximum intermessage gap time accuracy when using the IGT_Counter, the value within the Intermessage Gap Time Word should be maximized and that within the IGT_Counter minimized, for a given desired intermessage gap time.

Message Block Pointer	Written by user

The Message Block Pointer is a sixteen bit word which points to the beginning of a 1553 Message.

Example :

(1) User writes message starting at address: 1000 (H)
(2) write 1000 (H) to the Message Block pointer location.



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The user loads the Message Block anywhere within the Instruction Stack/Message Block Area (see: BC Memory Map). Message Blocks do NOT have to be stored in sequential locations within the memory since the Message Block Pointers "point" to the Message Blocks in sequence.

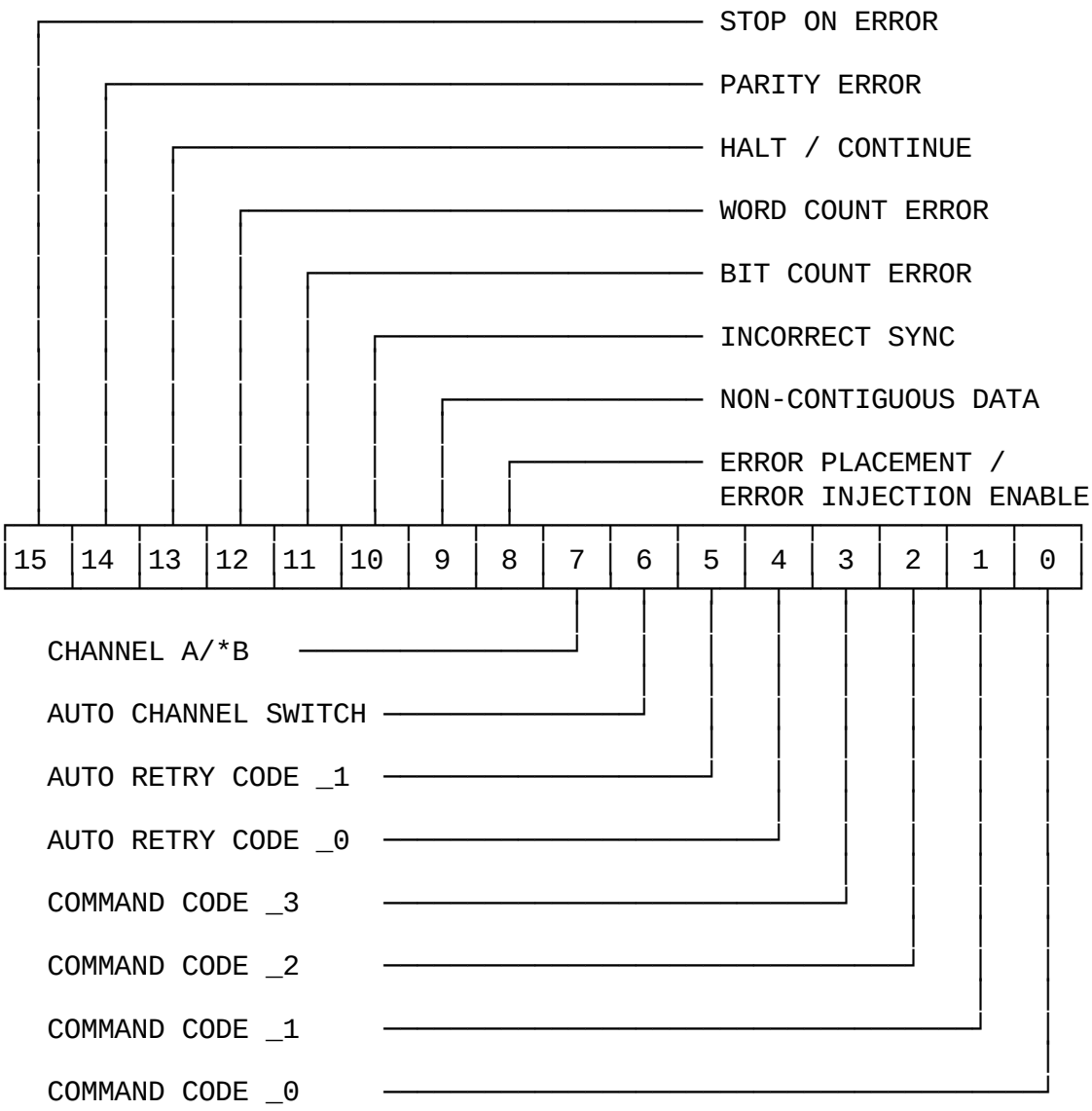
Each block contains a 1553 message plus its Control Word. This Control Word is written into the first word of each block. The Control Word instructs the EXC-1553VME/E-V as to the type of message to be transmitted (i.e. RT to RT, Mode Code, Broadcast, Error injection, etc.). The size of the message block is not fixed and is dependent upon the size of the message itself.

The description of the various message block formats (ie BC to RT, RT to BC and RT to RT) are illustrated in the section titled "Message Block Formats".

The description of each bit within the Control Word follows.

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Control Word



NOTE : A LOGIC "1" ENABLES THE FUNCTION, A "0" DISABLES THE FUNCTION.

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Control Word Definitions:

15	Stop on Error	Message error stops the BC operation. The user can restart by writing to the instruction count and "START".
14	Parity Er	Selects 'Even' parity within 1553 word
13	Halt / Continue	1= HALT. This stops BC transfer operation. This bit MUST BE reset ('0') in order to RUN or CONTINUE. (see text)
12	Word Count Error	Transmits fewer or more words than are indicated by the WORD COUNT field (see: Word Count Register). This function is valid for 'BC to RT' messages only.
11	Bit Count Error	Transmits invalid number of bits within 1553 words (see: Bit Count Register)
10	Incorrect Sync	Transmits incorrect sync. Data-type sync is transmitted within the command word
09	Non-Contg Data	First 1553 data word is transmitted with invalid gap time (between command and data word)
08	Error Placement / Error Injection Enable	For BC to RT, BROADCAST RECEIVE and MODE CODE with DATA messages, this bit selects the 'Parity', 'Sync' and 'Bit Count' errors injection placements; '0' - in Command word '1' - in Data word For other error injection types or other message types this bit must be set to enable error injection
07	CHANNEL A / B	Selects active 1553 channel. Logic '1' selects channel 'A' while a logic '0' selects channel 'B'
06	Auto Chnl Switch	On error, the BC will retry message transfer on alternate channel (* auto-retry must be selected *)
05-04	Auto Rtry Code	On error, selects the number of retries before transfer of next message Code _1 _0 0 0 -No Retry 0 1 - 1 Retry 1 0 - 2 Retry 1 1 - 3 Retry
03-00	COMMAND CODE	0000 - TRANSMIT COMMAND (RT to BC) 0001 - RECEIVE COMMAND (BC to RT) 0010 - RT to RT COMMAND 0011 - MODE CODE 0100 - BROADCAST RECEIVE COMMAND 0101 - BROADCAST RT to RT COMMAND

BC Mode

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		0110 - BROADCAST MODE CODE	
		0111 - SKIP MESSAGE (see text)	
		1000 - JUMP COMMAND (see text)	

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HALT Bit Operation

The user normally sets this bit to a logic "0" before writing to the Start Register. The user may ,IN REAL-TIME, set this bit (to a logic"1"). The board, when operating on that particular Message Block's Control Word, will HALT transfer operations until the bit is reset to a logic "0".

When the board detects that the HALT bit is set, it sets the "WAIT FOR CONTINUE" bit within the Message Status Register (see: Control Register Section). This bit can be used by the user in order to know when the board has arrived at this Message Block. When the board detects that the Halt bit has been reset by the user (continue mode) the board will then reset the "WAIT FOR CONTINUE" bit within the Message Status Register and continue BC operation.
It is important to note that this function can only be implemented within Message Blocks which have NOT [AS YET] BEEN EXECUTED BY THE BOARD.

Note: This operation can be used in conjunction with the JUMP feature described below.

SKIP Message Operation

The SKIP MESSAGE command allows the user to easily skip a message defined in a certain Message Block by only modifying the Command field within the Control Word. This allows the user to selectively send a message within the current frame. The Intermessage Gap Time associated with the SKIP Message has no effect.

JUMP Command Operation

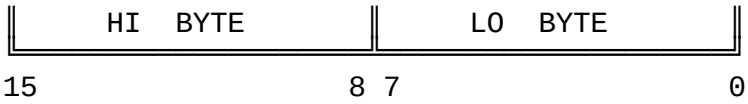
The EXC-1553VME/E-V allows the user to modify the BC transfer cycle by setting the "JUMP" command within the BC Control Word. The Jump command instructs the board to operate on a NEW instruction stack or NEW stack entry within the same stack. This Control word is followed by a Stack Pointer word instead of the usual 1553 Command Word. In addition, the Stack Pointer is followed by an Instruction Count value. The Jump command is tested AFTER the board has tested the HALT/CONTINUE bit within the Control Word. The Intermessage Gap Time associated with the JUMP Command has no effect.

The memory location sequence is illustrated below:

I N S T R U C T I O N C O U N T E R	3rd Word
S T A C K P O I N T E R	2nd Word
C O N T R O L W O R D	1st Word

BC Mode

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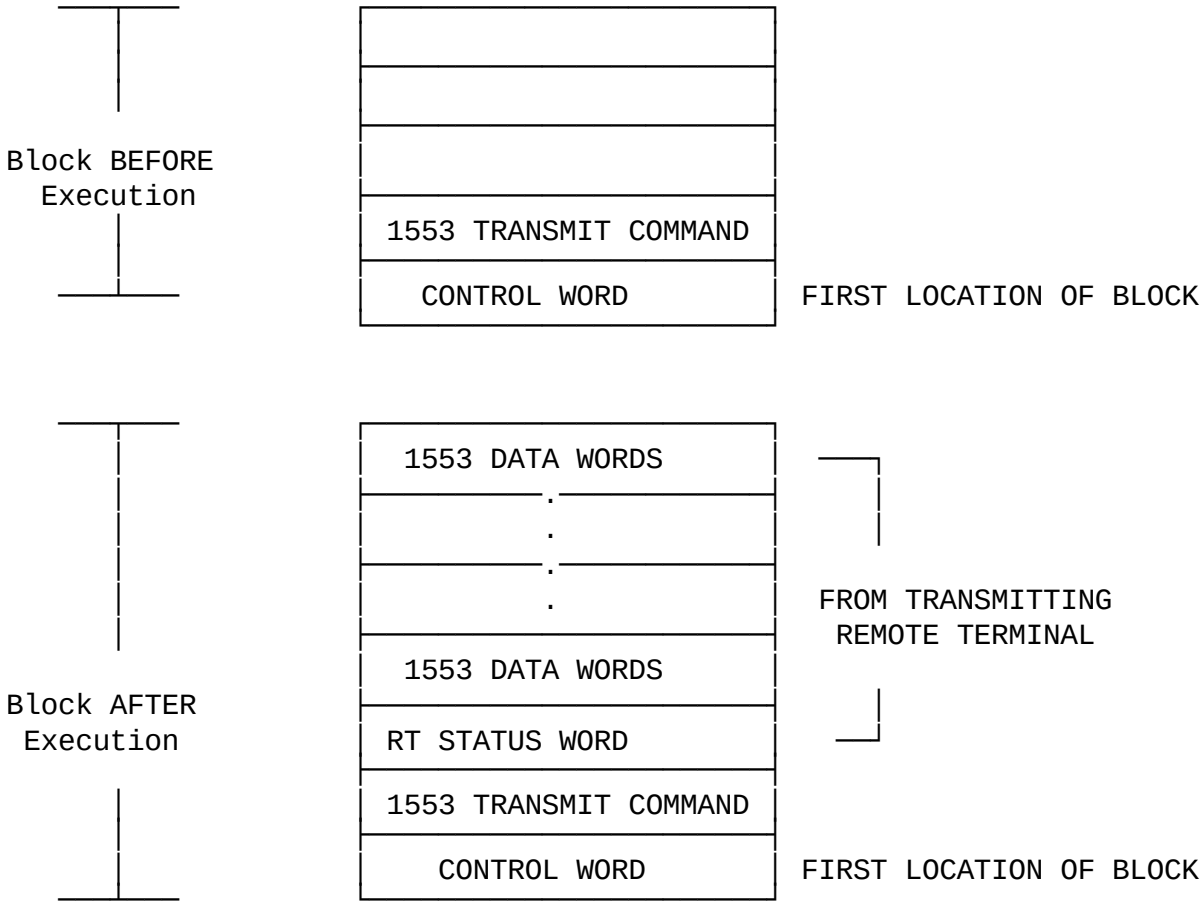


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MESSAGE BLOCK FORMATS

The Message Block contains, or will contain, the entire 1553 message as it appears on the 1553 bus - including Command Word(s), Data Words, and Status Word(s).

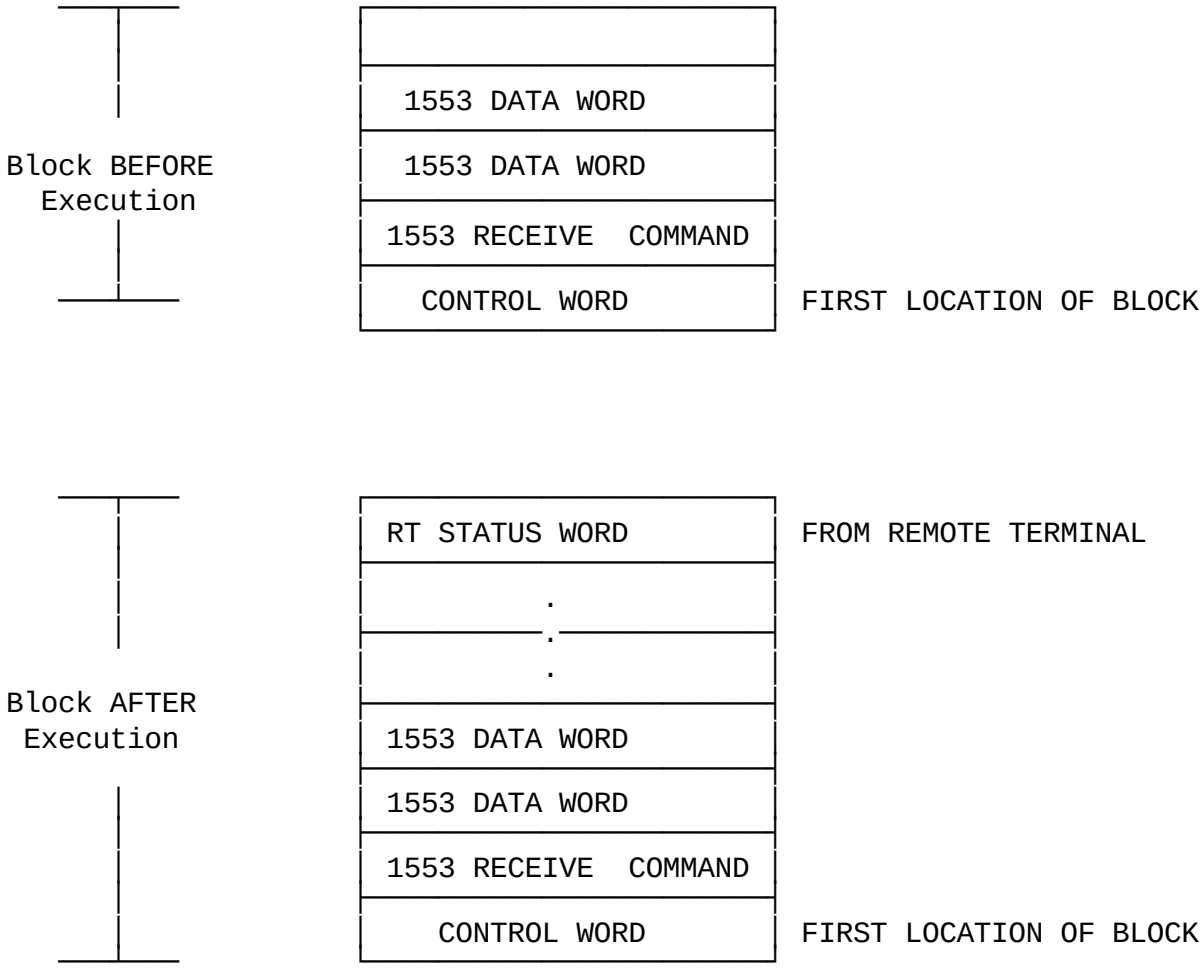
Examples #1 — TRANSMIT COMMAND



BC Mode

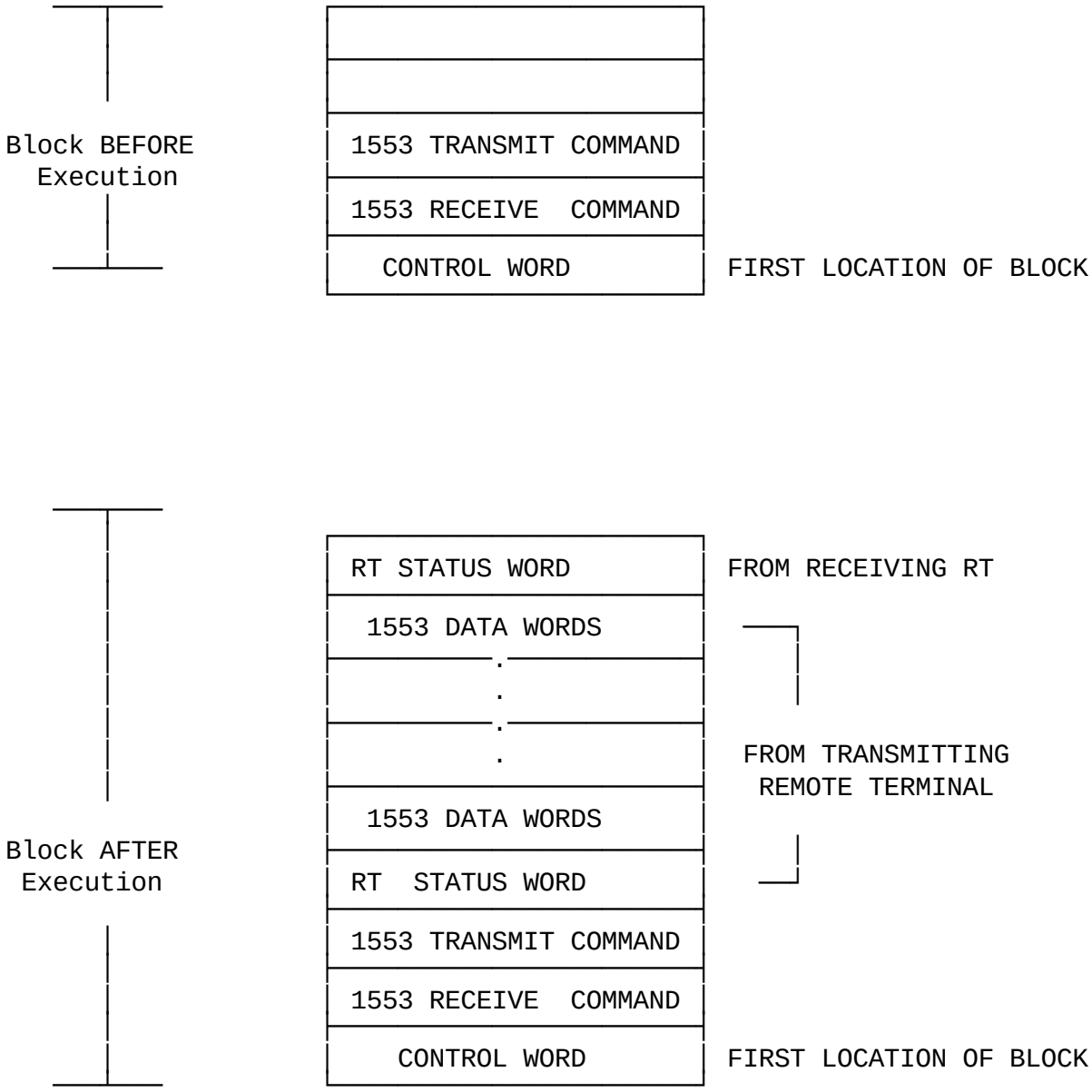
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Examples #2 RECEIVE COMMAND



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Examples | #3 | RT to RT COMMAND



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CONTINUOUS or ONE-SHOT MODES

The EXC-1553VME/E-V offers the capability of transferring all programmed messages once, in a continuous loop, or for 'N number of times'.

In the One-Shot mode, the board transfers all messages [after receipt of a "START" command], sets the Message Complete Bit within the Message Status Register, issues an Interrupt [if programmed] and waits for a new "START". This mode is selected via the Start Register (see Control Register definitions).

In the 'N' Times Mode, the user loads the Loop Count Register with the number of times to transmit the messages [frame] and sets the LOOP and START bits within the Start Register. The user can select to transmit from one to 255 times (see: Start and Loop Count Registers). The time between frames is predetermined via Frame Time Register (see below).

In the Continuous mode, the EXC-1553VME/E-V will re-transmit the message frame at a predetermined, user-programmable rate. This mode is selected via the Start Register and the Loop Count Register (see Register definitions). In this mode, all messages relating to the [active] Stack Pointer and Instruction Counter are continuously "looped" until the user halts the board's operation (see Start Register definition).

The "loop" time or Frame Time is a function of two Control registers; the Frame Time Register and the Frame Time Resolution Register. The internal Frame Time counter is loaded upon receipt of a "START" command with the 16-bit value found within the Frame Time Register. The Frame Time counter is decremented every N x 155 nsec - where N is the value of Frame Time Resolution Register. After the execution of all instructions (1 frame), the EXC-1553VME/E-V will wait until the internal Frame Time Counter reaches ZERO before re-transmitting the next frame.

NOTE: If the Frame time is less than the time required to transmit all messages [within 1 frame], the subsequent frames will be transmitted with the minimum delay between them. The minimum delay is 20 µsec approximately, measured as dead time on the bus.

The user can implement the desired Frame time by programming the appropriate combinations of the two registers. An example using one method is illustrated below.

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EXAMPLE: FRAME TIME CALCULATION

Given: User requires a Frame Time of 500msec.

Operation:

Select Frame Time Resolution of 3225 (Dec) ----- 0C99(H).
Frame Time Resolution = 3225 x 155 nsec. = 500 µsec (.5 msec)

Subsequently; the Frame Time Register value must equal to :
(500 msec (desired time) / .5 msec = 1000 (Dec))-1 --> 03E7(H)
Count-1

Load Frame Time Register = 03E7 (H) (before "START")
Load Frame Time Resolution Register = 0C99 (Hex) (" ")

MODE CODES

The EXC-1553VME/E-V handles all Dual-Redundant 1553B Mode Codes. This is to say that the Word Count field is decoded according to MIL-STD-1553B. The two quad-redundant mode codes, "Selected Transmitter Shutdown" and "Override Selected Transmitter Shutdown" are not implemented by the board.

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PROGRAM EXAMPLE BC MODE

note: ALL values are in HEX unless stated

```
10 POKE  &H6FFF,01      ' LOAD CONFIGURATION REG. = BC MODE
20 POKEW &H6FF0,0000    ' LOAD STACK POINTER REGISTERS WITH "0000"
                        ' (STACK NOW BEGINS AT ADDRESS:0000)
30 POKE  &H6FF2,xx      ' LOAD VARIABLE AMPLITUDE REGISTER
35 POKEW &H6FF3,xx      ' LOAD BC RESPONSE TIME-OUT REGISTER

40 POKEW &H0000,0100    ' POINTER TO FIRST MESSAGE. LOCATION OF MESSAGE
                        ' IS 0100(H)
60 POKEW &H0002,xxxx    ' LOAD INTERMESSAGE GAP TIME LOCATION

80 POKEW &H0008,&H0140  ' POINTER TO SECOND MESSAGE. LOCATION OF MESSAGE
                        ' IS 0140(H)
100 POKEW &H000A,xxxx   ' LOAD INTERMESSAGE GAP TIME LOCATION

120 POKEW &H100,&H80    ' LOAD CONTROL WORD WITH: TX COMMAND, BUS A,
                        ' AND NO ERRORS INJECTED
140 POKEW &H102,&H0C23  ' LOAD COMMAND WORD: 0C23

160 POKEW &H140,0002    ' LOAD CONTROL WORD WITH: RT to RT COMMAND, BUS B,
                        ' AND NO ERRORS INJECTED
190 POKEW &H142,&H0823  ' LOAD  FIRST [RECEIVE] COMMAND WORD: 0823
210 POKEW &H144,&H1C43  ' LOAD SECOND [TRANSMIT] COMMAND WORD: 1C43

230 POKEW &H6FEA,2      ' LOAD INSTRUCTION COUNTER WITH "2" (2 MESSAGES)
240 POKEW &H6FEE,xxxx   ' LOAD FRAME TIME REGISTERS
250 POKEW &H6FEC,xxxx   ' LOAD FRAME TIME RESOLUTION REGISTERS
260 POKE &H6FF6,4       ' LOAD LOOP COUNT REGISTER WITH "4" (TRANSMIT
                        ' THESE TWO MESSAGES 4 TIMES AND STOP)
270 POKE &H6FFC,5       ' LOAD START REGISTER WITH "5". STARTS MESSAGE
                        ' TRANSFERS IN LOOP MODE.

280 STOP
```


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CONTROL REGISTER DEFINITIONS

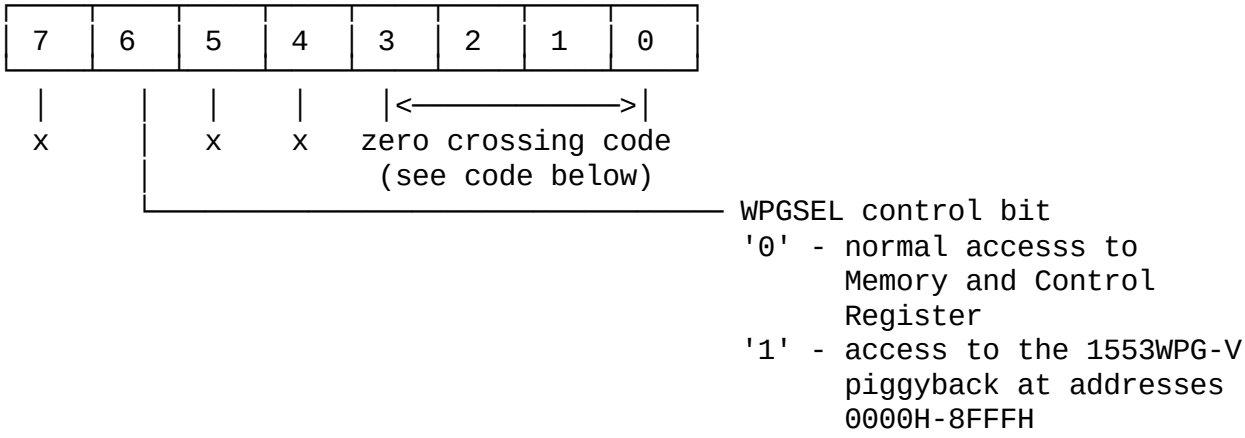
TIME TAG RESET REGISTER — 8-bit EFA3 (H) WRITE ONLY

Writing to this register (data field = don't care) will reset the RT hardware Time Tag counter. The counter will start to count from 0 immediately after the reset.

Note: The Time Tag counter is not used in the Bus Controller Mode.

ZERO CROSSING REGISTER — 8-bit EFA1 (H) READ/WRITE

This register is reset at power-up (all bits set to "0").



Definition of data bits 0,1,2,3 within the register:

Bit Position: 3 2 1 0	operation:
0 0 0 0 (0)	Selects: NO zero crossing deviation (no error)
0 0 0 1 (1)	Selects:+150 nsec from '0' (border-no error)
0 0 1 1 (3)	Selects:-150 nsec from '0' (border-no error)
0 1 0 1 (5)	Selects:+190 nsec from '0' (above 1553 limit)
0 1 1 1 (7)	Selects:-190 nsec from '0' (below 1553 limit)
1 0 0 0 (8)	Selects: Manchester Hi-Bit Error
1 0 0 1 (9)	Selects: Manchester Lo-Bit Error
1 0 1 0 (A)	Selects: Manchester Dead-Bit Error

Note: When activated, these zero crossing and manchester errors are inserted into the first data bit of every word which is transmitted by the board (this

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includes: Command, Status and Data words). The user can modify this register at any time. The board checks the [code] value within the register between the transmission of each word.

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CARD SOFTWARE RESET REGISTER — 8/16-bit 6F92 (H) WRITE ONLY

Writing to this location (data field = don't care) will RESET the EXC-1553VME/E card. All card functions will be reset upon writing to this register. In addition, all Dual Port Ram will be cleared to "0". The Board Status, the Board ID, Firmware Revision and Variable Amplitude registers are written by the board after the reset operation has been completed.

BC/RT SOFTWARE RESET REGISTER — 8/16-bit 6F90 (H) WRITE ONLY

Writing to this location (data field = don't care) will RESET only the BC/RT portion of the EXC-1553VME/E-V card. In addition, the Dual Port Ram used in the BC mode of operation will be cleared to "0". The Board Status, the Board ID, Firmware Revision and Variable Amplitude registers are written by the board after the reset operation has been completed.

BOARD CONFIGURATION REGISTER — 8-bit 6FFF (H)

The operating mode of the board is set via this register. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

HEX VAL	7	6	5	4	3	2	1	0	
01	0	0	0	0	0	0	0	1	BC MODE
02	0	0	0	0	0	0	1	0	RT MODE
04	0	0	0	0	0	1	0	0	BC / CONCURRENT-RT
08	0	0	0	0	1	0	0	0	reserved
10	0	0	0	1	0	0	0	0	reserved
20	0	0	1	0	0	0	0	0	reserved
40	0	1	0	0	0	0	0	0	reserved
80	1	0	0	0	0	0	0	0	reserved
ED	1	1	1	0	1	1	0	1	reserved
FF	1	1	1	1	1	1	1	1	reserved

BC Mode

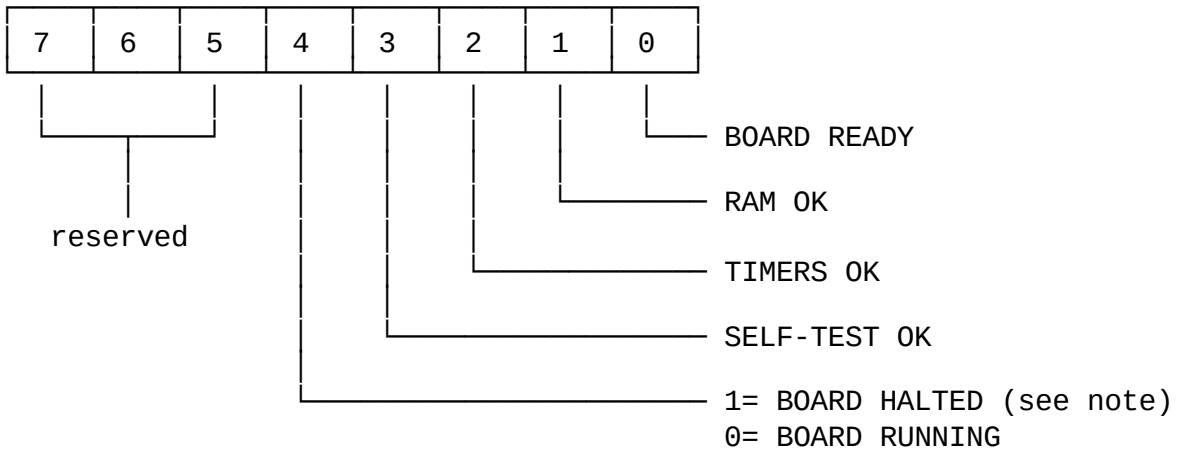
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BOARD ID REGISTER 8-bit 6FFE (H)

This register contains a fixed value which can be read by a user's initialization routine to detect the presence of the EXC-1553VME/E-V card. The one-byte value of this register is: 45 (Hex) ; ASCII "E".

BOARD STATUS REGISTER 8-bit 6FFD (H)

This register indicates the status of the EXC-1553VME/E-V card. In addition, this register indicates options as defined below (Status bits are active "1"). This register should not be modified by the user.

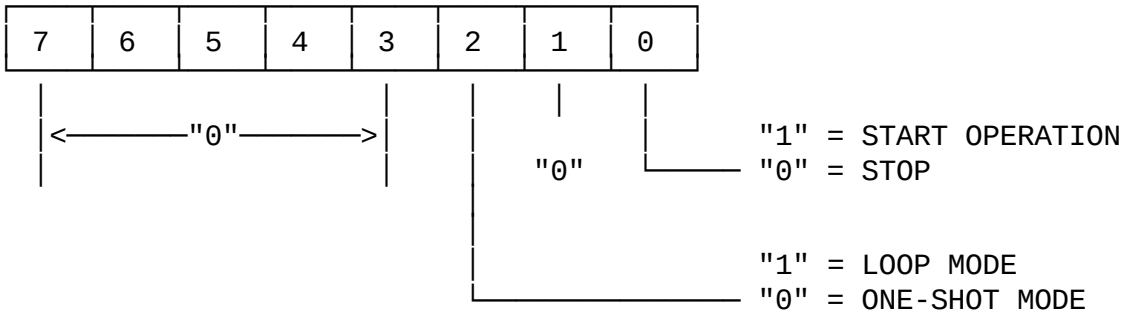


NOTE: Bit "04" (Board Halted) is set by the board after the user "stops" the current operation (by resetting the START bit within the Start Register). The user must check this bit first before modifying registers which first require a "STOP" operation. The board resets this bit after receiving a subsequent START command (by writing to the Start Register). The condition of this bit after power-on or software reset is a logic "1".

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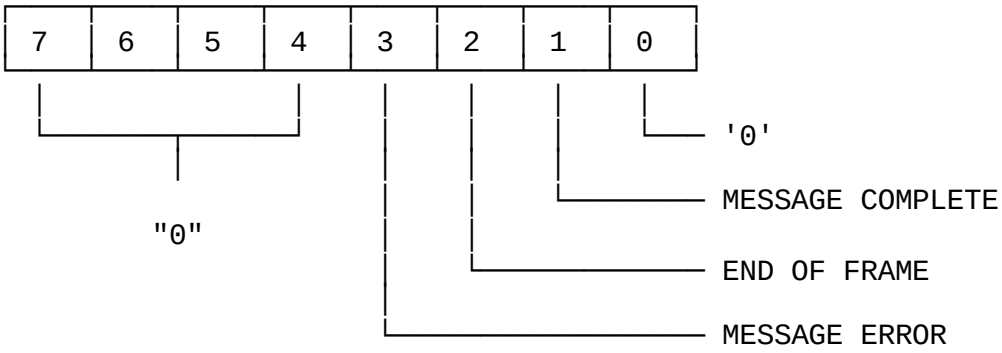
START REGISTER 8-bit 6FFC (H)

This register controls the 'START/STOP' operation of the EXC-1553VME/E-V. Writing to this register with the appropriate bit set begins the Bus Controller transfer operation. When operating in the "Loop" or "N Times" mode, the user must set the Start and Loop bits within this register. The "loop" and "N-times" number is selected via the Loop Count Register. In the One-Shot and "N-Times" modes, the board RESETS the Start bit within the register after ALL messages have been transferred. The board does not reset any bit while in the Continuous loop mode. Write "0" to bit "00" to halt the LOOP operation between messages. Write, instead, a "0" to bit "02" in order to halt the operation at the end of the entire frame (this bit is not tested between message transfers). See the related bit (data bit "04") within the Board Status Register which indicates when the board has been halted.



INTERRUPT CONDITION REGISTER 8-bit 6FFB (H)

This register allows the user to set different interrupt triggers. When a condition that has been enabled within this register occurs, an interrupt will be generated. The user may check the Message Status Register to determine which condition caused the interrupt. A logic '1' enables the interrupt condition. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).



BC Mode

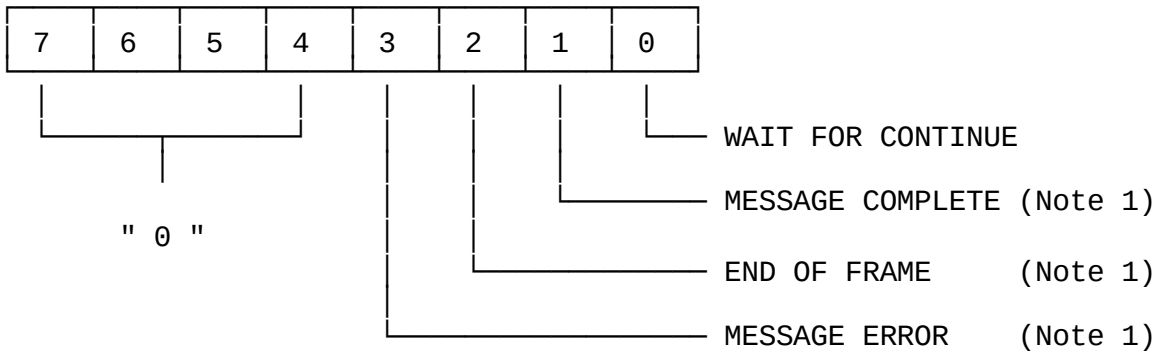
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Note: For all Interrupt conditions the interrupt will be sent at the end of the message.

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MESSAGE STATUS REGISTER	8-bit 6FFA (H)

This register indicates the status of the EXC-1553VME/E-V card. The figure below illustrates the definition of each Status bit. A logic "1" indicates active condition.



WAIT FOR CONTINUE - A message with the halt bit set has been encountered. The user must reset the halt bit in the Control word to continue.

MESSAGE COMPLETE - The last word of a message has been sent

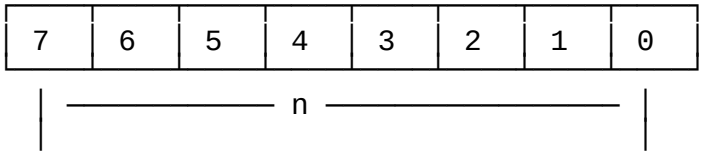
END OF FRAME - The last word of the last message in a frame has been sent

MESSAGE ERROR - A message has been sent resulting in the error bit being set in the Message Status Word

Note: 1) Status bits are NOT reset by the board and should be reset by the user after reading them.

LOOP COUNT REGISTER	8-bit 6FF6 (H)

This register is used in conjunction with the Loop Bit in the Start Register. If that bit is set, the user sets this register to specify the number of times the Message Frame will be transmitted. A value of zero is interpreted as a request for continuous looping. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).



Value = 0 : Retransmits in continuous loop

BC Mode

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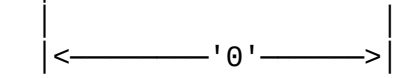
Value = 1-255 : Sends message frame "n" times (1 to 255) as defined

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BIT COUNT REGISTER 8-bit 6FF5 (H)

Sets the number of total bit times within the 1553 word including Sync(3) and Parity(1). When NO error is selected (see: Control Word), this register is ignored (20-bit word is selected). This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

7	6	5	4	3	2	1	0

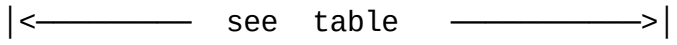


	2	1	0	# of bits
-3	0	0	0	17
-2	0	0	1	18
-1	0	1	0	19
0	0	1	1	20
+1	1	0	0	21
+2	1	0	1	22
+3	1	1	0	23

WORD COUNT REGISTER 8-bit 6FF4 (H)

This register controls the number of 1553 words (+/- 3) within the message. The variation is relative to the 1553 Command Word's WORD COUNT FIELD. When NO error is selected (see: Control Word), this register is ignored. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

7	6	5	4	3	2	1	0



(No Word Count Error injected) -

-3	FD (H)
-2	FE (H)
-1	FF (H)
0	00 (H)
+1	01 (H)
+2	02 (H)
+3	03 (H)

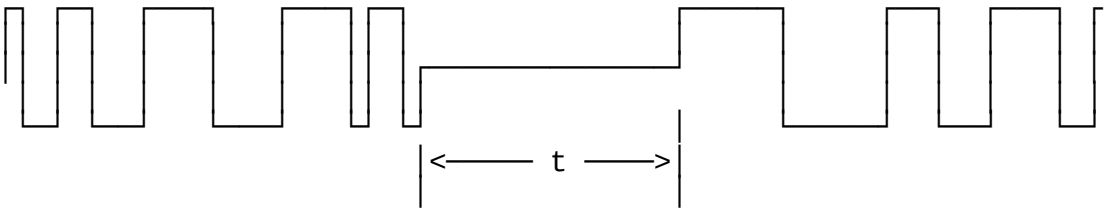
BC Mode

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BC RESPONSE TIME REGISTER 8-bit 6FF3 (H)

This register sets the Bus Controller's RESPONSE TIME WINDOW. This value determines the maximum [wait] time until an RT's Status Response is considered "INVALID" by the BC. The resolution of this register is 155 nanoseconds per bit. This time is measured as the "DEAD TIME" on the 1553 bus. The minimum time is approximately 2 µsec. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

Example: To set up a BC response time of 14 usec write a 90 to this register
90 * 0.155 = ~14µsec



VARIABLE AMPLITUDE REGISTER 8-bit 6FF2 (H)

This register specifies the amplitude of the 1553 output signal. The signal can be programmed from 0 volts up to 7.5volts (p-p) - measured on the 1553 bus with specified 1553 coupling and 35ohm load (two 70 ohm termination resistors were used). A higher Transmit [output] amplitude will appear on the 1553 bus if 78 ohm termination resistors are used. The register has a resolution of 30mv/bit (p-p) on the bus. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register). This register defaults to FFH after Reset, providing maximum amplitude.

STACK POINTER 16-bit Register 6FF0 (H)

The Stack Pointer points to the Instruction Stack. The pointer value must be equal to the ADDRESS of the [first] Instruction block and must always be even (LSB set to 0). The Instruction Stack can reside anywhere within locations 0000 through 67FE (Hex). To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

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FRAME TIME REGISTER	16-bit 6FEE (H)

This register contains the 16-bit Frame Time Value for Continuous and N-times Modes Operation. The value written to this register is multiplied by the value set within the Frame Time Resolution Register described below. The value set must equal the desired multiplication factor - 1. See FRAME TIME CALCULATION above. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

FRAME TIME RESOLUTION REGISTER	16-bit 6FEC (H)

This 16-bit value represents the resolution of the Frame Time Counter in increments of 155 nsec. See CONTINUOUS OR ONE-SHOT MODES section described above. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

INSTRUCTION COUNTER	16-bit 6FEA (H)

The Instruction Counter is loaded with the number of instructions (1553 Messages) in the current frame to execute. The value must be greater than "0" before beginning transmission (by writing to the "START REGISTER"). Load "1" for one message, "2" for two messages, etc. The EXC-1553VME/E-V updates this register by decrementing the value and writing it back to the memory. This register must be set before issuing a START to the board. This register is decremented and updated by the board at the end of each message transfer. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register). When in the "loop mode", this register cycles from the initial value to "1".

FIRMWARE REVISION REGISTER	8-bit 6FE7 (H)

This register indicates the revision level of the on-board firmware. The value 0001 0010 would be read as revision level: 1.2

BC Mode

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RT MODE OPERATION

The EXC-1553VME/E-V can be configured to simulate up to 32 Remote Terminals. The user selects which terminal(s) are operating ["ACTIVE"]. The EXC-1553VME/E-V handles all message transfers subsequent to receiving a "START" command (see Control Registers). In addition, errors can be injected into the message responses. The RT data transfers operates via a 2Kx16 Look Up Table which points to the data block area. The user loads the 1553 data blocks with transmit data and reads the received 1553 data from the blocks.

The EXC-1553VME/E-V can operate within various 1553 environments since most 1553 parameters such as Response Time, Status Word content,etc. are user-programmable. The EXC-1553VME/E-V also allows the user to enable or disable the 1553 BROADCAST function - reserving RT address 31 (11111) or utilize all 32 RT addresses by disallowing Broadcast Commands (See Configuration Control Register).

Another feature of the RT mode involves the return of the Status Word to the Bus Controller. The user can specify, for example, that the Remote Terminal transmit its 1553 Status Word at the end of a message even if INVALID DATA WORDS [only "invalid" - as specified by 1553] were received within the message. This feature is selected via the Status Response Register (see: Control Registers).

The user can program the 1553 Mode Code Subaddress Identifier (RT Control Register) so that either "11111","00000", or both, can be used to indicate that the 1553 Command Word is a Mode Code.

The Remote Terminal transmits its 1553 Status Word in approx. 4.0 usec. (measured as: "dead time on the bus") - a value which can be INCREASED via the RT Response Time Register.

The board will respond properly to messages received at the maximum rate permitted by the 1553 specification, i.e., it will respond properly to messages received with an intermessage gap of 2.0μsec measured as dead time on the bus.

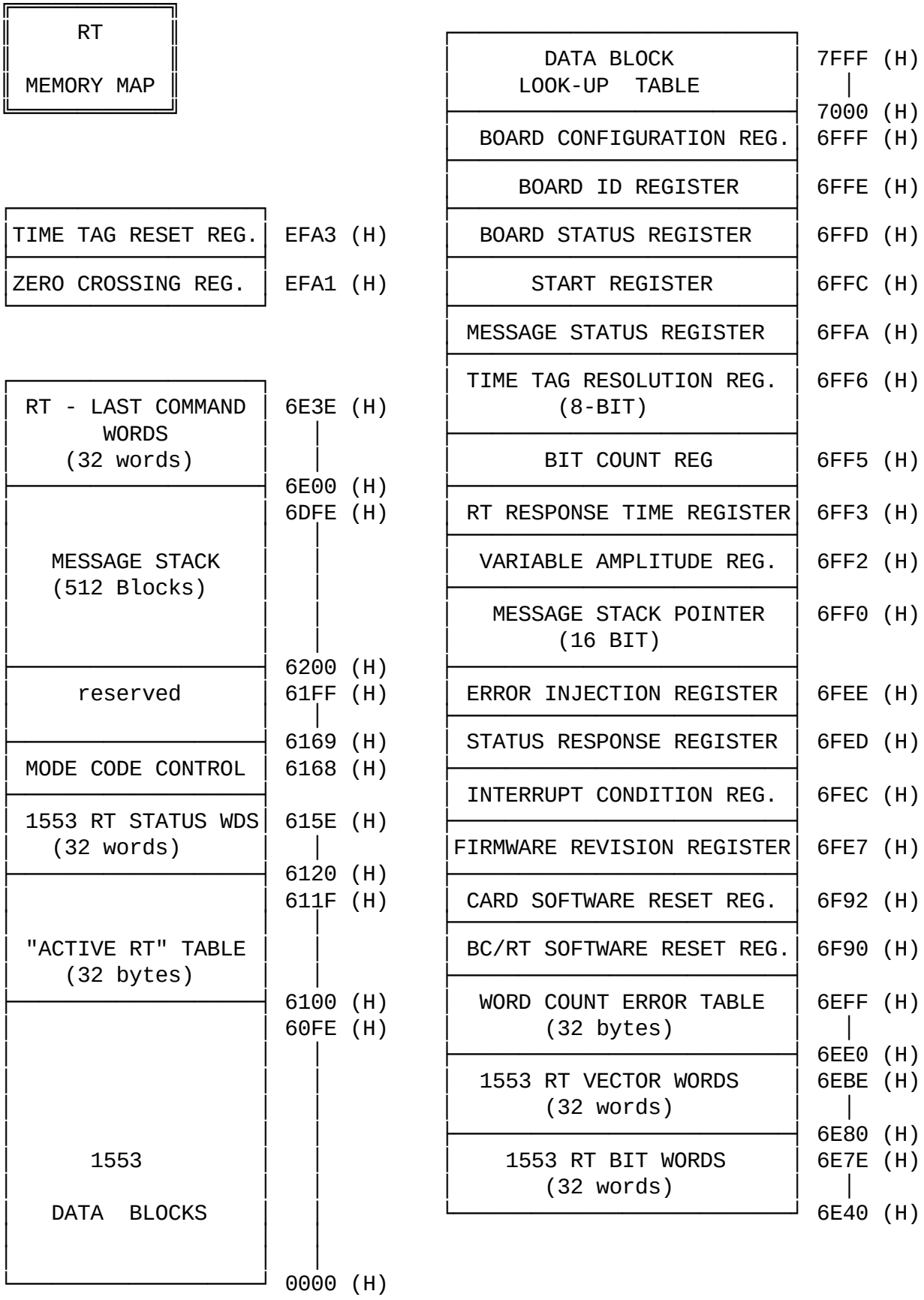
NOTE:

The user should use the following sequence to determine whether the board is installed AND ready to operate:

* Check the Board ID register (test for value = 45 Hex)
* Check Board Status Register (test for Board Ready bit = "1")

The board is installed and ready when BOTH of these registers contain the correct values (as written above). This sequence should be used after power-on and Software Reset operations. For Software Reset operations, these values should be set to ZERO by the user immediately prior to writing to the Initialization Register.

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RT Mode

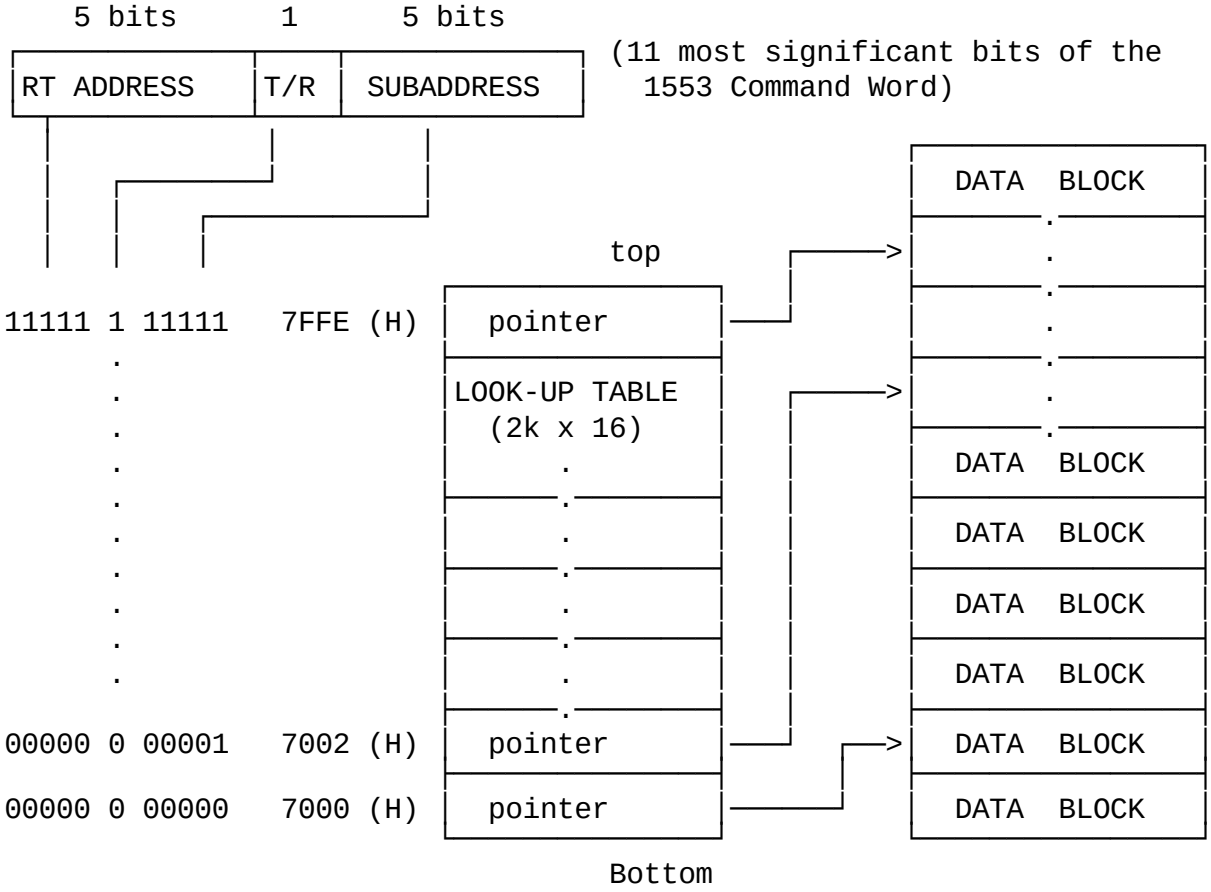
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Note: Areas not specified in the map are reserved and should not be accessed by the user.

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DATA BLOCK LOOK-UP TABLE 7000 ---> 7FFF (H)

The received Command word's RT Address, T/R bit, and Subaddress Fields are used to index into the [user-programmed] look-up table. Each entry in the table contains a 16 bit "DATA BLOCK POINTER". This pointer points to the starting location of a data block which will be used for transferring 1553 data to/from the board. Each Data Block can contain up to 32 words (only 1553 Data Words are stored within the block).



Important Note For RT to RT messages

When the board is simulating both RT's in an RT to RT message transfer, the simulated receiving RT's data block is not updated with the transmit data. (The data IS transmitted over the 1553 bus).

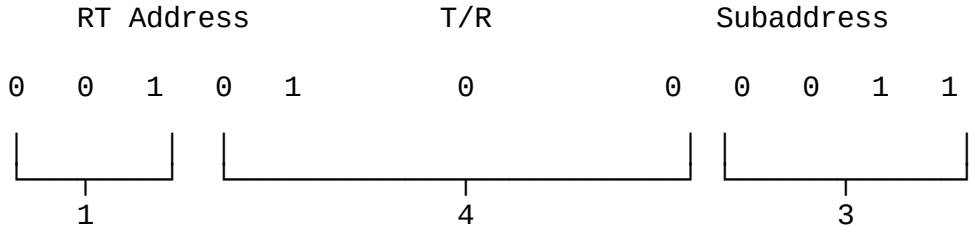
RT Mode

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HOW TO CREATE THE ADDRESS TO THE TABLE

1. Isolate the ELEVEN (most significant) bits of the 1553 Command Word (RT Address, T/R, and Subaddress Field).

Example : RT Address =5
T/R bit = 0 (receive)
Subaddress = 3



The HEX representation = 143 (H)

2. Multiply the value by 2 (since it is a word index).

143 (H) * 2 = 286 (H)

3. Add this value to the base address of the Look-Up table (7000).

```
  7000 (H)
+  286 (H)
----------
  7286 (H)
```

4. Write Data Block Pointer to this location.

example:

```
POKEW &H7286, xxxx        "writes 16-bit value to table
```

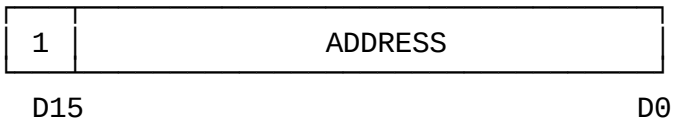

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HOW TO CREATE THE DATA BLOCK POINTER

1. Select start address of data block (from 0000 to 60FE [HEX]). This address must be even (LSB = 0).

2. Set D15=1 (where D15 represents the most significant bit)

3. Write 16-bit Value into Look-Up Table with the LSB of the address corresponding to D0.



EXAMPLE:

User wants 1553 message to be stored [starting] at address : 5002 (H)

-Set bit "D15"in word as shown in figure above
-New Pointer value = D002 (H)
-Write value into Look-Up Table

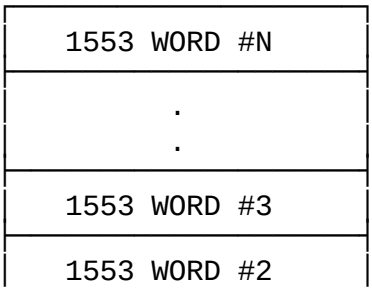
COMBINING THE TWO EXAMPLES ABOVE:

```
POKEW &H7286, &HD002
```

This writes the [pointer] Block Address :D002(H) into the Look-Up table Address : 7286(H).

DATA STORAGE

The data words must be stored and/or read in the following format within the data block:



RT Mode

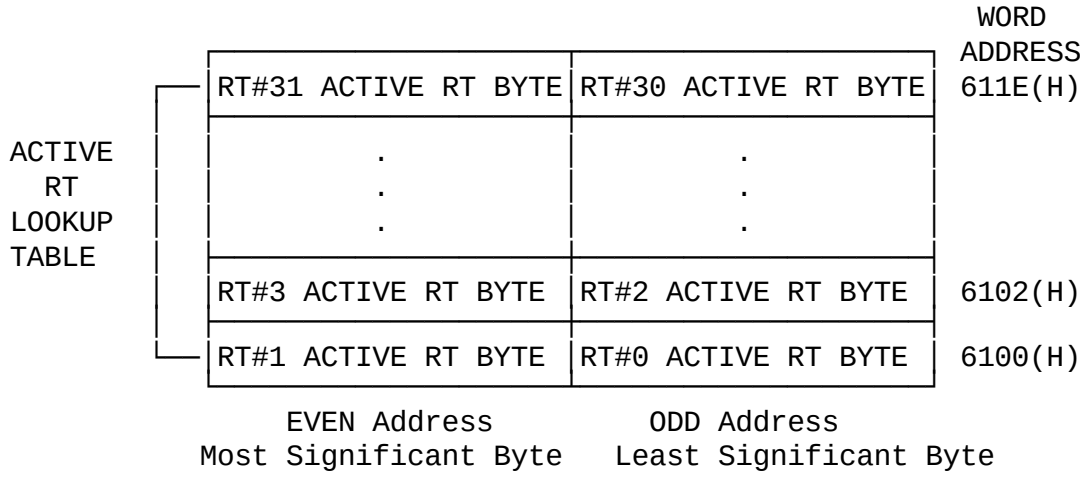
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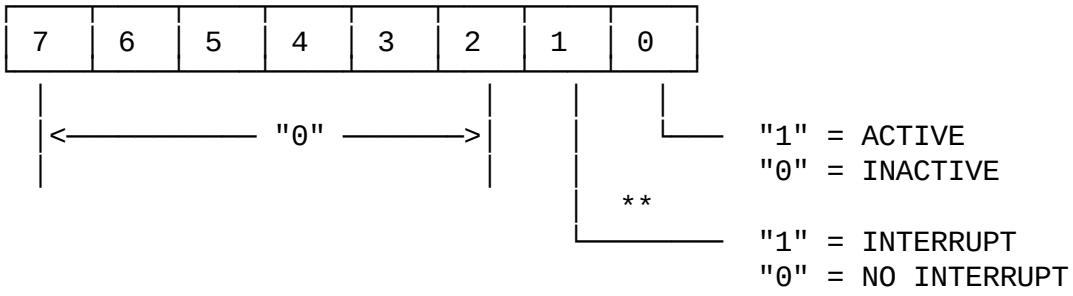
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"ACTIVE RT" TABLE	6100 ---> 611F (H)

These locations contain the list of Active Remote Terminals. Each desired (Active) RT is selected by setting the bit "0" within the Active Remote Terminal Byte to a logic "1". The first Active RT byte relates to RT #0, the next to RT #1, while the last locations relates to RT #31 (note that the first Active RT BYTE resides in the first [least significant] byte - which is an ODD address, followed by the EVEN address).



ACTIVE REMOTE TERMINAL BYTE FORMAT:



** = User must set this interrupt bit and the bit within the Interrupt Condition Register in order to generate an interrupt to the computer.

RT Mode

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1553 RT STATUS WORDS 6120 ---> 615F (H)

These locations are reserved for the [32] 1553 RT STATUS Words. The user loads the desired STATUS Words into related locations within the block. The first word relates to RT #0, the next word to RT #1, while the last word relates to RT #31. For each RT, which is to be simulated, all 16 bits must be defined within its STATUS word.

In a non-1553B environment (see "STATUS RESPONSE REGISTER") the user defined STATUS word is sent, whenever the RT has to respond with a STATUS Word.

In a 1553B environment (see "STATUS RESPONSE REGISTER"), the same STATUS word is sent with the following conditions:

MESSAGE ERROR (bit #10) - In case an error occured in the previous message, this bit will be sent set (`1') in the current Mode Code message (of type Send Status or Send Last Command), even if the user defined value for this bit is `0'. If the user defined value is `1' this bit will be sent set.

BUSY (bit #3) - This bit is always sent as defined by the user. In the case of TRANSMIT COMMANDs, when BUSY is set, NO DATA words will be tranmsitted by the RT following the tranmission of the STATUS Word.

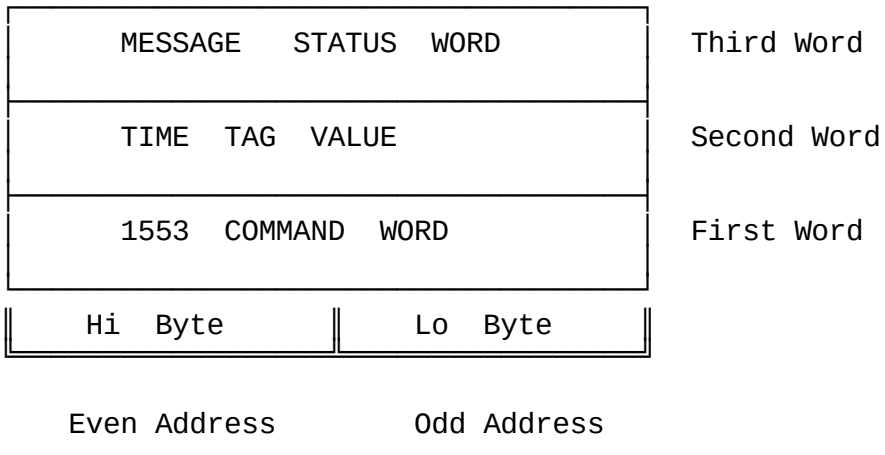
Note: The 1553B Format for the STATUS word is defined in following

Bit #	Bit Name
15-11	RT Address
10	Message Error
9	Instrumentation
8	Service Request
7-5	Reserved
4	Broadcast
3	Busy
2	Subsystem Flag
1	Dynamic Bus
0	Terminal Flag

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MESSAGE STACK

The EXC-1553VME/E-V generates a Message Stack within the dual-port memory. This stack contains information which can be utilized by the user for post processing of the Remote Terminal messages. The stack is divided into 512 blocks - each containing three words. The stack operates as a Circular Buffer. The Message Stack Pointer points to the beginning of the [next] unused block. Only "ACTIVE" RT messages are stored. The figure below illustrates one instruction block.



NOTE : RT to RT message

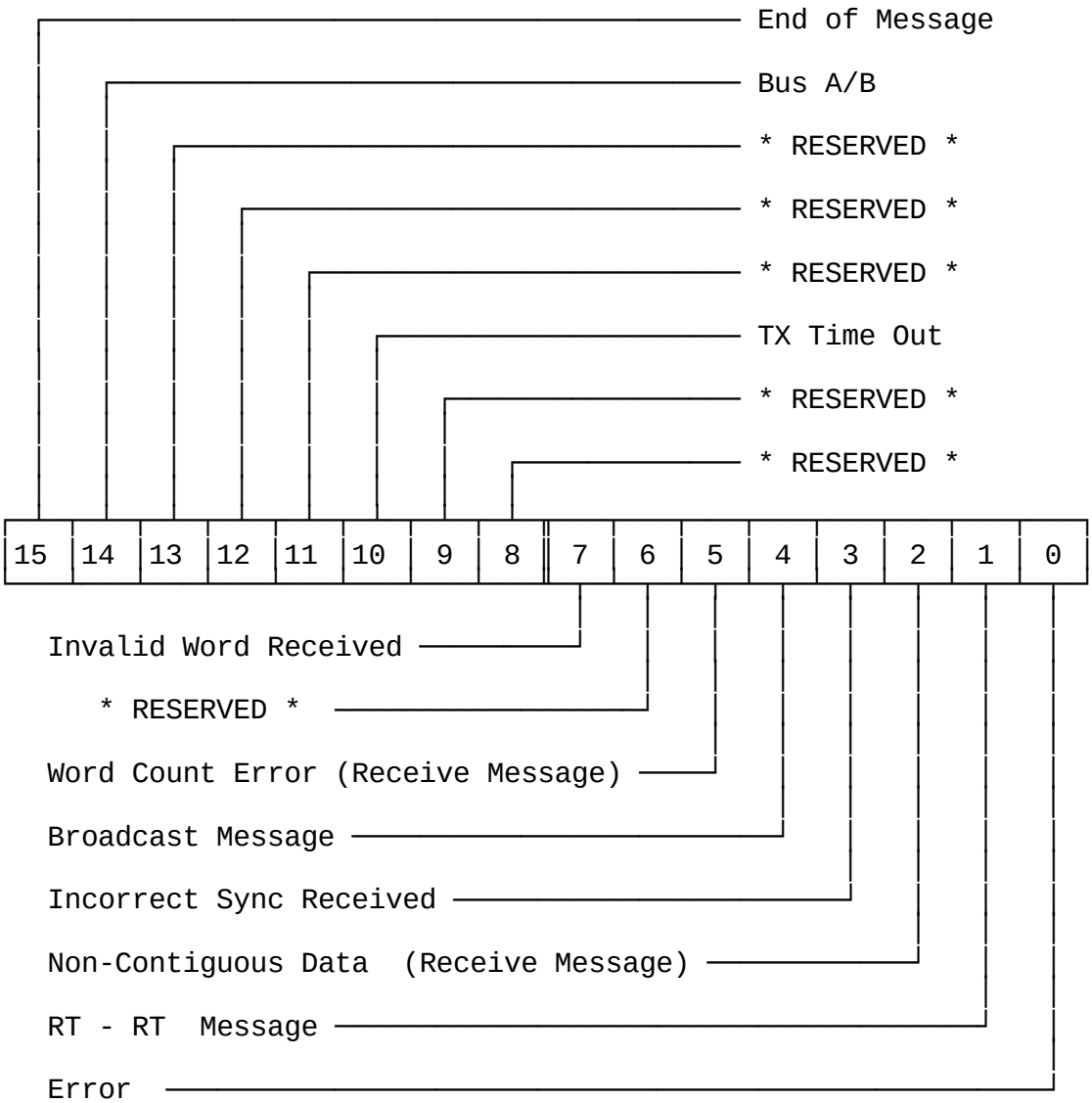
In the event that an RT to RT message is received - whereby the board operates as BOTH RT's, the Message Stack would be updated as follows:

1. Two Message Stack Blocks are utilized
2. The 1553 "Receive" Command Word is written into the FIRST Message Stack Block
3. The RT-RT bits within BOTH Message Status Words will be set (=1)
4. The Time Tag Word within the SECOND stack block is updated by the board as is the second Message Status Word. The "RT to RT" bit is the only bit within the FIRST Message Status Word which is updated (active).
5. The 1553 "Transmit" Command Word is written into the SECOND message block.

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MESSAGE STATUS WORD

The Message Status Word indicates the status of the message transfer. This word is created by the Board and is NOT the 1553 "STATUS WORD". The contents of the Message Status word are shown below:



NOTE: A LOGIC "1" INDICATES OCCURRENCE OF STATUS FLAG

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Message Status Word Definitions:

15	End of Message	Indicates that the message transfer has been completed
14	Bus A/B	Indicates on which bus the message was transferred. '0' = BUS B '1' = BUS A
13	Reserved	Set to logic '0'
12	Reserved	Set to logic '0'
11	Reserved	Set to logic '0'
10	Tx Time Out	Card,acting as receiver in RT to RT message, did not sense a transmitter status word (within 14 µsec)
09	Reserved	Set to logic '0'
08	Reserved	Set to logic '0'
07	Invalid Word	Indicates the reception of at least one invalid 1553 word (i.e. Bit Count, Manchester code, Parity)
06	Reserved	Set to logic '0'
05	Word Ct Error	Indicates that an incorrect number of words were received within the message
04	Broadcast Message	Indicates that a broadcast command word has been received
03	Incorrect Sync	Indicates that the sync of either the command or the data word(s) was incorrect
02	Non-Contiguous	Indicates occurrence of an invalid gap between received 1553 words
01	RT - RT Message	Indicates that an 'RT to RT' message has been received, in which the board simulates both RT's.
00	ERROR	Indicates the occurrence of an error (defined within one of the other message status bit locations)

RT Mode

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Time Tag Value (Read by user)

The Time Tag Value is a sixteen bit word which may be used to determine the time elapsed since 'START' or to determine the time between the 1553 messages. The Time Tag implementation utilizes a 16-bit, free running counter whose resolution is set by the 8-bit "Time Tag Resolution Register" at address 6FF6 (Hex). This register has a resolution of 4 µsec per bit. The equation to determine the resolution of the counter is: (register value+1) * 4 µsec.

Example:
register value = 0 --> counter's resolution = 4µsec
register value = 4 --> counter's resolution = 20µsec

The Time Tag counter can be reset (to '0') any time by writing to the "Time Tag Reset Register" (see the section entitled: Control Register Definitions). The timer's value is written to the dual port RAM during the reception of the [first] command of each message.

1553 Command Word

This location contains the 1553 Command Word associated with the message.
Only ACTIVE RT Commands are stored !!!.

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RT LAST COMMAND WORDS	6E00 ---> 6E3E (H)

These locations are reserved for the [32] 1553 Last Command Words. The EXC-1553VME/E-V writes these locations at the end of each message transfer to an "active" RT. The first word relates to RT #0, the next word to RT #1, while the last word relates to RT #31. These words are used for the implementation of the 'Transmit Last Command Word' Mode Code.

Note: Only command words of valid messages containing no errors will be recorded in this table.

1553 RT BIT WORDS	6E40 ---> 6E7E (H)

These locations are reserved for the [32] 1553 Bit Words. The user loads the desired Bit Words into the related locations within the block. The first word relates to RT #0, the next word to RT #1, while the last word relates to RT #31. These words are used for the implementation of the 'Transmit BIT Word' Mode Code.

1553 RT VECTOR WORDS	6E80 ---> 6EBE (H)

These locations are reserved for the [32] 1553 Vector Words. The user loads the desired Vector Words into the related locations within the block. The first word relates to RT #0, the next word to RT #1, while the last word relates to RT #31. These words are used for the implementation of the 'Transmit Vector Word' Mode Code.

RT to RT MESSAGES

When the board is operating as both RT's in an "RT to RT" transfer, then:

1. The board transmits both 1553 Status and Data words out onto the bus.
2. The Transmit Data Block is NOT copied [by the board] into the Receiver Data Block area (pointed to by the look-up table pointer).

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MODE CODES

The user can program the Subaddress code that will indicate the reception of a Mode Command. Either or both of the following codes can be used: "11111" and "00000". The user must program the Mode Code Control Register as described within the Control Register section.

The EXC-1553VME/E-V handles all Dual-Redundant 1553B Mode Codes. This is to say that the Word Count field is decoded according to MIL-STD-1553B. One of the Mode Codes (SYNCHRONIZE WITH DATA WORD) is operated upon as a "standard" message transfer - using the Data Block Look-Up Table. In such a case, the Command Word's RT Address, T/R bit and Subaddress fields are used as a pointer to the look-up table. The table entries that are addressed when the T/R bit ="0" and Subaddress = "00000" or "11111" should contain a Data Block Pointer pointing to where the "Synchronize With Data Word" data word should be stored.

Mode Codes such as : Transmit Last Command, Transmit Vector Word, and Transmit Bit Word are accomplished by using the dedicated blocks within the on-board memory. (Described above)

BROADCAST MODE

The EXC-1553VME/E-V can operate within the Broadcast environment by selecting the BRDCSTEN bit within the Control Register defined in the VME/VXI Configuration Register section.

When operating in the BROADCAST mode, the user must set the ACTIVE RT Table entry RELATING TO RT #31 (last location) as NOT ACTIVE !. The
EXC-1553VME/E-V will then test the BRDCSTEN bit to see whether the board is operating in the Broadcast mode.

In addition (while operating in the Broadcast mode) the board will store the received message into a 1553 data block area as is done with "standard" message formats (RT address, T/R bit, and Subaddress are used as a pointer to the Data Block Look-Up table memory).

Note: When operating in the Broadcast Mode, the Broadcast bits within the
1553 Status Words are NOT updated by the board's processor.

ERROR INJECTION FEATURES

The board allows two types of error injection; Global (for all RT's) and a "per RT" error. The Global errors such as Parity, Sync, Non-Contiguous Data and Bit Count are detailed in the Error Injection Register description. These errors are either "ON" or "OFF" for all RT's. The ability to inject a 1553 Word Count error, however, is on a per RT basis.

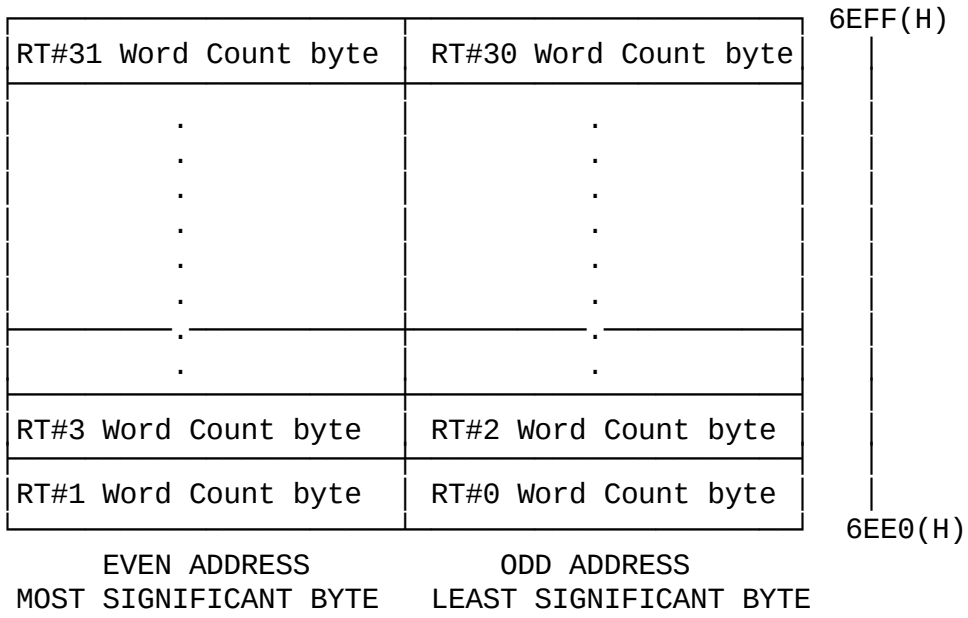
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WORD COUNT ERROR TABLE	6EE0 ---> 6EFF (H)

The Word Count error is selected by writing to the Word Count Error Table. This table contains 32 bytes (one per Remote Terminal). The first byte relates to RT #0, the second to RT #1, while the last location relates to RT #31 (note that the first Word Count Byte resides in the first [least significant] byte - which is an odd address (6EE1) followed by an even address (6EE0)).



The contents of each location controls the number of 1553 words (up to +/-3) within the message. The variation is an offset relative to the 1553 Command Word's WORD COUNT FIELD. The "resulting" message (after error is programmed) must contain at least ONE data word. This table is defaulted to '00' by the board upon power-on or software reset. This table must be set before issuing a START to the board. To modify this table: issue a "STOP", modify the contents and then issue a "START" (see Start Register).

(No Word Count Error injected) -

OFFSET	TABLE VALUE
-3 Words	FD (H)
-2 Words	FE (H)
-1 Word	FF (H)
0	00 (H)
+1 Word	01 (H)
+2 Words	02 (H)
+3 Words	03 (H)

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PROGRAM EXAMPLE — RT MODE

note: all values are in HEX unless stated

```
10 POKE &H6FFF,02        ' LOAD CONFIGURATION REG. = RT MODE
15 POKE &H6FF2,xx        ' LOAD VARIABLE AMPLITUDE REGISTER
20 POKE &H6100,1         ' ENABLE RT#1
30 POKE &H6105,1         ' ENABLE RT#4

40 POKEW &H6122,&H0800   ' LOAD STATUS WORD (RT#1) WITH '0800H'
60 POKEW &H6128,&H2000   ' LOAD STATUS WORD (RT#4) WITH '2000H'

80 POKE &H6FF6,xx        ' LOAD TIME TAG RESOLUTION REGISTER

100 POKE &H6168,00       ' LOAD MODE CODE CONTROL REG = SA 00000&11111

120 POKE &H6FEE,00       ' NO GLOBAL ERROR INJECTION

130 POKEW &H7xxx,xxxx    ' LOAD LOOK-UP TABLE WITH BLOCK POINTER FOR DATA
                         ' STORAGE
140 POKEW &H7xxx,xxxx    ' LOAD LOOK-UP TABLE WITH BLOCK POINTER FOR DATA
                         ' STORAGE

150 POKE &H6FFC,1        ' LOAD START REGISTER WITH "1". STARTS RT MODE
160 STOP
```


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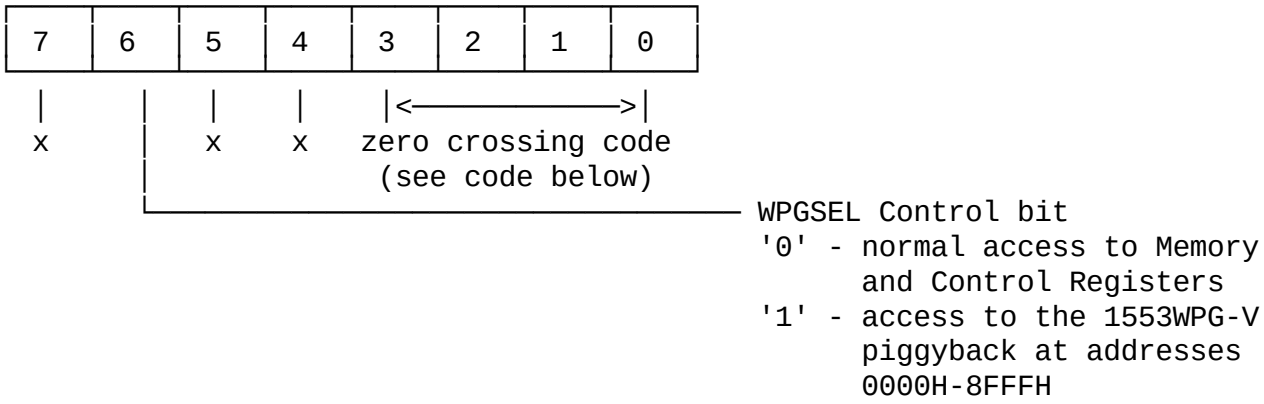
CONTROL REGISTER DEFINITIONS

TIME TAG RESET REGISTER — 8-bit EFA3 (H)

Writing to this register (data field = don't care) will reset the RT hardware Time Tag counter. The counter will start to count from 0 immediately after the reset.

ZERO CROSSING REGISTER — 8-bit EFA1 (H) READ/WRITE

This register is reset at power-up (all bits set to "0").



Definition of data bits 0,1,2,3 within the register:

Bit Position: 3 2 1 0	operation:
0 0 0 0 (0)	Selects: NO zero crossing deviation (no error)
0 0 0 1 (1)	Selects:+150 nsec from '0' (border-no error)
0 0 1 1 (3)	Selects:-150 nsec from '0' (border-no error)
0 1 0 1 (5)	Selects:+190 nsec from '0' (above 1553 limit)
0 1 1 1 (7)	Selects:-190 nsec from '0' (below 1553 limit)
1 0 0 0 (8)	Selects: Manchester Hi-Bit Error
1 0 0 1 (9)	Selects: Manchester Lo-Bit Error
1 0 1 0 (A)	Selects: Manchester Dead-Bit Error

Note: When activated, these zero crossing and manchester errors are inserted into the first data bit of every word which is transmitted by the board (this includes: Command, Status and Data words). The user can modify this register at any time. The board checks the [code] value within the register between the transmission of each word.

RT Mode

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CARD SOFTWARE RESET REGISTER — 8/16-bit 6F92 (H)

Writing to this location (data field = don't care) will RESET the EXC-1553VME/E-V card. All card functions will be reset upon writing to this register. In addition, all Dual Port Ram will be cleared to "0". The Board Status, Board ID, Firmware Revision and Variable Amplitude registers are written by the board after reset operation has been completed.

BC/RT SOFTWARE RESET REGISTER — 8/16-bit 6F90 (H)

Writing to this location (data field = don't care) will RESET only the BC/RT section of the EXC-1553VME/E-V card. In addition, the Dual Port Ram used in the RT mode of operation will be cleared to "0". The Board Status, the Board ID, Firmware Revision and Variable Amplitude registers are written by the board after the reset operation has been completed.

BOARD CONFIGURATION REGISTER — 8-bit 6FFF (H)

The operating mode of the board is set via this register. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

HEX VAL	7	6	5	4	3	2	1	0	
01	0	0	0	0	0	0	0	1	BC MODE
02	0	0	0	0	0	0	1	0	RT MODE
04	0	0	0	0	0	1	0	0	BC / CONCURRENT-RT
08	0	0	0	0	1	0	0	0	reserved
10	0	0	0	1	0	0	0	0	reserved
20	0	0	1	0	0	0	0	0	reserved
40	0	1	0	0	0	0	0	0	reserved
80	1	0	0	0	0	0	0	0	reserved
ED	1	1	1	0	1	1	0	1	reserved
FF	1	1	1	1	1	1	1	1	reserved

BOARD ID REGISTER — 8-bit 6FFE(H)

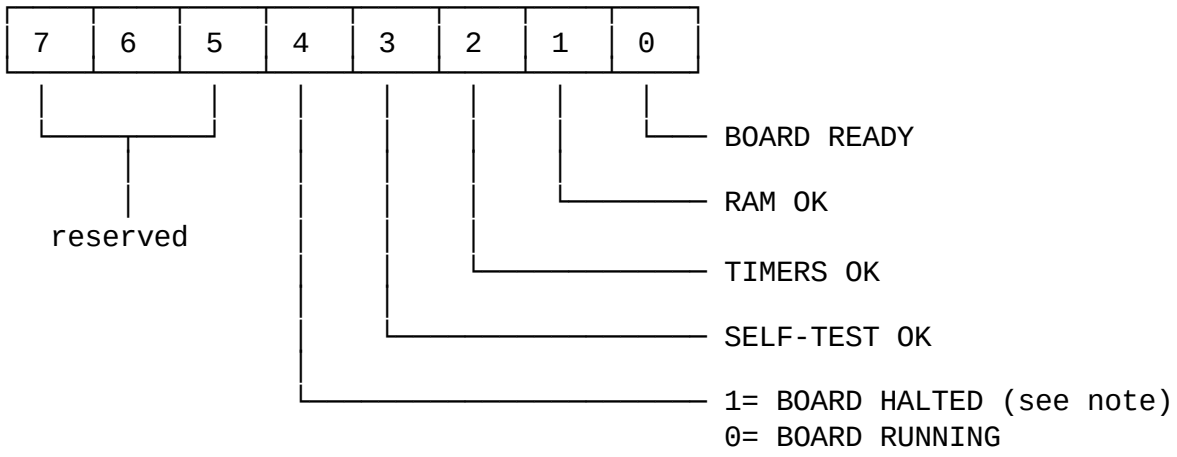
This register contains a fixed value which can be read by a user's initialization routine to detect the presence of the card. The one-byte value of this register is: 45 (Hex) ; ASCII "E".

RT Mode

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BOARD STATUS REGISTER 8-bit 6FFD (H)

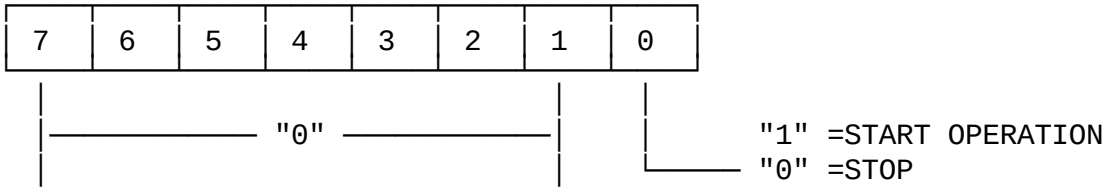
This register indicates the status of the EXC-1553VME/E-V card. In addition, this register indicates options as defined below (Status bits are active "1").



NOTE: Bit "04" (Board Halted) is set by the board after the user "stops" the current operation (by resetting the START bit within the Start Register). The user must check this bit first before modifying registers which first require a "STOP" operation. The board resets this bit after receiving a subsequent START command (by writing to the Start Register). The condition of this bit after power-on or software reset is a logic "1".

START REGISTER 8-bit 6FFC (H)

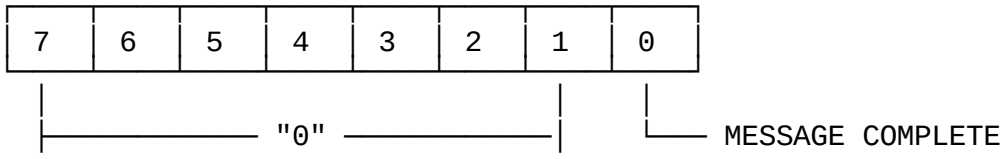
This register controls the "START / STOP" operation of the card. The user can Start then Stop the RT operation, modify RT parameters (example: the Error Injection register or Response Time), and then re-issue a new Start in real-time. See note on the Board Status Register (Board Halted/Running) Bit 04.



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MESSAGE STATUS REGISTER	8-bit 6FFA (H)

This register indicates that a 1553 message has been received. The figure below illustrates the placement of the status bit. A logic "1" indicates active condition (bit is also set for messages with errors).



Note: Message Complete bit is NOT reset by the board and should be reset by the user after reading it.

TIME TAG RESOLUTION REGISTER	8-bit 6FF6 (H)

This 8-bit value represents the resolution of the Time Tag Counter in increments of 4 µsec. See Time Tag description above. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

The Time Tag Resolution is implemented using an on-board hardware timer circuit. This timer has a resolution of 4µsec per bit. The equation to determine the resolution of the Time Tag is: (register value+1) * 4µsec.

Examples:
register value = 0 --> 4µsec resolution time
register value = 4 --> 20µsec resolution time

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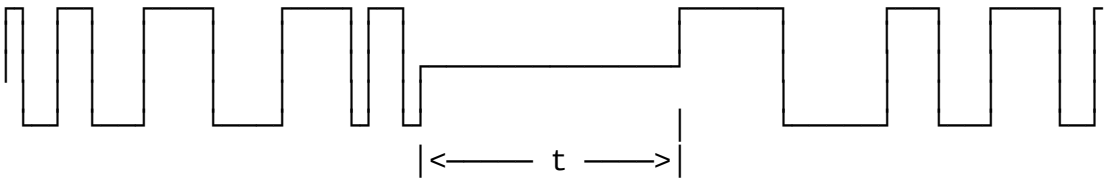
BIT COUNT REGISTER 8-bit 6FF5 (H)

Sets the number of total bits within the 1553 Data word ; including Sync(3) & Parity(1). This register is utilized by the board only if the "Bit Count Error bit" is set within the Error Injection Register. If the bit is not set, then a [valid] 20 bit word is transmitted regardless of the contents of this register. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

7	6	5	4	3	2	1	0	# of bits	
<———— `0' ————>					0	0	0	18	-2
					0	0	1	22	+2
					0	1	0	19	-1
					0	1	1	20	
					1	0	0	21	+1
					1	0	1	17	-3
					1	1	0	23	+3

RT RESPONSE TIME REGISTER 8-bit 6FF3 (H)

This register sets the RESPONSE TIME of the Remote Terminal. The resolution of this register is 155 nsec. per bit. This time is measured as the "DEAD TIME" on the 1553 bus. The minimum time is equal to approximately 4.0 µsec.
Write a "00" in order to use the minimum response time. Any value above zero will result in a response time equal to 4µsec plus the contents of the register. The actual Response Time will be +/- 1µsec tolerance. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see: START Register).

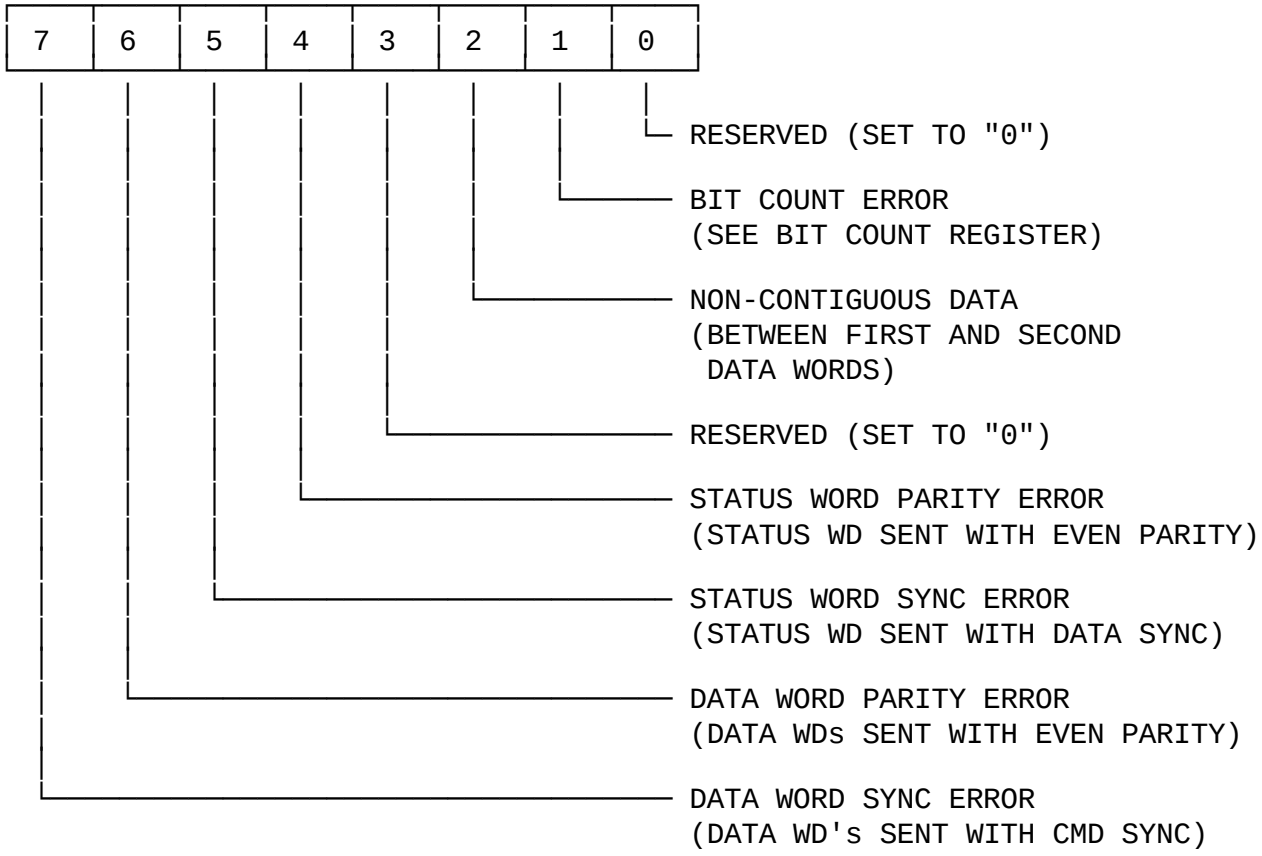


Example: To request a response time of 9 µsec write 32 to this register.
32 * 0.155 = ~5 µsec + 4 µsec = 9 µsec

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ERROR INJECTION REGISTER	8-bit 6FEE (H)

The Error Injection register is a global register which allows the user to select the type of error to be injected within a transmitted message. This register is read by the board upon the receipt of a "START" (by writing to the Start Register). To modify this register: issue a "STOP", modify and then re-issue a START (see: START Register).



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VARIABLE AMPLITUDE REGISTER — 8-bit 6FF2 (H)

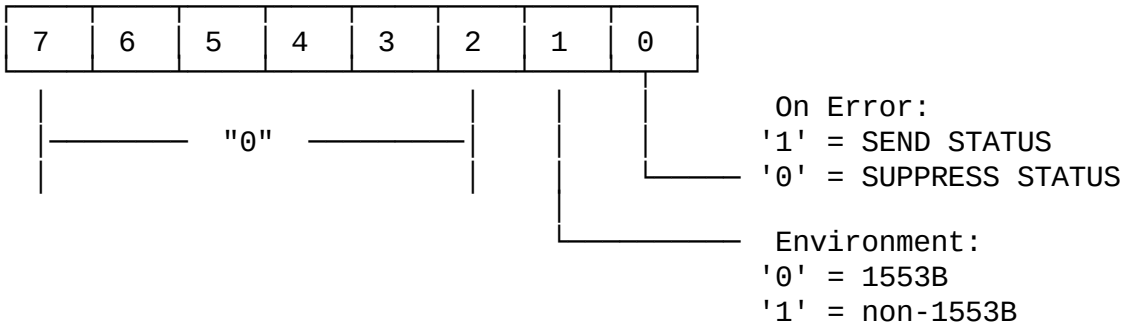
This register specifies the amplitude of the 1553 output signal. The signal can be programmed from 0 volts up to 7.5volts (p-p) - measured on the 1553 bus with specified 1553 coupling and 35ohm load (two 70 ohm termination resistors were used). A higher Transmit [output] amplitude will appear on the 1553 bus if 78 ohm termination resistors are used. The register has a resolution of 30mv/bit (p-p) on the bus. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register). This Register defaults to FFH after Reset, providing maximum amplitude.

MESSAGE STACK POINTER — 16-bit 6FF0 (H)

The Stack Pointer indicates the Message Stack position. This pointer is updated (incremented by 6) after the entire message has been received. This word "circulates" with the Message between 6200(H) to 6DFE(H). It is initialized to 6200 (H).

STATUS RESPONSE REGISTER — 8-bit 6FED (H)

This register is used to control the Status Response mode of operation.
The user can select to respond with a 1553 Status Word [following a receive message] EVEN if an INVALID 1553 Data Word was received. The user can also select the 1553 environment which affects some 1553 RT STATUS WORD bits (see 1553 RT STATUS WORD section). This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).



FIRMWARE REVISION REGISTER — 8-bit 6FE7 (H)

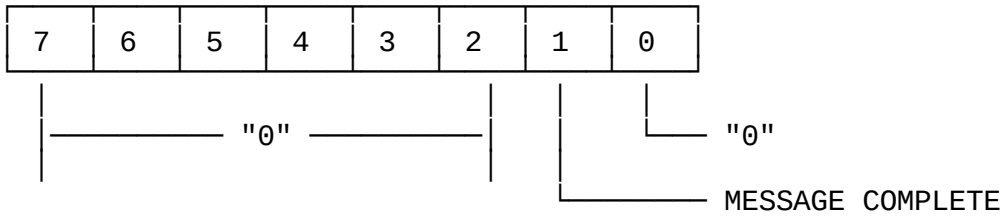
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This register indicates the revision level of the on-board firmware. The value 0001 0010 would be read as revision level: 1.2

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INTERRUPT CONDITION REGISTER — 8-bit 6FEC (H)

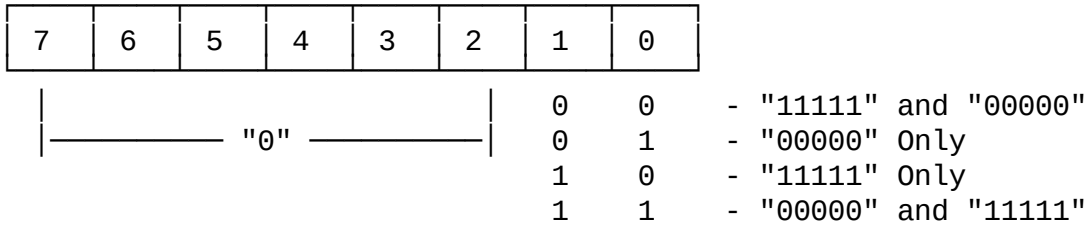
This register allows the user to enable an interrupt trigger. A logic '1' enables the interrupt condition. When Message Complete is enabled an interrupt will be generated at the end of processing for every message directed to an RT being simulated by the board for which the Interrupt Bit in its Active RT Lookup Table entry has been set. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).



Note: The interrupt will be sent at the end of the message.

MODE CODE CONTROL REGISTER — 8-bit 6168 (H)

This register allows the user to determine which 1553 Subaddress value indicates the reception of a 1553 Mode command. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).



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BC / CONCURRENT-RT MODE OPERATION

The EXC-1553VME/E-V can operate as the Bus Controller and up to 32 Remote Terminals. The user loads the messages and the Instruction Stack as per the BC Operation.

In the Concurrent RT Mode, the user also loads the message blocks with the RT's 1553 Status and data words. These words must be loaded into the appropriate locations within the message blocks - in the sequence that the 1553 words appear on the 1553 bus.

NOTE : THIS IS ONLY FOR THOSE REMOTE TERMINALS WHICH THE USER IS ACTIVELY SIMULATING !! For those RT's which are not ACTIVE (not simulated by the EXC-1553VME/E-V within a single message), the user must leave the related locations blank within the associated 1553 message blocks.

The Remote Terminals simulated in this mode have a minimum Response Time of approximately 4µsec. (measured as: "dead time" on the bus).

NOTE:

The user should use the following sequence to determine whether the board is installed AND ready to operate:

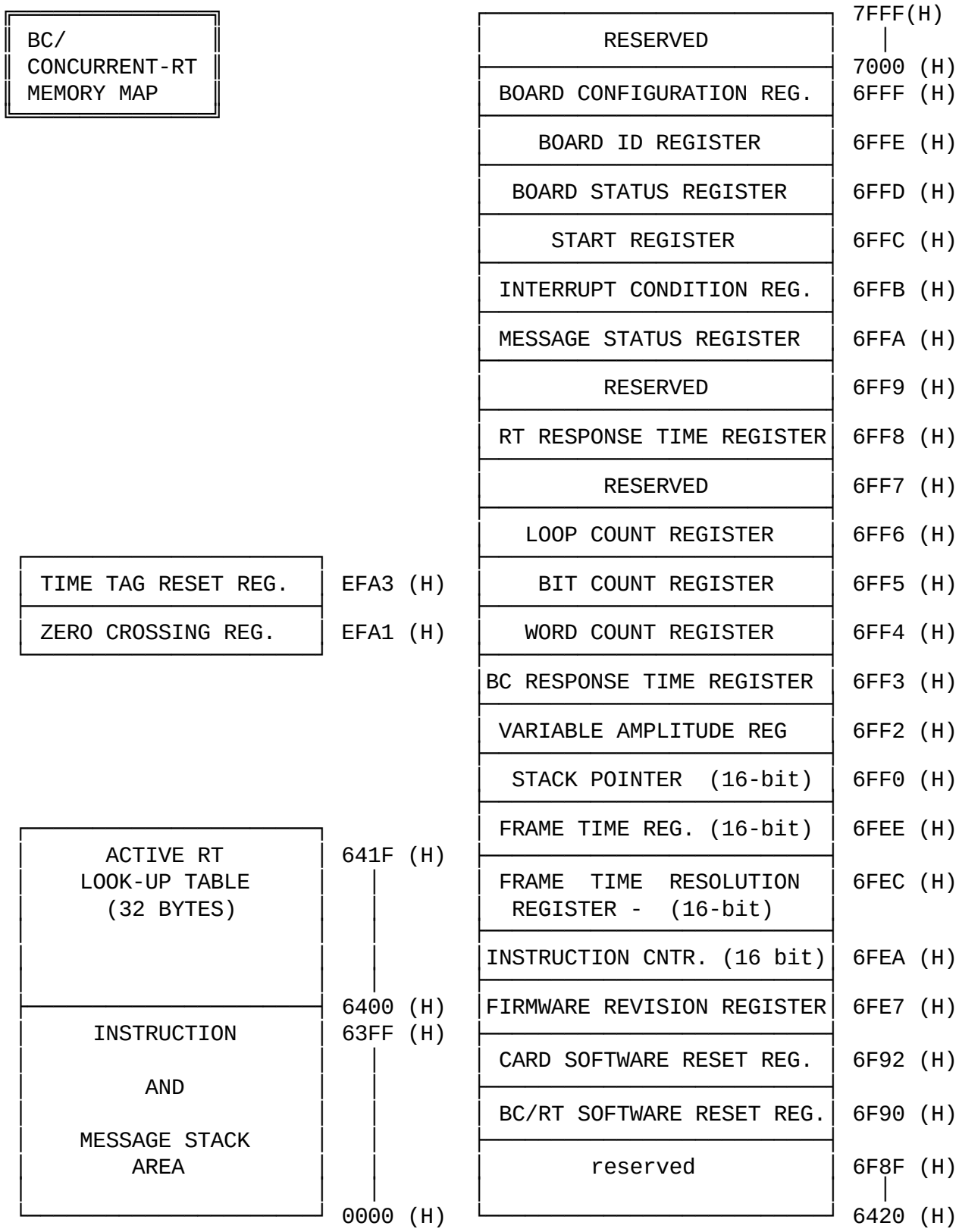
* Check the Board ID register (test for value = 45 Hex)

* Check Board Status Register (test for Board Ready bit = "1")

The board is installed and ready when BOTH of these registers contain the correct values (as written above). This sequence should be used after power-on and Software Reset operations. For Software Reset operations, these values should be set to ZERO by the user immediately prior to writing to the Initialization Register.

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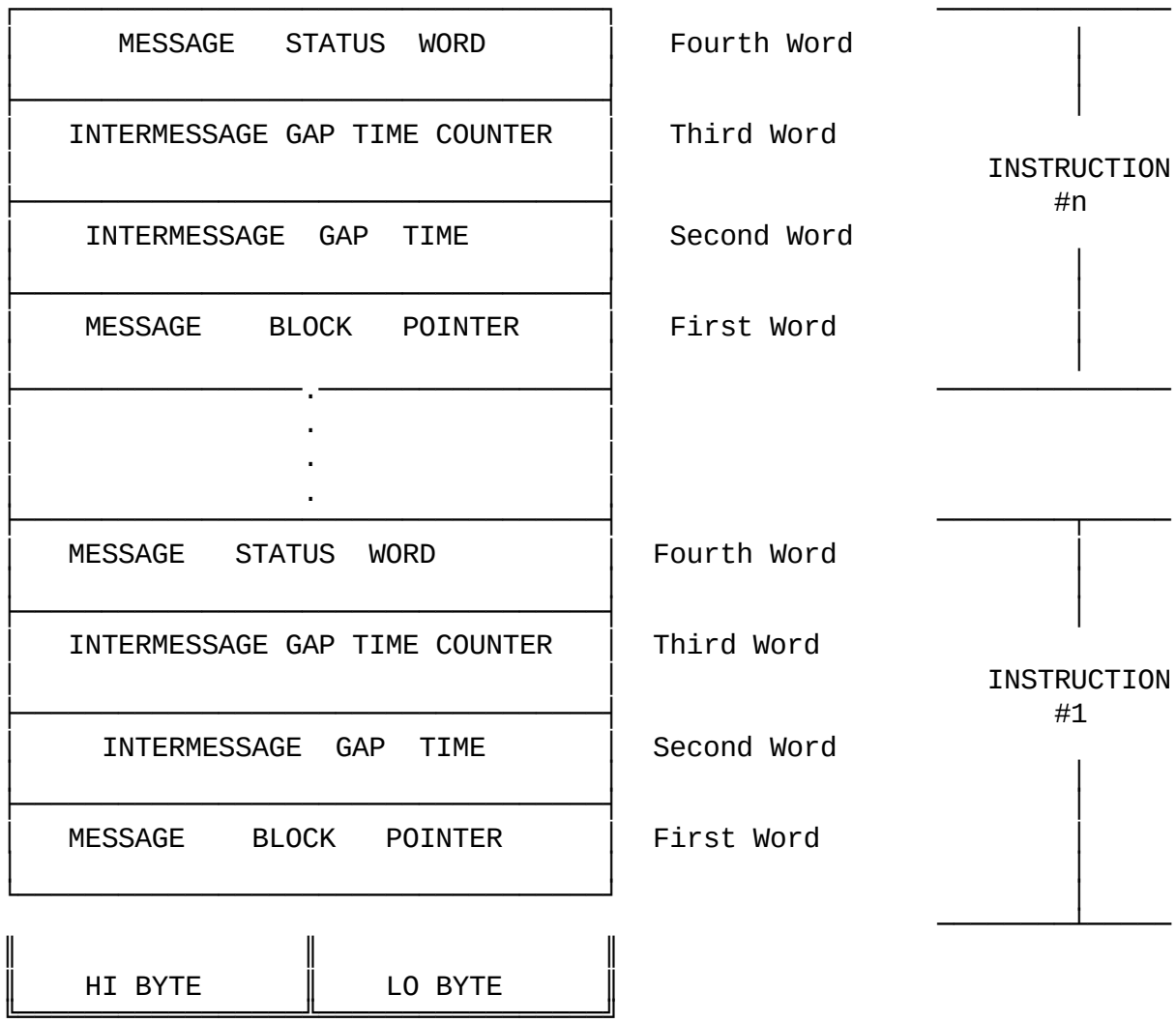
The following figure below shows the memory map of the EXC-1553VME/E-V in the BC/Concurrent-RT Mode of operation.



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INSTRUCTION STACK

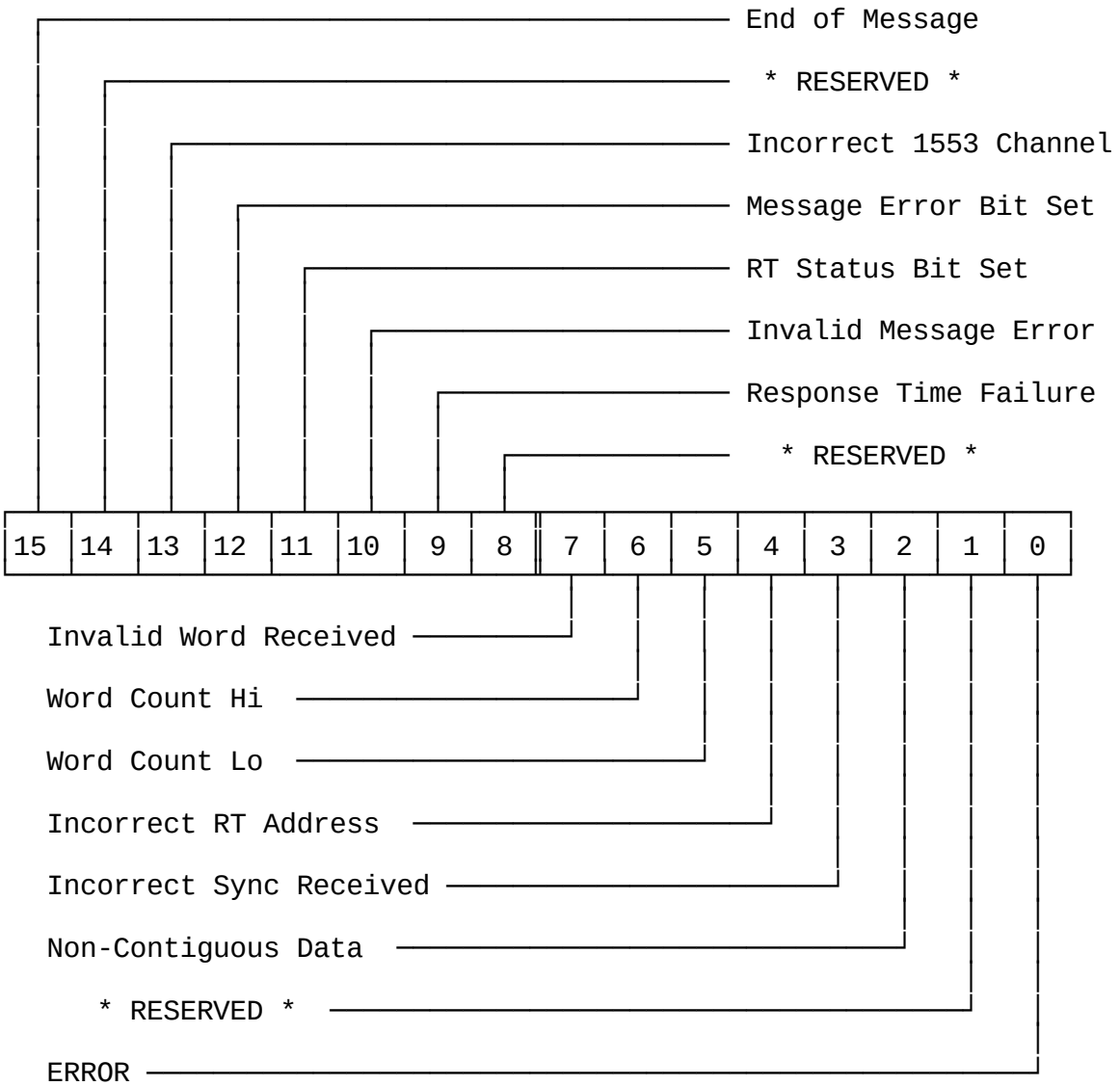
The user programs the EXC-1553VME/E-V via the Instruction Stack. The stack is divided into instruction blocks - each containing four words. The figure below illustrates the instruction blocks.



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MESSAGE STATUS

The Message Status Word indicates the status of the message transfer. This word is created by the Board and is NOT the 1553 "STATUS WORD". The contents of the Message Status word is shown below:



NOTE: A LOGIC "1" INDICATES OCCURRENCE OF STATUS FLAG

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Message Status Word Definitions:

15	END OF MESSAGE	Indicates that the message transfer has been completed
14	RESERVED	Set to logic '0'
13	INCORRECT CHANNEL	Indicates that the remote terminal response was not received on the active 1553 channel
12	MESSAGE ERR. BIT SET	Indicates the 'MESSAGE ERROR BIT' (bit '10') within the RT status word was set
11	RT STATUS BIT SET	Indicates that a bit was set within the RT status word (other than the 'MESSAGE ERROR BIT')
10	INVALID MESSAGE	Indicates that a 1553 'message level' error occurred (i.e. Word count, incorrect sync - detailed below)
09	RESPONSE TIME ERROR	Indicates that the RT responded late (see: Programmable BC Response Time Register)
08	RESERVED	Set to '0'
07	INVALID WORD	Indicates the reception of at least one invalid 1553 word (i.e. Bit count, manchester code, parity)
06	WORD CT HI	Indicates that the RT transmitted too many words
05	WORD CT LO	Indicates that the RT transmitted too few words
04	INCORRECT RT ADDRESS	Indicates that the received 1553 status word did not contain the correct 'RT address'
03	INCORRECT SYNC	Indicates that the sync of either the status or data word(s) was incorrect
02	NON-CONTIGUOUS	Indicates occurrence of an invalid gap between received 1553 words
01	RESERVED	Set to logic '0'
00	ERROR	Indicates the occurrence of an error (defined within one of the other message status bit locations)

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| Intermessage Gap Time Value | Written by user

The Intermessage Gap Time Value is a sixteen bit word which allows the user to insert a unique intermessage delay time between the current message and the next message. The minimum Intermessage Gap Time is approximately 4µsec measured as dead time on the bus. The value in the word is ADDED to this minimum time. The resolution of this word is 155 nanoseconds per bit.

| Intermessage Gap Time Counter | Written by user

The Intermessage Gap Time Counter (IGT_Counter) is a sixteen bit word which allows the user to increase the Intermessage Gap Time by repeating the number of times the Intermessage Gap Time Value is used. If the counter equals "0", for example, then the gap time is NOT repeated and is per the contents of the Intermessage Gap Time location. For example, if the gap time counter equals "1" then the gap time is repeated once and equals the Intermessage gap time value x 2.

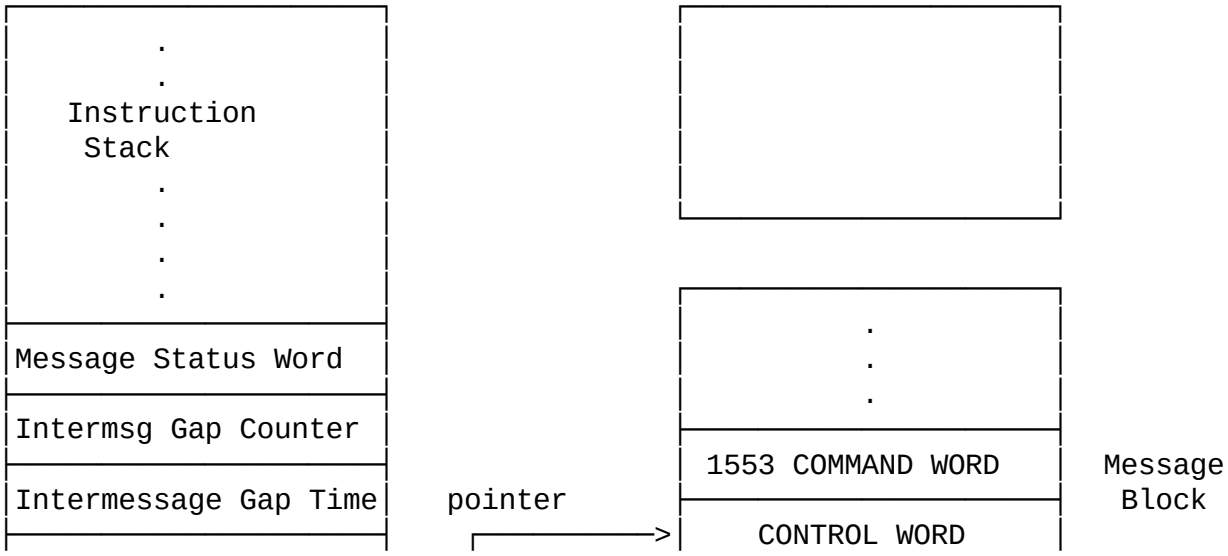
Note: To ensure maximum intermessage gap time accuracy when using the IGT_Counter, the value within the Intermessage Gap Time Word should be maximized and that within the IGT_Counter minimized, for a given desired intermessage gap time.

| Message Block Pointer | Written by user

The Message Block Pointer is a sixteen bit word which points to the beginning of a 1553 Message. The pointer value must be even (LSB set to 0).

Example :

(1) User writes message starting at address: 2000 (H)
(2) write 2000(H) to the Message Block pointer location



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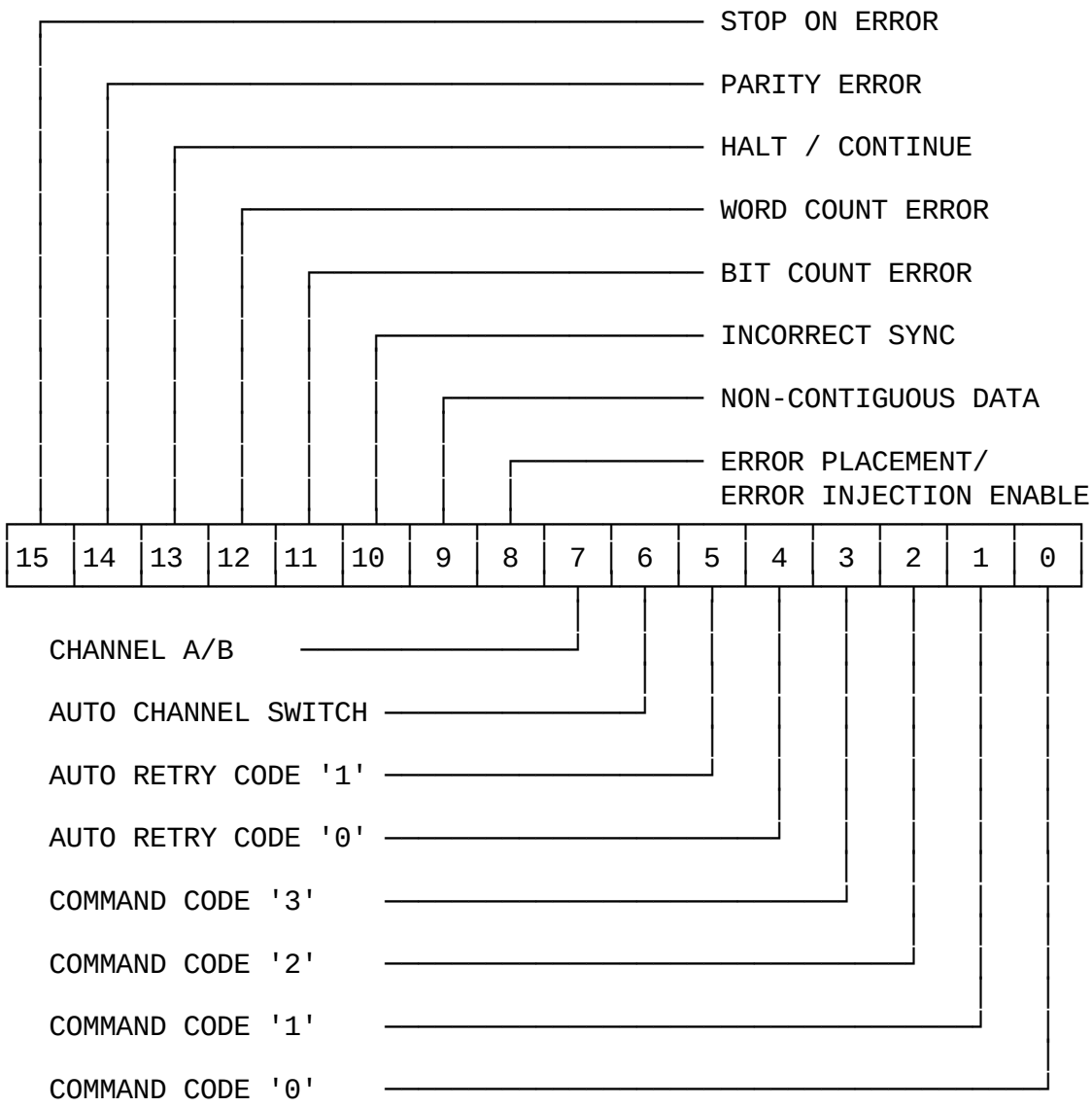
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MESSAGE BLOCK

The user loads the Message Block anywhere within the Instruction STACK/MESSAGE BLOCK AREA (see: Memory Map). Message Blocks do NOT have to be stored in sequential locations within the memory since the Message Block Pointers "point" to the Message Blocks in sequence.

Each block contains a 1553 message plus its Control Word. This Control Word is written into the FIRST location of each block. The Control Word instructs the EXC-1553VME/E-V as to the type of message to be transmitted (i.e. RT to RT, Mode Code, Broadcast, Error injection, etc.). The size of the message block is not fixed and is dependent upon the size of the message itself.

Control Word



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NOTE : A LOGIC '1' ENABLES THE FUNCTION, A '0' DISABLES THE FUNCTION.

BC/RT Mode

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Control Word Definitions:

15	Stop on Error	Message error stops the BC operation. The user can restart by writing to the instruction count and "START".
14	Parity Er	Selects 'Even' parity within 1553 word
13	Halt / Continue	1= HALT. This stops BC transfer operation. This bit MUST BE reset ('0') in order to RUN or CONTINUE. (see text)
12	Word Count Error	Transmits fewer or more words than are indicated by the WORD COUNT field (see: Word Count Register). This function is valid for 'BC to RT' messages only.
11	Bit Count Error	Transmits invalid number of bits within 1553 words (see: Bit Count Register)
10	Incorrect Sync	Transmits incorrect sync. Data-type sync is transmitted within the command word
09	Non-Contg Data	First 1553 data word is transmitted with invalid gap time (between command and data word)
08	Error Placement / Error Injection Enable	For BC to RT, BROADCAST RECEIVE and MODE CODE with DATA messages, this bit selects the 'Parity', 'Sync' and 'Bit Count' errors injection placements; '0' - in Command word '1' - in Data words For other error injection types or other message types this bit must be set to enable error injection
07	CHANNEL A / B	Selects active 1553 channel. Logic '1' selects channel 'A' while a logic '0' selects channel 'B'
06	Auto Chnl Switch	On error, the BC will retry message transfer on alternate channel (* auto-retry must be selected *)
05-04	Auto Rtry Code	On error, selects the number of retries before transfer of next message Code _1 _0 0 0 -No Retry 0 1 - 1 Retry 1 0 - 2 Retry 1 1 - 3 Retry
03-00	COMMAND CODE	0000 - TRANSMIT COMMAND (RT to BC) 0001 - RECEIVE COMMAND (BC to RT) 0010 - RT to RT COMMAND 0011 - MODE CODE 0100 - BROADCAST RECEIVE COMMAND 0101 - BROADCAST RT to RT COMMAND 0110 - BROADCAST MODE CODE

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		0111 - SKIP MESSAGE (see text)	
		1000 - JUMP COMMAND (see text)	

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HALT Bit Operation

The user normally sets this bit to a logic "0" before writing to the Start Register. The user may ,in real time (during execution), set this bit (to a logic '1'). The board, when operating on that particular Message Block's Control Word, will HALT transfer operations until the bit is reset to a logic '0'.

When the board detects that the HALT bit is set, it sets the "WAIT FOR CONTINUE" bit within the Message Status Register (see: Control Register Definitions Section). This bit can be used by the user in order to know when the board has arrived at this Message block. When the board detects that the Halt bit has been reset by the user (continue mode), the board will then reset the "WAIT FOR CONTINUE" bit within the Message Status Register and continue BC/RT operation.
It is important to note that this function can only be implemented within Message Blocks which have NOT [AS YET] BEEN EXECUTED BY THE BOARD.

Note: This operation can be used in conjunction with the JUMP feature described below.

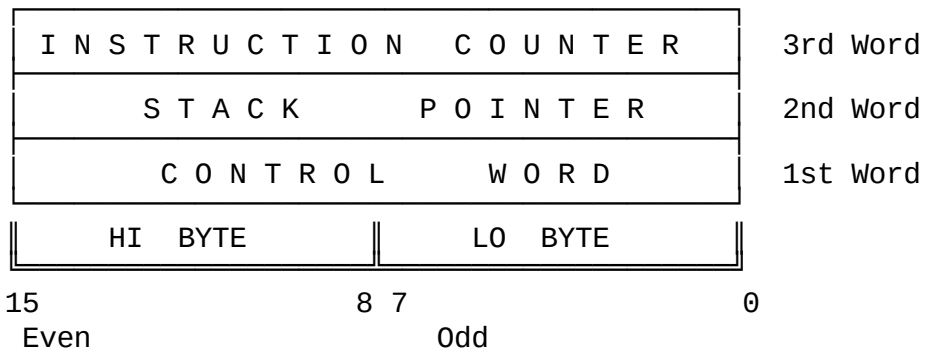
SKIP Message Operation

The SKIP MESSAGE command allows the user to easily skip a message defined in a certain Message Block by only modifying the Command field within the Control Word. This allows the user to selectively send a message within the current frame. The Intermessage Gap Time associated with the SKIP Message has no effect.

JUMP Command Operation

The EXC-1553VME/E-V allows the user to modify the BC transfer cycle by setting the "JUMP" command within the BC Control Word. The Jump command instructs the board to operate on a NEW instruction stack or NEW stack entry within the same stack. This Control word is followed by a Stack Pointer word instead of the usual 1553 Command Word. In addition, the Stack Pointer is followed by an Instruction Count value. The Jump command is tested AFTER the board has tested the HALT/CONTINUE bit within the Control Word. The Intermessage Gap Time associated with the JUMP Command has no effect.

The memory location sequence is illustrated below:



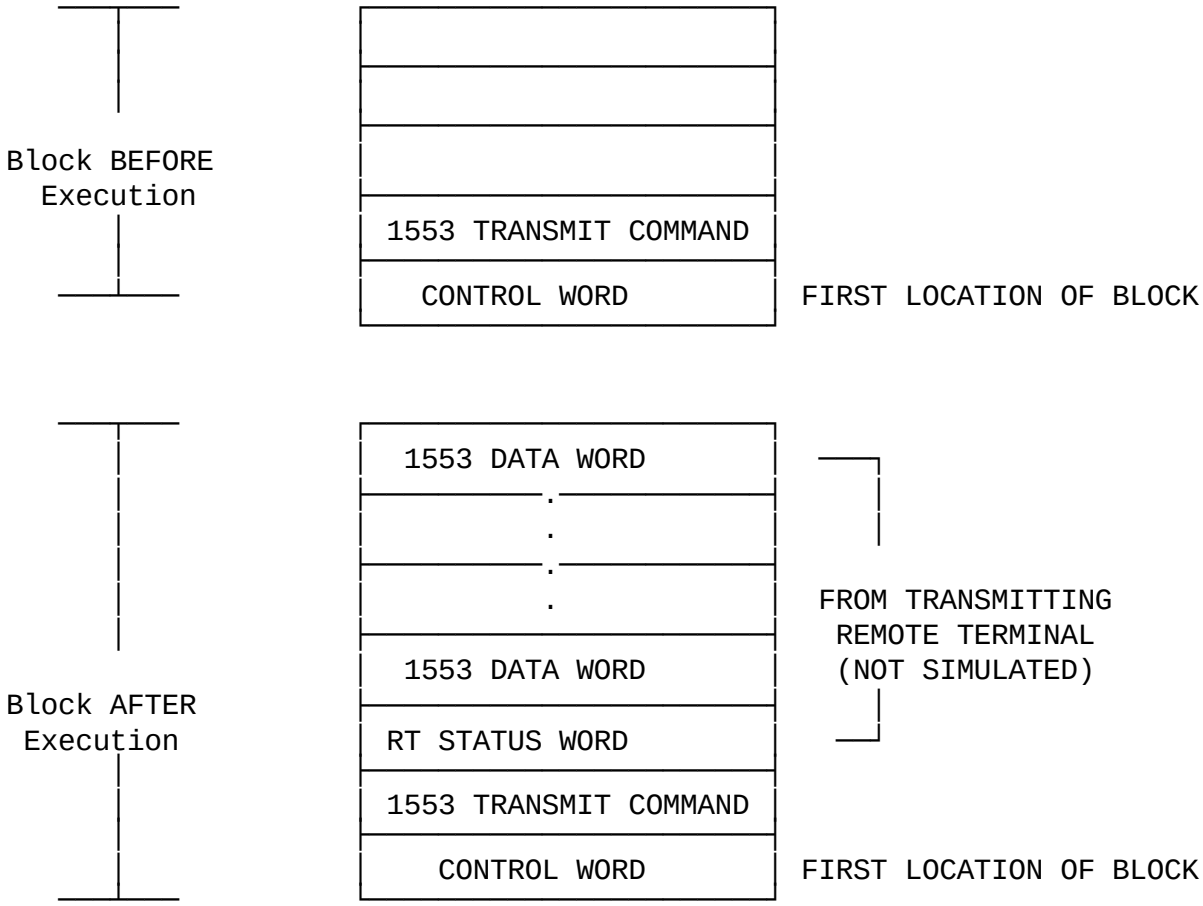
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MESSAGE BLOCK FORMATS

The Message Block contains, or will contain, the entire 1553 message as it appears on the 1553 bus - including Command Word(s), Data Words, and Status Word(s).

Examples #1

TRANSMIT COMMAND
OPERATING AS BC ONLY

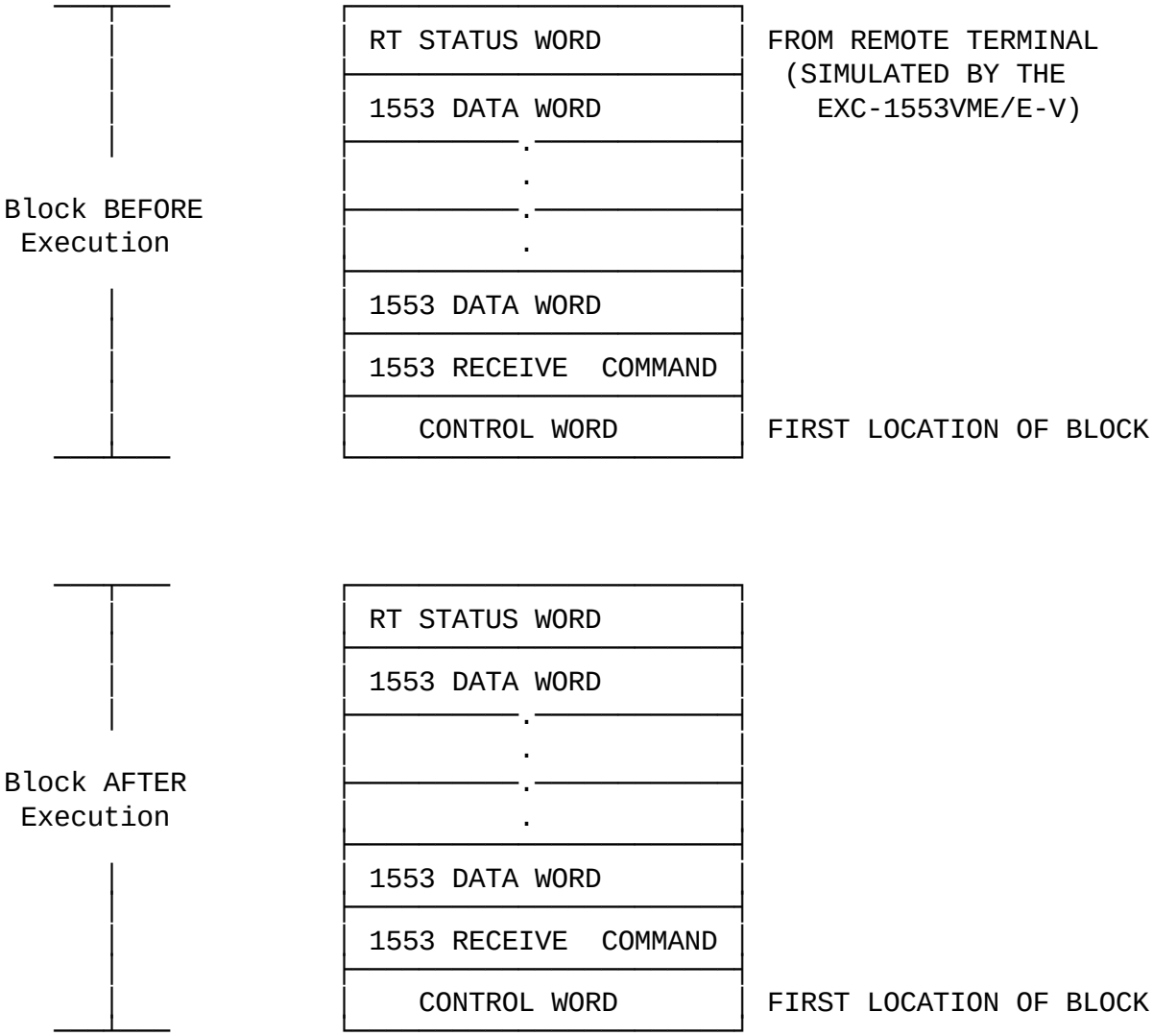


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Examples #2

RECEIVE COMMAND

OPERATING AS BOTH BC AND RECEIVING RT

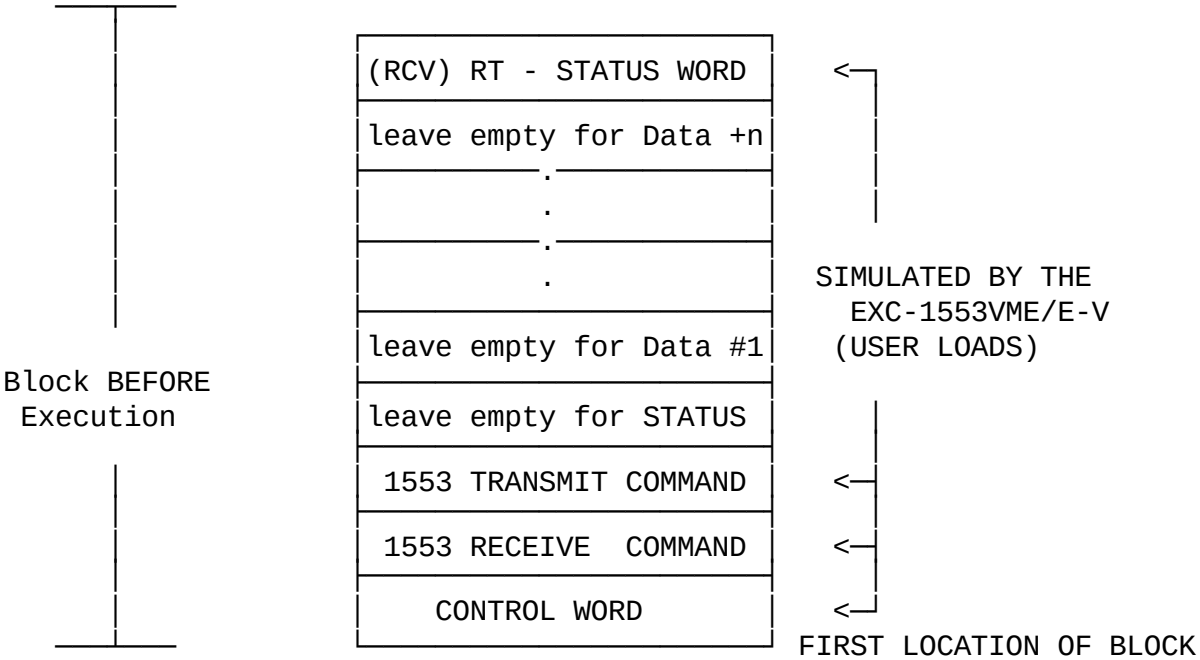


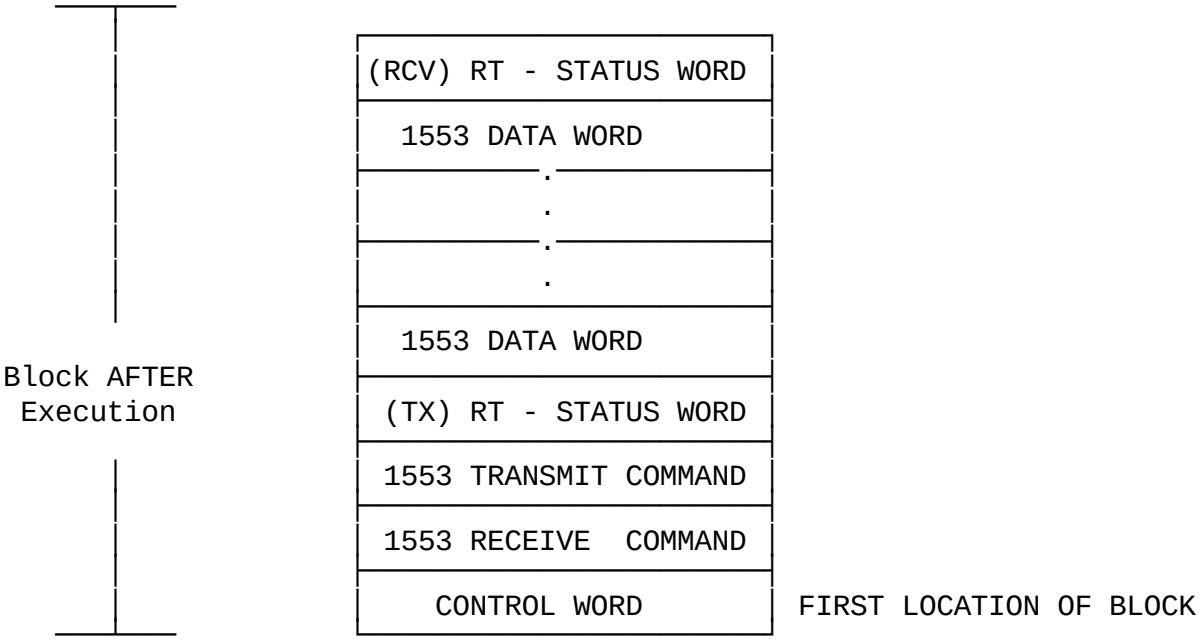
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Examples | #3

RT to RT COMMAND

OPERATING AS BC and RECEIVING RT



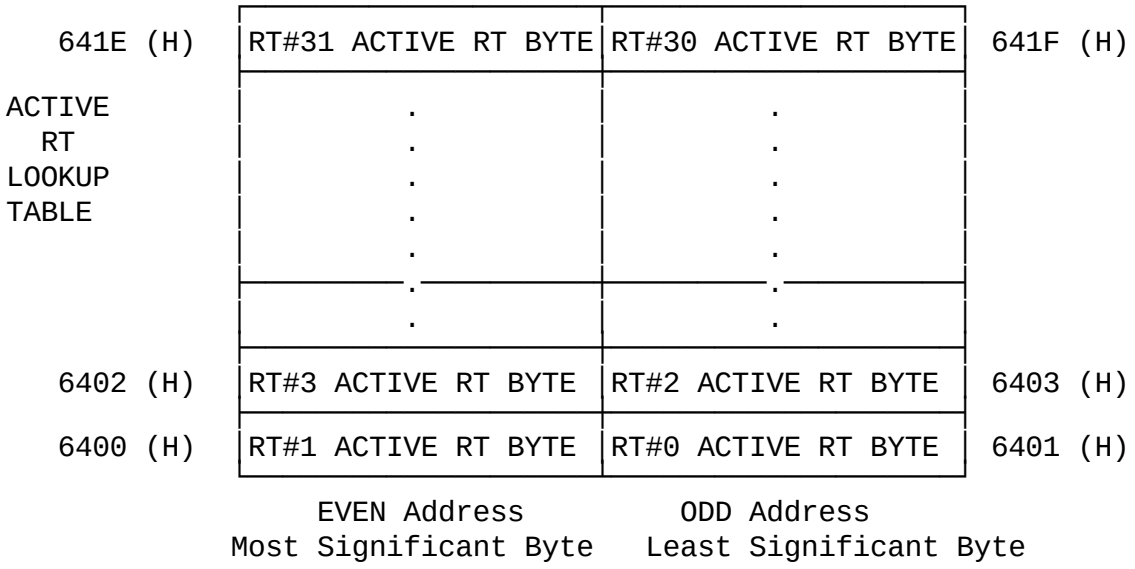


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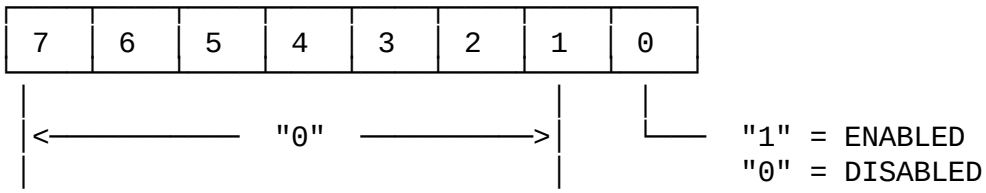
REMOTE TERMINAL SIMULATION

In the case where the board is simulating both the Bus Controller and one or more Remote Terminals, the user must write [into the Message Block] the simulated Remote Terminal 1553 Status Word and data word(s) in the sequence in which it appears over the 1553 bus (see MESSAGE BLOCK FORMATS).

The user instructs the board as to which Remote Terminals are to be simulated by writing to the (32-byte) Active Remote Terminal Look-Up Table. Each entry within the 32-byte table relates to a specific Remote Terminal. The first location relates to RT #00, while the last location relates to RT #31 (for a total of 32 locations). Writing a value "01" to the table entry ENABLES the Remote Terminal simulation by the board. A value of "00" written to the table disables the simulation by the board (note that the first Active RT BYTE resides in the first [least significant] byte - which is an ODD address, followed by the EVEN address).



ACTIVE REMOTE TERMINAL BYTE FORMAT:



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CONTINUOUS or ONE-SHOT MODES

The EXC-1553VME/E-V offers the capability of transferring all programmed messages once, in a continuous loop, or for 'N number of times'.

In the One-Shot mode, the board transfers all messages [after receipt of a "START" command], sets the Message Complete Bit within the Message Status Register, issues an Interrupt [if programmed] and waits for a new "START". This mode is selected via the Start Register (see Control Register definitions).

In the 'N' Times Mode, the user loads the Loop Count Register with the number of times to transmit the messages [frame] and sets the LOOP and START bits within the Start Register. The user can select to transmit from one to 255 times (see: Start and Loop Count Registers). The time between frames is predetermined via Frame Time Register (see below).

In the Continuous mode, the EXC-1553VME/E-V will re-transmit the message frame at a predetermined, user-programmable rate. This mode is selected via the Start Register and the Loop Count Register (see Register definitions). In this mode, all messages relating to the [active] Stack Pointer and Instruction Counter are continuously "looped" until the user halts the board's operation (see Start Register definition).

The "loop" time or Frame Time is a function of two Control registers; the Frame Time Register and the Frame Time Resolution Register. The internal Frame Time counter is loaded upon receipt of a "START" command with the 16-bit value found within the Frame Time Register. The Frame Time counter is decremented every N x 155 nsec - where N is the value of Frame Time Resolution Registers (Hi and Lo). After the execution of all instructions (1 frame), the EXC-1553VME/E-V will wait until the internal Frame Time Counter reaches ZERO before re-transmitting the next frame.

NOTE: If the Frame time is less than the time required to transmit all messages [within 1 frame], the subsequent frames will be transmitted with the minimum delay between them. The minimum delay is 20 µsec approximately measured as dead time on the bus.

The user can implement the desired Frame time by programming the appropriate combinations of the two registers. An example using one method is illustrated below.

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EXAMPLE:

Given: User requires a Frame Time of 500msec.

Operation:

Select Frame Time Resolution of 3225 (Dec) ----- 0C99(H).
Frame Time Resolution = 3225 x 155 nsec. = 500 usec (.5 msec)

Subsequently; the Frame Time Register value must equal to :

(500 msec (desired time) / .5 msec = 1000 (Dec))-1 --> 03E7(H)
Count-1

Load Frame Time Register = 03E7 (H) (before "START")
Load Frame Time Resolution Register = 0C99 (Hex) (" ")

MODE CODES

The EXC-1553VME/E-V handles all Dual-Redundant 1553B Mode Codes. This is to say that the Word Count field is decoded according to MIL-STD-1553B. The two quad-redundant mode codes, "Selected Transmitter Shutdown" and "Override Selected Transmitter Shutdown" are not implemented by the board.

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PROGRAM EXAMPLE BC/CONCURRENT-RT MODE

```
10 POKE  &H6FFF,04       ' LOAD CONFIGURATION REG. = BC/RT MODE
20 POKEW &H6FF0,0000     ' LOAD STACK POINTER REGISTERS WITH "0000"
                         ' (STACK NOW BEGINS AT ADDRESS:0000)

30 POKE &H6FF2,xx        ' LOAD VARIABLE AMPLITUDE REGISTER

40 POKEW &H00,0100       ' POINTER TO FIRST MESSAGE (LOCATION OF MESSAGE
                         ' IS 0100(H) )
60 POKEW &H02,xxxx       ' LOAD INTERMESSAGE GAP TIME LOCATION

80 POKEW &H08,&H0140     ' POINTER TO SECOND MESSAGE (LOCATION OF MESSAGE
                         ' IS 0140(H) )
100 POKEW &H0A,xxxx      ' LOAD INTERMESSAGE GAP TIME LOCATION

120 POKEW &H100,&H0080   ' LOAD CONTROL WORD WITH: TX COMMAND, BUS A,
                         ' AND NO ERRORS INJECTED
140 POKEW &H102,&H0C23   ' LOAD COMMAND WORD: 0C23

160 POKEW &H140,0002     ' LOAD CONTROL WORD WITH: RT to RT COMMAND, BUS B,
                         ' AND NO ERRORS INJECTED
190 POKEW &H142,&H0823   ' LOAD  FIRST [RECEIVE] COMMAND WORD: 0823
210 POKEW &H144,&H0C43   ' LOAD SECOND [TRANSMIT] COMMAND WORD: 0C43

230 POKEW &H6FEA,2       ' LOAD INSTRUCTION COUNTER WITH "2" (2 MESSAGES)

235 POKEW &H6FEC,xxxx    ' LOAD FRAME TIME RESOLUTION REGISTERS

245 POKEW &H6FEE,xxxx    ' LOAD FRAME TIME REGISTERS

                         ' ENABLE RT's VIA THE RT [ACTIVE] LOOK-UP TABLE.
                         ' BOARD WILL SIMULATE THESE REMOTE TERMINALS
260 POKE &H6400,1        ' ENABLE RT#1
270 POKE &H641F,1        ' ENABLE RT#30 (DECIMAL)

290 POKE &H6FFC,1        ' LOAD START REGISTER WITH "1". STARTS MESSAGE
                          TRANSFERS IN ONE-SHOT MODE.

300 STOP
```


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CONTROL REGISTER DEFINITIONS

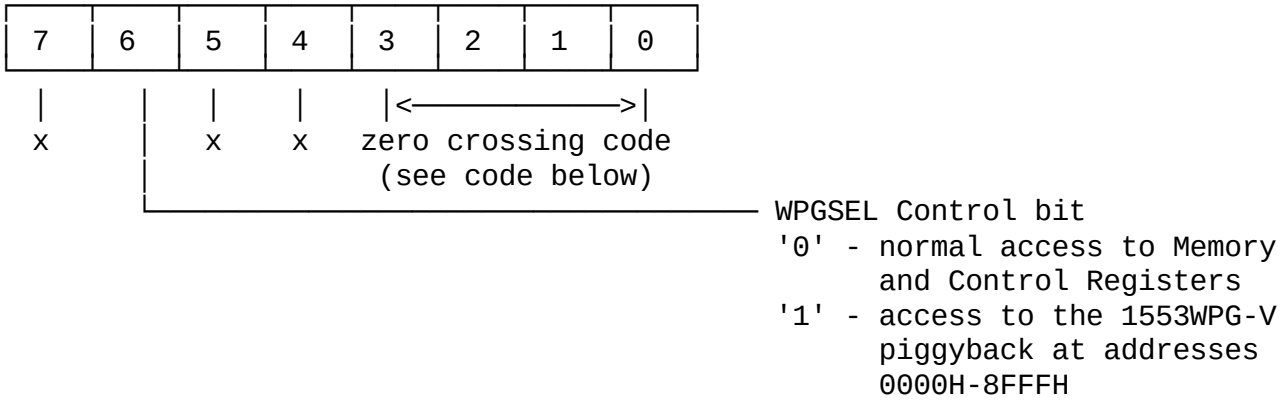
TIME TAG RESET REGISTER — 8-bit EFA3 (H)

Writing to this register (data field = don't care) will reset the RT hardware Time Tag counter. The counter will start to count from 0 immediately after the reset.

Note: The Time Tag counter is not used in the BC/CONCURRENT-RT Mode.

ZERO CROSSING REGISTER — 8-bit EFA1 (H) READ/WRITE

This register is reset at power-up (all bits set to "0").



Definition of data bits 0,1,2,3 within the register:

Bit Position: 3 2 1 0	operation:
0 0 0 0 (0)	Selects: NO zero crossing deviation (no error)
0 0 0 1 (1)	Selects:+150 nsec from '0' (border-no error)
0 0 1 1 (3)	Selects:-150 nsec from '0' (border-no error)
0 1 0 1 (5)	Selects:+190 nsec from '0' (above 1553 limit)
0 1 1 1 (7)	Selects:-190 nsec from '0' (below 1553 limit)
1 0 0 0 (8)	Selects: Manchester Hi-Bit Error
1 0 0 1 (9)	Selects: Manchester Lo-Bit Error
1 0 1 0 (A)	Selects: Manchester Dead-Bit Error

Note: When activated, these zero crossing and manchester errors are inserted into the first data bit of every word which is transmitted by the board (this includes: Command, Status and Data words). The user can modify this register at

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any time. The board checks the [code] value within the register between the transmission of each word.

BC/RT Mode

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CARD SOFTWARE RESET REGISTER — 8/16-bit 6F92 (H) WRITE ONLY

Writing to this location (data field = don't care) will RESET the EXC-1553VME/E-V card. All card functions will be reset upon writing to this register. In addition, all Dual Port Ram will be cleared to "0". The Board Status, Board ID, Firmware Revision and Variable Amplitude registers are written by the board after reset operation has been completed.

BC/RT SOFTWARE RESET REGISTER — 8/16-bit 6F90 (H) WRITE ONLY

Writing to this location (data field = don't care) will RESET only the BCRT function of the EXC-1553VME/E-V card. In addition, the Dual Port Ram used in the BCRT mode of operation will be cleared to "0". The Board Status, Board ID, Firmware Revision and Variable Amplitude registers are written by the board after the reset operation has been completed.

BOARD CONFIGURATION REGISTER — 8-bit 6FFF (H)

The operating mode of the board is set via this register. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

HEX VAL	7	6	5	4	3	2	1	0	
01	0	0	0	0	0	0	0	1	BC MODE
02	0	0	0	0	0	0	1	0	RT MODE
04	0	0	0	0	0	1	0	0	BC / CONCURRENT-RT
08	0	0	0	0	1	0	0	0	reserved
10	0	0	0	1	0	0	0	0	reserved
20	0	0	1	0	0	0	0	0	reserved
40	0	1	0	0	0	0	0	0	reserved
80	1	0	0	0	0	0	0	0	reserved
ED	1	1	1	0	1	1	0	1	reserved
FF	1	1	1	1	1	1	1	1	reserved

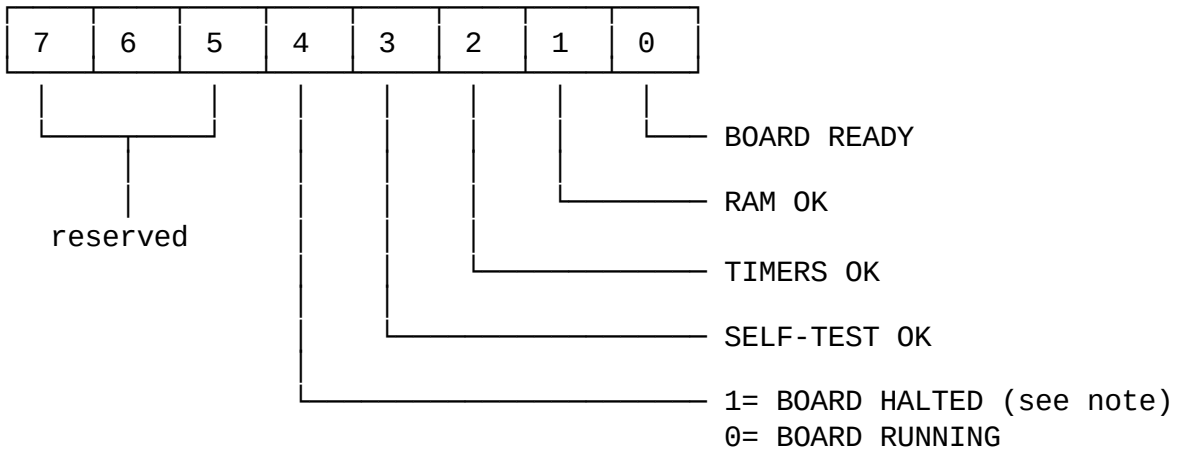
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BOARD ID REGISTER 8-bit 6FFE (H)

This register contains a fixed value which can be read by a user's initialization routine to detect the presence of the EXC-1553VME/E-V card. The one-byte value of this register is: 45 (Hex) ; ASCII "E".

BOARD STATUS REGISTER 8-bit 6FFD (H)

This register indicates the status of the EXC-1553VME/E-V card. In addition, this register indicates option selection as defined below. (Status bits are active "1").

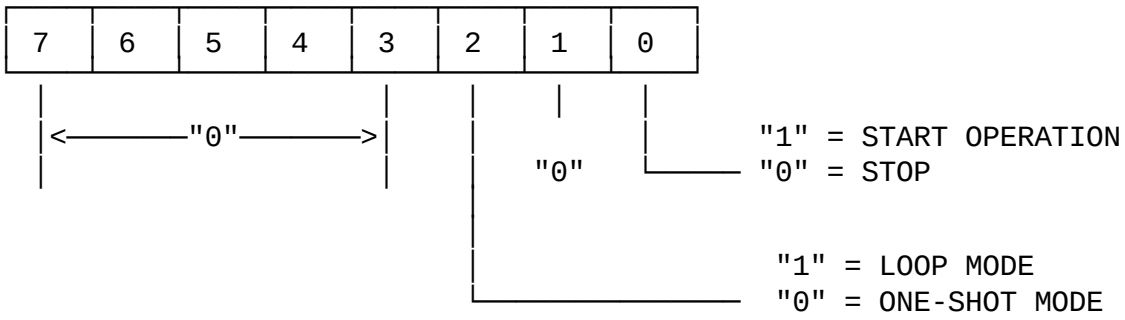


NOTE: Bit "04" (Board Halted) is set by the board after the user "stops" the current operation (by resetting the START bit within the Start Register). The user must check this bit first before modifying registers which first require a "STOP" operation. The board resets this bit after receiving a subsequent START command (by writing to the Start Register). The condition of this bit after power-on or software reset is a logic "1".

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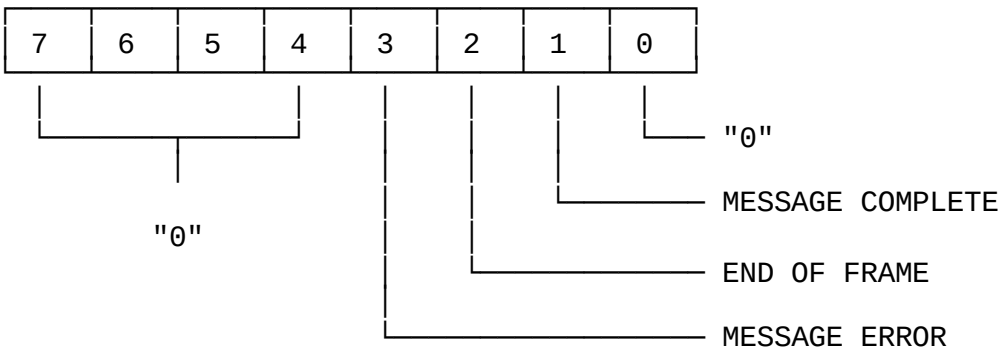
START REGISTER 8-bit 6FFC (H)

This register controls the 'START/STOP' operation of the EXC-1553VME/E-V. Writing to this register with the appropriate bit set begins the Bus Controller transfer operation. When operating in the "Loop" or "N Times" mode, the user must set the Start and Loop bits within this register. The "loop" and "N-times" number is selected via the Loop Count Register. In the One-Shot and "N-Times" modes, the board RESETS the Start bit within the register after ALL messages have been transferred. The board does not reset any bit while in the Continuous loop mode. Write "0" to bit "00" to halt the LOOP operation between messages. Write, instead, a "0" to bit "02" in order to halt the operation at the end of the entire frame (this bit is not tested between message transfers). See the related bit (data bit "04") within the Board Status Register which indicates when the board has been halted.



INTERRUPT CONDITION REGISTER 8-bit 6FFB (H)

This register allows the user to set different interrupt triggers. When a condition that has been enabled within this register occurs, an interrupt will be generated. The user may check the Message Status Register to determine which condition caused the interrupt. A logic '1' enables the interrupt condition. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).



Note: For all interrupt conditions the interrupt will be sent at the end of the

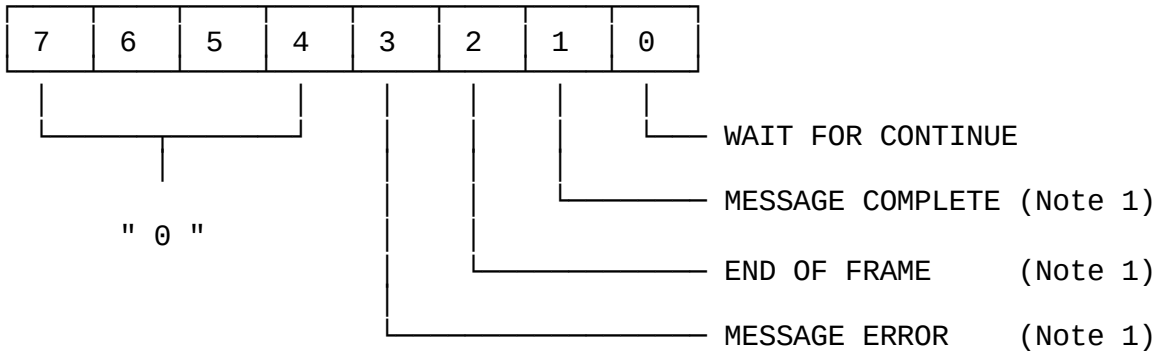
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message.

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MESSAGE STATUS REGISTER — 8-bit 6FFA (H)

This register indicates the status of the EXC-1553VME/E-V card. The figure below illustrates the definition of each Status bit. A logic "1" indicates active condition.



WAIT FOR CONTINUE - A message with the halt bit set has been encountered. The user must reset the halt bit in the Control word to continue.

MESSAGE COMPLETE - The last word of a message has been sent

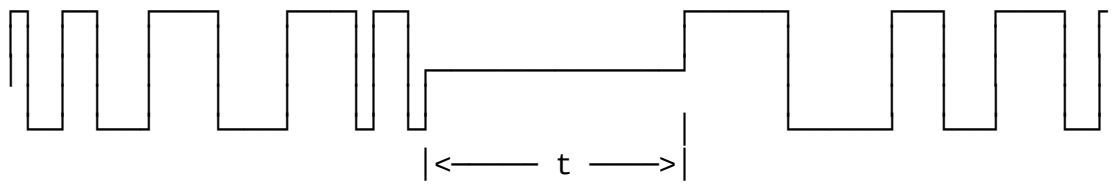
END OF FRAME - The last word of the last message in a frame has been sent

MESSAGE ERROR - A message has been sent resulting in the error bit being set in the Message Status Word

Note: 1) Status bits are NOT reset by the board and should be reset by the user after reading them.

RT RESPONSE TIME REGISTER — 8-bit 6FF8 (H)

This register sets the RESPONSE TIME of the Remote Terminal. The resolution of this register is 155 nsec. per bit. This time is measured as the "DEAD TIME" on the 1553 bus. The minimum time is equal to approximately 4usec. The value in the register is ADDED to the minimum time. The actual Response Time will be ± 1µsec tolerance. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).



Example: For a response time of 9 microseconds, write a 32 to this register.

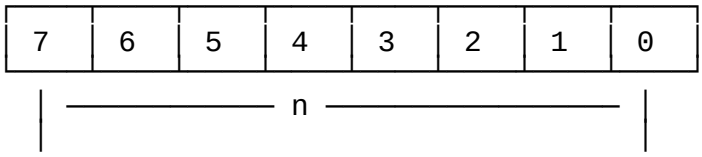
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32 * 0.155 = ~ 5 usec + 4 usec = 9usec

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LOOP COUNT REGISTER — 8-bit 6FF6 (H)

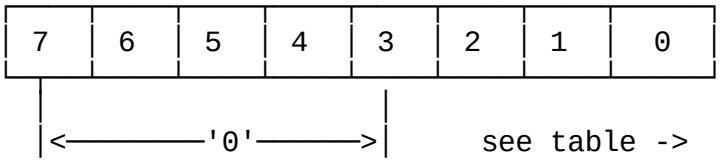
This register is used in conjunction with the Loop Bit in the Start Register. If that bit is set, the user sets this register to specify the number of times the Message Frame will be transmitted. A value of zero is interpreted as a request for continuous looping. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).



Value = 0 : Retransmits in continuous loop
Value = 1-255 : Sends message frame "n" times (1 to 255) as defined

BIT COUNT REGISTER — 8-bit 6FF5 (H)

Sets the number of total bit times within the 1553 word including Sync(3) and Parity(1). When NO error is selected (see: Control Word), this register is ignored (20-bit word is selected). This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).



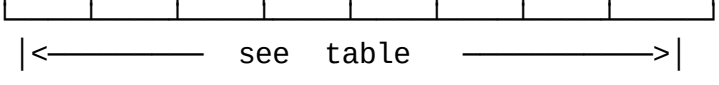
	2	1	0	# of bits
-3	0	0	0	17
-2	0	0	1	18
-1	0	1	0	19
0	0	1	1	20
+1	1	0	0	21
+2	1	0	1	22
+3	1	1	0	23

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WORD COUNT REGISTER	8-bit 6FF4 (H)

This register controls the number of 1553 words (+/- 3) within the message. The variation is relative to the 1553 Command Word's WORD COUNT FIELD. When NO error is selected (see: Control Word), this register is ignored. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

7	6	5	4	3	2	1	0



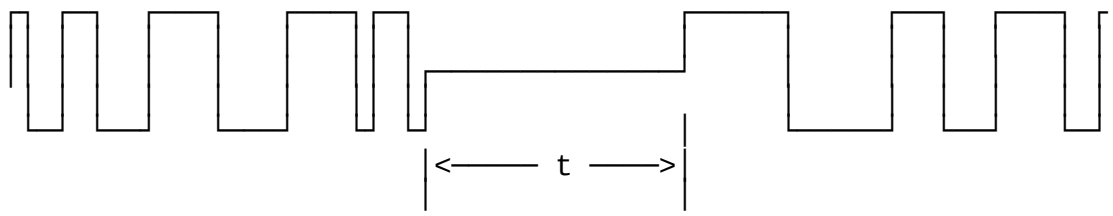
(No Word Count Error injected) -

-3	FD (H)
-2	FE (H)
-1	FF (H)
0	00 (H)
+1	01 (H)
+2	02 (H)
+3	03 (H)

BC RESPONSE TIME REGISTER	8-bit 6FF3 (H)

This register sets the Bus Controller's RESPONSE TIME WINDOW. This value determines the maximum [wait] time until an RT's Status Response is considered "INVALID" by the BC. The resolution of this register is
155nsec. per bit. This time is measured as the "DEAD TIME" on the 1553 bus. The minimum time is approx. 2 usec. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

Example: To set up a BC response time of 14 usec write a 90 to this register
90 * 0.155 = ~14µsec.



BC/RT Mode

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VARIABLE AMPLITUDE REGISTER	8-bit 6FF2 (H)

This register specifies the amplitude of the 1553 output signal. The signal can be programmed from 0 volts up to 7.5volts (p-p) - measured on the 1553 bus with specified 1553 coupling and 35ohm load (two 70 ohm termination resistors were used). A higher Transmit [output] amplitude will appear on the 1553 bus if 78 ohm termination resistors are used. The register has a resolution of 30mv/bit (p-p) on the bus. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register). This register defaults to FFH after Reset, providing maximum amplitude.

STACK POINTER	16-bit 6FF0 (H)

The Stack Pointer points to the Instruction Stack. The pointer value must be an EVEN value and equal to the ADDRESS of the [first] Instruction block. The Instruction Stack can reside anywhere within locations 0000 (H) and 63FF (H). This register must be set before issuing a START to the board. To modify this register: issue a STOP, modify and then re-issue a START.

FRAME TIME REGISTER	16-bit 6FEE (H)

This register contains the 16-bit Frame Time Value for Continuous and N-times Modes Operation. The value written to this register is multiplied by the value set within the Frame Time Resolution Register described below. The value set must equal the desired multiplication factor - 1. See ONE-SHOT / CONTINUOUS MODE OPERATION described above. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

FRAME TIME RESOLUTION REGISTER	16-bit 6FEC (H)

This 16-bit value represents the resolution of the Frame Time Counter in increments of 155 nsec. See ONE-SHOT/CONTINUOUS MODE OPERATION section described above. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

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INSTRUCTION COUNTER	16-bit 6FEA (H)

The Instruction Counter is loaded with the number of instructions (1553 Messages) in the current frame to execute. The value must be greater than "0" before beginning transmission (by writing to the "START REGISTER"). Load "1" for one message, "2" for two messages, etc. The EXC-1553VME/E-V updates this register by decrementing the value and writing it back to the memory. This register must be set before issuing a START to the board. This register is decremented and updated by the board at the end of each message transfer. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register). When in the "loop mode", this register cycles from the initial value to "1".

FIRMWARE REVISION REGISTER	8-bit 6FE7 (H)

This register indicates the revision level of the on-board firmware. The value 0001 0010 would be read as revision level: 1.2

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BUS MONITOR MODE OPERATION

The Bus Monitor can operate in two basic modes of operation. The first is the sequential mode - whereby 1553 Message Blocks are stored in sequential locations within memory. This mode includes two methods of operation. The first is called the FIXED BLOCK operation because the 1553 messages are stored at "fixed" sequential blocks within the memory. The second is called the LINK-LIST operation whereby the 1553 messages are "packed" one after another within the memory - separated by a header. Trigger capability is available within the Sequential Fixed Block Mode.

The second mode of operation utilizes a Look-Up table approach. In this mode, each unique 1553 message can be stored in a unique area of memory. The user-programmable Look-Up table is addressed by the EXC-1553VME/E-V upon receipt of a 1553 Command Word. The Command Word's RT Address, T/R bit, and Subaddress fields make up the 11-bit pointer to the Look-Up table. This equates to a table totalling 2048 locations (2Kx16). The contents of the table are in the form of 16-bit pointers (written by the user). The desired mode of operation is programmed via the Configuration Register.

NOTE:

The user should use the following sequence to determine whether the board is installed AND ready to operate:

* Check the Board ID register (test for value = 45 Hex)

* Check Board Status Register (test for Board Ready bit = "1")

The board is installed and ready when BOTH of these registers contain the correct values (as written above). This sequence should be used after power-on and Software Reset operations. For Software Reset operations, these values should be set to ZERO by the user immediately prior to writing to the Initialization Register.

Time Tag Value

In all monitor modes a Time Tag value is associated with each incoming message. The Time Tag Value is a 32 bit word which may be used to determine the time between the 1553 messages. The Time Tag implementation utilizes a 32-bit, free running counter whose resolution is FIXED at 4µsec. per bit. The Time Tag counter can be reset (to '0') by writing to the "Time Tag Reset Register" (see the section: Control Register Definitions).

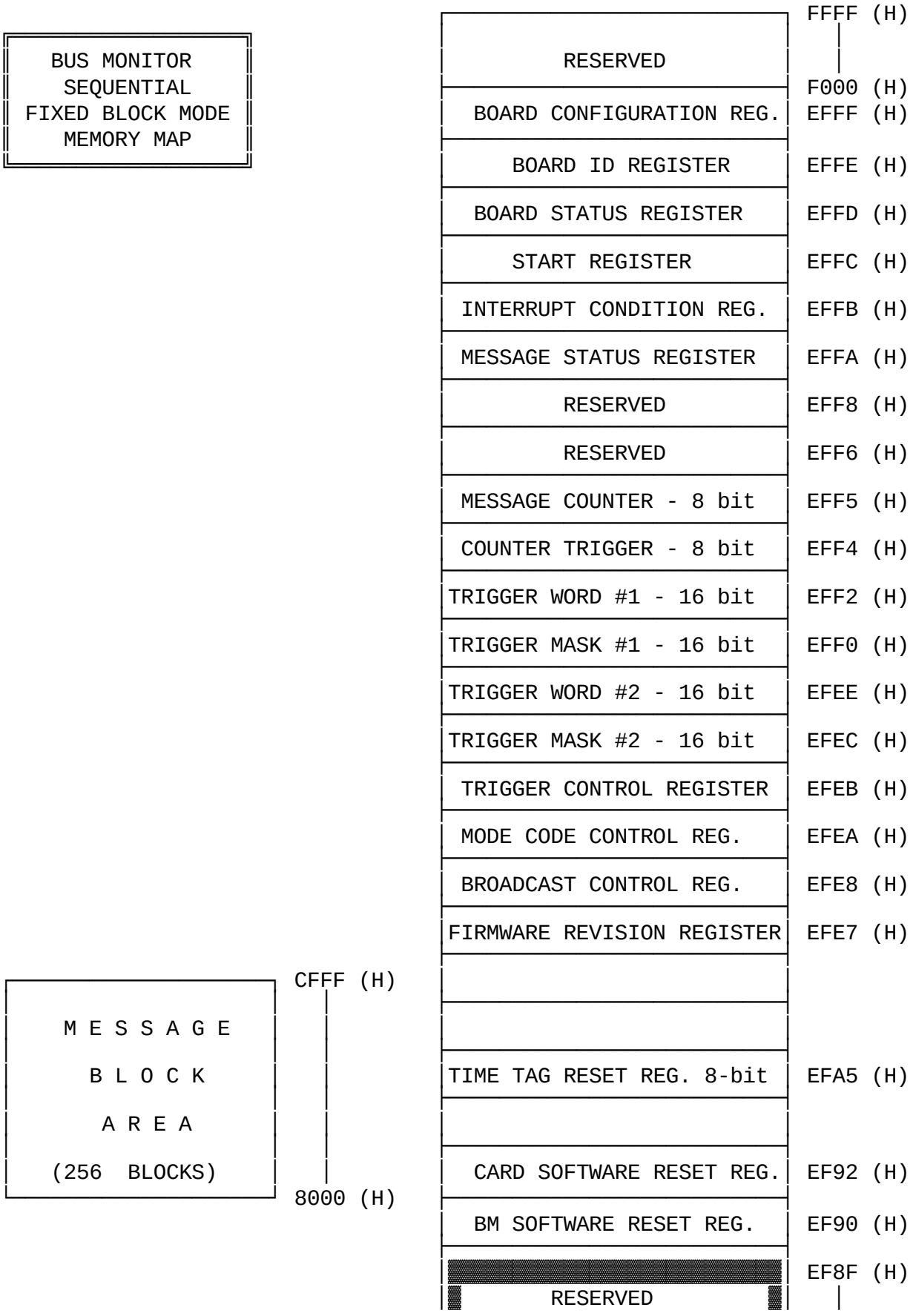
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The timer's value is written to the dual port RAM during the reception of the [first] command of each message.

BM Mode

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The following figure shows the memory map of the EXC-1553VME/E-V in the Bus Monitor Sequential Fixed Block Mode of operation.

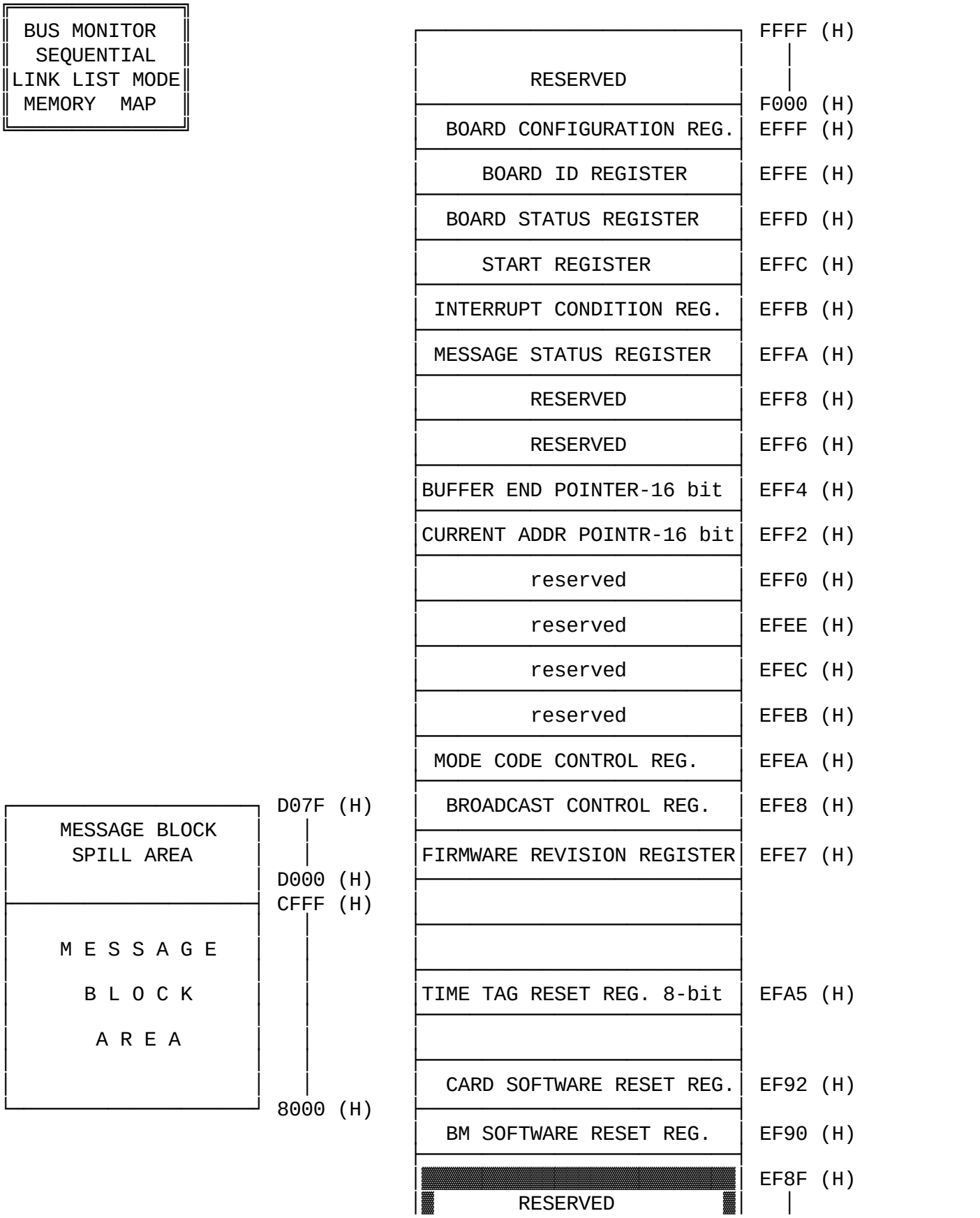


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The following figure shows the memory map of the EXC-1553VME/E-V in the Bus Monitor Sequential Linked List mode of operation.



BM Mode

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BM Mode

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SEQUENTIAL MODES

SEQUENTIAL MODES: MESSAGE BLOCK AREA

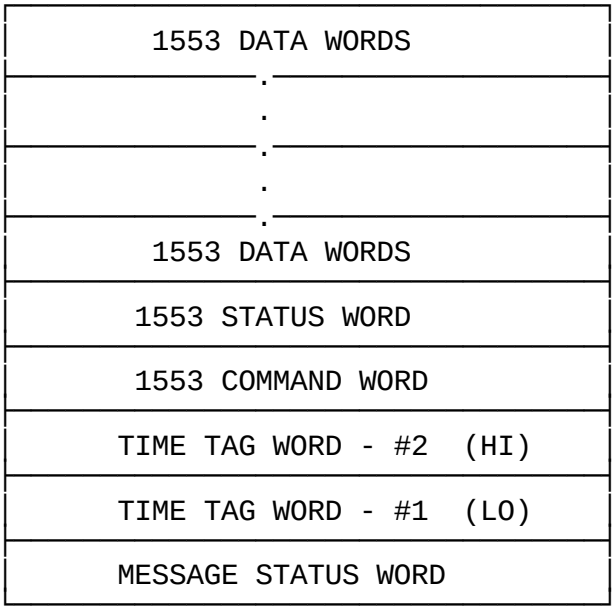
The Message Block Area is partitioned into either blocks of fixed length or into a "LINK LIST" organized memory. The partitioning is determined by the Configuration Register.

FIXED BLOCK OPERATION

In this mode, the Message Block Area is divided into 256 blocks - each consisting of 40 words. The first block starts at address 0000(H), the second at 0050(H),the third at 00A0(H), etc. The trigger option can be used in this mode only (see Trigger Operation)

BUS MONITOR MESSAGE BLOCK

FIXED BLOCK MODE



NOTE: Example of a 1553 Transmit Command

1st location of block

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LINK - LIST OPERATION

In this mode, the Message Block Area appears to be one continuous block of data. The first word location within the Message Block Area form the Message HEADER. This header points to the offset address of NEXT Message Block [Header].

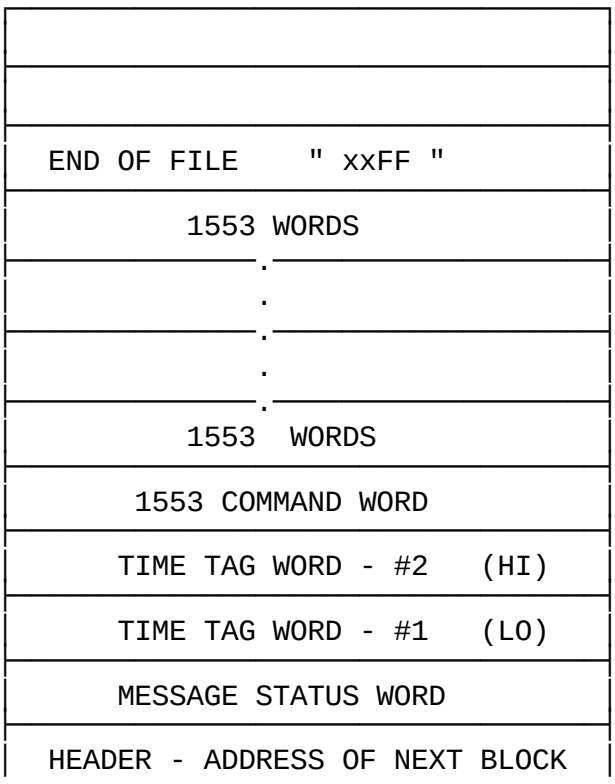
Example:

Header = 0008 (H) (value read from memory)
Thus the next message is located at 8008 (H)

The Header of the LAST 1553 block received will contain "xxFF"("End of File")- indicating that no more messages have been stored. After each message has been processed and stored in memory, the HEADER of the preceding message block will be updated from "xxFF" to the offset address of the newly stored message (points to the Header within the block). This method allows for the storage of more data than can be realized using the fixed-block mode of operation.

Special care is to be taken with the message appearing at the end of the Messsage Block Area. Since the buffer never wraps around in mid message and a message may start at any address upto CFFEH, the Final message in the buffer may extend passed the end of the standard Message Block Area into the Message Block Spill Area. For this case a special register exists (Buffer End Pointer), which points to the last location of the message in order to be able to recognize the message lenght. The next message will start at the first location of the Message Block Area (8000H).

BUS MONITOR MESSAGE BLOCK LINK-LIST MODE



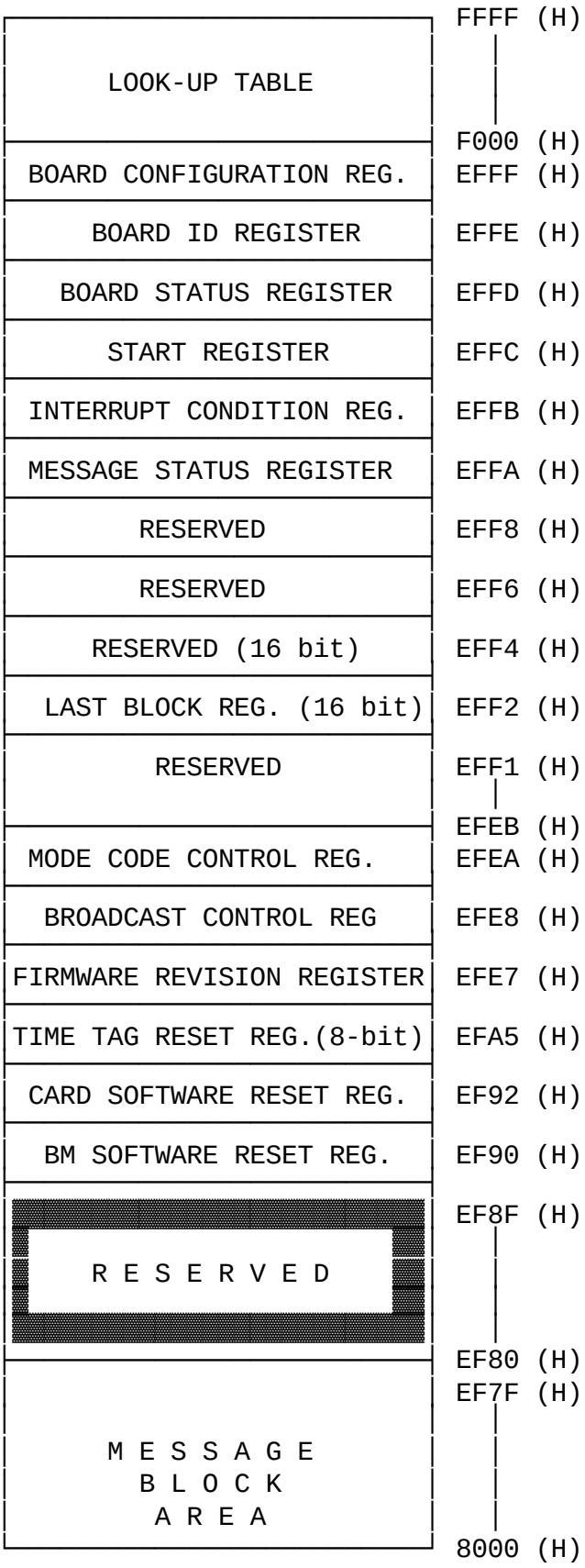
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BM Mode

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BUS MONITOR

LOOK-UP TABLE
MEMORY MAP

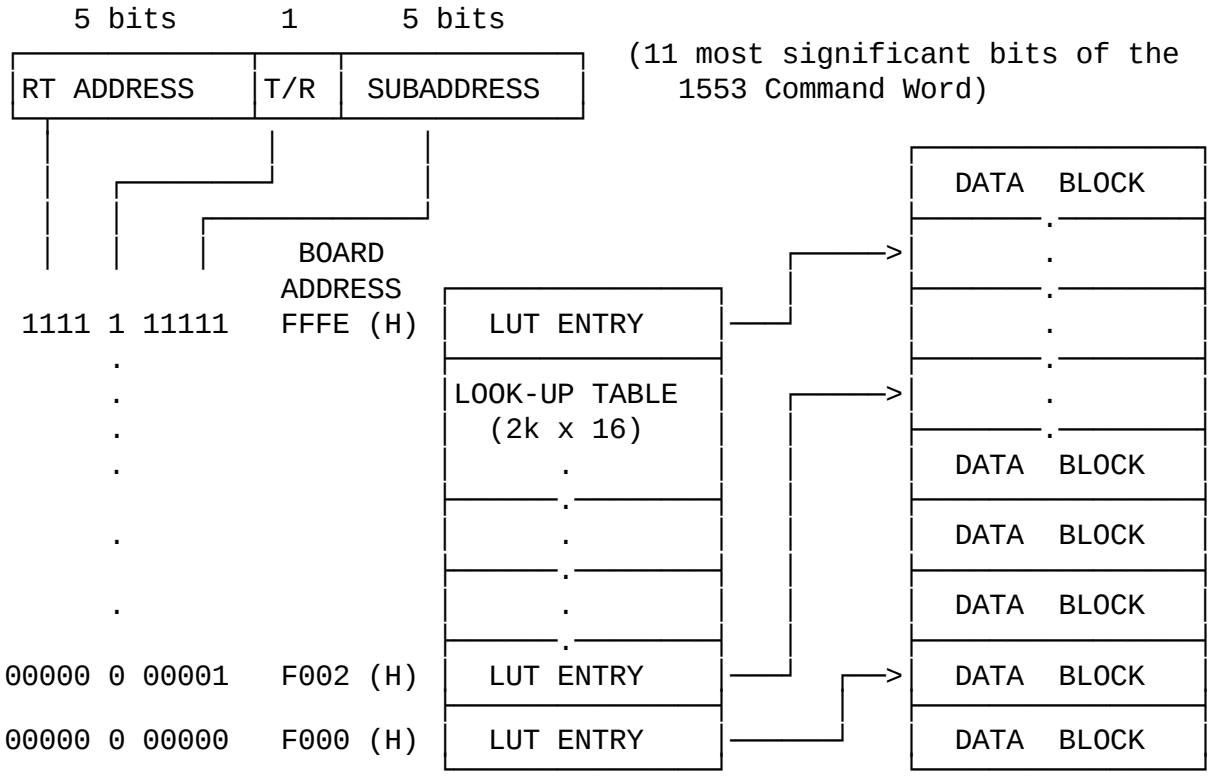


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LOOK-UP TABLE OPERATION

In this mode of operation, the EXC-1553VME/E-V stores 1553 messages into a minimum of 356 unique Message Blocks. The user may assign a Message Block to each RT#, SA#, T/R combination. This is accomplished via a 2k x 16 Look-Up Table within the on-board memory. Each [table] entry is divided into a 15-bit Block Address and an Interrupt Select bit as described below. The user can select which messages will generate an interrupt via the Interrupt Select bit. The Interrupt Condition register must also be programmed.

The received Command word's RT Address, T/R bit, and Subaddress Fields are used as an index into the user-programmed, look-up table (see figure below).



Note: The user defines only the start of the Data Block Area, not its length. The board will use only the amount of memory necessary for the message thus allowing the user to assign blocks in a space efficient manner.

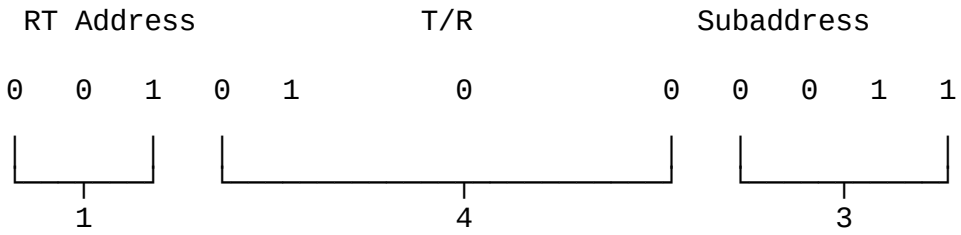
BM Mode

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HOW TO CREATE THE ADDRESS TO THE TABLE

(1) Isolate the ELEVEN (most significant) bits of the 1553 Command Word (RT Address, T/R, and Subaddress Field).

Example : RT Address =5
T/R bit = 0 (receive)
Subaddress = 3



The HEX representation = 143 (H)

(2) Multiply the value by 2.(since it is a word index)

143 (H) * 2 = 286 (H)

(3) Add this value to the base address of the Look-Up table (F000).

```
  F000 (H)
+  286 (H)
----------
  F286 (H)
```

(4) Write Data Block Pointer to this location.

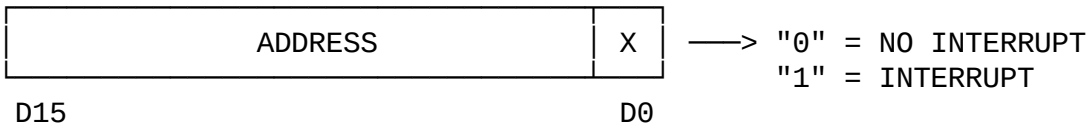
Example:

```
POKEW &HF286, &H8752        "writes 16-bit value to table
```


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HOW TO CREATE THE DATA BLOCK POINTER

1. Select start address of data block (from 8000 to EF7E [Hex]). This address must be even.
2. Write 16-bit Value into Look-Up Table with the LSB of the address corresponding to D0.
3. "D0" bit is used to select an interrupt per message (you must also set the Interrupt Condition Register).



EXAMPLE:

User wants 1553 message to be stored [starting] at address : D002 (H)

Write value into Look-Up Table

COMBINING THE TWO EXAMPLES ABOVE:

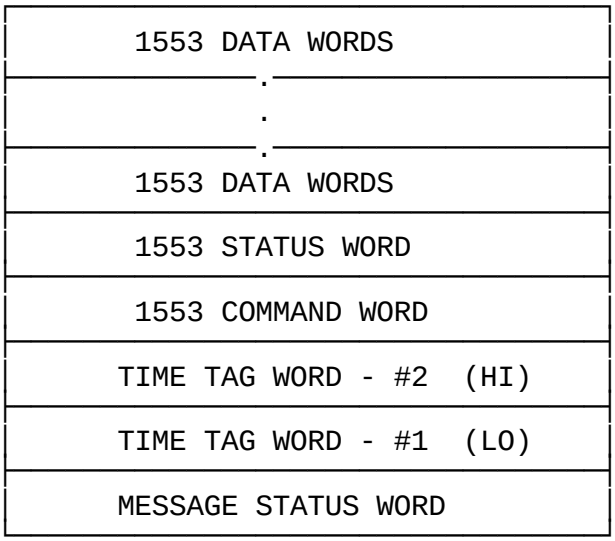
```
POKEW &HF286, &HD002
```

This writes the [pointer] Block Address :D002(H) into the Look-Up table Address : F286(H).

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BUS MONITOR MESSAGE BLOCK — LOOK-UP TABLE MODE

Each 1553 message is "tagged" with a Message Status Word and a 32-bit Time Tag Word. The figure below illustrates the contents of one Message Block and the sequence in which the words are stored in memory.



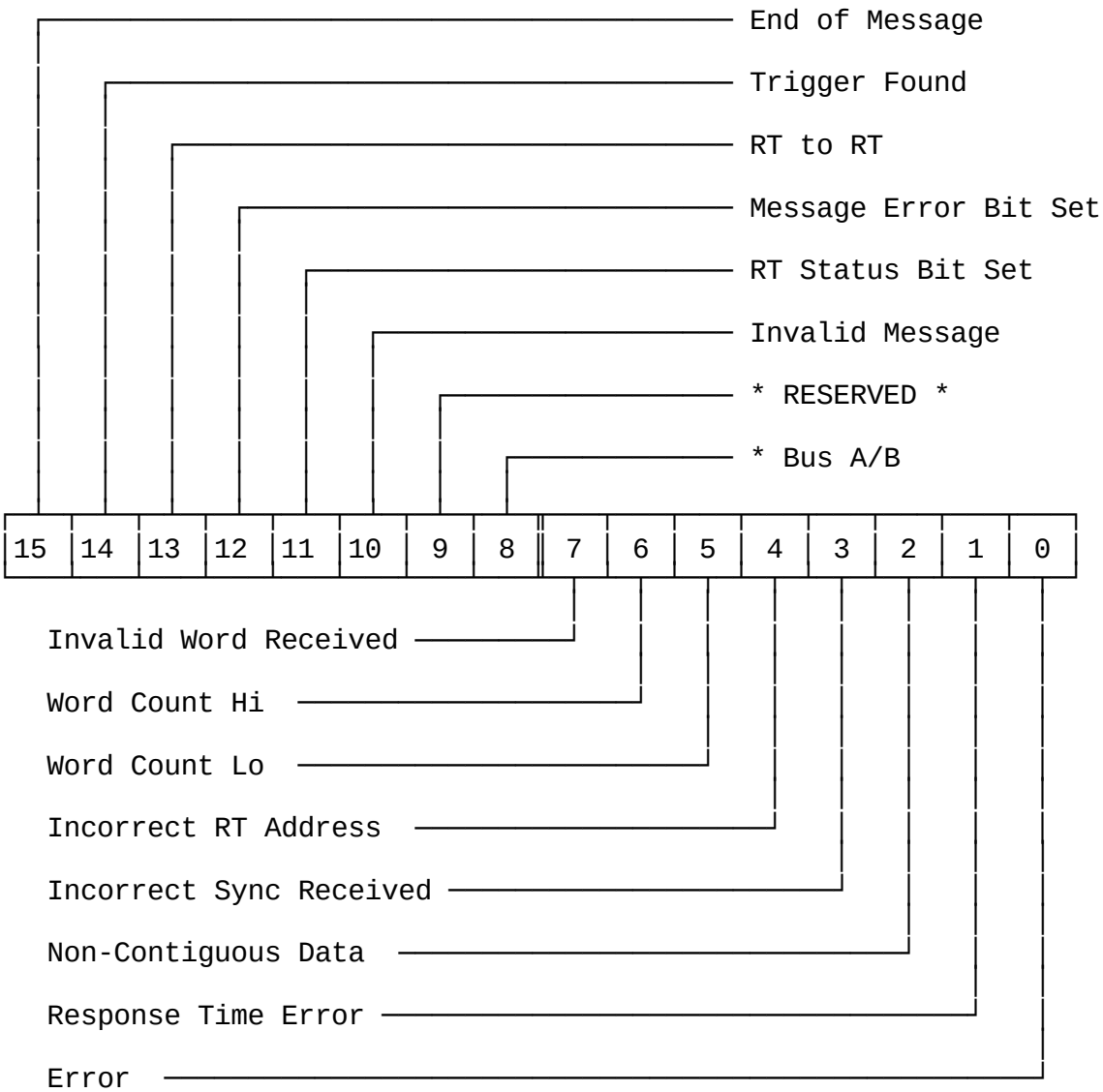
NOTE: Example of a 1553 Transmit Command

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MESSAGE STATUS WORD

Note: For ALL Modes

The Message Status Word indicates the status of the message transfer. This word is created by the Board and is NOT the 1553 "STATUS WORD".
The contents of the Message Status word is shown below:



NOTE: A LOGIC "1" INDICATES OCCURRENCE OF STATUS FLAG

BM Mode

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Message Status Word Definitions:

15	End of Message	Indicates that the message transfer has been completed
14	Trigger Found *	Indicates reception and storage of trigger message. valid for sequential fixed block mode with 'store after' and 'store only' operations (see note below)
13	RT to RT	Indicates reception of a rt to rt message
12	Message Err. Bit Set	Indicates the Message Error Bit (bit #10) within the RT Status Word was set.
11	RT Status Bit Set	Indecates that a bit was set within the RT Status Word (other than the Message Error Bit). The ERROR Bit is NOT set in conjunction with this bit.
10	Invalid Message	Indicates that a 1553 'message level' error occurred (i.e. Word Count, Incorrect Sync) - detailed below
09	Reserved	Set to logic '0'
08	Bus A/B	Indicates on which bus the message was transferred. '0' = Bus B; '1' = Bus A
07	Invalid Word	Indicates the reception of at least one invalid 1553 Word (i.e. Bit Count, Manchester code, Parity)
06	Word Ct Hi	Indicates that the RT transmitted too many words
05	Word Ct Lo	Indicates that the RT transmitted too few words
04	Incorrect RT Addr.	Indicates that the received 1553 status word did not contain the correct 'RT ADDRESS'
03	Incorrect Sync	Indicates that the sync of either the status or data word(s) was incorrect
02	Non-Contiguous	Indicates occurrence of an invalid gap between received 1553 words
01	Response Time Err	Indicates a response time error has occurred within the message
00	ERROR	Indicates the occurrence of an error (defined within one of the other message status bit locations)

* Note: Trigger Found (Bit 14)
STORE ONLY MODE - Each Trigger message will have this bit set.

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STORE AFTER MODE - ONLY FIRST Trigger Message will have this bit set.

BM Mode

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TRIGGER OPERATION

SEQUENTIAL FIXED BLOCK MODE ONLY

The EXC-1553VME/E-V can be programmed to store messages in the following manner:

1. STORE ALL (STORES ALL 1553 MESSAGES-NO TRIGGERS ACTIVE)
2. STORE ONLY (ONLY MESSAGES WHICH MEET THE TRIGGER CONDITION)
3. STORE AFTER (AFTER RECEIPT OF A TRIGGER MESSAGE - STORES TRIGGER MESSAGE, too)

The user can define up to 2 triggers. Each trigger is defined using two registers: the TRIGGER WORD and TRIGGER MASK registers. The TRIGGER WORD register defines a 1553 Command Word value or a Message Status Word value which triggers storage as defined above, while the TRIGGER MASK register allows the user to define which bit(s) of the TRIGGER WORD are relevant or are to be ignored ("Don't Care"). See detailed description within the Control Register section below).

In this way, the user can define a trigger as being a unique 1553 message (by using the 1553 Command Word as the trigger) or via the status of the message (by using the Message Status word). Using the Message Status Word as the trigger source allows for storage of, for example, all messages on Bus A, or only messages with errors, or messages with errors received over Bus B, etc.

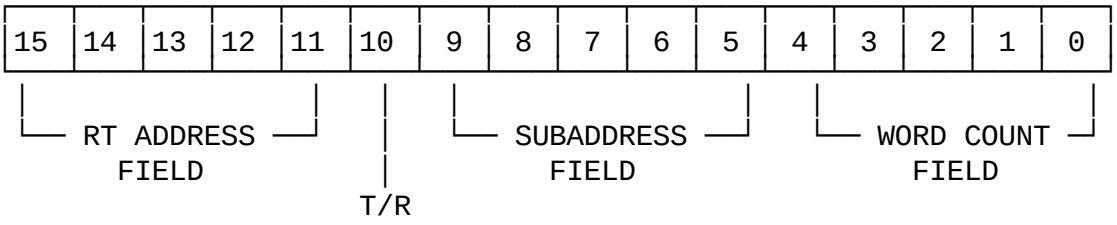
The trigger source, mode and conditions are set via the TRIGGER CONTROL REGISTER (see Control Register Definitions). The Trigger Word and Mask Registers must be written before issuing a START to the board. To modify these registers, the user must first set the "Initialize" bit within the START Register (10H), modify the registers and then issue a "START" (81H).

The user can define which trigger is active (Trigger #1, Trigger #2, or BOTH) via the Trigger Control Register. The Trigger Mask Registers (see below) MUST be defined when using the trigger function.

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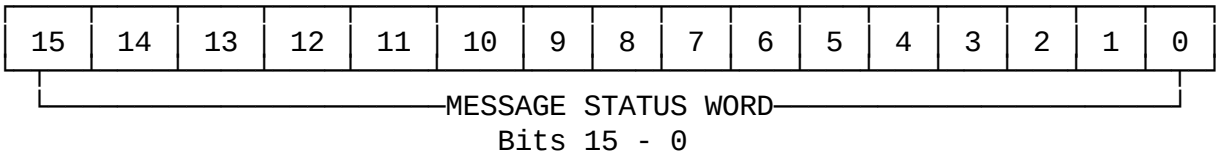
TRIGGER WORD REGISTERS (1 and 2) EFF2, EFEE (H)

USING THE 1553 COMMAND WORD



The user loads these locations with the desired 1553 Command Words which are be used as the trigger source. The user can define which trigger is active (Trigger #1, Trigger #2, or BOTH) via the Trigger Control Register. The Trigger Mask Registers (see below) MUST be defined when using the trigger function.

USING THE MESSAGE STATUS WORD

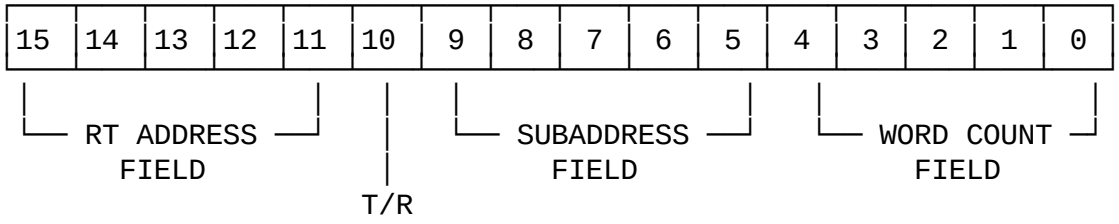


The user loads these locations with the desired Message Status Word (as described above).

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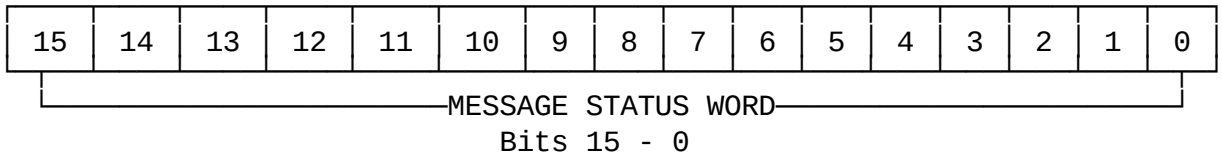
TRIGGER MASK REGISTERS (1 and 2) EFF0, EFEC (H)

USING THE 1553 COMMAND WORD



1 = Use Value From Trigger Word Register
0 = Don't Care

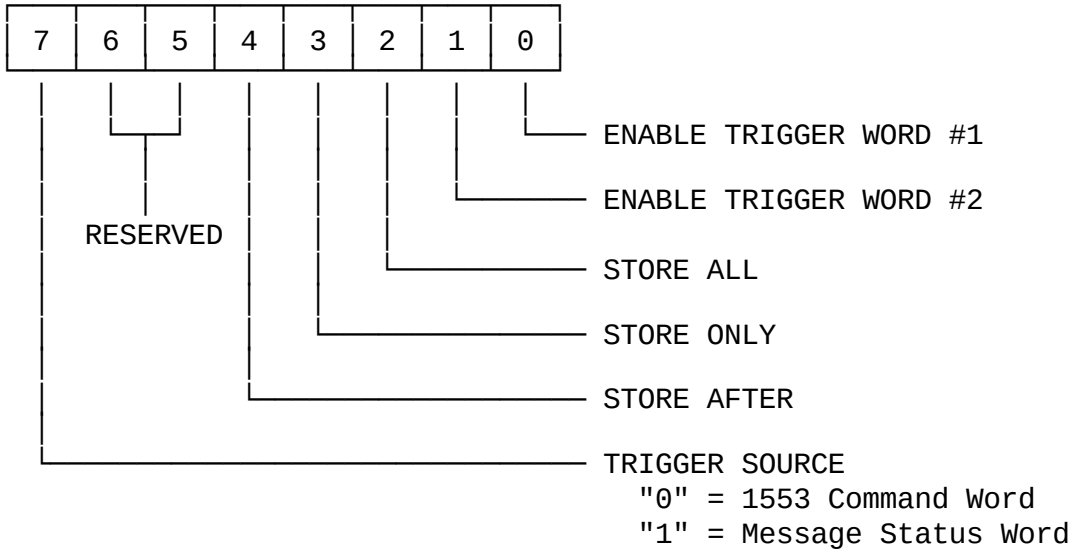
USING THE MESSAGE STATUS WORD



1 = Use Value From Trigger Word Register
0 = Don't Care

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TRIGGER CONTROL REGISTER | 8-bit | EFEB (H) | SEQUENTIAL BLOCK MODE ONLY



NOTE: A logic "1"
selects function

EXAMPLE

User defines the Command Word "0825"(H) as Trigger Word #1 (Receive Command for RT#1 , Subaddress #1 and 5 words) but selects to ignore the Word Count Field and disables Trigger Word #2. In addition, the user wants to store only message type(s) defined by Trigger Word #1.

Load Trigger Word #1 Register with the Value : 0825 (Hex)
Load Trigger Mask #1 Register with the Value : FFE0 (Hex)
Load Trigger Control Register with the Value : 09 (Hex)

Note: ONE of the bits; Store All, Store Only, Store After MUST be set if Trigger(s) are utilized.

BM Mode

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PROGRAM EXAMPLE — BUS MONITOR SEQUENTIAL FIXED BLOCK MODE

```
10 POKE &HEFFF,08      ' LOAD CONFIGURATION REG; BM SEQ BLOCK MODE
```

(See example above regarding the use of Trigger words)

```
60 POKEW &HEFF0,xxxx   ' LOAD TRIGGER MASK #1: xxxx
80 POKEW &HEFF2,xxxx   ' LOAD TRIGGER WORD #1: xxxx
100 POKE &HEFEB,xx     ' LOAD TRIGGER CONTROL REGISTER

110 POKE &HEFEA,00     ' LOAD MODE CODE CONTROL REG; 1's AND 0's
120 POKE &HEFE8,00     ' LOAD BROADCAST CONTROL REG: RT31 = REGULAR

130 POKE &HEFFC,&H81   ' START
```

Note: Messages are read from memory starting from address `0000'.

PROGRAM EXAMPLE — BUS MONITOR SEQUENTIAL LINK LIST MODE

```
10 POKE &HEFFF,&H10    ' LOAD CONFIGURATION REG; BM LINK-LIST MODE

110 POKE &HEFEA,00     ' LOAD MODE CODE CONTROL REG; 1's  AND  0's
120 POKE &HEFE8,01     ' LOAD BROADCAST CONTROL REG: RT31 = BROADCAST

130 POKE &HEFFC,&H81   ' START
```

Note: Messages are read from memory starting from address `0000´.

PROGRAM EXAMPLE — BUS MONITOR LOOK-UP TABLE MODE

```
10 POKE &HEFFF,&H20    ' LOAD CONFIGURATION REG; BM LOOK-UP TABLE
20 POKEW &HFxxx,&Hpppp ' SET UP THE LOOK-UP TABLE WITH REQUIRED
                         POINTER: pppp

60 POKE &HEFEA,00      ' LOAD MODE CODE CONTROL REG; 1's  AND  0's
70 POKE &HEFE8,00      ' LOAD BROADCAST CONTROL REG: RT31 = REGULAR

80 POKE &HEFFC,&H81    ' START
```

Note: Messages are read from memory according to address pointer derived from Command Word - see example above

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CONTROL REGISTER DEFINITIONS

TIME TAG RESET REGISTER — 8-bit EFA5 (H)

Writing to this register (data field = don't care) will reset the hardware Bus Monitor Time Tag counter. The counter will start to count from 0 immediately after the reset.

CARD SOFTWARE RESET REGISTER — 8/16-bit EF92 (H)

Writing to this location (data field = don't care) will RESET the EXC-1553VME/E-V card. All card functions will be reset upon writing to this register. In addition, all Dual Port Ram will be cleared to "0". The Board Status, Board ID, Firmware Revision and Variable Amplitude registers are written by the board after reset operation has been completed.

BM SOFTWARE RESET REGISTER — 8/16-bit EF90 (H)

Writing to this location (data field = don't care) will RESET only the BM section of the EXC-1553VME/E-V card. In addition, the Dual Port Ram used in the BM mode of operation will be cleared to "0". The Board Status, Board ID and Firmware Revision registers are written by the board after the reset operation has been completed.

BOARD CONFIGURATION REGISTER — 8-bit EFFF (H)

* set the desired bit to a logic "1"

The operating mode of the board is set via this register. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register for START and INITIALIZE bits).

HEX VAL	7	6	5	4	3	2	1	0	
01	0	0	0	0	0	0	0	1	reserved
02	0	0	0	0	0	0	1	0	reserved
04	0	0	0	0	0	1	0	0	reserved
08	0	0	0	0	1	0	0	0	BM - SEQUENTIAL BLOCK MODE
10	0	0	0	1	0	0	0	0	BM - SEQUENTIAL LINK LIST
20	0	0	1	0	0	0	0	0	BM - LOOK-UP TABLE MODE
40	0	1	0	0	0	0	0	0	reserved
80	1	0	0	0	0	0	0	0	reserved

BM Mode

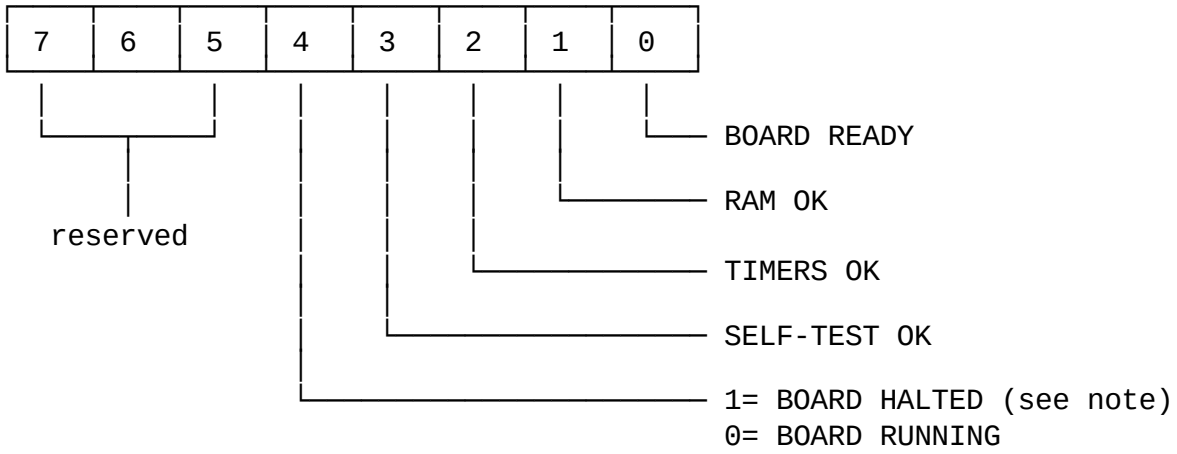
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BOARD ID REGISTER 8-bit EFFE (H)

This register contains a fixed value which can be read by a user's initialization routine to detect the presence of the EXC-1553VME/E-V card. The one-byte value of this register is: 45 (Hex) ; ASCII "E".

BOARD STATUS REGISTER 8-bit EFFD (H)

This register indicates the status of the EXC-1553VME/E-V card. In addition, this register indicates option selection as defined below.

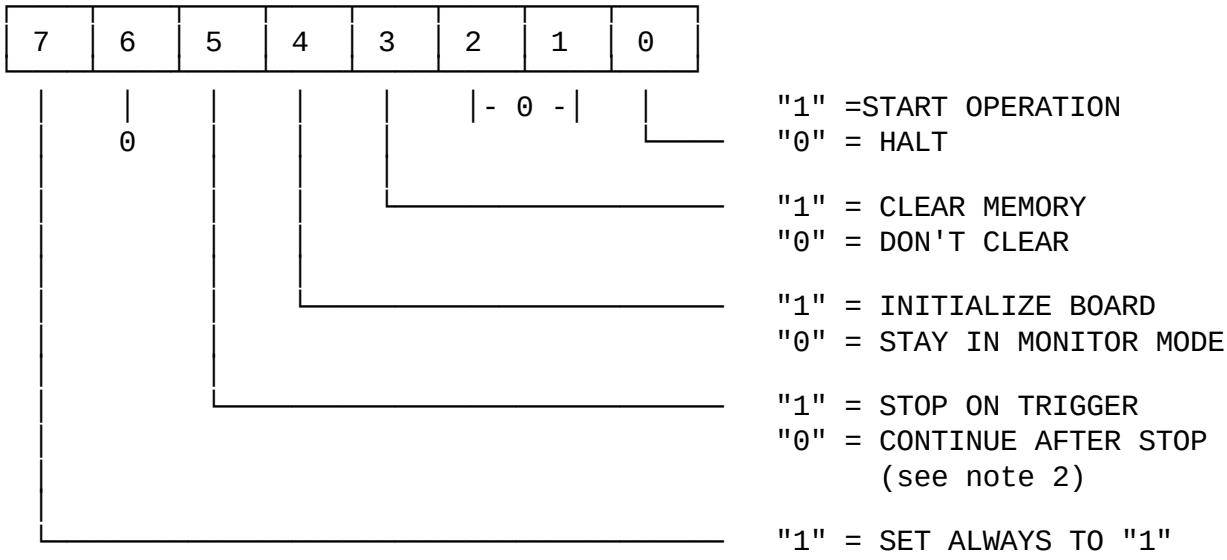


NOTE: Bit "04" (Board Halted) is set by the board after the user "stops" the current operation (by resetting the START bit within the Start Register). The user must check this bit first before modifying registers which first require a "STOP" operation. The board resets this bit after receiving a subsequent START command (by writing to the Start Register). The condition of this bit after power-on or software reset is a logic '1'.

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START REGISTER	8-bit EFFC (H)

This register controls the "START / HALT" operation of the board. Writing to this register with the appropriate bit set executes one of the functions as listed below:



NOTES:

1. The "Clear Memory" and "Initialize Board" bits are tested by the EXC-1553VME/E-V board only when the "Start/Halt" bit is '0'. The "Clear Memory" function clears the 1553 message Blocks and all "readable" control registers. The "Initialize Board" function enables the user to re-initialize the board, change the board's mode of operation (modify the Configuration Register) and start [again]. You cannot change Monitor modes of operation by [just] "stopping" and "starting" the board (START/HALT bit). These bits are cleared by the board after the specific function is completed.

2. The STOP ON TRIGGER/CONTINUE bit is used in the Sequential Fixed Block Mode ONLY. This bit is tested when the Message Counter equals the Message Counter Trigger. The board will stop storage of 1553 messages if this bit is then a '1'. Setting this bit to a '0' will then allow the board to continue monitoring operations. You must first "continue" before "HALTING" the board (setting START/HALT bit to a '0')

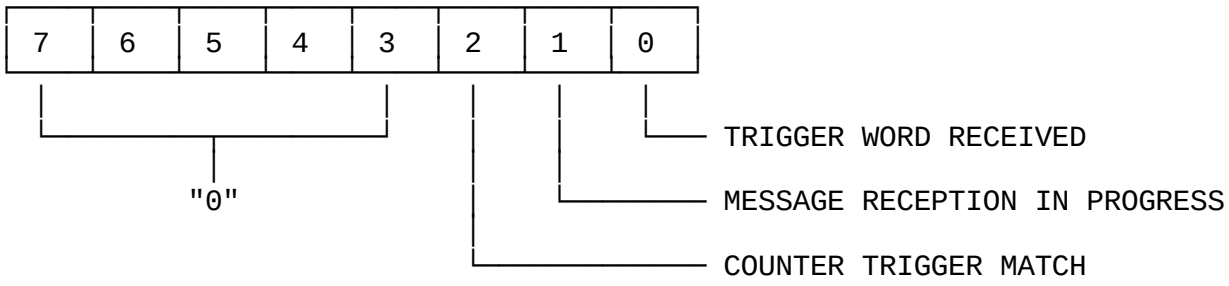
3. Bit "04" of the Board Status Register is set on two conditions:

   a) When a HALT is issued (set bit "00" of this register to a logic '0').
   b) When an INITIALIZE BOARD is issued.

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INTERRUPT CONDITION REGISTER 8-bit EFFB (H)

This register allows the user to set different interrupt triggers. When an interrupt occurs, the interrupt flag will be set and the condition(s) that triggered the interrupt are accessible via the Message Status Register. A logic '1' enables the interrupt condition. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).

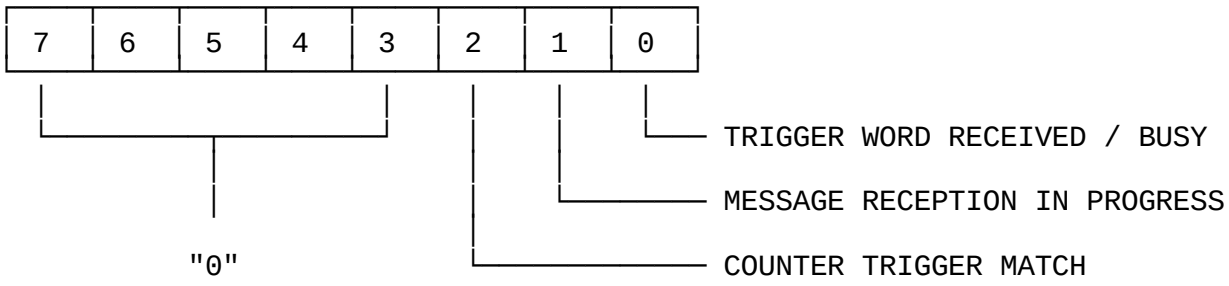


Notes:

1. Trigger Word Received and Counter Trigger Match are valid for Sequential Fixed Block Mode only.
2. Message Reception in Progress is valid for all modes.
3. For all Interrupt Conditions the Interrupt will be sent at the end of the message.

MESSAGE STATUS REGISTER 8-bit EFFA (H)

This register indicates the status of the EXC-1553VME/E-V card. The figure below illustrates the definition of each Status bit. A logic "1" indicates active condition.



Notes:

1) Status bits are NOT reset by the board! (except for BUSY bit - see note 2) The User is advised to reset these bits after reading them.
2) TRIGGER WORD RECEIVED is valid for Sequential Block mode only. In Linked List and Look-Up Table modes this bit represents BUSY and is set while the board is processing a message. It is set together with MESSAGE RECEPTION IN PROGRESS but it is reset approximately 5 usec after the end of each message. For consecutive messages with short

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intermessage gap times it may not be reset between messages.

BM Mode

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MESSAGE COUNTER REGISTER	8-bit	EFF5 (H)	SEQUENTIAL BLOCK MODE ONLY

This register indicates the current Message Block number (0-255). The value is incremented by the board upon reception of each message. The counter increments to "1" (indicates first message received) upon receipt of the second 1553 message. Check the Message Status Word of the FIRST Message Block in order to determine the arrival of the first 1553 message (the End of Message bit within the Message Status Word will be set).

COUNTER TRIGGER REGISTER	8-bit	EFF4 (H)	SEQUENTIAL BLOCK MODE ONLY

This register allows the user to know when a specific message block number has been updated by the EXC-1553VME/E-V. This register is loaded by the user with a value that when equal to the Message Counter, will set a bit within the Message Status Register and, if programmed within the Interrupt Condition Register, cause an interrupt. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register). In addition, the board can be programmed to STOP monitoring when the Counter Trigger is equal to the Message Counter (see STOP/CONTINUE bit within the Start Register)

CURRENT ADDRESS POINTER	16-bit	EFF2 (H)	LINK-LIST MODE ONLY

This pointer indicates the offset address location of the 1553 message, which is about to be written. This register is updated at the end of each message storage operation. It cycles from 0H to 4FFEH.

BUFFER END POINTER	16-bit	EFF4 (H)	LINK-LIST MODE ONLY

This register contains the offset (from 8000H) of the last word in the final message in the Message Block Area, and is updated each time the final message is written into the buffer. Note that `final messages', which are longer than the remaining available space in the Message Block Area, do not wrap around to the start of the buffer, but rather, are `spilled' into the Message Block Spill Area, which is contiguous with the Message Block Area. The offset value in this register varies from 4FFEH (end of Message Block Area) to 507EH (end of Message Block Spill Area). Until the first buffer wrap around occurs, this register contains 0000H.

LAST BLOCK REGISTER	16-bit	EFF2 (H)	LOOK-UP TABLE MODE ONLY

This register indicates the [LOOK-UP TABLE] block offset (from 8000H) of the current 1553 message. This register can be utilized to identify the location of

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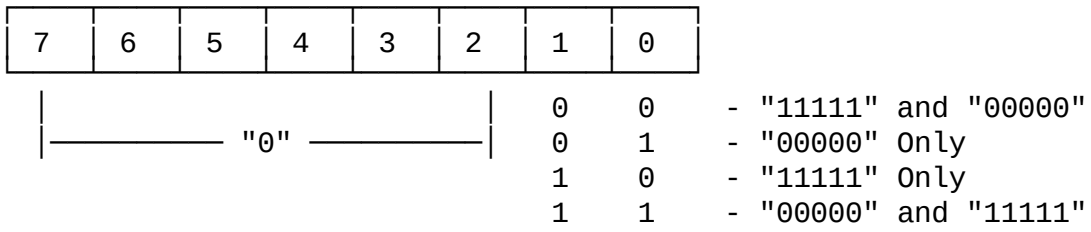
that message. This register is updated at the end of each message reception.

BM Mode

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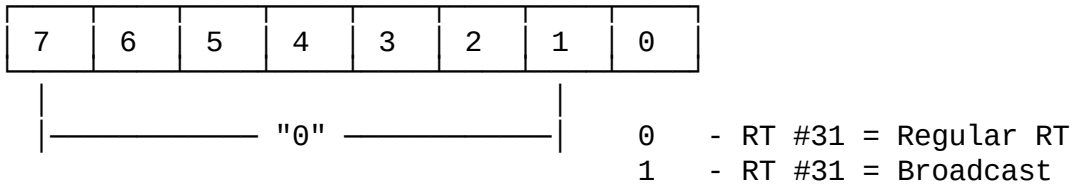
MODE CODE CONTROL REGISTER — 8-bit EFEA (H)

This register allows the user to determine which 1553 Subaddress value indicates the reception of a 1553 Mode command. This register must be set before issuing a START to the board. To modify this register: issue a "STOP", modify and then re-issue a START (see START Register).



BROADCAST CONTROL REGISTER — 8-bit EFE8 (H)

This register allows the user to select whether RT Address "11111" should be regarded as a valid RT number or as the Broadcast address.



FIRMWARE REVISION REGISTER — 8-bit EFE7 (H)

This register indicates the revision level of the on-board firmware. The value 0001 0010 would be read as revision level: 1.2

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SWITCHING BETWEEN MODES OF OPERATION

The user can switch between modes of operation (ex. between Bus Controller and Remote Terminal) by "HALTING" the operation of the board (VIA THE START REGISTER), modify the Configuration Register ,setup the memory as required, and then set the START bit within the Start Register.

1553 A /B / MULTI-PROTOCOL CONSIDERATIONS

The EXC-1553VME/E-V offers the user a wide range of options that can be utilized for various 1553 applications. The EXC-1553VME/E-V's flexibility does not come at the expense of complicated software or development time for the user -as the board is memory mapped and easy to use. The various options are controlled via control registers which are described within this document.

Examples of options:

1. RT can return Status Word [even] if the received 1553 Data Words were not valid (note: the word count was correct).

2. Selectable Broadcast mode

3. Variable Response Time

4. Select Mode Code Subaddress ("00000", "11111", or both)

5. 1553A RT Timing

6. User can define all bits within the 1553 Status Word

OPTIONAL 1553WPG-V PIGGYBACK

The 1553WPG-V is a an optional adapter card which plugs onto the EXC-1553VME/E-V. It is designed to enhance the error injection capability of the EXC-1553VME/E-V. Its primary use is for implementing the Manchester type errors within the RT Validation Test Plan.

The 1553WPG-V permits the user control over the 1553 buses to a resolution of 50 nsec. For each 50 nsec the user may select a Manchester bi-level coded Hi pulse, a Lo pulse or a Null level. Proper Manchester encoded transmissions are composed of combinations of Hi and Lo pulses while a Null level represents no transmission over the bus. See the 1553WPG-V User's Manual for more information regarding the WPG.

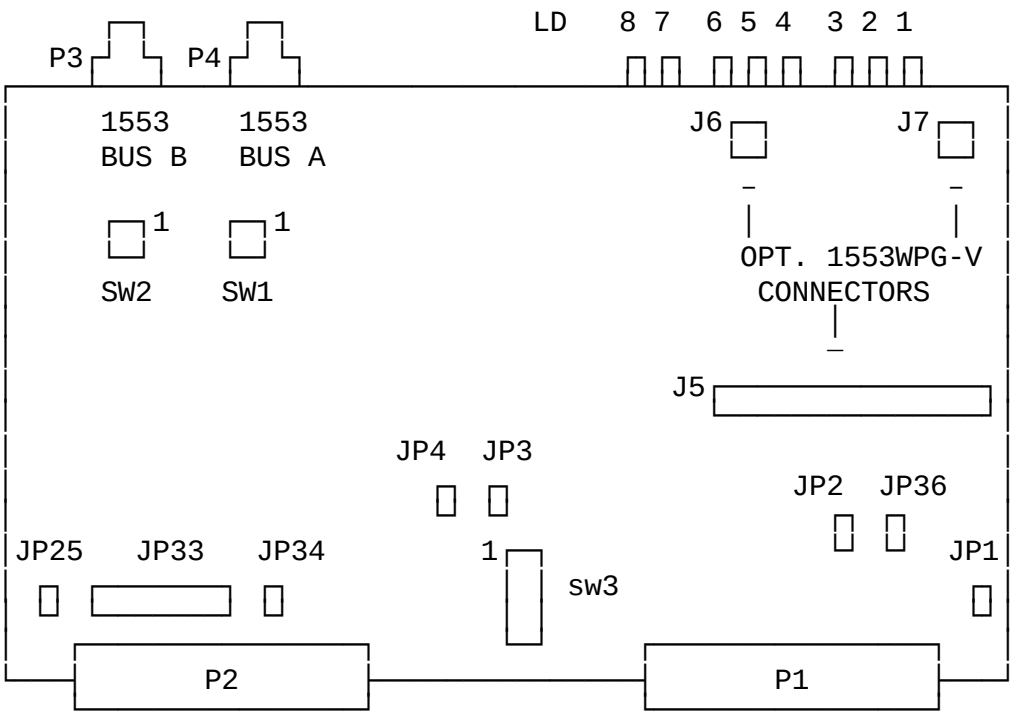
Writing a '1' to the WPGSEL bit within the Zero Crossing Register maps the

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1553WPG-V to addresses 0000H to 8FFFH within memory map. Setting WPGSEL to '0' disables the WPG accesses, enabling the standard operational modes of the EXC-1553VME/E-V.

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BOARD LAYOUT



Note: B size card shown.

LEDS

The individual functions of the front panel leds are listed below.

MODID (LD1) Reflects the state of the MODID pin on the VXI bus (JP25 must be installed). This LED has no function in a VME system.

PASSED (LD2) Indicates that the card passed the power-on self test routine. Reflects the state of the bit of the same name in the Configuration Status Register.

READY (LD3) Indicates that the card is ready to receive commands. Reflects the state of the bit of the same name in the Configuration Status Register.

BC (LD4) Indicates that the card is operating in the BC or BC/RT mode.

RT (LD5) Indicates that the card is operating in the RT mode.

BM (LD6) Indicates that the card is operating in the BM mode (this LED may be lit alone or with the RT or BC LED).

BUS A (LD7) Indicates activity on Bus A

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BUS B (LD8)	Indicates activity on BUS B

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DIP SWITCH SETTINGS

The EXC-1553VME/E-V board contains 3 Dip Switches which control the 1553 coupling of the EXC-1553VME/E-V (direct or transformer) and the Logical Address of board. The definition of each switch is described below.

Card Logical Address DIP SWITCH SETTING

Dip switch SW3 is used to select the card's Logical Address as described in the section "VME/VXI Configuration Registers". The Logical Address is set as shown below.

Logical Address Switch (SW3)

MSB							LSB
1	2	3	4	5	6	7	8
A13	A12	A11	A10	A9	A8	A7	A6

note: numbers indicate switch positions.

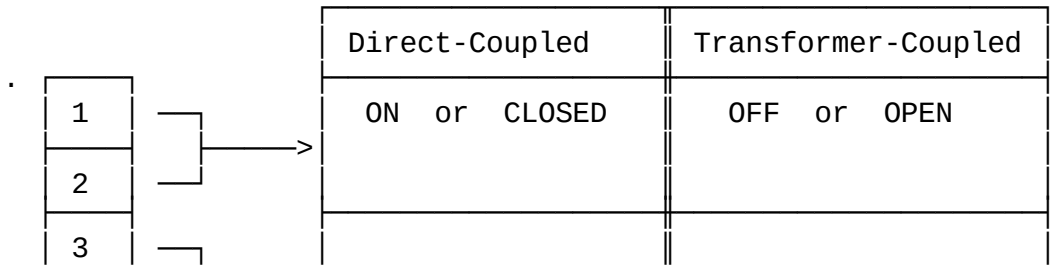
Switch "ON" or "Closed" = logic 0 at bit position
Switch "OFF" or "OPEN" = logic 1 at bit position

Example: for a logical address of 80Hex, set position `1' to "OFF" or "OPEN" and ALL other switches to "ON" or "CLOSED". This is the factory default setting.

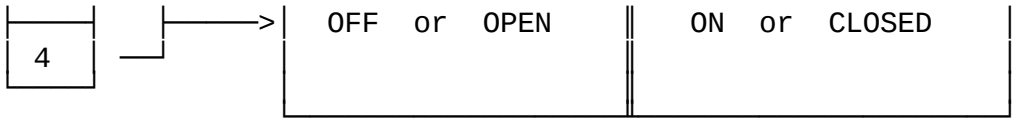
1553 Coupling Mode Select DIP SWITCH SETTING

These 2 switches (SW1 for 1553 Channel "A", SW2 for 1553 Channel "B") select the coupling mode to the 1553 Bus. The EXC-1553VME/E-V can be either DIRECT or TRANSFORMER coupled (factory default) to the 1553 BUS.

Refer to this diagram for BOTH (Channel A and Channel B) switches.



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Factory Default Dip Switch Settings

SW1, SW2 are set to Transformer (Stub) Coupled mode (1,2 off; 3,4 on)
SW3 is set to Logical Address 80H (1 off; 2-8 on = A16 address E000 H)

JUMPERS

Unless otherwise specified, all jumpers should be normally "out".
Because the placement of jumpers is user specific, care should be
taken that signals which the user chooses to jumper are not already
in use on the VME bus.

VME AND VXI RELATED JUMPERS

JP1	SYSFAIL*	-	P1-C10	Connects card SYSFAIL* to backplane
JP5			------	Factory set
JP31			------	Factory set
JP32			------	Factory set
JP35			------	Factory set
JP2	A32SEL		------	Jumper in: A24 address space
				Jumper out: A32 address space
JP36	TTAGCKSRC		------	Time Tag Clock Source:
				Jumper out - internal oscillator
				Jumper in - VME `SYSCLK' signal

VME RELATED JUMPERS

JP29 & JP8	1553BH	-	P2-C04	Connects 1553 bus to backplane P2 connector
JP30 & JP14	1553BL	-	P2-C08	"
JP10	SHIELDB	-	P2-C05	"
JP27 & JP24	1553AH	-	P2-C24	"
JP28 & JP22	1553AL	-	P2-C20	"
JP26	SHIELDA	-	P2-C25	"

NOTE: 10 jumpers are needed to connect the 1553 bus to the backplane.

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If the 1553 bus is not to be connected to the backplane then all 10 jumpers should be removed.

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VXI RELATED JUMPERS To continue the VXI Local Bus

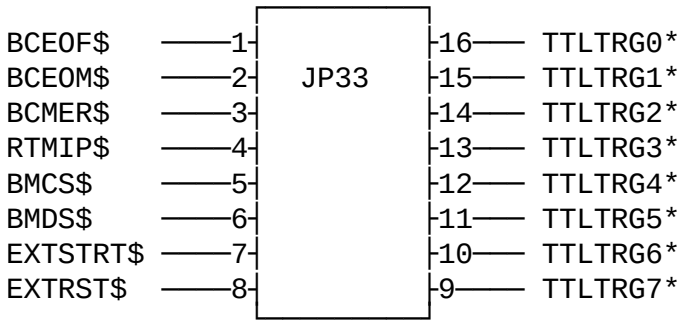
JP9 LBUS00 - (P2-A05) Connects LBUSA00 to LBUSC00 (P2-C05)
JP11 LBUS01 - (P2-A06) Connects LBUSA01 to LBUSC01 (P2-C06)
JP13 LBUS02 - (P2-A08) Connects LBUSA02 to LBUSC02 (P2-C08)
JP12 LBUS03 - (P2-A09) Connects LBUSA03 to LBUSC03 (P2-C09)
JP15 LBUS04 - (P2-A11) Connects LBUSA04 to LBUSC04 (P2-C11)
JP16 LBUS05 - (P2-A12) Connects LBUSA05 to LBUSC05 (P2-C12)
JP17 LBUS06 - (P2-A14) Connects LBUSA06 to LBUSC06 (P2-C14)
JP18 LBUS07 - (P2-A15) Connects LBUSA07 to LBUSC07 (P2-C15)
JP19 LBUS08 - (P2-A17) Connects LBUSA08 to LBUSC08 (P2-C17)
JP20 LBUS09 - (P2-A18) Connects LBUSA09 to LBUSC09 (P2-C18)
JP21 LBUS10 - (P2-A20) Connects LBUSA10 to LBUSC10 (P2-C20)
JP23 LBUS11 - (P2-A21) Connects LBUSA11 to LBUSC11 (P2-C21)

JP25 MODID - P2-A30 Connects card MODID* to backplane
JP34 EXTRST$ ------ External card reset

JP3, JP4, JP6 & JP7 ASTRT/ASTP ------ Async. Start/Stop BCRT

JP33 TTLTRG0* - TTLTRG7* 16 pin jumper block for TTL TRIGGER SIGNALS, described below.

The jumper block JP33 is provided with wire wrap pins. Each one of the pins 1-8 may be wired to any one of the TTL TRIGGER LINES 0-7 according to the needs of the user.



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TTL TRIGGER OUTPUT SIGNALS:

BCEOF$ - Signal pulses low (~50ns.) at END OF FRAME in BC mode.

BCEOM$ - Signal pulses low (~50ns.) at END OF MESSAGE in BC mode.

BCMER$ - Signal pulses low (~50ns.) if ERROR IN MESSAGE in BC mode.

RTMIP$ - Signal remains low for duration of message in RT mode.

BMCS$ - Signal remains low (16usec.) while COMMAND is on bus in BM mode.

BMDS$ - Signal remains low (16usec.) while DATA is on bus in BM mode.

TTL TRIGGER INPUT SIGNALS:

EXTSTRT$ - The BCRT section of the card may be "started" externally. This achieves the same effect as writing a "1" to bit 0 of the Start register. The card may be started synchronously or asynchronously depending on the state of jumpers JP6, JP7, JP3, and JP4. When started synchronously, the card starts synchronously with the ECL clock CLK10-+ after EXTSTRT$ is held low (150ns. minimum). When started asynchronously, the card starts immediately after a falling edge on EXTSTRT$.

SYNCHRONOUS START:
JP3 Short pins 2 and 3
JP4 Short pins 1 and 2
JP6 & JP7 ; BOTH shorted
ASYNCHRONOUS START:
JP3 Short pins 1 and 2
JP4 Short pins 2 and 3

EXTRST$ - The card may be initialized by applying a low going pulse (100ns. minimum) on this line. The initialization function performed here is the same as that performed by writing to the Card Initialization Register. If this function is enabled then pins 1 and 2 of JP34 must be shorted. If it is not, then pins 2 and 3 of JP34 **must** be shorted together.

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JUMPER SETTINGS VME ; FACTORY DEFAULT SETTINGS
(minimum configuration mode)

JP2	Installed:	A24 Address Space (default)
	Removed :	A32 Address Space
JP34	Short pins 2 and 3:	No External Reset Option allowed on VME bus. (default)
JP3	unshorted (2 & 3):	No External Start Option allowed on VME bus (default)

Note: All other jumpers should be left open.

JUMPER SETTINGS VXI ; FACTORY DEFAULT SETTINGS
(minimum configuration mode)

JP2	Installed:	A24 Address Space (default)
	Removed :	A32 Address Space
JP34	Short pins 2 and 3:	Disable Ext. Reset Option (default)
JP3	2 and 3 Not shorted:	Disable External Start Option
JP25	Installed ;	Connect MODID to bus

Note: For this minimum configuration, all other jumpers should be left open.

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CONNECTORS

The EXC-1553VME/E-V contains four connectors:

a) two female 1553 Twinax concentric connectors (P3 and P4) designed to mate with Trompeter "PL75" male-type twinax connector (not supplied).

b) two DIN type 96 pin VME/VXI connectors (P1 and P2)

CONNECTOR P4 PINOUT

Pin Name	Signal Name
CENTER	BUS A (HI)
INNER SHEATH	BUS A* (LO)
OUTER SHEATH	SHIELD

CONNECTOR P3 PINOUT

Pin Name	Signal Name
CENTER	BUS B (HI)
INNER SHEATH	BUS B* (LO)
OUTER SHEATH	SHIELD

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CONNECTOR P1 PINOUT

Pin #	Signal Name
A1	D00
A2	D01
A3	D02
A4	D03
A5	D04
A6	D05
A7	D06
A8	D07
A9	GND
A10	SYSCLK
A11	GND
A12	DS1*
A13	DS0*
A14	WRITE*
A15	GND
A16	DTACK*
A17	GND
A18	AS*
A19	GND
A20	IACK*
A21	IACKIN*
A22	IACKOUT*
A23	AM4
A24	A07
A25	A06
A26	A05
A27	A04
A28	A03
A29	A02
A30	A01
A31	-12V
A32	+5V

Pin #	Signal Name
B1	
B2	
B3	
B4	BG0IN*
B5	BG0OUT*
B6	BG1IN*
B7	BG1OUT*
B8	BG2IN*
B9	BG2OUT*
B10	BG3IN*
B11	BG3OUT*
B12	
B13	
B14	
B15	
B16	AM0
B17	AM1
B18	AM2
B19	AM3
B20	GND
B21	
B22	
B23	GND
B24	IRQ7*
B25	IRQ6*
B26	IRQ5*
B27	IRQ4*
B28	IRQ3*
B29	IRQ2*
B30	IRQ1*
B31	
B32	+5V

Pin #	Signal Name
C1	D08
C2	D09
C3	D10
C4	D11
C5	D12
C6	D13
C7	D14
C8	D15
C9	GND
C10	SYSFAIL*
C11	
C12	SYSRESET*
C13	LWORD*
C14	AM5
C15	A23
C16	A22
C17	A21
C18	A20
C19	A19
C20	A18
C21	A17
C22	A16
C23	A15
C24	A14
C25	A13
C26	A12
C27	A11
C28	A10
C29	A09
C30	A08
C31	+12V
C32	+5V

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CONNECTOR P2 PINOUT

Pin #	Sig. Name		Pin #	Sig. Name		Pin #	Sig. Name	
A1			B1	+5V		C1	CLK10+	(x)
A2			B2	GND		C2	CLK10-	(x)
A3			B3			C3		
A4			B4	A24		C4	-5.2V/1553BH	(x)
A5	LBUSA00	(x)	B5	A25		C5	LBUSC00/SHLDB	(x)
A6	LBUSA01	(x)	B6	A26		C6	LBUSC01	(x)
A7			B7	A27		C7		
A8	LBUSA02	(x)	B8	A28		C8	LBUSC02/1553BL	(x)
A9	LBUSA03	(x)	B9	A29		C9	LBUSC03	(x)
A10			B10	A30		C10		
A11	LBUSA04	(x)	B11	A31		C11	LBUSC04	(x)
A12	LBUSA05	(x)	B12	GND		C12	LBUSC05	(x)
A13			B13	+5V		C13		
A14	LBUSA06	(x)	B14			C14	LBUSC06	(x)
A15	LBUSA07	(x)	B15			C15	LBUSC07	(x)
A16			B16			C16		
A17	LBUSA08	(x)	B17			C17	LBUSC08	(x)
A18	LBUSA09	(x)	B18			C18	LBUSC09	(x)
A19			B19			C19		
A20	LBUSA10	(x)	B20			C20	LBUSC10/1553AL	(x)
A21	LBUSA11	(x)	B21			C21	LBUSC11	(x)
A22			B22	GND		C22		
A23	TTLTRG0*	(x)	B23			C23	TTLTRG1*	(x)
A24	TTLTRG2*	(x)	B24			C24	TTLTRG3*/1553AH	(x)
A25			B25			C25	SHLDA	(x)
A26	TTLTRG4*	(x)	B26			C26	TTLTRG5*	(x)
A27	TTLTRG6*	(x)	B27			C27	TTLTRG7*	(x)
A28			B28			C28		
A29			B29			C29		
A30	MODID	(x)	B30			C30		
A31			B31	GND		C31		
A32			B32	+5V		C32		

Notes: (x) - VXI or optional 1553 signals (each of them is unconnected, unless the specific jumper is shorted. see JUMPERS above)

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POWER REQUIREMENTS

BOARD TYPE	+5v	+12v	-12v
EXC-1553VME-VXI/E-V	2.8A	150ma	150ma
EXC-1553VME-VXI/E-V-NM	2.1A	150ma	150ma

ORDERING INFORMATION

EXC-1553VME/E-V 1553 VME/VXI B-size (6"x9") board with variable amplitude, "universal" transceivers.
Supports BC, RT, BC/RT and BM Modes.

EXC-1553VME/E-V-NM As EXC-1553VME/E-V excluding BM Mode.

EXC-1553VXI/E-V 1553 VXI C-size (13"x9") board with variable amplitude, "universal" transceivers.
Supports BC, RT, BC/RT and BM Modes.
Supplied with RFI/EMI shield.

EXC-1553VXI/E-V-NM As EXC-1553VXI/E-V excluding BM Mode, supplied with RFI/EMI shield.

EXC-1553VXI/E-V-NM-NS As EXC-1553VXI/E-V excluding BM Mode, supplied without RFI/EMI shield.

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Version Description Document

EXC-1553VME/E-V & EXC-1553VXI/E-V

Firmware revision 3.0

In accordance with Excalibur's proven track record as an industry leader in the field of avionics board level test and simulation products, Excalibur has introduced an extensive range of improvements to its VME and VXI series of Mil-Std-1553 testers.

Excalibur EXC-1553VME/E-V and EXC-1553VXI/E-V boards bearing firmware revisions 3.0 and higher represent a quantum jump in both hardware and firmware functionality. While these boards remain upward compatible with earlier versions of the board, hardware and firmware changes make them the most robust and high performance Excalibur 1553 products ever. Most notably, all modes now handle intermessage gap times of four microseconds. Additionally, programmable intermessage gap times in the Bus Controller mode are far more accurate than in the past.

The following list of changes is divided into those that are global and those which are relevant to a particular operational mode. Points denoted with an asterisk represent minor programming changes which the user is requested to take special note of.

Global Changes

1) The Variable Amplitude Register now defaults to 255 (7.5 Volts peak to peak on bus) on power up or software reset.

2) A new jumper, JP36, enables the user to select whether the time tag clock source comes from an internal clock or the VME 'SYSCLK'. The latter permits the synchronization of multiple cards.

3) Cards now support an optional piggyback Word Pattern Generator (1553WPG-V) adapter which can be used to transmit sequences of 1553 words with a resolution of 50 nsec. This is ideal for injecting the manchester error patterns defined in the RT Validation Test Plan. The WPG occupies addresses 0 - 8FFFH and is enabled by settings its associated enable bit within the Zero Crossing Register.

4) In the Board Status Register, the '16K RAM OK' and '2K RAM OK' bit definitions have been changed to 'RAM OK' and 'TIMERS OK', respectively.

5) In the BC, RT, an BC concurrent RT operational modes, hardware has been added to allow two separate self- test functions: Internal_Loopback_Test and External_Loopback_Test (requires external loopback cable). The loopback

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tests may be activated by writing appropriate codes to the Board Configuration Register and starting the card.

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6) Card internal operation is significantly faster and thus recovery times after power-on and software reset have been greatly decreased.

7) The board's +5 Volt power requirements have been increased.

BC Mode Changes

1)* In BC mode the programmable intermessage gap time (IGT) range is programmable from 4 usec. (bus dead time) to 665 seconds. The programmed value is added to the minimum 4 usec. (a value of '0' sets the IGT to 4 usec.).

2) The Jump command has been included within the BC Command Code of the Control Word.

3) The minimum gap between transmission of the last word in frame and transmission of the first word in the following frame is now 20 microseconds (down from 120 usec.).

4) Word count error injection now allows sending BC to RT messages with '0' data words.

5) In the Message Status Word, the Internal Test Error bit is now reserved.

6)* The Instruction Counter now cycles between its initial value and 1, rather than from its initial value minus 1 and 0. This simplifies checking of the current message.

RT Mode Changes

1) The RT can now handle messages with the minimum 4 usec. intermessage gap time (mid bit to mid bit) permitted by the 1553 specification.

2)* The RT time tag is derived from a 16 bit hardware counter whose resolution may be set in steps of 4 usec. by the 8 bit Time Tag Resolution Register. The time tag is stored during the reception of the command word (the first command word in the case of RT-RT commands). Note that the Time Tag Preset Register is no longer implemented.

3) Bit count error injection now supports +/- 1, 2 or 3 bits.

4)* The RT response time is now fully programmable from 4 usec. to 43.5 usec. (bus dead time).

5)* A new bit which selects either 1553B or non-1553B environments has been defined in the Status Response Register (applies to firmware revision 3.4

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and higher).

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BC/Concurrent RT Mode Changes

1) All changes listed under BC mode also apply to BC Concurrent RT mode.

2)* The Message Block Conrol Word is now the same as that in BC mode (error placement can be selected either in a Command or Data words).

Bus Monitor Mode Changes

1)* A new register, the Broadcast Control Register, enables the user to instruct the board whether or not to expect Status Words on messages directed to RT #31.

2)* The time tag is a 32 bit counter and is stored during reception of the command word (the first command word in the case of RT-RT commands). Note that the 16 bit time tag mode, Time Tag Preset, and Time Tag Resolution registers are no longer implemented.

3)* Two new bits have been defined in the Message Status Word: MESSAGE ERROR SET BIT and RT STATUS BITS SET. These bits operate as in the BC Message Status Word.

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