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DAS-429PCI/Mx

Multi-channel ARINC 429
Test and Simulation Board
for PCI Systems

User's Manual

EXCALIBUR SYSTEMS

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1 Introduction

Chapter 1 provides an overview of the *DAS-429PCI/Mx* avionics communication board. The following topics are covered:

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1.1 Overview

The *DAS-429PCI/Mx* is a modular ARINC-429 memory-mapped, multi-channel (up to 24) test, simulation, and monitor board for PCI systems. The *DAS-429PCI/Mx* provides a total solution for developing and testing ARINC-429 interfaces and for performing system simulation of the ARINC-429 bus, both in the lab and in the field.

The *DAS-429PCI/Mx* is based on the latest Surface Mount Technology, which substantially reduces the area required. The *DAS-429PCI/Mx* comes configured with 2(x) transmit and 4(x) receive channels (where x = number of modules ordered). The channels are organized in four independent modules (P/N: M429R4T2), each configured with 4 receive and 2 transmit channels. Each module contains an on board hi-speed controller and 16K x 16 true dual-port RAM. Each module is accessed through a paging mechanism and operates independently. Each module can be set up to generate interrupts to the host in a variety of circumstances through an extensive interrupt structure. Both transmit and receive channels may be programmed for Hi (100Khz) or Lo (12.5Khz) speed bit rates. In addition, either odd or even parity may be programmed for transmit channels.

All control registers and data blocks can be accessed directly in real time. The board supports filtering of receive data and multiple data storage modes. Status and time tag information are appended to each word. The transmit channels operate via a transmitter "instruction" stack which allows scheduling of data transmissions and reduces the need for host computer intervention. The *DAS-429PCI/Mx* comes complete with C driver software libraries, including source code.

The *DAS-429PCI/Mx* is ideally suited for developing, simulating, testing and monitoring ARINC-429 interfaces for multi-channel applications requiring a single PCI board.

DAS-429PCI/Mx Board Features:

- Up to 24 ARINC-429 channels (Receive and Transmit)
- Eurocard 3U size
- Compatible with PCI computers
- Easy to install and operate
- Organized in 4 modules, each containing:
  - 4 Receive channels
  - 2 Transmit channels
  - 16k ×16 true dual-port RAM
  - On board 32 bit processor
- 12.5Khz bit and 100Khz bit data rates
- Selectable even/odd parity
- Programmable interword gap
- Real time operation
- Transmission modes:
  - One-shot
  - Loop
  - N-times
- Two Receive/Monitor modes:
  - Sequential
  - Look-up table
- 32 bit time tagging per word
- Merge mode stores data from multiple receive channels in one buffer
- Label filtering
- Start triggers
- Receive count interval triggers
- Interrupt and polling modes of operation

See **Chapter 6: Ordering Information** for exact part numbers.

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Figure 1-1 below illustrates the *DAS-429PCI/Mx*'s block diagram

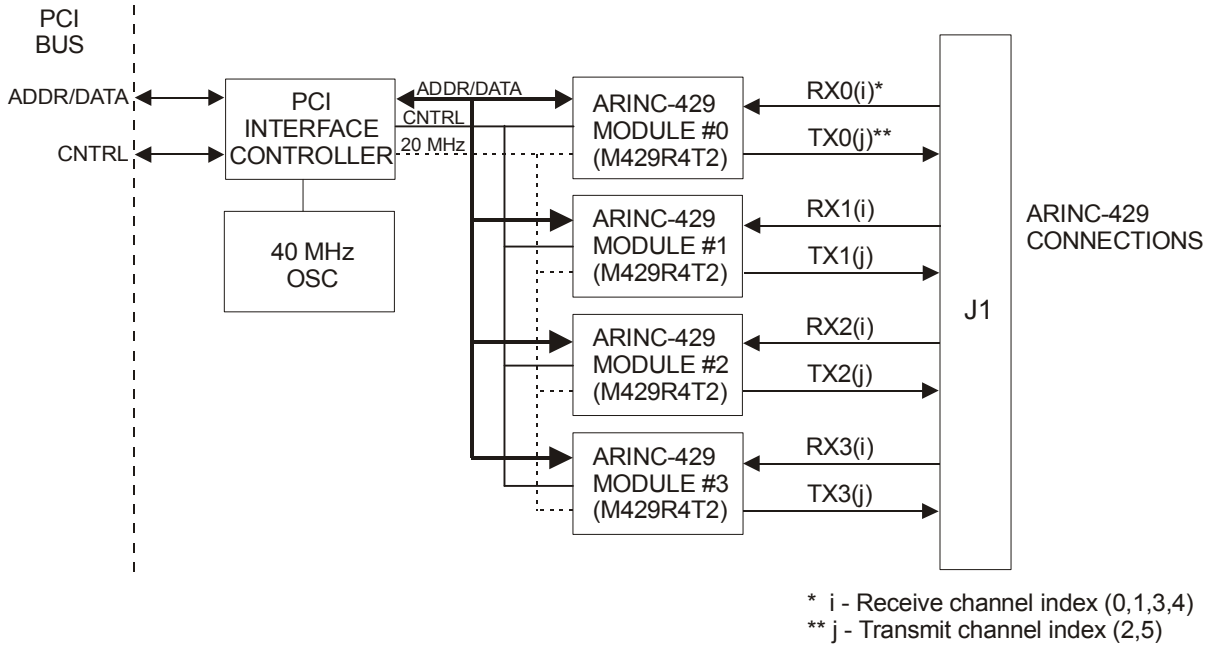


Figure 1-1 *DAS-429PCI/Mx* Block Diagram

Figure 1-2 below illustrates the block diagram of a single M429R4T2 module.

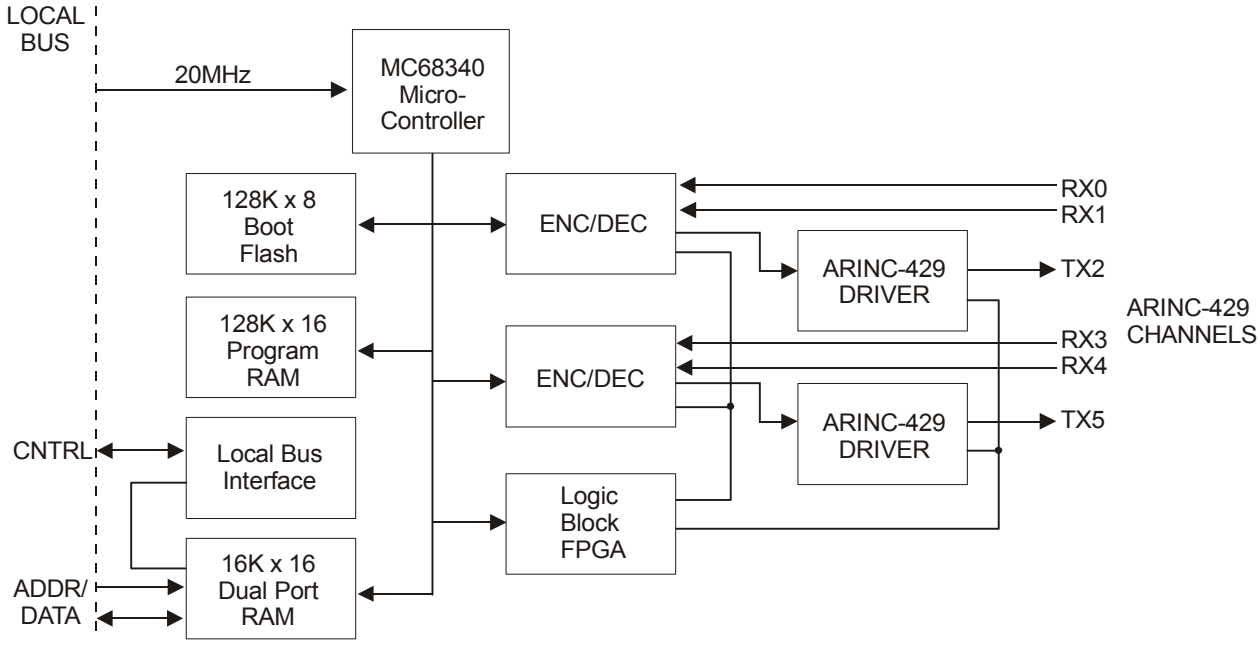


Figure 1-2 M429R4T2 Module Block Diagram

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1.2 Installation

DAS-429PCI/Mx installation includes installing the software for each system and installing the board.

1.2.1 Software Installation

The *DAS-429PCI/Mx* is delivered with software compatible with several operating systems. For information about installing the accompanying software drivers, see the appropriate **ReadMe.pdf** on the *Excalibur Installation CD* that came with your board.

1.2.2 Board Installation

Installation of the *DAS-429PCI/Mx* board is similar to that of all PCI "Local Bus" boards. The *DAS-429PCI/Mx* complies with the "Plug and Play" specification of the PCI standard, and as such its absolute address is determined by the BIOS at system start-up.

Warning Wear a suitably grounded electrostatic discharge wristband whenever handling an Excalibur board.

To install the DAS-429PCI/Mx:

1. **Make certain the computer power source is disconnected.**
   Insert the *DAS-429PCI/Mx* board into any PCI compatible slot.
2. Attach the mating connector (wired with the ARINC-429 connections) to the board. The cables may be connected to and disconnected from the board while power to the computer is turned on, but not while the board is transmitting over the bus.

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1.3 Memory Structure

There are two distinct areas of memory in the *DAS-429PCI/Mx*. The first area, the PCI Configuration Space Header Region, is located in a fixed location in host memory and contains all information necessary for the Plug and Play operation of the board. The address of this region is fixed in the hardware.

The second area, the Control/Data Region, contains dual-port RAM and the Control Registers used in setting up the board as a ARINC-429 interface. The Control/Data Region is divided into five memory Pages (Pages 0-4). A Page is a block of memory which has been assigned a unique base address by the Plug and Play BIOS. The base address of each Page is determined by the BIOS following power-up and is written into the Base Address Registers 0-4 located in the PCI Configuration Space Header. The memory structure is shown below in Figure 1-3.

PCI Configuration Space Header Region	256 bytes	PCI Bus Plug and Play Parameters
Control/Data Region	64 bytes - Page 0	PCI Global Interrupt Control Registers
	16K × 16 - Page 1	Module 0 (4 Rx and 2 Tx 429 channels)
	16K × 16 - Page 2	Module 1 (4 Rx and 2 Tx 429 channels)
	16K × 16 - Page 3	Module 2 (4 Rx and 2 Tx 429 channels)
	16K × 16 - Page 4	Module 3 (4 Rx and 2 Tx 429 channels)

Figure 1-3 *DAS-429PCI/Mx* Memory Structure

Note: Throughout this manual the following terms are used interchangeably:
Page 1 and Module 0
Page 2 and Module 1
Page 3 and Module 2
Page 4 and Module 3

Page 1/Module 0 refers to ARINC-429 Module 0
Page 2/Module 1 refers to the optional ARINC-429 Module 1
Page 3/Module 2 refers to the optional ARINC-429 Module 2
Page 4/Module 3 refers to the optional ARINC-429 Module 3

If you have the DAS-429PCI/M1, DAS-429PCI/M2 or DAS-429PCI/M3 boards, ignore references to the modules not included on your board.

See **Chapter 6: Ordering Information** for exact part numbers.

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1.4 PCI Configuration Space Header

The *DAS-429PCI/Mx* includes a PCI Configuration Space Header, as required by the PCI specification. The registers contained in this header enable software to set up the Plug and Play operation of the board, and set aside system resources.

The PCI Configuration Space Header contents are stored in on-board non-volatile memory (nvRAM), at the factory. You should not alter the contents of the nvRAM. When you power-up, this 'Boot-Load' nvRAM is automatically loaded into the PCI Configuration Space Header.

MAX_LAT	MIN_GNT	Interrupt Pin	Interrupt Line	3C H
Reserved = 0s				38 H
Reserved = 0s				34 H
Expansion ROM Base Address (not used)				30 H
Reserved =0s				2C H
Reserved =0s				28 H
Base Address Register #5 (not used)				24 H
Base Address Register #4 (not used)				20 H
Base Address Register #3 (not used)				1C H
Base Address Register #2 (Control/Data Region Page 2)				18 H
Base Address Register #1 (Control/Data Region Page 1				14 H
Base Address Register #0 (Control/Data Region Page 0				10 H
BIST	Header Type = 0	Latency Timer	Cache Line Size	0C H
Class Code			Rev ID	08 H
Status Register		Command Register		04 H
Device ID		Vendor ID		00 H
31 24	**23 16**	**15 08**	**07 00**	

Figure 1-4 PCI Configuration Space Header

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1.5 PCI Configuration Registers

This section describes the registers contained in the PCI Header Space.

1.5.1 Vendor Identification Register (VID) Address: 00–01 (H)

Power-up value	1405 H
Boot-load	External nvRAM offset 040–41 H
Attribute	Read Only
Size	16 bits

The Vendor Identification register contains the PCI Special Interest Group vendor identification number assigned to Excalibur Systems.

Bit	Description
00-15	1405 H

1.5.2 Device Identification Register (DID) Address: 02–03 (H)

Power-up value	2000 H
Boot-load	External nvRAM offset 042–43 H
Attribute	Read Only
Size	16 bits

The Device Identification register contains the vendor assigned device identification number.

Bit	Description
00-15	2000 H

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1.5.3 PCI Command Register

Address: 04–05 (H)

Power-up value	0000 H
Boot-load	Not used
Attribute	Read/Write (R/W on bits 6, Read Only for all others)
Size	16 bits

The PCI Command register contains the PCI Command.

Bit	Bit Name	Description
10-15	**Reserved**	Set to 0s
09	**Fast Back-to Back Enable**	Always set to 0
08	**System Error Enable**	When set to 1, this bit permits the PCI Controller to drive the open drain output pin, SERR#. This bit is cleared to 0 upon RESET#. The SERR# pin driven active normally signifies a parity error on the address/control bus.
07	**Wait Cycle Enable**	Always set to 1
06	**Parity Error Enable**	When set to 1, this bit allows this controller to check for parity errors. When a parity error is detected, the PCI bus signal PERR# is asserted. This bit is cleared (parity testing disabled) upon the assertion of RESET#.
05	**Palette Snoop Enable**	Always set to 0
04	**Memory Write and Invalidate Enable**	Always set to 0
03	**Special Cycle Enable**	Always set to 0
02	**Bus Master Enable**	Always set to 0
01	**Memory Access Enable**	This bit allows the PCI Controller to decode and respond as a target for memory regions that may be defined in one of the three base address registers. This bit is initialized to 0 upon the assertion of signal pin RESET#.
00	**I/O Access Enable**	This bit allows the PCI Controller to decode and respond as a target to I/O cycles which are to regions defined by any one of the three base address registers. This bit is initialized to 0 upon the assertion of signal pin RESET#.

PCI Command Register

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1.5.4 PCI Status Register (PCISTS) Address: 06–07 (H)

Power-up value: 0080 H
Boot-load: Not used
Attribute: Read Only (RO), Read/Write Clear (RWC)
Size: 16 bits

The PCI Status register contains the PCI status information. Most status bits in this register are designated as "write clear," meaning that in order to clear a given bit, the bit must be written as a 1. All bits written with a 0 are left unchanged. These bits are identified below as (R/WC), while those which are Read Only are shown as (RO).

Bit	Bit Name	Description
15	Detected Parity Error (R/WC)	This bit is set whenever a parity error is detected. It functions independently from the state of Command Register Bit 6. This bit may be cleared by writing a 1 to this location.
14	Signaled System Error (R/WC)	This bit is set whenever the device asserts the signal SERR#. This bit can be reset by writing a 1 to this location.
13	Received Master Abort (R/WC)	This bit is set whenever a bus master abort occurs. This bit can be reset by writing a 1 to this location.
12	Received Target Abort (R/WC)	This bit is set whenever this device has one of its own initiated cycles terminated by the currently addressed target. This bit can be reset by writing a 1 to this location.
11	Signaled Target Abort (R/WC)	This bit is set whenever this device aborts a cycle when addressed as a target. This bit can be reset by writing a 1 to this location.
09-10	Device Select (DEVSEL#) Timing Status (RO)	These bits are read-only and define the signal behavior of DEVSEL# from this device when accessed as a target.

Bit 09	Bit 10	Description
0	0	Fast (PCI Controller)
0	1	Medium
1	0	Slow
1	1	Reserved

08	Data Parity Reported (R/WC)	This bit is set upon the detection of a data parity error for a transfer involving the PCI Controller as the master. The Parity Error Enable bit (D6 of the Command Register) must be set in order for this bit to be set. Once set, it can only be cleared by either writing a 1 to this location or by the assertion of the signal RESET#.
07	Fast Back-to-Back Capable (RO)	When equal to 1, this indicates that the device can accept fast back-to-back cycles as a target.
00-06	Reserved (RO)	Always returns 0s

PCI Status Register

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1.5.5 Revision Identification Register (RID) Address: 08 (H)

Power-up value: 00 H

Boot-load: External nvRAM/EPROM offset 048 H

Attribute Read only

Size: 8 bits

The Revision Identification register contains the revision identification number of the *DAS-429PCI/Mx*.

Bit	Description
00-07	Revision identification number

Revision Identification Register

1.5.6 Class Code Register (CLCD) Address: 09–-0B (H)

Power-up value: FF0000 H

Boot-load: External nvRAM offset 049–4B H

Attribute Read only

Size: 24 bits

The Class Code register is divided into three one-byte fields, residing in the following locations:

- Base class - 0B H
- Sub-class - 0A H
- Programming interface - 09 H

The Class Codes of the *DAS-429PCI/Mx* are set as indicated below:

Bit	Address	Fields	Value	Description
00-07	0B H	Base Class	07H	Simple communication controller
00-07	0A H	Sub-Class	80H	Other communications device
00-07	09 H	Prog I/F	00H	Register Level Programming Interface

Class Code Register

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1.5.7 Cache Line Size Register (CALN) Address: 0C (H)

Power-up value: 00 H, hardwired
Boot-load: Not used
Attribute: Read only
Size: 8 bits

The Cache Line Size Register is hardwired to 0.

Bit	Description
00-07	Cache Line Size (RO)

Cache Line Size Register

1.5.8 Latency Timer Register (LAT) Address: 0D (H)

Power-up value: 00 H
Boot-load: External nvRAM offset 04D H
Attribute: Read/Write bits 03–07; Read only bits
Size: 8 bits

The Latency Timer register has meaning only for bus masters and therefore is not used with the *DAS-429PCI/Mx*.

Bit	Bit Name	Description
03-07	Latency Timer Value (R/W)	Always set to 0
00–02		Always returns to 0

Latency Timer Register

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1.5.9 Header Type Register (HDR). Address: 0E (H)

Power-up value: 00 H
Boot-load: External nvRAM offset 04E H
Attribute: Read only
Size: 8 bits

The Header Type register consists of two fields:

Bits 00–06 define the format for bytes 10 H – 3F H of the device configuration header

Bit 07 = 0 established that the PCI controller is a single function PCI device.

Bit	Description
07	0 PCI Controller is a single function PCI device
00–06	Always returns 0

Header Type Register

1.5.10 Built-In Self-Test Register (BIST) Address: 0F (H)

Power-up value: 00 H
Boot-load: External nvRAM/EPROM offset 04F H
Attribute: Read only: bits 07 and 00–05
Write only: bit 06 as PCI bus
Size: 8 bits

The Built-In Self-Test register is not implemented in the *DAS-429PCI/Mx*.

Bit	Bit Name	Description
07	BIST Capable (RO)	Always returns 0
06	Start BIST (WO)	Always set to 0
04–05	Reserved	Always returns 0
00–03	User Defined Completion Code (RO)	Always returns 0

Built-in Self-Test Register

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1.5.11 Base Address Registers (BADR) Address: 10, 14, 18, 1C, 20, 24 (H)

Power-up value: FFFFFFC1 H for offset 10 H; 00000000 H for all other registers

Boot-load: External nvRAM offset 50 H, 54 H, 58 H, 5C H, 60 H (BADRO–4)

Attribute: Read/Write: high bits; Read only: Low bits

Size: 32 bits

The Base Address Registers are used by the system BIOS to determine the number, size and base addresses of memory pages required by the board, within host address space.

The host determines the page base addresses by interrogating these registers after BIOS power-up initialization. Bit zero of each field is used to select whether the space required is to be decoded as memory (bit 00 = 0) or I/O (bit 00 = 1). The absolute base addresses of these pages are determined from information written back to the Base Address Registers, by the BIOS (see also "Determining Base Address Size").

Up to five memory pages are required by the *DAS-429PCI/Mx*: one for each ARINC-429 module present and one for the PC Global Interrupt Control Registers (see the table below).

Register	Offset	Size	Function
Base Address Register 0 (PAGE 0)	10H	64Byte	PCI Global Interrupt Control Registers
Base Address Register 1 (PAGE 1)	14H	32Kb	ARINC-429 Module 0
Base Address Register 2 (PAGE 2)	18H	32Kb	ARINC-429 Module 1
Base Address Register 3 (PAGE 3)	1CH	32Kb	ARINC-429 Module 2
Base Address Register 4 (PAGE 4)	20H	32Kb	ARINC-429 Module 3

Base Address Registers Definitions

Note: The contents of Base Address Register 0 are not loadable from nvRAM.

DETERMINING BASE ADDRESS SIZE

The address space defined by a given base address register is determined by writing all 1s to a given base address register from the PCI bus and then reading that register back. The number of 0s returned starting from D4 for memory space and D2 for I/O space toward the high-order bits reveals the amount of address space desired. The table below gives the required nvRAM/EPROM boot values corresponding to Pages 1–4.

PAGE	nvRAM Offset	nvRAM Contents
PAGE 1	50 H	FFFF8000 H
PAGE 2	54 H	FFFF8000 H
PAGE 3	58 H	FFFF8000 H
PAGE 4	5C H	FFFF8000 H

Table 1-1 Address nvRAM/EPROM Boot Values

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Bit	Bit Name	Description
04-31	Base Address Location (RW)	These bits are used to position the decoded region in memory space. Only bits which return a 1 after being written as 1 are usable for this purpose. Except for Base Address Register 0, these bits are individually enabled by the contents sourced from the external boot memory.
03	Prefetchable (RO)	When set as a 1, this bit signifies that this region of memory can be cached. Cachable regions can only be located in the region altered through PCI bus memory writes. This bit, when set, also implies that all read operations will return the data associated for all bytes regardless of the Byte Enables. Memory space which cannot support this behavior should leave this bit in the zero state. For Base Addresses 1 through 4, this bit is set by the Reset pin and later initialized by the external boot memory (if present). Base Address Register 0 always has this bit set to 0. This bit is read only from the PCI interface.
01-02	Memory Type (RO)	These two bits identify whether the memory space is 32 or 64 bits wide and if the space location is restricted to be in the first megabyte of memory space. The encoding is as follows:

Bits 02	01	Description
0	0	Region is 32 bits wide and can be located anywhere in 32 bit memory space.
0	1	Region is 32 bits wide and must be mapped below the first MByte of memory space.
1	0	Not support
1	1	Not supported

00	Memory Space Indicator (RO)	When set to 0, this bit identifies a base address region as a memory space.

Base Address Register – Memory (bit 00 = 0)

Bit	Bit Name	Description
02-31	Base Address Location (R/W)	These bits are used to position the decoded region in I/O space. Only bits which return a 1 after being written as 1 are usable for this purpose. Except for Base Address 0, these bits are individually enabled by the contents sourced from the external boot memory (EPROM or nvRAM).
01	Reserved	This bit should be zero. (Note: Disabled Base Address Registers will return all zeros for the entire register location, bits 31 through 00).
00	I/O Space Indicator (RO)	When set to 1, this bit identifies a base address region as an I/O space.

Base Address Register – I/O (bit 0 = 1)

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1.5.12 Expansion ROM Base Address Register (XROM) Address: 30 (H)

Power-up value: 00000000 H
Boot-load: External nvRAM offset 70 H
Attribute Read/Write: bits 11–31, bit 00; Read only: bits 01–10
Size: 32 bits

The Expansion ROM Space is not implemented on the *DAS-429PCI/Mx*.

Bit	Bit Name	Description
11-31	Expansion ROM Base Address Location (R/W)	Don't Care
01–10	Reserved	Always returns 0
00	Address Decode Enable (R/W)	Always set to 0

Expansion ROM Base Address Register

1.5.13 Interrupt Line Register (INTLN) Address: 3C (H)

Power-up value: FF H
Boot-load: External nvRAM offset 7C H
Attribute: Read/Write
Size: 8 bits

The Interrupt Line register indicates the interrupt routing for the PCI Controller. The ultimate value for this register is system-architecture specific. For *x*86-based PCs, the values in this register correspond with the established interrupt numbers associated with the dual 8259 controllers used in those machines. In *x*86-based PC systems, the values of 0 to 15 correspond with the IRQ numbers 0 through 15, and the values from 16 to 254 are reserved. The value of 255 (the controller's default power-up value) signifies either "unknown" or "no connection" for the system interrupt. This register is boot-loaded from the external boot memory, if present, and may be written by the PCI interface.

Bit	Description
00–07	Desired IRQ#

Interrupt Line Register

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1.5.14 Interrupt Pin Register (INTPIN) Address: 3D (H)

Power-up value: 01 H
Boot-load: External nvRAM offset 7D H
Attribute: Read only
Size: 8 bits

The Interrupt Pin register identifies which PCI interrupt, if any, is connected to the controller's PCI interrupt pins. The allowable values are 0 (no interrupts) or 1 (INTA#). The default power-up value assumes INTA#.

Bit	Bit Name	Description			
03-07	Reserved	All zeros (RO)			
00-02	Pin Number	**Bit 02**	**Bit 01**	**Bit 00**	**Description**
		0	0	0	None
		0	0	1	INTA#

Interrupt Pin Register

1.5.15 Minimum Grant Register (MINGNT) Address: 3E (H)

Power-up value: 00 H
Boot-load: External nvRAM offset 7E H
Attribute: Read only
Size: 8 bits

The Minimum Grant register is not implemented on the *DAS-429PCI/Mx*.

Bit	Description
00–07	Don't Care

Maximum Grant Register

1.5.16 Maximum Latency Register (MAXLAT) Address: 3F (H)

Power-up value: 00 H
Boot-load: External nvRAM offset 7F H
Attribute Read only
Size: 8 bits

The Maximum Latency register is not implemented on the *DAS-429PCI/Mx*.

Bit	Description
00–07	Don't Care

Maximum Latency Register

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1.6 PCI Global Interrupt Registers

The PCI Global Interrupt Control Registers are used to enable /disable and check the status of interrupts generated on the PCI bus. These registers are located in Page 0 of the *DAS-429PCI/Mx*.

Note: To generate interrupts on the PCI bus, the interrupt condition registers in Modules 0-3 must be programmed according to the interrupt conditions desired.

1.6.1 PCI Interrupt Status Register

Register Name	PCI Interrupt Status Register
Address	1CH
Attribute:	Read/Write
Size:	32 bits

The PCI Interrupt Status register is used to determine the source of the board generated PCI bus interrupt, Module 0-3.

Bit	Bit Name	Description
28-31	Not Used	Don't Care
27	IFLAG3	When set, indicates that Module 3 generated interrupt
26	IFLAG2	When set, indicates that Module 2 generated interrupt
25	IFLAG1	When set, indicates that Module 1 generated interrupt
24	IFLAG0	When set, indicates that Module 0 generated interrupt
00-23	Not Used	Don't Care

PCI Interrupt Status Register

1.6.2 PCI Interrupt Control Register

Register Name	PCI Interrupt Control Register
Address	38H
Attribute:	Read/Write
Size:	32 bits

The PCI Interrupt Control register provides a global enable/disable of board generated PCI interrupts.

Bit	Bit Name	Description
18-31	Not Used	Don't Care
17	GINT	When set, indicates that an interrupt occurred. This bit must be reset, to enable further interrupts. To reset, write a 1 to this bit location.
13-16	Not Used	Always set to 00 H
12	GINTEN	To enable PCI interrupts, write a 1 to this bit.
00-11	INTSEL	Always set to F00 H

PCI Interrupt Control Register

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2 Module Operation

Chapter 2 describes the general principle of module operation, the module memory map, global registers and the module control registers.

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2.5.10 Receiver Merge Configuration Register 2-13
2.5.11 Receiver Merge Interrupt Condition Register 2-14
2.5.12 Receiver Merge Status Register 2-14

Each Page (Module) handles 4 receive and 2 transmit channels, is controlled by its own processor and works independently of the other modules. All 24 channels may be run simultaneously although you may only access one Page (six channels) at a time. The manual describes the functionality of a single Page; all Pages work in an identical manner.

To determine if a module is installed and ready to operate after a power-up or a software reset:

1. Check the Module ID register (test for value = E429 H).
2. Check the Module Status register (See **Module Status Register,** page 2-8)

The module is installed and ready when both registers contain the correct values (as written above). For software reset operations, set these values to 0 immediately prior to writing to the Board Software Reset register.

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2.1 Module General Operation

The M429R4T2 module operation makes extensive use of pointers for setting up the size and location of both receiver and transmitter data blocks, transmitter instruction stacks, and receiver look-up tables. Pointers on the board represent **byte offsets** into the memory area of the board. Each channel has its own pointer registers so that unique memory areas may be allocated for each channel. It is also possible for multiple channels to share memory areas. For example, more than one receiver channel may point to and use the same Label Look-Up Table, which controls which labels will be stored by the board.

After power-up or reset the module is initialized in a "wait" loop — looking for a Start command from the host computer. This command, issued by writing to the Module Start Register, instructs the module to begin operation on the active channel(s).

The transmitter and receiver operations necessary to operate the board are described below in general terms. For more information about operating in these modes, see **Chapter 3: Transmit Mode** and **Chapter 4: Receive/ Monitor Mode**.

After power-up:

1. Set and verify the Module Control registers:
   Check the results of the power-up self-test by reading the Module Status register.
2. Set the Transmitter-related Channel Control registers:
   Program the Channel Configuration registers (bit rate, rise time, etc.)
   Update the Transmit Instruction Stack pointer for each channel.
   Update the Transmit Instruction counter
3. Set the Transmit Instruction blocks:
   Update the Instruction Blocks with information relating to each ARINC TX data block (i.e., parity, pointer to the Tx Data blocks, delay between data blocks) (See **Transmit Instruction Stack,** page 3-6)
4. Write the Transmit Data Blocks:
   Write the ARINC words into the on-board memory at locations pointed to by the instruction stack's TX Data pointers
5. Set up the Receiver-related Channel Control registers:
   Program the Channel Configuration registers (bit rate, etc.)
   Update the [receive data] Start and End pointers.
   Update the "Look-Up Table" Start Address register (if using this mode).
   Update the Filter Table Start Address register.
   Update the Label Trigger register (if using a Label to start storage)
   Update Counter Trigger registers (not required).
6. Start
   Write to the [Module] Start Register setting the appropriate channel(s) "start" bits. Each channel can be "started" individually at different times (See **Start/Stop Register,** page 2-7)
7. Read the Receive Status registers (i.e. Word Counter):
   Read the Receiver Status registers to know how many words have been received
8. Read the Receive Data block:
   Read the ARINC words (and RCV Status and Time Tag Words) from the on-board memory.

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2.2 Module Memory Map

Figure 2-1 Module M429R4T2 Memory Map illustrates the module memory usage.

Global Registers	0000–000E H
Module Control Registers	0010–007E H
Channel Control Register Block 0	0080–00AE H
Channel Control Register Block 1	00B0–00DE H
Channel Control Register Block 2	00E0–010E H
Channel Control Register Block 3	0110–013E H
Channel Control Register Block 4	0140–016E H
Channel Control Register Block 5	0170–019E H
Area Used For: TX Instruction Stacks TX Data Blocks RCV Data Blocks RCV Look-up Tables	01A0–7FFE H

Figure 2-1 Module M429R4T2 Memory Map

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2.3 Global Registers

Reserved	0000–0001 H
Global Software Reset Register	0002 H
Global Interrupt Reset Register	0004 H
Global Interrupt Status Register	0006 H
Reserved	0008–000E H

Figure 2-2 Global Registers Memory Map

2.3.1 Global Software Reset Register **Address: 0002 (H)**

Write

The Global Software Reset register is used to reset the board. Writing a value of 1 to the appropriate bit will reset the corresponding Module. Writing a value of 0 has no effect.

Warning Reset erases all memory locations in the dual-port RAM. The Module Status, Firmware Revision, Module ID and Channel *x* Receive Look-Up Table Start Address registers are written by the board after reset operation has been completed.

Bit	Description
04-15	X - Don't Care
03	Module 3 Software Reset
02	Module 2 Software Reset
01	Module 1 Software Reset
00	Module 0 Software Reset

Global Software Reset Register

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2.3.2 Global Interrupt Reset Register — Address: 0004 (H)

Write

The Global Interrupt Reset register is used to reset the board interrupt request. Writing a value of 1 to the appropriate bit will reset the corresponding Module interrupt request. Writing a value of 0 has no effect.

Bit	Description
04-15	X - Don't Care
03	Module 3 Interrupt Reset
02	Module 2 Interrupt Reset
01	Module 1 Interrupt Reset
00	Module 0 Interrupt Reset

Global Interrupt Reset Register

2.3.3 Global Interrupt Status Register — Address: 0006 (H)

Read

The Global Interrupt Status register indicates the board pending interrupts status. A value of 1 at the appropriate bit indicates a corresponding Module active interrupt. A value of 0 indicates no interrupt has been generated.

Bit	Description
04-15	X - Don't Care
03	Module 3 Interrupt Status
02	Module 2 Interrupt Status
01	Module 1 Interrupt Status
00	Module 0 Interrupt Status

Global Interrupt Status Register

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2.4 Module Control Registers

Start Register	0010 H
Module Status Register	0012 H
Firmware Revision Register	0014 H
Channel Interrupt Register	0016 H
Receiver Data Storage Mode Register	0018 H
Interrupt Status Busy Register	001A H
Reset Time Tag Register	001C H
Module ID Register	001E H
Receiver Merge Start Pointer *	0020 H
Receiver Merge End Pointer *	0022 H
Receiver Merge Current Pointer *	0024 H
Receiver Merge Filter Table Start Address *	0026 H
Receiver Merge Word Counter *	0028 H
Receiver Merge Buffer Wraparound Register *	002A H
Receiver Merge Word Count Trigger Register *	002C H
Receiver Merge Interval Count Trigger *	002E H
Reserved	0030 H
Receiver Merge Label Trigger Register *	0032 H
Receiver Merge Configuration Register *	0034 H
Receiver Merge Interrupt Condition Register *	0036 H
Receiver Merge Status Register *	0038 H
Reserved	003A–007E H

Figure 2-3 Module Control Registers Map

Note: * For an explanation of these registers, See **Receiver Merge Mode Control Registers**, page 2-11

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2.4.1 Start/Stop Register **Address: 0010 (H)**

Read/Write The Start/Stop register starts and stops channel operation. The user can start one or more channels at the same time. Writing a 1 to bit 00 starts channel #0 operation, writing a 1 to the next location starts channel #1, etc. Writing a 0 to the bit location will stop that channel's operation. Wait a minimum of 350 µsec. between writes to the Start/Stop register.

Bit	Bit Name
06-15	0
05	Channel 5 Start Bit
04	Channel 4 Start Bit
03	Channel 3 Start Bit
02	Channel 2 Start Bit
01	Channel 1 Start Bit
00	Channel 0 Start Bit

Start/Stop Register

Note: 1. A change in a channel's Configuration register or in the Receiver Data Storage Mode register is acted upon by the firmware only after the Start/Stop register contains a 0 for at least 1 µsec.

2. When a transmit channel (channels 2 or 5) has completely finished transmitting all of its data, its start bit is automatically cleared.

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2.4.2 Module Status Register — Address: 0012 (H)

Read The Module Status register indicates the result of the self-test of the module.

Bit	Bit Name	Description
15	Internal Error	1 = Error 0 = OK
07-14	Reserved	
06	Memory	1 = OK 0 = Memory Test Fail
05	Channel 5 Status Bit	1 = Self Test OK 0 = Self Test Fail
04	Channel 4 Status Bit	1 = Self Test OK 0 = Self Test Fail
03	Channel 3 Status Bit	1 = Self Test OK 0 = Self Test Fail
02	Channel 2 Status Bit	1 = Self Test OK 0 = Self Test Fail
01	Channel 1 Status Bit	1 = Self Test OK 0 = Self Test Fail
00	Channel 0 Status Bit	1 = Self Test OK 0 = Self Test Fail

Module Status Register

Note:
1. Module status should be tested by checking all non-reserved bits for current value. For example, statreg & 0×807F == 0×007F.
2. The "Self Test Fail" is set when the channel self-test fails or when the channel is not present on the module.
3. The module will continue to operate on condition of Channel Self-Test Failures, but will not continue to operate on condition of a Memory failure.
4. The memory and channel self tests are performed once, immediately after the module is reset. On the other hand, Internal Error status is monitored continuously. If the module detects an illegal condition during normal module operation, this register will be cleared, except for the Internal Error bit, which will be set. An example of an illegal condition would be setting a pointer register to a byte boundary address (odd address).

2.4.3 Firmware Revision Register — Address: 0014 (H)

Read The Firmware Revision register indicates the revision level of the firmware. For example, 0100 (H) = Rev 1.00.

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2.4.4 Channel Interrupt Register

Address: 0016 (H)

Read/Write The Channel Interrupt register indicates which channel issued the interrupt (1 = Active). Reset the status bits by writing to this register or to the reset register.

Bit	Bit Name
06-15	Reserved
05	Channel 5 Interrupt Bit
04	Channel 4 Interrupt Bit
03	Channel 3 Interrupt Bit
02	Channel 2 Interrupt Bit
01	Channel 1 Interrupt Bit
00	Channel 0 Interrupt Bit

Channel Interrupt Register

2.4.5 Receiver Data Storage Mode Register

Address: 0018 (H)

Write The Receiver Data Storage Mode register is used to select the Receiver Data Storage Mode and the Merge Mode option. ARINC-429 data words can be stored with Time Tag and Status words appended to the data block or they can be stored without these additional words. Set bit 00 to a logic 0 to select the standard mode which appends both Time Tag and Status Words to each ARINC-429 word stored in memory. Set register bit 00 to a logic 1 to select **Data Only mode.**

Bit 01 controls the Receiver Merge Mode selection. A logic 0 selects the standard independent mode which utilizes different receive buffer areas for each receive channel. A logic 1 selects the **Merge Mode** which utilizes a single receiver buffer for all channels. Each Receive Status Word, in this case, is tagged with Channel Code information. The Merge Module Control registers are used only when the Merge Mode option is selected (See **Receiver Merge Mode Control Registers,** page 2-11).

Bit	Description
02-15	0
01	Merge Mode Option 0 = Independent Mode 1 = Merge Mode
00	Receive Data Storage Mode 0 = Standard Mode 1 = Store Only Data

Receiver Data Storage Mode Register

Note:
1. If Data Only Storage Mode is selected (bit 00 set to 1), storage will be per independent channel regardless of the state of bit 01.
2. Data Only Storage Mode is not available in Lookup Table Mode.
3. The Receiver Data Storage Mode register can only be changed when all channels are turned off (Start/Stop register = 0).
4. Merge mode merges the 4 receive channels in each bank.

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2.4.6 Interrupt Status Busy Register — Address: 001A (H)

Read The Interrupt Status Busy register indicates whether the user can access a particular channel's interrupt status register. A 1 in the appropriate bit position indicates that the channel's interrupt status register is busy and you should not access it. A 0 in the appropriate bit position indicates that the contents of interrupt status register are valid and you may access it. Bit 06 corresponds to whether the (Receiver) Merge Mode Interrupt Status register is busy.

Bit	Bit Name
07-15	Reserved
06	Merge Mode Busy Bit
05	Channel 5 Busy Bit
04	Channel 4 Busy Bit
03	Channel 3 Busy Bit
02	Channel 2 Busy Bit
01	Channel 1 Busy Bit
00	Channel 0 Busy Bit

Interrupt Status Busy Register

2.4.7 Reset Time Tag Register — Address: 001C (H)

Write Writing any non-zero value to the Reset Time Tag register resets the Time Tag to 0.

2.4.8 Module ID Register — Address: 001E (H)

Read The module will write the value E429 (H) into the Module ID register when it has finished its initialization sequence and is ready to be accessed by the Host.

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2.5 Receiver Merge Mode Control Registers

Select the Merge Mode option via bit 01 in the Receiver Data Storage Mode register (see page 2-9). This section describes the Merge Mode Control registers, which are used only when the Merge Mode option is selected.

2.5.1 Receiver Merge Start Pointer — Address: 0020 (H)

Write The Receiver Merge Start pointer sets the start address of the Receive Data buffer. The address must be on a word boundary within the Receive Data Blocks area. For example, to cause the Merge buffer to begin at byte offset 1A0 (H), write a 1A0 (H) to this register.

2.5.2 Receiver Merge End Pointer — Address: 0022 (H)

Write The Receiver Merge End pointer sets the End Address of the Receive Data buffer. The data will wrap around or stop when the buffer is full, (when the end address is reached), depending upon the contents of the Receiver Wrap Around bit Receiver Merge Configuration Register.

2.5.3 Receiver Merge Current Pointer — Address: 0024 (H)

Read The Receiver Merge Current pointer indicates the current address where the next ARINC receive word is to be placed in the Receiver buffer. This pointer value is incremented after the entire receiver block (ARINC word, time tag, and status) is written into memory.

2.5.4 Receiver Merge Filter Table Start Address — Address: 0026 (H)

Write The Receiver Merge Filter Table Start address sets the start address of the (256 x 8) Label Filter Table as described in the Sequential storage mode (see **Figure 4-5 Receive Sequential Mode Filter Table,** page 4-6). The address must be on a word boundary.

2.5.5 Receiver Merge Word Count — Address: 0028 (H)

Read/Write The Receiver Merge Word counter indicates the number of ARINC words received (0 – 65535). This register wraps around to 0 after it reaches 65535. You can reset it only when the channel is stopped.

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2.5.6 Receiver Merge Buffer Wraparound Register Address: 002A (H)

Read/Write The Receiver Merge Buffer Wraparound register contains 2 bits for synchronization with the host. If bit 14 is set to 1, the receive buffer has wrapped around once since the last time this register was cleared. If bit 15 is set to 1, there have been multiple wraparounds. Clear bit 14 each time the first word of the buffer is read. When the module wraps around it checks bit 14. If bit 14 is not set the module sets it, otherwise the module sets bit 15.

Note: Excalibur C drivers handle these bits. If you use these drivers, you don't need to deal with them.

Bit	Description
15	Multiple Wraparound - Data Lost
14	Single Wraparound
00-13	0

Receiver Merge Buffer Wraparound Register

2.5.7 Receiver Merge Word Count Trigger Register Address: 002C (H)

Write The Receiver Merge Word Count Trigger register lets the user generate an interrupt and set a flag which indicates when a specific number of words have been received (1 - 65535). To generate an interrupt, the appropriate bit in the Receiver Merge Interrupt Condition Register must also be set. (See **Receiver Merge Interrupt Condition Register,** page 2-14.)

Note: This trigger is set when the value in the Receiver Merge Word Counter matches the value set in this register.

2.5.8 Receiver Merge Interval Count Trigger Register Address: 002E (H)

Write The Receiver Merge Interval Count Trigger register (a 16-bit value) lets the user generate an interrupt and set a flag upon reception of every "n" number of words, where "n" is the value written to this register. For example, to request an interrupt after every 5 ARINC words, write 05 to this register. If you want to generate an interrupt, you must also set the appropriate bit in the Receiver Merge Interrupt Condition Register. (See **Receiver Merge Interrupt Condition Register,** page 2-14.)

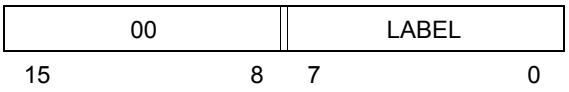
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2.5.9 Receiver Merge Label Trigger Register

Address: 0032 (H)

Write

The Receiver Merge Label Trigger register is used in conjunction with the Receiver Label Trigger bit in the Receiver Merge Configuration Register to begin the reception and storage of data upon receipt of a unique ARINC-429 label. All ARINC words received prior to the first instance of this label will not be stored by the board.



Receiver Merge Label Trigger Register

2.5.10 Receiver Merge Configuration Register

Address: 0034 (H)

Write

The Receiver Merge Configuration register sets up various run parameters for Merge Mode.

Bit	Bit Name	Description
10-15	Reserved	0
09	Enable Receive Filter Table	1 = Enable filter table. (Stores Labels per table) 0 = Disables table. Stores all Labels.
08	Reserved	0
07	Receive Label Trigger	1 = Start data storage upon receipt of Label xx. 0 = Receiver stores data without Start Label Trigger.
06	Receiver Wrap Around	1 = Data storage is halted when the buffer is full. 0 = Receiver wraps around the data in the block.
00-05	Reserved	0

Receiver Merge Configuration Register

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2.5.11 Receiver Merge Interrupt Condition Register

Address: 0036 (H)

Write

The Receiver Merge Interrupt Condition register selects which conditions will cause an interrupt to be generated. Bits 02-06 are the Interrupt Condition bits.

Bit	Description - Interrupt Conditions
07-15	0
06	Stopped on Buffer Full (see bit 06 in "Receiver Merge Configuration Register," page 2-13).
05	Error Word Received
04	Data Word Count Trigger
03	Interval Count Trigger
02	Label Received (See **Receive Sequential Mode Filter Table Diagram,** page 4-6)
00-01	Reserved

Receiver Merge Interrupt Condition Register

Note:
1. The Label Received interrupt only occurs upon reception of a label which has been marked for interrupt in the filter table.
2. To activate the Interval Count Trigger interrupt, you must also set the Receiver Merge Interval Count Trigger register (See **Receiver Merge Interval Count Trigger Register,** page 2-12).
3. In order to activate the Data Word Count Trigger interrupt, also set the Receiver Merge Word Count Trigger register (See **Receiver Merge Word Count Trigger Register,** page 2-12).

2.5.12 Receiver Merge Status Register

Address: 0038 (H)

Read/Write

The Receiver Merge Status register indicates the operational status of the Merge Mode receive buffer. Use this register to poll the status of the channel or it can be used with interrupts. When used in conjunction with interrupts, the register indicates the condition(s) which caused the interrupt. A logic 1 indicates an active bit. To reset status bits, write a 0 to this register.

Bit	Description
07-15	Reserved
06	Stopped on Buffer Full
05	Error Word Received
04	Data Word Count Trigger
03	Interval Count Trigger
02	Label Received
00-01	Reserved

Receiver Merge Status Register

Note: The Label Received Status bit is set upon receipt of any label for which an interrupt has been requested via the filter table.

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3 Transmit Mode

Chapter 3 describes transmitter operation. The following topics are covered:

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3.3.3 Interword Delay 3-7
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Perform the following procedure to implement transmit mode:

1. Create an instruction stack for the transmitter channel.
2. Write the data into the dual-port RAM.
3. Start transmission by writing to the Start register found in the Module Control Register area.

The sequence of writes to memory is not important except that writing to the Module Start Register, step 3 above, must be performed last.

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3.1 Transmit Channel Control Register Block Maps

3.1.1 Channel 2 Control Register Block Map

Channel 2 Configuration Register	00E0 H
Reserved	00E2–00FA H
Channel 2 Tx Instruction Stack Pointer	00FC H
Channel 2 Tx Instruction Counter	00FE H
Channel 2 Tx Loop Counter	0100 H
Channel 2 Tx Current Word Register	0102 H
Channel 2 Tx Current Loop Register	0104 H
Channel 2 Interrupt Condition Register	0106 H
Channel 2 Status Register	0108 H
Reserved	010A–010E H

Figure 3-1 Channel 2 Control Register Block Map

3.1.2 Channel 5 Control Register Block Map

Channel 5 Configuration Register	0170 H
Reserved	0172–018A H
Channel 5 Tx Instruction Stack Pointer	018C H
Channel 5 Tx Instruction Counter	018E H
Channel 5 Tx Loop Counter	0190 H
Channel 5 Tx Current Word Register	0192 H
Channel 5 Tx Current Loop Register	0194 H
Channel 5 Interrupt Condition Register	0196 H
Channel 5 Status Register	0198 H
Reserved	019A–019E H

Figure 3-2 Channel 5 Control Register Block Map

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3.2 Transmit Channel Control Registers

3.2.1 Channel x Configuration Register

The Channel *x* Configuration register sets up the run parameters for both the receive and transmit channels (see **Channel x Configuration Register** on page 4-14 in **Chapter 4: Receive/ Monitor Mode**). The module ignores unused bits (e.g. receiver-related bits for a transmitter channel).

Bit	Bit Name	Description
10-15	0	
09	Receiver Enable Filter Table	Not used in Transmit mode
08	0	
07	Receiver Label Trigger	Not used in Transmit mode
06	Receiver Wrap Around	Not used in Transmit mode
05	Receiver Storage Mode	Not used in Transmit mode
03-04	0	
02	Transmit Rise/Fall Time	1 = Low Speed (10 ± 5 μsec.) 0 = High Speed (1.5 ± 0.5 μsec.)
01	0	
00	Bit Rate	1 = 12.5 KHz (Lo speed) 0 = 100KHz (Hi speed)

Channel x Configuration Register – Transmit Mode

Note:
1. It is recommended that you set up **all** [active channel] Configuration Registers before programming any other parameters
2. The user can only write to this register when **all** channels are turned **off** (via the Start Register).
3. Start the module (via the Start Register) **only** after a minimum of 500 μsec from the time that the contents of this register have been modified.

3.2.2 Channel x Transmit Instruction Stack Pointer

Write

The Channel *x* Transmit Instruction Stack pointer sets the starting address of the Transmit Instruction Stack. The address must be a word boundary within the Transmit Instruction Stack area. For example, to place the Transmit Instruction stack at location 300 (H), write a 300 (H) to this register.

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3.2.3 Channel x Transmit Instruction Counter

Write The Channel *x* Transmit Instruction counter sets the number of Transmit Instruction blocks to process. These instruction blocks taken together comprise a **frame.**

3.2.4 Channel x Transmit Loop Counter

Write The Channel *x* Transmit Loop counter sets the number of times to execute the Transmit instruction blocks (the frame); *N* Times or Continuous Loop. If the continuous value is selected, the channel's operation can be terminated by setting the related channel bit in the Module Start/Stop register to a 0.

Value	
0000	= Continuous
0001	= One Time
0002	= Two Times
	•
	•
	•
FFFF	= 65535 Times

Channel x Transmit Loop Counter

3.2.5 Channel x Transmit Current Word Register

The Channel *x* Transmit Current Word register contains the number of words that have already been sent in the current loop. This allows you to determine which word is currently being sent out.

The register is updated as the last bit of the word is transmitted. After the first word in a loop goes out the register will be incremented to 1. After the final word in a loop goes out, the register will be updated to 0.

3.2.6 Channel x Transmit Current Loop Register

Read The Channel *x* Transmit Current Loop register contains the number of times the TX instruction blocks have been executed (i.e. the number of loops completed).

Note: The Transmit Current Word register is cleared before the Transmit Current Loop register is incremented.

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3.2.7 Channel x Interrupt Condition Register

Write

The Channel *x* Interrupt Condition register sets which conditions cause interrupts to be generated by the modules Bits00 and 01 are used for transmit channels and bits 02 through 06 are used for receive channels (see **Channel x Interrupt Condition Register** on page 4-17 in **Chapter 4: Receive/ Monitor Mode**).

Bit	Description - Interrupt Conditions
07-15	0
02-06	Not used in Transmit mode
01	Transmitter - End of Frame[1]
00	Transmitter - End of Block [2]

Channel x Interrupt Condition Register

1. The End of Block interrupt will occur at the completion of transmission of *each* Instruction Block.
2. The End of Frame interrupt will occur at the completion of transmission of the *final* Instruction Block (or in loop mode, at the end of each loop cycle)

3.2.8 Channel x Status Register

Read/Write

The Channel *x* Status register indicates the operational status of the channel. Use this register to poll the status of the channel or it can be used with interrupts. When used in conjunction with interrupts, the register indicates the condition(s) which caused the interrupt. A logic 1 indicates an active bit. You must reset the status bits. Only the two least significant bits are used for transmit channels and only bits 02 through 06 are used for receive channels. (See **Channel x Status Register** on page 4-18 in **Chapter 4: Receive/ Monitor Mode**).

Bit	Description - Interrupt Conditions
07-15	0
02-06	Not used in Transmit mode
01	Transmitter - End of Frame
00	Transmitter - End of Block

Channel x Status Register – Transmit Mode

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3.3 Transmit Instruction Stack

The Transmit Instruction Stack is divided into Instruction Blocks, each containing 8 words. Each Instruction Block is associated with a Data Buffer. A data buffer contains one or more ARINC-429 words that you want to transmit with the same amount of delay time between each word.

The first word in each instruction block is the Control Word which contains error injection parameters (i.e. parity type). The second word is the Word Count which instructs the module as to the number of ARINC words in a data buffer to transmit. The third word, the Interword Delay, determines the delay time between words from the same data buffer. The fourth word contains a 16-bit, user-supplied, data pointer. This Transmit Data Pointer is a 16-bit address (byte offset into the module) which points to the beginning of the data words in the memory. The remaining four words are reserved.

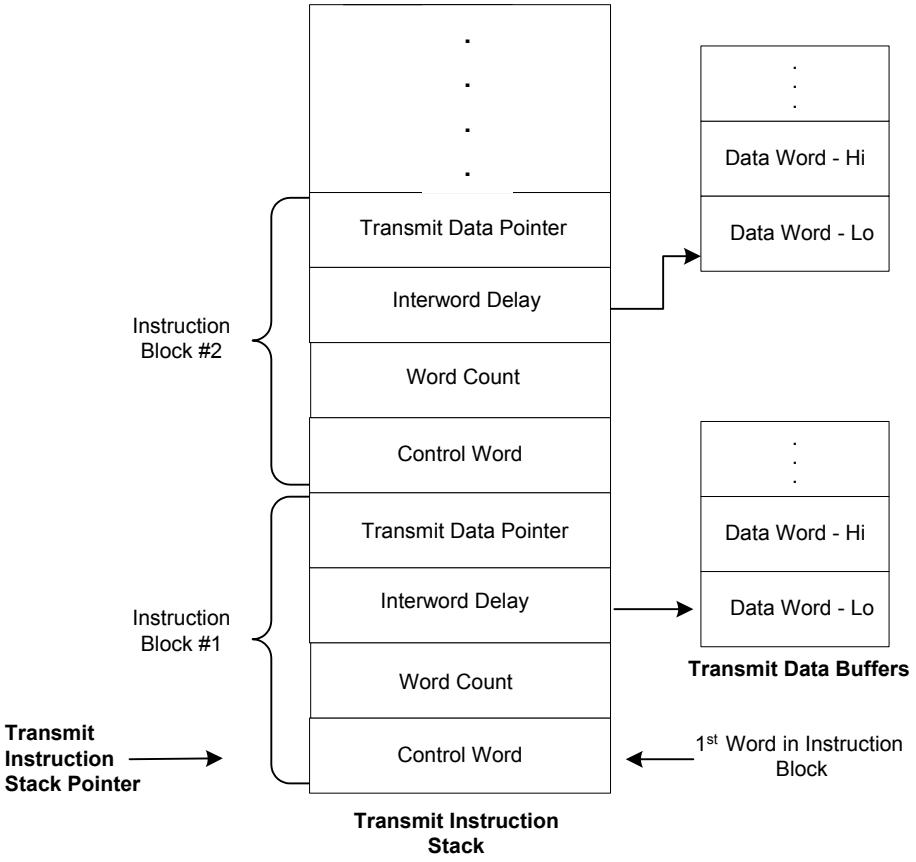


Figure 3-3 Transmit Instruction Stack Structure

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3.3.1 Control Word Definition

1st word in instruction block

Bit	Bit Name	Description
01-15	Reserved	0
00	Parity Error	0 = Normal Odd Parity (Standard ARINC-429 parity) 1 = Even Parity (Error Injection)

Control Word Definition

3.3.2 Word Count

The Word Count is used to specify the number of 32 bit ARINC-429 Data Words in this instruction block (1 – 65535).

3.3.3 Interword Delay

The Interword delay is used to set the delay (4 - 65504) between words in the block and between the final word in this block and the first word in the following block. Its resolution is 1 bit time. For high speed this gives it a range of 40 microseconds (interword value 4) to just over 655 milliseconds (interword value 65504). For low speed the range is 320 microseconds (interword value 4) to over 5 seconds (interword value 65504).

Note: The ARINC-429 specification does not allow interword times less than 4 bit times, so interword delay values of less than 4 will be interpreted as the minimum legal interword time.

3.3.4 Transmit Data Pointer

The Transmit Data Pointer register is used to set the start address of the transmit data buffer. The address must be a word boundary. The size of the buffer is determined by the Word Count value.

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3.4 Transmit Data Block Format

Figure 3-4 illustrates the format of the Transmit data words in the memory.

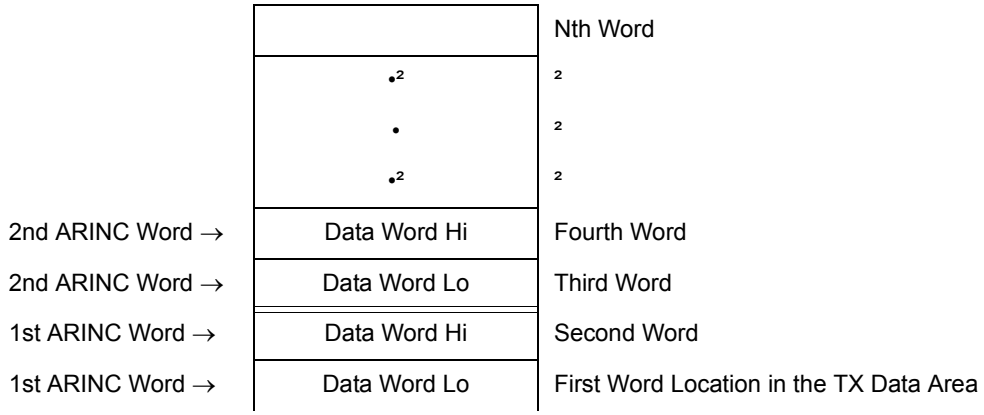


Figure 3-4 Transmit Data Words memory Format

Figure 3-5 defines the locations and bit definitions of the data bytes in the memory. The numbers shown in the four bytes represent the ARINC-429 bit locations in the 32-bit word.

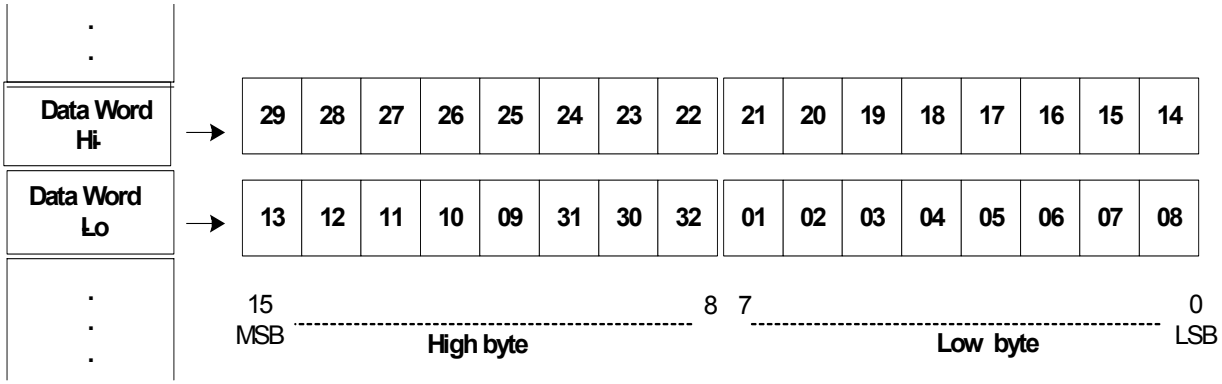


Figure 3-5 Data Bytes In Memory

Note: 1. The data in ARINC-429 bit 32 is ignored and instead a value calculated using the selected parity is transmitted over the bus.

2. The ARINC word bits are transmitted in the following order:

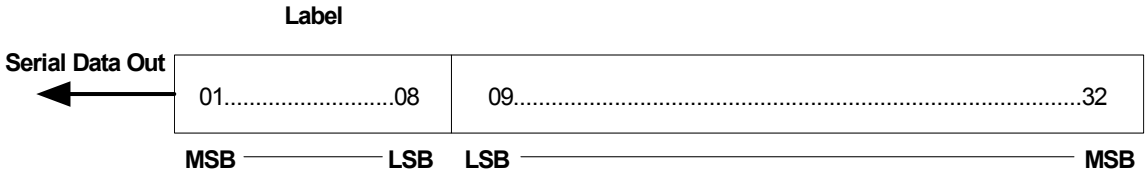


Figure 3-6 32-bit ARINC Word Bit order

3. Bits 09 through 29 are ordered from LSB to MSB (opposite from the Label field which is organized MSB to LSB). It is for this reason that the data block is built the way it is.

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4 Receive/ Monitor Mode

Chapter 4 describes receiver/monitor operation.

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4.1 General Information

The user sets up each receive channel's mode of operation by writing to various Control Registers (global and channel specific, one per channel). Each receive channel has three basic modes of operation:

Sequential Mode	Stores data in sequential locations within the receive data area
Merge Mode	Siphons all ARINC receive channels data into *one* receive buffer area
Look-Up Table Mode	Allows the user to store Words in specific locations of memory according to the Label

In all these modes, the Data Words are stored with a 16-bit Receive Status Word and a 32-bit Time Tag value. In Merge Mode, the channel code information (indicating on which channel the data was received) is contained in the Receiver Status word. Sequential mode also has a data only option which will not write the Status word and Time tag along with each Data word.

4.1.1 Sequential Mode

The Sequential Mode has a software-selectable feature that filters the storage of the specific, user-defined Labels or stores all Labels within a buffer. The data buffer's size and location within the memory is programmed via a Start and End pointer. (See Channel x Receive Data Start Pointer and Channel x Receive Data End Pointer, on page 4-15). Each received ARINC Data Word is tagged with a status Word, indicating the status of the receive Word and a 32-bit Time Tag value.

The ARINC Data Word, Time Tag and Status Word make up a single receive data block. Alternatively, Sequential Mode offers the user the capability of storing only the ARINC data without the Time Tag and Status Words. This global selection affects all receive channels. (See **Receiver Data Storage Mode Register,** page 2-9.) Interrupts and pollable status registers allow for numerous event recognition and are described in the Channel Control Register section of this manual. (See **2.4 Module Control Registers** on page 2-6 and **4.5 Receive Channel Control Registers** on page 4-14.)

4.1.2 Look-Up Table Mode

In the Look-up table mode, the word's **label** is used by the module as an offset to a 256-word Look-up table. To program the table with address pointers, indicate where to write the Receiver Data Block. Each block contains the 32-bit ARINC word, 32-bit Time Tag word, and Status word. The 256-word table can be placed anywhere in the memory via Receiver Look-up Table Pointer which the user can program.

The user can poll the operational status of each channel and generate interrupts in various circumstances. (See **Channel x Interrupt Condition Register** on page 4-17.)

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4.1.3 Merge Mode

The Merge Mode operates in the same manner as the Sequential Mode except that all the receive channels are merged into one Data Buffer area. The Control registers for the Merge Mode are located and defined in section **2.4 Module Control Registers** on page 2-6. In this mode the Receive Data Blocks are stored in sequential order and each receive Status Word is tagged with a channel code, indicating the channel on which the data was received. Each data block contains a Time tag word as in the standard Sequential Mode of operation.

4.2 Sequential/Merge Mode Operation

4.2.1 Receive Buffer Storage Sequence

The Start and End pointers set up the buffer size. The receive data storage will stop when the end pointer is reached or will wrap around to the beginning of the buffer, depending upon the condition of the Receiver Wrap Around bit in the Channel Configuration Register. The Time tag resolution is 10 μsec/bit.

Figure 4-1 illustrates how Receive Data Blocks are stored within the dual-port RAM, while in the Sequential Mode of operation.

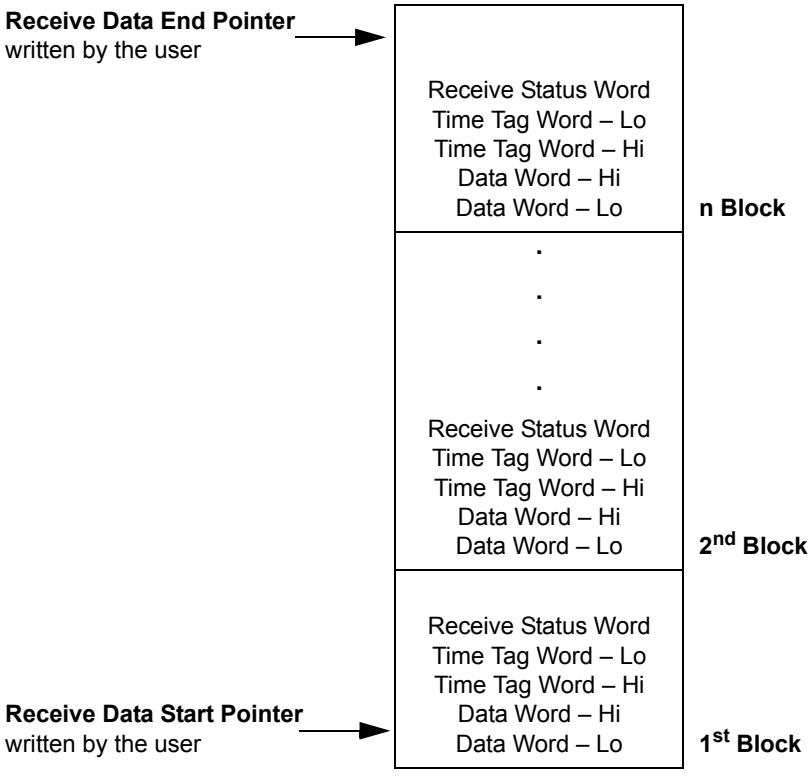


Figure 4-1 Receive Sequential Mode Buffer Structure

The contents of the Receiver Status Word are described in sections Receive Sequential Mode Status Word and Receive Merge Mode Status Word on page 4-7

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4.2.2 Receive Data Word Format

The received 32-bit ARINC-429 word is stored as two 16-bit words in the memory (Lo-Word followed by Hi-Word). The numbers shown in the two words represent the ARINC-429 bit locations in the 32-bit word.

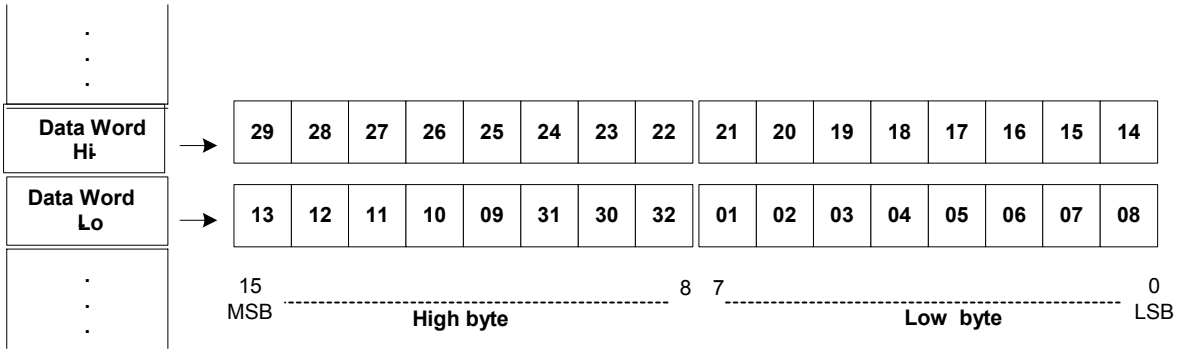


Figure 4-2 Receive Data Word Format

Note: 1. The data in ARINC-429 bit 32 is **not** a parity bit, but a parity status bit. 0 denotes odd parity received, while 1 denotes even parity received

2. The ARINC word bits are received in the following order:

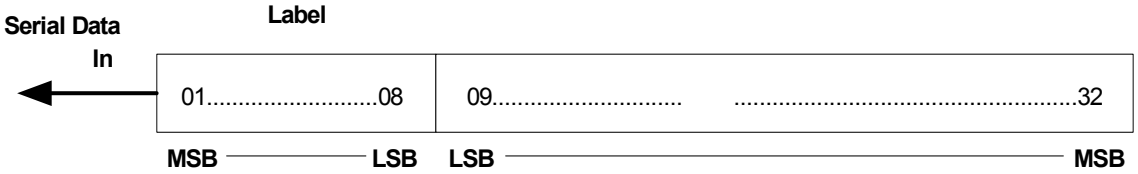


Figure 4-3 Receive Word Order

3. Bits 09 through 29 are ordered from LSB to MSB (opposite from the Label field which is organized MSB to LSB). It is for this reason that the data block is built the way it is.

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4.2.3 Time Tag Word Description

The Time Tag is a 32-bit word made up of two 16-bit words; Time Tag-Hi and Time Tag-Lo. The resolution of the Time tag is 10 µsec/bit.

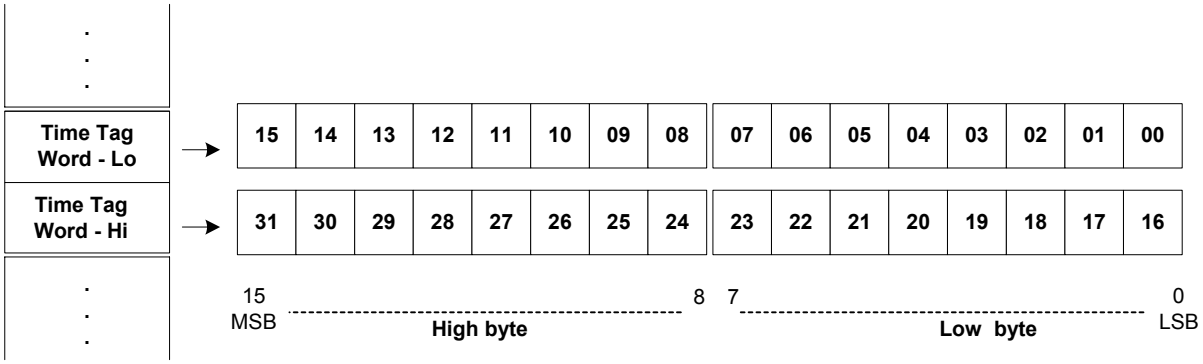


Figure 4-4 Time Tag Word Description

Note: There is a latency between the time a Word is received on the bus and the time that Word is recorded in dual-port RAM. This latency is affected by the number of channels and data rate of these channels. The Time tag reflects the time the Word is written to dual-port RAM rather than the time the Word is received over the bus. In no event shall this latency exceed a single hi-speed Word time i.e., 360 microseconds.

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4.2.4 Receive Sequential Mode Filter Table Diagram

Figure 4-5 below illustrates the structure of the Filter table.

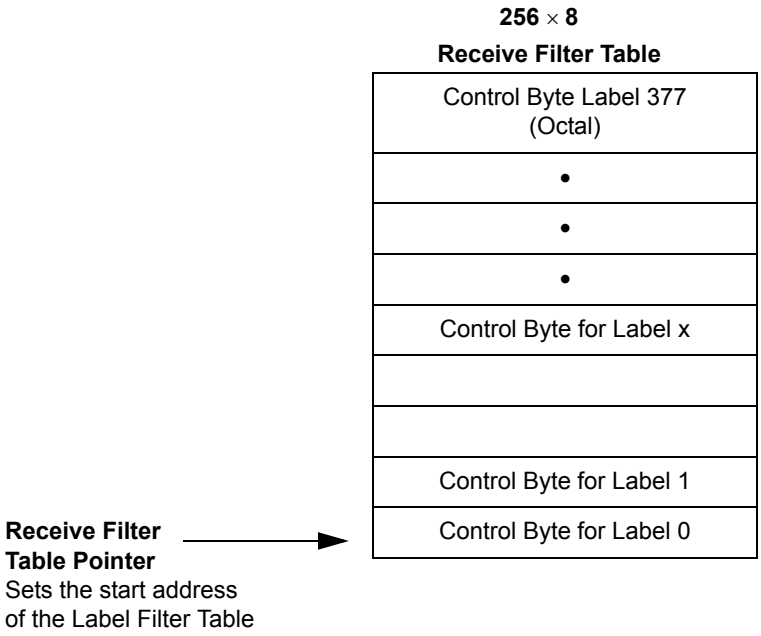


Figure 4-5 Receive Sequential Mode Filter Table

Bit	Description
02-07	Reserved
01	1 = Interrupt 0 = Don't Interrupt
00	1 = Store Word 0 = Don't Store

Label Control Byte Structure (Write)

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4.2.5 Receive Sequential Mode Status Word

Read

Bit	Bit Name	Description
08-15	**Reserved**	
07	**Valid Word**	Global Bit. Indicates that the received ARINC-429 word was valid in all respects.
04-06	**Reserved**	
03	**Parity Error**	Indicates that a parity error was detected in the ARINC-429 word.
01-02	**Reserved**	
00	**Word Received**	A logic 1. This bit is cleared while data is in the process of being updated. When the bit is set, valid data is in memory.

Receive Sequential Mode Status Word (Read)

4.2.6 Receive Merge Mode Status Word

Read

Bit	Bit Name	Description
12-15	Reserved	
08-11	Merge Channel Code	100 - Data received over channel 4 011 - Data received over channel 3 001 - Data received over channel 1 000 - Data received over channel 0
07	Valid Word	Global Bit. Indicates that the received ARINC-429 word was valid in all respects.
04-06	Reserved	
03	Parity Error	Indicates that a parity error was detected in the ARINC-429 word.
01-02	Reserved	
00	Word Received	A logic 1. This bit is cleared while data is in the process of being updated. When the bit is set, valid data is in memory.

Receive Merge Mode Status Word

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4.3 Look-up Table Mode Operation

4.3.1 Receive Look-Up Table Storage Sequence

In the Look-up table mode, the Word's **label** is used by the module as an offset to a 256-word Look-up table. You can program the table with address pointers indicating where to write the Receiver Data Block. Each block contains the 32-bit ARINC word, 32-bit Time Tag, and status word. The 256-word table can be placed anywhere in the memory via a Receiver Look-up Table Pointer that you can program.

You can poll the operational status of each channel and generate interrupts in various circumstances.

4.3.2 Receive Look-Up Table Mode Diagram

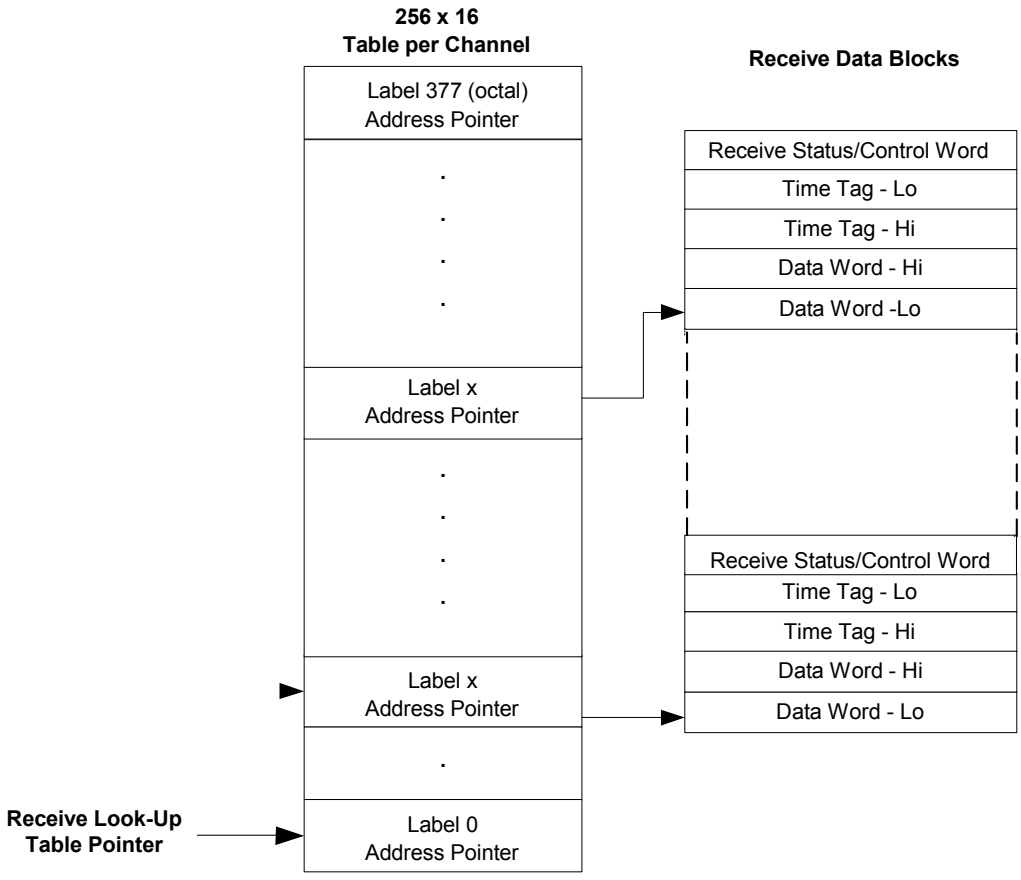


Figure 4-6 Receive Look-up Table Mode Structure

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4.3.3 Receive Look-Up Table Status/Control Word

Bit	Bit Name	Description
15	Enable Label Interrupt	Enables the “interrupt on label received” capability. This bit is used in conjunction with the interrupt Condition Register.
08-14	Reserved	
07	Valid Word	Global Bit. Indicates that the received ARINC-429 word was valid in all respects.
04-06	Reserved	
03	Parity Error	Indicates that an even parity error was detected in the ARINC-429 word.
01-02	Reserved	
00	Word Received	A logic 1. This bit is cleared while data is in the process of being updated. When the bit is set, valid data is in memory.

Receive Look-up Table Status/Control Word

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4.4 Receive Channel Control Register Block Maps

4.4.1 Channel 0 Control Register Block Map

Channel 0 Configuration Register	0080 H
Reserved	0082 H
Channel 0 RCV Data Start Pointer	0084 H
Channel 0 RCV Data End Pointer	0086 H
Channel 0 RCV Data Current Pointer	0088 H
Channel 0 RCV Look-up Table Start Address	008A H
Channel 0 RCV Filter Table Start Address	008C H
Channel 0 RCV Data Word Count Register	008E H
Channel 0 RCV Buffer Wraparound Register	0090 H
Channel 0 RCV Word Counter Trigger	0092 H
Reserved	0094 H
Channel 0 RCV Interval Counter Trigger	0096 H
Reserved	0098 H
Channel 0 RCV Label Trigger Register	009A H
Reserved	009C H
Reserved	009E H
Reserved	00A0 H
Reserved	00A2 H
Reserved	00A4 H
Channel 0 Interrupt Condition Register	00A6 H
Channel 0 Status Register	00A8 H
Reserved	00AA H
Reserved	00AC H
Reserved	00AE H

Figure 4-7 Channel 0 Control Register Block Map

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4.4.2 Channel 1 Control Register Block Map

Channel 1 Configuration Register	00B0 H
Reserved	00B2 H
Channel 1 RCV Data Start Pointer	00B4 H
Channel 1 RCV Data End Pointer	00B6 H
Channel 1 RCV Data Current Pointer	00B8 H
Channel 1 RCV Look-up Table Start Address	00BA H
Channel 1 RCV Filter Table Start Address	00BC H
Channel 1 RCV Data Word Count Register	00BE H
Channel 1 RCV Buffer Wraparound Register	00C0 H
Channel 1 RCV Word Counter Trigger	00C2 H
Reserved	00C4 H
Channel 1 RCV Interval Counter Trigger	00C6 H
Reserved	00C8 H
Channel 1 RCV Label Trigger Register	00CA H
Reserved	00CC H
Reserved	00CE H
Reserved	00D0 H
Reserved	00D2 H
Reserved	00D4 H
Channel 1 Interrupt Condition Register	00D6 H
Channel 1 Status Register	00D8 H
Reserved	00DA H
Reserved	00DC H
Reserved	00DE H

Figure 4-8 Channel 1 Control Register Block Map

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4.4.3 Channel 3 Control Register Block Map

Channel 3 Configuration Register	0110 H
Reserved	0112 H
Channel 3 RCV Data Start Pointer	0114 H
Channel 3 RCV Data End Pointer	0116 H
Channel 3 RCV Data Current Pointer	0118 H
Channel 3 RCV Look-up Table Start Address	011A H
Channel 3 RCV Filter Table Start Address	011C H
Channel 3 RCV Data Word Count Register	011E H
Channel 3 RCV Buffer Wraparound Register	0120 H
Channel 3 RCV Word Counter Trigger	0122 H
Reserved	0124 H
Channel 3 RCV Interval Counter Trigger	0126 H
Reserved	0128 H
Channel 3 RCV Label Trigger Register	012A H
Reserved	012C H
Reserved	012E H
Reserved	0130 H
Reserved	0132 H
Reserved	0134 H
Channel 3 Interrupt Condition Register	0136 H
Channel 3 Status Register	0138 H
Reserved	013A H
Reserved	013C H
Reserved	013E H

Figure 4-9 Channel 3 Control Register Block Map

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4.4.4 Channel 4 Control Register Block Map

Channel 4 Configuration Register	0140 H
Reserved	0142 H
Channel 4 RCV Data Start Pointer	0144 H
Channel 4 RCV Data End Pointer	0146 H
Channel 4 RCV Data Current Pointer	0148 H
Channel 4 RCV Look-up Table Start Address	014A H
Channel 4 RCV Filter Table Start Address	014C H
Channel 4 RCV Data Word Count Register	014E H
Channel 4 RCV Buffer Wraparound Register	0150 H
Channel 4 RCV Word Counter Trigger	0152 H
Reserved	0154 H
Channel 4 RCV Interval Counter Trigger	0156 H
Reserved	0158 H
Channel 4 RCV Label Trigger Register	015A H
Reserved	015C H
Reserved	015E H
Reserved	0160 H
Reserved	0162 H
Reserved	0164 H
Channel 4 Interrupt Condition Register	0166 H
Channel 4 Status Register	0168 H
Reserved	016A H
Reserved	016C H
Reserved	016E H

Figure 4-10 Channel 4 Control Register Block Map

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4.5 Receive Channel Control Registers

4.5.1 Channel x Configuration Register

The Channel *x* Configuration register sets up the run parameters for both the receive and transmit channels (See **Channel x Configuration Register,** page 3-3 in **Chapter 3: Transmit Mode**). Bits which are unused (e.g. transmit-related bits for a receiver channel) are ignored by the module.

Bit	Bit Name	Description
10-15	**0**	
09	**Receiver Enable Filter Table**	1 = Enable Filter Table (Stores labels per table) 0 = Disables table. Stores all labels.
08	**0**	
07	**Receiver Label Trigger**	1 = Start data storage upon receipt of Label xx. 0 = Receiver stores data without Start Label Trigger (see Note 4 below)
06	**Receiver Wrap Around**	1 = Data storage is halted when the buffer is full. 0 = Receiver wraps around the data in the block. This bit is used in the Sequential Storage Mode only (See **Sequential/Merge Mode Operation,** page 4-3).
05	**Receiver Storage Mode**	1 = Sequential Storage Mode 0 = Look-up Table Mode (See **Channel x Receive Look-up Table Start Address,** page 4-15).
03-04	**0**	
02	**Transmit Rise/ Fall Time**	Not used in Receive mode
01	**0**	
00	**Bit Rate**	1 = 12.5 KHz (Lo speed) 0 = 100 KHz (Hi speed) Available for channels 0 and 3 only (see Note 5 below).

Channel x Configuration Register – Receive Mode

Note:
1. It is recommended that you set up **all** [active channel] Configuration Registers before programming any other parameters.
2. You can only write to this register when **all** channels are turned **off** (via the Start Register).
3. You should "start" the module (via the Start Register) only after a minimum of 500 µsec from the time that the contents of this register have been modified.
4. Receiver Label Trigger (see See **Channel x Receive Label Trigger Register,** page 4-17).
5. The selected speed for channels 0 and 1 must be the same. Similarly, the selected speed for channels 3 and 4 must be the same. Therefore, bit 00 of the Channel Configuration Register is not used for channels 1 and 4.

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4.5.2 Channel x Receive Data Start Pointer — Write

The Channel *x* Receive Data Start pointer register sets the start address of the Receive Data buffer. The address must be a word boundary within the Receive Data Blocks area. For example, to cause the Receive Data buffer to begin at byte offset 1A0 (H), write a 1A0 (H) to this register. This register is used in the sequential mode of operation.

4.5.3 Channel x Receive Data End Pointer — Write

The Channel *x* Receive Data End pointer sets the End Address of the Receiver Data buffer. This is used in the sequential mode of operation. The data will wrap around or stop when the buffer is full, (when the end address is reached), depending upon the contents of the Receiver Wrap Around control bit in the Configuration Register.

4.5.4 Channel x Receive Data Current Pointer — Read

The Channel *x* Receive Data Current pointer indicates the current address where the next ARINC receive word is to be placed in the buffer. This pointer value is incremented after the entire receiver block (ARINC word, Time tag, and Status) is written into memory.

4.5.5 Channel x Receive Look-up Table Start Address — Write

Look-up Table mode

The Channel *x* Receive Look-Up Table Start address sets the start address of the [256 × 16] Receiver Look-Up Table (See **Channel x Configuration Register,** page 4-14, bit 05). This address represents the byte offset into the modules memory of the first location of the look-up table. The module will store one ARINC-429 data block for each Label received. The data block contains: 32-bit ARINC-429 word, 32-bit Time Tag, and the 16 bit Receive Status word. The 429 data block will be overwritten by the subsequent reception and storage of another ARINC-429 word with the same ARINC Label. The address must be a word boundary (See **Receive Look-up Table Mode Structure,** page 4-8).

Note: After reset, the Channel *x* Receive Look-Up Table Start Address register is loaded with a default value of 7E00 (H).

4.5.6 Channel x Receive Filter Table Start Address — Write

Sequential mode

The Channel *x* Receive Filter Table Start address sets the start address of the (256 × 8) Label Filter Table as described in section **4.2 Sequential/Merge Mode Operation** on page 4-3. The address must be a word boundary. It is valid for several channels to use the same filter table. This table is only valid if the Configuration Register Receiver Enable Filter Table bit is set. See **Channel x Configuration Register,** page 4-14, bit 09.

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4.5.7 Channel x Receive Data Word Count Register — Read/Write

Sequential Mode

The Channel *x* Receive Data Word Count register indicates the number of ARINC words received (0 – 65535). This register wraps around to 0 after it reaches 65535. You can reset it only when the channel is stopped.

4.5.8 Channel x Receive Buffer Wraparound Register — Read/Write

The Channel *x* Receive Buffer Wraparound register contains 2 bits for synchronization with the host. If bit 14 is set to 1, the receive buffer has wrapped around once since the last time this register was cleared. If bit 15 is set to 1, there have been multiple wraparounds. You are expected to clear bit 14 each time the first word of the buffer is read. When the module wraps around it checks bit 14. If bit 14 is not set, the module sets it; otherwise the module sets bit 15.

Note: Excalibur C drivers handle these bits. If you use these drivers, you don't need to deal with them.

Bit	Description
15	Multiple Wraparound - Data Lost
14	Single Wraparound
00-13	0

Channel x Receive Buffer Wraparound Register

4.5.9 Channel x Receive Data Word Counter Trigger Register — Write

Sequential Mode

The Channel *x* Receive Data Word Counter Trigger register lets you generate an interrupt and set a flag which indicates when a specific number of words have been received (1 - 65535). If you want to generate an interrupt, you must also set the appropriate bit in the Channel x Interrupt Condition Register (See **Channel x Interrupt Condition Register,** page 4-17).

Note: This trigger is set when the value in the Channel *x* Receive Data Word Counter matches the value set in this register.

4.5.10 Channel x Receive Interval Counter Trigger Register — Write

Sequential Mode

The Channel *x* Receive Interval Counter Trigger register lets you generate an interrupt and set a flag upon reception of every "n" number of words, where *n* is the value written to this register. For example, to request an interrupt after every 5 ARINC words, write 05 to this register. If you want to generate an interrupt, you must also set the appropriate bit in the Channel *x* Interrupt Condition Register (See **Channel x Interrupt Condition Register,** page 4-17).

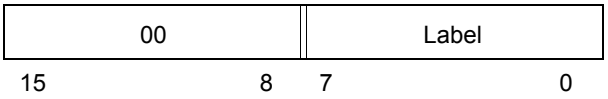
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4.5.11 Channel x Receive Label Trigger Register — Write

Sequential Mode

The Channel *x* Receive Label Trigger register is used in conjunction with the Receiver Label Trigger bit in the Channel *x* Configuration Register. (See **Channel x Configuration Register** on page 3-3 in Transmit mode and **Channel x Configuration Register** on page 4-14 in Receive/Monitor mode).

This register enables the reception and storage of data upon receipt of a unique ARINC-429 label. All ARINC words received prior to the first instance of this label will not be stored by the board.



Channel x Receive Label Trigger Register

4.5.12 Channel x Interrupt Condition Register — Write

The Channel *x* Interrupt Condition register selects which conditions will cause an interrupt to be generated. Bits 02 through 06 are used for receive channels. Bits 00 and 01 are used in Transmit mode. (See Transmit mode **Channel x Interrupt Condition Register** on page 3-5.)

Bit	Description - Interrupt Conditions
07-15	0
06	Receiver - Stopped on Buffer Full
05	Receiver - Error Word Received
04	Receiver - Data Word Count Trigger [1]
03	Receiver - Interval Count Trigger [2]
02	Receiver - Label Received [3]
01	Not used in Receiver mode
00	Not used in Receiver mode

Channel x Interrupt Condition Register – Receive Mode

1. To activate the Data Word Count Trigger interrupt, set the Channel x Receive Word Counter Trigger Register (See **Channel x Receive Data Word Counter Trigger Register,** page 4-16).
2. To activate the Interval Count Trigger interrupt, set the Channel x Receive Interval counter Trigger register. See **Channel x Receive Interval Counter Trigger Register,** page 4-16
3. The Label Received interrupt only occurs upon reception of a label which has been marked for interrupt in a Filter table or Look-up table

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4.5.13 Channel x Status Register **Read/Write**

The Channel *x* Status register indicates the operational status of the channel. Use this register to poll the status of the channel or with interrupts. When used in conjunction with interrupts, the register indicates the condition(s) which caused the interrupt. A logic 1 indicates an active bit. You must reset the status bits by writing a 0 to this register. Bits 02 through 06 are used for receive channels Bits 00 and 01 are used for transmit channels. (See Transmit mode **Channel x Status Register** on page 3-5).

Bit	Description - Interrupt Condition
07-15	0
06	Receiver - Stopped on Buffer Full
05	Receiver - Error Word Received
04	Receiver - Data Word Count Trigger
03	Receiver - Interval Count Trigger
02	Receiver - Label Received
00-01	Not used in Receive mode

Channel x Status Register – Receive Mode

In Look Up Mode, the Label Received Status bit is set upon receipt of any label for which an interrupt has been requested via the label's Control byte. In Sequential Mode, it is set upon receipt of any label for which an interrupt has been requested via the Filter table.

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5 Mechanical and Electrical Specifications

Chapter 5 describes the mechanical and electrical specifications of the *DAS-429PCI/Mx* board.

5.1 Board Layout 5-1
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5.3.2 Connector J1 Pin Assignments 5-3
5.3.3 Connector J1 Communication I/O Signals Description 5-4
5.3.4 PCI Bus Edge Connector Pinout 5-5
5.4 Power Requirements 5-6

5.1 Board Layout

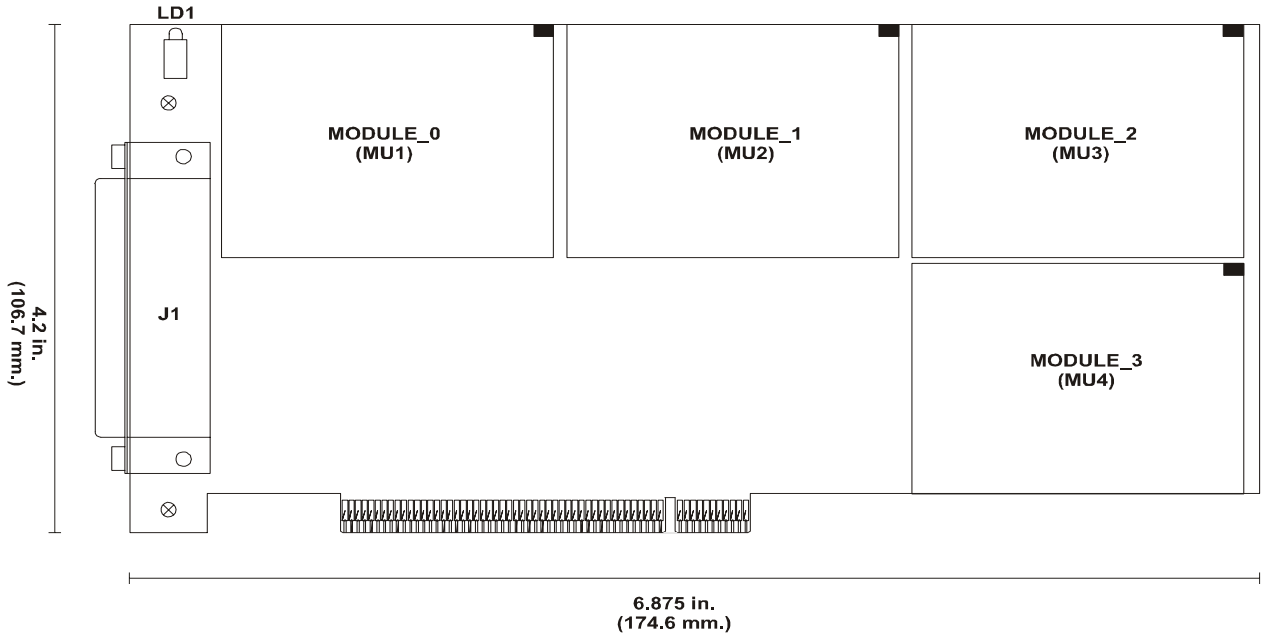


Figure 5-1 *DAS-429PCI/Mx* Board Layout

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5.2 LED Indicators

The *DAS-429PCI/Mx* board contains one LED:

LD1 **Power-up**

5.3 Connectors

The *DAS-429PCI/Mx* board contains two connectors:

- Front panel mounted female DB-62 connector (J1)
  Contains all communication I/O signals (P/N: HDL-62SLC PCB). Mating connectors (P/N: HDT 62-PD) with plastic hoods are included.
- PCI Bus Edge connector

5.3.1 Connector J1 Layout

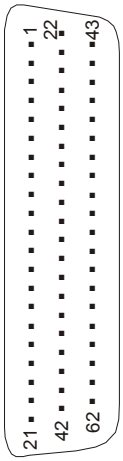


Figure 5-2 Connector J1 Layout (Front View)

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5.3.2 Connector J1 Pin Assignments

1	RXH00	**22**	RXH02	**43**	TXH00
2	RXL00	**23**	RXL02	**44**	TXL00
3	CASE	**24**	CASE	**45**	CASE
4	RXH01	**25**	RXH03	**46**	TXH01
5	RXL01	**26**	RXL03	**47**	TXL01
6	RXH10	**27**	RXH12	**48**	TXH10
7	RXL10	**28**	RXL12	**49**	TXL10
8	CASE	**29**	CASE	**50**	CASE
9	RXH11	**30**	RXH13	**51**	TXH11
10	RXL11	**31**	RXL13	**52**	TXL11
11	RXH20	**32**	RXH22	**53**	TXH20
12	RXL20	**33**	RXL22	**54**	TXL20
13	CASE	**34**	CASE	**55**	CASE
14	RXH21	**35**	RXH23	**56**	TXH21
15	RXL21	**36**	RXL23	**57**	TXL21
16	RXH30	**37**	RXH32	**58**	TXH30
17	RXL30	**38**	RXL32	**59**	TXL30
18	CASE	**39**	CASE	**60**	CASE
19	RXH31	**40**	RXH33	**61**	TXH31
20	RXL31	**41**	RXL33	**62**	TXL31
21	GND	**42**	N/C		

Table 5-1 Connector J1 Pin Assignments

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5.3.3 Connector J1 Communication I/O Signals Description

RXL00-03	Module 0 Receive channels 0,1,3,4 Lo connection
RXH00-03	Module 0 Receive channels 0,1,3,4 Hi connection
TXL00-01	Module 0 Transmit channels 2,5 Lo connection
TXH00-01	Module 0 Transmit channels 2,5 Hi connection
RXL10-13	Module 1 Receive channels 0,1,3,4 Lo connection
RXH10-13	Module 1 Receive channels 0,1,3,4 Hi connection
TXL10-11	Module 1 Transmit channels 2,5 Lo connection
TXH10-11	Module 1 Transmit channels 2,5 Hi connection
RXL20-23	Module 2 Receive channels 0,1,3,4 Lo connection
RXH20-23	Module 2 Receive channels 0,1,3,4 Hi connection
TXL20-21	Module 2 Transmit channels 2,5 Lo connection
TXH20-21	Module 2 Transmit channels 2,5 Hi connection
RXL30-33	Module 3 Receive channels 0,1,3,4 Lo connection
RXH30-33	Module 3 Receive channels 0,1,3,4 Hi connection
TXL30-31	Module 3 Transmit channels 2,5 Lo connection
TXH30-31	Module 3 Transmit channels 2,5 Hi connection
CASE	Case connection. Provided for cable shield connection. This signal is connected to the case of the computer via the board bracket.

Table 5-2 Connector J1 Communication I/O Signals Description

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5.3.4 PCI Bus Edge Connector Pinout

Pin	Pad Names	Signal Names
B1	-12V	-12V
B2	TCK	
B3	GROUND	GND
B4	TDO	
B5	+5V	VCC
B6	+5V	VCC
B7	INTB#	
B8	INTD#	
B9	PRSNT1#	
B10	RESERVED	
B11	PRSNT2#	GND
B12	GROUND	GND
B13	GROUND	GND
B14	RESERVED	
B15	GROUND	GND
B16	CLK	CLK
B17	GROUND	GND
B18	REQ#	REQn
B19	+5V (I/O)	VCC
B20	AD[31]	AD31
B21	AD[29]	AD29
B22	GROUND	GND
B23	AD[27]	AD27
B24	AD[25]	AD25
B25	+3.3V	
B26	C/BE[3]#	C_BE3n
B27	AD[23]	AD23
B28	GROUND	GND
B29	AD[21]	AD21
B30	AD[19]	AD19
B31	+3.3V	
B32	AD[17]	AD17
B33	C/BE[2]#	C_BE2n
B34	GROUND	GND
B35	IRDY#	IRDYn
B36	+3.3V	
B37	DEVSEL#	DEVSELn
B38	GROUND	GND
B39	LOCK#	LOCKn
B40	PERR#	PERRn
B41	+3.3V	
B42	SERR#	SERRn
B43	+3.3v	
B44	C/BE[1]#	C_BE1n
B45	AD[14]	AD14
B46	GROUND	GND
B47	AD[12]	AD12
B48	AD[10]	AD10
B49	GROUND	GND
B50 B51	CONNECTOR KEY	
B52	AD[08]	AD8
B53	AD[07]	AD7
B54	+3.3V	
B55	AD[05]	AD5
B56	AD[03]	AD3
B57	GROUND	GND
B58	AD[01]	AD1
B59	+5V (I/O)	VCC
B60	ACK64#	
B61	+5V	VCC
B62	+5V	VCC

Pin	Pad Names	Signal Names
A1	TRST#	
A2	+12V	+12V
A3	TMS	
A4	TDI	
A5	+5V	VCC
A6	INTA#	INTAn
A7	INTC#	
A8	+5V	VCC
A9	RESERVED	
A10	+5V	VCC
A11	RESERVED	
A12	GROUND	GND
A13	GROUND	GND
A14	RESERVED	
A15	RST#	RSTn
A16	+5V	VCC
A17	GNT#	GNTn
A18	GROUND	GND
A19	RESERVED	
A20	AD[30]	AD30
A21	+3.3V	
A22	AD[28]	AD28
A23	AD[26]	AD26
A24	GROUND	GND
A25	AD[24]	AD24
A26	IDSEL	IDSEL
A27	+3.3V	
A28	AD[22]	AD22
A29	AD[20]	AD20
A30	GROUND	GND
A31	AD[18]	AD18
A32	AD[16]	AD16
A33	+3.3V	
A34	FRAME#	FRAMEn
A35	GROUND	GND
A36	TRDY#	TRDYn
A37	GROUND	GND
A38	STOP#	STOPn
A39	+3.3V	
A40	SDONE	
A41	SBO#	
A42	GROUND	GND
A43	PAR	PAR
A44	AD[15]	AD15
A45	+3.3V	
A46	AD[13]	AD13
A47	AD[11]	AD11
A48	GROUND	GND
A49	AD[09]	AD9
A50 A51	CONNECTOR KEY	
A52	C/BE[0]#	C_BE0n
A53	+3.3V	
A54	AD[06]	AD6
A55	AD[04]	AD4
A56	GROUND	GND
A57	AD[02]	AD2
A58	AD[00]	AD0
A59	+5V	VCC
A60	REQ64#	
A61	+5V	VCC
A62	+5V	VCC

Table 5-3 PCI Bus Edge Connector Pinout

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5.4 Power Requirements

The board's maximum power supply requirements are defined below.

DAS-429PCI/Mx with no modules installed:

+5V @ 310 mA

Each installed module requires:

+5V @ 400mA
+12V @ 90mA (see Note)
-12V @ 90mA (see Note)

Note: Conditions: Both transmit channels at full speed and full load.

Example: Full (M4) board maximum power requirements will be:

+5V @ 1.8A	(0.31A + 4 x 0.4A = 1.91A)
+12V @ 0.36A	(4 x 0.09A = 0.36A)
-12V @ 0.36A	(4 x 0.09A = 0.36A)

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6 Ordering Information

Chapterr 6 explains how to indicate which options you want when ordering a *DAS-429PCI/Mx* board.

The "*x*" indicates the number of modules required (1-4).

Part Number	Description
DAS-429PCI/Mx	ARINC-429 interface board for PCI systems. Supports 4(x) Receive and 2(x) Transmit channels.
x	Number of modules required (1-4) Each module is configured as R4T2.
M429R4T2	Additional module for field upgrades (6 channels, configured as 4 Receive and 2 Transmit)

Ordering examples:

DAS-429PCI/M2	ARINC-429 interface board for PCI systems, with 2 modules. Supports 8 Receive and 4 Transmit channels.

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